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TS5N412 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER HIGH-BANDWIDTH BUS SWITCH

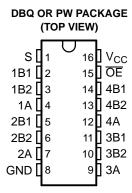
SCDS207-AUGUST 2005

FEATURES

- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range $(r_{on} = 3 \Omega \text{ Typ})$
- 0- to 10-V Switching on Data I/O Ports
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes
 Loading and Signal Distortion
 (C_{io/OFF)} = 20 pF Max, B Port)
- V_{CC} Operating Range From 4.75 V to 5.25 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications

APPLICATIONS

- PCI Interface
- Differential Signal Interface
- Memory Interleaving
- Bus Isolation
- Low-Distortion Signal Gating



DESCRIPTION/ORDERING INFORMATION

The TS5N412 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the TS5N412 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The TS5N412 is a 4-bit 1-of-2 multiplexer/demultiplexer with a single output-enable (\overline{OE}) input. The select (S) inputs control the data path of the multiplexer/demultiplexer. When \overline{OE} is low, the multiplexer/demultiplexer is enabled and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the multiplexer/demultiplexer is disabled and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T _A	PACKAGE(1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
40°C to 95°C	SSOP (QSOP) – DBQ	Tape and reel	TS5N412DBQR	VD440		
–40°C to 85°C	TSSOP - PW	Tape and reel	TS5N412PWR	YB412		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



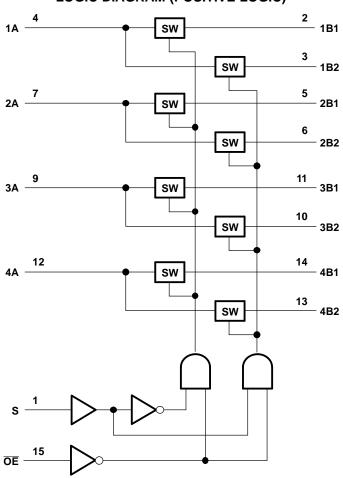
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



FUNCTION TABLE

INP	UTS	INPUT/OUTPUT	FUNCTION		
ŌĒ	S	FUNCTION			
L	L	B1	A port = B1 port		
L	Н	B2	A port = B2 port		
Н	X	Z	Disconnect		

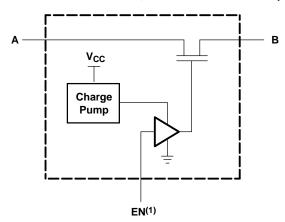
LOGIC DIAGRAM (POSITIVE LOGIC)





SCDS207-AUGUST 2005

SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V	
V_{IN}	Control input voltage range (2)(3)		-0.5	7	V
V _{I/O}	/ _{I/O} Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾				V
I _{I/O}	VO ON-state switch current ⁽⁵⁾				mA
	Continuous current through V _{CC} or GND			±100	mA
0	Darling the supply in an address (6)	DBQ package		90	0000
θ_{JA}	Package thermal impedance (6)		108	°C/W	
T _{stg}	Storage temperature range				°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with respect to ground, unless otherwise specified.
- The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- V_I and V_O are used to denote specific conditions for $V_{I/O}$. (4)
- $\rm I_{l}$ and $\rm I_{O}$ are used to denote specific conditions for $\rm I_{l/O}$. The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	٧
V_{IH}	High-level control input voltage	2	5.25	V
V_{IL}	Low-level control input voltage	0	0.8	V
V _{I/O}	Data input/output voltage	0	10	V
T _A	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

TS5N412 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER HIGH-BANDWIDTH BUS SWITCH

SCDS207-AUGUST 2005



Electrical Characteristics (1)

over recommended operating free-air temperature range, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TEST CONDITIONS MIN TYP ⁽²⁾ MAX			UNIT
I _{IN}	Control inputs	V _{CC} = 5.25 V,	$V_{IN} = 0$ to V_{CC}			10	μΑ
I _{OZ} (3)		V _{CC} = 5.25 V,	$V_O = 0 \text{ to } 10 \text{ V},$ $V_I = 0,$	Switch OFF, $V_{IN} = V_{CC}$ or GND		10	μΑ
02		V _{CC} = 0 V,	V _O = Open,	V _I = 0 to 10 V		10	
I _{CC}		V _{CC} = 5.25 V,	$I_{I/O} = 0$, Switch ON or OFF,	$V_{IN} = V_{CC}$ or GND		10	mA
C _{in}	Control inputs	V _{CC} = 5 V,	V _{IN} = 10 V or 0			10	pF
0	A port	V _{CC} = 5 V,	Switch OFF, $V_{IN} = V_{CC}$ or GND,	$V_{I/O} = 10 \text{ V or } 0$		35	~F
C _{io(OFF)}	B port	V _{CC} = 5 V,	Switch OFF, V _{IN} = V _{CC} or GND,	V _{I/O} = 10 V or 0		20	pF
C _{io(ON)}		V _{CC} = 5 V,	Switch ON, V _{IN} = V _{CC} or GND,	V _{I/O} = 10 V or 0		80	pF
			$V_1 = 0$,	I _O = 50 mA	3	7.5	
r _{on} ⁽⁴⁾		$V_{CC} = 4.75 \text{ V},$ TYP at $V_{CC} = 5 \text{ V}$	V _I = 8 V,	I _O = -50 mA		7.5	Ω
		= 0 •	$V_1 = 10 V,$	$I_O = -50 \text{ mA}$		12.5	

- V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
- For I/O ports, the parameter I_{OZ} includes the I/O leakage current.

 Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM TO $\pm 0.25 \text{ V}$ (INPUT) (OUTPUT)					
	(INFOT)	(001F01)	MIN MAX	ı		
t _{pd} ⁽¹⁾	A or B	B or A	3	ns		
t _{pd(s)}	S	A	200	ns		
	S	В	200	20		
^L en	ŌĒ	A or B	200	ns		
	S	В	200			
t _{dis}	OE	A or B	200	ns		

⁽¹⁾ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Dynamic Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 5% (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN TYP(1) MAX	UNIT
Bandwidth (BW) ⁽²⁾	$R_L = 50 \Omega$, $V_I = 0.632 V$ (P-P), See Figure 4	25	MHz
OFF isolation (O _{ISO})	$R_L = 50 \Omega$, $V_I = 0.632 V$ (P-P), $f = 25 \text{ MHz}$, See Figure 5	-50	dB
Crosstalk (X _{TALK})	$R_L = 50 \Omega$, $V_I = 0.632 \text{ V (P-P)}$, $f = 25 \text{ MHz}$, See Figure 6 and Figure 7	-50	dB

- All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C. Bandwidth is the frequency at which the gain is -3 dB below the DC gain.



TYPICAL PERFORMANCE

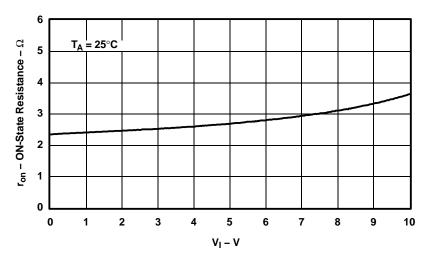


Figure 1. Typical r_{on} vs $V_{I},\,V_{CC}$ = 5 V and I_{O} = –50 mA

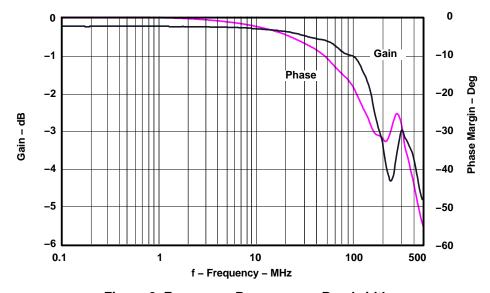


Figure 2. Frequency Response vs Bandwidth



TYPICAL PERFORMANCE

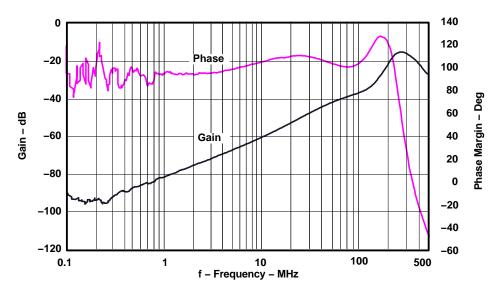


Figure 3. Frequency Response vs OFF Isolation

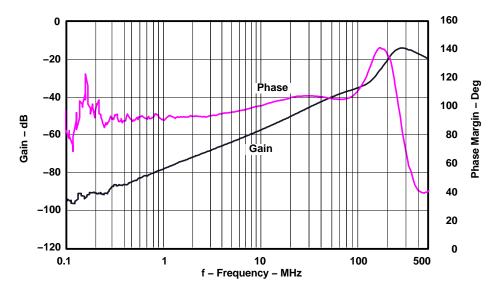
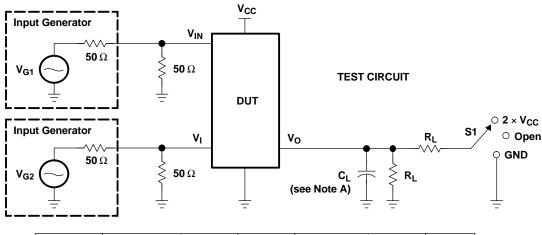


Figure 4. Frequency Response vs Crosstalk

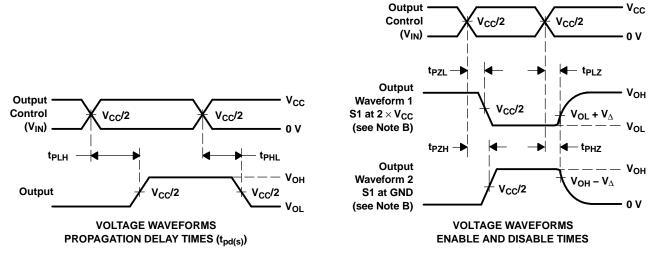


PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	VI	CL	$oldsymbol{V}_\Delta$
t _{pd(s)} †	5 V ± 0.25 V	Open	100 Ω	V _{CC}	35 pF	
t _{PLZ} /t _{PZL}	5 V ± 0.25 V	2 × V _{CC}	100 Ω	GND	35 pF	0.3 V
t _{PHZ} /t _{PZH}	5 V ± 0.25 V	GND	100 Ω	V _{CC}	35 pF	0.3 V

 $^{^{\}dagger}$ t_{pds} is measured with Demux inputs at opposite voltage levels, i.e. V_{B1} = 5 V, V_{B2} = GND.



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 25$ ns, $t_f < 25$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tpLH and tpHL are the same as tpd(s). The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Test Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION

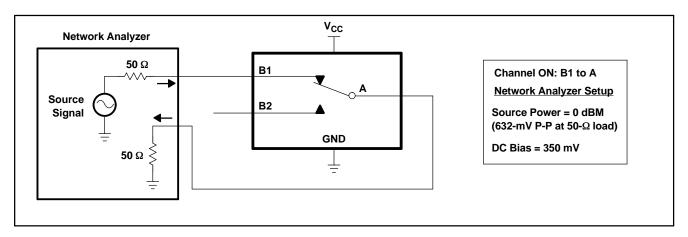


Figure 6. Bandwidth (BW)

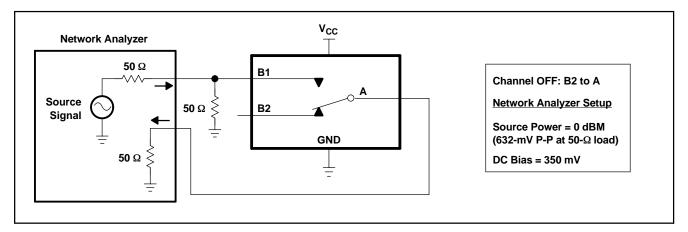


Figure 7. OFF Isolation (O_{ISO})

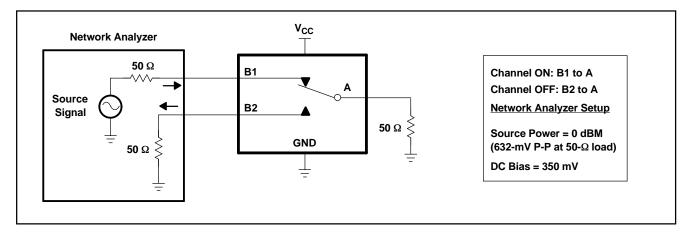


Figure 8. Crosstalk (X_{TALK})



SCDS207-AUGUST 2005

PARAMETER MEASUREMENT INFORMATION (continued)

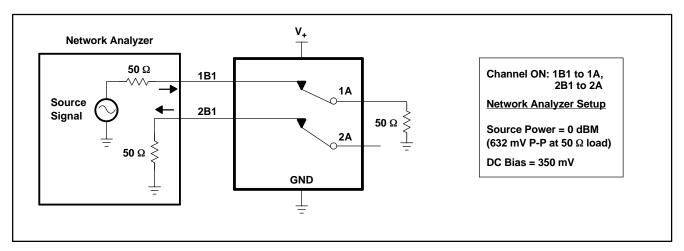
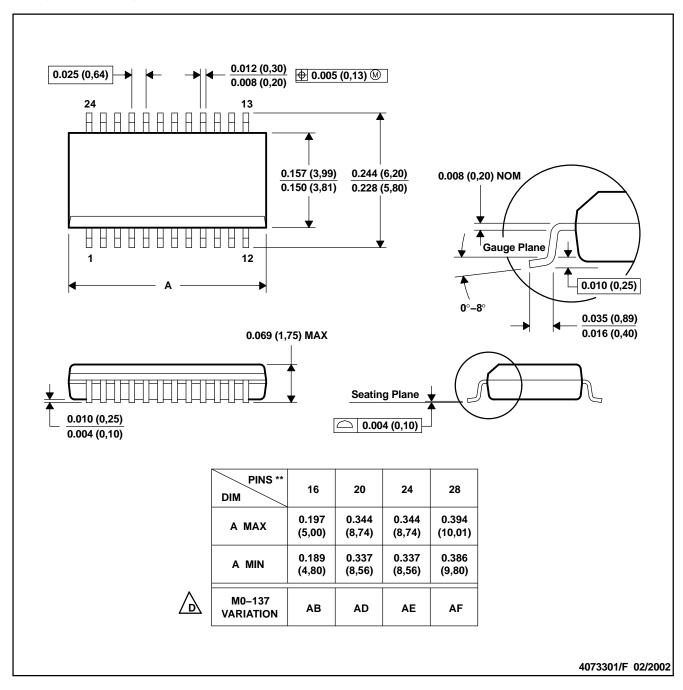


Figure 9. Adjacent Channel Crosstalk (X_{TALK})



MECHANICAL DATA

DBQ (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-137.

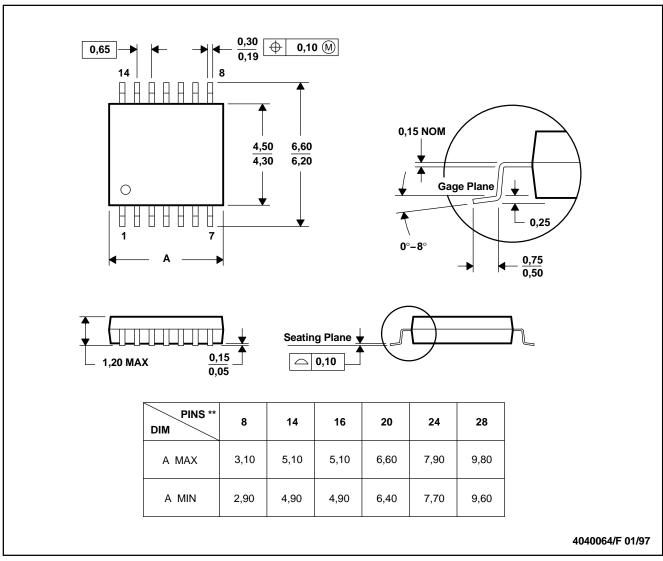
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PW (R-PDSO-G**)

14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
TS5N412DBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YB412
TS5N412DBQR.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YB412
TS5N412PW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YB412
TS5N412PW.A	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YB412

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5N412DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025



*All dimensions are nominal

Ì	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	TS5N412DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TS5N412PW	PW	TSSOP	16	90	530	10.2	3600	3.5
TS5N412PW.A	PW	TSSOP	16	90	530	10.2	3600	3.5



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SHRINK SMALL-OUTLINE PACKAGE



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- 4. This dimension does not include interlead flash.5. Reference JEDEC registration MO-137, variation AB.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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