TS5A63157 12-Ω SPDT analog switch 5-V/3.3-V single-channel 2:1 multiplexer/demultiplexer

1 Features

- Overshoot and Undershoot Voltage Protection
- Isolation in Powered-Off Mode, V_+ = 0 V
- Specified Break-Before-Make Switching
- Low ON-State Resistance (12 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

3 Description

The TS5A63157 is a single-pole, double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to V_+ (peak) can be transmitted in either direction.

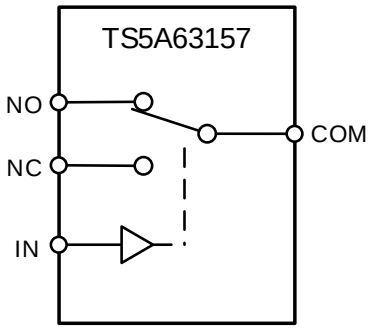
TI has integrated overshoot and undershoot protection circuitry. The TS5A63157 senses overshoot and undershoot events at the I/Os and responds by preventing voltage differentials from developing and turning the switch on.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A63157	SOT-23 (DBV)	2.90 mm x 1.60 mm
	SC-70 (DCK)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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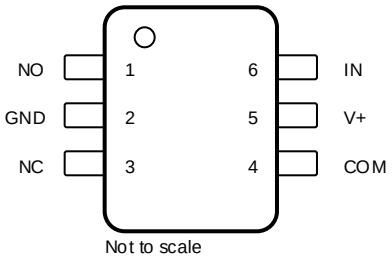
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2009) to Revision B	Page
• Added *Device Information* table, *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted the YEP or YZP package option	3
• Deleted 2 table notes from the *Absolute Minimum and Maximum Ratings* : "The input and output voltage ratings..." and "This value is limited to 5.5 V maximum."	4

5 Pin Configuration and Functions

DBV or DCK Package
SOT-23 or SC-70 (6 Pin)
Top View



Not to scale

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
NO	1	Normally open
GND	2	Digital ground
NC	3	Normally closed
COM	4	Common
V+	5	Power supply
IN	6	Digital control. Logic H = COM to NO, Logic = L COM to NC

6 Specifications

6.1 Absolute Minimum and Maximum Ratings(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	6.5	V
V_{NO} V_{NC} V_{COM}	Analog voltage range(3)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NO}, V_{NC}, V_{COM} > V_+	–50	50	mA
I_{NO} I_{NC} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–50	50	mA
V_I	Digital input voltage range(3)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+		–100	100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or V ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Supply voltage range	1.65	5.5	V
V_{NO} V_{NC} V_{COM}	Analog voltage range	0	V_+	V
V_I	Digital input voltage range	0	5.5	V

6.4 Thermal Information

THERMAL METRIC(1)		TS5A63157		UNIT
		DBV	DCK	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	209.9	298.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	147.1	103.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.8	107.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	65.3	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.5	106.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Voltage undershoot	V_{IKU}	0 ≥ (I_{NC}, I_{NO}, or I_{COM}) ≥ –50 mA			5.5 V			–2	V
Peak ON-state resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	4.5 V		4.6	11	Ω
				Full				13	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 0, I_{COM} = 30 mA	Switch ON, See Figure 13	25°C	4.5 V		4	6.5	Ω
				Full				8	
		V_{NO} or V_{NC} = 2.4 V, I_{COM} = –30 mA		25°C			4	8	
				Full				10	
		V_{NO} or V_{NC} = 4.5 V, I_{COM} = –30 mA		25°C			5.5	10	
				Full				12	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 3.15 V, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.1	0.14	Ω
				Full				0.15	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	4.5 V		1.5	2	Ω
				Full				4	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	5.5 V		0.001	0.03	µA
				Full				0.05	
	$I_{NC(PWROFF)}$, $I_{NOPWROFF)}$	V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, See Figure 14	25°C	0		0.15	1	
				Full				5	
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{COM} = 0 to 5.5 V, V_{NC} or V_{NO} = 5.5 V to 0,	Switch ON, See Figure 14	25°C	0		0.2	1	µA
				Full				10	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V		0.001	0.01	µA
				Full				0.02	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 15	25°C	5.5 V		0.003	0.03	µA
				Full				0.05	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V		0.05	0.1	µA
				Full				0.02	

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 17	25°C	5 V	2	3.4	5	ns
				Full	4.5 V to 5.5 V	2		5.5	
Turn-off time	t_{OFF}	V_{COM} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 17	25°C	5 V	1	2.8	3.4	ns
				Full	4.5 V to 5.5 V	1		3.8	
Output voltage during undershoot	V_{OUTU}	See Figure 18				2.5	V_{OH} – 0.3		V
Output voltage during overshoot	V_{OUTO}	See Figure 18					V_{OL} + 0.3	2	V
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 50 pF, See Figure 19	25°C	5 V	0.5	5	12	ns
				Full	4.5 V to 5.5 V	0.5		14	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 23	25°C	5 V		–21		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		14.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		14.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	5 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	5 V		371		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 21	25°C	5 V		–61		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 22	25°C	5 V		–61		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	5 V		0.06%		
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	μA
				Full				0.75	

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Voltage undershoot	V_{IKU}	0 ≥ (I_{NC}, I_{NO}, or I_{COM}) ≥ –50 mA			3.6 V				V
Peak ON-state resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V		6.4	14	Ω
				Full				18	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 0, I_{COM} = 24 mA	Switch ON, See Figure 13	25°C	3 V		4.8	8	Ω
				Full				10	
		V_{NO} or V_{NC} = 3 V, I_{COM} = –24 mA		25°C			6.3	12	
				Full				15	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.1 V, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V		0.1	0.2	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V		2.8	4	Ω
				Full				7	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	3.6 V		0	0.03	µA
				Full				0.05	
	$I_{NC(PWROFF)}$, $I_{NOPWROFF)}$	V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0		0.15	0.50	
				Full				2	
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NC} or V_{NO} = 3.6 V to 0,	Switch ON, See Figure 14	25°C	0		0.2	0.5	µA
				Full				5	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, SeeFigure 15	25°C	3.6 V		0.001	0.01	µA
				Full				0.02	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 15	25°C	3.6 V		0.003	0.03	µA
				Full				0.05	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V		0.005	0.01	µA
				Full				0.02	

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 17	25°C	3.3 V	2	4.3	6.6	ns
				Full	3 V to 3.6 V	2		7	
Turn-off time	t_{OFF}	V_{COM} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 17	25°C	3.3 V	1	3.3	6.3	ns
				Full	3 V to 3.6 V	1		7	
Output voltage during undershoot	V_{OUTU}	See Figure 18				2.5	V_{OH} – 0.3		V
Output voltage during overshoot	V_{OUTO}	See Figure 18					V_{OL} + 0.3	2	V
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 50 pF, See Figure 19	25°C	3.3 V	0.5	7	17	ns
				Full	3 V to 3.6 V	0.5		19.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 23	25°C	3.3 V		–11.5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		15		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		15		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	3.3 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	3.3 V		370		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 21	25°C	3.3 V		–60		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 22	25°C	3.3 V		–60		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	3.3 V		0.1%		
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.05	0.1	μA
				Full				0.6	

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Voltage undershoot	V_{IKU}	0 mA ≥ (I_{NC}, I_{NO}, or I_{COM}) ≥ –50 mA			2.7 V				V
Peak ON-state resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V		9.2	30	Ω
				Full				35	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 0, I_{COM} = 8 mA	Switch ON, See Figure 13	25°C	2.3 V		5.4	8.5	Ω
				Full				12	
		V_{NO} or V_{NC} = 2.3 V, I_{COM} = –8 mA		25°C			8.6	15.5	
				Full				25	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.6 V, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.05	0.3	Ω
				Full				0.5	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V		5	9	Ω
				Full				15	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch OFF, See Figure 14	25°C	2.7 V		0	0.03	µA
				Full				0.05	
	$I_{NC(PWROFF)}$, $I_{NOPWROFF)}$	V_{NC} or V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,	Switch OFF, See Figure 14	25°C	0		0.15	0.50	
				Full				0.75	
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{COM} = 0 to 2.7 V, V_{NC} or V_{NO} = 2.7 V to 0,	Switch ON, See Figure 14	25°C	0		0.2	0.5	µA
				Full				1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V		0.001	0.01	µA
				Full				0.02	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 15	25°C	2.7 V		0.003	0.03	µA
				Full				0.05	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.75		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.25	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V		0.005	0.01	µA
				Full				0.02	

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 17	25°C	2.5 V	3	5.8	9.6	ns
				Full	2.3 V to 2.7 V	3		12	
Turn-off time	t_{OFF}	V_{COM} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 17	25°C	2.5 V	1.5	4.5	7.3	ns
				Full	2.3 V to 2.7 V	1.5		7.5	
Output voltage during undershoot	V_{OUTU}	See Figure 18				2.5	V_{OH} – 0.3		V
Output voltage during overshoot	V_{OUTO}	See Figure 18					V_{OL} + 0.3	2	V
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 50 pF, See Figure 19	25°C	2.5 V	0.5	10	25	ns
				Full	2.3 V to 2.7 V	0.5		28.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 23	25°C	2.5 V		–8		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		15		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		15		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	2.5 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	2.5 V		367		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 21	25°C	2.5 V		–60		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, SeeFigure 22	25°C	2.5 V		–60		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	2.5 V		0.15%		
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.05	0.1	nA
				Full				0.5	

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Voltage undershoot	V_{IKU}	0 ≥ (I_{NC}, I_{NO}, or I_{COM}) ≥ –50 mA			1.95 V				V
Peak ON-state resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.65 V		13.8	60	Ω
				Full				120	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 0, I_{COM} = 4 mA	Switch ON, See Figure 13	25°C	1.65 V		5.9	15	Ω
				Full				15	
		V_{NO} or V_{NC} = 1.65 V, I_{COM} = –4 mA		25°C			12.8	40	
				Full				45	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.15 V, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.65 V		0.1	0.5	Ω
				Full				0.8	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.65 V		26.5	60	Ω
				Full				80	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch OFF, See Figure 14	25°C	1.95 V		0	0.03	µA
				Full				0.05	
	$I_{NC(PWROFF)}$, $I_{NOPWROFF)}$	V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch OFF, See Figure 14	25°C	0		0.15	0.50	
				Full				0.75	
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{COM} = 0 to 1.95 V, V_{NC} or V_{NO} = 1.95 V to 0,	Switch ON, See Figure 14	25°C	0		0.2	0.5	µA
				Full				1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V		0.001	0.01	µA
				Full				0.02	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 15	25°C	1.95 V		0.003	0.03	µA
				Full				0.05	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.75		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.25	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V		0.005	0.01	µA
				Full				0.02	

Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 17	25°C	1.8 V		9.5	23	ns
				Full	1.65 V to 1.95 V			24	
Turn-off time	t_{OFF}	V_{COM} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 17	25°C	1.8 V		5.9	10	ns
				Full	1.65 V to 1.95 V			12	
Output voltage during undershoot	V_{OUTU}	See Figure 18				2.5	V_{OH} – 0.3		V
Output voltage during overshoot	V_{OUTO}	See Figure 18					V_{OL} + 0.3	2	V
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 50 pF, See Figure 19	25°C	1.8 V	0.5	18	50	ns
				Full	1.65 V to 1.95 V	0.5		55	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 23	25°C	1.8 V		–5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		5.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		15.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		15.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	1.8 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	1.8 V		369		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 21	25°C	1.8 V		–60		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 22	25°C	1.8 V		–60		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	1.8 V		0.4%		
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.05	0.06	μA
				Full				0.3	

6.9 Typical Characteristics

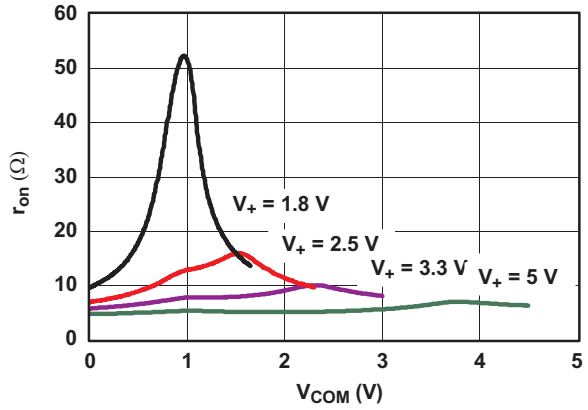


Figure 1. r_{on} vs V_{COM}

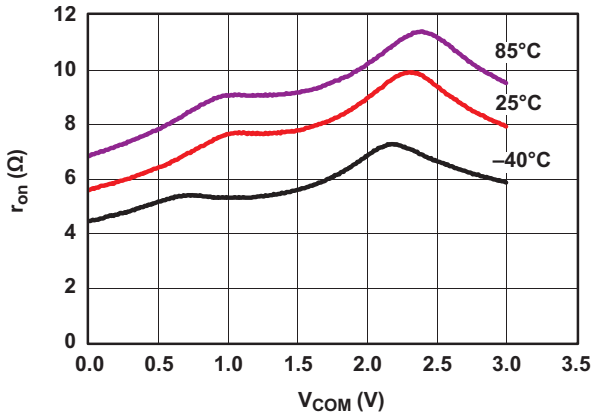


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

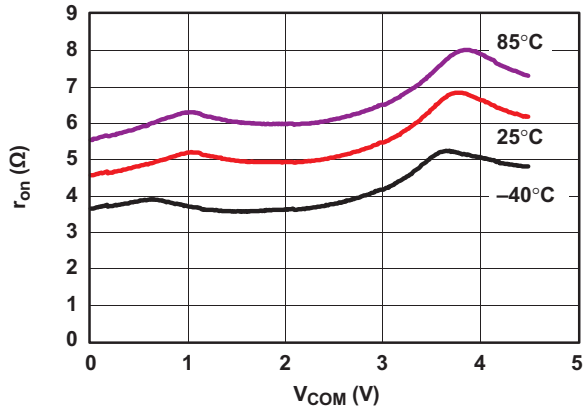


Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)

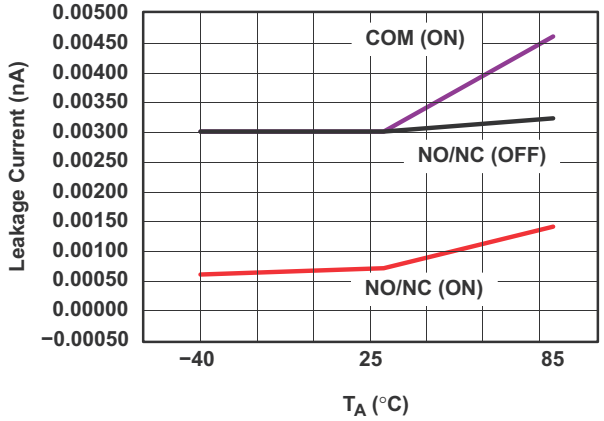


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

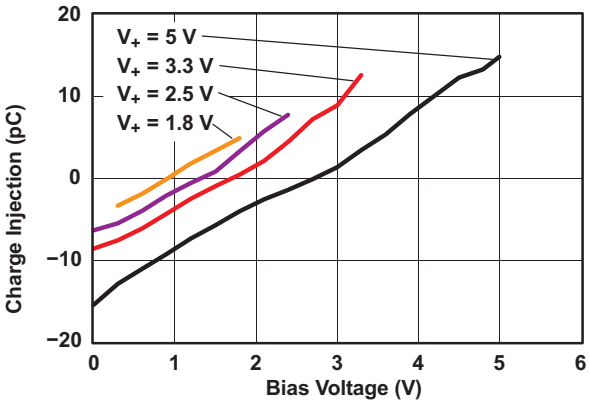


Figure 5. Charge Injection (Q_C) vs V_{COM}

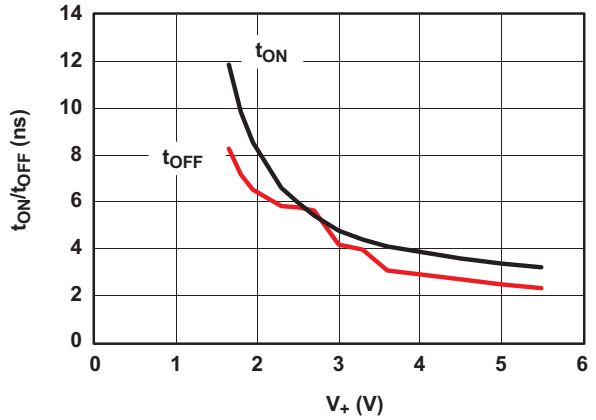


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

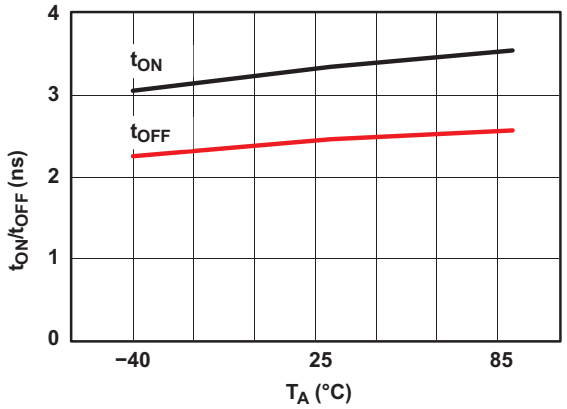


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

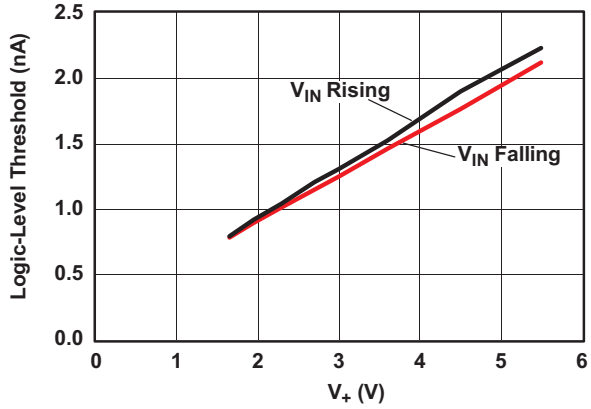


Figure 8. Logic-Level Threshold vs V_+

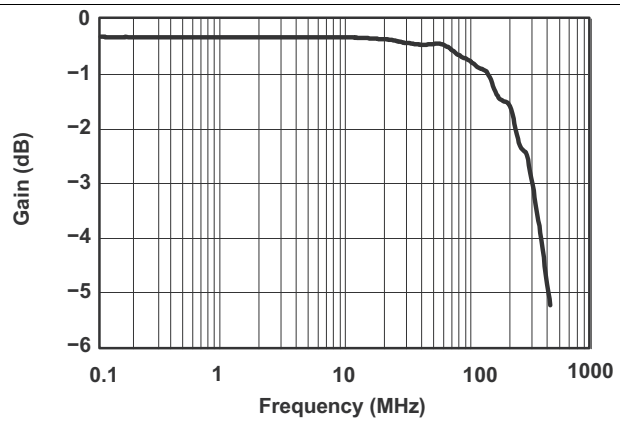


Figure 9. Bandwidth (V_+ = 3.3 V)

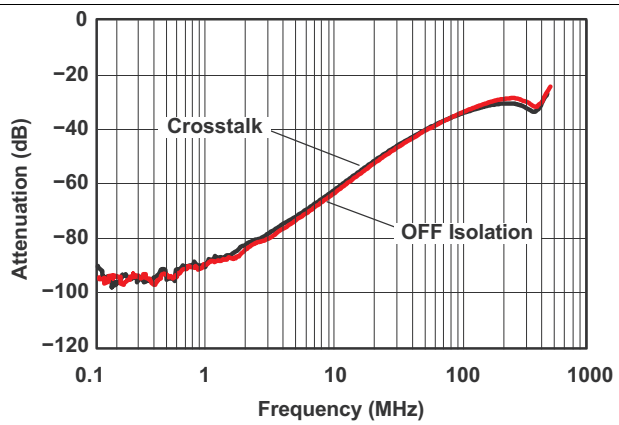


Figure 10. OFF Isolation and Crosstalk (V_+ = 3.3 V)

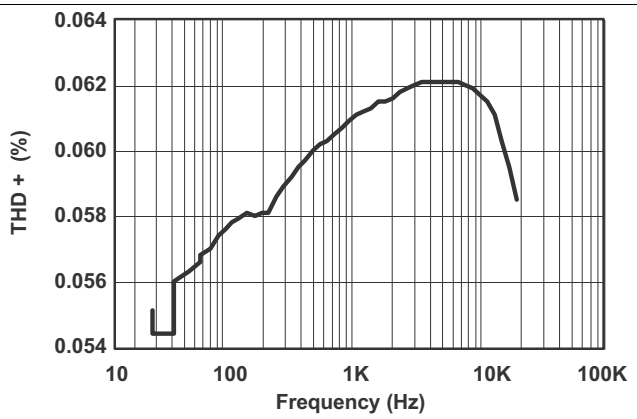


Figure 11. Total Harmonic Distortion (THD) vs Frequency (V_+ = 3.3 V)

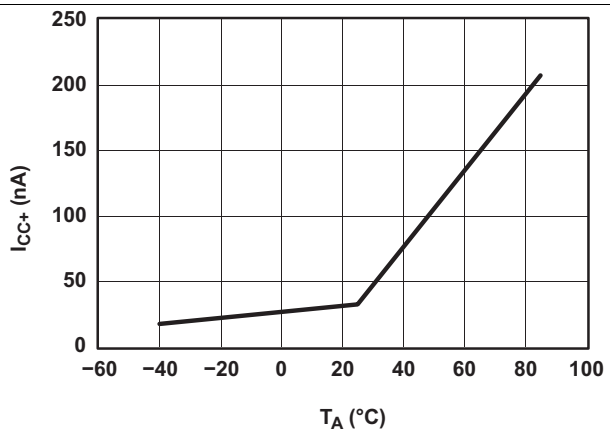


Figure 12. Power-Supply Current vs Temperature (V_+ = 5 V)

7 Parameter Measurement Information

Table 1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_+ = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input.Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
V_{OUTU}	Output voltage during an undershoot event. This is measured by turning off a specific channel and applying an undershoot voltage at the input of the switch.
V_{OUTO}	Output voltage during an overshoot event. This is measured by turning off a specific channel and applying an overshoot voltage at the input of the switch.

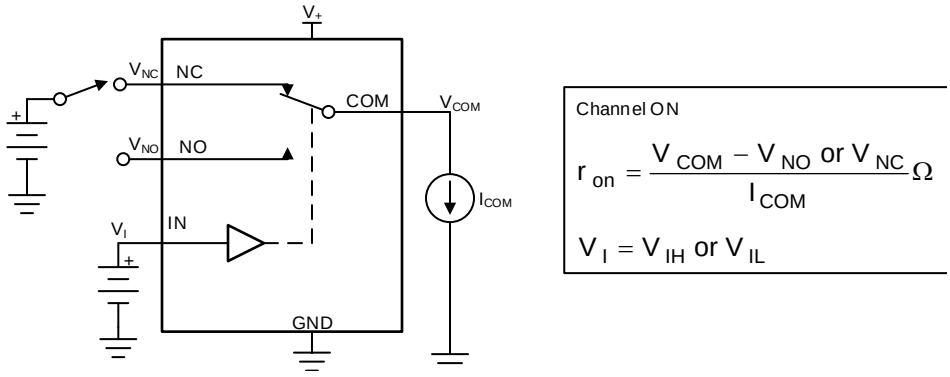


Figure 13. ON-State Resistance (r_{on})

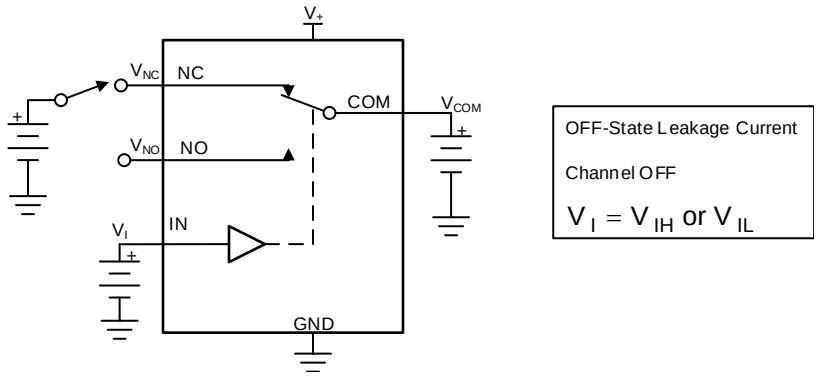


Figure 14. OFF-State Leakage Current
($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

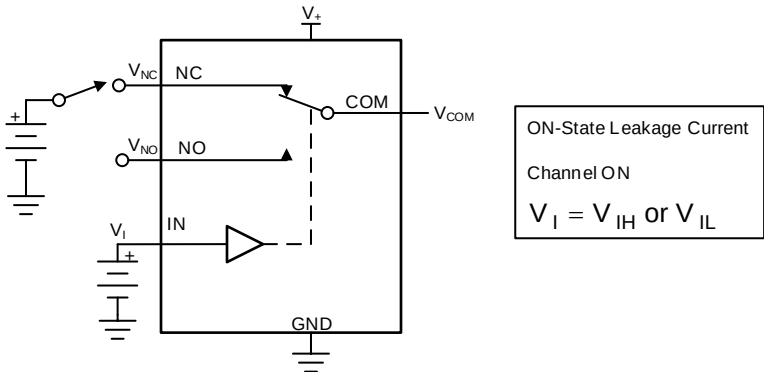


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

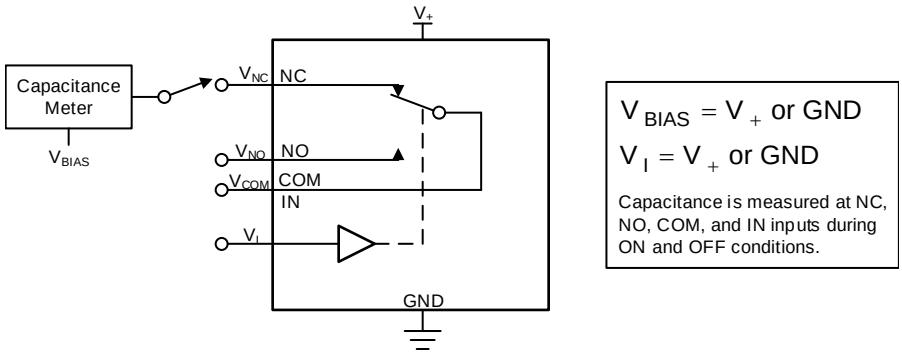
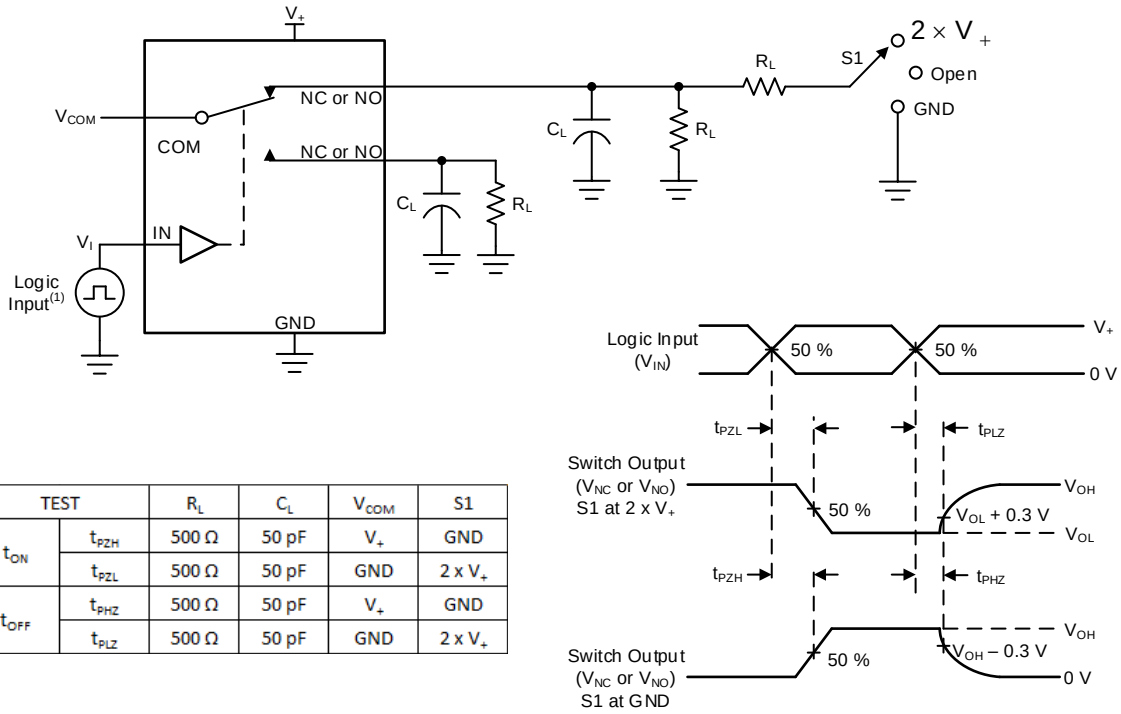


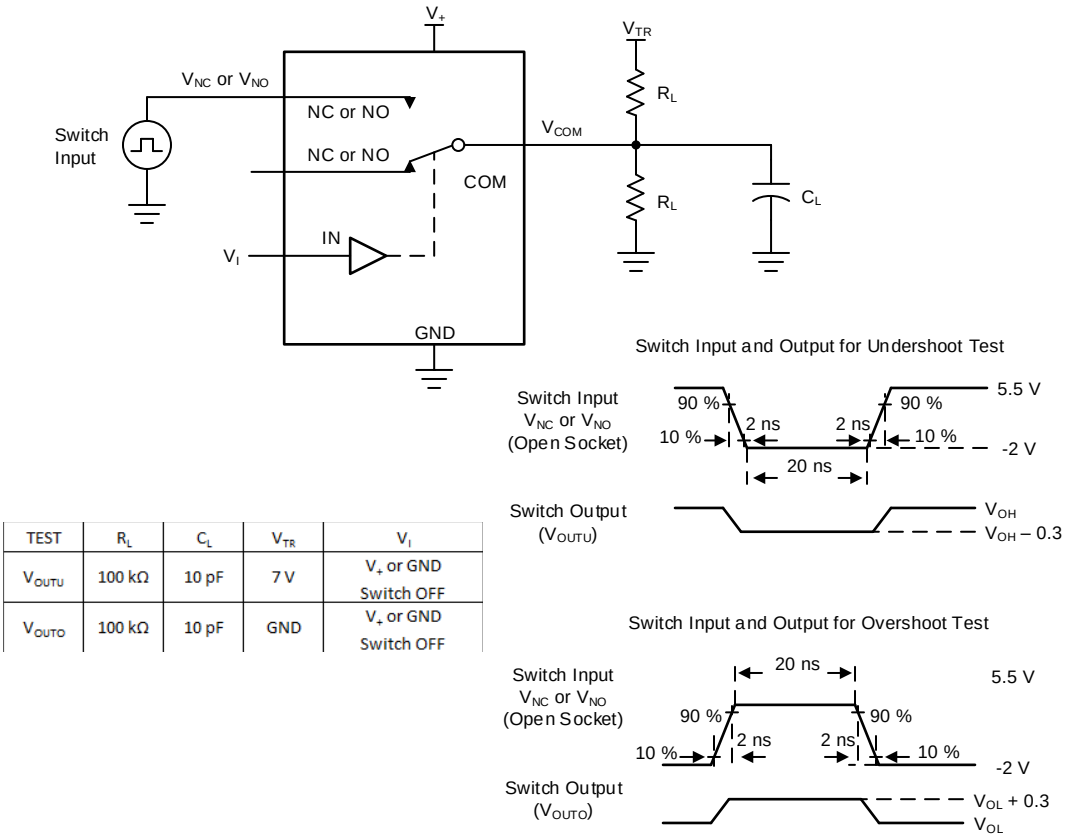
Figure 16. Capacitance (C_{IN}, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



TEST		R_L	C_L	V_{COM}	S1
t_{ON}	t_{PZH}	500 Ω	50 pF	V_+	GND
	t_{PZL}	500 Ω	50 pF	GND	2 x V_+
t_{OFF}	t_{PHZ}	500 Ω	50 pF	V_+	GND
	t_{PLZ}	500 Ω	50 pF	GND	2 x V_+

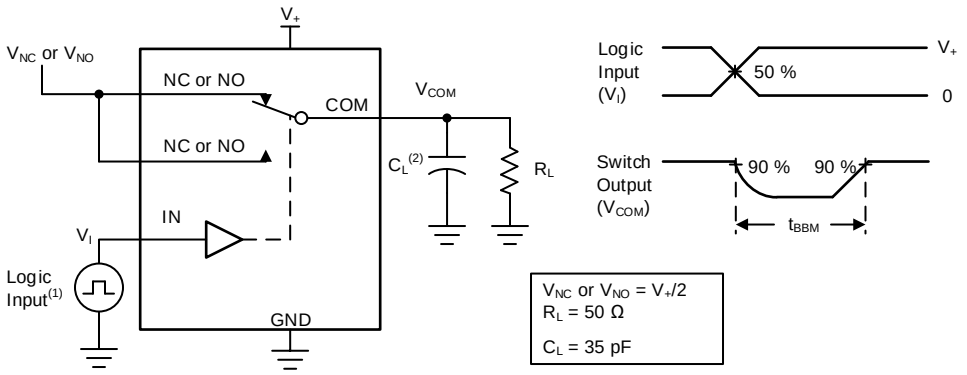
(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 17. Turn-On (t_{ON}) and Turn-Off (t_{OFF}) Time



TEST	R_L	C_L	V_{TR}	V_I
V_{OUTU}	100 kΩ	10 pF	7 V	V_+ or GND Switch OFF
V_{OUTO}	100 kΩ	10 pF	GND	V_+ or GND Switch OFF

Figure 18. Undershoot and Overshoot Test



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 19. Break-Before-Make (t_{BBM}) Time

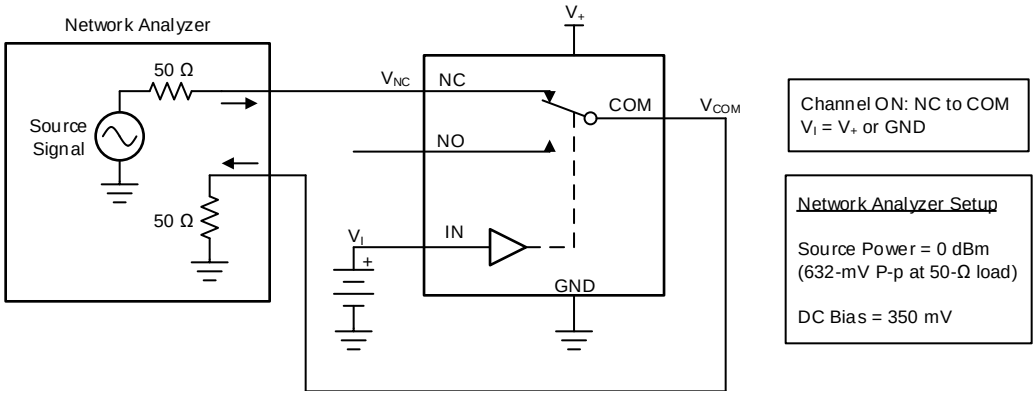


Figure 20. Bandwidth (BW)

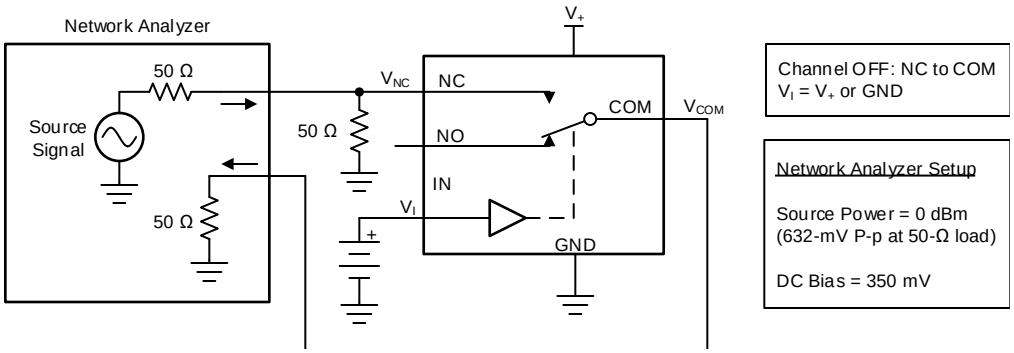


Figure 21. OFF Isolation (O_{ISO})

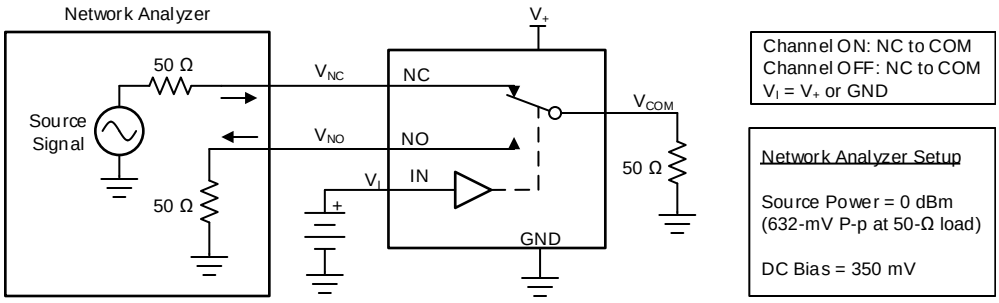
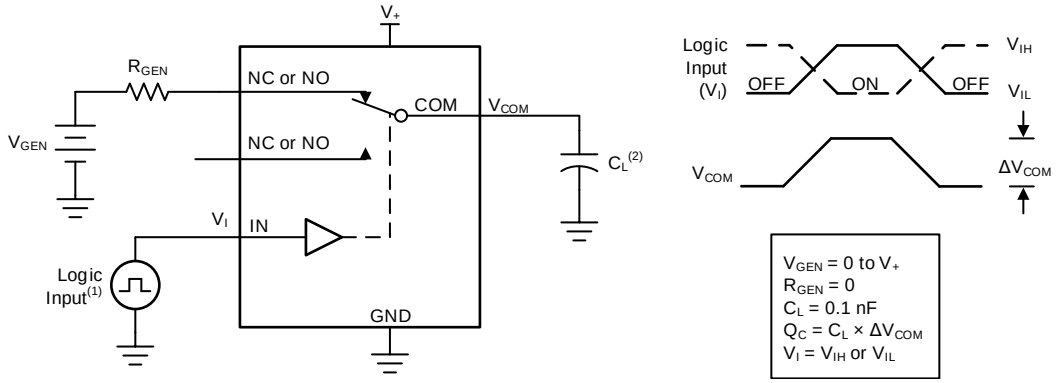


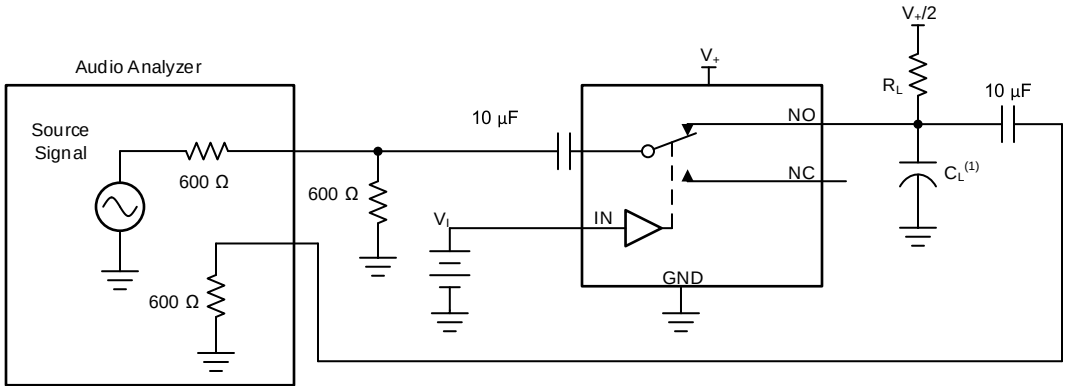
Figure 22. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 23. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

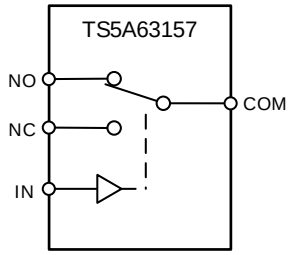
Figure 24. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A63157 is a single-pole, double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to V_+ (peak) can be transmitted in either direction.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Integrated Overshoot and Undershoot Protection Circuitry

The TS5A63157 senses overshoot and undershoot events at the I/Os and responds by preventing voltage differentials from developing and turning the switch on.

8.3.2 Isolation in Powered-Off Mode, V+ = 0 V

The TS5A63157 provides isolation when the supply voltage is removed (V+ = 0 V). When the TMUX1511 is powered-off, the I/Os of the device remain in a high-Z state. Powered-off protection minimizes system complexity by removing the need for power supply sequencing on the signal path.

8.3.3 Break-before-make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the break and the make is known as break-before-make delay.

8.4 Device Functional Modes

Table 2. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A63157 can be used in a variety of customer systems. The TS5A63157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

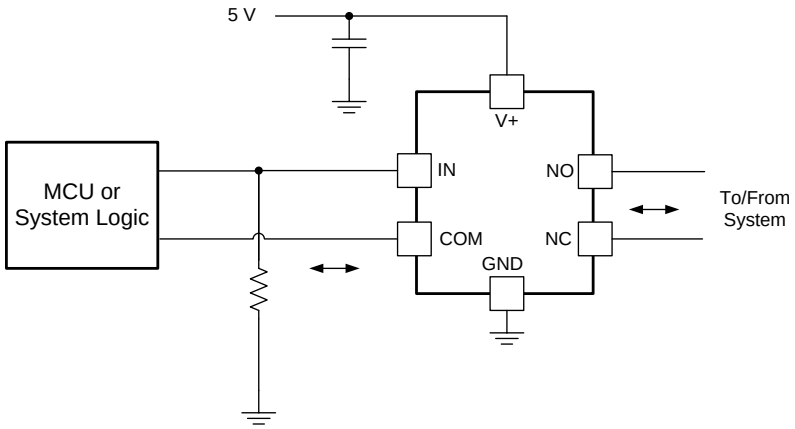


Figure 25. System Schematic for TS5A63157

9.2.1 Design Requirements

In this particular application, V_+ was 1.8 V, although V_+ is allowed to be any voltage specified in . A decoupling capacitor is recommended on the V+ pin. See for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

9.2.3 Application Curve

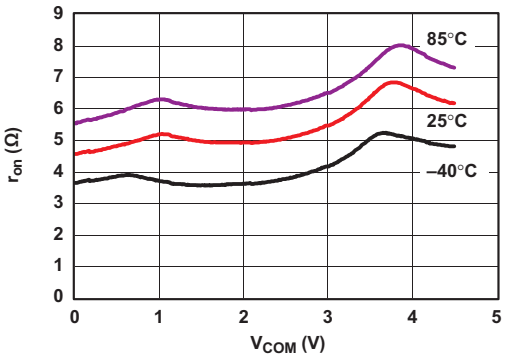


Figure 26. r_{on} vs V_{COM}, V_+ = 5 V

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the .

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

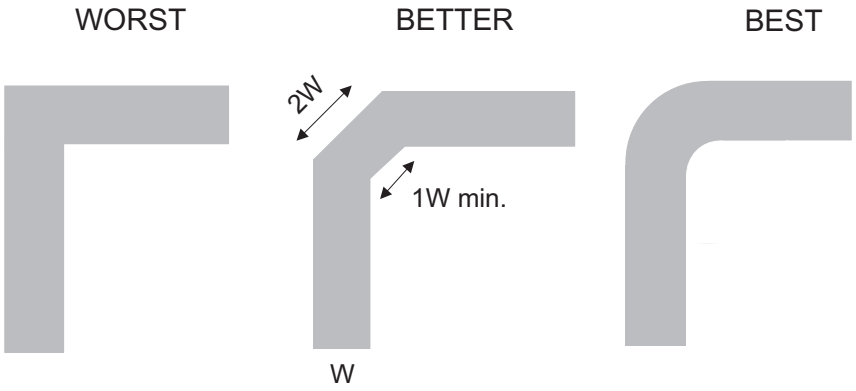


Figure 27. Trace Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A63157DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JBEF, JBER)
TS5A63157DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JBEF, JBER)
TS5A63157DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBEF
TS5A63157DBVRG4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBEF
TS5A63157DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	(J75, J7F, J7R)
TS5A63157DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(J75, J7F, J7R)
TS5A63157DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	J7F
TS5A63157DCKRG4.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	J7F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

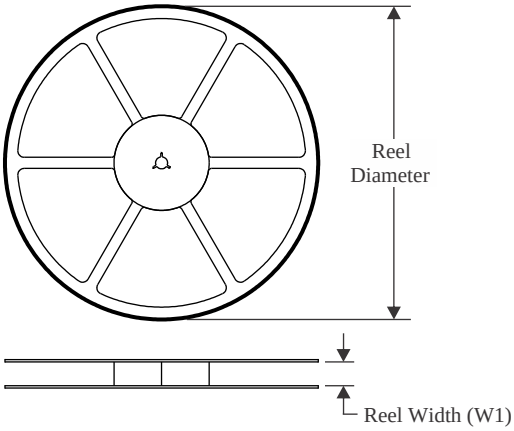
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

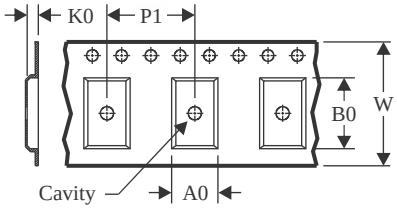
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

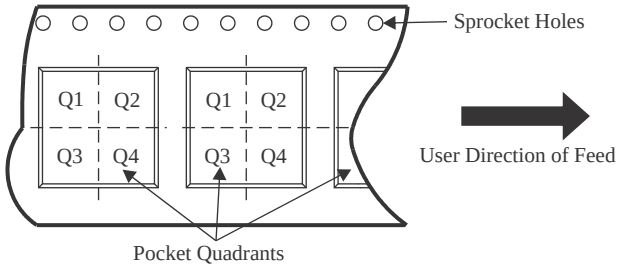


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

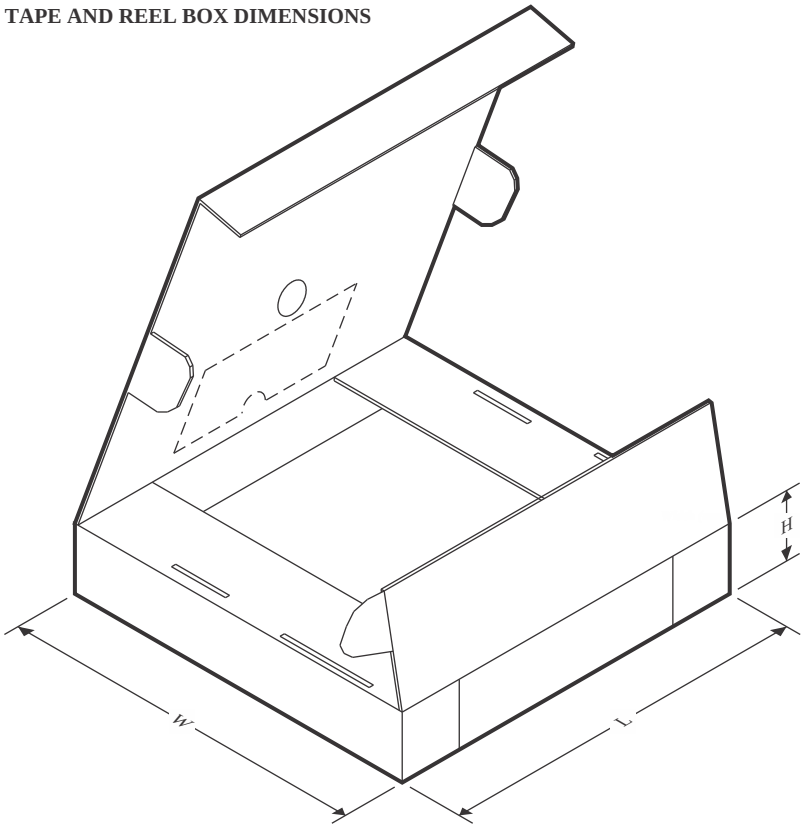
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A63157DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A63157DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A63157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A63157DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

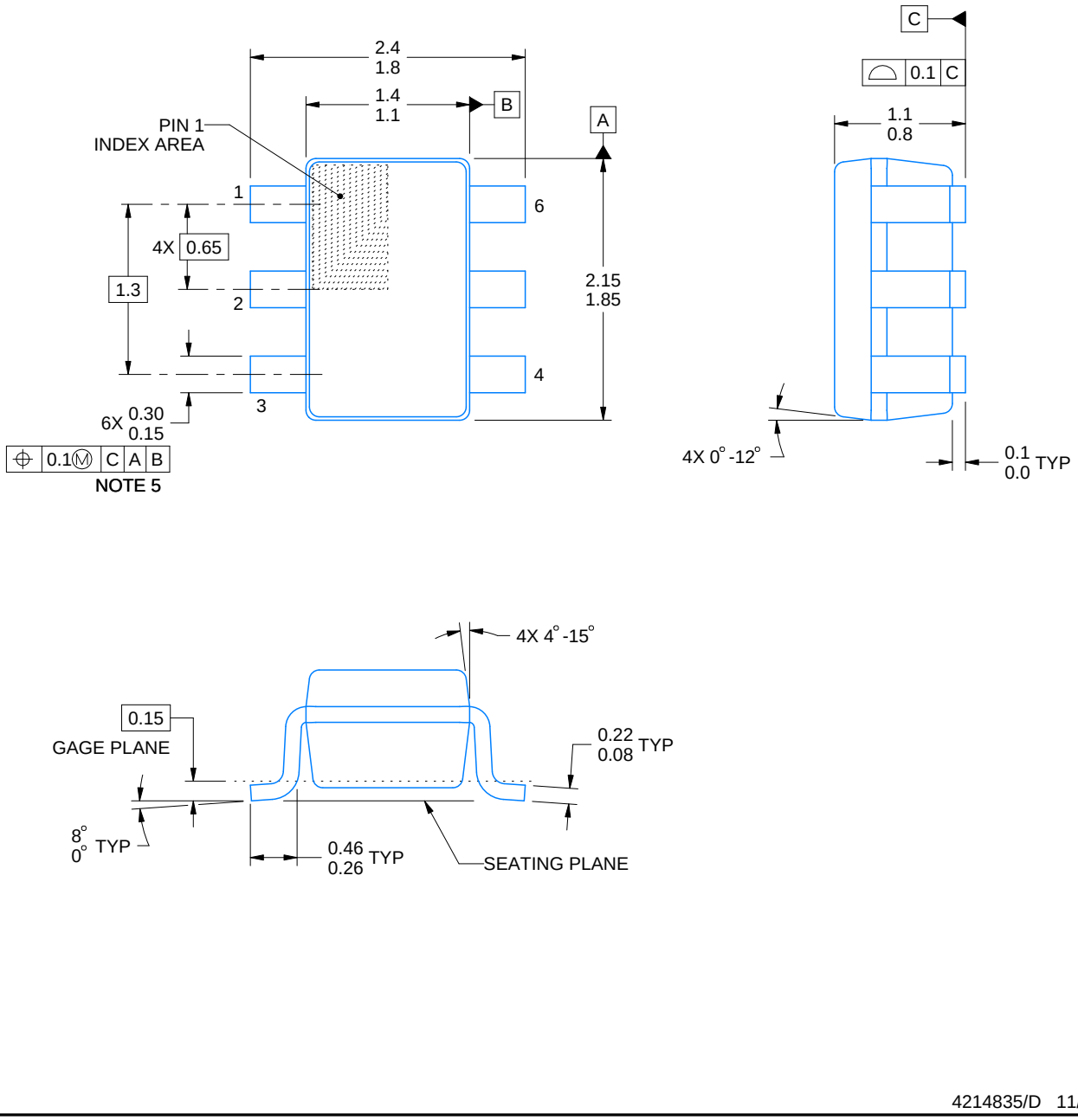
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A63157DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TS5A63157DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
TS5A63157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TS5A63157DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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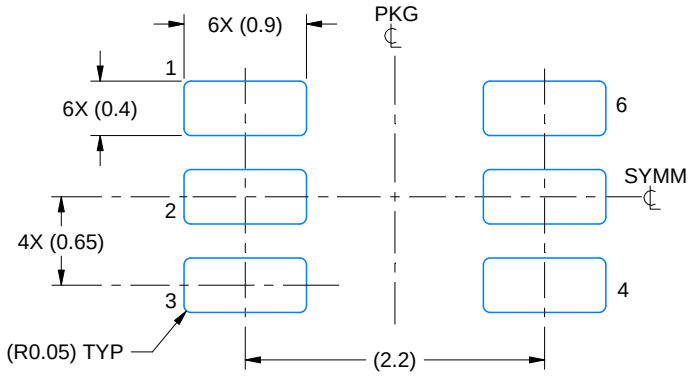
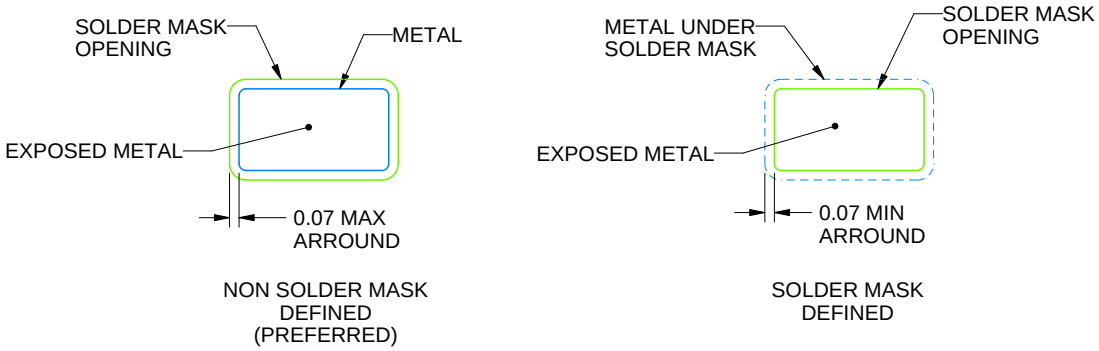
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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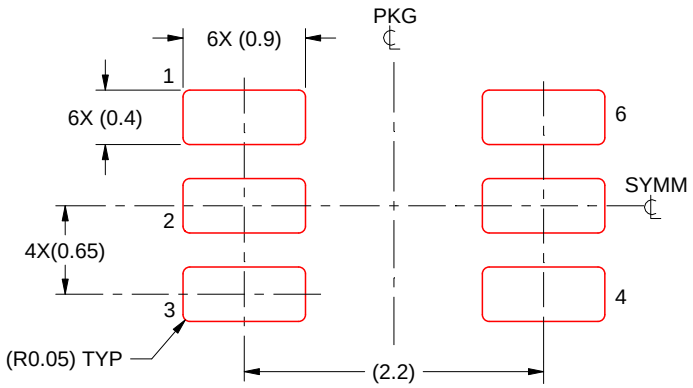
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

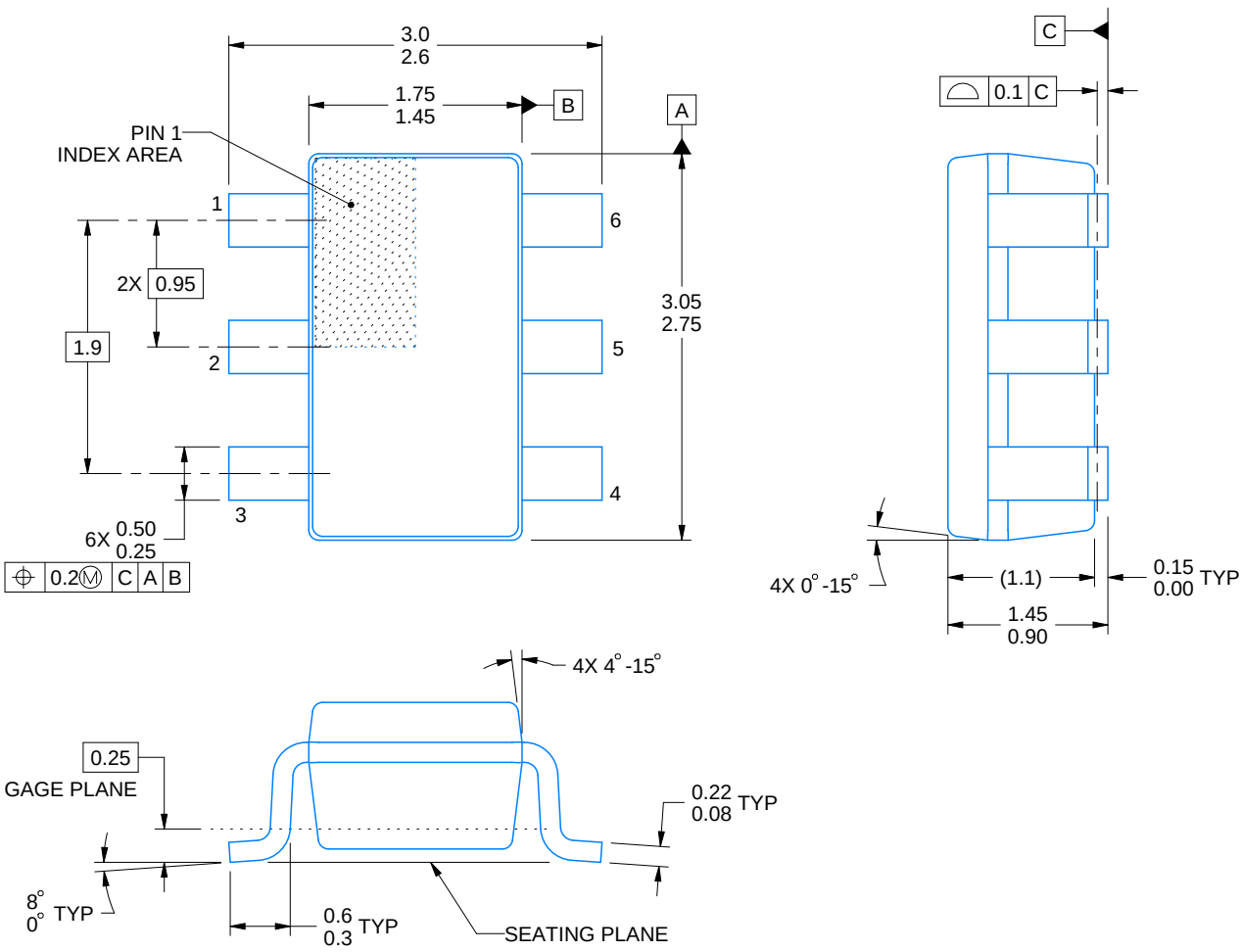
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

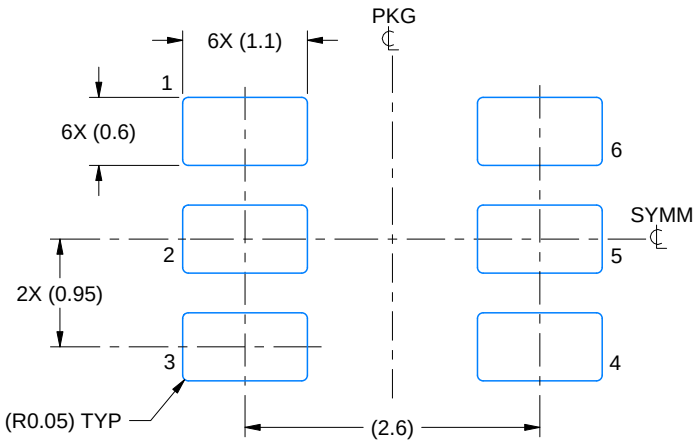
SMALL OUTLINE TRANSISTOR



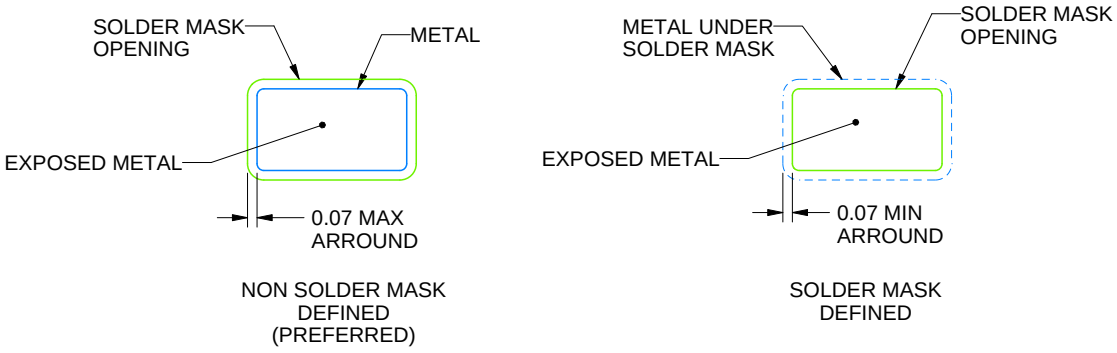
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

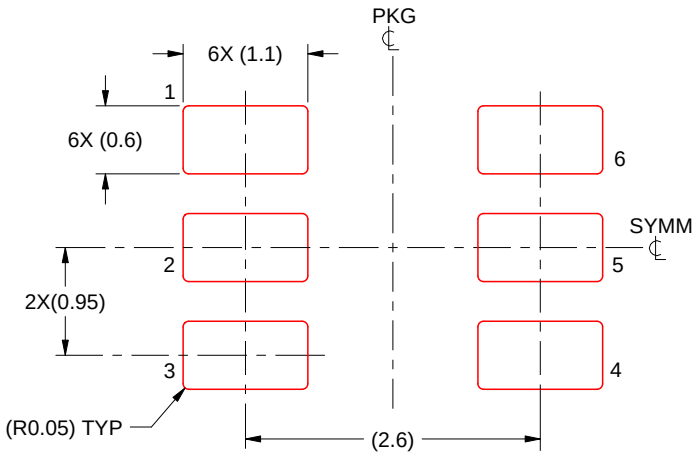


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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