

## TS5A22364-Q1 0.65-Ω Dual SPDT Analog Switch with Negative Signaling Capability

### 1 Features

- Qualified for automotive applications
- Specified Break-Before-Make (BBM) switching
- Negative signal swing capability: Maximum swing From  $-2.75\text{ V}$  to  $2.75\text{ V}$  ( $V_{CC} = 2.75\text{ V}$ )
- Internal shunt switch prevents audible click-and-pop when switching between two sources
- Low On-state resistance ( $0.65\ \Omega$  typical)
- Low charge injection
- Excellent channel to channel On-state resistance matching
- 2.3-V to 5.5-V power supply ( $V_{CC}$ )
- Latch-up performance meets 100 mA per AEC Q100-004
- ESD performance
  - 2500-V Human-Body Model tested per AEC Q100-002
  - 1500-V Charged-Device Model tested per AEC Q100-011

### 2 Applications

- Automotive infotainment
- Audio routing
- Industrial automation
- Medical imaging

### 3 Description

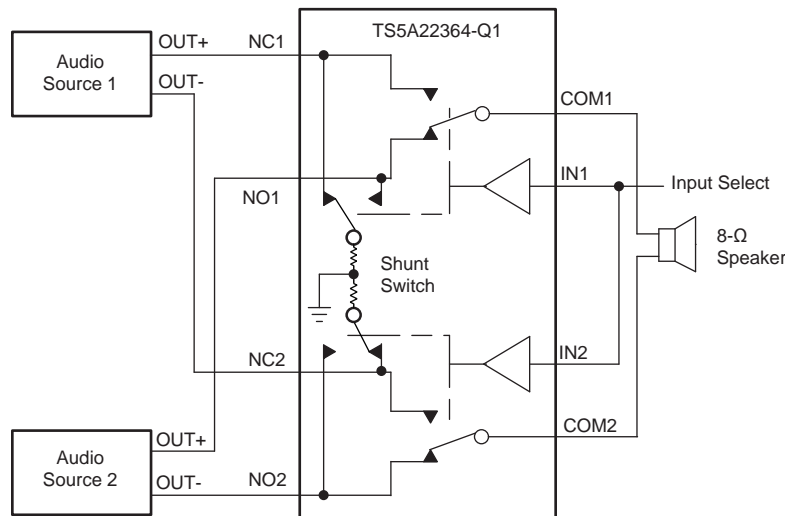
The TS5A22364-Q1 is a 2-channel single-pole double-throw (SPDT) analog switch designed to operate from 2.3 V to 5.5 V supply. The device features negative signal swing capability that allows signals below ground to pass through the switch without distortion. Additionally, the TS5A22364-Q1 includes an internal shunt switch, which automatically discharges any capacitance at the NC or NO terminals when they are unconnected to COM. This reduces the audible click-and-pop noise when switching between two sources. The break-before-make feature prevents signal distortion during the transfer of a signal from one path to another. Low On-state resistance, excellent channel-to-channel On-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A22364-Q1	VSSOP (10)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Simplified Schematic



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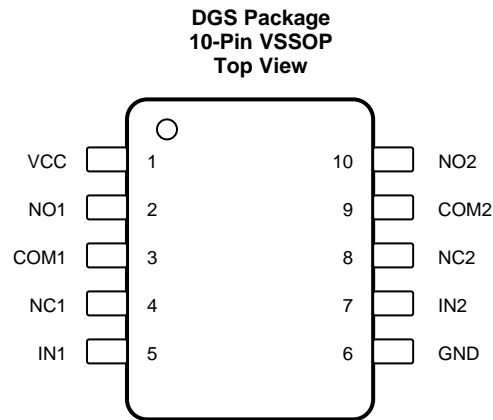
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## 4 Revision History

Changes from Original (October 2014) to Revision A	Page
<ul style="list-style-type: none"> <li>• Changed device status from <i>Product Preview</i> to <i>Production Data</i> ..... 1</li> </ul>	1

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VCC	I	Supply power
2	NO1	I/O	Normally open (NO) signal path, switch 1
3	COM1	I/O	Common signal path, switch 1
4	NC1	I/O	Normally closed (NC) signal path, switch 1
5	IN1	I	Digital control pin to connect COM1 to NO1, switch 1
6	GND	—	Ground
7	IN2	I	Digital control pin to connect COM2 to NO2, switch 2
8	NC2	I/O	Normally closed (NC) signal path, switch 2
9	COM2	I/O	Common signal path, switch 2
10	NO2	I/O	Normally open (NO) signal path, switch 2

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(3)</sup>	-0.5	6	V
V <sub>NC</sub>	Analog voltage on NC1-NC2 pin <sup>(3) (4) (5)</sup>	V <sub>CC</sub> - 6	V <sub>CC</sub> + 0.5	V
V <sub>NO</sub>	Analog voltage on NO1-NO2 pin <sup>(3) (4) (5)</sup>			
V <sub>COM</sub>	Analog voltage on COM1-COM2 pin <sup>(3) (4) (5)</sup>			
I <sub>I/O</sub> K	Analog port diode input clamp current V <sub>NC</sub> , V <sub>NO</sub> , V <sub>COM</sub> < 0 or V <sub>NC</sub> , V <sub>NO</sub> , V <sub>COM</sub> > V <sub>CC</sub>	-50	50	mA
I <sub>NC</sub>	On-state switch continuous current	-150	150	mA
I <sub>NO</sub> I <sub>COM</sub>	On-state switch peak current <sup>(6)</sup>	-300	300	
I <sub>RSH</sub>	Off-state switch shunt resistor current	-20	20	mA
V <sub>IN</sub>	Digital input voltage	-0.5	6.5	V
I <sub>IK</sub>	Digital input clamp current <sup>(3) (4)</sup> V <sub>IN</sub> < 0	-50	50	mA
I <sub>CC</sub> I <sub>GND</sub>	Continuous current through V <sub>CC</sub> or GND	-100	100	mA
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration <10% duty cycle.

### 6.2 ESD Ratings

		MIN	MAX	UNIT	
V <sub>ESD</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	-2500	2500	V
		Charged device model (CDM), per AEC Q100-011 all pins	-1500	1500	

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	5.5	V
V <sub>NC</sub>	Signal path voltage	V <sub>CC</sub> - 5.5	V <sub>CC</sub>	V
V <sub>NO</sub>				
V <sub>COM</sub>				
V <sub>IN</sub>	Digital control	GND	V <sub>CC</sub>	V

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup> (2)		TS5A22364-Q1		UNIT
		DGS (VSSOP)		
		10 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	163.3		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.4		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	83.1		°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	6.8		°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	81.8		°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics—2.5-V Supply

V<sub>CC</sub> = 2.3 V to 2.7 V, T<sub>A</sub> = –40°C to +125°C (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>								
Analog signal	V <sub>COM</sub> V <sub>NO</sub> V <sub>NC</sub>				V <sub>CC</sub> – 5.5		V <sub>CC</sub>	V
On-state resistance	R <sub>on</sub>	V <sub>NC</sub> or V <sub>NO</sub> = V <sub>CC</sub> , 1.5 V, V <sub>CC</sub> = 5.5 V I <sub>COM</sub> = –100 mA	25°C –40°C to +125°C	2.7 V		0.65	0.94 1.3	Ω
On-state resistance match between channels	ΔR <sub>on</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 1.5 V, I <sub>COM</sub> = –100 mA	25°C –40°C to +125°C	2.7 V		0.023	0.11 0.15	Ω
On-state resistance flatness	R <sub>on(flat)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = V <sub>CC</sub> , 1.5 V, V <sub>CC</sub> = 5.5 V I <sub>COM</sub> = –100 mA	25°C –40°C to +125°C	2.7 V		0.18	0.46 0.56	Ω
Shunt switch resistance	R <sub>SH</sub>	I <sub>NO</sub> or I <sub>NC</sub> = 10 mA	–40°C to +125°C	2.7 V		25	55	Ω
On-state leakage current	I <sub>COM(ON)</sub>	V <sub>NC</sub> and V <sub>NO</sub> = floating, V <sub>COM</sub> = V <sub>CC</sub> , V <sub>CC</sub> = 5.5 V	25°C –40°C to +125°C	2.7 V	–200		200 2500	nA
<b>DIGITAL CONTROL INPUTS (IN)<sup>(2)</sup></b>								
Input logic high	V <sub>IH</sub>		–40°C to +125°C		1.4		V <sub>CC</sub>	V
Input logic low	V <sub>IL</sub>		–40°C to +125°C				0.4	V
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>IN</sub> = V <sub>CC</sub> or 0	25°C –40°C to +125°C	2.7 V	–250		250 250	nA
<b>DYNAMIC</b>								
Turnon time	t <sub>ON</sub>	V <sub>COM</sub> = V <sub>CC</sub> , R <sub>L</sub> = 300 Ω	25°C –40°C to +125°C	2.5 V 2.3 V to 2.7 V		44	80 120	ns
Turnoff time	t <sub>OFF</sub>	V <sub>COM</sub> = V <sub>CC</sub> , R <sub>L</sub> = 300 Ω	25°C –40°C to +125°C	2.5 V 2.3 V to 2.7 V		22	70 70	ns
Break-before-make time	t <sub>BBM</sub>		25°C	2.5 V	1	7		ns
Charge injection	Q <sub>C</sub>	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	25°C	2.5 V		215		pC
On-State NC, NO, COM capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>CC</sub> or GND, Switch ON, f = 10 MHz	25°C	2.5 V		370		pF
Digital input capacitance	C <sub>I</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	25°C	2.5 V		2.6		pF
Bandwidth	BW	R <sub>L</sub> = 50 Ω, –3 dB	25°C	2.5 V		17		MHz

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report, [SCBA004](#).

**Electrical Characteristics—2.5-V Supply (continued)**
 $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +125^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER	TEST CONDITIONS	$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
Off-state isolation	$O_{ISO}$	$R_L = 50 \Omega$ $f = 100 \text{ kHz}$ , See <a href="#">Figure 21</a>	25°C	2.5 V		-66	dB
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$ $f = 100 \text{ kHz}$ , See <a href="#">Figure 22</a>	25°C	2.5 V		-75	dB
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 35 \text{ pF}$ $f = 20 \text{ Hz to } 20 \text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	2.5 V		0.01	%
<b>SUPPLY</b>							
Positive supply current	$I_{CC}$	$V_{COM}$ and $V_{IN} = V_{CC}$ or GND, $V_{NC}$ and $V_{NO} = \text{floating}$	25°C	2.7 V	0.2	1.1	$\mu\text{A}$
			-40°C to +125°C			1.3	
		$V_{COM} = V_{CC} - 5.5 \text{ V}$ , $V_{IN} = V_{CC}$ or GND, $V_{NC}$ and $V_{NO} = \text{floating}$	-40°C to +125°C	2.7 V		3.3	$\mu\text{A}$

**6.6 Electrical Characteristics—3.3-V Supply**
 $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +125^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER	TEST CONDITIONS	$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
Analog signal	$V_{COM}$ $V_{NO}$ $V_{NC}$			$V_{CC} - 5.5$		$V_{CC}$	V
On-state resistance	$R_{on}$	$V_{NC}$ or $V_{NO} \leq V_{CC}$ , 1.5 V, $V_{CC} - 5.5 \text{ V}$ , $I_{COM} = -100 \text{ mA}$ COM to NO or NC, See <a href="#">Figure 14</a>	25°C -40°C to +125°C	3 V	0.61	0.87	$\Omega$
On-state resistance match between channels	$\Delta R_{on}$	$V_{NC}$ or $V_{NO} = 1.5 \text{ V}$ , $I_{COM} = -100 \text{ mA}$ COM to NO or NC, See <a href="#">Figure 14</a>	25°C -40°C to +125°C	3 V	0.024	0.13	$\Omega$
On-state resistance flatness	$R_{on(flat)}$	$V_{NC}$ or $V_{NO} \leq V_{CC}$ , 1.5 V, $V_{CC} - 5.5 \text{ V}$ , $I_{COM} = -100 \text{ mA}$ COM to NO or NC, See <a href="#">Figure 14</a>	25°C -40°C to +125°C	3 V	0.12	0.46	$\Omega$
Shunt switch resistance	$R_{SH}$	$I_{NO}$ or $I_{NC} = 10 \text{ mA}$	-40°C to +125°C	3 V	25	40	$\Omega$
On-state leakage current	$I_{COM(ON)}$	$V_{NC}$ and $V_{NO} = \text{floating}$ , $V_{COM} = V_{CC}, V_{CC} - 5.5 \text{ V}$ COM to NO or NC, See <a href="#">Figure 16</a>	25°C -40°C to +125°C	3.6 V	-200	200	nA
					-2500	2500	
<b>DIGITAL CONTROL INPUTS (IN)<sup>(2)</sup></b>							
Input logic high	$V_{IH}$		-40°C to +125°C		1.4	$V_{CC}$	V
Input logic low	$V_{IL}$		-40°C to +125°C			0.6	V
Input leakage current	$I_{IH}, I_{IL}$	$V_{IN} = V_{CC}$ or 0	25°C -40°C to +125°C	3.6 V	-250	250	nA
					-250	250	
<b>DYNAMIC</b>							
Turnon time	$t_{ON}$	$V_{COM} = V_{CC}$ , $R_L = 300 \Omega$ $C_L = 35 \text{ pF}$ , See <a href="#">Figure 18</a>	25°C	3.3 V	34	80	ns
			-40°C to +125°C	3 V to 3.6 V		80	
Turnoff time	$t_{OFF}$	$V_{COM} = V_{CC}$ , $R_L = 300 \Omega$ $C_L = 35 \text{ pF}$ , See <a href="#">Figure 18</a>	25°C	3.3 V	19	70	ns
			-40°C to +125°C	3 V to 3.6 V		70	
Break-before-make time	$t_{BBM}$	See <a href="#">Figure 19</a>	25°C	3.3 V	1	7	ns
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1 \text{ nF}$ , See <a href="#">Figure 23</a>	25°C	3.3 V		300	pC
On-State NC, NO, COM capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND, $f = 10 \text{ MHz}$ See <a href="#">Figure 17</a>	25°C	3.3 V		370	pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report, [SCBA004](#).

## Electrical Characteristics—3.3-V Supply (continued)

 $V_{CC} = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }+125^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
Digital input capacitance	$C_I$	$V_{IN} = V_{CC}$ or GND	See Figure 17	25°C	3.3 V		2.6		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , -3 dB	Switch ON, See Figure 20	25°C	3.3 V		17.5		MHz
Off-state isolation	$O_{ISO}$	$R_L = 50\ \Omega$	$f = 100\text{ kHz}$ , See Figure 21	25°C	3.3 V		-68		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$	$f = 100\text{ kHz}$ , See Figure 22	25°C	3.3 V		-76		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 35\text{ pF}$	$f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 24	25°C	3.3 V		0.008		%
<b>SUPPLY</b>									
Positive supply current	$I_{CC}$	$V_{COM}$ and $V_{IN} = V_{CC}$ or GND, $V_{NC}$ and $V_{NO} =$ floating		25°C	3.6 V		0.1	1.2	$\mu\text{A}$
				-40°C to +125°C				1.3	
		$V_{COM} = V_{CC} - 5.5\text{ V}$ , $V_{IN} = V_{CC}$ or GND, $V_{NC}$ and $V_{NO} =$ floating		-40°C to +125°C	3.6 V			3.4	$\mu\text{A}$

## 6.7 Electrical Characteristics—5-V Supply<sup>(1)</sup>

 $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }+125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>									
Analog signal	$V_{COM}$ , $V_{NO}$ , $V_{NC}$					$V_{CC} - 5.5$		$V_{CC}$	V
On-state resistance	$R_{on}$	$V_{NC}$ or $V_{NO} = V_{CC}$ , 1.6 V, $V_{CC} = -5.5\text{ V}$ , $I_{COM} = -100\text{ mA}$	COM to NO or NC, See Figure 14	25°C	4.5 V		0.52	0.74	$\Omega$
				-40°C to +125°C				0.83	
On-state resistance match between channels	$\Delta R_{on}$	$V_{NC}$ or $V_{NO} = 1.6\text{ V}$ , $I_{COM} = -100\text{ mA}$	COM to NO or NC, See Figure 14	25°C	4.5 V		0.04	0.23	$\Omega$
				-40°C to +125°C				0.30	
On-state resistance flatness	$R_{on(Flat)}$	$V_{NC}$ or $V_{NO} = V_{CC}$ , 1.6 V, $V_{CC} = -5.5\text{ V}$ , $I_{COM} = -100\text{ mA}$	COM to NO or NC, See Figure 14	25°C	4.5 V		0.076	0.46	$\Omega$
				-40°C to +125°C				0.5	
Shunt switch resistance	$R_{SH}$	$I_{NO}$ or $I_{NC} = 10\text{ mA}$		-40°C to +125°C	4.5 V		16	36	$\Omega$
On-state leakage current	$I_{COM(ON)}$	$V_{NC}$ and $V_{NO} =$ Floating, $V_{COM} = V_{CC}$ , $V_{CC} - 5.5\text{ V}$	See Figure 16	25°C	5.5 V		-200	200	nA
				-40°C to +125°C				-2500	
<b>DIGITAL CONTROL INPUTS (IN)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$			-40°C to +125°C		2.4		$V_{CC}$	V
Input logic low	$V_{IL}$			-40°C to +125°C				0.8	V
Input leakage current	$I_{IH}$ , $I_{IL}$	$V_{IN} = V_{CC}$ or 0		25°C	5.5 V		-250	250	nA
				-40°C to +125°C				-250	
<b>DYNAMIC</b>									
Turnon time	$t_{ON}$	$V_{COM} = V_{CC}$ , $R_L = 300\ \Omega$	$C_L = 35\text{ pF}$ , See Figure 18	25°C	5 V		27	80	ns
				-40°C to +125°C	4.5 V to 5.5 V			80	
Turnoff time	$t_{OFF}$	$V_{COM} = V_{CC}$ , $R_L = 300\ \Omega$	$C_L = 35\text{ pF}$ , See Figure 18	25°C	5 V		13	70	ns
				-40°C to +125°C	4.5 V to 5.5 V			70	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_{CC}/2$ , $R_L = 300\ \Omega$	$C = 35\text{ pF}$ , See Figure 19	25°C	5 V	1	3.5		ns
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$	$C_L = 1\text{ nF}$ , See Figure 23	25°C	5 V		500		pC

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

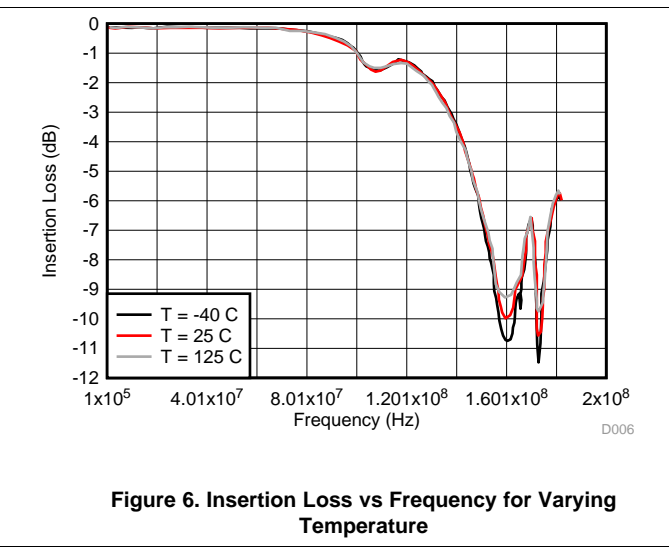
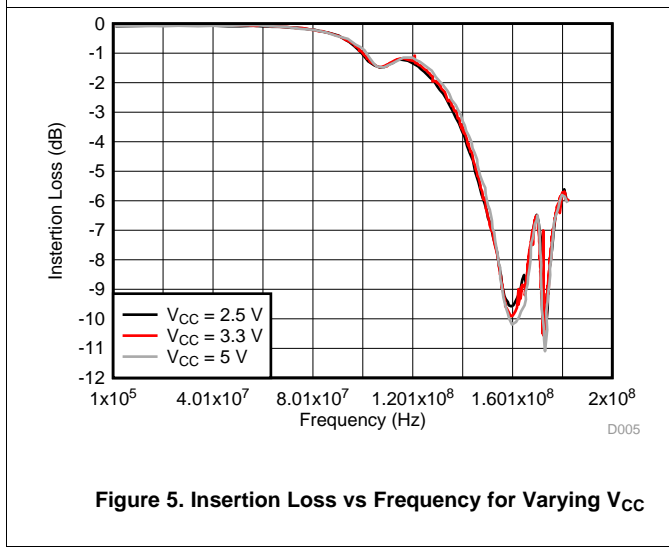
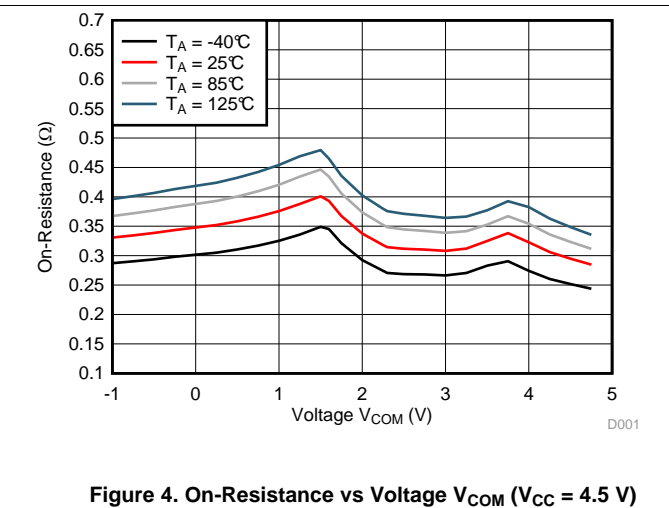
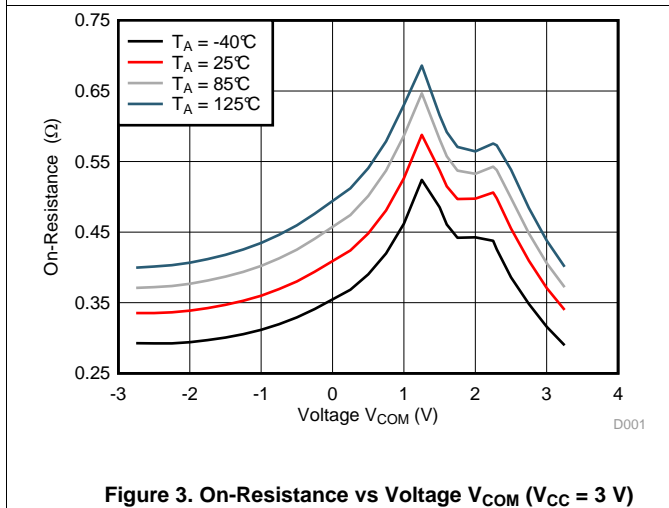
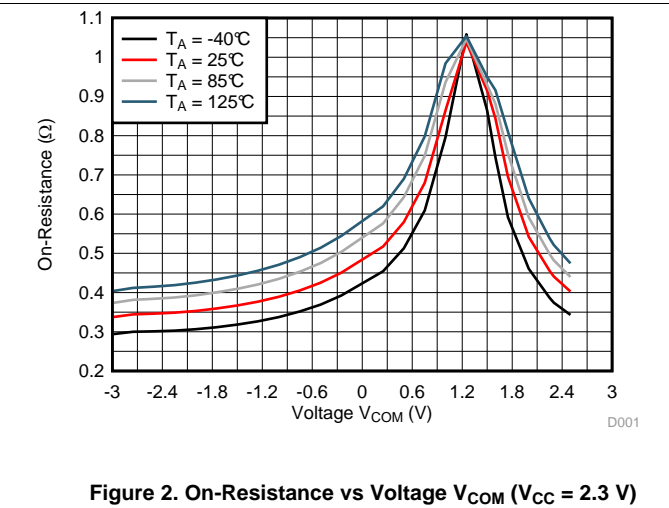
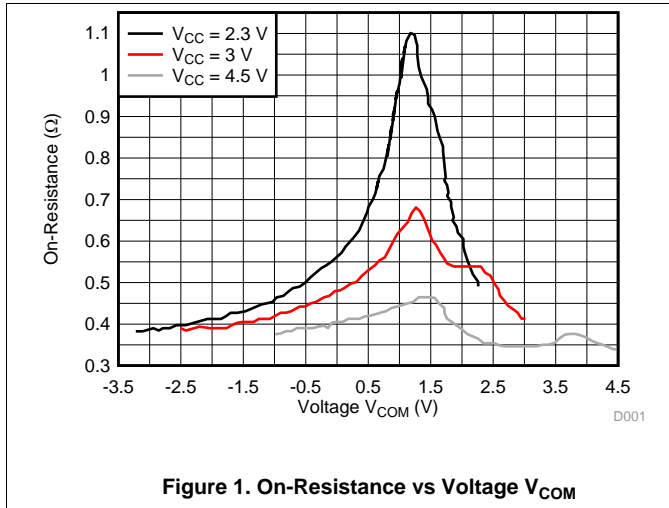
(2) All unused digital inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report, [SCBA004](#).

**Electrical Characteristics—5-V Supply<sup>(1)</sup> (continued)**
 $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
ON-State NC, NO, COM capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND	See <a href="#">Figure 17</a>	25°C	5 V		370		pF
Digital input capacitance	$C_I$	$V_{IN} = V_{CC}$ or GND	See <a href="#">Figure 17</a>	25°C	5 V		2.6		pF
Bandwidth	BW	$R_L = 50 \Omega$	See <a href="#">Figure 20</a>	25°C	5 V		18.3		MHz
Off-state isolation	$O_{ISO}$	$R_L = 50 \Omega$	$f = 100 \text{ kHz}$ , See <a href="#">Figure 21</a>	25°C	5 V		-70		dB
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$	$f = 100 \text{ kHz}$ , See <a href="#">Figure 22</a>	25°C	5 V		-78		dB
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 35 \text{ pF}$	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	5 V		0.009		%
<b>SUPPLY</b>									
Positive supply current	$I_{CC}$	$V_{COM}$ and $V_{IN} = V_{CC}$ or GND, $V_{NC}$ or $V_{NO} = \text{floating}$	25°C	5.5 V	0.2	1.3	$\mu\text{A}$		
			-40°C to +125°C		3.5				
		$V_{COM} = V_{CC} - 5.5 \text{ V}$ , $V_{IN} =$ $V_{CC}$ or GND, $V_{NC}$ or $V_{NO} =$ floating	-40°C to +125°C		5				



### 6.8 Typical Characteristics



Typical Characteristics (continued)

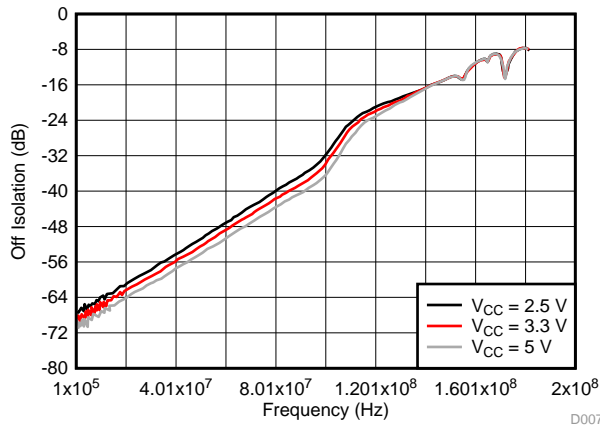


Figure 7. Off Isolation vs Frequency for Varying  $V_{CC}$

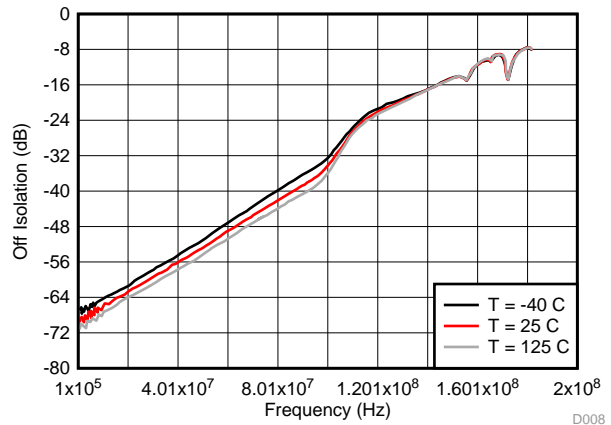


Figure 8. Off Isolation vs Frequency for Varying Temperature

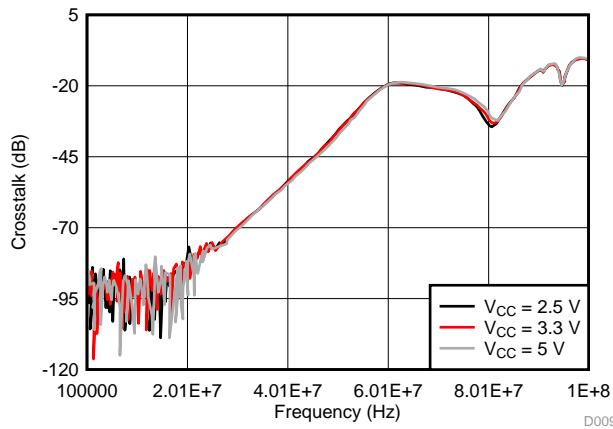


Figure 9. Crosstalk vs Frequency for Varying  $V_{CC}$

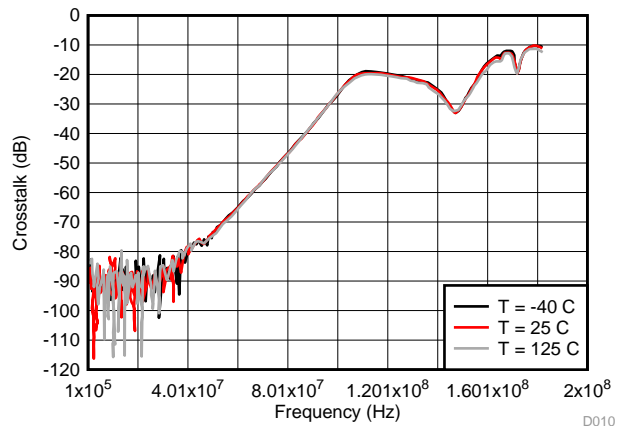


Figure 10. Crosstalk vs Frequency ( $V_{CC} = 3.3\text{ V}$ )

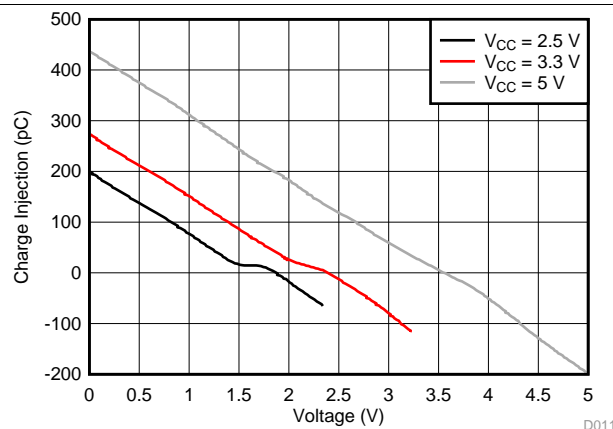


Figure 11. Charge Injection vs Voltage  $V_{COM}$

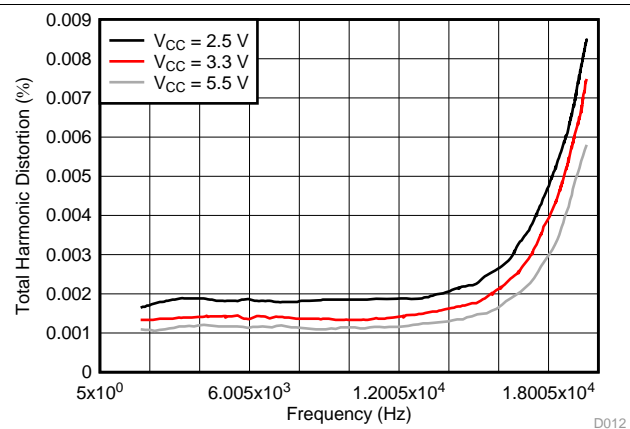
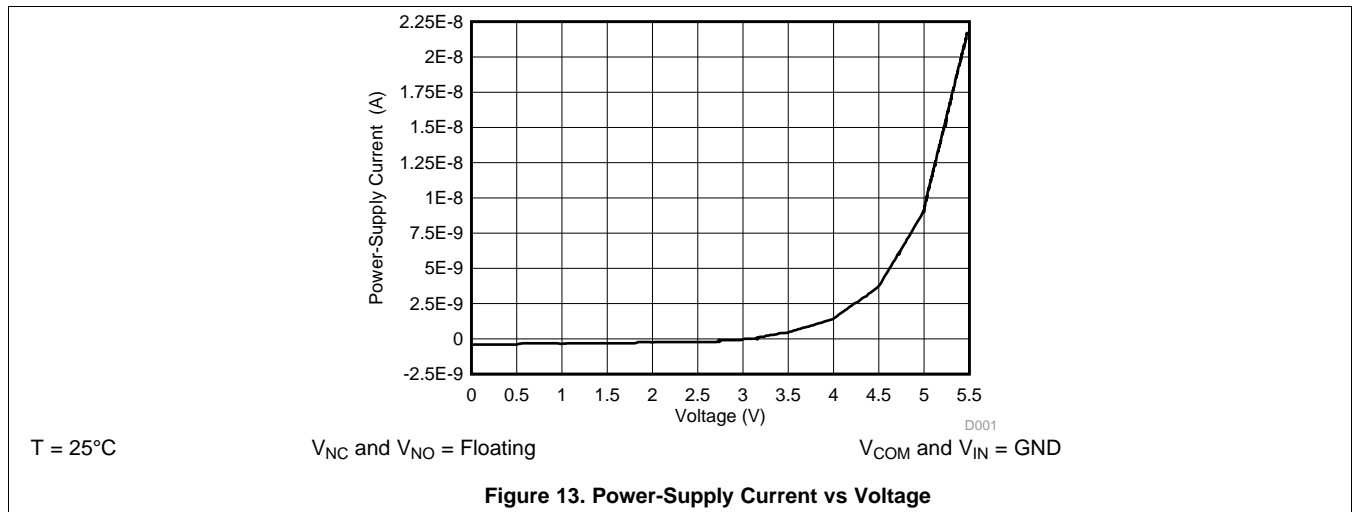
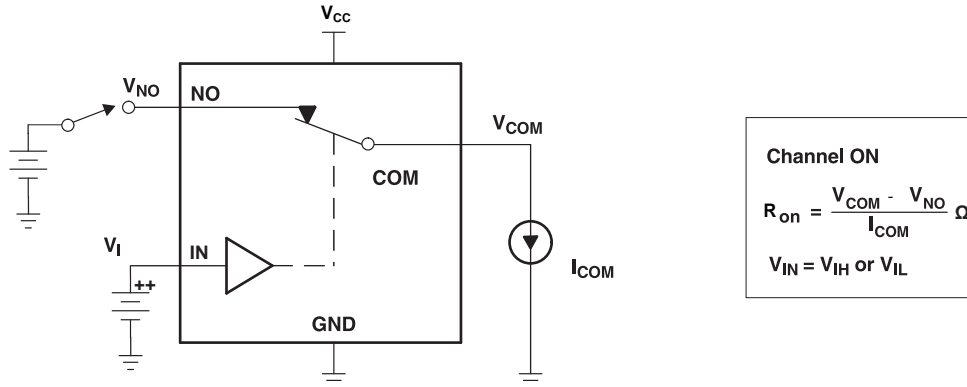


Figure 12. Total Harmonic Distortion vs Frequency

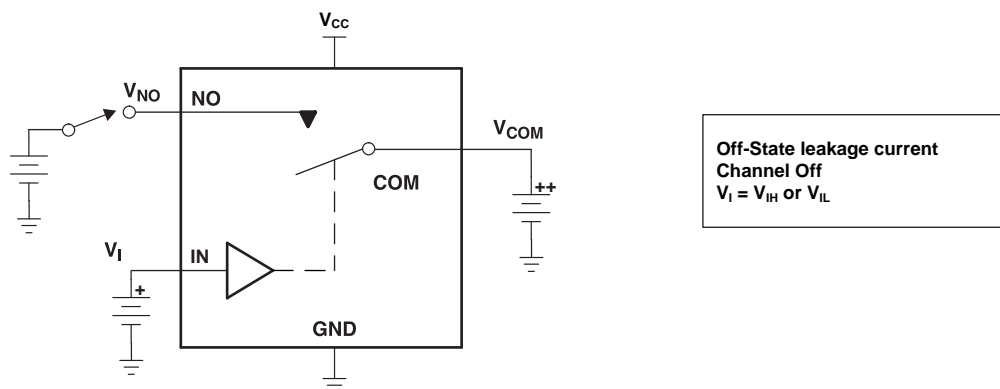
Typical Characteristics (continued)



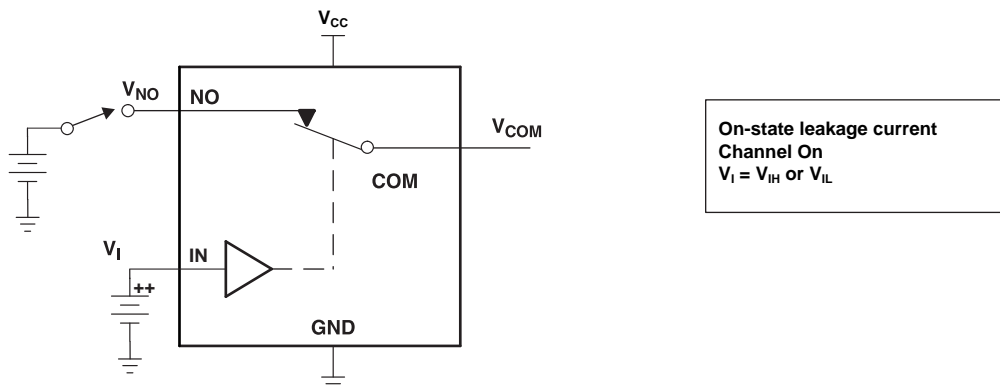
## 7 Parameter Measurement Information



**Figure 14. On-State Resistance ( $R_{on}$ )**



**Figure 15. Off-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NO(OFF)}$ )**



**Figure 16. On-State Leakage Current  
( $I_{COM(ON)}$ ,  $I_{NO(ON)}$ )**

Parameter Measurement Information (continued)

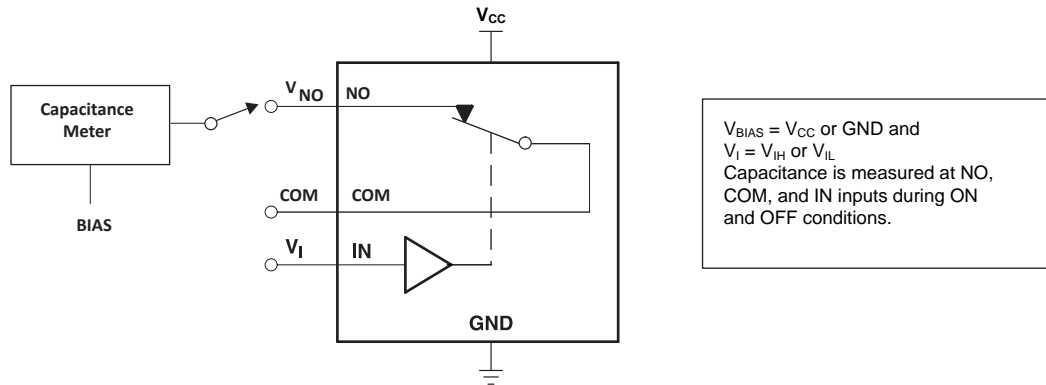
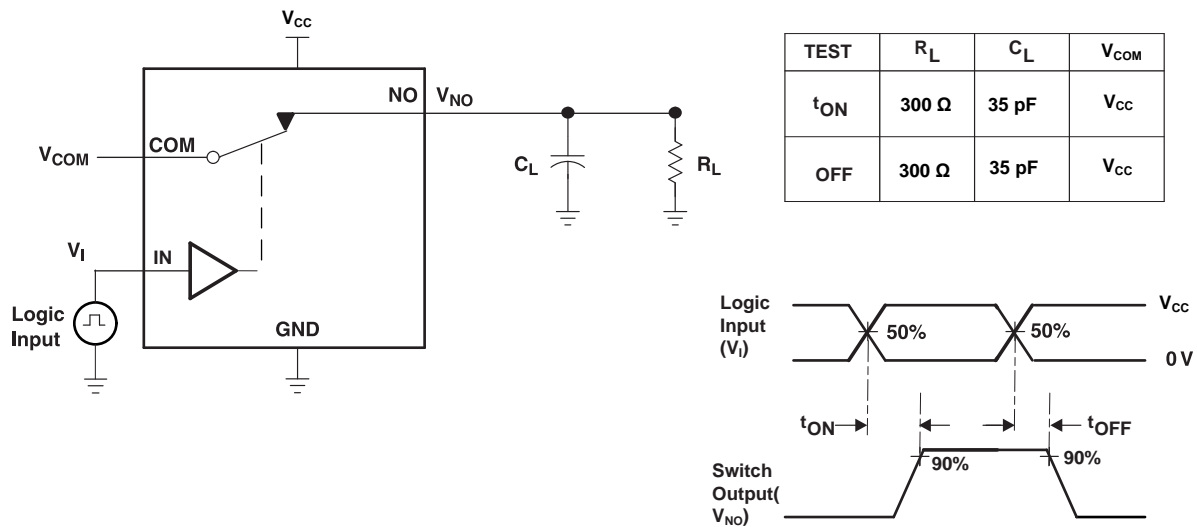


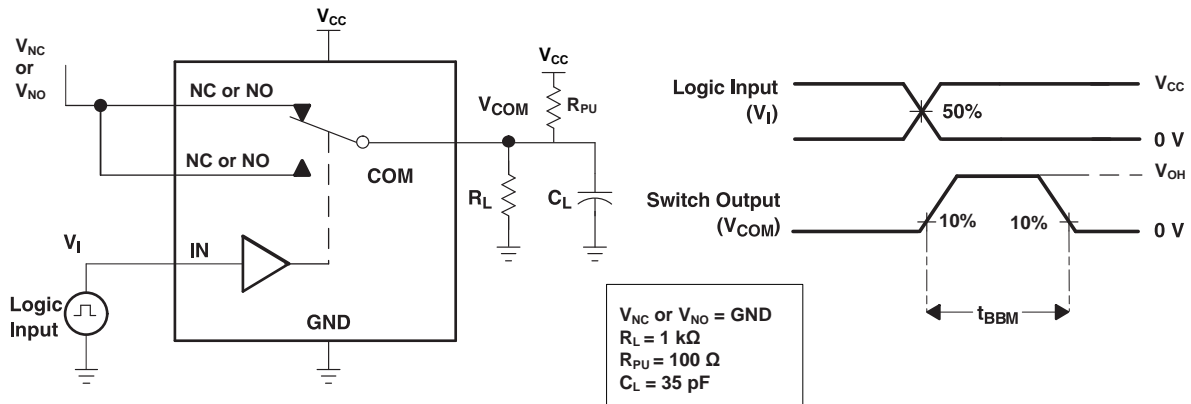
Figure 17. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NO(OFF)}$ ,  $C_{NO(ON)}$ )



- A. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- B.  $C_L$  includes probe and jig capacitance.

Figure 18. Turnon ( $t_{ON}$ ) and Turnoff time ( $t_{OFF}$ )

Parameter Measurement Information (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.

Figure 19. Break-Before-Make Time ( $t_{BBM}$ )

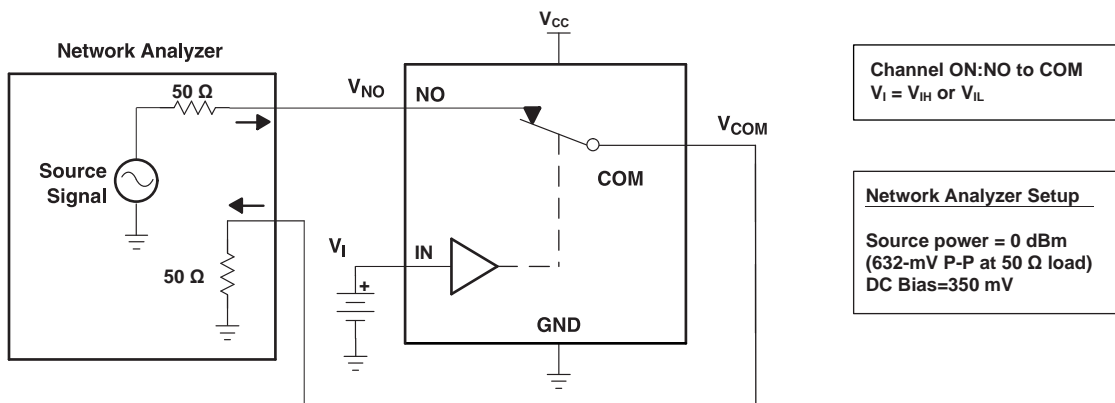


Figure 20. Bandwidth (BW)

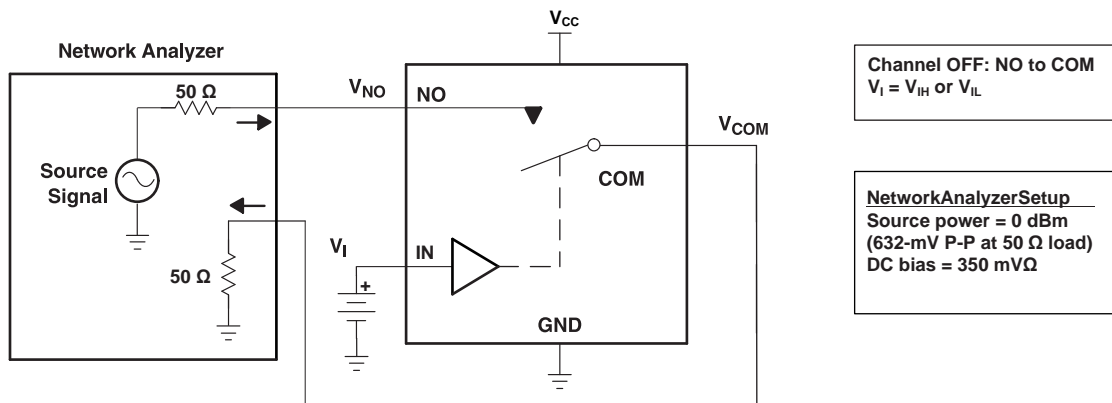


Figure 21. Off Isolation ( $O_{ISO}$ )

Parameter Measurement Information (continued)

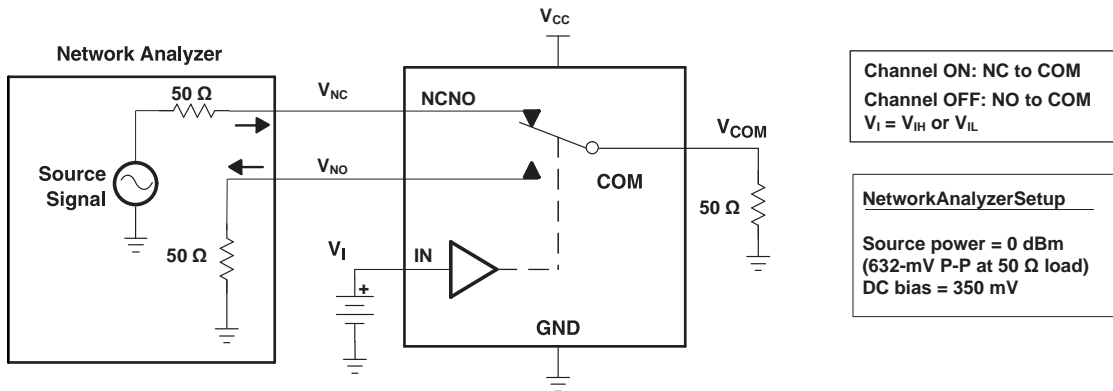
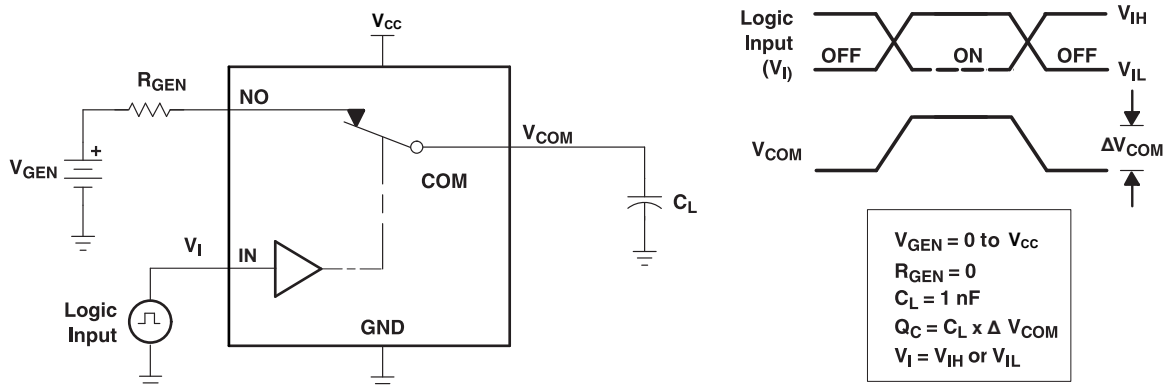


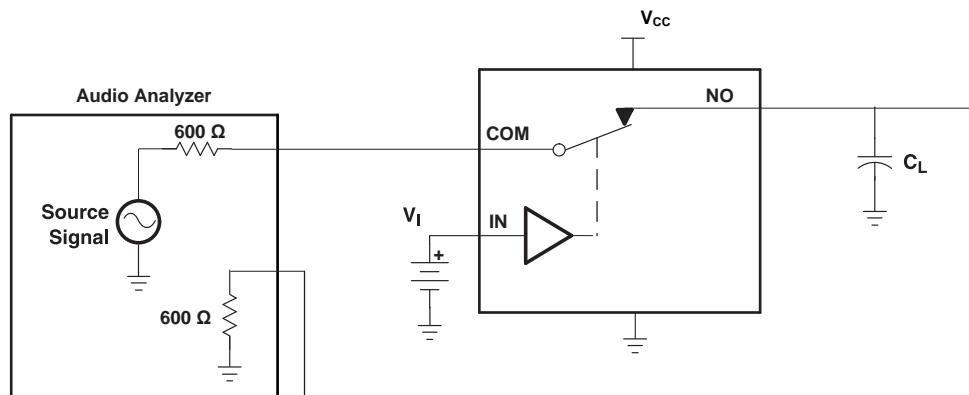
Figure 22. Crosstalk ( $X_{TALK}$ )



- A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- B.  $C_L$  includes probe and jig capacitance.

Figure 23. Charge Injection ( $Q_C$ )

Channel ON: COM to NO     $V_I = V_{IH}$  or  $V_{IL}$      $R_L = 600 \Omega$   
 $V_{SOURCE} = 0.5$  V P-P     $f_{SOURCE} = 20$  Hz to 20 kHz     $C_L = 35$  pF



- A.  $C_L$  includes probe and jig capacitance.

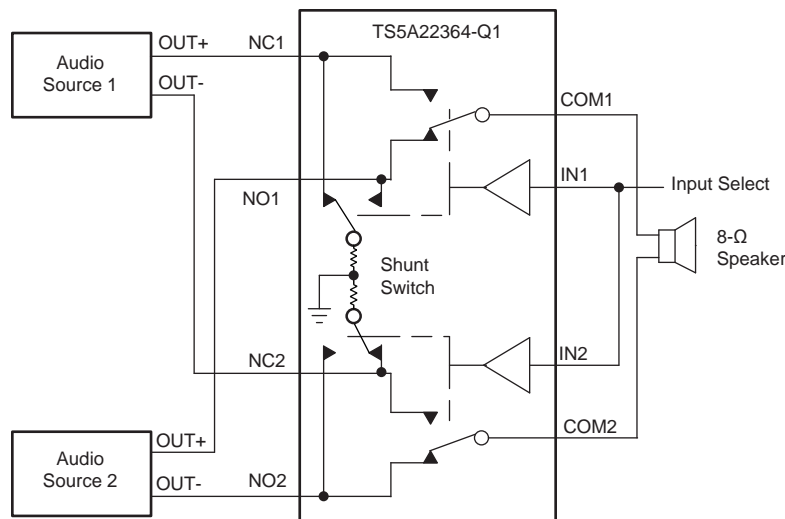
Figure 24. Total Harmonic Distortion (THD)

## 8 Detailed Description

### 8.1 Overview

The TS5A22364-Q1 is a 2-channel single-pole double-throw (SPDT) analog switch designed to operate from 2.3-V to 5.5-V power supply. The device features negative signal swing capability that allows signals below ground to pass through the switch without distortion. Additionally, the TS5A22364-Q1 includes an internal shunt switch, which automatically discharges any capacitance at the NC or NO terminals when they are not connected to COM. This reduces the audible click-and-pop noise when switching between two sources. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low On-state resistance, excellent channel-to-channel On-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

#### 8.3.1 Click-and-Pop Reduction

The 50-Ω shunt switches on the TS5A22364-Q1 automatically discharge any capacitance at the NC or NO terminals when they are not connected to COM. This reduces the audible click-and-pop sounds that occur when switching between audio sources. Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops.

### 8.4 Device Functional Modes

Table 1 shows the function table for the TS5A22364-Q1.

**Table 1. Function Table**

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Negative Signal Swing Capability

The TS5A22364-Q1 dual SPDT switches feature negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single 2.3-V to 5.5-V supply. The input and output signal swing of the device is dependant on the supply voltage  $V_{CC}$ : the device can pass signals as high as  $V_{CC}$  and as low as  $V_{CC} - 5.5$  V, including signals below ground with minimal distortion. The Off state signal path (either NC or NO) during the operation of the TS5A22364-Q1 cannot handle negative DC voltage.

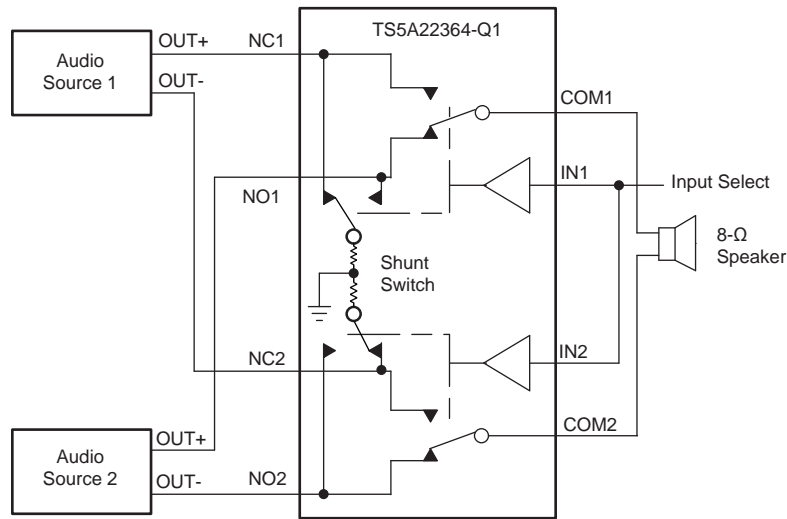
Table 2 shows the input-output signal swing the user can get with different supply voltages.

**Table 2. Input-Output Signal Swing**

SUPPLY VOLTAGE, $V_{CC}$	MINIMUM ( $V_{NC}, V_{NO}, V_{COM}$ ) = $V_{CC} - 5.5$	MAXIMUM ( $V_{NC}, V_{NO}, V_{COM}$ ) = $V_{CC}$	MINIMUM ( $V_{NC}, V_{NO}, V_{COM}$ ) = $V_{CC} - 5.5$	MAXIMUM ( $V_{NC}, V_{NO}, V_{COM}$ ) = $V_{CC}$
	ON State signal path		OFF state signal path	
5.5 V	0 V	5.5 V	0 V	5.5 V
4.2 V	-1.3 V	4.2 V	0 V	4.2 V
3.3 V	-2.2 V	3.3 V	0 V	3.3 V
3 V	-2.5 V	3 V	0 V	3 V
2.5 V	-3 V	2.5 V	0 V	2.5 V

### 9.2 Typical Application

The 50- $\Omega$  shunt switches on the TS5A22364-Q1 automatically discharge any capacitance at the NC or NO terminals when they are unconnected to COM. This reduces audible click-and-pop sounds that occur when switching between audio sources. Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops. See Figure 25.

**Typical Application (continued)**


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**Figure 25. Shunt Switch Block Diagram**
**9.2.1 Design Requirements**

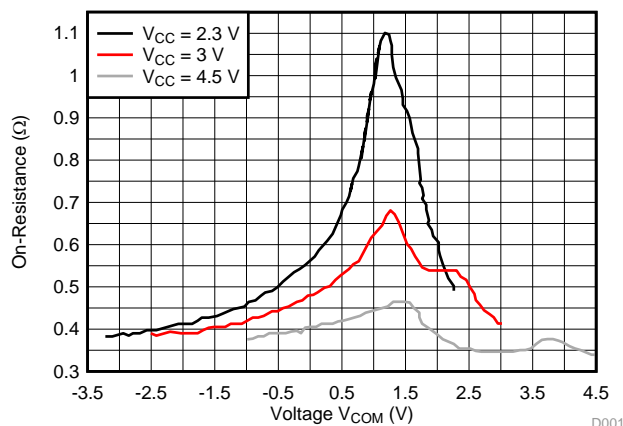
Tie the digitally controlled input select pins IN1 and IN2 to  $V_{CC}$  or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

**9.2.2 Detailed Design Procedure**

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A22364-Q1 operates from a single 2.3-V to 5.5-V supply and the input-output signal swing of the device is dependant of the supply voltage  $V_{CC}$ . The device passes signals as high as  $V_{CC}$  and as low as  $V_{CC} - 5.5$  V. Use Table 2 as a guide for selecting supply voltage based on the signal passing through the switch.

Limit the current through the shunt resistor so as not to exceed the  $\pm 20$  mA.

Ensure that the device is powered up with a supply voltage on  $V_{CC}$  before a voltage can be applied to the signal paths NC and NO.

**9.2.3 Application Curve**

**Figure 26. On-Resistance vs Voltage  $V_{COM}$**

## 10 Power Supply Recommendations

The TS5A22364-Q1 operates from a single 2.3-V to 5.5-V supply. The device must be powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO. It is recommended to include a 100  $\mu$ s delay after VCC is at voltage before applying a signal on NC and NO paths.

It is also good practice to place a 0.1- $\mu$ F bypass capacitor on the supply pin VCC to GND to smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

## 11 Layout

### 11.1 Layout Guidelines

It is recommended to place a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

Minimize trace lengths and vias on the signal paths in order to preserve signal integrity.

### 11.2 Layout Example

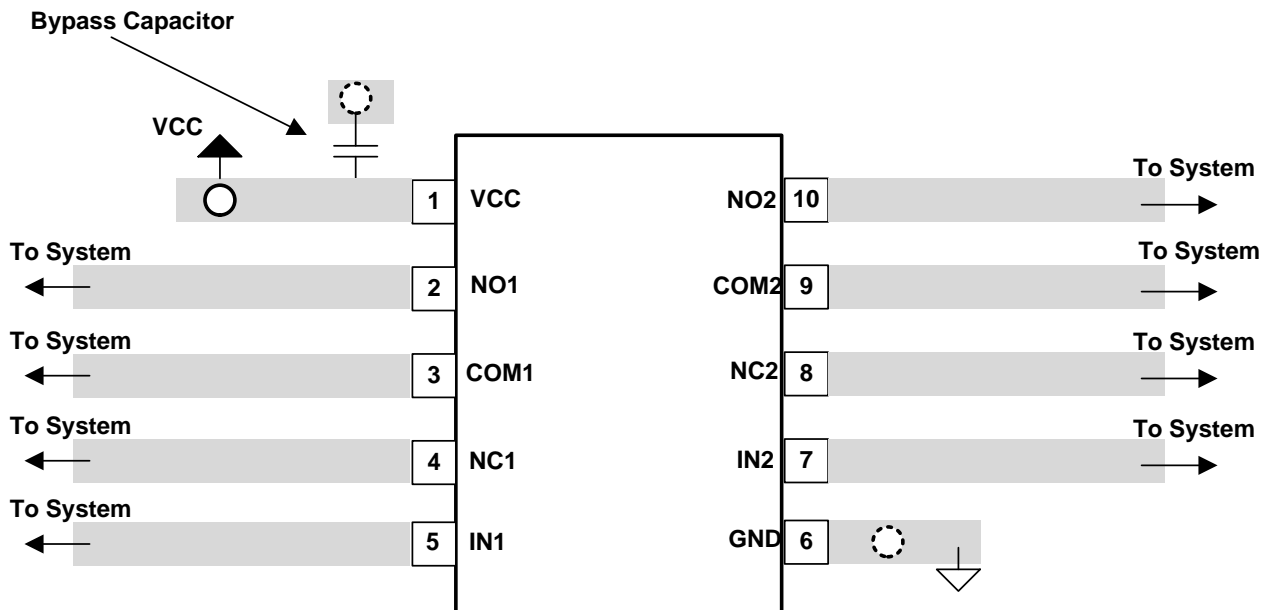
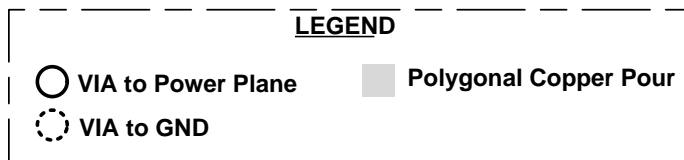


Figure 27. Layout Example of TS5A22364-Q1

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TS5A22364QDGSRQ1</a>	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJN
TS5A22364QDGSRQ1.B	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJN

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TS5A22364-Q1 :**

- Catalog : [TS5A22364](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A22364QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A22364QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0

# DGS0010A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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