











TS5A2066

SCDS184F - JANUARY 2005-REVISED AUGUST 2018

# TS5A2066 Dual-Channel 10-Ω SPST Analog Switch

#### **Features**

- Low ON-State Resistance (10  $\Omega$ )
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- **Excellent ON-State Resistance Matching**
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### **Applications**

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits
- Cell Phones
- Low-Voltage Data-Acquisition Systems
- **PDAs**

#### Description 3

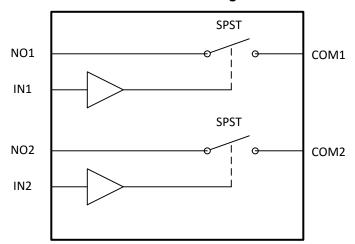
The TS5A2066 device is a dual single-pole singlethrow (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V<sub>CC</sub> can be transmitted in either direction.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
	SSOP (DCT)	2.95 mm x 2.80 mm
TS5A2066	VSSOP (DCU)	2.30 mm x 2.00 mm
	DSBGA (YZP)	1.25 mm x 2.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### **Functional Block Diagram**





### **Table of Contents**

1	Features 1		8.2 Functional Block Diagram	<mark>2</mark> 1
2	Applications 1		8.3 Feature Description	. 21
3	Description 1		8.4 Device Functional Modes	21
4	Revision History2	9	Application and Implementation	. 22
5	Pin Configuration and Functions		9.1 Application Information	. 22
6	Specifications4		9.2 Typical Application	22
U	6.1 Absolute Maximum Ratings	10	Power Supply Recommendations	. 23
	6.2 ESD Ratings	11	Layout	. 24
	6.3 Recommended Operating Conditions		11.1 Layout Guidelines	
	6.4 Thermal Information		11.2 Layout Example	. 24
	6.5 Electrical Characteristics For 5-V Supply	12	Device and Documentation Support	. 25
	6.6 Electrical Characteristics For 3.3-V Supply 7		12.1 Receiving Notification of Documentation Updates	s <mark>25</mark>
	6.7 Electrical Characteristics For 2.5-V Supply 9		12.2 Community Resources	25
	6.8 Electrical Characteristics For 1.8-V Supply		12.3 Trademarks	. 25
	6.9 Typical Performance		12.4 Electrostatic Discharge Caution	. 25
7	Parameter Measurement Information		12.5 Glossary	. 25
8	Detailed Description	13	Mechanical, Packaging, and Orderable	
•	8.1 Overview		Information	. 25
	O.1 OVOIVION			

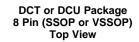
### 4 Revision History

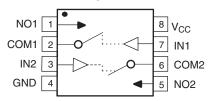
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Cł	nanges from Revision E (June 2017) to Revision F	Page
•	Changed the YZP Package From: Top View To: Bottom View	3
Cł	nanges from Revision D (April 2010) to Revision E	Page
•	Added Device Information table, Pin Configuration and Functions section, ESD Ratings table, Recommended Operating Conditions table, Thermal Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
•	Deleted the Summary of Characteristics table	3
•	Changed pin 8 From: V <sub>+</sub> To: V <sub>CC</sub> in the pinout images	3
•	Deleted the ON-state resistance Min values of 10 $\Omega$ and 12 $\Omega$ in the <i>Electrical Characteristics For 3.3-V Suppy</i> table	<mark>7</mark>
•	Deleted the ON-state resistance Min values of 20 $\Omega$ in the <i>Electrical Characteristics For 2.5-V Supply</i> table	9
•	Changed Test Conditions for Charge injection From: See Figure 23 To; See Figure 24 in the <i>Electrical Characteristics For 2.5-V Supply</i> table	10
•	Deleted the ON-state resistance Min values of 80 $\Omega$ and 90 $\Omega$ in the <i>Electrical Characteristics For 1.8-V Supply</i> table.	11
•	Changed V <sub>+</sub> to V <sub>CC</sub> in the <i>Typical Performance</i> graphs	13
•	Changed V <sub>+</sub> to V <sub>CC</sub> in the <i>Parameter Measurement Information</i> images	

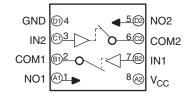


### 5 Pin Configuration and Functions





#### YZP Package 8 Pin (DSBGA) Bottom View



### **Pin Functions**

NO.	NAME	DESCRIPTION
1	NO1	Normally open
2	COM1	Common
3	IN2	Digital control to connect COM to NO
4	GND	Digital ground
5	NO2	Normally open
6	COM2	Common
7	IN1	Digital control to connect COM to NO
8	V <sub>CC</sub>	Power supply



### 6 Specifications

### 6.1 Absolute Maximum Ratings (1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range <sup>(3)</sup>		-0.5	6.5	V
$V_{NO} \ V_{COM}$	Analog voltage range (3)(4)(5)		-0.5	V <sub>CC</sub> + 0.5	V
$I_{K}$	Analog port diode current	$V_{NO}$ , $V_{COM} < 0$ or $V_{NO}$ , $V_{COM} > V_{CC}$	-50	50	mA
$I_{NO}$ $I_{COM}$	On-state switch current	$V_{NO}$ , $V_{COM} = 0$ to $V_{CC}$	-50	50	mA
$V_{\text{IN}}$	Digital input voltage range (3)(4)		-0.5	6.5	V
I <sub>IK</sub>	Digital input clamp current	V <sub>IN</sub> < 0	-50		mA
I <sub>CC</sub>	Continuous current through V <sub>CC</sub>			100	mA
$I_{\text{GND}}$	Continuous current through GND	·	-100	100	mA
T <sub>stg</sub>	Storage temperature range	·	-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

3) All voltages are with respect to ground, unless otherwise specified.

### 6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

#### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	1.65	5.5	V
$V_{NO} V_{COM}$	Analog voltage range	0	$V_{CC}$	V
$V_{IN}$	Digital input voltage range	0	5.5	V

#### 6.4 Thermal Information

			TS5A2066					
	THERMAL METRIC <sup>(1)</sup>	DCT (SSOP)	DCU (VSSOP)	YZP (DSBGA)	UNIT			
		8 PINS	8 PINS	8 PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.1	212.8	99.8	°C/W			
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	106.8	93.6	1.0	°C/W			
$R_{\theta JB}$	Junction-to-board thermal resistance	127.8	133.6	29.6	°C/W			
ΨЈТ	Junction-to-top characterization parameter	30.2	30.4	0.5	°C/W			
ΨЈВ	Junction-to-board characterization parameter	125.5	133.1	29.8	°C/W			

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

<sup>(4)</sup> The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>(5)</sup> This value is limited to 5.5 V maximum.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .



### 6.5 Electrical Characteristics For 5-V Supply<sup>(1)</sup>

 $V_{CC}$  = 4.5 V to 5.5 V,  $T_A$  = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST	CONDITIONS	T <sub>A</sub>	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub>					0		V <sub>CC</sub>	V
ON-state resistance	r <sub>on</sub>	$0 \le V_{NO} \le V_{CC}$ , $I_{COM} = -32 \text{ mA}$ ,	Switch ON, See Figure 16	25°C Full	4.5 V		7.5	10 15	Ω
ON-state				25°C			0.4	1	
resistance match between channels	$\Delta r_{on}$	$V_{NO} = 3.15 \text{ V},$ $I_{COM} = -32 \text{ mA},$	Switch ON, SeeFigure 16	Full	4.5 V			3	Ω
ON-state		0 ≤ V <sub>NO</sub> ≤ V <sub>CC</sub> ,	Switch ON,	25°C			3.5	5	
resistance flatness	r <sub>on(flat)</sub>	$I_{\text{COM}} = -32 \text{ mA},$	See Figure 16	Full	4.5 V			8	Ω
		V <sub>NO</sub> = 1 V,		25°C		-30	-10	30	
NO OFF leakage current	I <sub>NO(OFF)</sub>	$V_{COM} = 4.5 \text{ V},$ or $V_{NO} = 4.5 \text{ V},$ $V_{COM} = 1 \text{ V},$	Switch OFF, See Figure 17	Full	5.5 V	5 V -40		40	nA
		$V_{COM} = 1 V$ ,		25°C		-50	-8	50	
COM OFF leakage current	I <sub>COM(OFF)</sub>	$V_{NO} = 4.5 \text{ V},$ or $V_{COM} = 4.5 \text{ V},$ $V_{NO} = 1 \text{ V},$	Switch OFF, See Figure 17	Full	5.5 V	-50		50	nA
		V <sub>NO</sub> = 1 V,		25°C		-40	-12	40	
NO ON leakage current	I <sub>NO(ON)</sub>	$V_{COM} = Open,$ or $V_{NO} = 4.5 V,$ $V_{COM} = Open$	Switch ON, See Figure 18	Full	5.5 V	-4		40	nA
		$V_{COM} = 1 V$ ,		25°C		-70	-30	70	
COM ON leakage current	I <sub>COM(ON)</sub>	$V_{NO}$ = Open, or $V_{COM}$ = 4.5 V, $V_{NO}$ = Open,	Switch ON, See Figure 18	Full	5.5 V	-70		70	nA
Digital Control I	nput (IN)								
Input logic high	V <sub>IH</sub>			Full		V <sub>CC</sub> × 0.7		5.5	V
Input logic low	V <sub>IL</sub>			Full		0		$V_{CC} \times 0.3$	V
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>IN</sub> = 5.5 V or 0		25°C	5.5 V	-0.1	0.05	0.1	μA
Current	יורי יונ	. IIV — 0.0 V OI O		Full		-1		1	

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.



### Electrical Characteristics For 5-V Supply<sup>(1)</sup> (continued)

 $V_{CC}$  = 4.5 V to 5.5 V,  $T_A$  = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST C	ONDITIONS	T <sub>A</sub>	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
Dynamic									
				25°C	5 V	4.4	5.2	5.8	
Turn-on time	t <sub>ON</sub>	$V_{COM} = 3 V,$ $R_L = 300 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 20	Full	4.5 V to 5.5 V	3.4		6.1	ns
				25°C	5 V	1.7	2.6	3.6	
Turn-off time	t <sub>OFF</sub>	$V_{COM} = 3 V,$ $R_L = 300 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 20	Full	4.5 V to 5.5 V	1.3		4.2	ns
Charge injection	Q <sub>C</sub>	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C <sub>L</sub> = 0.1 nF, See Figure 24	25°C	5 V		1		pC
NO OFF capacitance	C <sub>NO(OFF)</sub>	$V_{NO} = V_{CC}$ or GND,	Switch OFF, See Figure 19	25°C	5 V		5.5		pF
COM OFF capacitance	C <sub>COM(OFF)</sub>	V <sub>COM</sub> = V <sub>CC</sub> or GND,	Switch OFF, See Figure 19	25°C	5 V		5.5		pF
NO ON capacitance	C <sub>NO(ON)</sub>	$V_{NO} = V_{CC}$ or GND,	Switch ON, See Figure 19	25°C	5 V		13.5		pF
COM ON capacitance	C <sub>COM(ON)</sub>	$V_{COM} = V_{CC}$ or GND,	Switch ON, See Figure 19	25°C	5 V		13.5		pF
Digital input capacitance	C <sub>IN</sub>	$V_{IN} = V_{CC}$ or GND,	See Figure 19	25°C	5 V		2.5		pF
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON, See Figure 21	25°C	5 V		300		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \ \Omega,$ $f = 10 \ MHz,$	Switch OFF, See Figure 22	25°C	5 V		-68		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \ \Omega,$ $f = 10 \ MHz,$	Switch ON, See Figure 23	25°C	5 V		-66		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 25	25°C	5 V		0.01%		
Supply									
Positive supply current	Icc	$V_{IN} = V_{CC}$ or GND,	Switch ON or OFF	25°C Full	5.5 V		0.1	1 5	μΑ



# 6.6 Electrical Characteristics For 3.3-V Supply<sup>(1)</sup>

 $V_{CC} = 3 \text{ V to } 3.6 \text{ V}, T_A = -40^{\circ}\text{C to } 85^{\circ}\text{C} \text{ (unless otherwise noted)}$ 

PARAMETER	SYMBOL	TEST C	CONDITIONS	TA	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
Analog Switch				•					
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub>					0		V <sub>CC</sub>	V
ON-state resistance	r <sub>on</sub>	$0 \le V_{NO} \le V_{CC},$ $I_{COM} = -24 \text{ mA},$	Switch ON, See Figure 16	25°C Full	3 V		12	15 20	Ω
ON-state resistance match	$\Delta r_{\sf on}$	V <sub>NO</sub> = 2.1 V,	Switch ON,	25°C	3 V		0.5	1.5	Ω
between channels	Δion	$I_{COM} = -24 \text{ mA},$	See Figure 16	Full	3 7			3.5	22
ON-state		0 ≤ V <sub>NO</sub> ≤ V <sub>CC</sub> ,	Switch ON.	25°C	0.17		7	8	•
resistance flatness	r <sub>on(flat)</sub>	$I_{COM} = -24 \text{ mA},$	See Figure 16	Full	3 V			12	Ω
		$V_{NO} = 1 V$ ,		25°C		-30	-6	30	
NO OFF leakage current	I <sub>NO(OFF)</sub>	$V_{COM} = 3 \text{ V},$ or $V_{NO} = 3 \text{ V},$ $V_{COM} = 1 \text{ V},$	Switch OFF, See Figure 17	Full	3.6 V	-40		40	nA
		$V_{COM} = 1 V$ ,		25°C		-50	-7	50	
COM OFF leakage current	I <sub>COM(OFF)</sub>	$V_{NO} = 3 V$ , or $V_{COM} = 3 V$ , $V_{NO} = 1 V$ ,	Switch OFF, See Figure 17	Full	3.6 V	-50		50	nA
		$V_{NO} = 1 V$ ,		25°C		-40	-7	40	
NO ON leakage current	I <sub>NO(ON)</sub>	$V_{COM} = Open,$ or $V_{NO} = 3 V,$ $V_{COM} = Open,$	Switch ON, See Figure 18	Full	3.6 V	-40		40	nA
		$V_{COM} = 1 V$ ,		25°C		-70	-20	70	
COM ON leakage current	I <sub>COM(ON)</sub>	$V_{NO} = Open,$ or $V_{COM} = 3 V,$ $V_{NO} = Open,$	Switch ON, See Figure 18	Full	3.6 V	-70		70	nA
Digital Control Ir	nput (IN)								
Input logic high	V <sub>IH</sub>			Full		V <sub>CC</sub> × 0.7		5.5	V
Input logic low	$V_{IL}$		_	Full		0		$V_{CC} \times 0.3$	V
Input leakage	L. L.	V <sub>IN</sub> = 5.5 V or 0		25°C	261/	-0.1	0.05	0.1	
current	I <sub>IH</sub> , I <sub>IL</sub>	VIN = 3.3 V 01 0		Full	3.6 V	-1		1	μA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.



# Electrical Characteristics For 3.3-V Supply<sup>(1)</sup> (continued)

 $V_{CC} = 3 \text{ V to } 3.6 \text{ V}, T_A = -40^{\circ}\text{C to } 85^{\circ}\text{C (unless otherwise noted)}$ 

PARAMETER	SYMBOL	TEST CO	ONDITIONS	TA	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
Dynamic		1						•	
		V 2.V	C 25 nF	25°C	3.3 V	4.9	5.6	6.4	
Turn-on time	$t_{ON}$	$V_{COM} = 2 \text{ V},$ $R_L = 300 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 20	Full	3 V to 3.6 V	4.3		7.1	ns
		V - 2 V	$C_1 = 35 \text{ pF},$	25°C	3.3 V	2	2.7	3.7	
Turn-off time	t <sub>OFF</sub>	$V_{COM} = 2 \text{ V},$ $R_L = 300 \Omega,$	See Figure 20	Full	3 V to 3.6 V	1.3		4.7	ns
Charge injection	Q <sub>C</sub>	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C <sub>L</sub> = 0.1 nF, See Figure 24	25°C	3.3 V		0.5		рС
NO OFF capacitance	C <sub>NO(OFF)</sub>	$V_{NO} = V_{CC}$ or GND,	Switch OFF, See Figure 19	25°C	3.3 V		5.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND,	Switch OFF, See Figure 19	25°C	3.3 V		6		pF
NO ON capacitance	C <sub>NO(ON)</sub>	$V_{NO} = V_{CC}$ or GND,	Switch ON, See Figure 19	25°C	3.3 V		14		pF
COM ON capacitance	C <sub>COM(ON)</sub>	$V_{COM} = V_{CC}$ or GND,	Switch ON, See Figure 19	25°C	3.3 V		14		pF
Digital input capacitance	$C_{l}$	$V_{IN} = V_{CC}$ or GND,	See Figure 19	25°C	3.3 V		3		pF
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON, See Figure 21	25°C	3.3 V		300		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 10 MHz,	Switch OFF, See Figure 22	25°C	3.3 V		-68		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \Omega$ , $f = 10 MHz$ ,	Switch ON, See Figure 23	25°C	3.3 V		-66		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 25	25°C	3.3 V	(	0.065%		
Supply									
Positive supply	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	Switch ON or OFF	25°C	3.6 V		0.1	1	μA
current	100	TIN - VCC OF SIND,	5	Full	3.0 V			5	μ, ,



# 6.7 Electrical Characteristics For 2.5-V Supply<sup>(1)</sup>

 $V_{CC} = 2.3 \text{ V}$  to 2.7 V,  $T_A = -40^{\circ}\text{C}$  to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST	CONDITIONS	T <sub>A</sub>	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub>					0		V <sub>CC</sub>	V
ON-state resistance	r <sub>on</sub>	$0 \le V_{NO} \le V_{CC},$ $I_{COM} = -8 \text{ mA},$	Switch ON, See Figure 16	25°C Full	2.3 V		22	30	Ω
ON-state resistance match between	$\Delta r_{\sf on}$	V <sub>NO</sub> = 1.6 V, I <sub>COM</sub> = -8 mA,	Switch ON, SeeFigure 16	25°C Full	2.3 V		0.5	1.5	Ω
Channels ON-state resistance	r <sub>on(flat)</sub>	0 ≤ V <sub>NO</sub> ≤ V <sub>CC</sub> ,	Switch ON,	25°C	2.3 V		16	18	Ω
flatness	ion(flat)	$I_{COM} = -8 \text{ mA},$	See Figure 16	Full	2.0 V			25	
NO OFF leakage	l	$V_{NO} = 0.5 \text{ V},$ $V_{COM} = 2.2 \text{ V},$ or	Switch OFF,	25°C	2.7 V	-30	-5.5	30	nA
current	I <sub>NO(OFF)</sub>	$V_{NO} = 2.2 \text{ V},$ $V_{COM} = 0.5 \text{ V},$	See Figure 17	Full	2.7 V	-40		40	11/5
COM		$V_{COM} = 0.5 \text{ V},$ $V_{NO} = 2.2 \text{ V},$		25°C		-50	-7.5	50	
OFF leakage current	I <sub>COM(OFF)</sub>	or $V_{COM} = 2.2 \text{ V},$ $V_{NO} = 0.5 \text{ V},$	Switch OFF, See Figure 17	Full	2.7 V	-50		50	nA
NO		V <sub>NO</sub> = 0.5 V,		25°C		-40	<b>-</b> 5	40	
ON leakage current	I <sub>NO(ON)</sub>	$V_{COM} = Open,$ or $V_{NO} = 2.2 \text{ V},$ $V_{COM} = Open,$	Switch ON, See Figure 18	Full	2.7 V	-40		40	nA
COM		V <sub>COM</sub> = 0.5 V,		25°C		-70	-12	70	
ON leakage current	I <sub>COM(ON)</sub>	$V_{NO}$ = Open, or $V_{COM}$ = 2.2 V, $V_{NO}$ = Open,	Switch ON, See Figure 18	Full	2.7 V	-70		70	nA
Digital Control In	nput (IN)							<u>.</u>	
Input logic high	V <sub>IH</sub>			Full		V <sub>CC</sub> × 0.7		5.5	V
Input logic low	V <sub>IL</sub>			Full		0		$V_{CC} \times 0.3$	V
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>IN</sub> = 5.5 V or 0		25°C Full	2.7 V	-0.1 -1	0.05	0.1	μΑ

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.



### Electrical Characteristics For 2.5-V Supply<sup>(1)</sup> (continued)

 $V_{CC}$  = 2.3 V to 2.7 V,  $T_A$  = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST C	ONDITIONS	TA	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
Dynamic									
		\/ 4 E \/	C 25 nF	25°C	2.5 V	5.7	6.4	8.1	
Turn-on time	t <sub>ON</sub>	$V_{COM} = 1.5 \text{ V},$ $R_L = 300 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 20	Full	2.3 V to 2.7 V	4.4		8.5	ns
		V <sub>COM</sub> = 1.5 V,	$C_1 = 35 pF$ ,	25°C	2.5 V	2.1	3.1	4.3	
Turn-off time	t <sub>OFF</sub>	$R_L = 300 \Omega$	See Figure 20	Full	2.3 V to 2.7 V	1.8		4.8	ns
Charge injection	Q <sub>C</sub>	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C <sub>L</sub> = 0.1 nF, See Figure 24	25°C	2.5 V		0.5		рС
NO OFF capacitance	C <sub>NO(OFF)</sub>	$V_{NO} = V_{CC}$ or GND,	Switch OFF, See Figure 19	25°C	2.5 V		6		pF
COM OFF capacitance	C <sub>COM(OFF)</sub>	V <sub>COM</sub> = V <sub>CC</sub> or GND,	Switch OFF, See Figure 19	25°C	2.5 V		6		pF
NO ON capacitance	C <sub>NO(ON)</sub>	$V_{NO} = V_{CC}$ or GND,	Switch ON, See Figure 19	25°C	2.5 V		14		pF
COM ON capacitance	C <sub>COM(ON)</sub>	$V_{COM} = V_{CC}$ or GND,	Switch ON, See Figure 19	25°C	2.5 V		14		pF
Digital input capacitance	C <sub>IN</sub>	$V_{IN} = V_{CC}$ or GND,	See Figure 19	25°C	2.5 V		3		pF
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON, See Figure 21	25°C	2.5 V		300		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 10 MHz,	Switch OFF, See Figure 22	25°C	2.5 V		-68		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \Omega$ , f = 10 MHz,	Switch ON, See Figure 23	25°C	2.5 V		-66		dB
Total harmonic distortion	THD	$R_L = 600 \ \Omega,$ $C_L = 50 \ pF,$	f = 20 Hz to 20 kHz, See Figure 25	25°C	2.5 V		0.35%		
Supply									
Positive supply current	I <sub>CC</sub>	$V_{IN} = V_{CC}$ or GND,	Switch ON or OFF	25°C Full	2.7 V		0.1	1 5	μΑ



### 6.8 Electrical Characteristics For 1.8-V Supply<sup>(1)</sup>

 $V_{CC}$  = 1.65 V to 1.95 V,  $T_A$  = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST C	ONDITIONS	TA	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub>					0		V <sub>CC</sub>	V
ON-state		$0 \le V_{NO} \le V_{CC}$	Switch ON,	25°C	1.65 V		85		Ω
resistance	r <sub>on</sub>	$I_{COM} = -4 \text{ mA},$	See Figure 16	Full	1.05 V			120	12
ON-state resistance match between channels	$\Delta r_{\sf on}$	$V_{NO} = 1.15 \text{ V},$ $I_{COM} = -4 \text{ mA},$	Switch ON, See Figure 16	25°C Full	1.65 V		0.9	6	Ω
ON-state		0 ≤ V <sub>NO</sub> ≤ V <sub>CC</sub> ,	Switch ON,	25°C			75	85	
resistance flatness	r <sub>on(flat)</sub>	$I_{COM} = -4 \text{ mA},$	See Figure 16	Full	1.65 V			100	Ω
		V <sub>NO</sub> = 0.3 V,		25°C		-30	-6	30	
NO OFF leakage current	I <sub>NO(OFF)</sub>	$V_{COM} = 1.65 \text{ V},$ or $V_{NO} = 1.65 \text{ V},$ $V_{COM} = 0.3 \text{ V},$	Switch OFF, See Figure 17	Full	1.95 V	-40		40	nA
		$V_{COM} = 0.3 \text{ V},$		25°C		-50	-7	50	
COM OFF leakage current	I <sub>COM(OFF)</sub>	$V_{NO} = 1.65 \text{ V},$ or $V_{COM} = 1.65 \text{ V},$ $V_{NO} = 0.3 \text{ V},$	Switch OFF, See Figure 17	Full	1.95 V	-50		50	nA
		$V_{NO} = 0.3 V$ ,		25°C		-40	7	40	
NO ON leakage current	I <sub>NO(ON)</sub>	$V_{COM} = Open,$ or $V_{NO} = 1.65 V,$ $V_{COM} = Open,$	Switch ON, See Figure 18	Full	1.95 V	-40		40	nA
		$V_{COM} = 0.3 \text{ V},$		25°C		-70	-8.5	70	
COM ON leakage current	I <sub>COM(ON)</sub>	$V_{NO}$ = Open, or $V_{COM}$ = 1.65 V, $V_{NO}$ = Open,	Switch ON, See Figure 18	Full	Full 1.95 V	-70		70	nA
Digital Control I	nput (IN)								
Input logic high	$V_{IH}$			Full		V <sub>CC</sub> × 0.65		5.5	V
Input logic low	V <sub>IL</sub>			Full		0		V <sub>CC</sub> × 0.35	V
Input leakage	1 1	V - 5 5 V or 0		25°C	1.95 V	-0.1	0.05	0.1	
current	I <sub>IH</sub> , I <sub>IL</sub>	$V_{IN} = 5.5 \text{ V or } 0$		Full	1.95 V	-1		1	μA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.



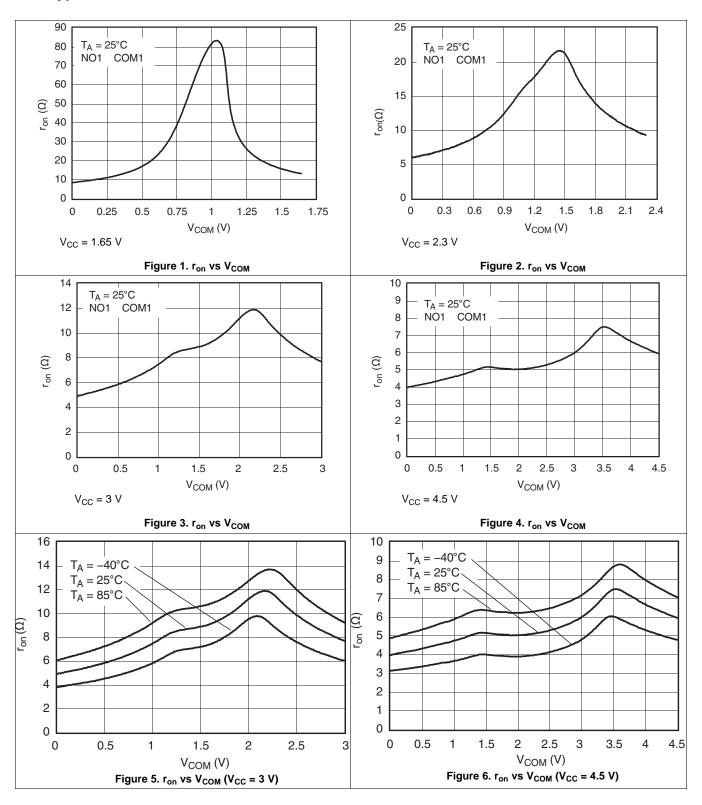
# Electrical Characteristics For 1.8-V Supply<sup>(1)</sup> (continued)

 $V_{CC}$  = 1.65 V to 1.95 V,  $T_A$  = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST COI	NDITIONS	T <sub>A</sub>	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
Dynamic									
				25°C	1.8 V	9.3	10.4	11.5	
Turn-on time	t <sub>ON</sub>	$V_{COM} = 1.3 \text{ V},$ $R_L = 300 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 20	Full	1.65 V to 1.95 V	6.8		12.9	ns
				25°C	1.8 V	3.3	4.3	5.2	
Turn-off time	t <sub>OFF</sub>	$V_{COM} = 1.3 \text{ V},$ $R_L = 300 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 20	Full	1.65 V to 1.95 V	2.4		6.5	ns
Charge injection	$Q_{\mathbb{C}}$	$V_{GEN} = 0,$ $R_{GEN} = 0,$	$C_L = 0.1 \text{ nF},$ See Figure 24	25°C	1.8 V		0.5		рС
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_{CC}$ or GND,	Switch OFF, See Figure 19	25°C	1.8 V		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND,	Switch OFF, See Figure 19	25°C	1.8 V		6		pF
NO ON capacitance	C <sub>NO(ON)</sub>	$V_{NO} = V_{CC}$ or GND,	Switch ON, See Figure 19	25°C	1.8 V		14.5		pF
COM ON capacitance	C <sub>COM(ON)</sub>	$V_{COM} = V_{CC}$ or GND,	Switch ON, See Figure 19	25°C	1.8 V		14.5		pF
Digital input capacitance	$C_{IN}$	$V_{IN} = V_{CC}$ or GND,	See Figure 19	25°C	1.8 V		3		pF
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON, See Figure 21	25°C	1.8 V		293		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 10 MHz,	Switch OFF, See Figure 22	25°C	1.8 V		-68		dB
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$ , $f = 10 MHz$ ,	Switch ON, See Figure 23	25°C	1.8 V		-66		dB
Total harmonic distortion	THD	$R_L = 10 \text{ k}\Omega,$ $C_L = 50 \text{ pF},$	f = 20 Hz to 20 kHz, See Figure 25	25°C	1.8 V		2.7%		
Supply									
Positive supply current	I <sub>CC</sub>	$V_{IN} = V_{CC}$ or GND,	Switch ON or OFF	25°C Full	1.95 V		0.1	1 5	μΑ



### 6.9 Typical Performance

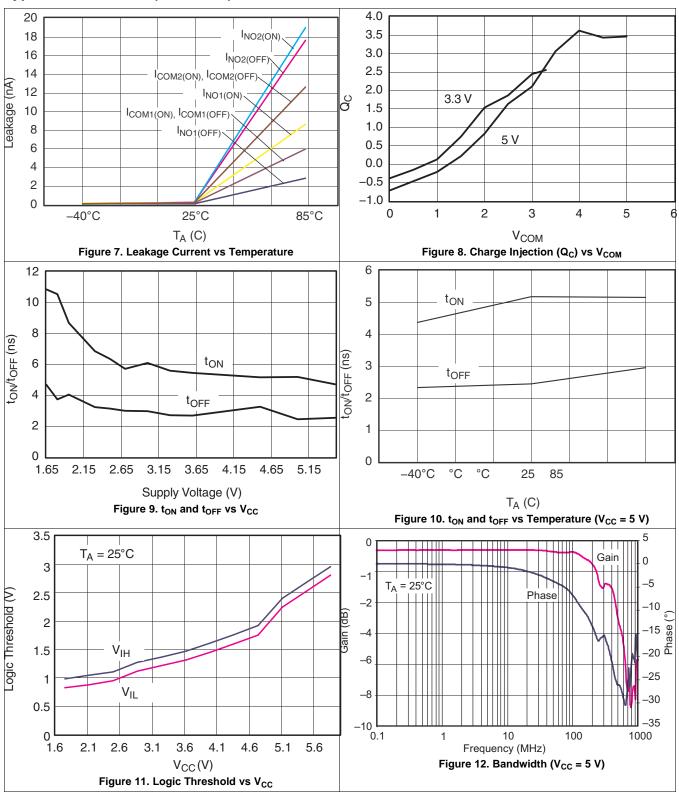


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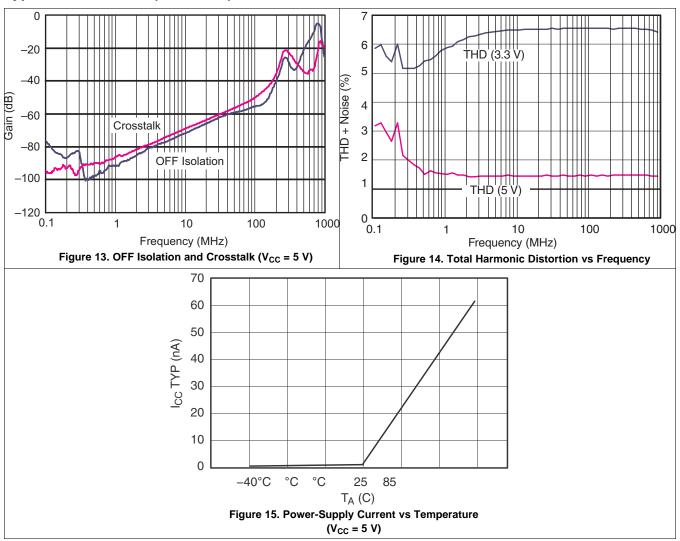
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### **Typical Performance (continued)**





### **Typical Performance (continued)**



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### 7 Parameter Measurement Information

**Table 1. Parameter Description** 

SYMBOL	DESCRIPTION
V <sub>COM</sub>	Voltage at COM
V <sub>NO</sub>	Voltage at NO
r <sub>on</sub>	Resistance between COM and NO ports when the channel is ON
$\Delta r_{\sf on}$	Difference of ron between channels in a specific device
r <sub>on(flat)</sub>	Difference between the maximum and minimum value of ron in a channel over the specified range of conditions
I <sub>NO(OFF)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I <sub>NO(ON)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I <sub>COM(OFF)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
I <sub>COM(ON)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V <sub>IH</sub>	Minimum input voltage for logic high for the control input (IN)
V <sub>IL</sub>	Maximum input voltage for logic low for the control input (IN)
$V_{IN}$	Voltage at the control input (IN)
I <sub>IH</sub> , I <sub>IL</sub>	Leakage current measured at the control input (IN)
t <sub>ON</sub>	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t <sub>OFF</sub>	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q <sub>C</sub>	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ , $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage.
C <sub>NO(OFF)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C <sub>NO(ON)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C <sub>COM(OFF)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C <sub>COM(ON)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C <sub>IN</sub>	Capacitance of IN
O <sub>ISO</sub>	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
X <sub>TALK</sub>	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is -3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I <sub>CC</sub>	Static power-supply current with the control (IN) pin at V <sub>CC</sub> or GND



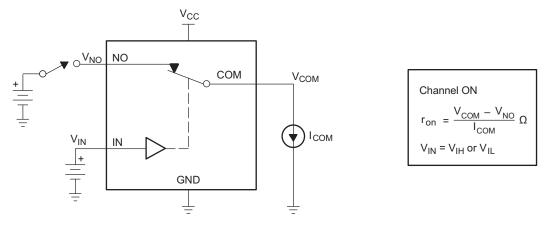


Figure 16. ON-State Resistance (ron)

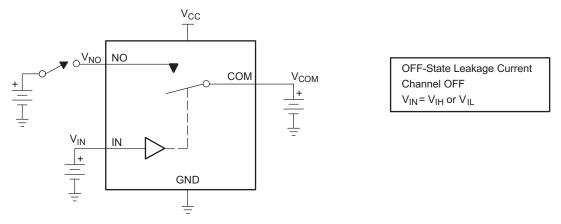


Figure 17. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NO(OFF)}$ )

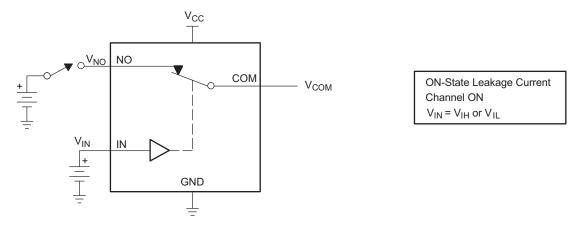


Figure 18. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NO(ON)}$ )



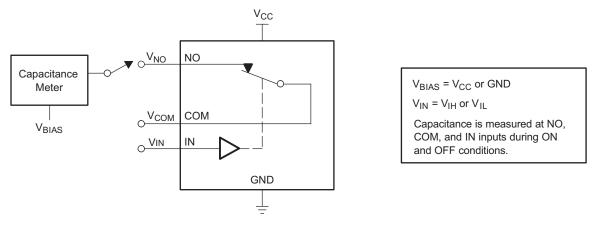
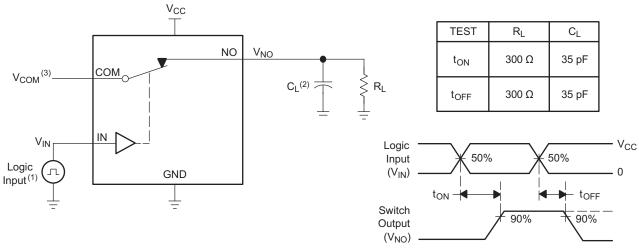


Figure 19. Capacitance (C<sub>IN</sub>, C<sub>COM(OFF)</sub>, C<sub>COM(ON)</sub>, C<sub>NO(OFF)</sub>, C<sub>NO(ON)</sub>)



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .
- (2) C<sub>L</sub> includes probe and jig capacitance.
- (3) See Electrical Characteristics tables for  $V_{\text{COM}}$ .

Figure 20. Turn-On  $(t_{ON})$  and Turn-Off Time  $(t_{OFF})$ 

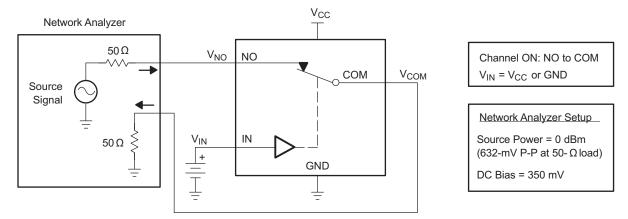


Figure 21. Bandwidth (BW)

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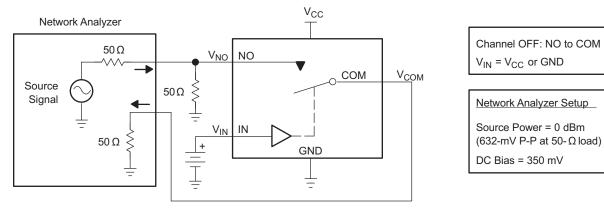


Figure 22. OFF Isolation (O<sub>ISO</sub>)

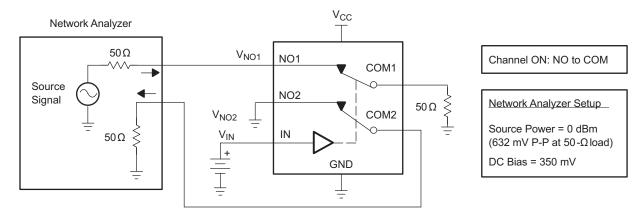
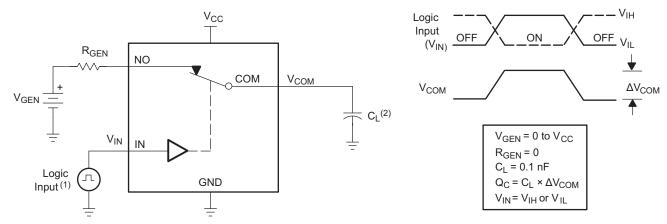


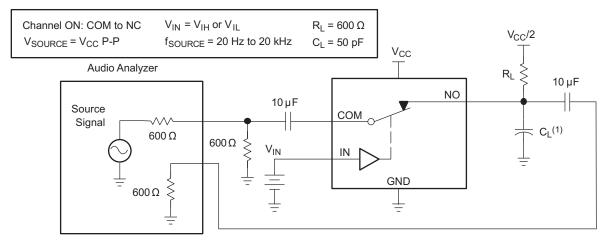
Figure 23. Crosstalk (X<sub>TALK</sub>)



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .
- (2) C<sub>L</sub> includes probe and jig capacitance.

Figure 24. Charge Injection (Q<sub>C</sub>)





(1)  $C_L$  includes probe and jig capacitance.

Figure 25. Total Harmonic Distortion (THD)

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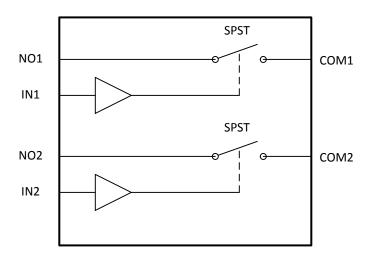


### 8 Detailed Description

#### 8.1 Overview

The TS5A2066 device is a 2-channel single-pole single-throw (1:1 SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to  $V_{CC}$  can be transmitted in either direction

### 8.2 Functional Block Diagram



### 8.3 Feature Description

5-V tolerant control inputs allow 5-V logic levels to be present on the IN pin irrespective of the voltage on VCC pin.

Low ON-resistance and THD performance allows minimal signal distortion through device.

### 8.4 Device Functional Modes

Table 2 shows the functional modes for TS5A23166.

**Table 2. Function Table** 

IN	NO TO COM, COM TO NO				
L	OFF				
Н	ON				



### 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TS5A2066 2-channel, 1:1 SPST analog switch is a basic component that could be used in any electrical system design that signal isolation.

### 9.2 Typical Application

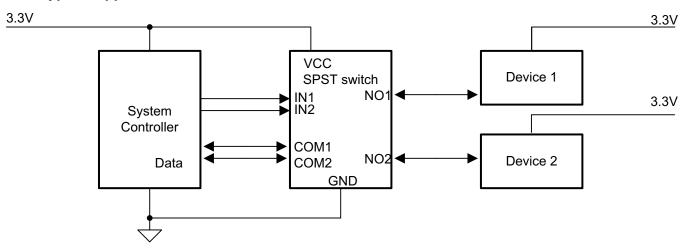


Figure 26. Typical Application Circuit

#### 9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the specified ranges in the recommended operating conditions to ensure proper performance.

#### 9.2.2 Detailed Design Procedure

The TS5A2066 can be properly operated without any external components.

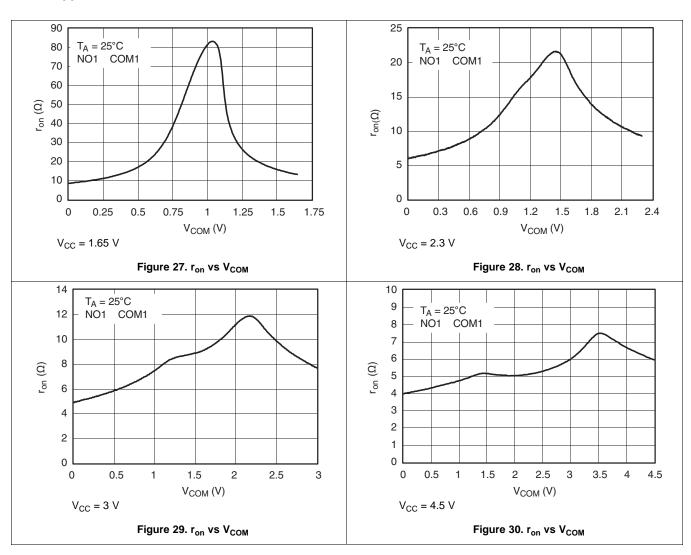
Unused signal path pins COM or NO maybe left floating or connected to ground through a  $50-\Omega$  resistor to prevent signal reflections back into the device.

TI recommends that the digital control pins (INX) be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin. Leaving the logic pins floating may increase I<sub>CC</sub>. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004), for further details.



### **Typical Application (continued)**

#### 9.2.3 Application Curves



### 10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1- $\mu$ F capacitor, connected from VCC to GND, is adequate for most applications. Copyright

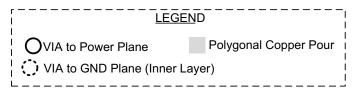


### 11 Layout

### 11.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

### 11.2 Layout Example



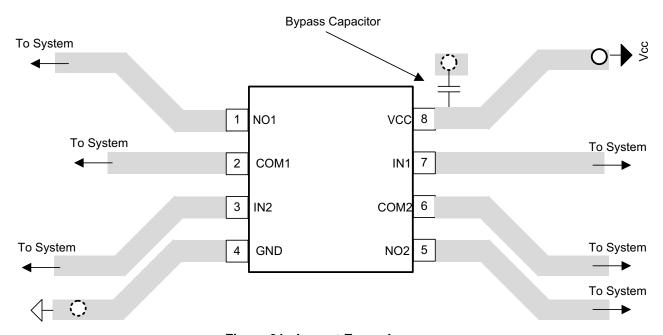


Figure 31. Layout Example



### 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.3 Trademarks

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All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(5)	(4)	(5)		(0)
TS5A2066DCTR	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAG Z
TS5A2066DCTR.B	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAG Z
TS5A2066DCUR	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	JAGR
TS5A2066DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	JAGR
TS5A2066YZPR	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	J4N
TS5A2066YZPR.B	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	J4N

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



### **PACKAGE OPTION ADDENDUM**

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**PACKAGE MATERIALS INFORMATION** 

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### TAPE AND REEL INFORMATION





	-
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A2066DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
TS5A2066DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
TS5A2066YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A2066DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
TS5A2066DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
TS5A2066YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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