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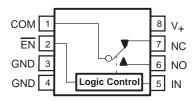
Description

The TS5A2053 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V_{+} can be transmitted in either direction.

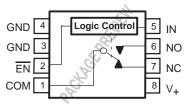
Applications

- Cell Phones
- Portable Audio Video Equipment
- Battery-Powered Equipment
- Low-Voltage Data-Acquisition Systems
- Test Equipment
- Communication Circuits

SSOP OR VSSOP PACKAGE (TOP VIEW)



YEP OR YZP PACKAGE (BOTTOM VIEW)



FUNCTION TABLE

EN	IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	L	ON	OFF
L	Н	OFF	ON
Н	Х	OFF	OFF

Features

- Low ON-State Resistance (10 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

Summary of Characteristics

 $V_{\perp} = 5 \text{ V and } T_{\Delta} = 25 \,^{\circ}\text{C}$

Configuration	Single Pole Double Throw (SPDT)
Number of channels	1
ON-state resistance (ron)	7.5 Ω
ON-state resistance match (Δr _{ON})	0.8 Ω
ON-state resistance flatness (ron(flat))	1.7 Ω
Turn-on/turn-off time (tON/tOFF)	6.8 ns/4.1 ns
Charge injection (Q _C)	3 pC
Bandwidth (BW)	330 MHz
OFF isolation (OISO)	-64 dB at 10 MHz
Crosstalk (XTALK)	-68 dB at 10 MHz
Total harmonic distortion (THD)	0.01%
Leakage current (ICOM(OFF))	±10 nA
Power-supply current (I ₊)	0.1 μΑ
Package options	8-pin DSBGA, SSOP, or VSSOP



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ORDERING INFORMATION

TA	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Townson	TS5A2053YEPR	
-40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	TS5A2053YZPR	
	SSOP - DCT	Tape and reel	TS5A2053DCTR	JAF
	VSSOP - DCU	Tape and reel	TS5A2053DCUR	JAF_

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Absolute Minimum and Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
٧+	Supply voltage range(3)		-0.5	6.5	V
V _{NO} V _{NC} V _{COM}	Analog voltage range(3)(4)(5)		-0.5	V ₊ + 0.5	V
lΚ	Analog port diode current	V_{NC} , V_{NO} , $V_{COM} < 0$ or V_{NO} , V_{NC} , $V_{COM} > V_{+}$	-50	50	mA
INO INC ICOM	On-state switch current	V_{NC} , V_{NO} , $V_{COM} = 0$ to V_{+}	-50	50	mA
VI	Digital input voltage range(3)(4)		-0.5	6.5	V
lıK	Digital input clamp current	V _I < 0	-50		mA
I ₊	Continuous current through V+			100	mA
IGND	Continuous current through GND		-100		mA
		DCT package		220	
θJΑ	Package thermal impedance(6)	DCU package		227	°C/W
		YEP/YZP package		102	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

⁽²⁾ DCT. The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

⁽²⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

⁽³⁾ All voltages are with respect to ground, unless otherwise specified.

⁽⁴⁾ The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽⁵⁾ This value is limited to 5.5 V maximum.

⁽⁶⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



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Electrical Characteristics for 5-V Supply⁽¹⁾ $V_+ = 4.5 \text{ V}$ to 5.5 V, $T_A = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITI	ONS	TA	٧+	MIN	TYP	MAX	UNIT
Analog Switch	•				•				
Analog signal range	V _{COM} , V _{NO} , V _{NC}					0		٧+	V
ON-state resistance	-	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$	Switch ON,	25°C	4.5 V		7.5	13.8	Ω
ON-State resistance	r _{on}	$I_{COM} = -32 \text{ mA},$	See Figure 13	Full	4.5 V			16	52
ON-state resistance		V _{NO} or V _{NC} = 3.15 V,	Switch ON,	25°C			0.8		_
match between channels	$\Delta r_{\sf on}$	$I_{COM} = -32 \text{ mA},$	See Figure 13	Full	4.5 V			4.5	Ω
ON-state resistance		$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$	Switch ON,	25°C	451/		1.7		0
flatness	ron(flat)	$I_{COM} = -32 \text{ mA},$	See Figure 13	Full	4.5 V			4.5	Ω
NO, NC	I _{NO(OFF)} ,	V _{NO} or V _{NC} = 1 V, V _{COM} = 4.5 V,	Switch OFF,	25°C		-100	5	100	
OFF leakage current	INC(OFF)	or V _{NO} or V _{NC} = 4.5 V, V _{COM} = 1 V,	See Figure 14	Full	5.5 V	-200		200	nA
СОМ		V _{COM} = 1 V, V _{NO} or V _{NC} = 4.5 V,	Switch OFF,	25°C	5.5.1/	-100	-1	100	- A
OFF leakage current	ICOM(OFF)	or V _{COM} = 4.5 V, V _{NO} or V _{NC} = 1 V,	See Figure 14	Full	5.5 V	-200		200	nA
NO, NC	I _{NO(ON),}	V _{NO} = 1 V, V _{COM} = Open,	Switch ON,	25°C		-100	5.5	100	
ON leakage current	INC(ON)	or V _{NO} = 4.5 V, V _{COM} = Open,	See Figure 15	Full	5.5 V	-200		200	nA
СОМ		V _{COM} = 1 V, V _{NO} or V _{NC} = Open,	Switch ON,	25°C	551/	-100	-1	100	
ON leakage current	ICOM(ON)	or V _{COM} = 4.5 V, V _{NO} or V _{NC} = Open,	See Figure 15	Full	5.5 V	-200		200	nA
Digital Control Input	s (IN, EN)				_	_			
Input logic high	VIH			Full		V ₊ × 0.7		5.5	V
Input logic low	V _{IL}			Full		0		$V_{+} \times 0.3$	V
Input leakage	lu e lu	V ₁ = 5.5 V or 0		25°C	551/	-0.1	0.05	0.1	^
current	¹IH, ¹IL	$V_{I} = 5.5 \text{ V or } 0$		Full	5.5 V	-1		1	μΑ

⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



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Electrical Characteristics for 5-V Supply⁽¹⁾ (continued) $V_+ = 4.5 \text{ V to } 5.5 \text{ V}, T_A = -40 ^{\circ}\text{C to } 85 ^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST COND	DITIONS	TA	V ₊	MIN	TYP	MAX	UNIT
Dynamic	•								
Turn-on time	4	V _{COM} = 3 V,	C _L = 35 pF,	25°C	5 V	3.8	5.3	6.8	20
Turr-on time	tON	$R_L = 300 \Omega$,	See Figure 17	Full	4.5 V to 5.5 V	3		7.1	ns
Turn-off time	tOFF	V _{COM} = 3 V,	$C_L = 35 \text{ pF},$	25°C	5 V	0.8	1.9	4.1	ns
	OFF	$R_L = 300 \Omega$	See Figure 17	Full	4.5 V to 5.5 V	0.4		4.5	110
Charge injection	QC	V _{GEN} = 0, R _{GEN} = 0,	C _L = 0.1 nF, See Figure 21	25°C	5 V		3		рС
NO, NC OFF capacitance	C _{NO(OFF)} , C _{NC(OFF)}	V_{NO} or $V_{NC} = V_{+}$ or GND, Switch OFF,	See Figure 16	25°C	5 V		6		pF
COM OFF capacitance	CCOM(OFF)	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	5 V		9.5		pF
NO, NC ON capacitance	C _{NO(ON)} , C _{NC(ON)}	V_{NO} or $V_{NC} = V_{+}$ or GND, Switch ON,	See Figure 16	25°C	5 V		18		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 16	25°C	5 V		18		pF
Digital input capacitance	Cl	$V_I = V_+ \text{ or GND},$	See Figure 16	25°C	5 V		2.5		pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See Figure 18	25°C	5 V		330		MHz
OFF isolation	O _{ISO}	$R_L = 50 \Omega$, f = 10 MHz,	Switch OFF, See Figure 19	25°C	5 V		-64		dB
Crosstalk	X _{TALK}	$R_L = 50 \Omega$, f = 10 MHz,	Switch ON, See Figure 20	25°C	5 V		-68		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 22	25°C	5 V		0.01		%
Supply				•					
Positive supply current	1+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C Full	5.5 V		0.1	1 5	μА

⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



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Electrical Characteristics for 3.3-V Supply⁽¹⁾ $V_+ = 3 \text{ V to } 3.6 \text{ V}, T_A = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C} \text{ (unless otherwise noted)}$

PARAMETER	SYMBOL	TEST CONDITIONS	3	TA	٧+	MIN	TYP	MAX	UNIT
Analog Switch				•					
Analog signal range	V _{COM} , V _{NO} , V _{NC}					0		V ₊	٧
ON-state resistance	r _{on}	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$ $I_{COM} = -24 \text{ mA},$	Switch ON, See Figure 13	25°C Full	3 V		13.2	20	Ω
ON-state resistance match	Δr _{on}	V_{NO} or $V_{NC} = 2.1 \text{ V}$,	Switch ON,	25°C	3 V		1		Ω
between channels	1.01	$I_{COM} = -24 \text{ mA},$	See Figure 13	Full				5.5	
ON-state resistance flatness	ron(flat)	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$ $I_{COM} = -24 \text{ mA},$	Switch ON, See Figure 13	25°C Full	3 V		5.3	11	Ω
NO, NC	INO(OFF),	V_{NO} or $V_{NC} = 1$ V, $V_{COM} = 3$ V,	Switch OFF,	25°C		-100	4	100	
OFF leakage current	INC(OFF)	V_{NO} or $V_{NC} = 3 \text{ V}$, $V_{COM} = 1 \text{ V}$,	See Figure 14	Full	3.6 V	-200		200	nA
COM OFF leakage	loor vorm	$V_{COM} = 1 \text{ V}, V_{NO} \text{ or } V_{NC} = 3 \text{ V},$	Switch OFF,	25°C	3.6 V	-100	-1	100	24
current	ICOM(OFF)	$V_{COM} = 3 \text{ V}, V_{NO} \text{ or } V_{NC} = 1 \text{ V},$	See Figure 14	Full	3.0 V	-200		200	nA
NO, NC	INO(ON),	V_{NO} or $V_{NC} = 1 \text{ V}$, $V_{COM} = \text{Open}$,	Switch ON,	25°C	3.6 V	-100	4.5	100	nA
ON leakage current	INC(ON)	V_{NO} or $V_{NC} = 3 \text{ V}$, $V_{COM} = \text{Open}$,	See Figure 15	Full	3.0 V	-200		200	ПА
COM		$V_{COM} = 1 V$, V_{NO} or $V_{NC} = Open$,	Switch ON,	25°C	0.01/	-100	-1	100	
ON leakage current	ICOM(ON)	$V_{COM} = 3 \text{ V}, V_{NO} \text{ or } V_{NC} = \text{Open},$	See Figure 15	Full	3.6 V	-200		200	nA
Digital Control Inpu	ts (IN, EN)								
Input logic high	VIH			Full		$V_{+} \times 0.7$		5.5	>
Input logic low	V _{IL}		·	Full		0		$V_{+} \times 0.3$	V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C Full	3.6 V	-0.1 -1	0.05	0.1	μΑ

⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



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Electrical Characteristics for 3.3-V Supply⁽¹⁾ (continued) $V_+ = 3 \text{ V to } 3.6 \text{ V}, T_A = -40^{\circ}\text{C to}$ 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST COND	OITIONS	TA	٧+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	tON	V _{COM} = 2 V,	C _L = 35 pF,	25°C	3.3 V	5	6.4	7.9	ns
	*ON	$R_L = 300 \Omega$	See Figure 17	Full	3 V to 3.6 V	4.5		8.2	110
Turn-off time	torr	$V_{COM} = 2 V$	$C_L = 35 pF$,	25°C	3.3 V	1.1	2.4	4.7	ns
Tarri on timo	tOFF	$R_L = 300 \Omega$,	See Figure 17	Full	3 V to 3.6 V	0.3		5	113
Charge injection	QC	V _{GEN} = 0, R _{GEN} = 0,	$C_L = 0.1 \text{ nF},$ See Figure 21	25°C	3.3 V		1		рС
NO, NC OFF capacitance	C _{NO(OFF)}	V_{NO} or $V_{NC} = V_{+}$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		6		pF
COM OFF capacitance	CCOM(OFF)	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		9.5		pF
NO, NC ON capacitance	C _{NO(ON)}	V_{NO} or $V_{NC} = V_{+}$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		18.5		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 16	25°C	3.3 V		18.5		pF
Digital input capacitance	Cl	$V_I = V_+ \text{ or GND},$	See Figure 16	25°C	3.3 V		3		pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See Figure 18	25°C	3.3 V		320		MHz
OFF isolation	O _{ISO}	$R_L = 50 \Omega$, f = 10 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		-64		dB
Crosstalk	XTALK	$R_L = 50 \Omega$, f = 10 MHz,	Switch ON, See Figure 20	25 °C	3.3 V		-68		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 22	25°C	3.3 V		0.035		%
Supply	•								
Positive supply current	I ₊	$V_I = V_+ \text{ or GND},$	Switch ON or OFF	25°C Full	3.6 V		0.1	1 5	μΑ

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Electrical Characteristics for 2.5-V Supply⁽¹⁾ $V_+ = 2.3 \text{ V to } 2.7 \text{ V, T}_A = -40 ^{\circ}\text{C}$ to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDIT	IONS	TA	٧+	MIN	TYP	MAX	UNIT
Analog Switch	1								
Analog signal range	V _{COM} , V _{NO} , V _{NC}					0		V ₊	V
ON-state resistance	r _{on}	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$ $I_{COM} = -8 \text{ mA},$	Switch ON, See Figure 13	25°C Full	2.3 V		20	40	Ω
ON-state resistance match between channels	Δr _{on}	V_{NO} or $V_{NC} = 1.6 \text{ V}$, $I_{COM} = -8 \text{ mA}$,	Switch ON, See Figure 13	25°C Full	2.3 V		1.1	6	Ω
ON-state resistance flatness	ron(flat)	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$ $I_{COM} = -8 \text{ mA},$	Switch ON, See Figure 13	25°C Full	2.3 V		15	20	Ω
NO, NC	INO(OFF),	V _{NO} or V _{NC} = 0.5 V, V _{COM} = 2.2 V,	Switch OFF,	25°C		-100	3.5	100	
OFF leakage current	INC(OFF)	or V _{NO} or V _{NC} = 2.2 V, V _{COM} = 0.5 V,	See Figure 14	Full	2.7 V	-200		200	nA
COM	loovyour	V _{COM} = 0.5 V, V _{NO} or V _{NC} = 2.2 V, or	Switch OFF,	25°C	2.7 V	-100	-2	100	nA
OFF leakage current	ICOM(OFF)	V _{COM} = 2.2 V, V _{NO} or V _{NC} = 0.5 V,	See Figure 14	Full	Z.7 V	-200		200	IIA
NO, NC	I _{NO(ON),}	V _{NO} or V _{NC} = 0.5 V, V _{COM} = Open,	Switch ON,	25°C	2.7 V	-100	4	100	nA
ON leakage current	INC(ON)	V _{NO} or V _{NC} = 2.2 V, V _{COM} = Open,	See Figure 15	Full	Z.1 V	-200		200	
COM	loor worn	V _{COM} = 0.5 V, V _{NO} or V _{NC} = Open, or	Switch ON,	25°C	2.7 V	-100	-2	100	nA
ON leakage current	ICOM(ON)	V _{COM} = 2.2 V, V _{NO} or V _{NC} = Open,	See Figure 15	Full	2.7 V	-200		200	IIA
Digital Control Input	s (IN, EN)								
Input logic high	VIH			Full		V ₊ ×0.7		5.5	V
Input logic low	V _{IL}			Full		0		$V_{+} \times 0.3$	V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C Full	2.7 V	-0.1 -1	0.05	0.1	μА

⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



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Electrical Characteristics for 2.5-V Supply⁽¹⁾ (continued) $V_+ = 2.3 \text{ V to } 2.7 \text{ V}, T_A = -40 ^{\circ}\text{C}$ to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDI	ITIONS	TA	V ₊	MIN	TYP	MAX	UNIT
Dynamic	•								
Turn-on time		V _{COM} = 1.5 V,	C _L = 35 pF,	25°C	2.5 V	5.9	7.1	9.3	
rum-on ume	tON	$R_L = 300 \Omega$,	See Figure 17	Full	2.3 V to 2.7 V	5.1		10	ns
Turn-off time	torr	V _{COM} = 1.5 V,	$C_L = 35 pF$,	25°C	2.5 V	2.1	3.2	5.1	ns
	tOFF	$R_L = 300 \Omega$,	See Figure 17	Full	2.3 V to 2.7 V	1.2		5.2	113
Charge injection	QC	V _{GEN} = 0, R _{GEN} = 0	$C_L = 0.1 \text{ nF},$ See Figure 21	25°C	2.5 V		0.5		рC
NO, NC OFF capacitance	C _{NO(OFF)} C _{NC(OFF)}	V_{NO} or $V_{NC} = V_{+}$ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		6.5		pF
COM OFF capacitance	CCOM(OFF)	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		10		pF
NO, NC ON capacitance	C _{NO(ON)}	V_{NO} or $V_{NC} = V_{+}$ or GND, Switch ON,	See Figure 16	25°C	2.5 V		18.5		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 16	25°C	2.5 V		18.5		pF
Digital input capacitance	Cl	$V_I = V_+$ or GND,	See Figure 16	25°C	2.5 V		3		pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See Figure 18	25°C	2.5 V		320		MHz
OFF isolation	O _{ISO}	$R_L = 50 \Omega$, f = 10 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		-64		dB
Crosstalk	XTALK	$R_L = 50 \Omega$, f = 10 MHz,	Switch ON, See Figure 20	25 °C	2.5 V		-68		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 22	25°C	2.5 V		0.26		%
Supply									
Positive supply current	I ₊	$V_I = V_+$ or GND,	Switch ON or OFF	25°C Full	2.7 V		0.1	1 5	μΑ

⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



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Electrical Characteristics for 1.8-V Supply⁽¹⁾ $V_+ = 1.65 \text{ V}$ to 1.95 V, $T_A = -40 ^{\circ}\text{C}$ to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIO	NS	T_{A}	٧+	MIN	TYP	MAX	UNIT
Analog Switch					•				
Analog signal range	VCOM, VNO, VNC					0		٧+	V
ON-state resistance	r _{on}	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$ $I_{COM} = -4 \text{ mA},$	Switch ON, See Figure 13	25°C Full	1.65 V		85	120	Ω
ON-state resistance match	Δr _{on}	V _{NO} or V _{NC} = 1.15 V, I _{COM} = -4 mA,	Switch ON, See Figure 13	25°C	1.65 V		2		Ω
between channels				Full			70	7.5	
ON-state resistance flatness	ron(flat)	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$ $I_{COM} = -4 \text{ mA},$	Switch ON, See Figure 13	25°C Full	1.65 V		76	100	Ω
NO, NC	INO(OFF),	V _{NO} or V _{NC} = 0.3 V, V _{COM} = 1.65 V,	Switch OFF,	25°C	4.05.1/	-100	3.5	100	
OFF leakage current	INC(OFF)	or V _{NO} or V _{NC} = 1.65 V, V _{COM} = 0.3 V,	See Figure 14	Full	1.95 V	-200		200	nA
COM		$V_{COM} = 0.3 \text{ V}, V_{NO} = 1.65 \text{ V},$	Switch OFF,	25°C		-100	1	100	
OFF leakage current	ICOM(OFF)	$V_{COM} = 1.65 \text{ V}, V_{NO} = 0.3 \text{ V},$	See Figure 14	Full	1.95 V	-200		200	nA
NO, NC	I _{NO(ON),}	V _{NO} or V _{NC} = 0.3 V, V _{COM} = Open, or	Switch ON,	25°C	1.95 V	-100	4	100	nA
ON leakage current	INC(ON)	V _{NO} or V _{NC} = 1.65 V, V _{COM} = Open,	See Figure 15	Full	1.95 V	-200		200	
СОМ		$V_{COM} = 0.3 \text{ V},$ $V_{NO} \text{ or } V_{NC} = \text{Open},$	Switch ON,	25°C	4.05.1/	-100	1	100	^
ON leakage current	ICOM(ON)	or V _{COM} = 1.65 V, V _{NO} or V _{NC} = Open,	See Figure 15	Full	1.95 V	-200		200	nA
Digital Control Input	ts (IN, EN)								
Input logic high	VIH			Full		V ₊ × 0.65		5.5	V
Input logic low	VIL			Full		0		$V_{+} \times 0.35$	V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C Full	1.95 V	-0.1 -1	0.05	0.1	μА

⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



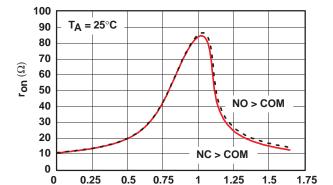
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Electrical Characteristics for 1.8-V Supply⁽¹⁾ (continued) $V_+ = 1.65 \text{ V}$ to 1.95 V, $T_A = -40 ^{\circ}\text{C}$ to $85 ^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST COND	DITIONS	TA	V ₊	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	ton	V _{COM} = 1.3 V,	C _L = 35 pF,	25°C	1.8 V	10.2	11.8	14.5	ns
Turr on time	tON	$R_L = 300 \Omega$,	See Figure 17	Full	1.65 V to 1.95 V	8.4		15.5	115
Turn-off time	tOFF	V _{COM} = 1.3 V,	C _L = 35 pF,	25°C	1.8 V	2.9	4.3	6.5	ns
Tarri on arrio	OFF	$R_L = 300 \Omega$	See Figure 17	Full	1.65 V to 1.95 V	2.2		7	113
Charge injection	QC	V _{GEN} = 0, R _{GEN} = 0	C _L = 0.1 nF, See Figure 21	25°C	1.8 V		0.5		рС
NO, NC OFF capacitance	C _{NO(OFF)} , C _{NC(OFF)}	V_{NO} or $V_{NC} = V_{+}$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		6.5		pF
COM OFF capacitance	CCOM(OFF)	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		10		pF
NO, NC ON capacitance	C _{NO(ON)} , C _{NC(ON)}	V_{NO} or $V_{NC} = V_{+}$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		19		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 16	25°C	1.8 V		14		pF
Digital input capacitance	Cl	$V_I = V_+$ or GND,	See Figure 16	25°C	1.8 V		3		pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See Figure 18	25°C	1.8 V		320		MHz
OFF isolation	O _{ISO}	$R_L = 50 \Omega$, $f = 10 MHz$,	Switch OFF, See Figure 19	25°C	1.8 V		-64		dB
Crosstalk	X _{TALK}	$R_L = 50 \Omega$, f = 10 MHz,	Switch ON, See Figure 20	25 °C	1.8 V		-68		dB
Total harmonic distortion	THD	$R_L = 10 \text{ k}\Omega,$ $C_L = 50 \text{ pF},$	f = 20 Hz to 20 kHz, See Figure 22	25°C	1.8 V		2.6		%
Supply	•								
Positive supply	I ₊	$V_1 = V_+$ or GND.	Switch ON or OFF	25°C	1.95 V		0.1	1	μА

⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE



 $V_{COM}(V)$ Figure 1A. r_{on} vs V_{COM} (V₊ = 1.65 V)

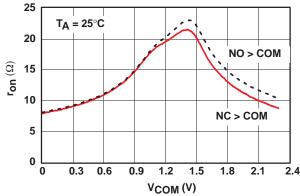


Figure 1B. r_{on} vs V_{COM} ($V_{+} = 2.3 \text{ V}$)

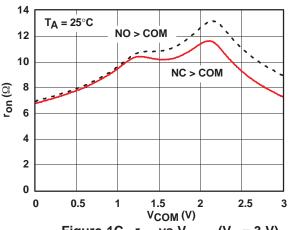


Figure 1C. r_{on} vs V_{COM} ($V_{+} = 3 V$)

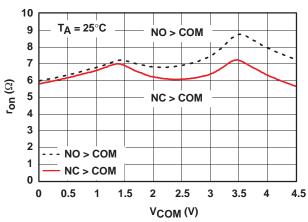


Figure 1D. r_{on} vs V_{COM} ($V_{+} = 4.5 \text{ V}$)

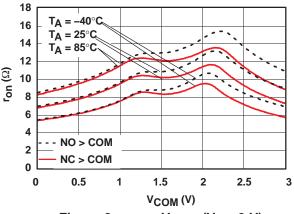


Figure 2. r_{on} vs V_{COM} ($V_{+} = 3 V$)

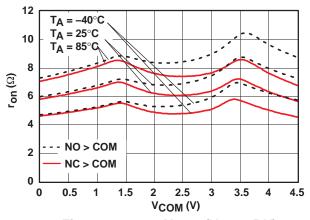


Figure 3. r_{on} vs V_{COM} ($V_{+} = 4.5 \text{ V}$)



TYPICAL PERFORMANCE (continued)

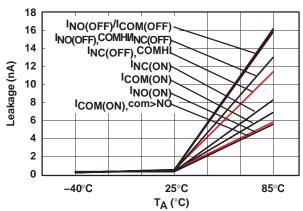


Figure 4. Leakage Current vs Temperature $(V_+ = 5.5 \text{ V})$

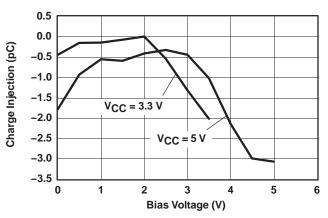


Figure 5. Charge Injection (Q_C) vs V_{COM}

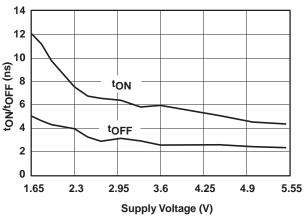


Figure 6. toN and toFF vs V+

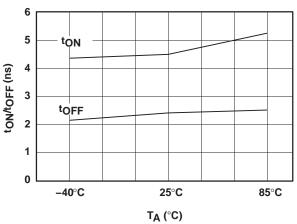


Figure 7. t_{ON} and t_{OFF} vs Temperature (V₊ = 5 V)

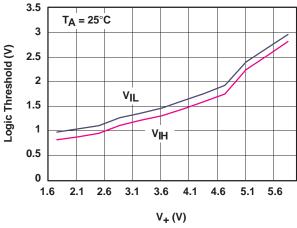


Figure 8. Logic Threshold vs V₊

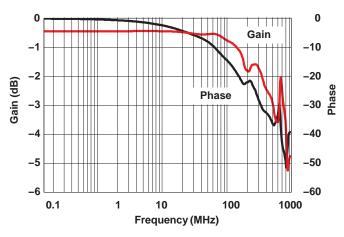
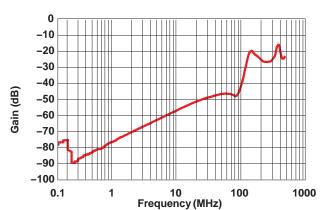


Figure 9. Bandwidth $(V_+ = 5 V)$

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TYPICAL PERFORMANCE (continued)



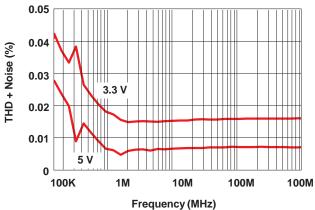


Figure 10. OFF Isolation $(V_+ = 5 V)$

Figure 11. Total Harmonic Distortion vs Frequency

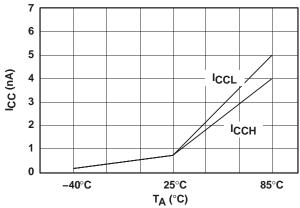


Figure 12. Power-Supply Current vs Temperature $(V_+ = 5 V)$

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PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	COM	Common
2	EN	Chip enable (active low)
3	GND	Digital ground
4	GND	Digital ground
5	IN	Digital control to connect COM to NC or NO
6	NO	Normally open
7	NC	Normally closed
8	٧+	Power supply

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
VCOM	Voltage at COM
V _{NC}	Voltage at NC
V _{NO}	Voltage at NO
r _{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{on}	Difference of r _{On} between channels in a specific device
ron(flat)	Difference between the maximum and minimum value of ron in a channel over the specified range of conditions
I _{NC} (OFF)	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
INO(OFF)	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
INC(ON)	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
ICOM(OFF)	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the OFF state and the output (NC or NO) open
ICOM(ON)	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
VIH	Minimum input voltage for logic high for the control input (IN, EN)
V _{IL}	Maximum input voltage for logic low for the control input (IN, EN)
VI	Voltage at the control input (IN, EN)
I _{IH} , I _{IL}	Leakage current measured at the control input (IN, EN)
tON	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
^t OFF	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.



$\begin{array}{c} \textbf{TS5A2053} \\ \textbf{SINGLE-CHANNEL 10-} \Omega \ \textbf{SPDT ANALOG SWITCH} \\ \textbf{WITH ENABLE} \end{array}$

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PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
C _{NC(OFF)}	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C _{NC(ON)}	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C _{COM(OFF)}	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is OFF
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
Cl	Capacitance of control input (IN, EN)
O _{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
XTALK	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is -3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic.
I ₊	Static power-supply current with the control (IN, EN) pin at V ₊ or GND



PARAMETER MEASUREMENT INFORMATION

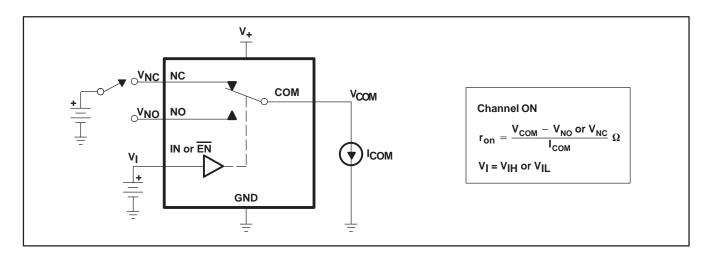


Figure 13. ON-State Resistance (ron)

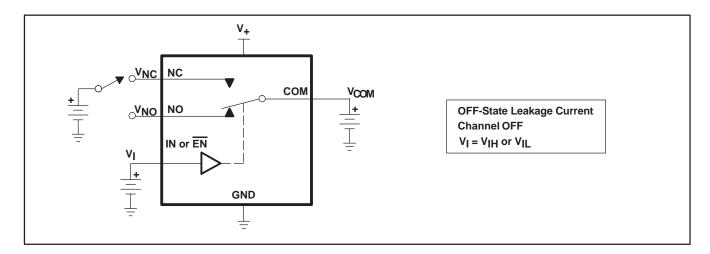


Figure 14. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{COM(OFF)}$)

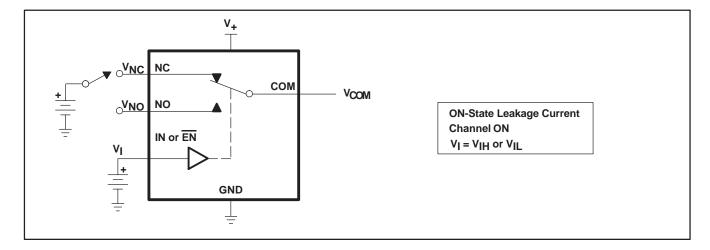
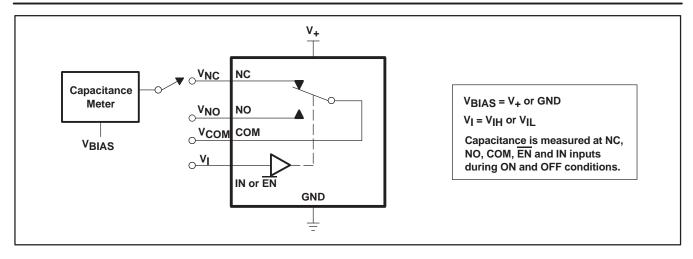
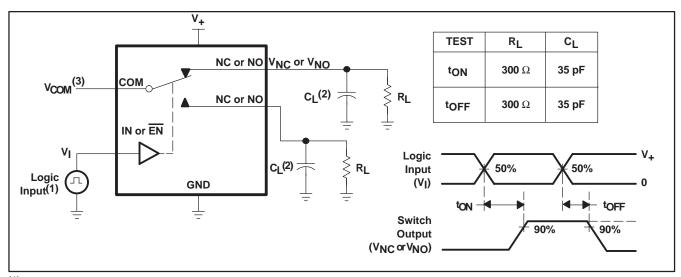


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)







- (1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- (2) C_L includes probe and jig capacitance.
- (3) See Electrical Characteristics for V_{COM}.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

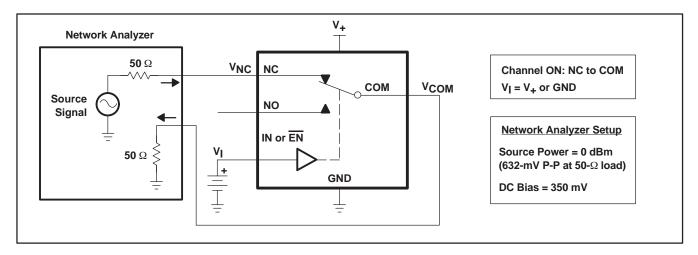


Figure 18. Bandwidth (BW)

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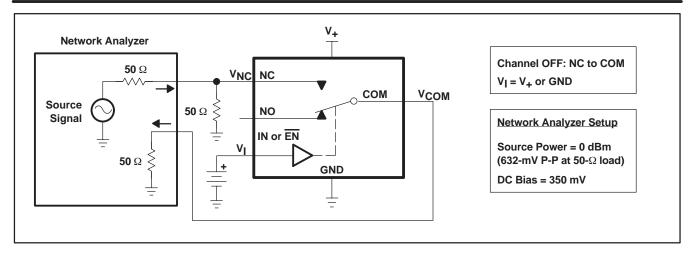


Figure 19. OFF Isolation (O_{ISO})

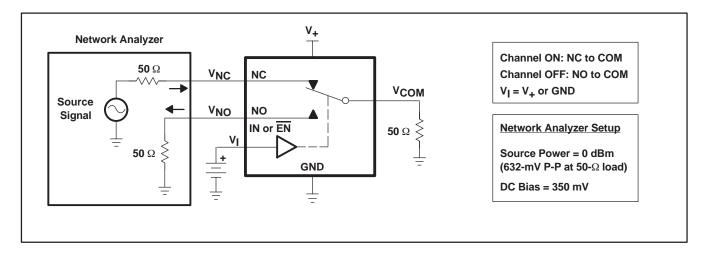
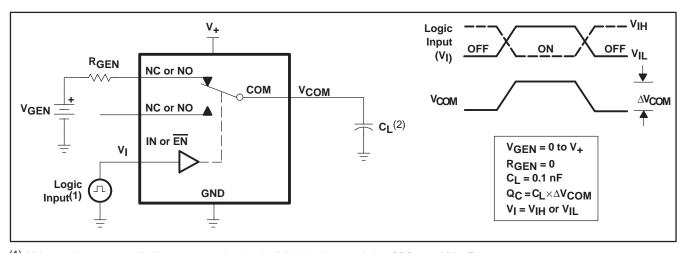


Figure 20. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f < 5$ ns.

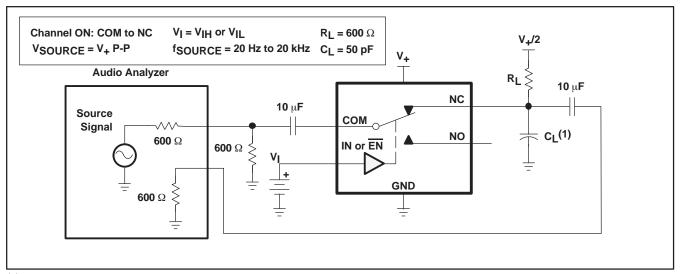
(2) C_L includes probe and jig capacitance.

Figure 21. Charge Injection (Q_C)

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WITH ENABLE



(1) C_L includes probe and jig capacitance.

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Figure 22. Total Harmonic Distortion (THD)

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(5)	(4)	(5)		(0)
TS5A2053DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAF (R, Z)
TS5A2053DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAF (R, Z)
TS5A2053DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(AF, JAFQ, JAFR) JZ
TS5A2053DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(AF, JAFQ, JAFR) JZ
TS5A2053DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAFR
TS5A2053DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAFR

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A2053DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
TS5A2053DCTR	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TS5A2053DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
TS5A2053DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3



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*All dimensions are nominal

7 III CHINICHOLO II CHININIA								
	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	TS5A2053DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
	TS5A2053DCTR	SSOP	DCT	8	3000	183.0	183.0	20.0
	TS5A2053DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
	TS5A2053DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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