

FEATURES

- Wide Bandwidth (BW = 900 MHz Typ)
- Low Crosstalk ($X_{TALK} = -41$ dB Typ)
- Low Bit-to-Bit Skew [$t_{sk(o)} = 0.2$ ns Max]
- Low and Flat ON-State Resistance
($r_{on} = 4 \Omega$ Typ, $r_{on(flat)} = 0.7 \Omega$ Typ)
- Low Input/Output Capacitance
($C_{ON} = 10$ pF Typ)
- Rail-to-Rail Switching on Data I/O Ports
(0 to 5 V)
- V_{DD} Operating Range From 3 V to 3.6 V
- I_{off} Supports Partial Power-Down-Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Suitable for 10-/100-/1000-Mbit Ethernet Signaling

APPLICATIONS

- 10/100/1000 Base-T Signal Switching
- Differential (LVDS, LVPECL) Signal Switching
- Digital Video Signal Routing
- Notebook Docking Signal Routing
- Hub and Router Signal Switching

DESCRIPTION/ORDERING INFORMATION

The TS3L301 is a 16-bit to 8-bit multiplexer/demultiplexer local area network (LAN) switch with a single select (SEL) input. The SEL input controls the data path of the multiplexer/demultiplexer.

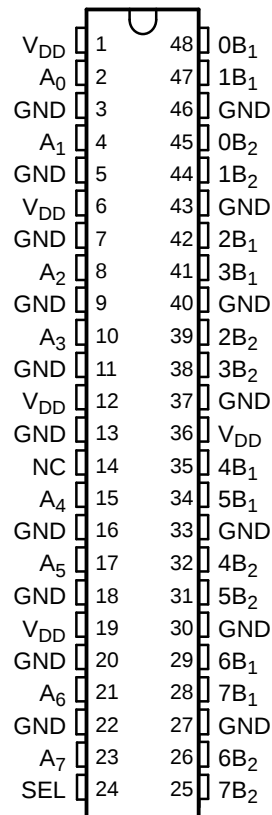
The device provides a low and flat ON-state resistance (r_{on}) and an excellent ON-state resistance match. Low input/output capacitance, high-bandwidth, low skew, and low crosstalk among channels make this device suitable for various LAN applications, such as 10/100/1000 Base-T.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	TS3L301DGGR	TS3L301
	TVSOP – DGV	Tape and reel	TS3L301DGVR	TK301

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DGG OR DGV PACKAGE
(TOP VIEW)



NC – No internal connection



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TS3L301

16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LOW AND FLAT ON-STATE RESISTANCE

SCDS178C–NOVEMBER 2004–REVISED APRIL 2006

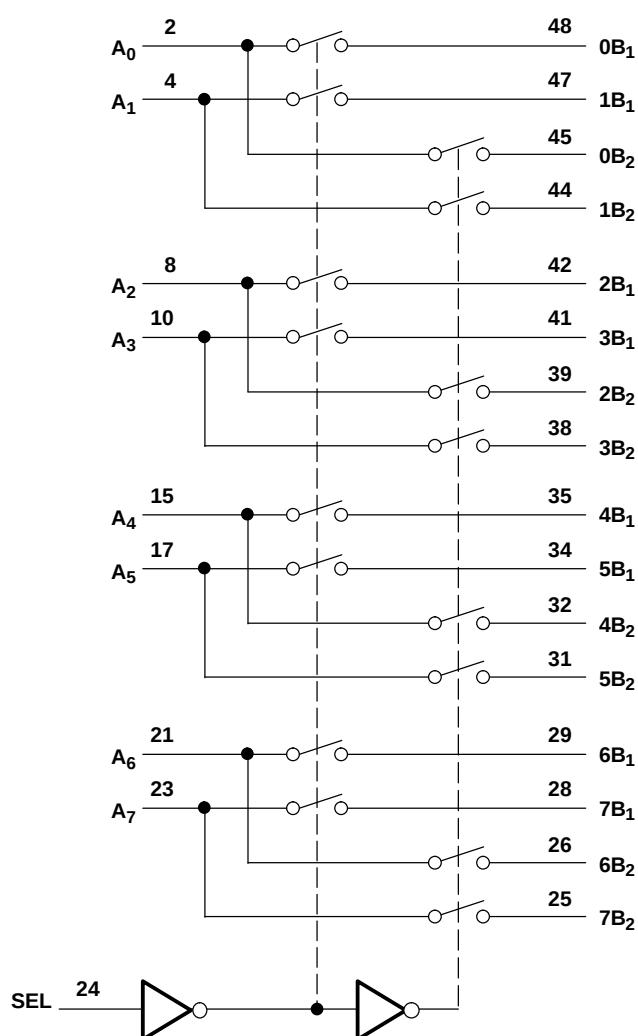
FUNCTION TABLE

INPUT SEL	INPUT/OUTPUT A_n	FUNCTION
L	nB_1	$A_n = nB_1$
H	nB_2	$A_n = nB_2$

PIN DESCRIPTION

NAME	DESCRIPTION
A_n	Data I/Os
nB_m	Data I/Os
SEL	Select input

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range	–0.5	4.6	V
V_{IN}	Control input voltage range ⁽²⁾⁽³⁾	–0.5	7	V
$V_{I/O}$	Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾	–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50 mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50 mA
$I_{I/O}$	ON-state switch current ⁽⁵⁾			±128 mA
	Continuous current through V_{DD} or GND			±100 mA
θ_{JA}	Package thermal impedance ⁽⁶⁾	DGG package		70 °C/W
		DGV package		58 °C/W
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.

(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage (SEL)	2	5.5	V
V_{IL}	Low-level control input voltage (SEL)	0	0.8	V
$V_{I/O}$	Input/output voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TS3L301

16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LOW AND FLAT ON-STATE RESISTANCE

SCDS178C – NOVEMBER 2004 – REVISED APRIL 2006

Electrical Characteristics

for 1000 Base-T Ethernet switching over recommended operating free-air temperature range, $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$
(unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}	SEL	$V_{DD} = 3.6 \text{ V}$,	$I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{IH}	SEL	$V_{DD} = 3.6 \text{ V}$,	$V_{IN} = V_{DD}$			± 1	μA
I_{IL}	SEL	$V_{DD} = 3.6 \text{ V}$,	$V_{IN} = \text{GND}$			± 1	μA
I_{off}		$V_{DD} = 0$,	$V_O = 0 \text{ to } 3.6 \text{ V}$,			1	μA
I_{DD}		$V_{DD} = 3.6 \text{ V}$,	$I_{IO} = 0$,		250	600	μA
C_{IN}	SEL	$f = 1 \text{ MHz}$,	$V_{IN} = 0$		2.5	3	pF
C_{OFF}	B port	$V_I = 0$,	$f = 1 \text{ MHz}$,		3.5	4	pF
C_{ON}		$V_I = 0$,	$f = 1 \text{ MHz}$,		10	10.9	pF
r_{on}		$V_{DD} = 3 \text{ V}$,	$1.5 \text{ V} \leq V_I \leq V_{DD}$,		4	8	Ω
$r_{on(flat)}^{(3)}$		$V_{DD} = 3 \text{ V}$,	$V_I = 1.5 \text{ V}$ and V_{DD} ,		0.7		Ω
$\Delta r_{on}^{(4)}$		$V_{DD} = 3 \text{ V}$,	$1.5 \text{ V} \leq V_I \leq V_{DD}$,		0.2	1.2	Ω

- (1) V_I , V_O , I_I , and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at $V_{DD} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from center (A_4 , A_5) ports to any other port.

Electrical Characteristics

for 10/100 Base-T Ethernet switching over recommended operating free-air temperature range, $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$
(unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}	SEL	$V_{DD} = 3.6 \text{ V}$,	$I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{IH}	SEL	$V_{DD} = 3.6 \text{ V}$,	$V_{IN} = V_{DD}$			± 1	μA
I_{IL}	SEL	$V_{DD} = 3.6 \text{ V}$,	$V_{IN} = \text{GND}$			± 1	μA
I_{off}		$V_{DD} = 0$,	$V_O = 0 \text{ to } 3.6 \text{ V}$,			1	μA
I_{DD}		$V_{DD} = 3.6 \text{ V}$,	$I_{IO} = 0$,		250	600	μA
C_{IN}	SEL	$f = 1 \text{ MHz}$,	$V_{IN} = 0$		2.5	3	pF
C_{OFF}	B port	$V_I = 0$,	$f = 1 \text{ MHz}$,		3.5	4	pF
C_{ON}		$V_I = 0$,	$f = 1 \text{ MHz}$,		10	10.9	pF
r_{on}		$V_{DD} = 3 \text{ V}$,	$1.25 \text{ V} \leq V_I \leq V_{DD}$,		4	8	Ω
$r_{on(flat)}^{(3)}$		$V_{DD} = 3 \text{ V}$,	$V_I = 1.25 \text{ V}$ and V_{DD} ,		0.7		Ω
$\Delta r_{on}^{(4)}$		$V_{DD} = 3 \text{ V}$,	$1.25 \text{ V} \leq V_I \leq V_{DD}$,		0.2	1.2	Ω

- (1) V_I , V_O , I_I , and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at $V_{DD} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from center (A_4 , A_5) ports to any other port.

Switching Characteristics

over recommended operating free-air temperature range, $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $R_L = 200 \, \Omega$, $C_L = 10 \text{ pF}$
(unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
$t_{pd}^{(2)}$	A or B	B or A		0.25		ns
t_{pZH} , t_{pZL}	SEL	A or B	1.5		11.5	ns
t_{pHZ} , t_{pLZ}	SEL	A or B	1		8.5	ns
$t_{sk(o)}^{(3)}$	A or B	B or A		0.1	0.2	ns
$t_{sk(p)}^{(4)}$				0.1	0.2	ns

(1) All typical values are at $V_{DD} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

(3) Output skew between center port (A_4 to A_5) to any other port

(4) Skew between opposite transitions of the same output in a given device $|t_{pHL} - t_{pLH}|$

Dynamic Characteristics

over recommended operating free-air temperature range, $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP ⁽¹⁾	UNIT
X_{TALK}	$R_L = 100 \, \Omega$,	$f = 250 \text{ MHz}$,	See Figure 7	–41	dB
O_{IRR}	$R_L = 100 \, \Omega$,	$f = 250 \text{ MHz}$,	See Figure 8	–39	dB
BW	$R_L = 100 \, \Omega$,	See Figure 6		900	MHz

(1) All typical values are at $V_{DD} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

OPERATING CHARACTERISTICS

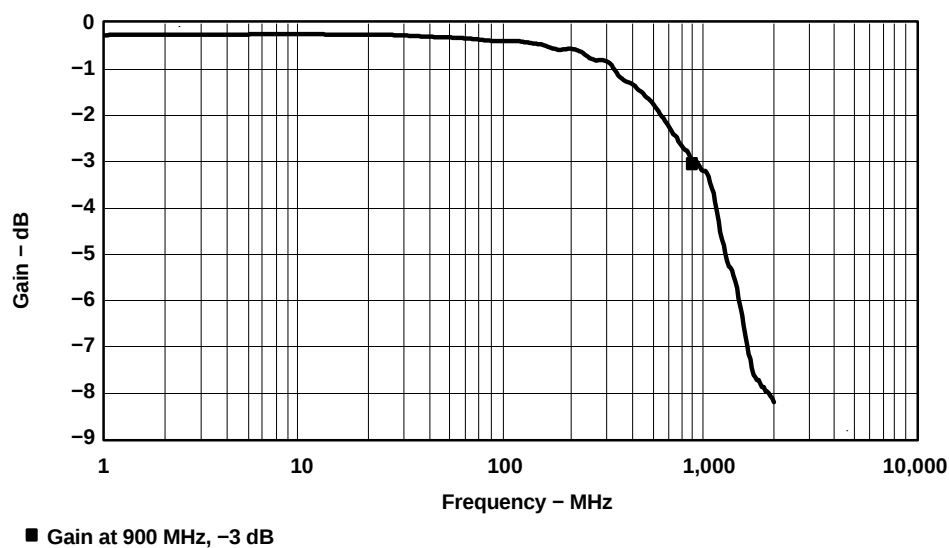


Figure 1. Gain vs Frequency

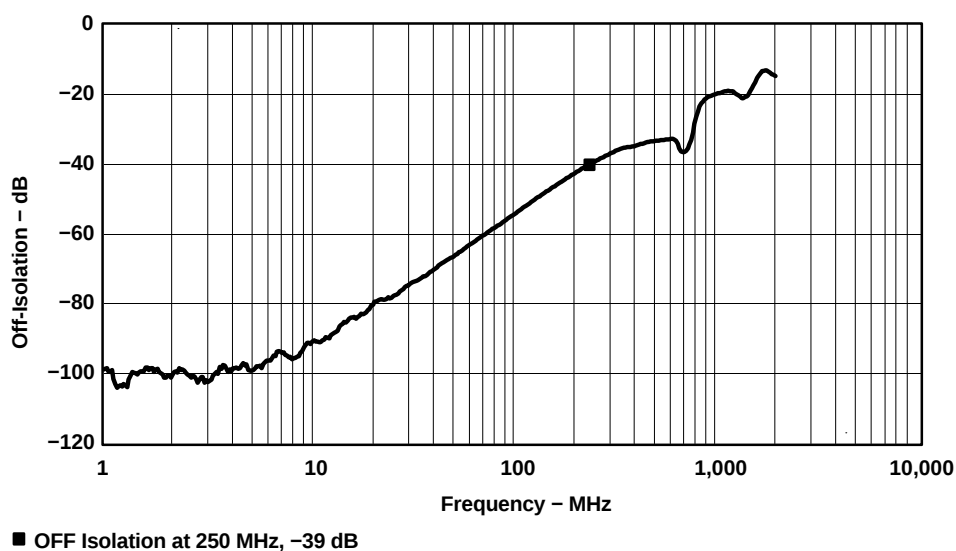


Figure 2. OFF Isolation vs Frequency

OPERATING CHARACTERISTICS (continued)

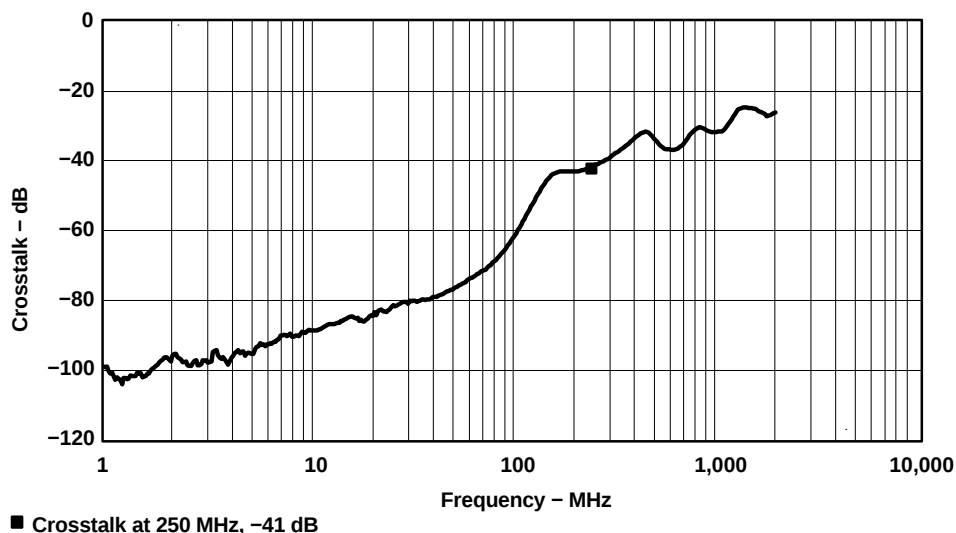
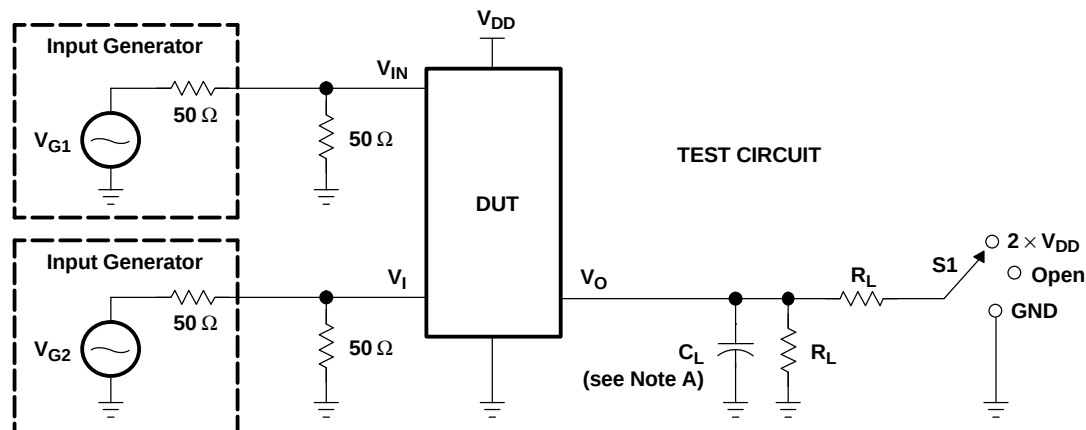
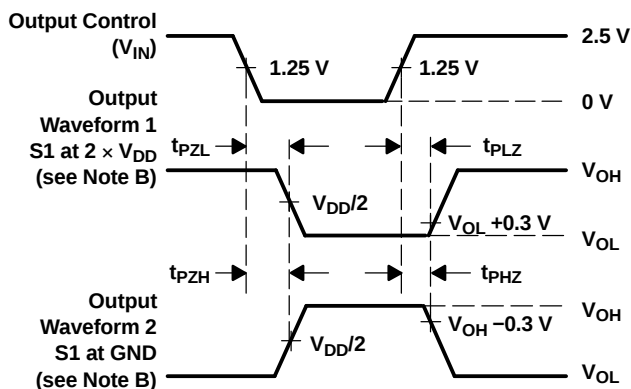


Figure 3. Crosstalk vs Frequency

PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	V _{DD}	S1	R _L	V _I	C _L	V _Δ
t _{PLZ} /t _{PZL}	3.3 V ± 0.3 V	2 × V _{DD}	200 Ω	GND	10 pF	0.3 V
t _{PHZ} /t _{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V _{DD}	10 pF	0.3 V

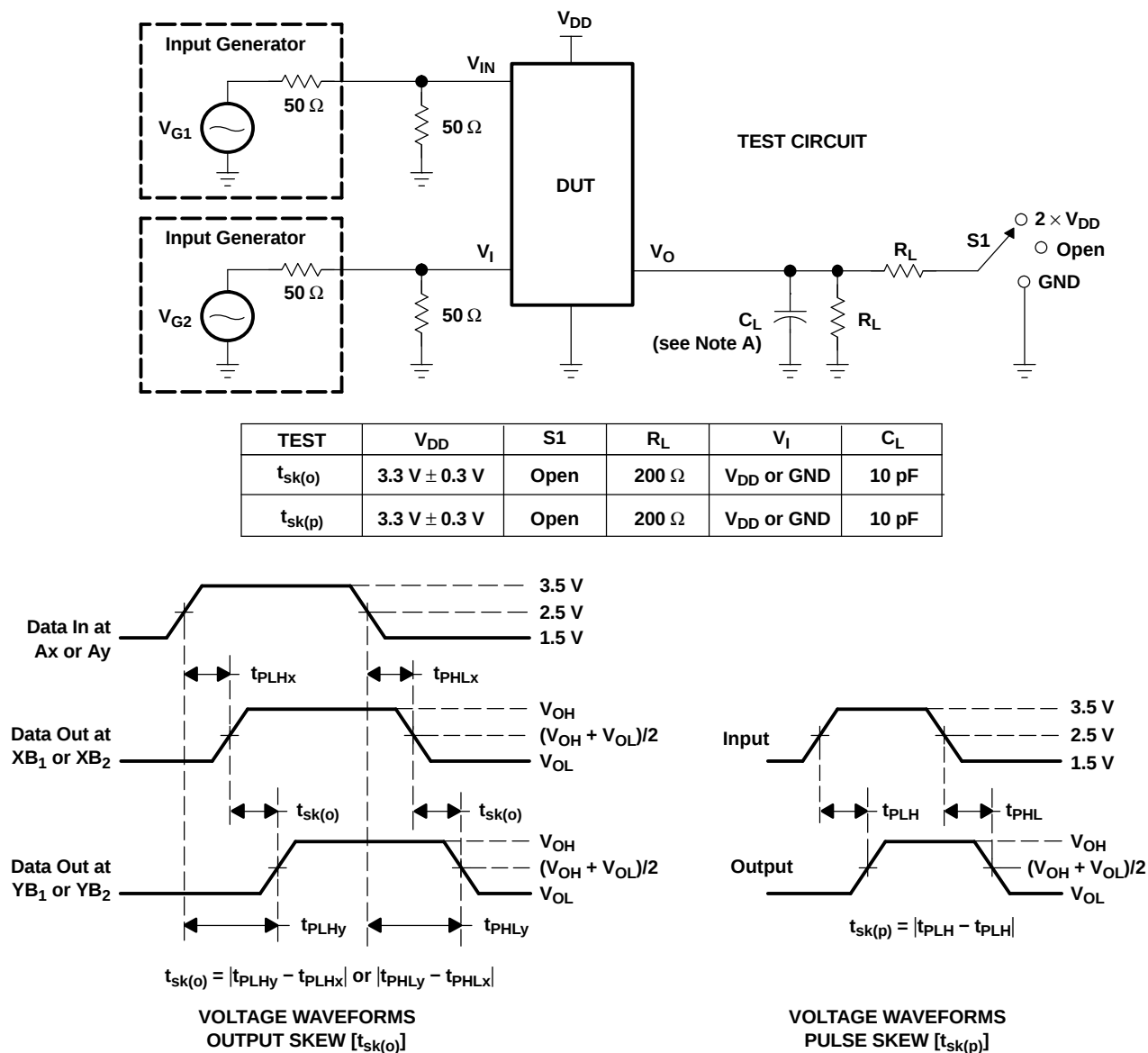


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 4. Test Circuit and Voltage Waveforms

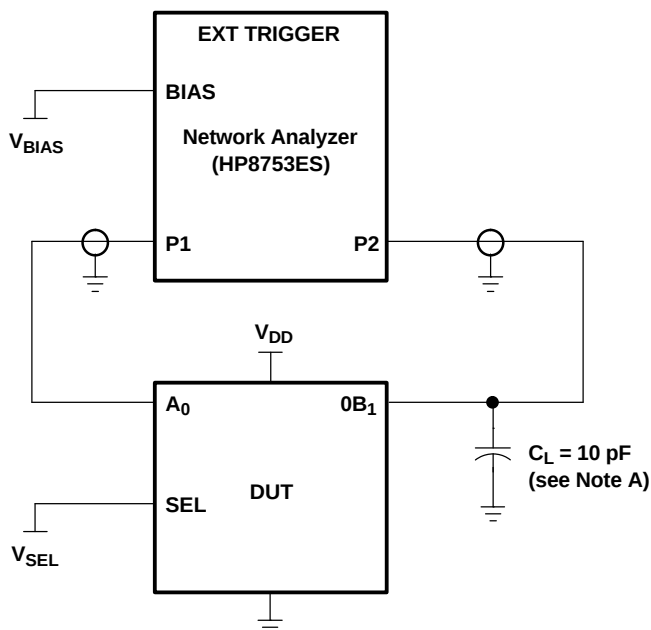
PARAMETER MEASUREMENT INFORMATION
(Skew)



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

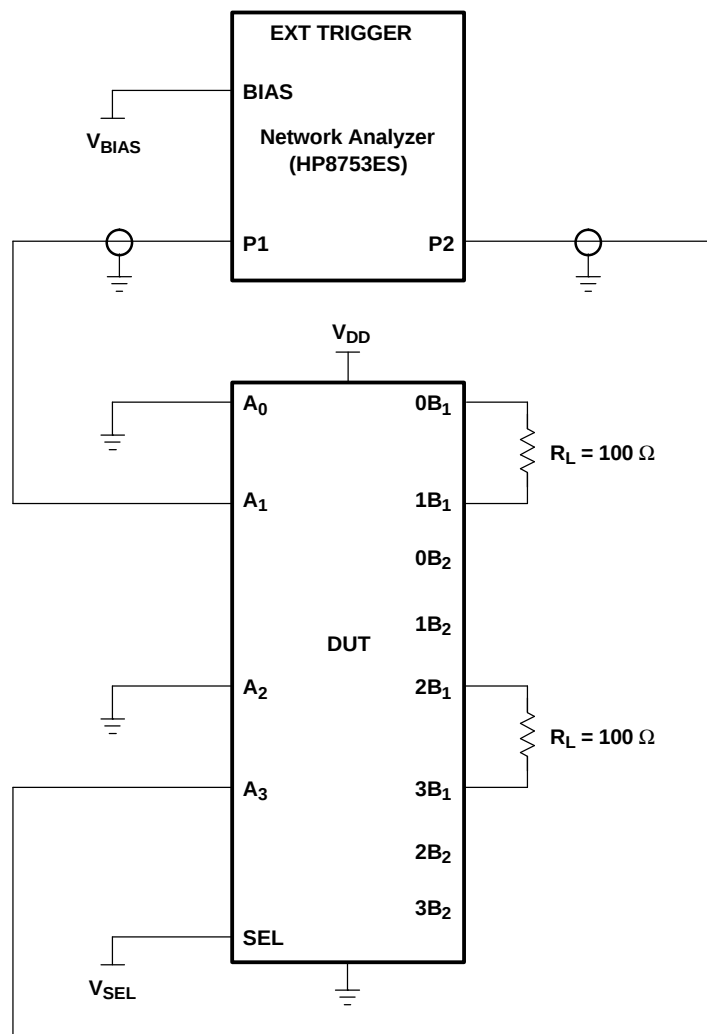
Figure 6. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_{SEL} = 0$ and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
ST = 2 s
P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

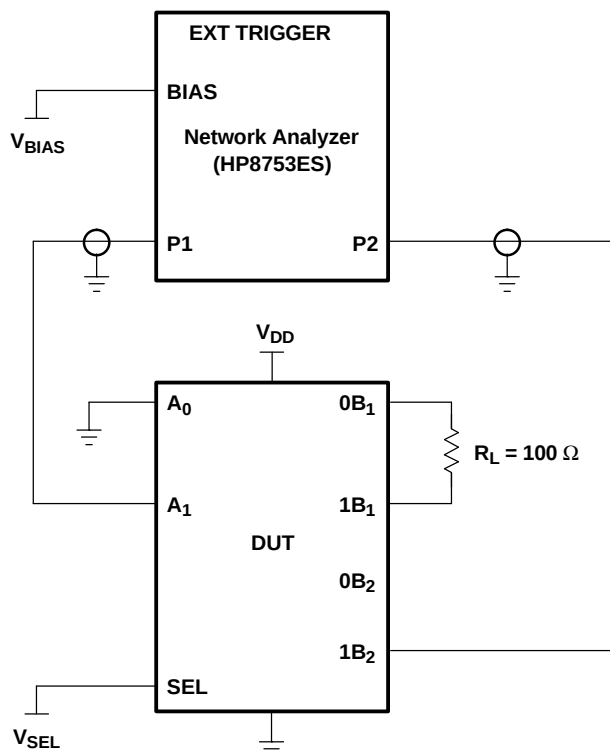
Figure 7. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{SEL} = 0$ and A_1 is the input, the output is measured at A_3 . All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
ST = 2 s
P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

Figure 8. Test Circuit for Off Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_{SEL} = GND$ and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
ST = 2 s
P1 = 0 dBm

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3L301DGG	Obsolete	Production	TSSOP (DGG) 48	-	-	Call TI	Call TI	-40 to 85	TS3L301
TS3L301DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L301
TS3L301DGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L301
TS3L301DGGRG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L301
TS3L301DGGRG4.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L301
TS3L301DGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK301
TS3L301DGVR.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK301
TS3L301DGVRG4	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK301
TS3L301DGVRG4.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK301

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L301DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
TS3L301DGVRG4	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L301DGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
TS3L301DGVRG4	TVSOP	DGV	48	2000	353.0	353.0	32.0

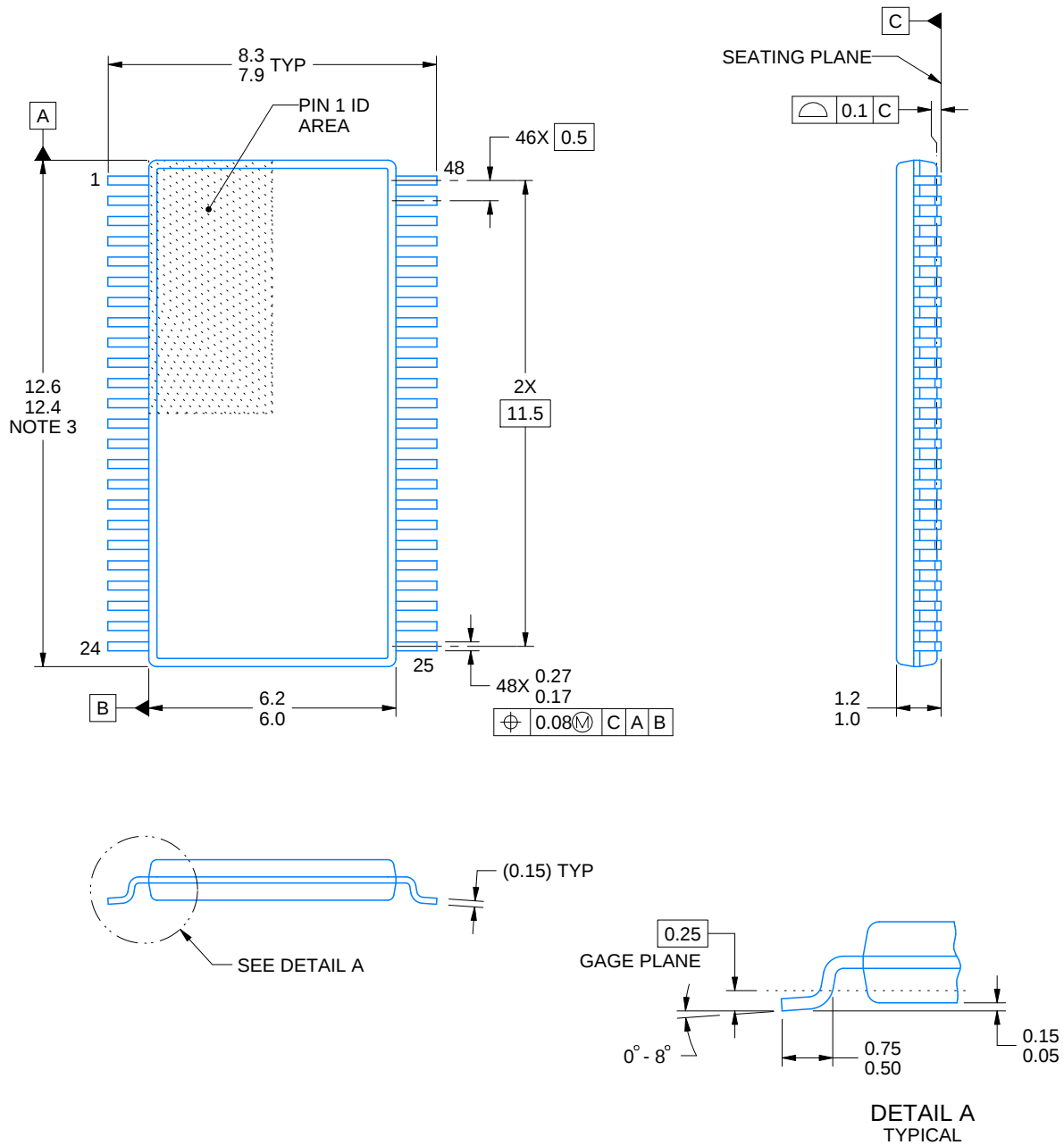
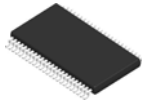
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4214859/B 11/2020

NOTES:

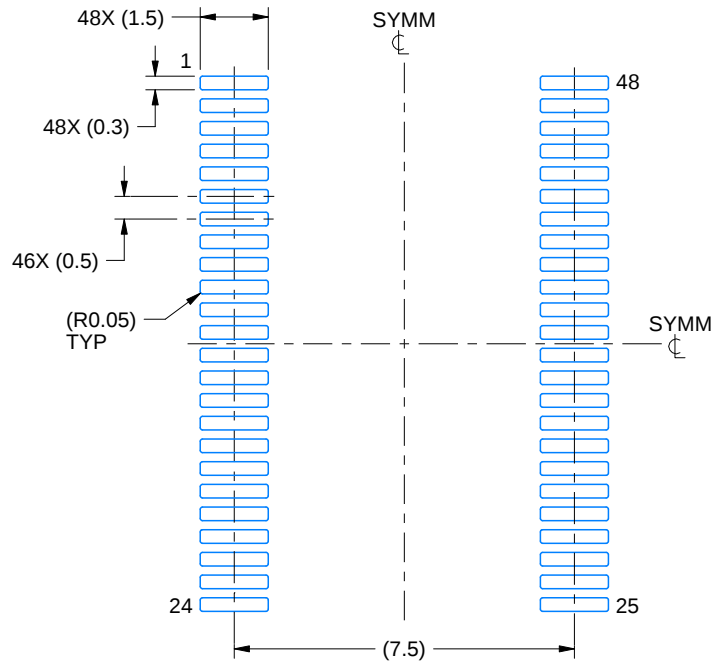
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

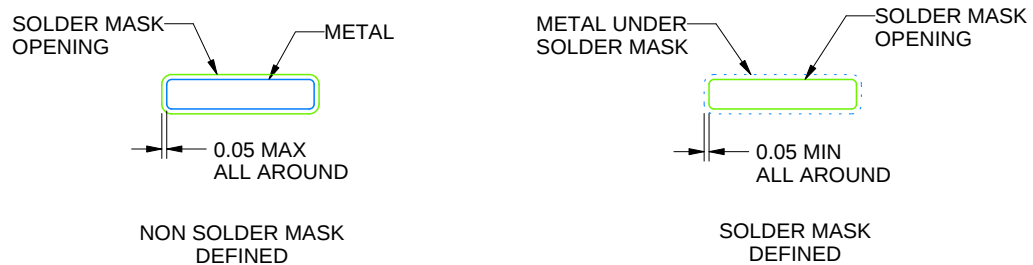
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

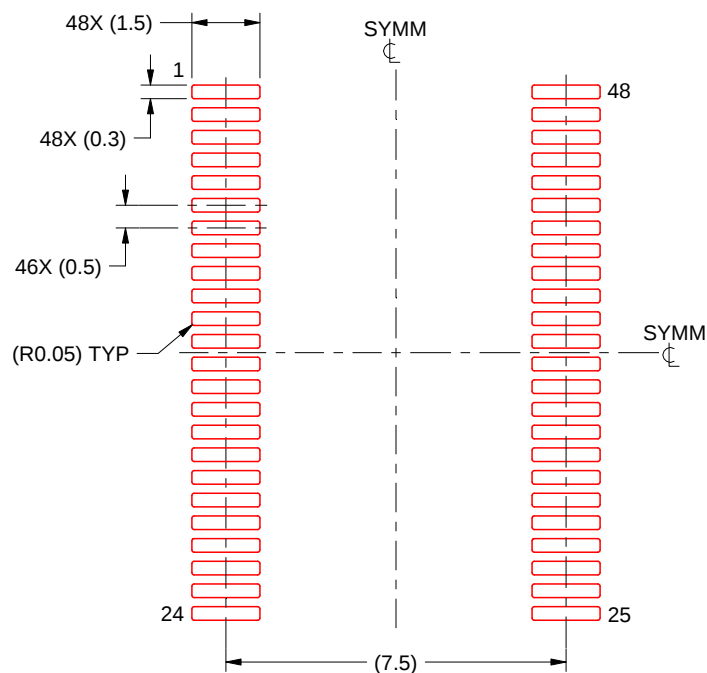
- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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