

TS3A4751 0.9- Ω Low-voltage, single-supply, 4-channel spst analog switch

1 Features

- Low ON-State Resistance (R_{ON})
 - 0.9 Ω Max (3-V Supply)
 - 1.5 Ω Max (1.8-V Supply)
- R_{ON} Flatness: 0.4 Ω Max (3-V)
- R_{ON} Channel Matching
 - 0.05 Ω Max (3-V Supply)
 - 0.15 Ω Max (1.8-V Supply)
- 1.6-V to 3.6-V Single-Supply Operation
- 1.8-V CMOS Logic Compatible (3-V Supply)
- High Current-Handling Capacity (100 mA Continuous)
- Fast Switching: $t_{ON} = 5$ ns, $t_{OFF} = 4$ ns
- Supports Both Digital and Analog Applications
- ESD Protection Exceeds JESD-22
 - ± 4000 -V Human Body Model (A114-A)
 - 300-V Machine Model (A115-A)
 - ± 1000 -V Charged-Device Model (C101)

2 Applications

- Power Routing
- Battery-Powered Systems
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- PCMCIA Cards
- Cellular Phones
- Modems
- Hard Drives

3 Description

The TS3A4751 device is a bidirectional, 4-channel, normally open (NO) single-pole single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

The TS3A4751 device has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in space-saving 14-pin VQFN (RGY) and micro X2QFN (RUC) packages.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A4751	TSSOP (14)	5.00 mm \times 4.40 mm
	VQFN (14)	3.50 mm \times 3.50 mm
	X2QFN (14)	2.00 mm \times 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

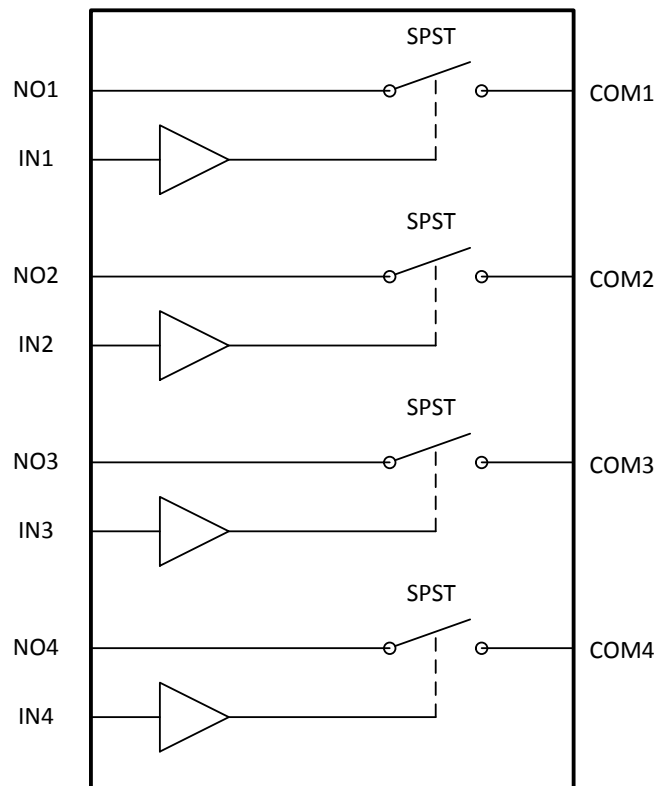


Table of Contents

1 Features	1	7.3 Feature Description.....	13
2 Applications	1	7.4 Device Functional Modes.....	13
3 Description	1	8 Application and Implementation	14
4 Revision History	2	8.1 Application Information.....	14
5 Pin Configuration and Functions	3	8.2 Typical Application	14
6 Specifications	4	9 Power Supply Recommendations	16
6.1 Absolute Maximum Ratings	4	10 Layout	16
6.2 ESD Ratings.....	4	10.1 Layout Guidelines	16
6.3 Recommended Operating Conditions.....	5	10.2 Layout Example	16
6.4 Thermal Information	5	11 Device and Documentation Support	17
6.5 Electrical Characteristics for 1.8-V Supply.....	6	11.1 Receiving Notification of Documentation Updates	17
6.6 Electrical Characteristics for 3-V Supply	7	11.2 Community Resources.....	17
6.7 Typical Characteristics	10	11.3 Trademarks	17
7 Detailed Description	13	11.4 Electrostatic Discharge Caution.....	17
7.1 Overview	13	11.5 Glossary	17
7.2 Functional Block Diagram	13	12 Mechanical, Packaging, and Orderable Information	17

4 Revision History

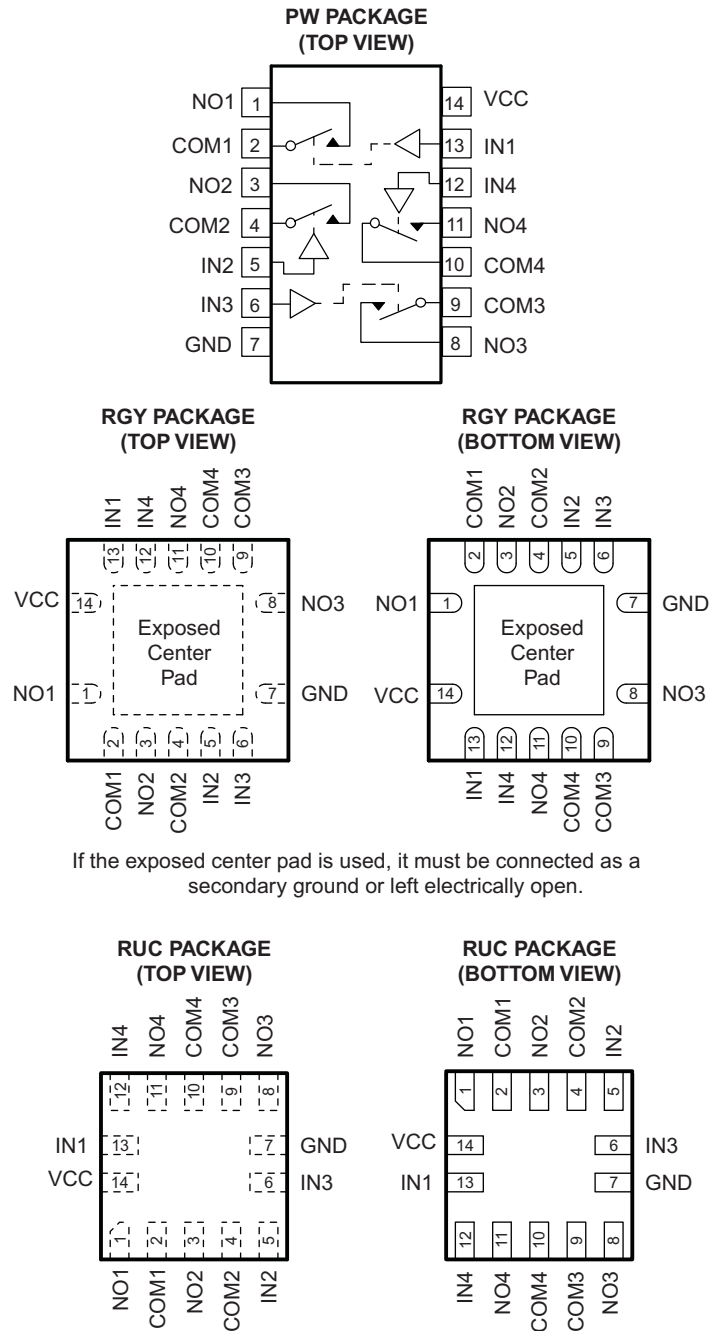
Changes from Revision E (January 2015) to Revision F Page

- Changed Supply Voltage from: 3.3 V to: 3.6 V in the *Recommended Operating Conditions* **5**

Changes from Revision D (July 2008) to Revision E Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section **1**

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NO1	I/O	Normally open signal path
2	COM1	I/O	Common signal path
3	NO2	I/O	Normally open signal path
4	COM2	I/O	Common signal path
5	IN2	I	Logic control input
6	IN3	I	Logic control input
7	GND	—	Ground
8	NO3	I/O	Normally open signal path
9	COM3	I/O	Common signal path
10	COM4	I/O	Common signal path
11	NO4	I/O	Normally open signal path
12	IN4	I	Logic control input
13	IN1	I	Logic control input
14	V _{CC}	I	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage referenced to GND ⁽²⁾	−0.3	4	V
V _{NO} V _{COM} V _{IN}	Analog and digital voltage	−0.3	V _{CC} + 0.3	V
I _{NO} I _{COM}	On-state switch current	V _{NO} , V _{COM} = 0 to V _{CC}		−100 100 mA
I _{CC} I _{GND}	Continuous current through V _{CC} or GND		±100	mA
V	Peak current pulsed at 1 ms, 10% duty cycle	COM, V _{I/O}		±200 mA
T _A	Operating temperature	−40	85	°C
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Signals on COM or NO exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000
		Machine Model	±300

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply Voltage	1.65	3.6	V
V _{NO} V _{COM} V _{IN}	Analog and digital voltage range	0	V _{CC}	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS3A4751			UNIT
		PW	RGY	RUC	
		14 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	132.3	68.5	196.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	60.6	83.1	73.9	
R _{θJB}	Junction-to-board thermal resistance	74.2	44.6	130.7	
Ψ _{JT}	Junction-to-top characterization parameter	11.2	7.8	2.1	
Ψ _{JB}	Junction-to-board characterization parameter	73.6	44.7	130.6	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	24.6	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics for 1.8-V Supply

 $V_{CC} = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$, $V_{IH} = 1\text{ V}$, $V_{IL} = 0.4\text{ V}$ (unless otherwise noted)^{(1) (2)}

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP ⁽³⁾	MAX	UNIT
ANALOG SWITCH								
V _{COM} , V _{NO}	Analog signal range				0		V _{CC}	V
R _{on}	ON-state resistance	V _{CC} = 1.8 V, I _{COM} = −10 mA, V _{NO} = 0.9 V		25°C		1	1.5	Ω
				Full			2	
ΔR _{on}	ON-state resistance match between channels ⁽⁴⁾	V _{CC} = 1.8 V, I _{COM} = −10 mA, V _{NO} = 0.9 V		25°C		0.09	0.15	Ω
				Full			0.25	
R _{on(flat)}	ON-state resistance flatness ⁽⁵⁾	V _{CC} = 1.8 V, I _{COM} = −10 mA, 0 ≤ V _{NO} ≤ V _{CC}		25°C		0.7	0.9	Ω
				Full			1.5	
I _{NO(OFF)}	NO OFF leakage current ⁽⁶⁾	V _{CC} = 1.95 V, V _{COM} = 0.15 V, 1.65 V, V _{NO} = 1.8 V, 0.15 V		25°C	−1	0.5	1	nA
				Full	−10		10	
I _{COM(OFF)}	COM OFF leakage current ⁽⁶⁾	V _{CC} = 1.95 V, V _{COM} = 0.15 V, 1.65 V, V _{NO} = 1.65 V, 0.15 V		25°C	−1	0.5	1	nA
				Full	−10		10	
I _{COM(ON)}	COM ON leakage current ⁽⁶⁾	V _{CC} = 1.95 V, V _{COM} = 0.15 V, 1.65 V, V _{NO} = 0.15 V, 1.65 V, or floating		25°C	−1	0.01	1	nA
				Full	−3		3	
DYNAMIC								
t _{ON}	Turn-on time	V _{NO} = 1.5 V, R _L = 50 Ω, C _L = 35 pF, See Figure 1		25°C		6	18	ns
				Full			20	
t _{OFF}	Turn-off time	V _{NO} = 1.5 V, R _L = 50 Ω, C _L = 35 pF, See Figure 1		25°C		5	10	ns
				Full			12	
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, See Figure 5		25°C		3.2		pC
C _{NO(OFF)}	NO OFF capacitance	f = 1 MHz, See Figure 2		25°C		23		pF
C _{COM(OFF)}	COM OFF capacitance	f = 1 MHz, See Figure 2		25°C		20		pF
C _{COM(ON)}	COM ON capacitance	f = 1 MHz, See Figure 2		25°C		43		pF
BW	Bandwidth	R _L = 50 Ω, Switch ON		25°C		123		MHz
O _{ISO}	OFF isolation ⁽⁷⁾	R _L = 50 Ω, C _L = 5 pF, See Figure 3	f = 1 MHz	25°C		−61		dB
			f = 10 MHz			−36		
X _{TALK}	Crosstalk	R _L = 50 Ω, C _L = 5 pF, See Figure 3	f = 10 MHz	25°C		−95		dB
			f = 100 MHz			−73		
THD	Total harmonic distortion	f = 20 Hz to 20 kHz, V _{COM} = 2 V _{P-P}	R _L = 32 Ω	25°C		0.14%		
			R _L = 600 Ω			0.013%		
DIGITAL CONTROL INPUTS (IN1–IN4)								
V _{IH}	Input logic high			Full	1			V
V _{IL}	Input logic low			Full			0.4	V
I _{IN}	Input leakage current	V _I = 0 or V _{CC}		25°C		0.1	5	nA
				Full	−10		10	
SUPPLY								
V _{CC}	Power-supply range				1.6		3.6	V
I _{CC}	Positive-supply current	V _I = 0 or V _{CC}		25°C			0.05	μA
				Full			0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.

(3) Typical values are at $T_A = 25^\circ\text{C}$.

(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$

(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.

(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at $T_A = 25^\circ\text{C}$.

(7) OFF isolation = $20_{\log} 10 (V_{COM}/V_{NO})$, V_{COM} = output, V_{NO} = input to OFF switch

6.6 Electrical Characteristics for 3-V Supply

 $V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$, $V_{IH} = 1.4\text{ V}$, $V_{IL} = 0.5\text{ V}$ (unless otherwise noted).^{(1) (2)}

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP ⁽³⁾	MAX	UNIT
ANALOG SWITCH							
V _{COM} , V _{NO}	Analog signal range			0		V _{CC}	V
R _{on}	ON-state resistance	V _{CC} = 2.7 V, I _{COM} = −100 mA, V _{NO} = 1.5 V	25°C	0.7	0.9		Ω
			Full		1.1		
ΔR _{on}	ON-state resistance match between channels ⁽⁴⁾	V _{CC} = 2.7 V, I _{COM} = −100 mA, V _{NO} = 1.5 V	25°C	0.03	0.05		Ω
			Full		0.15		
R _{on(flat)}	ON-state resistance flatness ⁽⁵⁾	V _{CC} = 2.7 V, I _{COM} = −100 mA, V _{NO} = 1 V, 1.5 V, 2 V	25°C	0.23	0.4		Ω
			Full		0.5		
I _{NO(OFF)}	NO OFF leakage current ⁽⁶⁾	V _{CC} = 3.6 V, V _{COM} = 0.3 V, 3 V, V _{NO} = 3 V, 0.3 V	25°C	−2	1	2	nA
			Full	−18		18	
I _{COM(OFF)}	COM OFF leakage current ⁽⁶⁾	V _{CC} = 3.6 V, V _{COM} = 0.3 V, 3 V, V _{NO} = 3 V, 0.3 V	25°C	−2	1	2	nA
			Full	−18		18	
I _{COM(ON)}	COM ON leakage current ⁽⁶⁾	V _{CC} = 3.6 V, V _{COM} = 0.3 V, 3 V, V _{NO} = 0.3 V, 3 V, or floating	25°C	−2.5	0.01	2.5	nA
			Full	−5		5	
DYNAMIC							
t _{ON}	Turn-on time	V _{NO} = 1.5 V, R _L = 50 Ω, C _L = 35 pF, See Figure 1	25°C	5	14		ns
			Full		15		
t _{OFF}	Turn-off time	V _{NO} = 1.5 V, R _L = 50 Ω, C _L = 35 pF, See Figure 1	25°C	4	9		ns
			Full		10		
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, See Figure 5	25°C	3			pC
C _{NO(OFF)}	NO OFF capacitance	f = 1 MHz, See Figure 2	25°C	23			pF
C _{COM(OFF)}	COM OFF capacitance	f = 1 MHz, See Figure 2	25°C	20			pF
C _{COM(ON)}	COM ON capacitance	f = 1 MHz, See Figure 2	25°C	43			pF
BW	Bandwidth	R _L = 50 Ω, Switch ON	25°C	125			MHz
O _{ISO}	OFF isolation ⁽⁷⁾	R _L = 50 Ω, C _L = 5 pF, See Figure 3	25°C	f = 10 MHz	−40		dB
				f = 1 MHz	−62		
X _{TALK}	Crosstalk	R _L = 50 Ω, C _L = 5 pF, See Figure 3	25°C	f = 10 MHz	−73		dB
				f = 1 MHz	−95		
THD	Total harmonic distortion	f = 20 Hz to 20 kHz, V _{COM} = 2 V _{P-P}	25°C	R _L = 32 Ω	0.04%		
				R _L = 600 Ω	0.003%		
DIGITAL CONTROL INPUTS (IN1–IN4)							
V _{IH}	Input logic high		Full	1.4			V
V _{IL}	Input logic low		Full			0.5	V
I _{IN}	Input leakage current	V _I = 0 or V _{CC}	25°C	0.5		1	nA
			Full	−20		20	
SUPPLY							
V _{CC}	Power-supply range			1.6		3.6	V
I _{CC}	Positive-supply current	V _{CC} = 3.6 V, V _{IN} = 0 or V _{CC}	25°C			0.075	μA
			Full			0.75	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.

(3) Typical values are at $V_{CC} = 3\text{ V}$, $T_A = 25^\circ\text{C}$.

(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$

(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.

(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at $T_A = 25^\circ\text{C}$.

(7) OFF isolation = $20_{\log 10} (V_{COM}/V_{NO})$, V_{COM} = output, V_{NO} = input to OFF switch

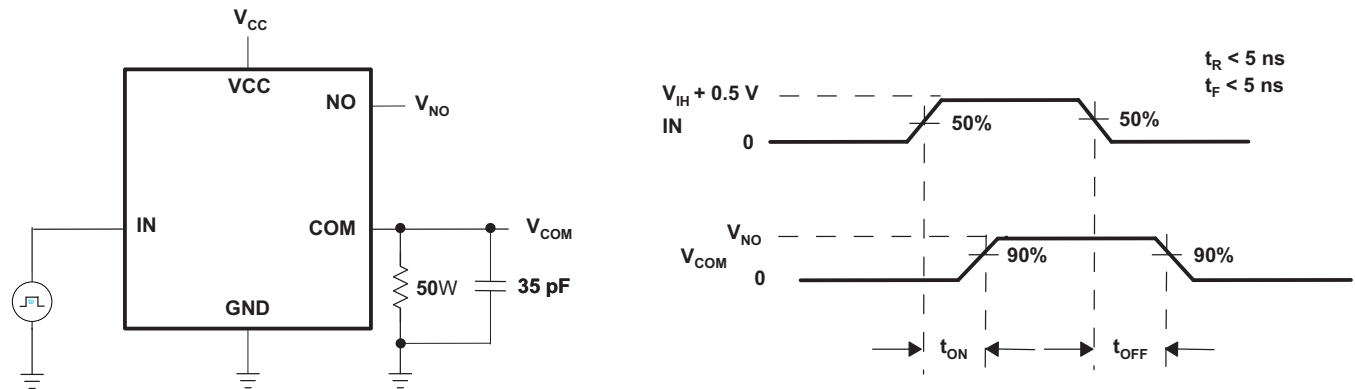


Figure 1. Switching Times

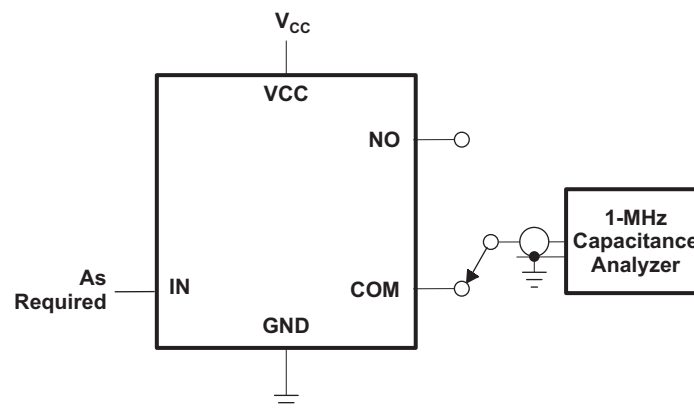
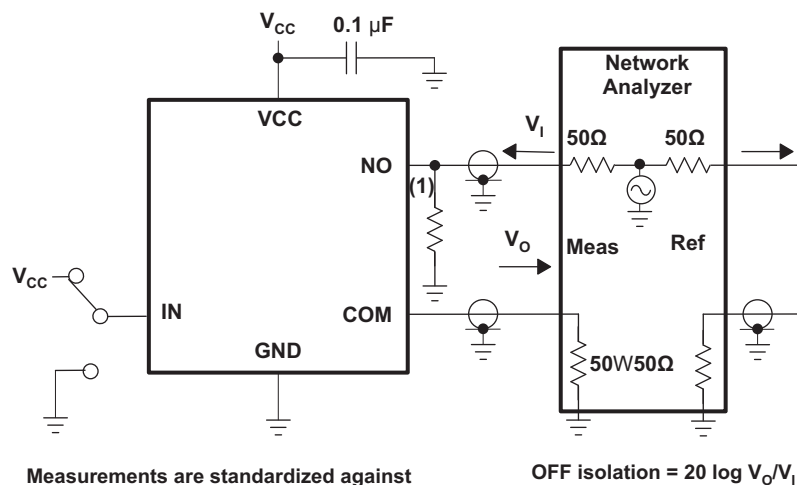


Figure 2. NO and COM Capacitance



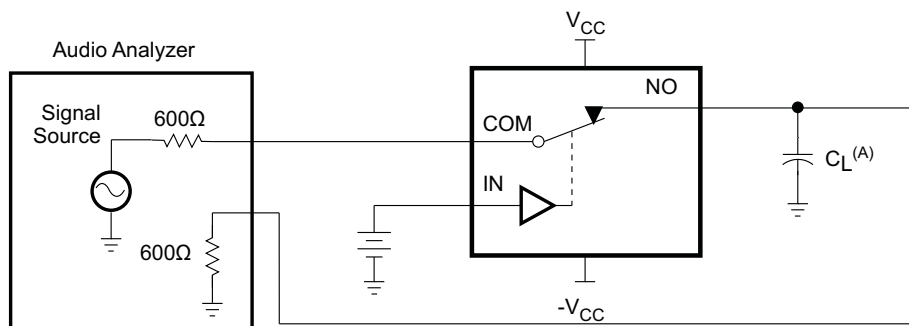
Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. Bandwidth is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF isolation} = 20 \log V_O/V_I$$

(1) Add 50-Ω termination for OFF isolation

Figure 3. OFF Isolation, Bandwidth, and Crosstalk

Channel ON: COM to NO $V_I = V_{CC}$ $C_L = 50 \text{ pF}$
 $V_{SOURCE} = V_{CC} \text{ P-P}$ $f_{SOURCE} = 20 \text{ Hz to } 20 \text{ kHz}$ $R_L = 600\Omega$



A. C_L includes probe and jig capacitance.

Figure 4. Total Harmonic Distortion (THD)

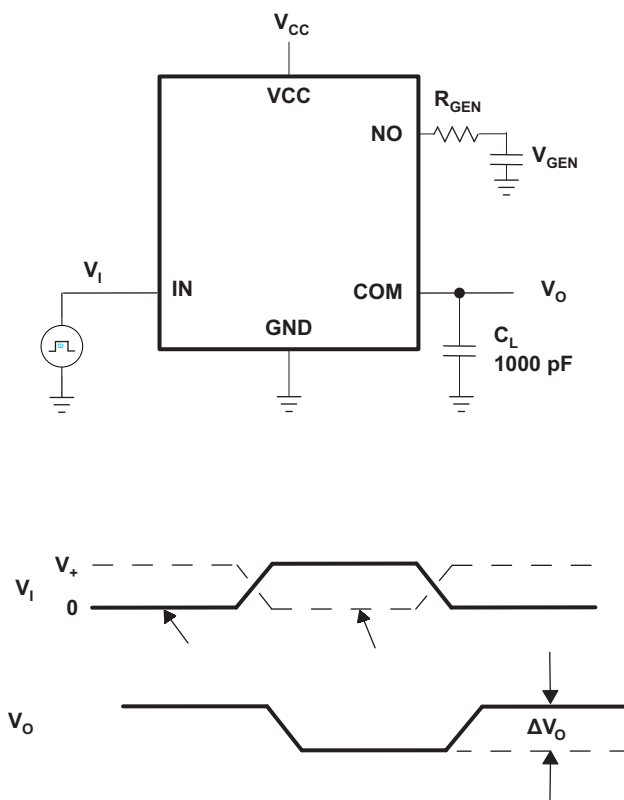


Figure 5. Charge Injection (Q_C)

6.7 Typical Characteristics

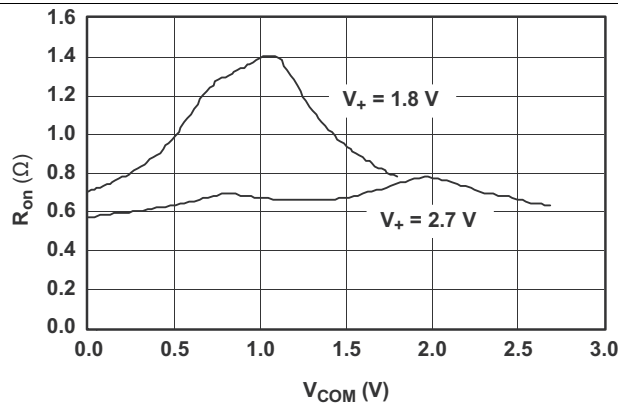


Figure 6. R_{on} vs V_{COM}

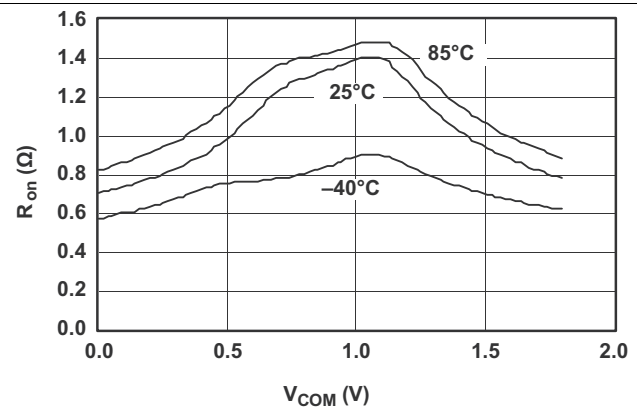


Figure 7. R_{on} vs V_{COM} ($V_{CC} = 1.8$ V)

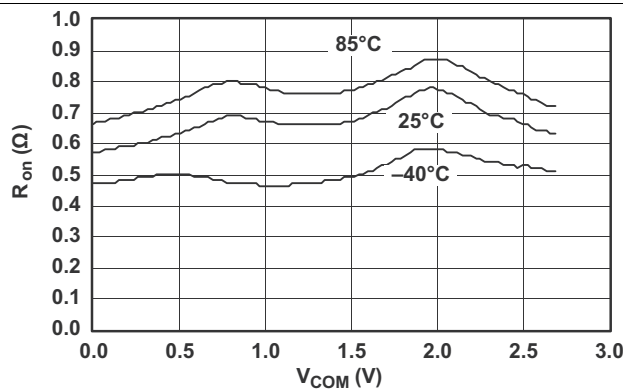


Figure 8. R_{on} vs V_{COM} ($V_{CC} = 2.7$ V)

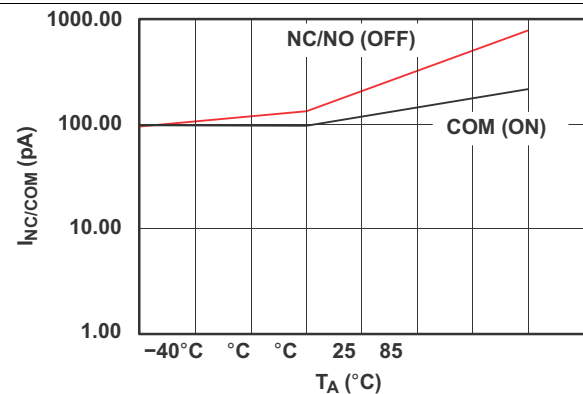


Figure 9. I_{ON} and I_{OFF} vs Temperature ($V_{CC} = 3.6$ V)

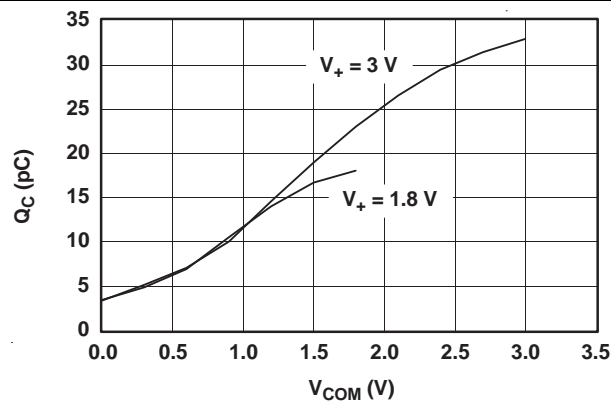


Figure 10. Q_C vs V_{COM}

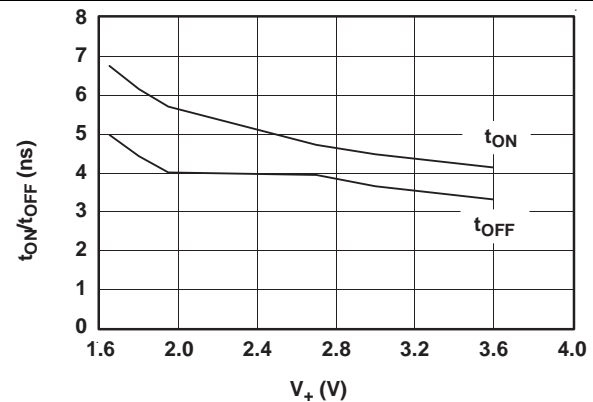


Figure 11. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

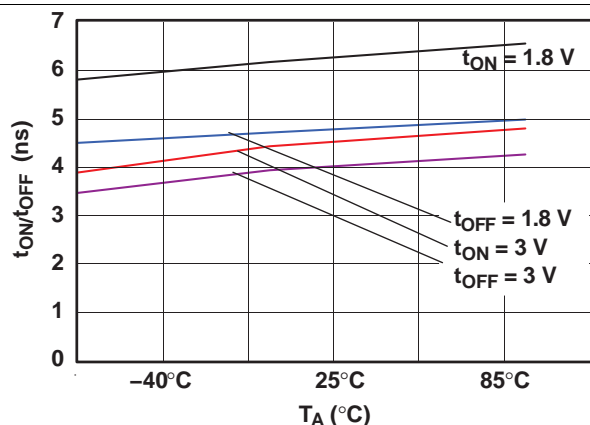


Figure 12. t_{ON} and t_{OFF} vs Temperature

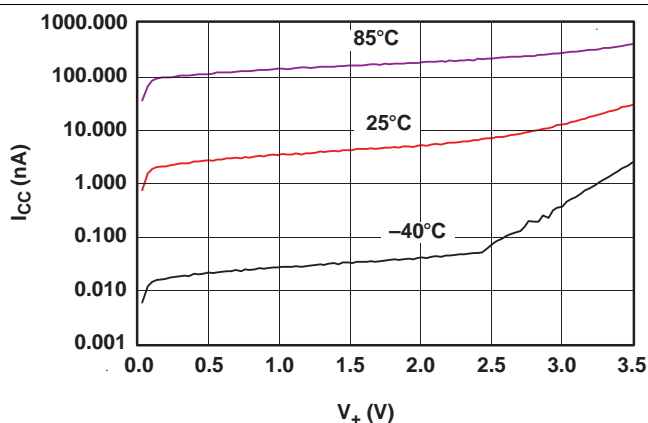


Figure 13. I_{CC} vs V_{CC}

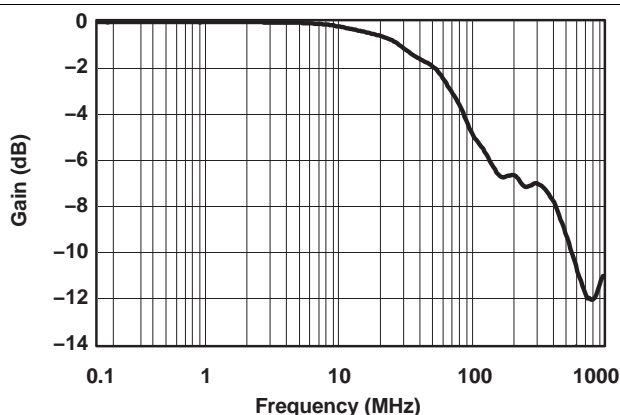


Figure 14. Gain vs Frequency
($V_{CC} = 3$ V)

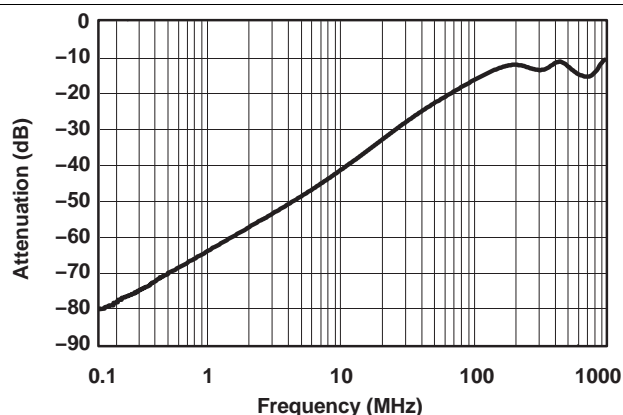


Figure 15. OFF Isolation vs Frequency
($V_{CC} = 3$ V)

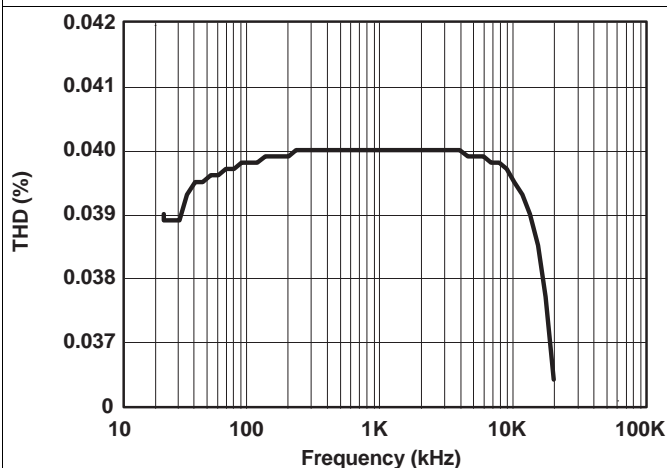


Figure 16. Total Harmonic Distortion vs Frequency
($R_L = 32 \Omega$)

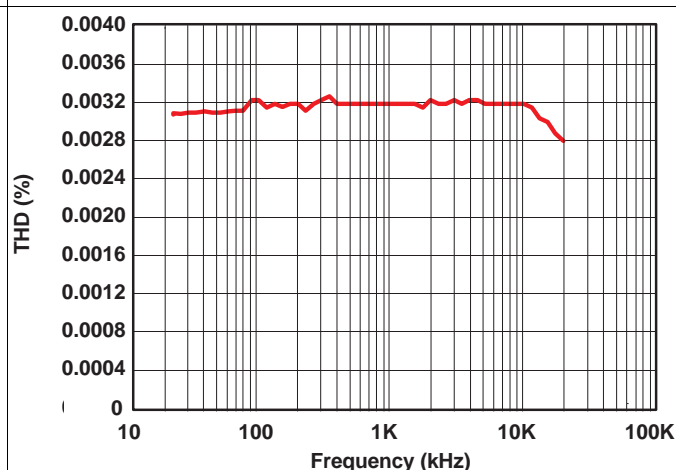


Figure 17. Total Harmonic Distortion vs Frequency
($R_L = 600 \Omega$)

Typical Characteristics (continued)

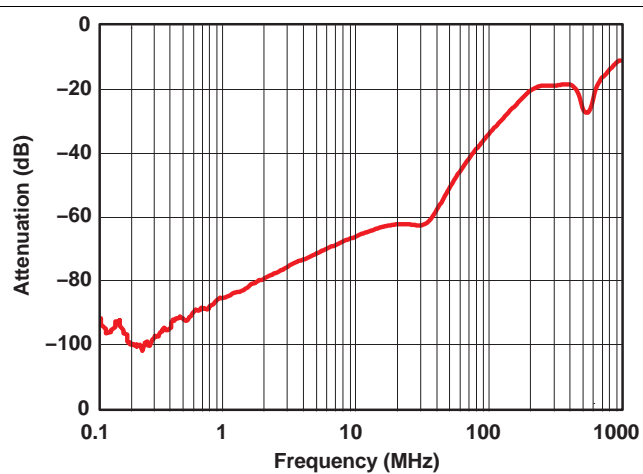


Figure 18. Crosstalk vs Frequency ($V_{CC} = 3\text{ V}$)

7 Detailed Description

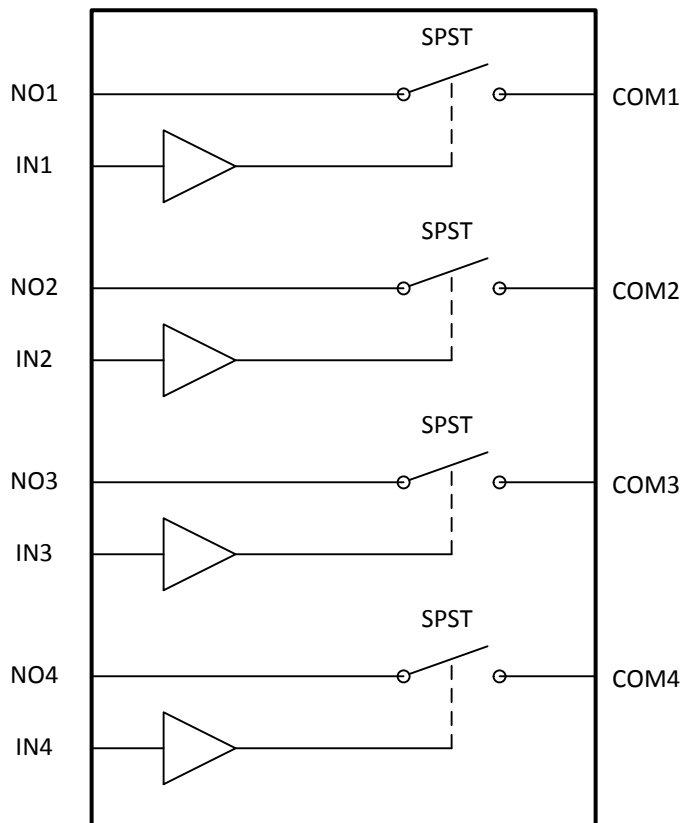
7.1 Overview

The TS3A4751 is a bidirectional, 4-channel, normally open (NO) single-pole single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

The TS3A4751 has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in space-saving 14-pin VQFN (RGY) and micro X2QFN (RUC) packages.

7.2 Functional Block Diagram



7.3 Feature Description

This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V TTL/CMOS compatible when using a 3-V supply.

7.4 Device Functional Modes

Table 1. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Logic Inputs

The TS3A4751 logic inputs can be driven up to 3.6 V, regardless of the supply voltage. For example, with a 1.8-V supply, IN may be driven low to GND and high to 3.6 V. Driving IN rail to rail minimizes power consumption.

8.1.2 Analog Signal Levels

Analog signals that range over the entire supply voltage (V_{CC} to GND) can be passed with very little change in R_{on} (see [Typical Characteristics](#)). The switches are bidirectional, so NO and COM can be used as either inputs or outputs.

8.2 Typical Application

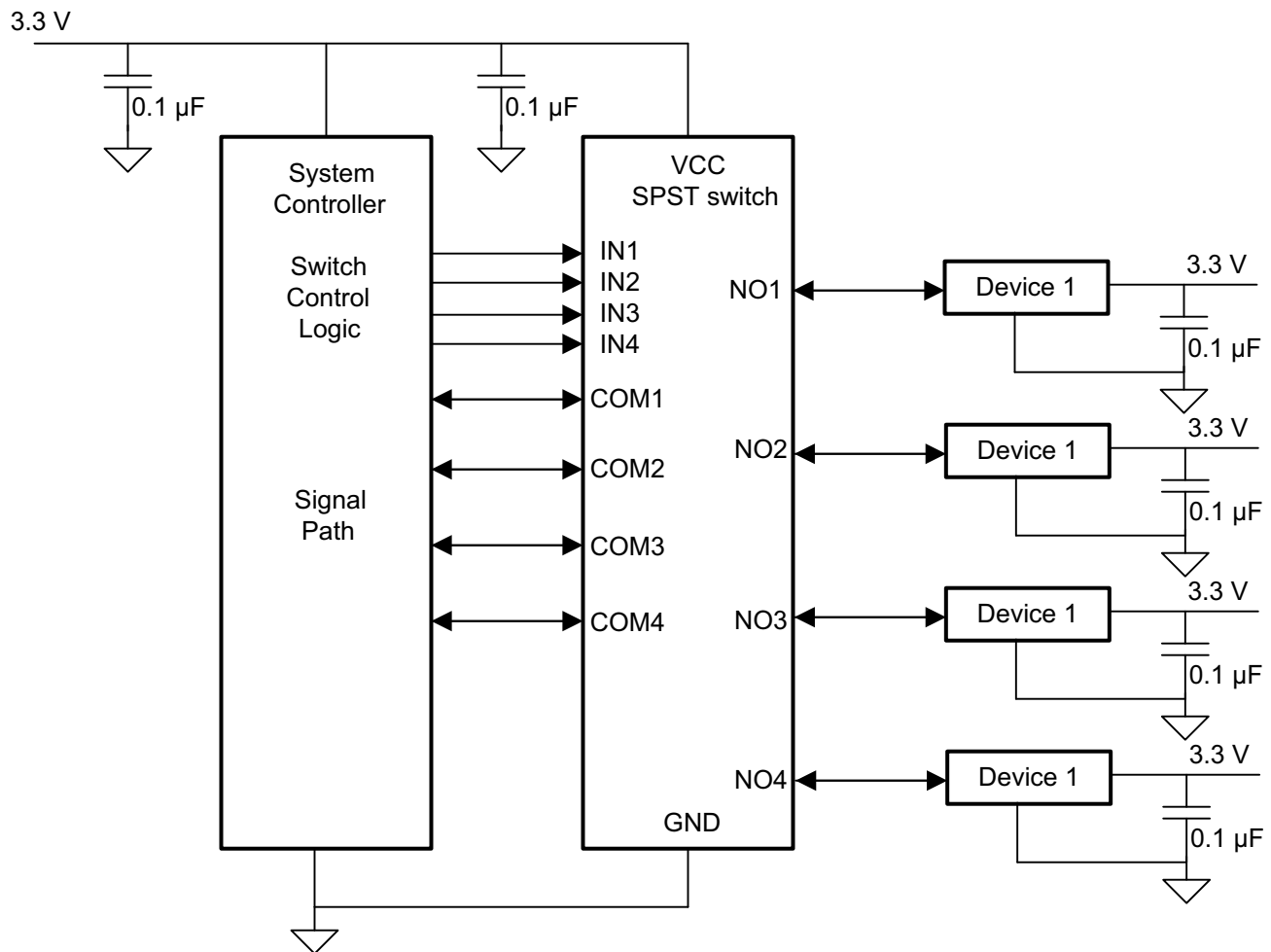


Figure 19. Typical Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the specified ranges to ensure proper performance.

8.2.2 Detailed Design Procedure

The TS3A4751 can be properly operated without any external components. However, it is recommended that unused pins should be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. It is also recommended that the digital control pins (INX) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

8.2.3 Application Curve

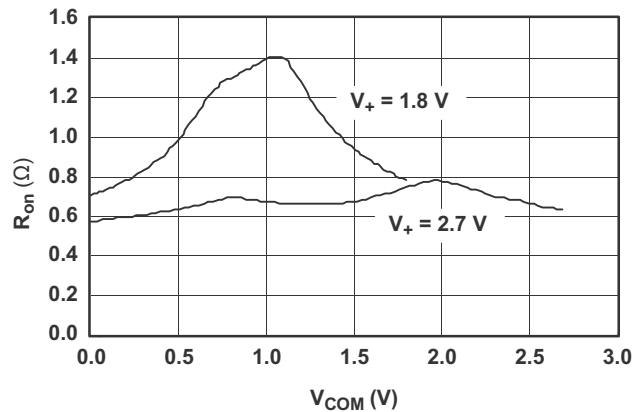


Figure 20. R_{on} vs V_{COM}

9 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1- μF capacitor, connected from V_{CC} to GND, is adequate for most applications.

10 Layout

10.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance.

Reduce stray inductance and capacitance by keeping traces short and wide.

Ensure that bypass capacitors are as close to the device as possible.

Use large ground planes where possible.

10.2 Layout Example

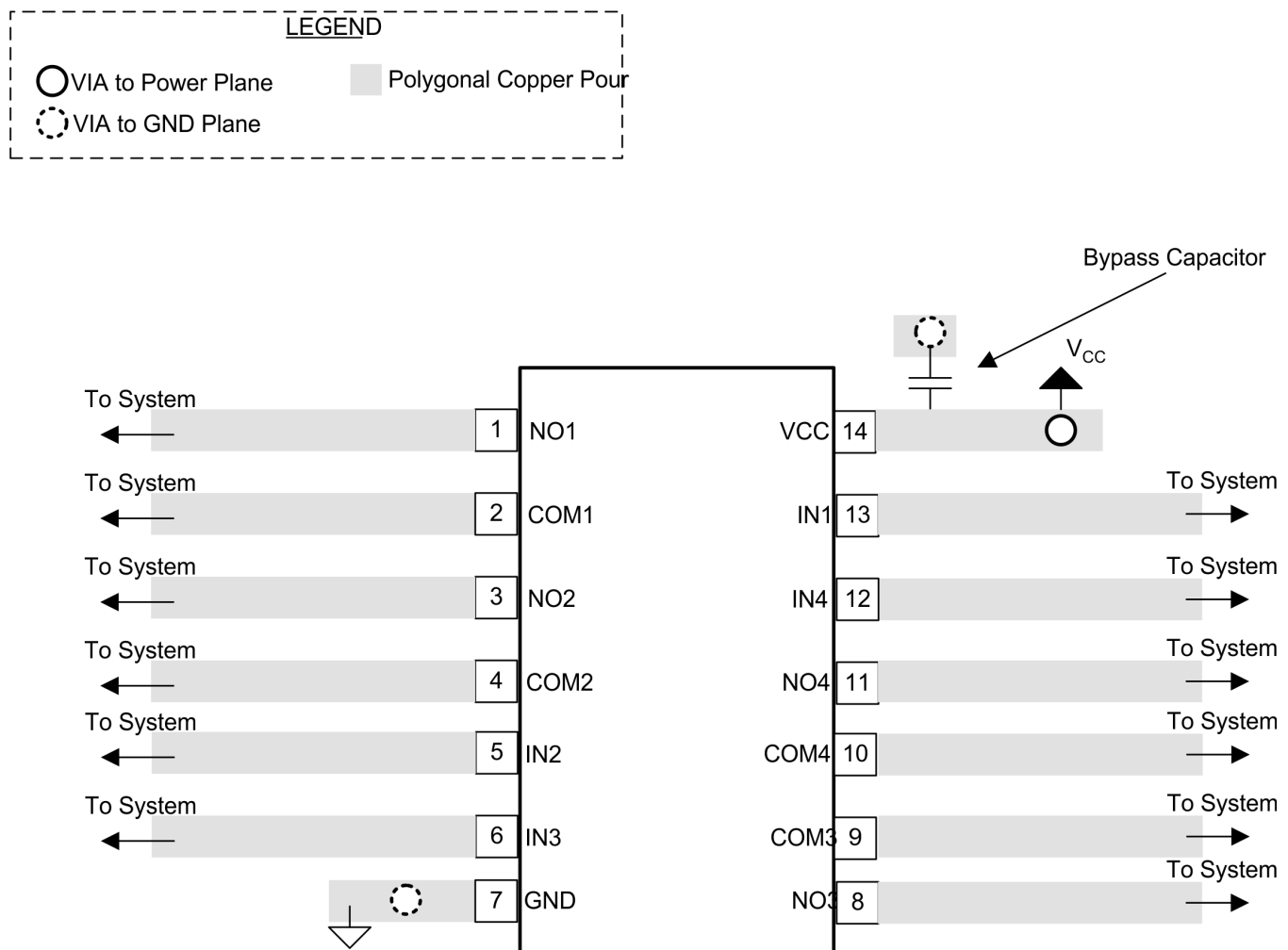


Figure 21. Layout Schematic

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3A4751PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC751
TS3A4751PWR.B	Active	Production	null (null)	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TS3A4751PWR	YC751
TS3A4751RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YC751
TS3A4751RGYR.B	Active	Production	null (null)	3000 LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	See TS3A4751RGYR	YC751
TS3A4751RGYRG4.B	Active	Production	null (null)	3000 LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	See TS3A4751RGYRG4	YC751
TS3A4751RUCR	Active	Production	QFN (RUC) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3MO
TS3A4751RUCR.B	Active	Production	null (null)	3000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TS3A4751RUCR	3MO
TS3A4751RUCRG4.B	Active	Production	null (null)	3000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TS3A4751RUCRG4	3MO

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A4751PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A4751RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TS3A4751RUCR	QFN	RUC	14	3000	180.0	9.5	2.2	2.2	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A4751PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TS3A4751RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0
TS3A4751RUCR	QFN	RUC	14	3000	189.0	185.0	36.0



4220202/B 12/2023

NOTES:

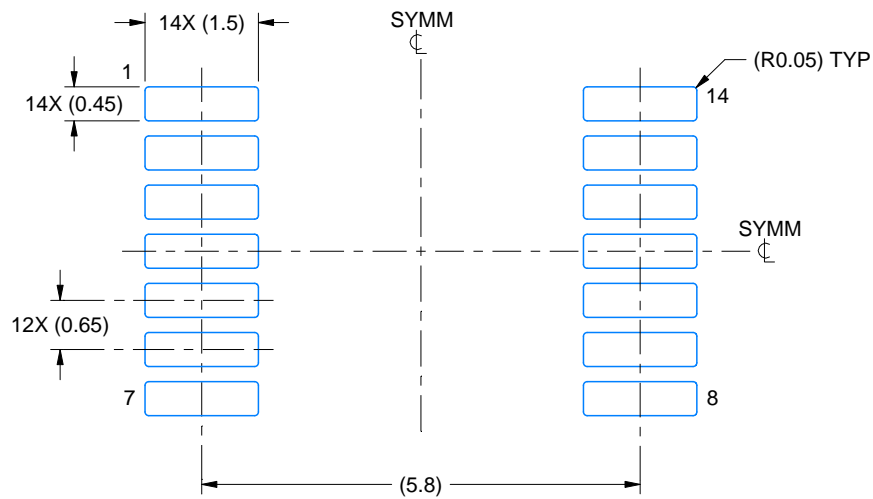
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

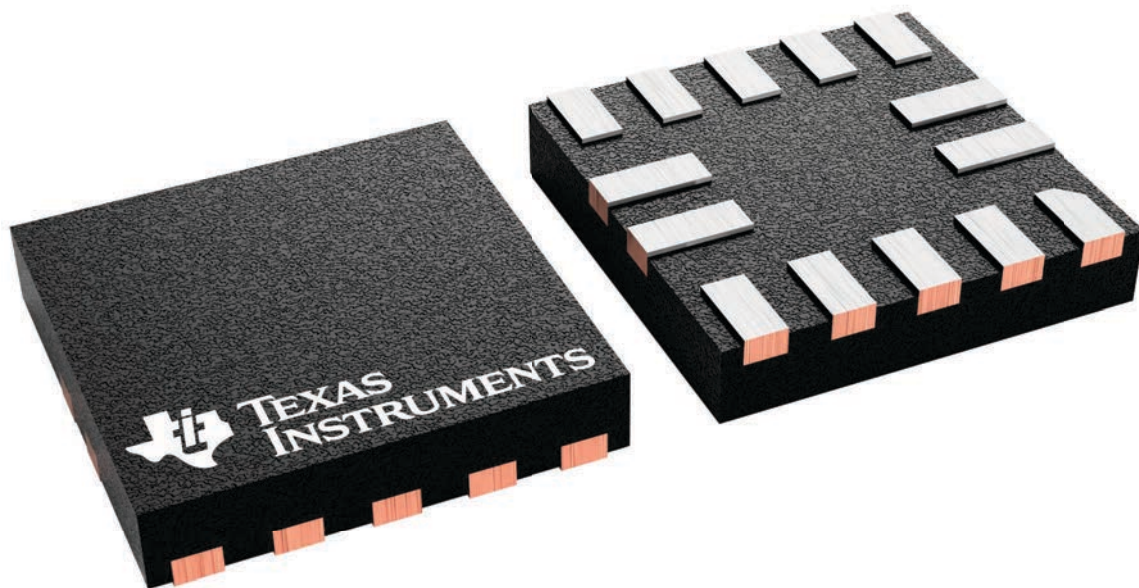
RUC 14

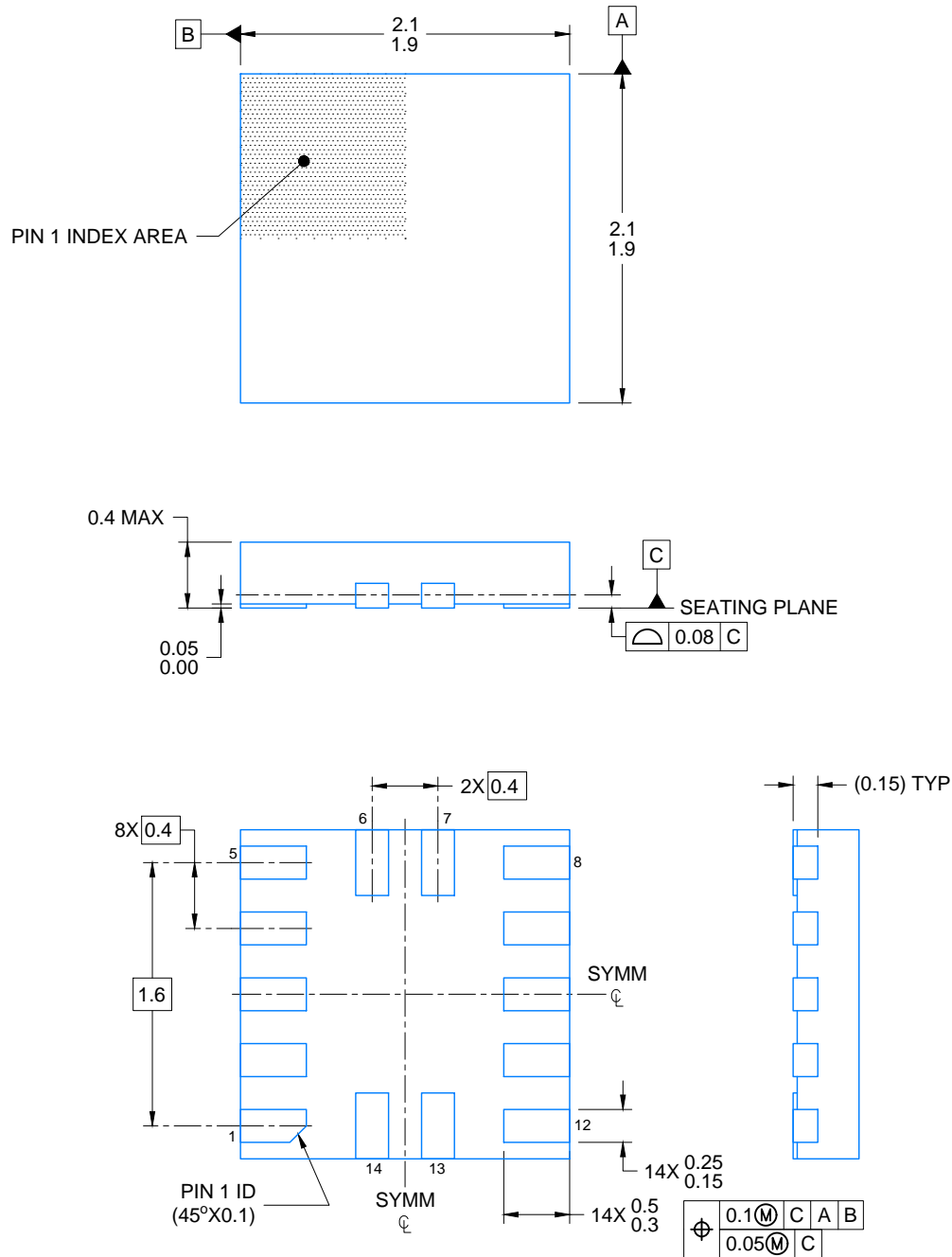
X2QFN - 0.4 mm max height

2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

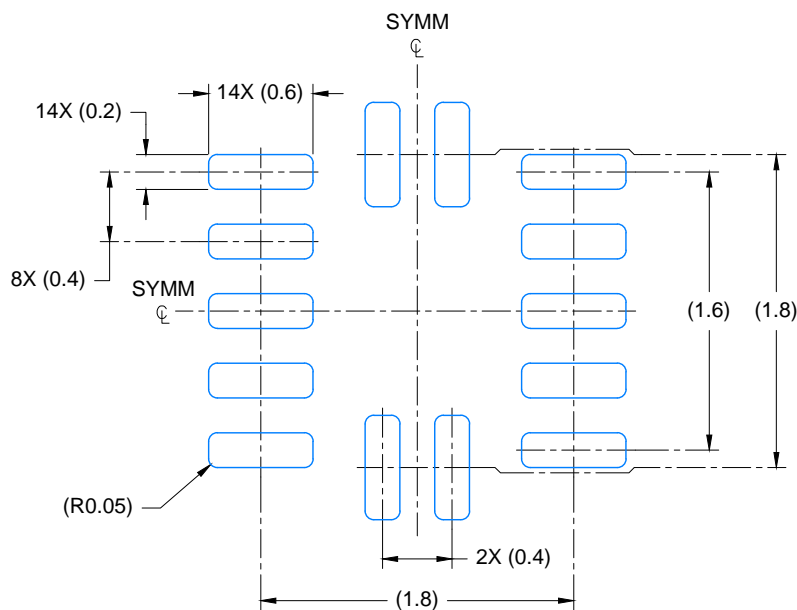




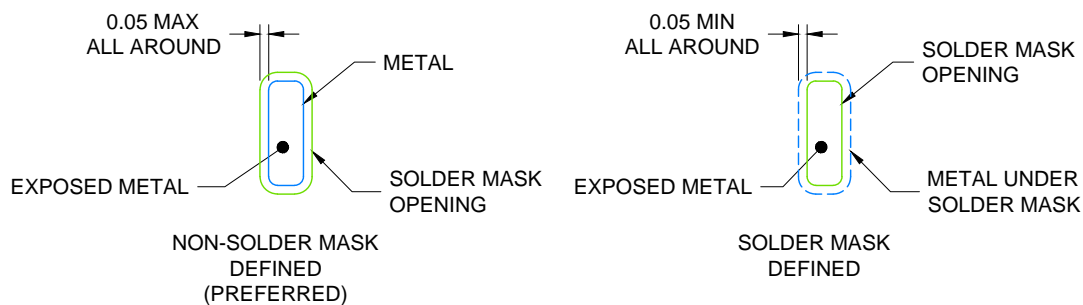
4220584/A 05/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X



SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

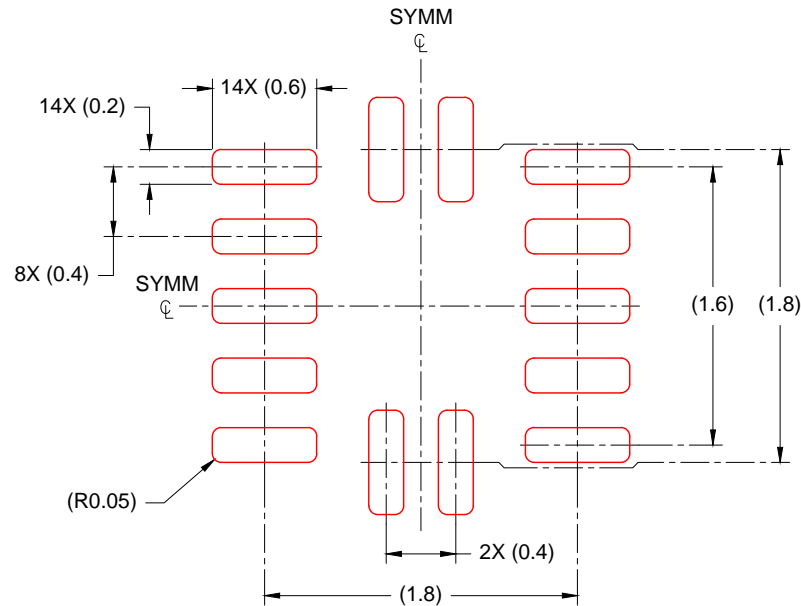
- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RUC0014A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

RGY 14

VQFN - 1 mm max height

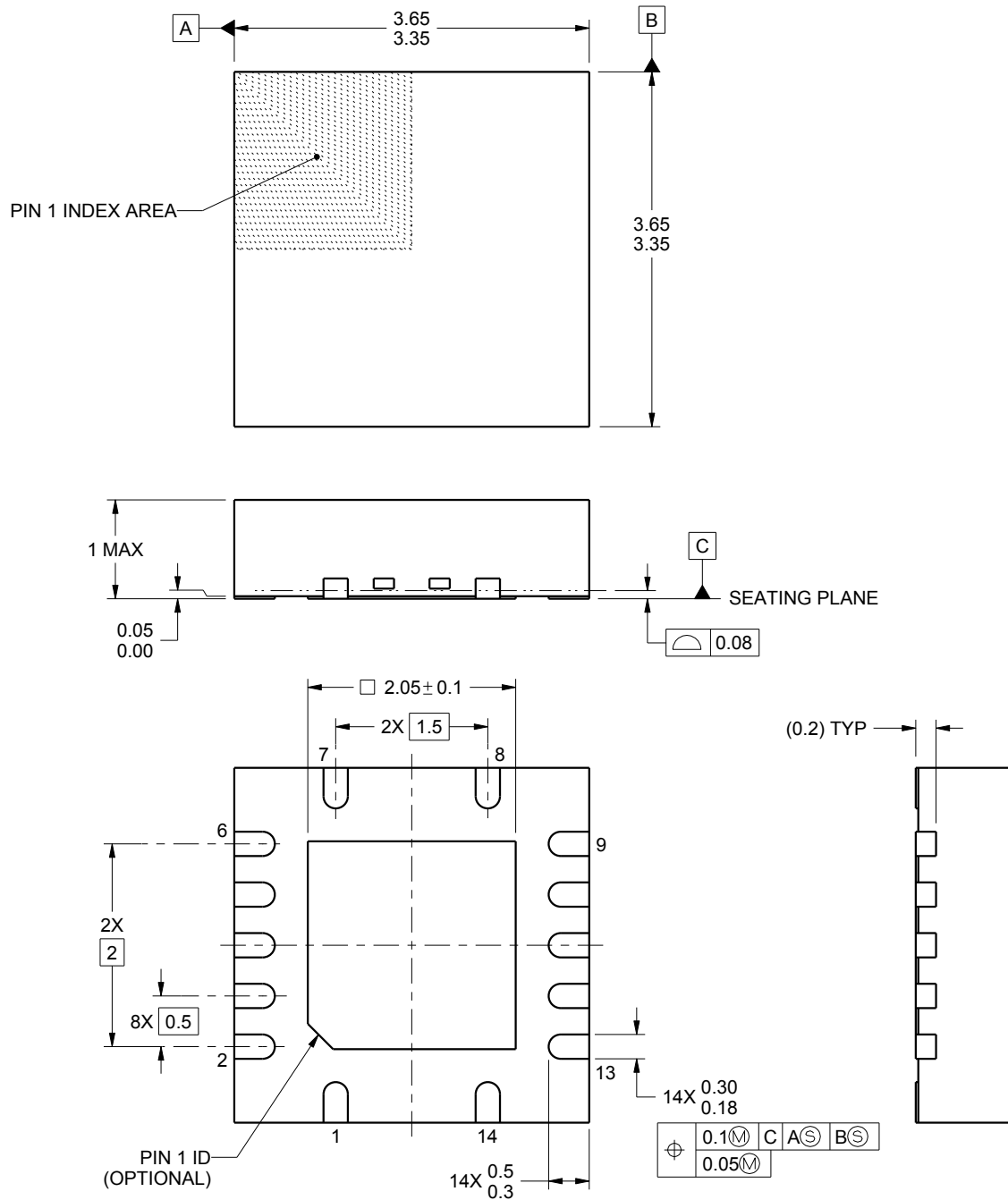
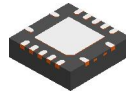
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A



4219040/A 09/2015

NOTES:

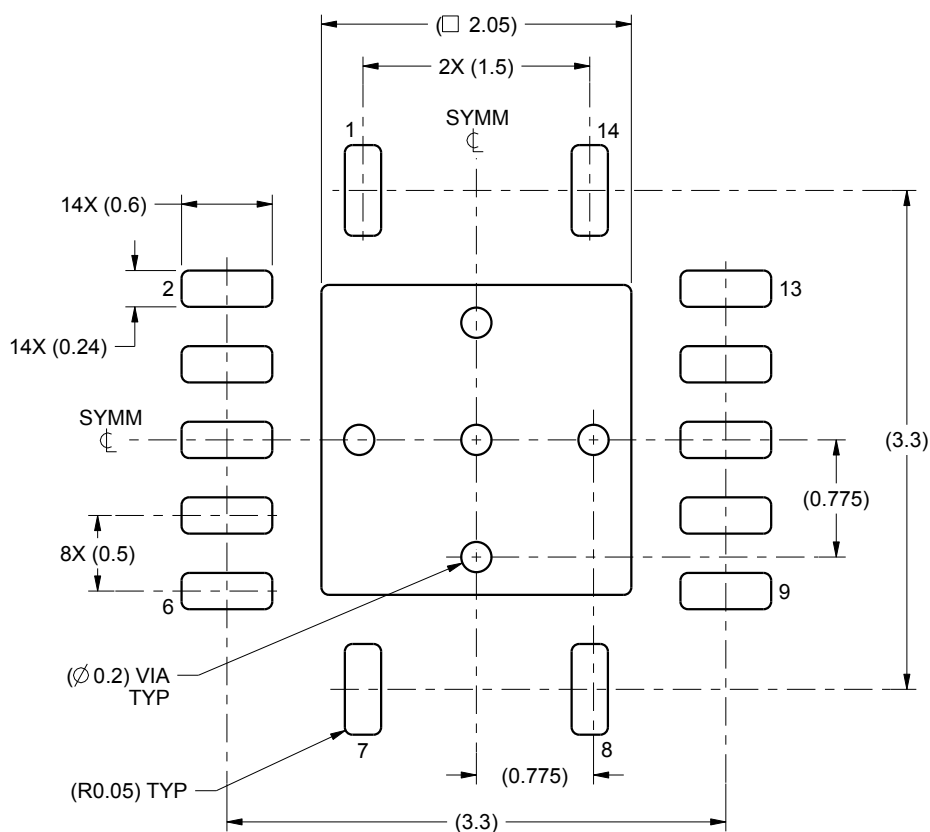
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

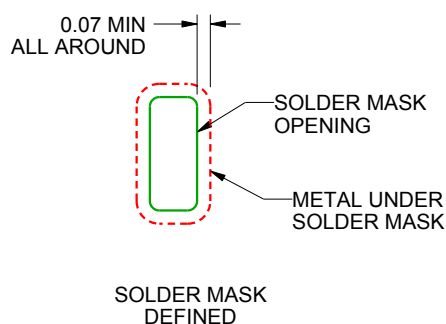
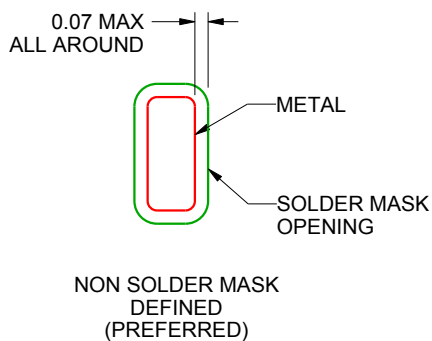
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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