

TRS3232E 3V to 5.5V Multichannel RS-232 Line Driver and Receiver With ±15kV IEC ESD Protection In Small Package

1 Features

- ESD protection for RS-232 bus pins
 - ±15kV (HBM)
 - ±8kV (IEC61000-4-2, Contact discharge)
 - ±15kV (IEC61000-4-2, Air-gap discharge)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU V.28 standards
- Operates with 3V to 5.5V V_{CC} supply
 - Interoperable with RS-232 down to 2.7V V_{CC}
- Operates up to 250kbps
- Two drivers and two receivers
- Low supply current: 300µA (typical)
- External capacitors: 4 × 0.1µF
- Accepts 5V logic input with 3.3V supply
- Available in near chip-scale package (QFN-16, 3mm x 3mm), 85% smaller than SOIC-16
- Pin compatible to alternative high-speed devices (1Mbps)
 - SN65C3232E (–40°C to +85°C)
 - SN75C3232E (0°C to 70°C)

2 Applications

- [Industrial PCs](#)
- [Wired networking](#)
- [Data center and enterprise computing](#)
- [Battery-powered systems](#)
- [Notebooks](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

3 Description

The TRS3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with ±15kV IEC ESD protection pin to pin (serial-port connection pins, including GND).

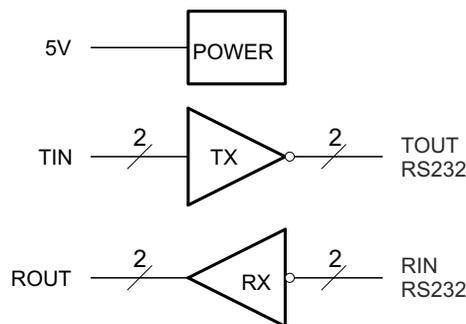
The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. The devices operate at data signaling rates up to 250kbps and a maximum of 30V/µs driver output slew rate.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TRS3232E	SOIC (D, 16)	9.9mm × 6mm
	SSOP (DB, 16)	6.2mm × 7.8mm
	SOIC (DW, 16)	10.3mm × 10.3mm
	TSSOP (PW, 16)	5mm × 6.4mm
	VQFN (RGT, 16)	3mm × 3mm
	SOT-23-THN (DYY, 16)	4.2mm × 2mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



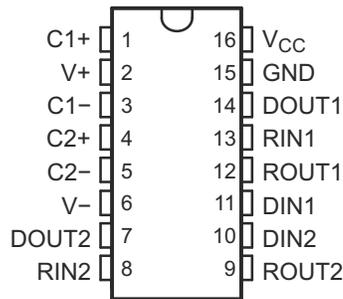
Simplified Diagram



Table of Contents

1 Features	1	7.2 Functional Block Diagram.....	11
2 Applications	1	7.3 Feature Description.....	11
3 Description	1	7.4 Device Functional Modes.....	12
4 Pin Configuration and Functions	3	8 Application and Implementation	13
5 Specifications	4	8.1 Application Information.....	13
5.1 Absolute Maximum Ratings.....	4	8.2 Typical Application.....	13
5.2 ESD Ratings.....	4	8.3 Power Supply Recommendations.....	14
5.3 ESD Ratings - IEC Specifications.....	4	8.4 Layout.....	14
5.4 Recommended Operating Conditions.....	5	9 Device and Documentation Support	16
5.5 Thermal Information.....	5	9.1 Receiving Notification of Documentation Updates....	16
5.6 Electrical Characteristics — Device.....	6	9.2 Support Resources.....	16
5.7 Electrical Characteristics — Driver.....	6	9.3 Trademarks.....	16
5.8 Electrical Characteristics — Receiver.....	7	9.4 Electrostatic Discharge Caution.....	16
5.9 Switching Characteristics.....	7	9.5 Glossary.....	16
6 Parameter Measurement Information	10	10 Revision History	16
7 Detailed Description	11	11 Mechanical, Packaging, and Orderable Information	17
7.1 Overview.....	11		

4 Pin Configuration and Functions



**Figure 4-1. DB, PW or DYY Package
 16-Pin SSOP, TSSOP, or SOT-23-THN
 (Top View)**

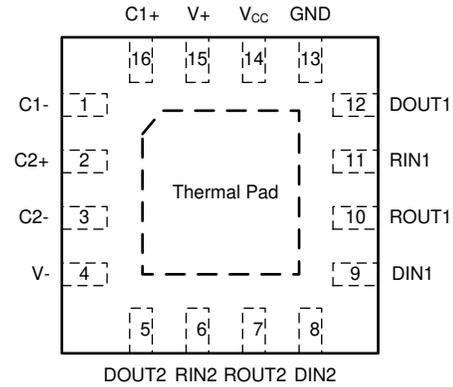


Figure 4-2. RGT package, 16 Pin VQFN, Top View

Table 4-1. Pin Functions

PIN		RGT	TYPE	DESCRIPTION
NAME	NO.			
C1+	1	16	—	Positive lead of C1 capacitor
C1-	3	1	—	Negative lead of C1 capacitor
C2+	4	2	—	Positive lead of C2 capacitor
C2-	5	3	—	Negative lead of C2 capacitor
DIN1	11	9	I	Logic data input (from UART)
DIN2	10	8	I	Logic data input (from UART)
DOUT2	7	5	O	RS232 line data output (to remote RS232 system)
DOUT1	14	12	O	RS232 line data output (to remote RS232 system)
GND	15	13	—	Ground
RIN1	13	11	I	RS232 line data input (from remote RS232 system)
RIN2	8	6	I	RS232 line data input (from remote RS232 system)
ROUT2	9	7	O	Logic data output (to UART)
ROUT1	12	10	O	Logic data output (to UART)
V+	2	15	O	Positive charge pump output for storage capacitor only
V-	6	4	O	Negative charge pump output for storage capacitor only
V _{CC}	16	14	—	Supply voltage, connect to external 3-V to 5.5-V power supply
Thermal Pad		Yes	—	Thermal pad for improving heat dissipation. Can be connected to GND or left floating.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage ⁽²⁾	-0.3	6	V	
V+	Positive output supply voltage ⁽²⁾	-0.3	7	V	
V-	Negative output supply voltage ⁽²⁾	0.3	-7	V	
V+ - V-	Supply voltage difference ⁽²⁾		13	V	
V _I	Input voltage	Drivers	-0.3	6	V
		Receivers	-25	25	V
V _O	Output voltage	Drivers	-13.2	13.2	V
		Receivers	-0.3	V _{CC} + 0.3	V
T _J	Operating virtual junction temperature		150	°C	
T _{stg}	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	All pins except RIN1, RIN2, DOUT1 and DOUT2	±2000	V
			Pins RIN1, RIN2, DOUT1 and DOUT2	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	All pins	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	IEC 61000-4-2, Contact Discharge ⁽¹⁾	Pins RIN1, RIN2, DOUT1, DOUT2 ⁽²⁾	±8000	V
		IEC 61000-4-2, Air-Gap Discharge ⁽¹⁾	Pins RIN1, RIN2, DOUT1, DOUT2 ⁽²⁾	±15000	

- (1) For RGT, D, DB and PW packages only: Minimum of 1-μF capacitor between VCC and GND is required to meet the specified IEC 61000-4-2 rating.
- (2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.4 Recommended Operating Conditions

See [Figure 8-1](#).⁽¹⁾

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	$V_{CC} = 3.3\text{ V}$	2	5.5	V
			$V_{CC} = 5\text{ V}$	2.4	5.5	
V_{IL}	Driver low-level input voltage	DIN	0		0.8	V
V_I	Receiver input voltage	RIN	-25		25	V
T_A	Operating free-air temperature		TRS3232EC	0	70	°C
			TRS3232EI	-40	85	

(1) C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TRS3232E						UNIT
		PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)	RGT (VQFN)	DYY (SOT-23- THN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.2	85.9	72.3	103.1	48.8	106.2	°C/W
$R_{\theta Jc\text{top}}$	Junction-to-case (top) thermal resistance	39.0	43.1	33.5	49.2	55.8	47.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	44.5	37.1	54.8	23.2	44.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.3	10.1	7.5	12.0	1.7	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53.8	44.1	37.1	54.1	23.2	43.7	°C/W
$R_{\theta Jc\text{bot}}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	9.0	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.6 Electrical Characteristics — Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 8-1](#)).⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _{CC}	Supply current	No load, V _{CC} = 3.3 V or 5 V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.7 Electrical Characteristics — Driver

over operating free-air temperature range (unless otherwise noted) (see [Figure 8-1](#)).⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at R _L = 3 kΩ to GND,	DIN = GND	5	5.4		V
V _{OL}	Low-level output voltage	DOUT at R _L = 3 kΩ to GND,	DIN = V _{CC}	–5	–5.4		V
I _{IH}	High-level input current	V _I = V _{CC}			±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND			±0.01	±1	μA
I _{OS} ⁽³⁾	Short-circuit output current	V _{CC} = 3.6 V,	V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V,	V _O = 0 V				
r _O	Output resistance	V _{CC} , V+, and V– = 0 V,	V _O = ±2 V	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.8 Electrical Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 8-1](#)).⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6	V _{CC} – 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
		V _{CC} = 5 V		1.8	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
		V _{CC} = 5 V	0.8	1.5		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})			0.3		V
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

5.9 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 8-1](#)).⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
Maximum data rate		R _L = 3 kΩ, C _L = 1000 pF, see Figure 6-1 One DOUT switching,	RGT package	250	500	kbps
		D, DB, DW and PW packages	150	250		
t _{sk(p)}	Driver pulse skew ⁽³⁾	R _L = 3 kΩ, C _L = 1000 pF, V _{CC} = 5 V Figure 6-2	RGT package		50	ns
		R _L = 3 kΩ to 7 kΩ, C _L = 150 pF to 2500 pF see Figure 6-2	D, DB, DW and PW packages		300	
SR(tr)	Driver slew rate, transition region (see Figure 6-1)	R _L = 3 kΩ to 7 kΩ, V _{CC} = 3.3 V	C _L = 150 pF to 1000 pF	6	30	V/μs
			C _L = 150 pF to 2500 pF	4	30	
t _{PLH}	Receiver propagation delay time, low- to high-level output	C _L = 150 pF, see Figure 6-3	RGT package		90	ns
			D, DB, DW and PW packages		300	
t _{PHL}	Receiver propagation delay time, high- to low-level output	C _L = 150 pF, see Figure 6-3	RGT package		100	ns
			D, DB, DW and PW packages		300	
t _{sk(p)}	Receiver pulse skew ⁽³⁾		RGT package		20	ns
			D, DB, DW and PW packages		300	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

Typical Characteristics

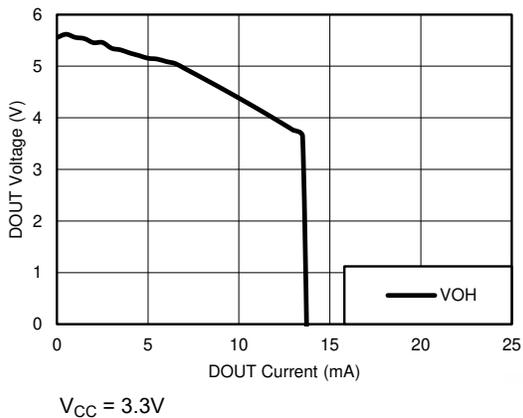


Figure 5-1. DOUT V_{OH} vs Load Current, Both Drivers Loaded

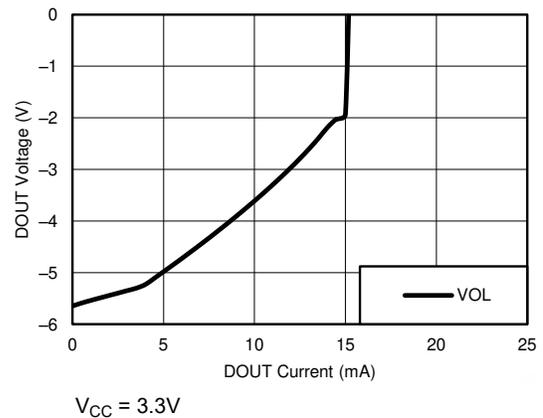


Figure 5-2. DOUT V_{OL} vs Load Current, Both Drivers Loaded

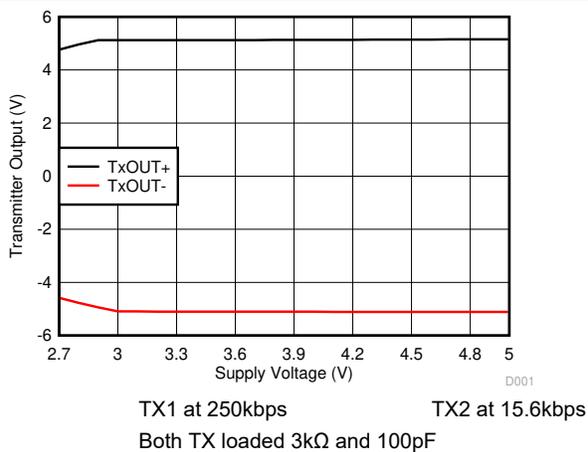


Figure 5-3. Driver Output Voltage vs. Supply Voltage, Both Drivers Loaded

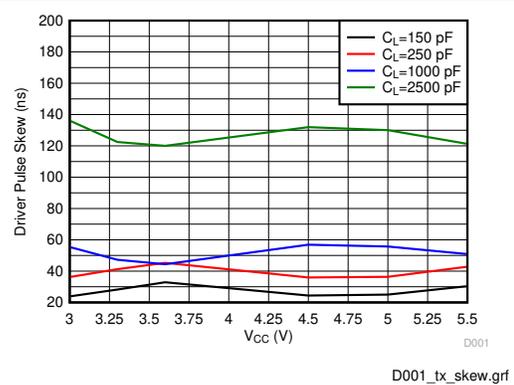


Figure 5-4. Driver Pulse Skew (RGT Package)

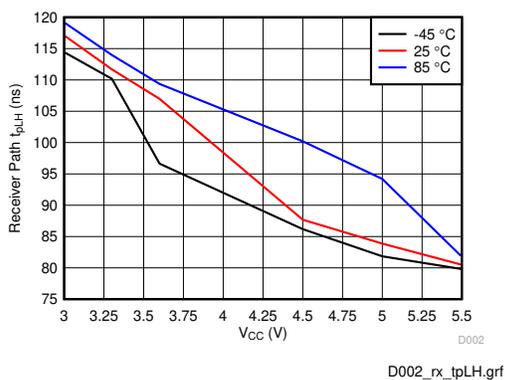


Figure 5-5. Receiver Path Low-to-High Propagation Delay (RGT Package)

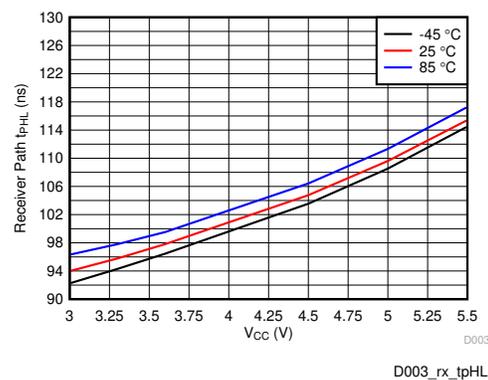


Figure 5-6. Receiver Path High-to-Low Propagation Delay (RGT Package)

Typical Characteristics

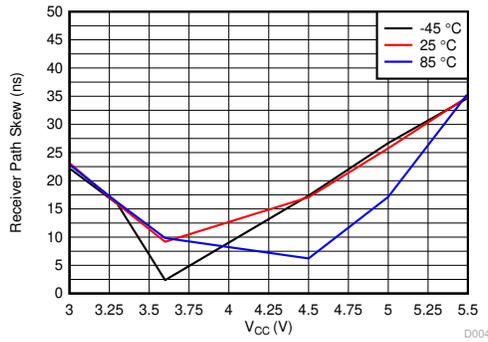
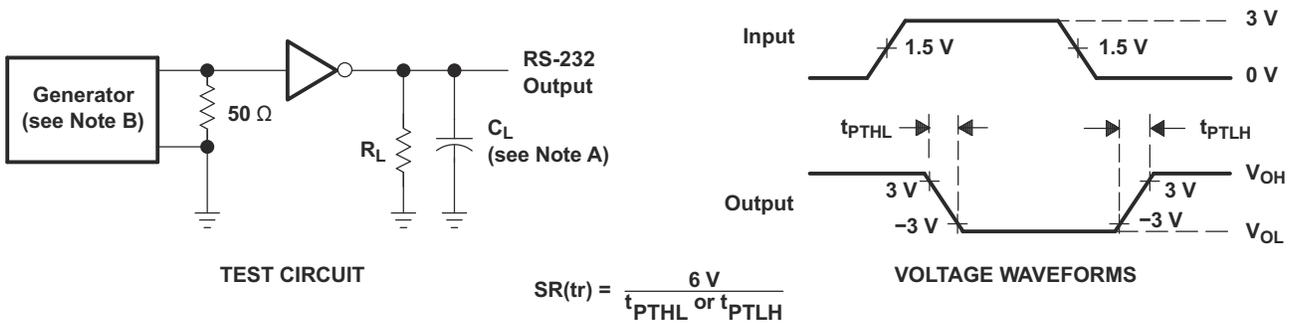


Figure 5-7. Receiver Path Skew ($|t_{pHL} - t_{pLH}|$) (RGT Package)

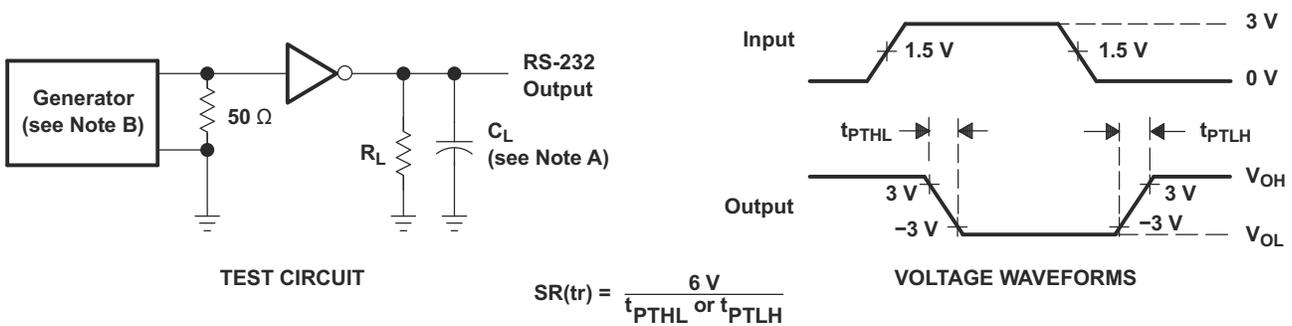
6 Parameter Measurement Information



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_0 = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$

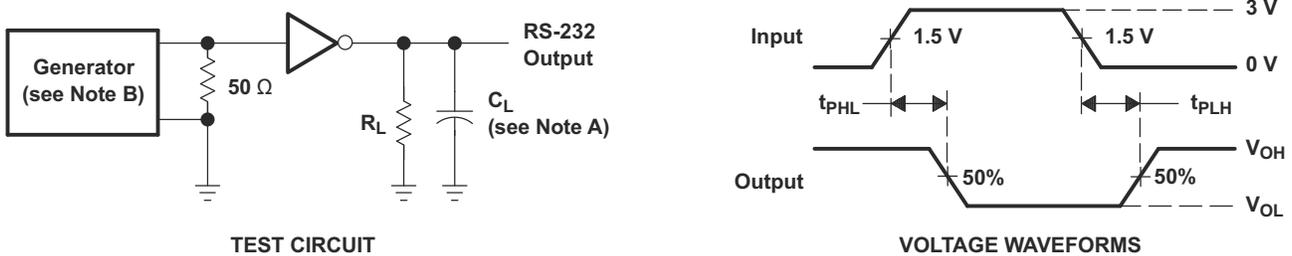
Figure 6-1. Driver Slew Rate



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_0 = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$

Figure 6-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: $Z_0 = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$

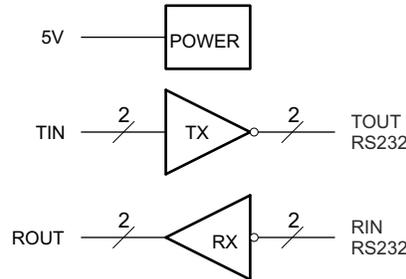
Figure 6-3. Receiver Propagation Delay Times

7 Detailed Description

7.1 Overview

The TRS3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with IEC61000-4-2 ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. The device operates at data signaling rates up to 250kbps and a maximum of 30V/μs driver output slew rate. Outputs are protected against shorts to ground.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors.

7.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

7.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

7.4 Device Functional Modes

Table 7-1 and Table 7-2 list the functional modes of the drivers and receivers of TRS3232E.

Table 7-1. Each Driver (1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Table 7-2. Each Receiver (1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

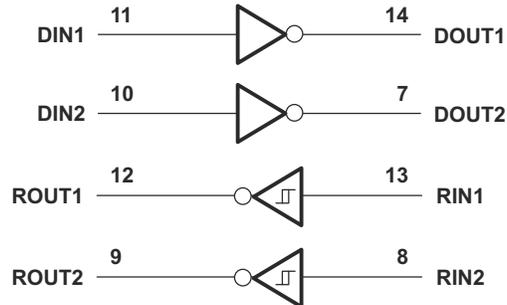


Figure 7-1. Logic Diagram

7.4.1 V_{CC} Powered by 3V to 5.5V

The device is in normal operation.

7.4.2 V_{CC} Unpowered, $V_{CC} = 0V$

When TRS3232E is unpowered, it can be safely connected to an active remote RS232 device.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

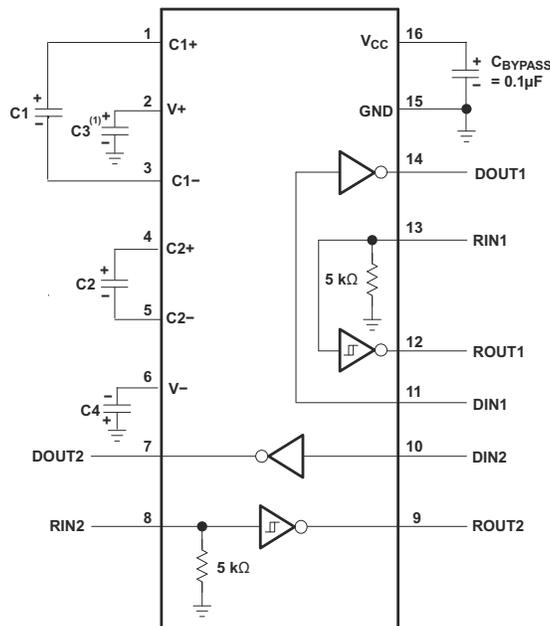
8.1 Application Information

The TRS3232E interfaces logic lines from a UART or microcontroller to the voltage and current levels needed for RS232 communication. The TIN inputs will accept 5V logic with 3.3V V_{CC} supply. All baud rates up to 250kbps are supported.

It is important to use the correct capacitors for the V_{CC} voltage. This will reduce ripple voltage on the TOUT outputs. If only one driver is needed, the unused driver input should be connected to V_{CC} or ground.

8.2 Typical Application

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable. For proper operation, add capacitors as shown in [Table 8-1](#).



A. C3 can be connected to V_{CC} or GND

Resistor values shown are nominal.

Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 8-1. Typical Operating Circuit and Capacitor Values

Table 8-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3V ± 0.3V	0.1μF	0.1μF
5V ± 0.5V	0.047μF	0.33μF
3V ± 5.5V	0.1μF	0.47μF

8.2.1 Design Requirements

The recommended V_{CC} is 3.3V or 5V. 3V to 5.5V is also possible.

The maximum recommended bit rate is 250kbps.

8.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on V_{CC} level for best performance.

8.2.3 Application Curve

Figure 8-2 curves are for 3.3V VCC and 250kbps alternative bit data stream.

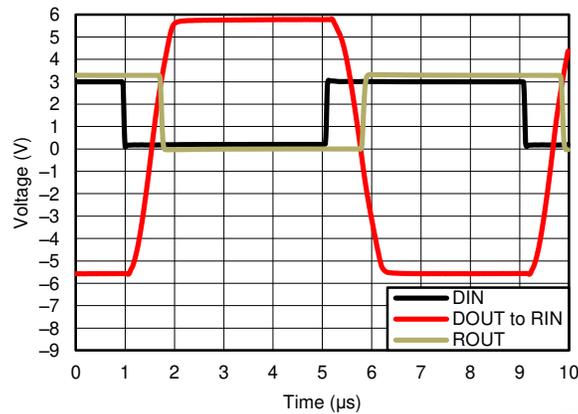


Figure 8-2. 250kbps Driver to Receiver Loopback Timing Waveform, V_{CC} = 3.3V

8.3 Power Supply Recommendations

The supply voltage, V_{CC} , should be between 3V and 5.5V. Select the values of the charge-pump capacitors using Table 8-1.

8.4 Layout

8.4.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

8.4.2 Layout Example

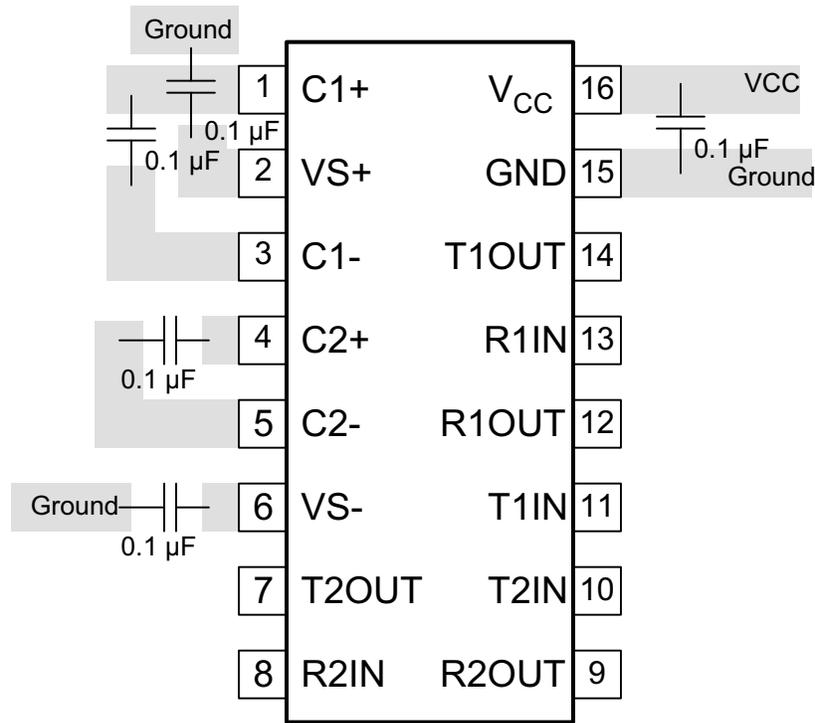


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2021) to Revision E (December 2024)	Page
• Changed the <i>Device Information</i> table to the <i>Package Information</i> table.....	1
• Added the SOT-23-THN (DYY) package to the data sheet.....	1
• Added Note 2 to the <i>ESD ratings - IEC Specifications</i>	4

Changes from Revision C (June 2021) to Revision D (June 2021)	Page
• Added <i>Applications</i> : Industrial PCs, Wired networking, and Data center and enterprise computing.....	1
• Changed the table note in the <i>ESD Ratings - IEC Specifications</i> to make it applicable to D, DB and PW packages.	4
• Changed the thermal parameter values for D, DB and PW packages in the <i>Thermal Information</i> table.....	5

Changes from Revision B (October 2017) to Revision C (June 2021)	Page
• Added RGT package to the <i>Device Information</i>	1
• Added the RGT <i>Pin Configuration</i>	3
• Added the <i>ESD Ratings - IEC Specifications</i>	4
• Added RGT to the <i>Thermal Information</i>	5
• Added RGT package to the <i>Switching Characteristics</i>	7
• Changed the capacitor value From: 1 µf To: 0.1 µf in the <i>Layout Diagram</i>	15

Changes from Revision A (July 2015) to Revision B (October 2017)	Page
• Added Feature: Interoperable with RS-232 down to 2.7-V V_{CC}	1
• Added Figure 5-3	8

Changes from Revision * (April 2007) to Revision A (July 2015)	Page
• Deleted <i>Ordering Information</i> table.....	1
• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes, Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS3232ECDR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC
TRS3232ECDR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC
TRS3232ECDW	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	0 to 70	TRS3232EC
TRS3232ECDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC
TRS3232ECDWR.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC
TRS3232ECPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	RS32EC
TRS3232ECPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32EC
TRS3232EIDBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI
TRS3232EIDBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI
TRS3232EIDR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI
TRS3232EIDR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI
TRS3232EIDRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI
TRS3232EIDRG4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI
TRS3232EIDW	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-40 to 85	TRS3232EI
TRS3232EIDWR	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-40 to 85	TRS3232EI
TRS3232EIDYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI
TRS3232EIDYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI
TRS3232EIPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI
TRS3232EIPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI
TRS3232EIPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI
TRS3232EIRGTR	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3232
TRS3232EIRGTR.A	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3232

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

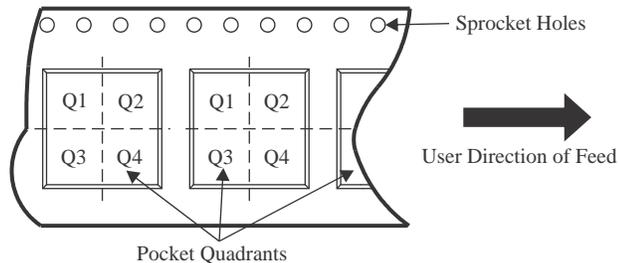
OTHER QUALIFIED VERSIONS OF TRS3232E :

- Automotive : [TRS3232E-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


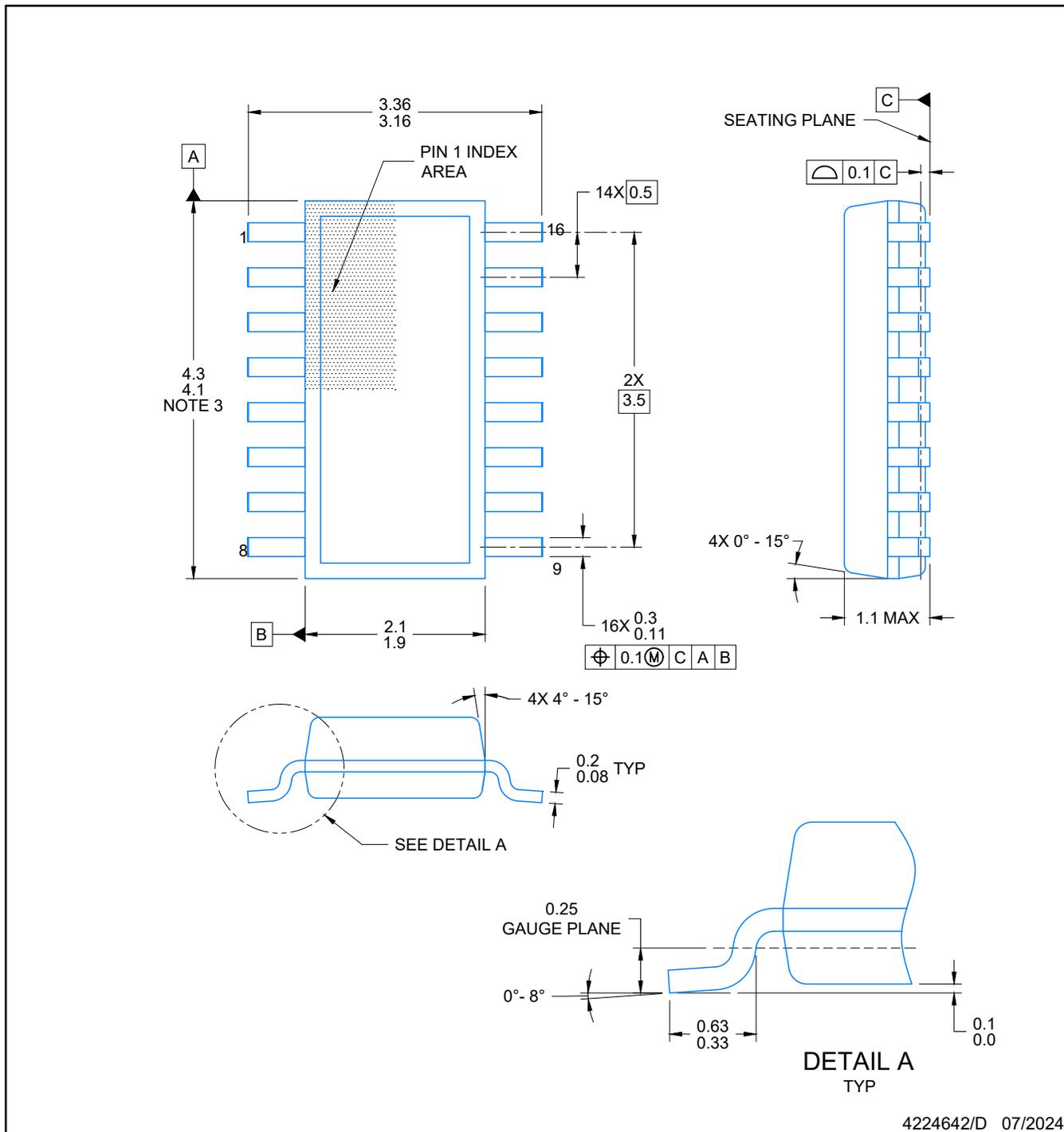
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3232EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRS3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232EIDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232EIDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TRS3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3232EIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

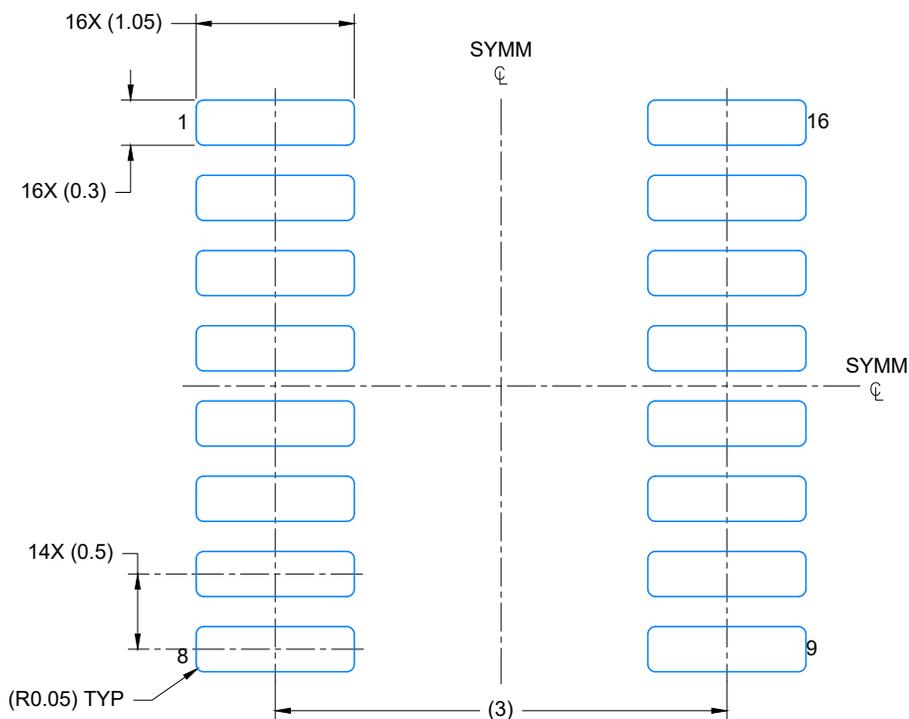
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3232ECDR	SOIC	D	16	2500	353.0	353.0	32.0
TRS3232ECDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TRS3232ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRS3232EIDBR	SSOP	DB	16	2000	353.0	353.0	32.0
TRS3232EIDR	SOIC	D	16	2500	353.0	353.0	32.0
TRS3232EIDR	SOIC	D	16	2500	353.0	353.0	32.0
TRS3232EIDRG4	SOIC	D	16	2500	353.0	353.0	32.0
TRS3232EIDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TRS3232EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TRS3232EIRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0



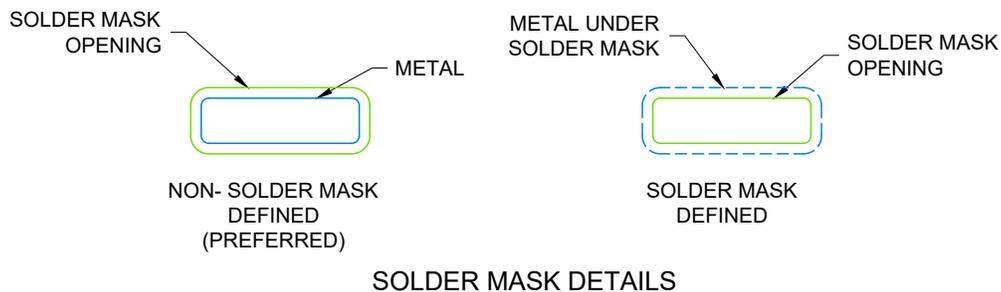
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

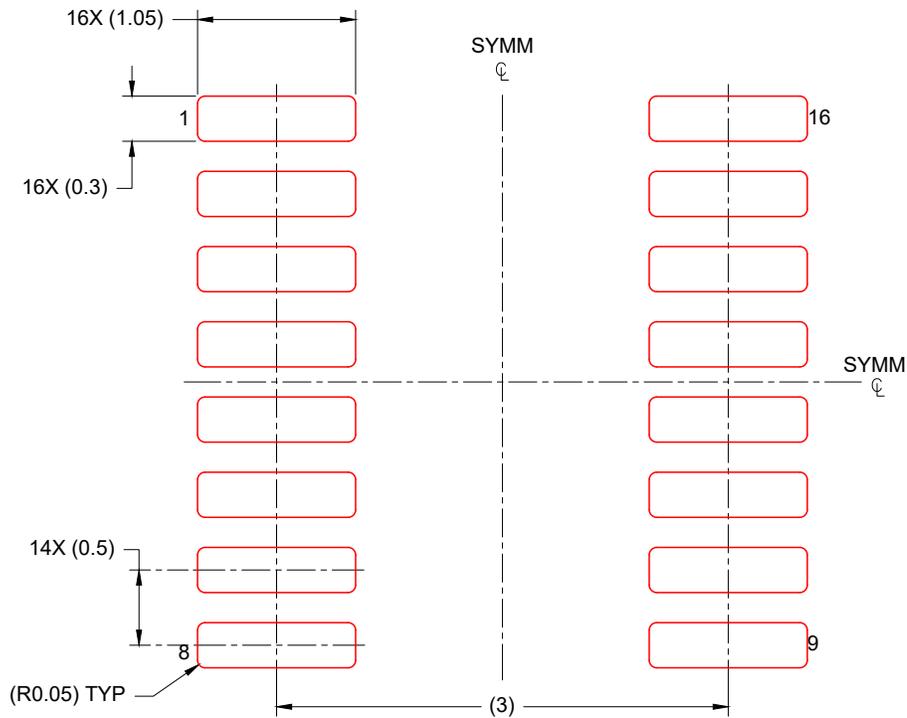


SOLDER MASK DETAILS

4224642/D 07/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

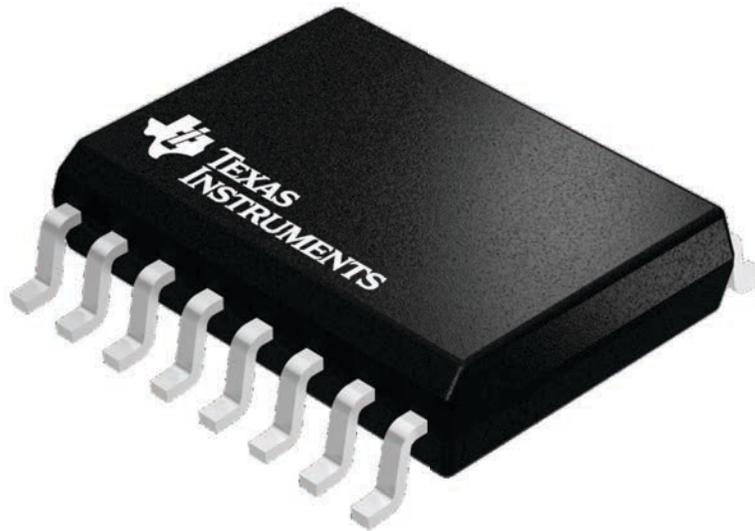
DW 16

SOIC - 2.65 mm max height

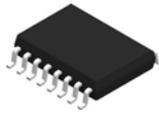
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



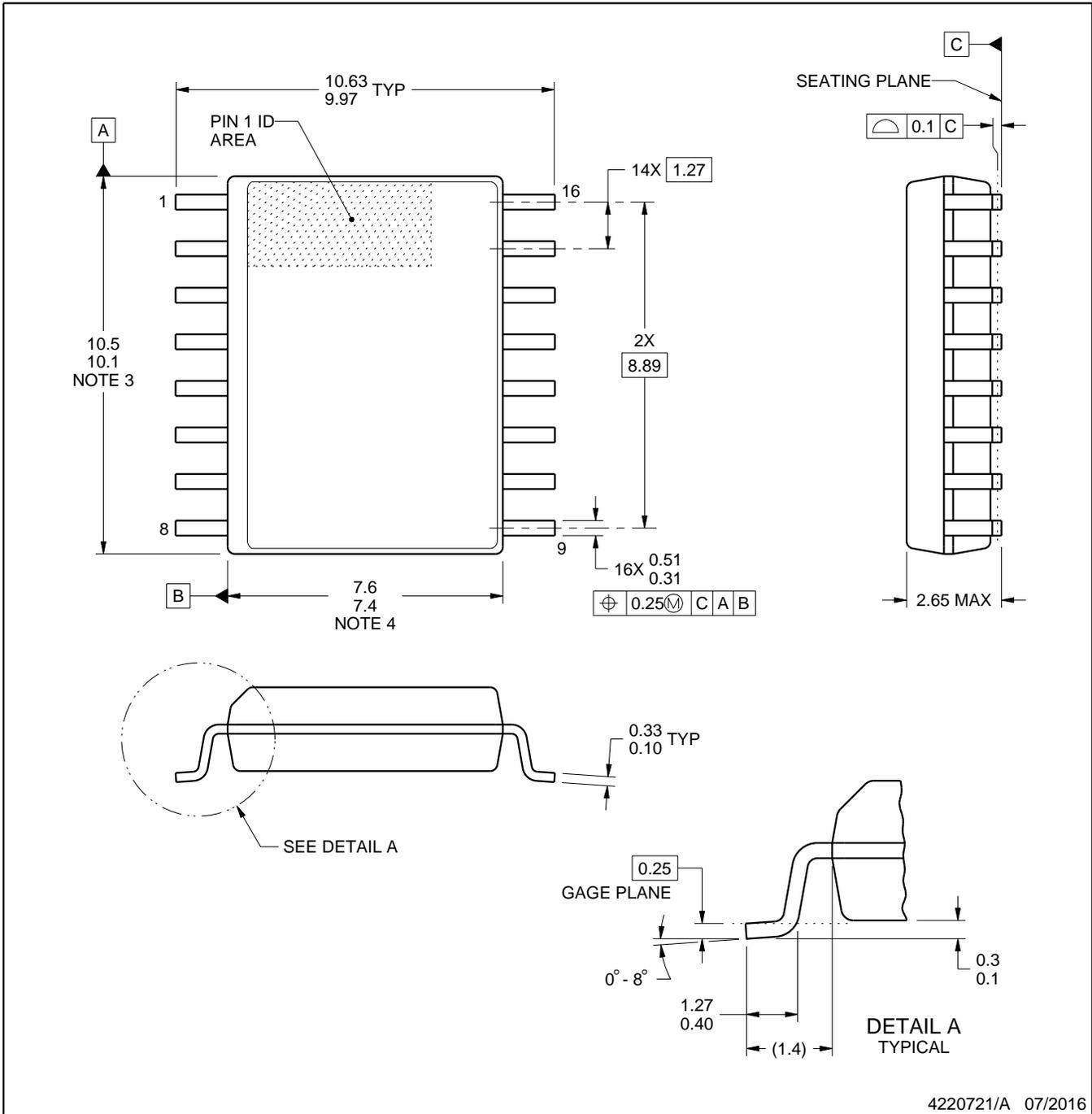
4224780/A



DW0016A

PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

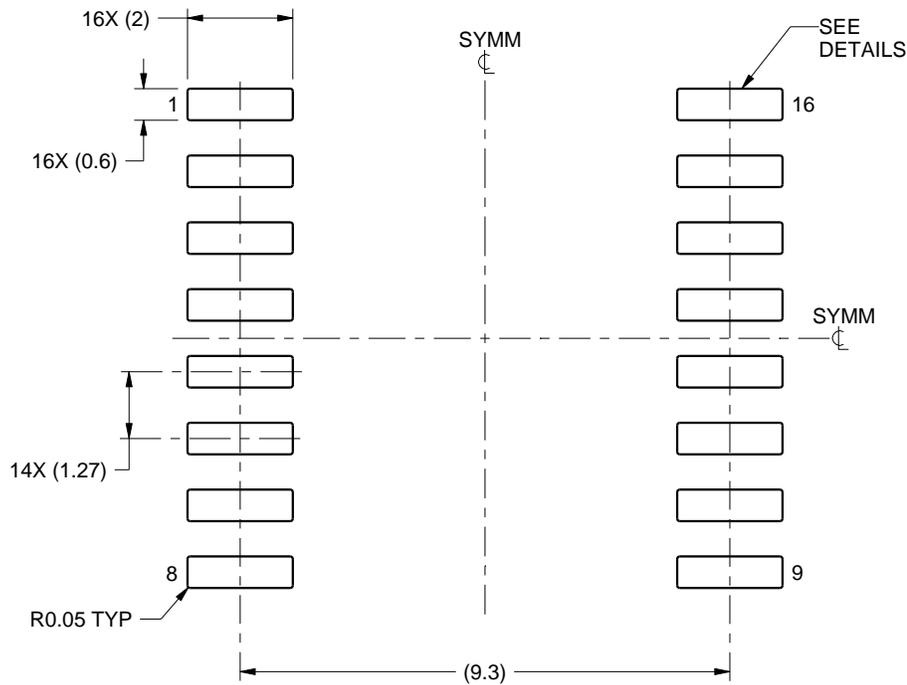
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

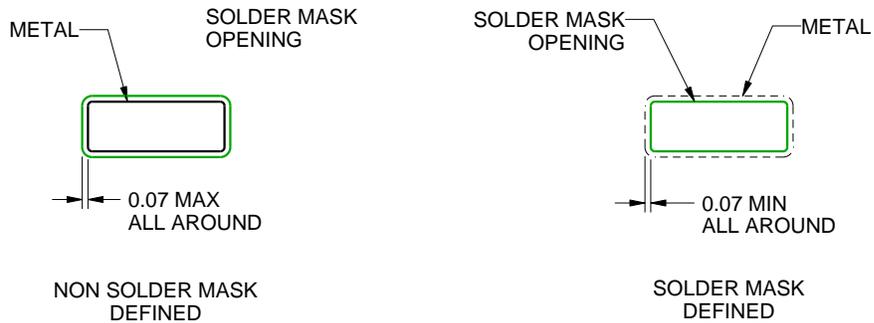
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

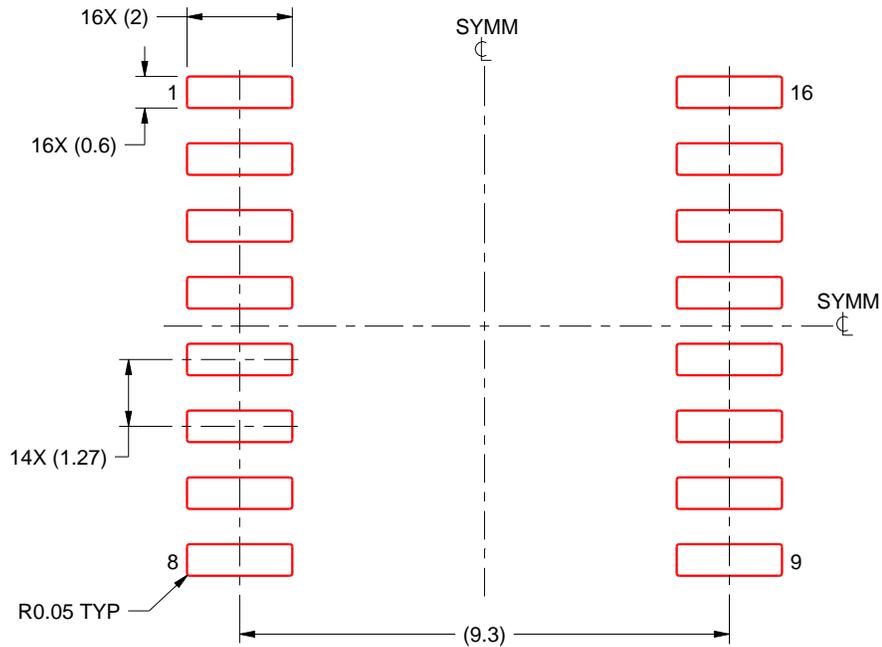
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC

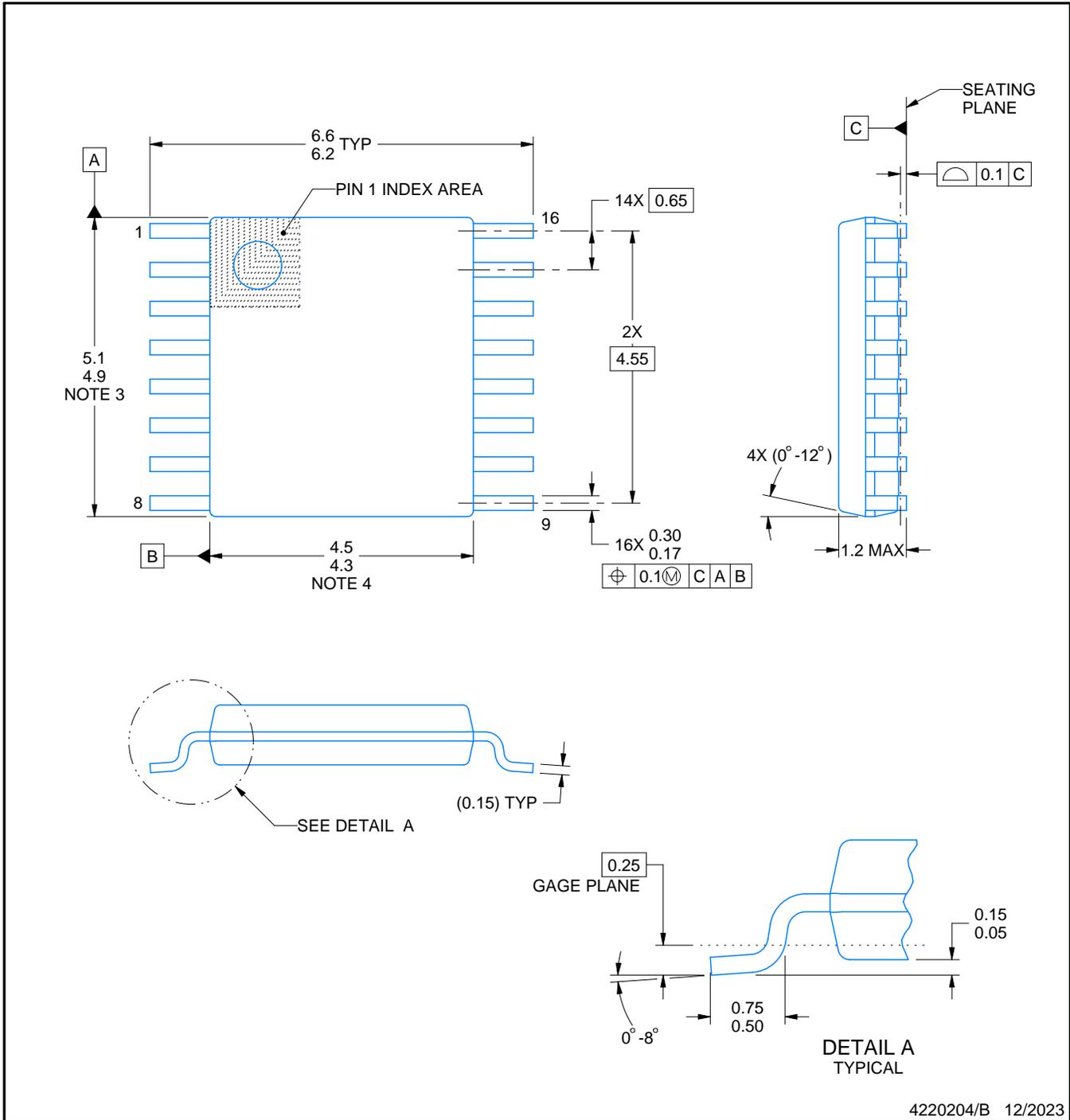


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220204/B 12/2023

NOTES:

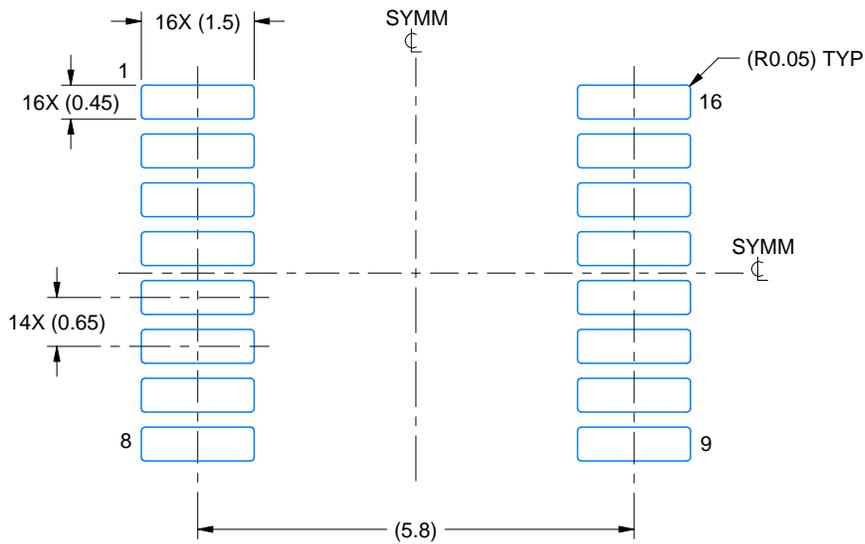
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

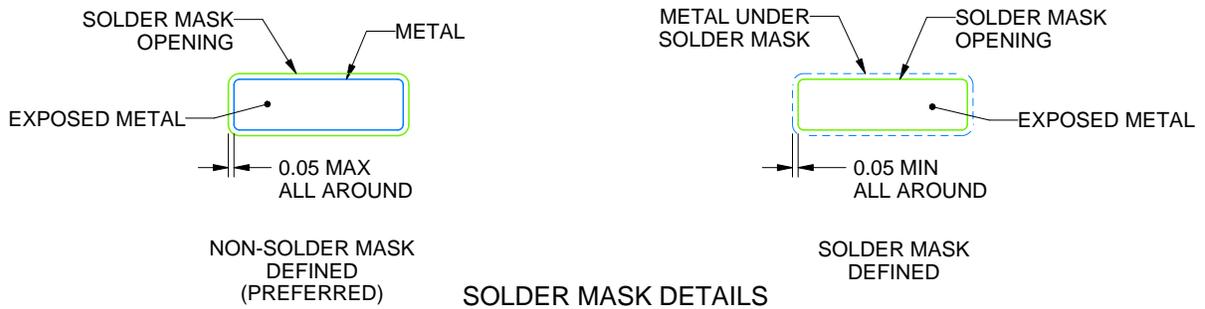
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

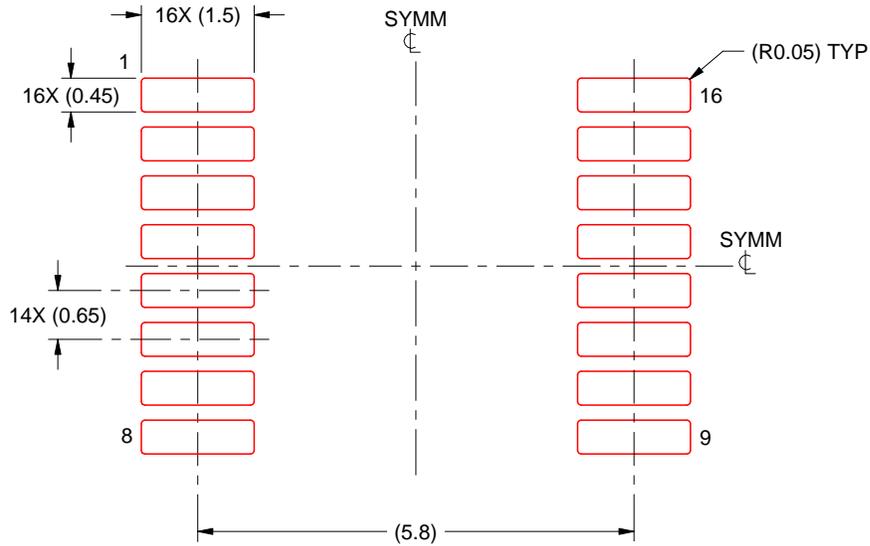
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

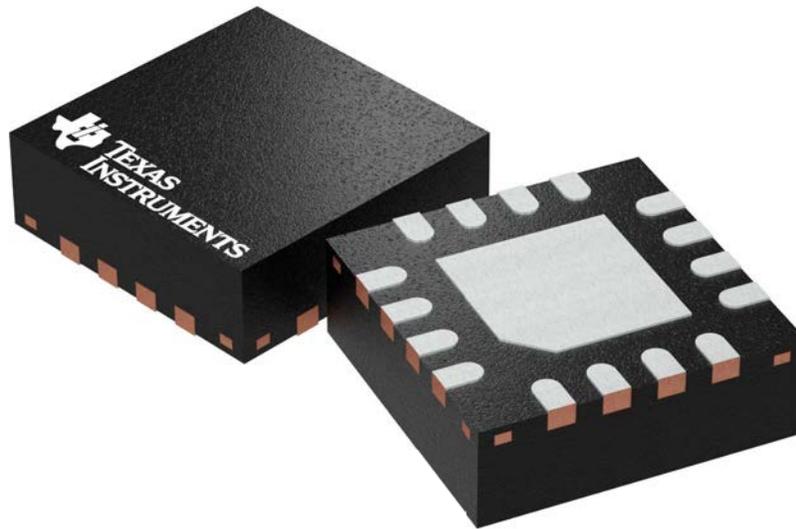
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGT 16

GENERIC PACKAGE VIEW

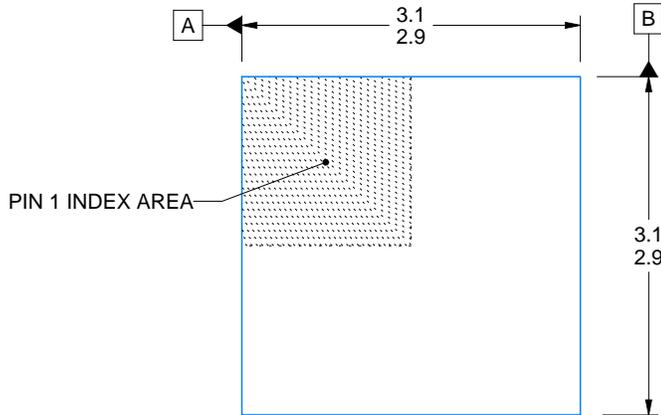
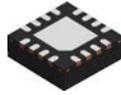
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

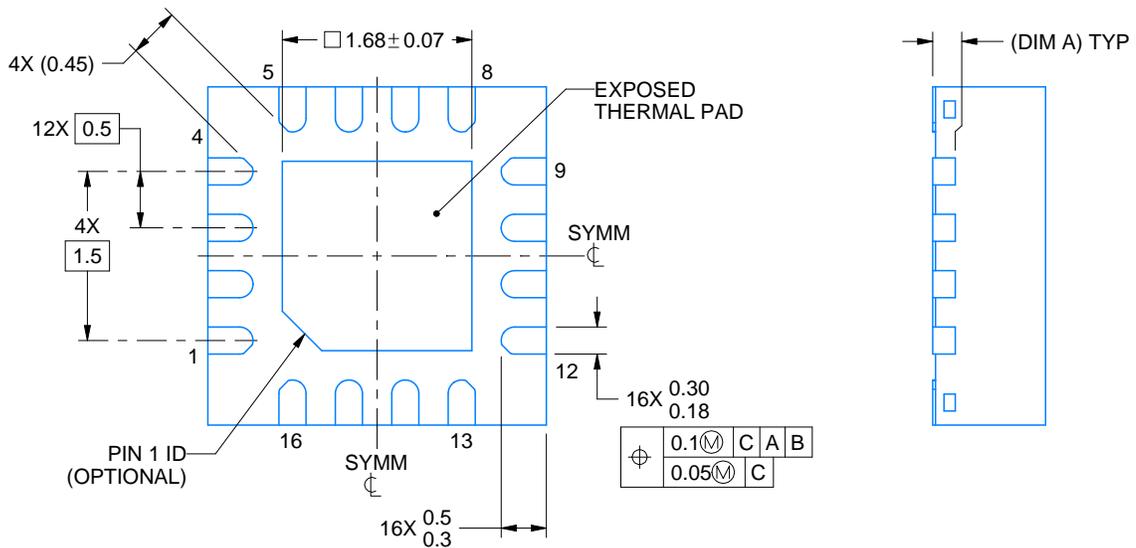
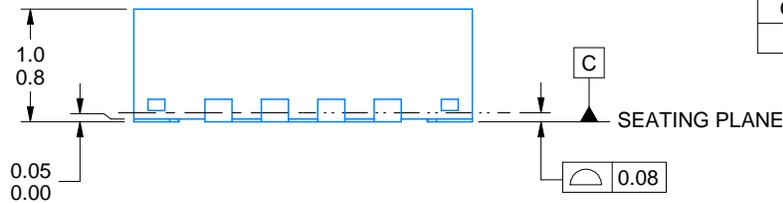


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4222419/E 07/2025

NOTES:

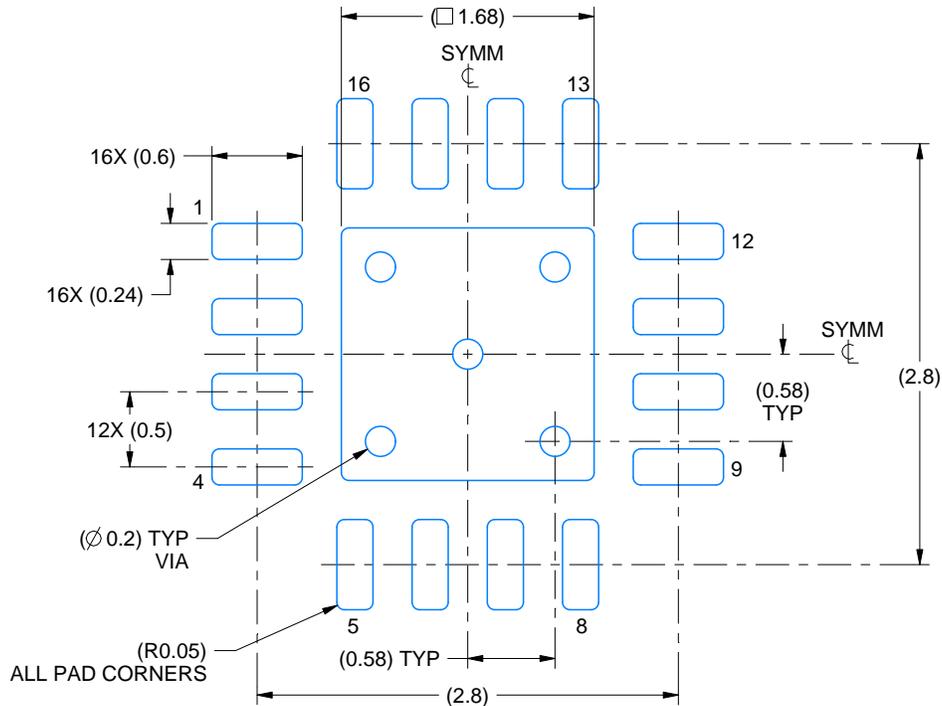
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

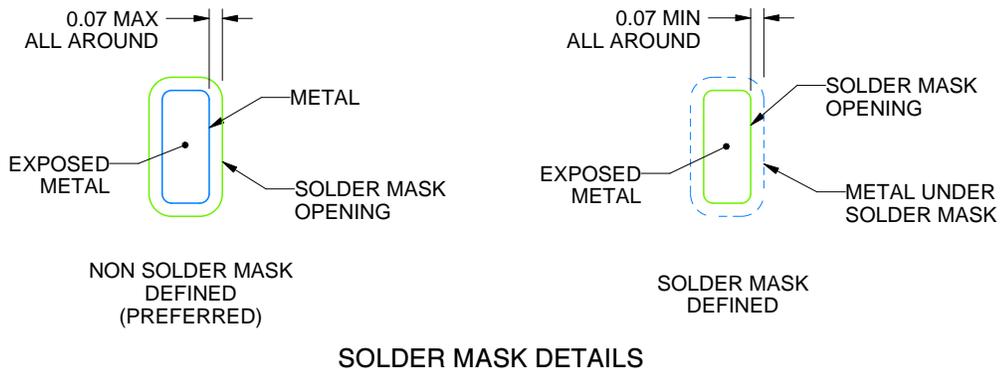
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

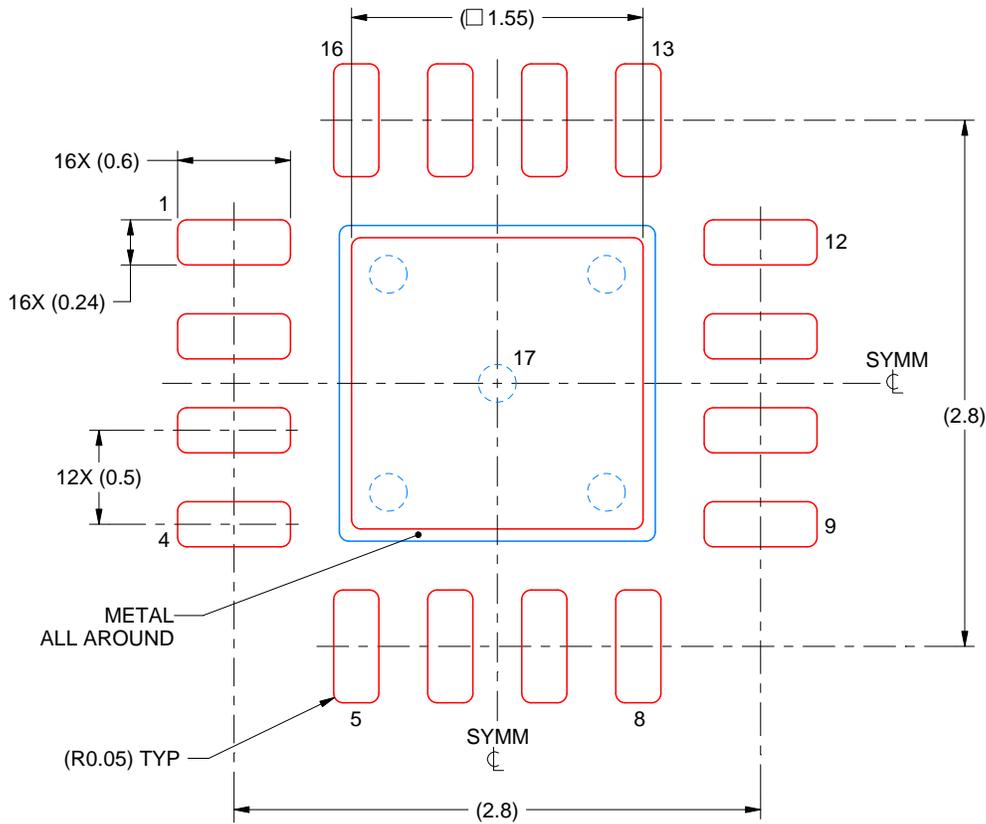
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

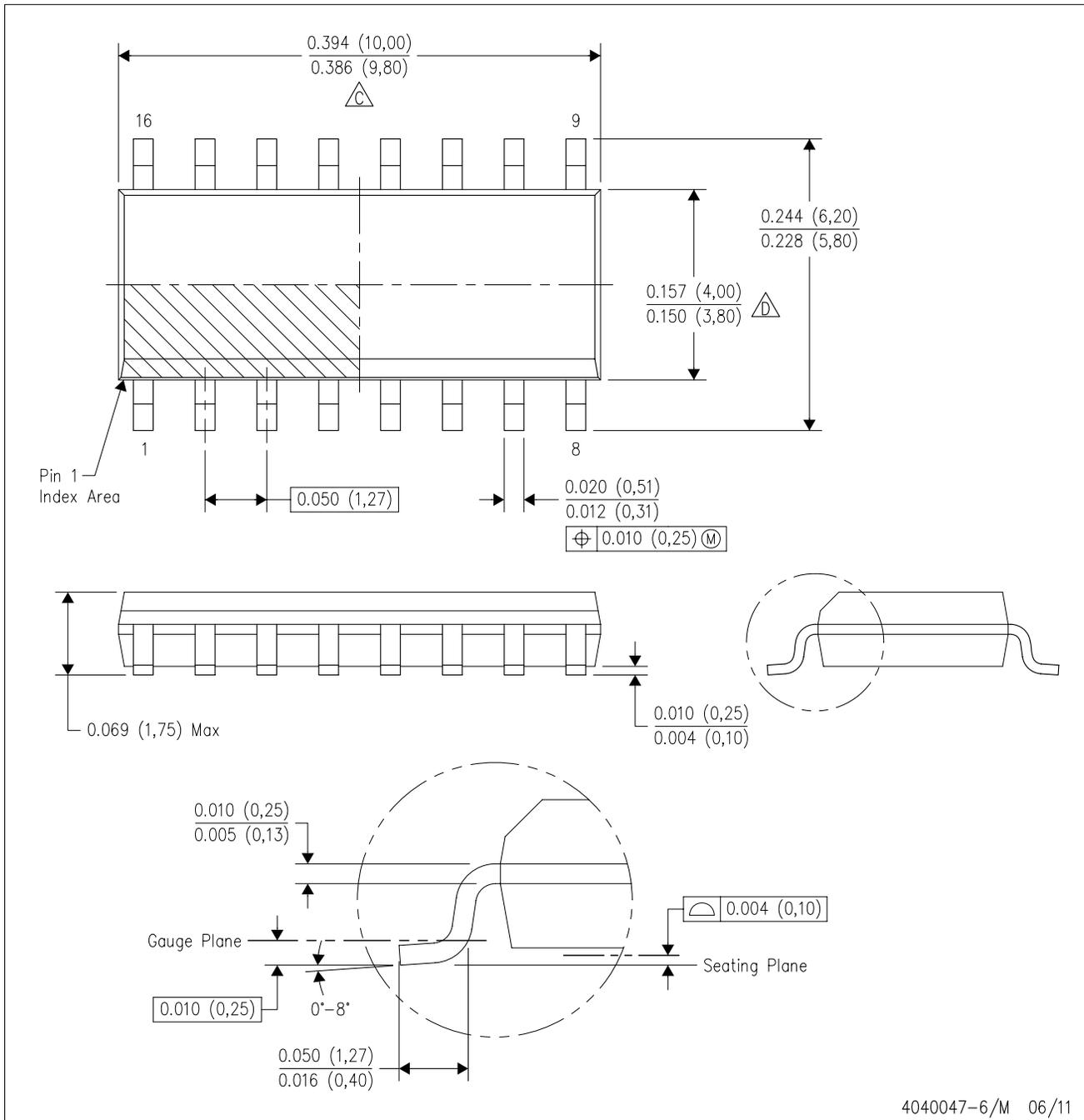
4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

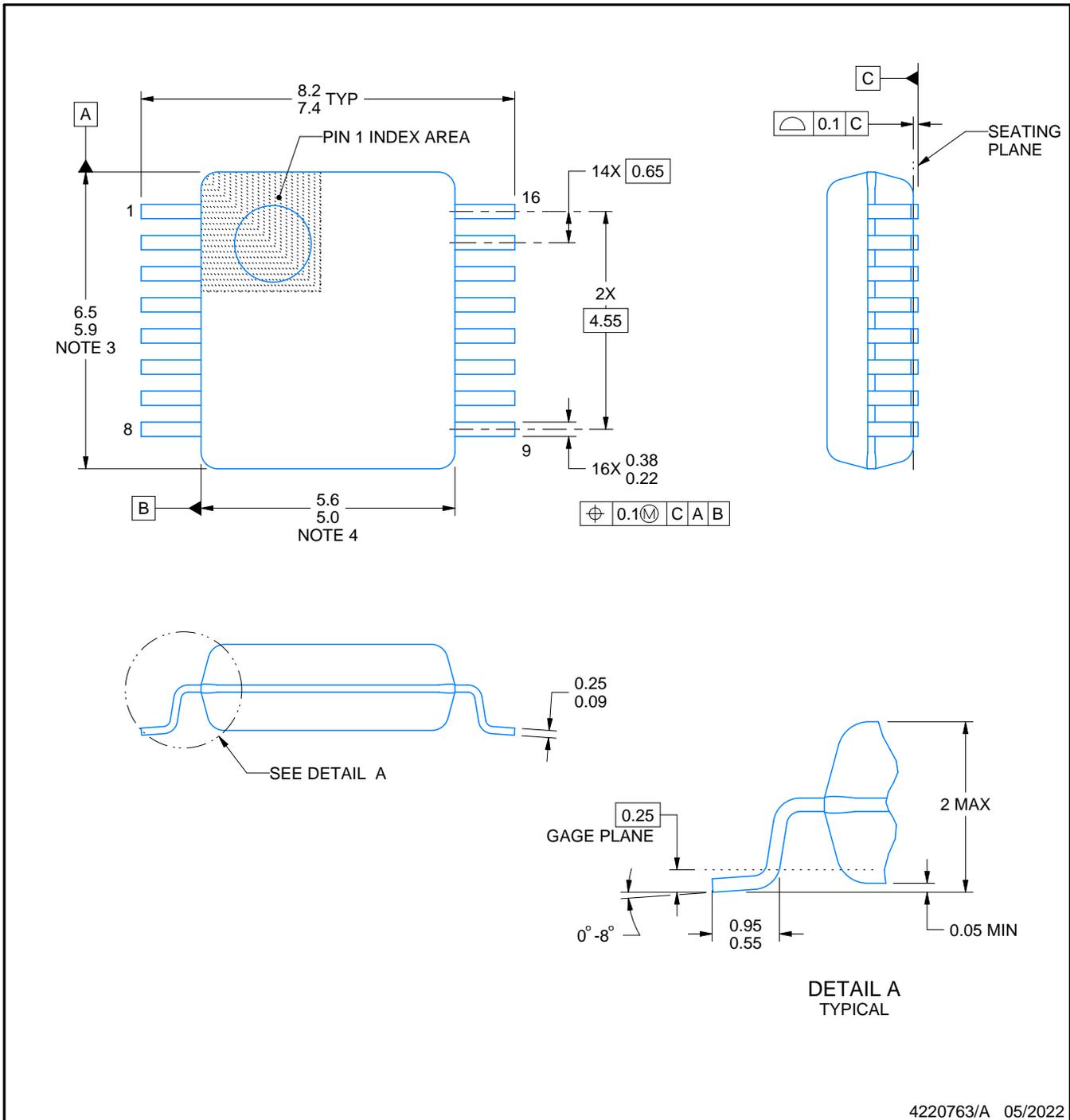
DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

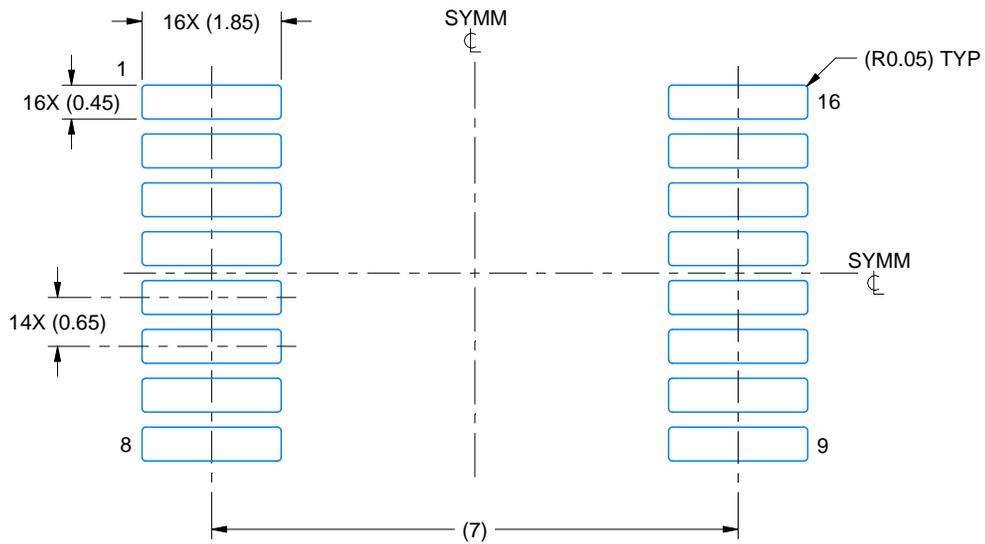
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

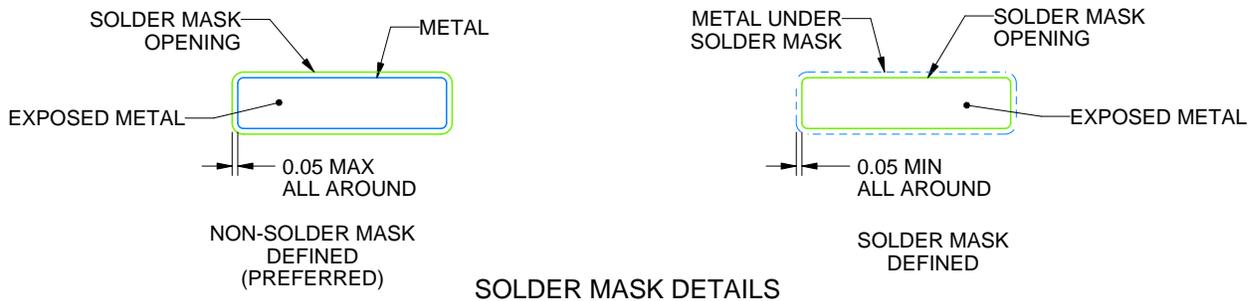
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

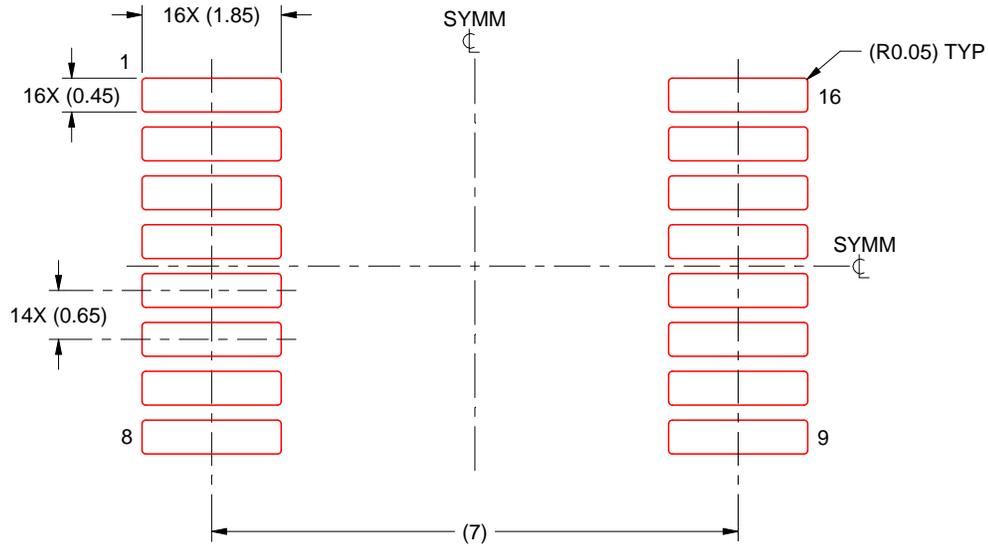
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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