TPSM843321 3.8V to 18V, 3A, Synchronous Buck Power Module With User Selectable Mode

1 Features

- Configured for a wide range of applications
  - 3.8V to 18V input voltage range
  - 0.6V to 12V output voltage range
  - Up to 3A continuous output current
  - 0.6V ±1% reference voltage (–40°C to 125°C)
  - Low quiescent current of 28uA (typical)
  - 70ns, 114ns minimum switching on, off-time
  - 8us maximum switching on-time
  - 98% maximum duty cycle
- Ease of use and small design size
  - Peak current control mode with internal compensation
  - 200kHz to 2.2MHz selectable frequency
  - Synchronizable to an external clock (support phase shift): 200kHz to 2.2MHz
  - Selectable PFM / FCCM at light load condition
  - Selectable adjustable soft-start time / power-good indicator function
  - Good EMI performance with frequency spread spectrum and optimized pinout
  - Hiccup overcurrent (OC) limit for both high-side and low-side MOSFETs
  - Non-latched protections for overtemperature protection (OTP), overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), and undervoltage lockout (UVLO)
  - Integrated bootstrap capacitor and inductor to support easy PCB layout
  - Operating junction temperature of –40°C to 125°C
  - 3.3mm × 4.5mm × 2mm QFN package
- Create a custom design with the TPSM843321 using the WEBENCH® Power Designer

2 Applications

- Medical and healthcare
- Test and measurement
- Building automation
- Wired networking, wireless infrastructure
- Distributed power systems with 5V and 12V input

3 Description

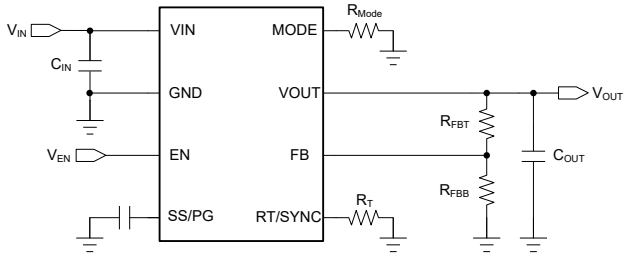
The TPSM843321 is a high-efficiency, high-power density, and easy-to-use, synchronous buck power module with high design flexibility. With operating input voltage ranging from 3.8V to 18V, the TPSM843321 is designed for systems powered from 5V, 12V power-bus rails. The device supports up to 3A continuous output current and 98% maximum duty cycle.

TPSM843321 uses fixed frequency peak current control with internal compensation for fast transient response and good line and load regulation. With the optimized internal loop compensation, the device eliminates the need for external compensation over a wide output voltage range and switching frequency.

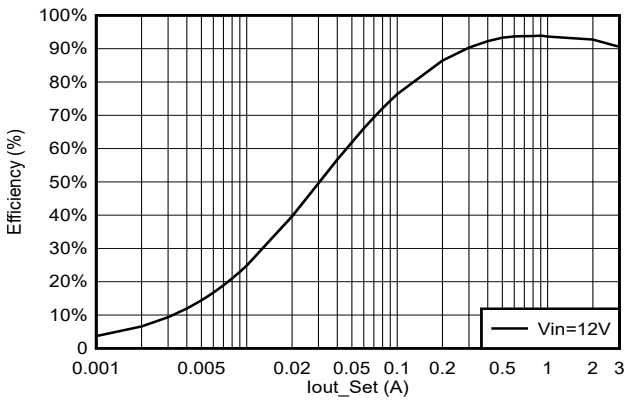
Package Information

PRT NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPSM843321	RCJ (QFN-FCMOD, 9)	3.3mm × 4.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



TPSM843321 Efficiency, V_{OUT} = 5V, f_{SW} = 1000kHz, FCCM

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

TPSM843321 allows high design flexibility with wide supported switching frequency of 200kHz – 2.2MHz set by the RT/SYNC pin. The device has the option for pulse frequency modulation (PFM), forced continuous conduction modulation (FCCM) at light load condition, and adjustable soft-start (SS) time / power-good (PG) indicator with different configuration of the MODE pin.

TPSM843321 provides protection functions including thermal shutdown, input undervoltage lockout, cycle-by-cycle current limit, and hiccup short-circuit protection. TPSM843321 is available in a 9-pin, 3.3mm × 4.5mm, QFN package, and the pinout is available for single-layer PCB layout. The junction temperature is specified from –40°C to 125°C.

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4 Pin Configuration and Functions

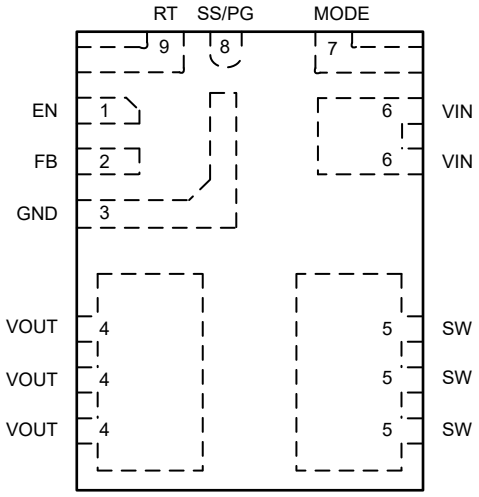

Figure 4-1. 9-Pin RCJ QFN-FCMOD, 3.3mm × 4.5mm Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN	1	A	Enable input to the converter. Driving EN high or leaving this pin floating enables the converter. An external resistor divider can be used to implement an adjustable V_{IN} UVLO function.
FB	2	A	Output feedback input. Connect FB to the tap of an external resistor divider from the output to GND to set output voltage.
GND	3	G	Ground pin. Connected to the source of the low-side FET as well as the ground pin for the controller circuit. Connect to system ground and the ground side of C_{IN} and C_{OUT}. The path to C_{IN} must be as short as possible.
VOUT	4	P	Output voltage. This pin is connected to the internal buck inductor. Connect the pin to the output load and connect external output capacitors between this pin and GND.
SW	5	P	Switching node. *Do not place any external component on this pin or connect to any signal.* The amount of copper placed on this pin must be kept to a minimum to prevent issues with noise and EMI.
VIN	6	P	Supply input pin to internal LDO and high-side FET. Input bypass capacitors must be directly connected to this pin and GND.
MODE	7	A	Mode selection pin in light load condition and Power-Good / Soft-Start function. See Mode Selection for details.
SS/PG	8	A	This pin can be a soft-start function or Power-Good function depending on the mode pin configuration. If the soft-start function is selected, an external capacitor connected from this pin to GND defines the rise time for the internal reference voltage. If the Power-Good function is selected, this pin is an open drain power-good indicator, which is asserted low if output voltage is out of PG threshold, overvoltage, or if the device is under thermal shutdown, EN shutdown, or during soft start.
RT/SYNC	9	A	Frequency select and external clock synchronization. A resistor to ground sets the switching frequency of the device. An external clock can also be applied to this pin to synchronize the switching frequency. See Section 6.3.5 for details.

(1) A = Analog, P = Power, G = Ground

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5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +125°C , unless otherwise noted(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	20	V
	EN	–0.3	6	
	FB	–0.3	6	
Output voltage	VOUT	–0.3	12	
	SS/PG	–0.3	6	
	MODE	–0.3	6	
	RT/SYNC	–0.3	6	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1ms, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000Hz		20	G
T_J	Operating junction temperature(2)	–40	125	°C
T_{stg}	Storage temperature	–65	125	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +125°C, unless otherwise noted(1)

		MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	3.8		18	V
	EN	–0.1		5.5	
	FB	–0.1		5.5	
	SS/PG	–0.1		5.5	
	MODE	–0.1		5.5	
Output voltage	V_{OUT}	0.8		12	
Ouput current	I_{OUT}	0		3	A
Temperature	Operating junction temperature, T_J	–40		125	°C

(1) The *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but do not specify specific performance limits. For compliant specifications, see the *Electrical Characteristics*.

5.4 Thermal Information

THERMAL METRIC(1)		TPSM843321	UNIT
		RCJ (QFN-FCMOD), 9 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.2	°C/W

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THERMAL METRIC(1)		TPSM843321 RCJ (QFN-FCMOD), 9 PINS	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W
$R_{\theta JA_EVM}$	Junction-to-ambient thermal resistance on official EVM board	46	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product. Typical values correspond to T_J = 25°C, V_{IN} = 12V. Minimum and maximum limits are based on T_J = –40°C to +125°C, V_{IN} = 3.8V to 18V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		3.8		18	V
I_Q	Nonswitching quiescent current	EN = 5V, V_{FB} = 0.65V, V_{IN} = 12V, PFM		28	34	µA
		EN = 5V, V_{FB} = 0.65V, V_{IN} = 12V, FCCM		40	47	
I_{SHDN}	Shutdown supply current	V_{EN} = 0V, V_{IN} = 12V		3	5.5	µA
V_{IN_UVLO}	Input undervoltage lockout thresholds	Rising threshold	3.4	3.6	3.8	V
		Falling threshold	3.2	3.4	3.6	V
		Hysteresis		200		mV
ENABLE (EN PIN)						
V_{EN_RISE}	Enable threshold	Rising enable threshold		1.15	1.22	V
V_{EN_FALL}	Disable threshold	Falling disable threshold	0.9	1		V
I_p	EN pullup current	V_{EN} = 1.0V		0.7		µA
I_h	EN pullup hysteresis current			1.76		µA
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	FB voltage	T_J = 25°C	596	600	604	mV
		T_J = 0°C to 85°C	595	600	605	mV
		T_J = –40°C to 125°C	594	600	606	mV
I_{FB}	Input leakage current	V_{IN} = 12V, V_{FB} = 0.8V, T_J = 25°C			0.1	µA
CURRENT LIMIT						
I_{HS_LIMIT}	High-side MOSFET current limit	V_{IN} = 12V	5.6	6.5	7.4	A
I_{LS_LIMIT}	Low-side MOSFET current limit	V_{IN} = 12V	3.6	4.5	5.6	A
I_{LS_NOC}	Reverse current limit	V_{IN} = 12V	2	3	4.2	A
I_{PEAK_MIN}	Minimum peak inductor current	V_{IN} = 12V		1.2		A
SOFT START (SS PIN)						
I_{SS}	Soft-start charge current		3.5	5.5	6.5	µA
T_{SS}	Fixed internal soft-start time	Mode with PG function. Time from 0%V_{out}-90%V_{out}		3.6		ms
POWER GOOD (PG PIN)						

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5.5 Electrical Characteristics (continued)

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product. Typical values correspond to T_J = 25°C, V_{IN} = 12V. Minimum and maximum limits are based on T_J = –40°C to +125°C, V_{IN} = 3.8V to 18V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PGTH}	PG threshold, V_{FB} percentage	V_{FB} falling, PG high to low		85%		
		V_{FB} rising, PG low to high		90%		
		V_{FB} falling, PG low to high		107%		
		V_{FB} rising, PG high to low		115%		
T_{PG_R}	PG delay time	PG from low to high		70		µs
T_{PG_F}	PG delay time	PG from high to low		13		µs
$V_{IN_PG_VALID}$	Minimum V_{IN} for valid PG output	Measured when PG < 0.5V with 100kΩ pullup to external 5V		2	2.5	V
V_{PG_OL}	PG output low-level voltage	I_{PG} = 0.5mA			0.3	V
I_{PG_LK}	PG leakage current when open drain is high	V_{PG} = 5.5V	–1		1	µA
OSCILLATOR FREQUENCY (RT PIN)						
f_{SW}	Switching center frequency	RT = floating	450	500	550	kHz
		RT = GND	870	1000	1130	
V_{SYNC_HI}	SYNC clock high level threshold		1.7			V
V_{SYNC_LO}	SYNC clock low level threshold				0.9	V
t_{ON_MIN} (1)	Minimum ON pulse width			70		ns
t_{OFF_MIN} (1)	Minimum OFF pulse width			114		ns
t_{ON_MAX} (1)	Maximum ON pulse width			8		µs
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP detect (L→H)	112%	115%	118%	
		Hysteresis		8%		
V_{UVP}	Output UVP threshold	UVP detect (H→L)		65%		
		Hysteresis		6%		
t_{hiccup_ON}	UV hiccup ON time before entering hiccup mode after soft start ends			256		µs
t_{hiccup_OFF}	UV hiccup OFF time before restart			9.8		cycles
THERMAL SHUTDOWN						
T_{SHDN} (1)	Thermal shutdown threshold	Shutdown temperature		165		°C
T_{HYS} (1)		Hysteresis		30		°C
SPREAD SPECTRUM FREQUENCY						
f_m (1)	Modulation frequency			10		kHz
f_{spread}	Internal spread oscillator frequency			±8%		

(1) Not production tested, specified by design.

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5.6 Typical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12V, unless otherwise noted.

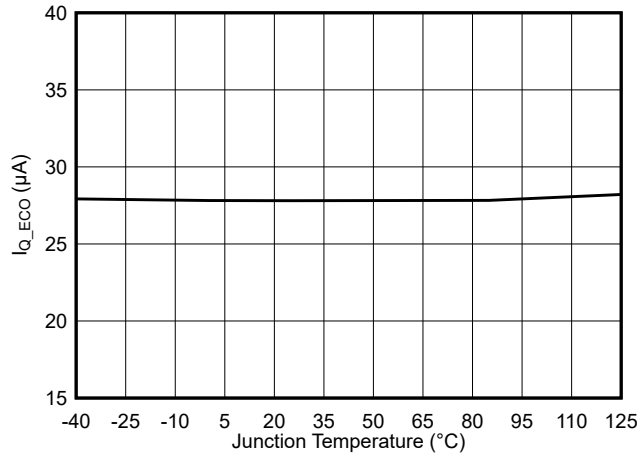

Figure 5-1. TPSM843321 Quiescent Current (PFM) vs Junction Temperature

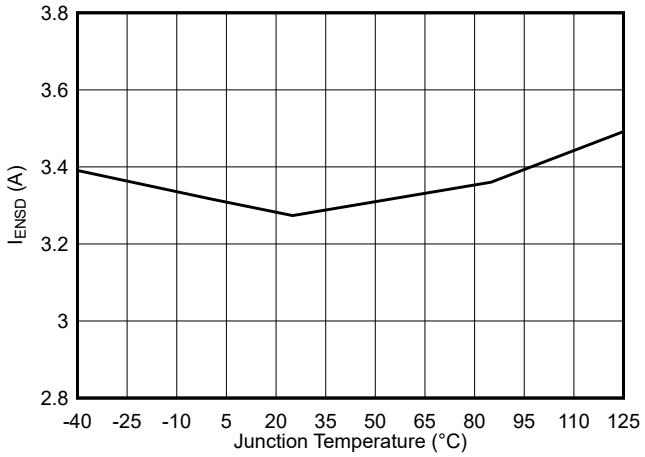

Figure 5-2. TPSM843321 Shutdown Current vs Junction Temperature

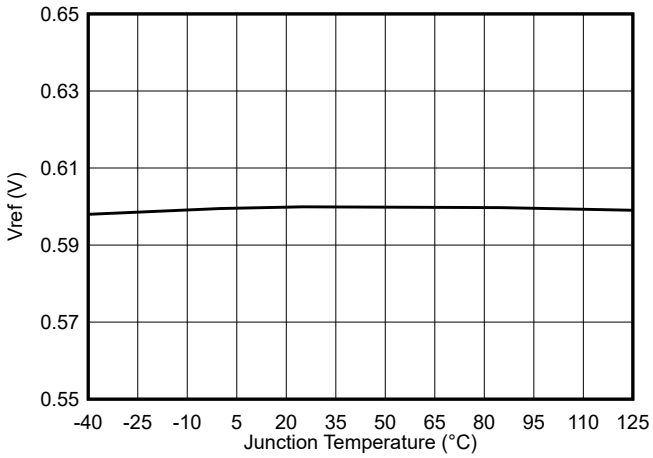

Figure 5-3. Feedback Voltage vs Junction Temperature

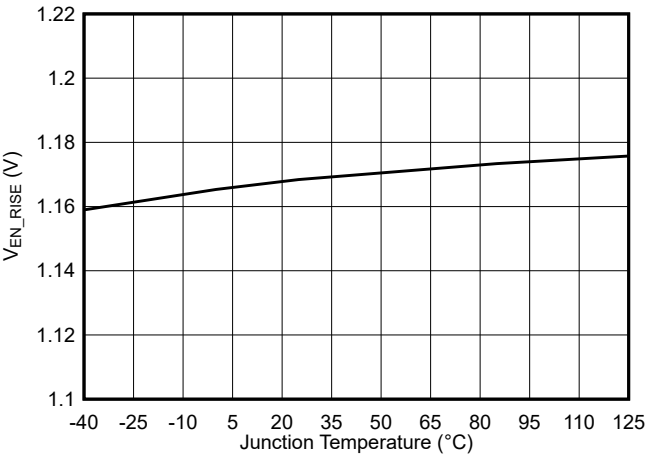

Figure 5-4. Enable Threshold vs Junction Temperature

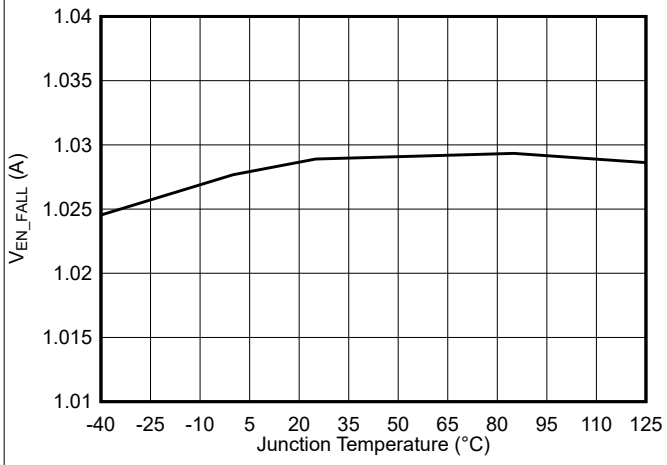

Figure 5-5. Disable Threshold vs Junction Temperature

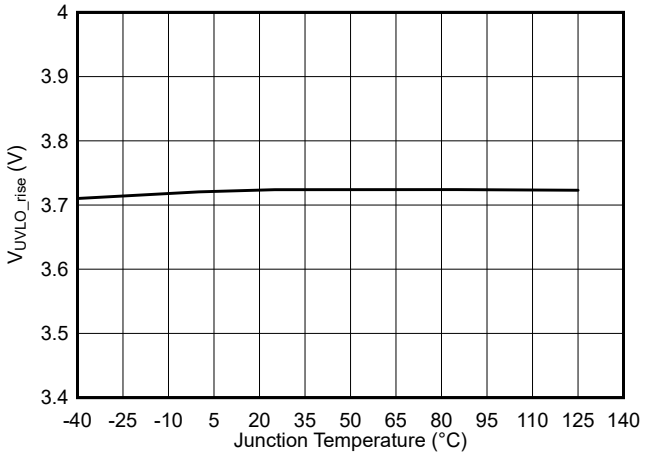

Figure 5-6. V_{IN} UVLO Rising Threshold vs Junction Temperature

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5.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12V, unless otherwise noted.

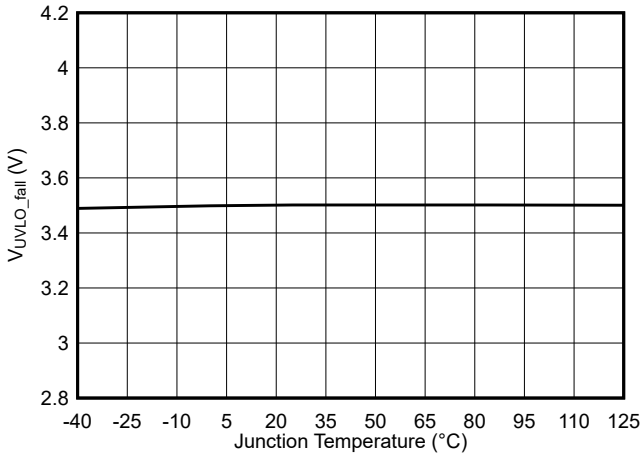

Figure 5-7. V_{IN} UVLO Falling Threshold vs Junction Temperature

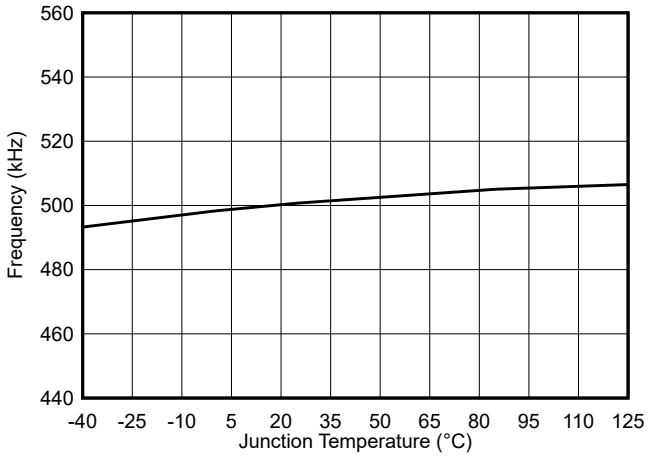

Figure 5-8. Switching Frequency (RT Floating) vs Junction Temperature

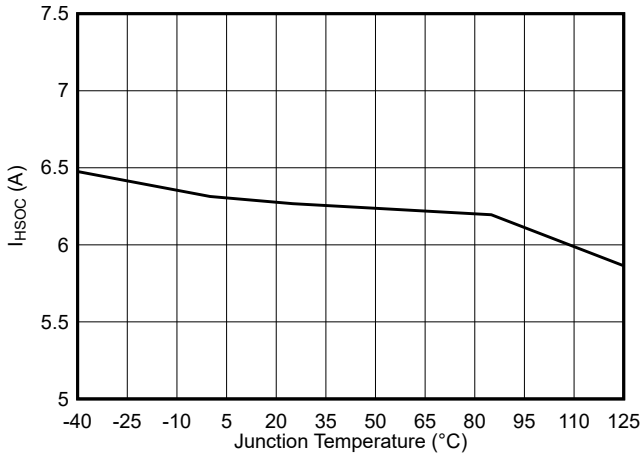

Figure 5-9. TPSM843321 High-Side Current Limit vs Junction Temperature

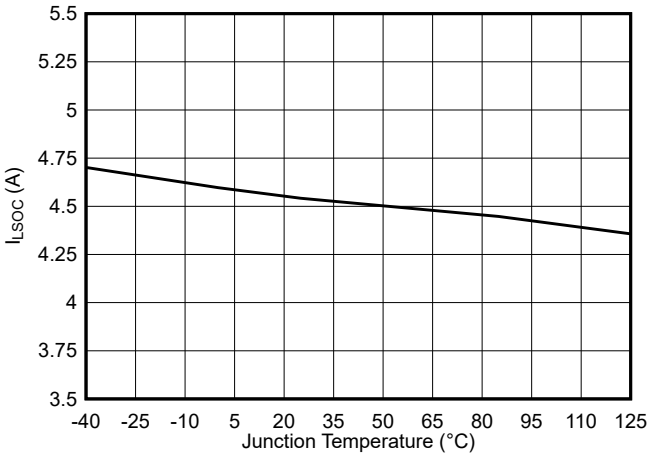

Figure 5-10. TPSM843321 Low-Side Current Limit vs Junction Temperature

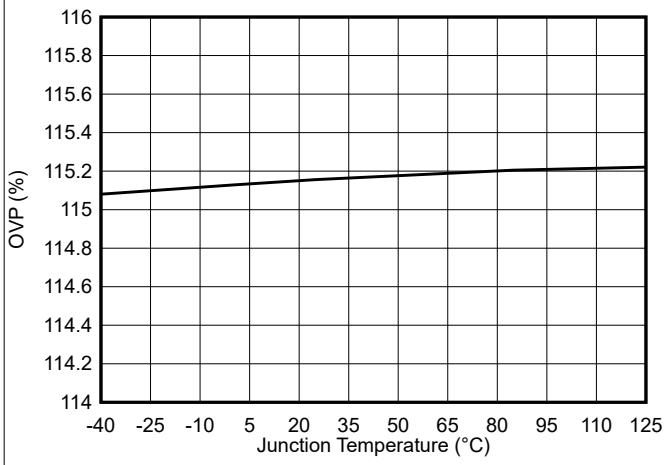

Figure 5-11. OVP Threshold vs Junction Temperature

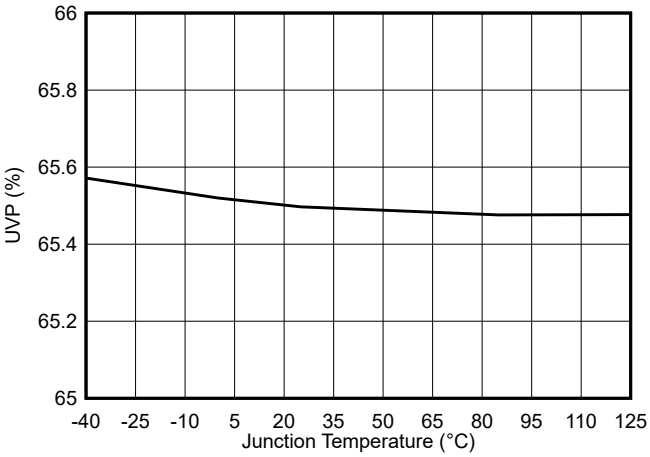

Figure 5-12. UVP Threshold vs Junction Temperature

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5.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12V, unless otherwise noted.

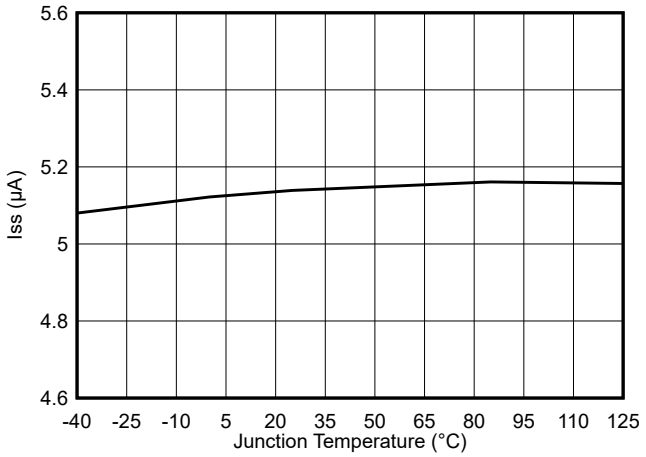

Figure 5-13. Soft-Start Charge Current vs Junction Temperature

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6 Detailed Description

6.1 Overview

The TPSM843321 is a high-efficiency, high-voltage input, and easy-to-use, synchronous buck power module with high design flexibility. With the wide operating input voltage range of 3.8V to 18V, the TPSM843321 is designed for systems powered from 5V, 12V power-bus rails. The device supports up to 3A continuous output current and 98% maximum duty cycle.

TPSM843321 uses peak current mode control with internal compensation for fast transient response and good line and load regulation. With the internal adaptive loop adjustment, the device eliminates the need for external compensation over a wide output voltage range and switching frequency. The integrated boostcap and the related circuit helps achieve single layer PCB and further reduce the external component count.

With different configuration of MODE pin, the device has option for pulse frequency modulation (PFM), forced continuous current modulation (FCCM) at light load condition and adjustable soft-start time / power-good indicator. When working at PFM mode, the device can attain high efficiency at light load. The FCCM mode helps TPSM843321 have low output ripple in all load conditions. A small value capacitor or resistor divider is connected to the SS/PG pin for soft-start time setting or voltage tracking when the device is set to have SS function. When PG function is selected, the device can indicate power good through the SS/PG pin.

The EN pin has an internal pullup current that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current.

The switching frequency can be set by the configuration of the RT/SYNC pin in the range of 200kHz to 2.2MHz, which allows for efficiency and design size optimization when selecting the output filter components. The frequency spread spectrum feature helps the device lower down EMI noise.

TPSM843321 has the on-time extension function with a maximum on time of 8µs (typical). During low dropout operation, the high-side MOSFET can turn on up to 8µs, then the high-side MOSFET turns off and the low-side MOSFET turns on with a minimum off time of 114ns (typical). The devices support the maximum 98% duty cycle.

Cycle-by-cycle current limiting on the high-side MOSFET protects the device in overload situations and is enhanced by a low-side sourcing current limit, which prevents current runaway. The TPSM843321 provides output undervoltage protection (UVP) when the regulated output voltage is lower than 65% of the nominal voltage due to overcurrent being triggered, approximately 256µs (typical) deglitch time later, both the high-side and low-side MOSFET turn off, the device steps into hiccup mode.

The devices minimize excessive output overvoltage transient by taking advantage of the overvoltage comparator. When the regulated output voltage is greater than 115% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and keep off until the output voltage is lower than 104%.

Thermal shutdown disables the devices when the die temperature, T_J, exceeds 165°C and enables the devices again after T_J decreases below the hysteresis amount of 30°C.

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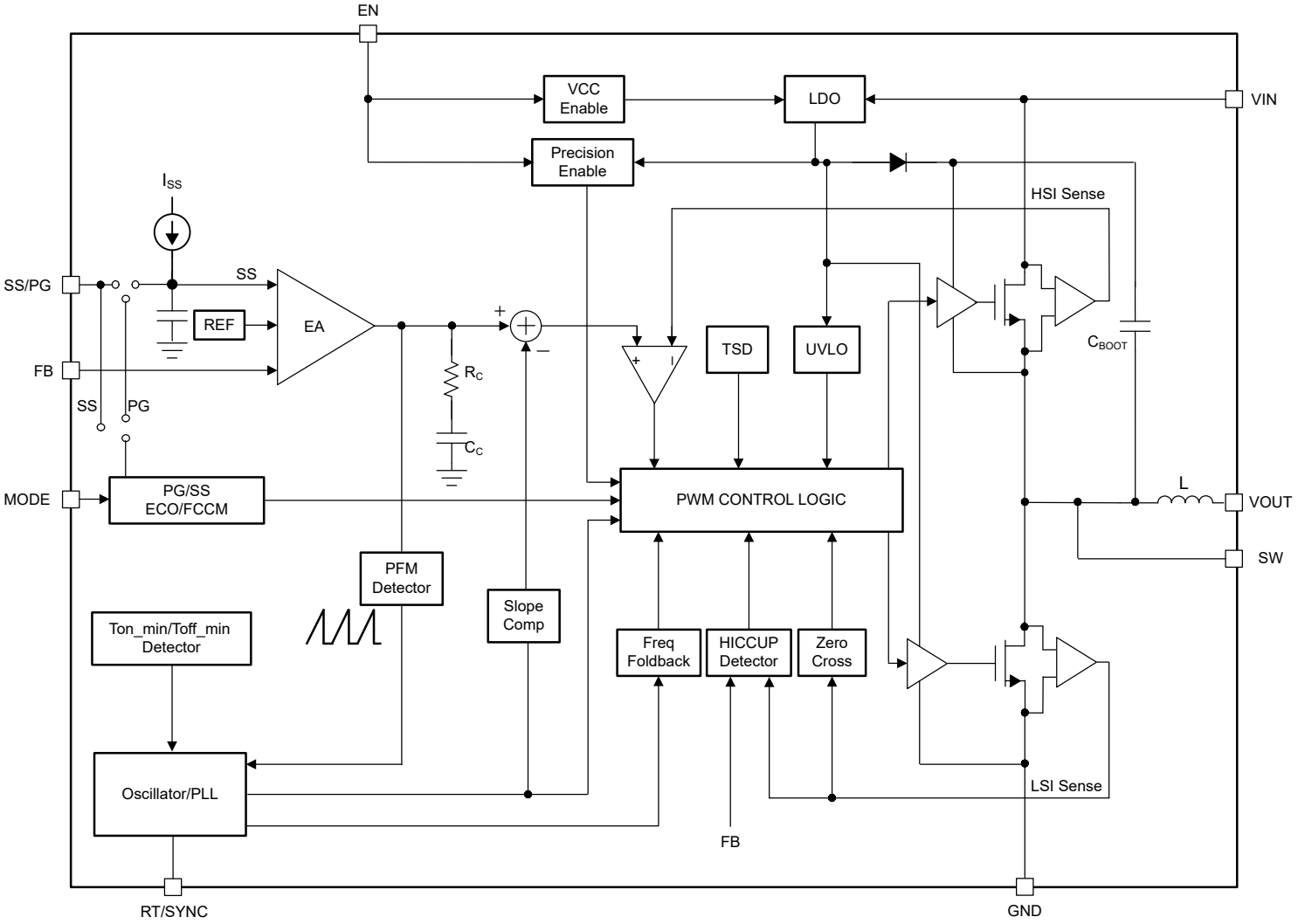
6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Fixed Frequency Peak Current Mode

The following operation description of the TPSM843321 refers to the functional block diagram and to the waveforms in Figure 6-1. The TPSM843321 is a synchronous buck converter with integrated high-side (HS) and low-side (LS) MOSFETs (synchronous rectifier). The TPSM843321 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch on time, the SW pin voltage swings up to approximately VIN, and the inductor current, iL, increases with linear slope (VIN – VOUT) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot–through dead time. Inductor current discharges through the low-side switch with a slope of –VOUT / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / t_{SW}, where t_{ON} is the high-side switch on time and t_{SW} is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = VOUT / VIN.

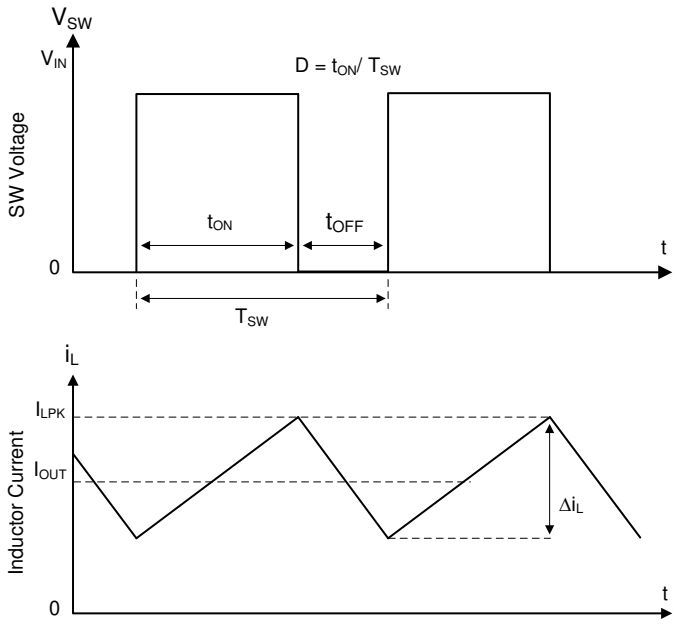

Figure 6-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The TPSM843321 employs the fixed-frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the HS switch and compared to the peak current threshold to control the on time of the HS switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes design easy, and provides stable operation with almost any combination of output capacitors.

6.3.2 Mode Selection

With different configuration of the MODE pin, the device is featured with selectable PFM/FCCM at light load, adjustable soft-start time function / power good indicator function for SS/PG pin and user-selectable spread spectrum feature for EMI enhancement. Table shows different MODE pin configurations, TI recommends using 1% tolerance resistors with a low temperature coefficient for MODE selection.

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Table 6-1. MODE Pin Configuration Table

Recommended Mode Resistor, kΩ	Operation in Light Load	Function of SS/PG Pin	Frequency Spread Spectrum Fss
< 4kΩ, short	PFM	SS	Yes
18kΩ	PFM	PG	Yes
180kΩ	FCCM	SS	Yes
330kΩ	FCCM	PG	Yes
680kΩ	FCCM	SS	No
> 1.3MΩ, floating	FCCM	PG	No

6.3.3 Voltage Reference

The internal reference voltage, V_{REF}, is designed at 0.6V (typical). The negative feedback system of converter produces a precise ±1% feedback voltage, V_{FB}, over full temperature by scaling the output of a temperature-stable internal band-gap circuit.

6.3.4 Output Voltage Setting

A precision 0.6V reference voltage, V_{REF}, is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from the output voltage to the FB pin. TI recommends using 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor, R_{FBB}, for the desired divider current and use Equation 1 to calculate the top-side resistor, R_{FBT}. Lower R_{FBB} increases the divider current and reduces efficiency at very light load. Larger R_{FBB} makes the FB voltage more susceptible to noise, so larger R_{FBB} values require a more carefully designed feedback path on the PCB. TI recommends setting R_{FBB} = 10kΩ and R_{FBT} in the range of 10kΩ to 300kΩ for most applications.

The tolerance and temperature variation of the resistor dividers affect the output voltage regulation.

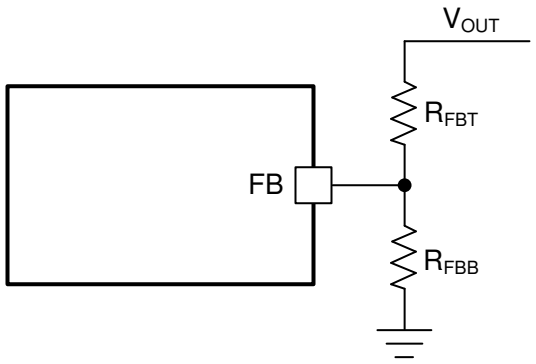

Figure 6-2. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (1)$$

where

- V_{REF} is the 0.6V (the internal reference voltage).
- R_{FBB} is 10kΩ (recommended).

6.3.5 Switching Frequency Selection, Synchronization

TPSM843321 can work under RT mode and SYNC mode by different configuration of the RT/SYNC pin. In RT mode, the switching frequency of TPSM843321 can be set with RT selection programming. Table 6-2 shows the RT selection programming. When RT is floating or connected to GND, the condition of this input is detected when the device is first enabled. After the converter is running, the switching frequency selection is fixed and cannot be changed until the next power-on cycle or EN toggle. When RT is connected with resistor, the switching frequency can be set between 200kHz and 2200kHz using the following equation.

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$$R_T = \frac{44500}{f_{SW}} - 2 \quad (2)$$

where

- RT is the value of RT timing resistor in kΩ.
- f_{SW} is the switching frequency in kHz.

Table 6-2. RT/SYNC Pin Resistor Settings

RT / SYNC Pin	Resistance	Switching Frequency
Floating	85kΩ	500kHz
GND	40kΩ	1000kHz
Resistor	18kΩ to 220kΩ	200kHz to 2200kHz

There are four cases where the switching frequency does not conform to the condition set by the RT/SYNC pin:

- Light load operation (PFM mode)
- Low dropout operation
- Minimum on-time operation
- Current limit tripped

Under all of these cases, the switching frequency folds back, meaning the switching frequency is less than that programmed by the RT/SYNC pin. During these conditions, the output voltage remains in regulation, except for current limit operation.

An internal Phase Locked Loop (PLL) has been implemented to allow synchronization from 200kHz to 2200kHz, and to easily switch from RT mode to SYNC mode. To implement the synchronization feature, connect a square wave clock signal to the RT/SYNC pin with a on time >= 100ns. The clock signal amplitude must transition lower than 0.9V and higher than 1.7V.

In applications where both RT mode and SYNC mode are needed, an RC circuit as shown in Figure 6-3 can be used to interface the RT/SYNC pin but the capacitive load slows down the transition back to RT mode. The RT/SYNC pin must not be left connect to GND / floating and 100pF capacitor is recommended. When using the series RC circuit, verify the amplitude of the signal at the RT/SYNC pin must transition lower than 0.9V and higher than 1.7V.

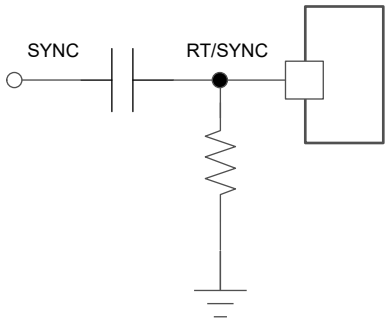

Figure 6-3. SYNC Mode Configuration

Note

- If SYNC is active before start-up, TPSM843321 works in SYNC clock.
- If SYNC not active before start-up, TPSM843321 works at default clock (based on RT resistor). When SYNC clock active, TPSM843321 works in SYNC mode.
  - If SYNC clock is out of range (200kHz to approximately 2.2MHz), TPSM843321 works at the end frequency (200kHz, 2.2MHz).
  - SYNC clock is not locked during operation.

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The switching frequency must be selected based on the output voltage setting of the device. See Table 6-3 for the allowable output voltage range for a given switching frequency with common input voltages

Table 6-3. Switching Frequency vs Output Voltage

F_{SW} (kHz)	V_{IN} = 5V		V_{IN} = 12V	
	V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
	MIN	MAX	MIN	MAX
200	0.6	4.5	0.6	1.2
400	0.6	4	0.6	2
600	1	4	0.9	3.3
800	1.5	3.5	1.2	9
1000	2	3	1.8	9
1200	N/A	N/A	2	9
1400	N/A	N/A	2.5	9
1600	N/A	N/A	3	9
1800	N/A	N/A	3.3	9
2000	N/A	N/A	4	9
2200	N/A	N/A	4.5	9

6.3.6 Phase Shift

When the TPSM843321 works in FCCM mode with SYNC to external clock, the phase shift function can be activated by adding a capacitor connect to the MODE pin, as is shown in Figure 6-4. When the phase shift function is disabled, let the capacitor float. The phase shift function is designed to reduce the input ripple and improve EMI performance for multi-rails, where step-down converters share the same input. Figure 6-5 shows how phase shift reduces input ripple with three buck converters sharing the same input. Calculate the capacitor value using Equation 3, where C_{MODE} is the MODE capacitor, θ is the degree of phase shift. Table 6-4 shows the typical capacitor value for the phase shift configuration.

$$C_{MODE} = \frac{\theta - 28°}{1.3585} \quad (3)$$

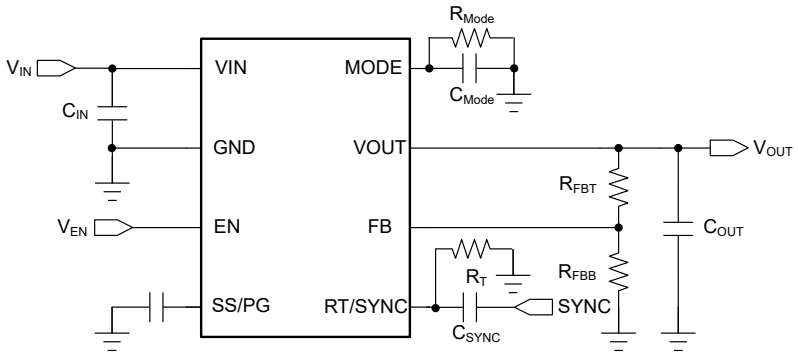

Figure 6-4. Phase Shift Operation Schematic

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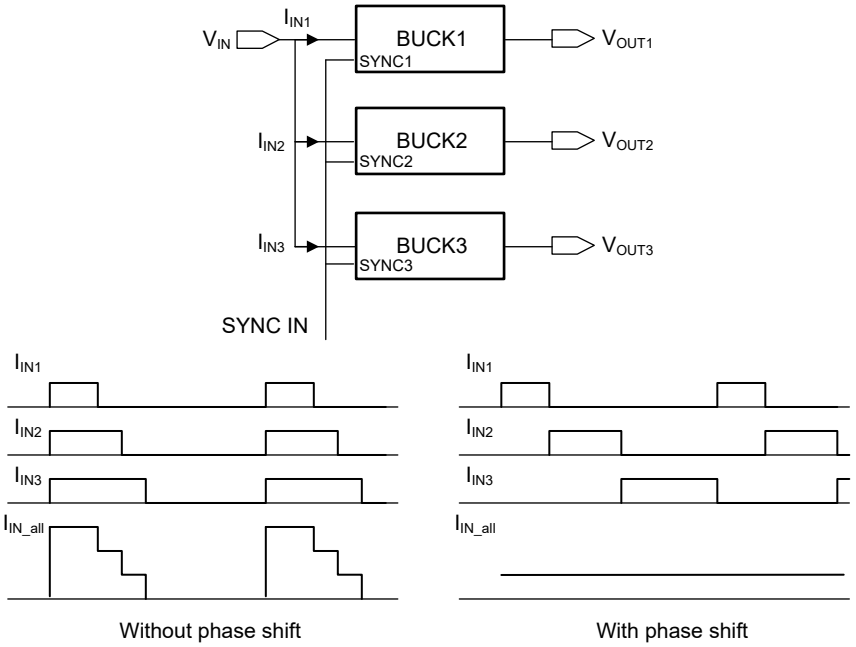

Figure 6-5. Phase Shift Operation Application

Table 6-4. Phase Shift Configuration

Recommended Mode Capacitor, pF	Phase Shift, Degree
47pF	90°
68pF	120°
120pF	180°
180pF	270°

6.3.7 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage exceeds the enable threshold voltage, V_{EN_RISE}, the TPSM843321 begins operation. If the EN pin voltage is pulled below the disable threshold voltage, V_{EN_FALL}, the converter stops switching and enters shutdown mode.

The EN pin has an internal pullup current source, which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use an open-drain or open-collector or GPIO output logic to interface with the pin.

The TPSM843321 implements internal undervoltage lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN_UVLO} threshold. The internal V_{IN_UVLO} threshold has a hysteresis of typical 200mV. If an application requires a higher UVLO threshold on the VIN pin, the EN pin can be configured as shown in Figure 6-6. When using the external UVLO function, TI recommends setting the hysteresis at a value greater than 500mV.

The EN pin has a small pullup current, I_p, which sets the default state of the EN pin to enable when no external components are connected. The pullup hysteresis current, I_h, is used to control the hysteresis voltage for the UVLO function when the EN pin voltage crosses the enable threshold. Use Equation 4 and Equation 5 to calculate the values of R1 and R2 for a specified UVLO threshold. After R1 and R2 are settled down, V_{EN} can be calculated by Equation 6, which must be lower than 5.5V with the maximum V_{IN}.

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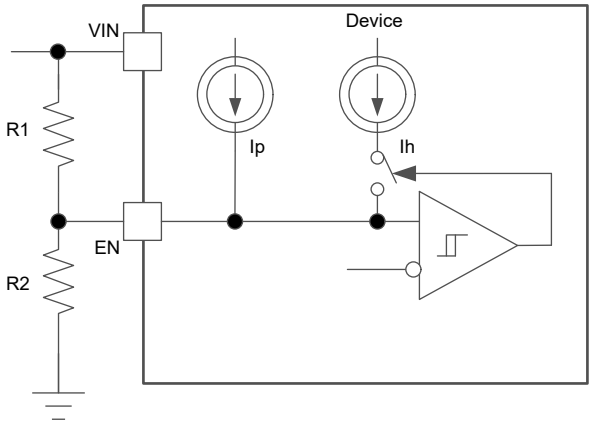

Figure 6-6. Adjustable V_{IN} Undervoltage Lockout

$$R_1 = \frac{V_{START} \times \frac{V_{EN_FALL}}{V_{EN_RISE}} - V_{STOP}}{I_p \times \left(1 - \frac{V_{EN_FALL}}{V_{EN_RISE}}\right) + I_h} \quad (4)$$

$$R_2 = \frac{R_1 \times V_{EN_FALL}}{V_{STOP} - V_{EN_FALL} + R_1 \times \left(I_p + I_h\right)} \quad (5)$$

$$V_{EN} = \frac{R_2 \times V_{IN} + R_1 \times R_2 \times \left(I_p + I_h\right)}{R_1 + R_2} \quad (6)$$

where

- I_p is 0.7µA.
- I_h is 1.76µA.
- V_{EN_FALL} is 1V.
- V_{EN_RISE} is 1.15V.
- V_{START} is the input voltage enabling the device.
- V_{STOP} is the input voltage disabling the device.

6.3.8 External Soft Start and Prebiased Soft Start

When the TPSM843321 is configured to the SS function by the MODE pin, the SS/PG pin of TPSM843321 is used to minimize inrush current when driving capacitive load. The devices use the lower voltage of the internal voltage reference, V_{REF}, or the SS/PG pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS/PG pin to ground implements a soft-start time. The device has an internal pullup current source that charges the external soft-start capacitor. Use the following equation to calculate the soft-start time (t_{SS}, 0% to 100%) and soft-start capacitor (C_{SS}).

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (7)$$

where

- V_{REF} is 0.6V (the internal reference voltage).
- I_{SS} is 5.5µA (typical), the internal pullup current.

If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage, V_{FB}. This scheme makes sure that the converters ramp up smoothly into regulation point. A resistor divider connected to the SS/PG pin can implement voltage tracking of the other power rail.

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6.3.9 Power Good

When the TPSM843321 is configured to the PG function, the SS/PG pin is used to indicate whether the output voltage has reached the appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage below 5.5V. TI recommends a pullup resistor of 10kΩ – 100kΩ. The device can sink approximately 4mA of current and maintain the specified logic low level. After the FB pin voltage is between 90% and 107% of the internal reference voltage (V_{REF}) and after a deglitch time of 70µs, the PG turns to high impedance status. The PG pin is pulled low after a deglitch time of 13µs when FB pin voltage is lower than 85% of the internal reference voltage or greater than 115% of the internal reference voltage, or in events of thermal shutdown, EN shutdown, or UVLO conditions. VIN must remain present for the PG pin to stay low.

Table 6-5. PG Status

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN = High)	V_{FB} does not trigger V_{PGTH}	√	
	V_{FB} triggers V_{PGTH}		√
Shutdown (EN = Low)			√
UVLO	2.5V < V_{IN} < V_{UVLO}		√
Thermal shutdown	T_J > T_{SD}		√
Power supply removal	V_{IN} < 2.5V	√	

6.3.10 Minimum On Time, Minimum Off Time, and Frequency Foldback

Minimum on time (t_{ON_MIN}) is the smallest duration of time that the high-side switch can be on. t_{ON_MIN} is typically 70ns in the TPSM843321. Minimum off time (t_{OFF_MIN}) is the smallest duration that the high-side switch can be off. t_{OFF_MIN} is typically 114ns. In CCM operation, t_{ON_MIN}, and t_{OFF_MIN}, limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = t_{ON_MIN} \times f_{SW} \quad (8)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - t_{ON_MIN} \times f_{SW} \quad (9)$$

Given a required output voltage, the maximum V_{IN} without frequency foldback is:

$$V_{IN_MAX} = \frac{V_{OUT}}{t_{ON_MIN} \times f_{SW}} \quad (10)$$

The minimum V_{IN} without frequency foldback is:

$$V_{IN_MIN} = \frac{V_{OUT}}{1 - t_{ON_MIN} \times f_{SW}} \quad (11)$$

In TPSM843321, a frequency foldback scheme is employed after t_{ON_MIN} or t_{OFF_MIN} is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on time decreases while V_{IN} voltage increases. After the on time decreases to t_{ON_MIN}, the switching frequency starts to decrease while V_{IN} continues to go up, which lowers the duty cycle further to keep V_{OUT} in regulation according to Equation 8.

The frequency foldback scheme also works after larger duty cycle is needed under low V_{IN} condition. The frequency decreases after the device hits the t_{OFF_MIN}, which extends the maximum duty cycle according to

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Equation 9. A wide range of frequency foldback allows the TPSM843321 output voltage to stay in regulation with a much lower supply voltage V_{IN}, which allows a lower effective dropout. With frequency foldback, V_{IN_MAX} is raised, and V_{IN_MIN} is lowered by decreased f_{SW}.

6.3.11 Frequency Spread Spectrum

To reduce EMI, the TPSM843321 introduces frequency spread spectrum. The jittering span is typically Δfc = ±8% of the switching frequency with the modulation frequency of 10kHz. The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. Figure 6-7 shows the frequency spread spectrum modulation. Figure 6-8 shows the energy is spread out at the center frequency, f_c.

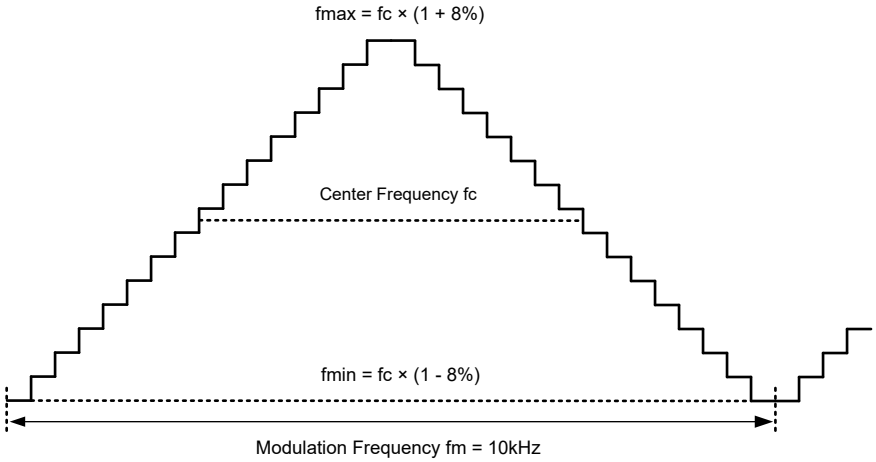

Figure 6-7. Frequency Spread Spectrum Diagram

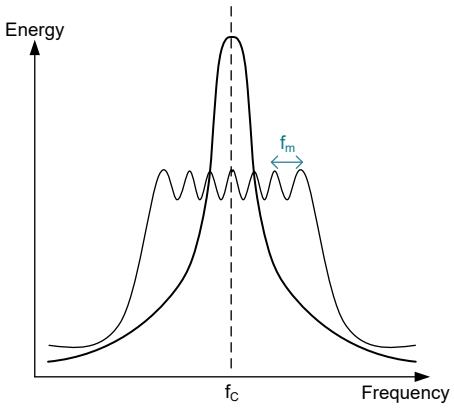

Figure 6-8. Energy vs Frequency

6.3.12 Overvoltage Protection

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold of 115%, the high-side MOSFET is turned off, which prevents current from flowing to the output and minimizes output overshoot. When the FB pin voltage drops lower than the OVP threshold minus hysteresis, the high-side MOSFET is allowed to turn on at the next clock cycle. This function is a non-latch operation.

6.3.13 Overcurrent and Undervoltage Protection

The TPSM843321 incorporates both peak and valley inductor current limits to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor

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current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Hiccup mode is also incorporated for sustained short circuits.

The high-side switch current is sensed when turned on after a set blanking time (t_{ON_MIN}), the peak current of high-side switch is limited by the peak current threshold, I_{HS_LIMIT}. The current going through low-side switch is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down.

As the device is overloaded, a point is reached where the valley of the inductor current cannot reach below I_{LS_LIMIT} before the next clock cycle, then the low-side switch is kept on until the inductor current ramps below the valley current threshold, I_{LS_LIMIT}, then the low-side switch is turned off and the high-side switch is turned on after a dead time. When this action occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, but the output voltage remains in regulation. As the overload is increased, both the inductor current ripple and peak current increase until the high-side current limit, I_{HS_LIMIT}, is reached. When this limit is tripped, the switch duty cycle is reduced and the output voltage falls out of regulation. This action represents the maximum output current from the converter and is given approximately by Equation 12. The output voltage and switching frequency continue to drop as the device moves deeper into overload while the output current remains at approximately I_{OMAX}. There is another situation, if the inductor ripple current is large, the high-side current limit can be tripped before the low-side limit is reached. In this case, Equation 13 gives the approximate maximum output current.

$$I_{OMAX} \approx \frac{I_{HS_LIMIT} + I_{LS_LIMIT}}{2} \tag{12}$$

$$I_{OMAX} \approx I_{HS_LIMIT} - \frac{(V_{IN} - V_{OUT})}{2 \times L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \tag{13}$$

Furthermore, if a severe overload or short circuit causes the FB voltage to fall below the V_{UVP} threshold, 65% of the V_{REF}, and triggering current limit, and the condition occurs for more than the hiccup on time (typical 256µs), the converter enters hiccup mode. In this mode, the device stops switching for hiccup off time, 10.5 × t_{SS}, and then goes to a normal restart with soft-start time. If the overload or short-circuit condition remains, the device runs in current limit and then shuts down again. This cycle repeats as long as the overload or short-circuit condition persists. This mode of operation reduces the temperature rise of the device during a sustained overload or short circuit condition on the output. After the output short is removed, the output voltage recovers normally to the regulated value.

For FCCM version, the inductor current is allowed to go negative. When this current exceed the LS negative current limit I_{LS_NEG}, the LS switch is turned off and HS switch is turned on immediately, which is used to protect the LS switch from excessive negative current.

6.3.14 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 165°C (typical), the device goes into thermal shutdown, both the high-side and low-side power FETs are turned off. When T_J decreases below the hysteresis amount of 30°C (typical), the converter resumes normal operation, beginning with a soft start.

6.4 Device Functional Modes

6.4.1 Modes Overview

The TPSM843321 moves between CCM, DCM, PFM, and FCCM mode as the load changes. Depending on the load current, the TPSM843321 is in one of the following modes:

- Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple
- Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation
- Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load
- Forced continuous conduction mode (FCCM) with fixed switching frequency even at light load

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6.4.2 Heavy Load Operation

The TPSM843321 operates in continuous conduction mode (CCM) when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. Regulating the output voltage provides excellent line and load regulation and minimum output voltage ripple, and the maximum continuous output current of 3A can be supplied by the TPSM843321.

6.4.3 Pulse Frequency Modulation

The TPSM843321 is designed to operate in pulse frequency modulation (PFM) mode at light load currents to boost light load efficiency when MODE pin is configured to PFM mode.

When the load current is lower than half of the peak-to-peak inductor current in CCM, the devices operate in discontinuous conduction mode (DCM). In DCM operation, the low-side switch is turned off when the inductor current drops to I_{LS_ZC} to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced CCM operation at light load.

At even lighter current load, pulse frequency modulation (PFM) mode is activated to maintain high-efficiency operation. When either the minimum high-side switch on time, t_{ON_MIN}, or the minimum peak inductor current I_{PEAK_MIN} is reached, the switching frequency decreases to maintain regulation. In PFM mode, the switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching actions. Because the integrated current comparator catches the peak inductor current only, the average load current entering PFM mode varies with the applications and external output LC filters.

In PFM mode, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long the feedback voltage takes to catch V_{REF}. The periodicity of these bursts is adjusted to regulate the output, while zero current crossing detection turns off the low-side MOSFET to maximize efficiency. This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads.

6.4.4 Forced Continuous Conduction Modulation

When the TPSM843321 is configured to operate in FCCM under light load conditions, the switching frequency is maintained at a constant level over the entire load range, which is an excellent choice for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. For some audio application, this mode can help avoid switching frequency drop into audible range that can introduce some "noise".

6.4.5 Dropout Operation

The dropout performance of any buck converter is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off time of the high-side MOSFET starts to approach the minimum value. Beyond this point, the switching frequency becomes erratic and the output voltage can fall out of regulation. To avoid this problem, the TPSM843321 automatically reduces the switching frequency (on-time extension function) to increase the effective duty cycle and maintain in regulation until the switching frequency reach to the lowest limit.

6.4.6 Minimum On-Time Operation

Every switching converter has a minimum controllable on time dictated by the inherent delays and blanking times associated with the control circuits, which imposes a minimum switch duty cycle and, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the TPSM843321 automatically reduces the switching frequency when the minimum on-time limit is reached. This way, the converter can regulate the lowest programmable output voltage at the maximum input voltage. Use Equation 14 to find an estimate for the approximate input voltage for a given output voltage before frequency foldback occurs. The values of t_{ON_MIN} and f_{SW} can be found in Section 5.5.

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$$V_{IN} \leq \frac{V_{OUT}}{t_{ON_MIN} \times f_{SW}} \quad (14)$$

As the input voltage is increased, the switch on time (duty-cycle) reduces to regulate the output voltage. When the on time reaches the minimum on time, t_{ON_MIN}, the switching frequency drops while the on time remains fixed.

6.4.7 Shutdown Mode

The EN pin provides electrical ON and OFF control for the device. When V_{EN} is below typical 1.15V, the TPSM843321 is in shutdown mode. The device also employs VIN UVLO protection. If V_{IN} voltage is below the respective UVLO level, the converter is turned off too.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPSM843321 device is typically used as a step-down module, which converts an input voltage from 5V to 18V to output voltage of 5V.

7.2 Typical Application

The application schematic of the following figure was developed to meet the requirements of the device. This circuit is available as the TPSM843321EVM evaluation module. The design procedure is given in this section.

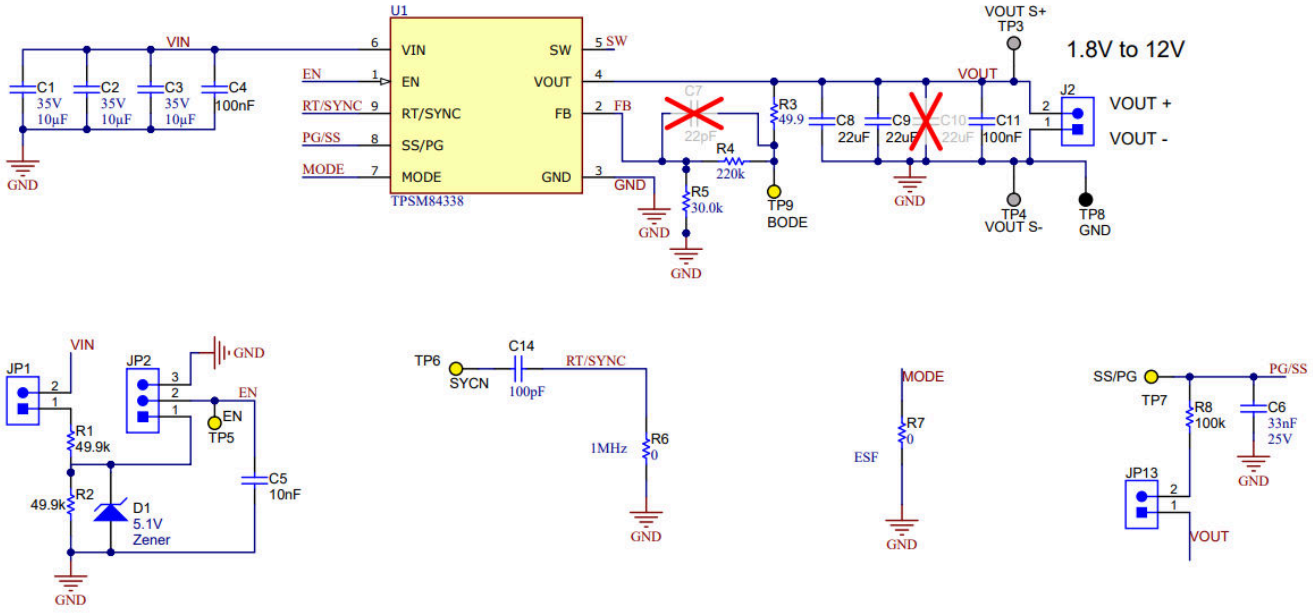

Figure 7-1. TPSM843321 5V Output, 3A Reference Design

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7.2.1 Design Requirements

The following table shows the design parameters for this application.

Table 7-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		5.5	12	18	V
V_{OUT}	Output voltage			5		V
I_{OUT}	Output current rating			3		A
$V_{IN(ripple)}$	Input ripple voltage			400		mV
$V_{OUT(ripple)}$	Output ripple voltage			30		mV
F_{SW}	Switching frequency	RT = floating		1000		kHz
t_{SS}	Soft-start time	C_{SS} = 33nF		3.6		mS
T_A	Ambient temperature			25		°C

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Create a custom design with the TPSM843321 using the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Referring to the application schematic of Figure 7-1, start with 30kΩ for R5 and use Equation 15 to calculate R4 = 220kΩ. To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the converter is more susceptible to noise and voltage errors from the FB input leakage current are noticeable.

$$R_4 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_5 \quad (15)$$

7.2.2.3 Choosing Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Higher switching frequency allows the use of smaller inductors and output capacitors, and hence, a more compact design. However, lower switching frequency implies reduced switching losses and usually results in higher system efficiency, so the 1000kHz switching frequency was chosen for this example, use 0Ω for R6.

Please note the switching frequency is also limited by the following as mentioned in Section 6.3.10:

- Minimum on time of the integrated power switch
- Input voltage
- Output voltage
- Frequency shift limitation

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7.2.2.4 Soft-Start Capacitor Selection

The large C_{SS} can reduce inrush current when driving large capacitive load. 33nF is chosen for C6, which sets the soft-start time, t_{SS}, to approximately 4ms.

7.2.2.5 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters, so using as little output capacitance as possible to keep cost and size down is desired. Choose the output capacitance, C_{OUT}, with care because the output capacitance directly affects the following specifications:

- Steady state output voltage ripple
- Loop stability
- Output voltage overshoot and undershoot during load current transient

The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT_ESR} = \Delta I_L \times ESR = K \times I_{OUT} \times ESR \tag{16}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT_C} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{17}$$

where

K is the ripple ratio of the inductor current (ΔI_L / I_{OUT_MAX}).

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

Output capacitance is usually limited by the load transient requirements rather than the output voltage ripple if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a large load step happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The control loop of the converter usually needs eight or more clock cycles to regulate the inductor current equal to the new load level. The output capacitance must be large enough to supply the current difference for about eight clock cycles to maintain the output voltage within the specified range. Equation 18 shows the minimum output capacitance needed for specified V_{OUT} overshoot and undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{\Delta I_{OUT}}{\Delta V_{OUT_SHOOT}} \left(\frac{6}{f_{SW}} - \frac{1}{SR_{\Delta I_{OUT}}} \right) \tag{18}$$

where

- D is V_{OUT} / V_{IN}, duty cycle of steady state.
- ΔV_{OUT_SHOOT} is the output voltage change.
- ΔI_{OUT} is the output current change.
- $SR_{\Delta IOUT}$ is the slew rate of output current change

For this design example, the target output ripple is 30mV. Presuppose ΔV_{OUT_ESR} = ΔV_{OUT_C} = 30mV and use K = 0.6. Equation 16 yields ESR no larger than 16.7mΩ and Equation 17 yields C_{OUT} no smaller than 7.5µF. For the overshoot and undershoot limitation of this design, ΔV_{OUT_SHOOT} < 5% × V_{OUT} = 250mV for an output current step of ΔI_{OUT} = 2.4A with $SR_{\Delta IOUT}$ = 0.8A/µs. C_{OUT} is calculated to be no smaller than 38µF by Equation 18. In summary, the most stringent criterion for the output capacitor is 22.8µF. By considering the ceramic capacitor has DC bias derating, the input capacitor can be achieved with a bank of 2 × 22µF, 35V, ceramic capacitor C3216X5R1V226M160AC in the 1206 case size.

More output capacitors can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases, an aluminum electrolytic capacitor can be placed in parallel

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with the ceramics to build up the required value of capacitance. When using a mixture of aluminum and ceramic capacitors, use the minimum recommended value of ceramics and add aluminum electrolytic capacitors as needed.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can reduce high frequency noise. Small case size ceramic capacitors in the range of 1nF to 100nF can help reduce spikes on the output caused by inductor and board parasitics.

7.2.2.6 Input Capacitor Selection

The TPSM843321 device requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10µF, and TI recommends an additional 0.1µF capacitor from the VIN pin to ground to provide high frequency filtering.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. TI recommends X5R and X7R ceramic dielectrics because X5R and X7R ceramic dielectrics have a high capacitance-to-volume ratio and are fairly stable over temperature. The capacitor must also be selected with the DC bias taken into account. The effective capacitance value decreases as the DC bias increases.

The capacitor voltage rating must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple. Use the following equation to calculate the input ripple current .

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN_MIN}} \times \frac{V_{IN_MIN} - V_{OUT}}{V_{IN_MIN}}} \quad (19)$$

Use the following equation to calculate the input voltage ripple.

$$\Delta V_{IN} = \frac{I_{OUT_MAX} \times 0.25}{f_{SW} \times C_{IN}} + \left(I_{OUT_MAX} \times R_{ESR_MAX}\right) \quad (20)$$

where

R_{ESR_MAX} is the maximum series resistance of the input capacitor, which is approximately 1mΩ of three capacitors in parallel.

7.2.2.7 Feedforward Capacitor C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop phase margin. This statement is especially true when values of R_{FBT} > 100kΩ are used. Large values of R_{FBT} in combination with the parasitic capacitance at the FB pin can create a small signal pole that interferes with the loop stability. A C_{FF} helps mitigate this effect. Use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor.

The *Optimizing Transient Response of Internally Compensated DC-DC Converters With Feedforward Capacitor* application note is helpful when experimenting with a feedforward capacitor.

For this example design, a 22pF capacitor C7 can be mounted to boost load transient performance.

7.2.2.8 Maximum Ambient Temperature

As with any power conversion device, the TPSM843321 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$, of the device
- PCB combination

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The maximum internal die temperature must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. Equation 21 shows the relationships between the important parameters. Seeing that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current is easy. The converter efficiency can be estimated by using the curves provided in this data sheet. Note that these curves include the power loss in the inductor. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics* application note, the value of $R_{\theta JA}$ given in the *Thermal Information* table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application. The data given for $R_{\theta JC(bott)}$ and Ψ_{JT} can be useful when determining thermal performance. See the *Semiconductor and IC Package Thermal Metrics* application note for more information and the resources given at the end of this section.

$$I_{OUT_MAX} = \frac{\left(T_J - T_A\right)}{R_{\theta JA}} \times \frac{\eta}{1-\eta} \times \frac{1}{V_{OUT}} \tag{21}$$

where

ŋ is efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature and flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

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7.2.3 Application Curves

V_{IN} = 12V, V_{OUT} = 5V, C_{OUT} = 44µF, T_A = 25°C (unless otherwise noted)

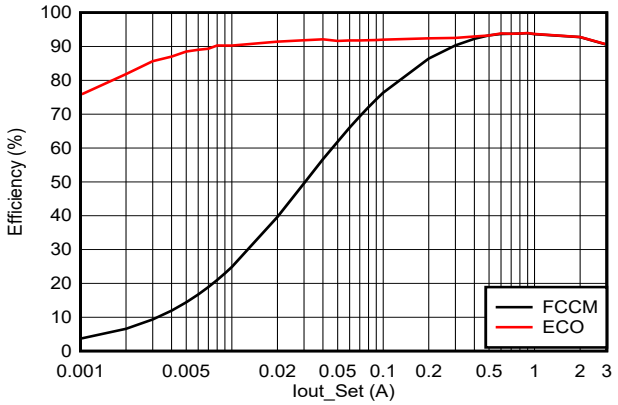

Figure 7-2. Efficiency (FCCM)

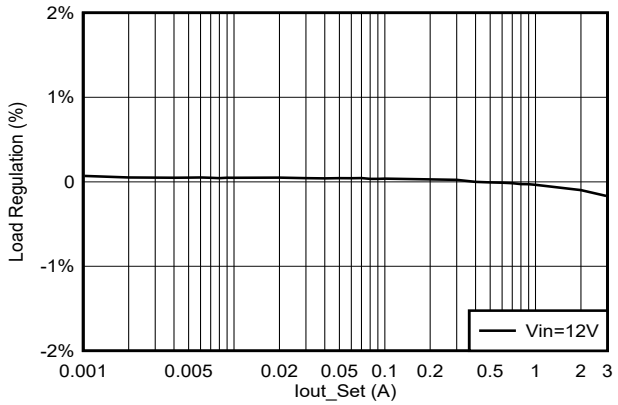

Figure 7-3. Load Regulation (ECO)

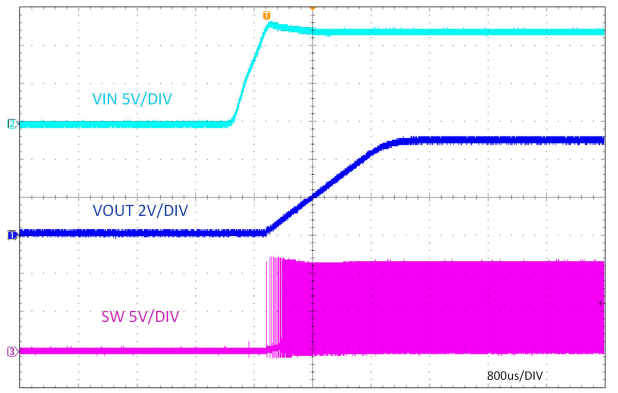

Figure 7-4. Start-Up Relative to V_{IN}, I_{OUT} = 3A

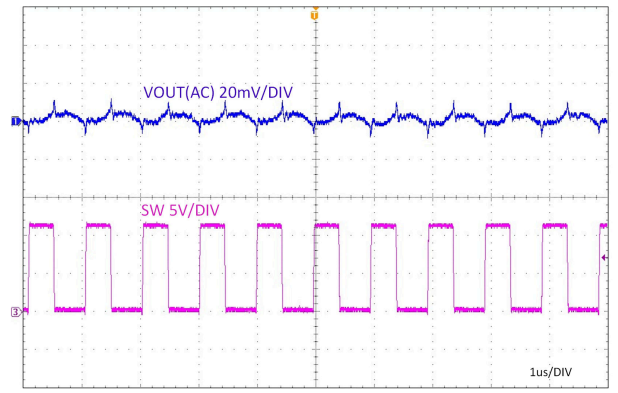

Figure 7-5. Steady State, I_{OUT} = 3A

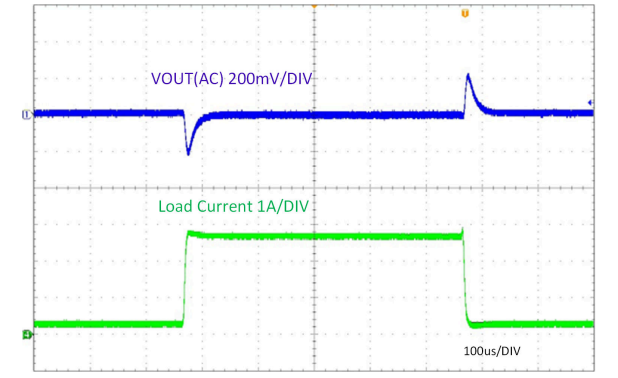

Figure 7-6. Load Transient Response, 0.3 to 2.7A, Slew Rate = 0.8A/µS

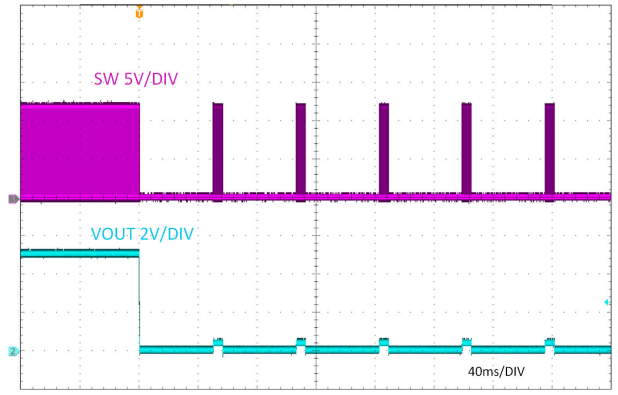

Figure 7-7. V_{OUT} Hard Short Protection

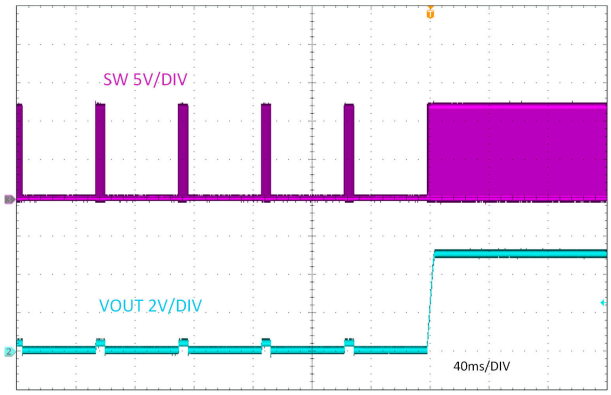

Figure 7-8. V_{OUT} Hard Short Recovery

7.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings.*
- Do not exceed the *Recommended Operating Conditions.*
- Do not exceed the *ESD Ratings.*
- Do not allow the SS pin floating.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Do not use the value of $R_{\theta JA}$ given in the *Thermal Information* table to design your application. See Section 7.2.2.8.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.
- Use a 100nF capacitor connected directly to the VIN and GND pins of the device. See Section 7.2.2.6 for details.

7.4 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.8V and 18V. This input supply must be well regulated and compatible with the limits found in the *Specifications* of this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded converter. The average input current can be estimated with Equation 22.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (22)$$

where

ŋ is efficiency.

If the converter is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the converter. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the converter. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the converter to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the converter and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help damp the input resonant circuit and reduce any overshoots. A value in the range of 20µF to 100µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

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TI recommends that the input supply must not be allowed to fall below the output voltage by more than 0.3V. Under such conditions, the output capacitors discharges through the body diode of the high-side power MOSFET. The resulting current can cause unpredictable behavior, and in extreme cases, possible device damage. If the application allows for this possibility, then use a Schottky diode from VIN to VOUT to provide a path around the converter for this current.

In some cases, a transient voltage suppressor (TVS) is used on the input of converters. One class of this device has a snap-back characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the converter, the output capacitors discharges through the device, as mentioned above.

Sometimes, for other system considerations, an input filter is used in front of the converter, which can lead to instability as well as some of the effects mentioned above, unless designed carefully. The *AN-2162 Simple Success with Conducted EMI from DC-DC Converters* application note provides helpful suggestions when designing an input filter for any switching converter.

7.5 Layout

7.5.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the excellent performance of the design. Bad PCB layout can disrupt the operation of a good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitors and power ground. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this action, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance.

TI recommends a 4-layer board with 2oz copper thickness of top and bottom layer, 1oz copper thickness of mid layer, and proper layout provides low current conduction impedance, proper shielding, and lower thermal resistance. Figure 7-9 and Figure 7-10 show the recommended layouts for the critical components of the TPSM843321.

- Place the input and output capacitors, and the IC on the same layer.
- Place the input and output capacitors as close as possible to the IC. The VIN and GND traces must be as wide as possible and provide sufficient vias on them to minimize trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
- Place a 0.1µF ceramic decoupling capacitor or capacitors as close as possible to VIN and GND pins, which is key to EMI reduction.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Place the feedback divider as close as possible to the FB pin. TI recommends a > 10-mil width trace for heat dissipation. Connect a separate V_{OUT} trace to the upper feedback resistor. Place the voltage feedback loop away from the high-voltage switching trace. The voltage feedback loop preferably has ground shield.
- Place the SS capacitor resistor close to the IC and routed with minimal lengths of trace. TI recommends a > 10-mil width trace for heat dissipation.

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7.5.2 Layout Example

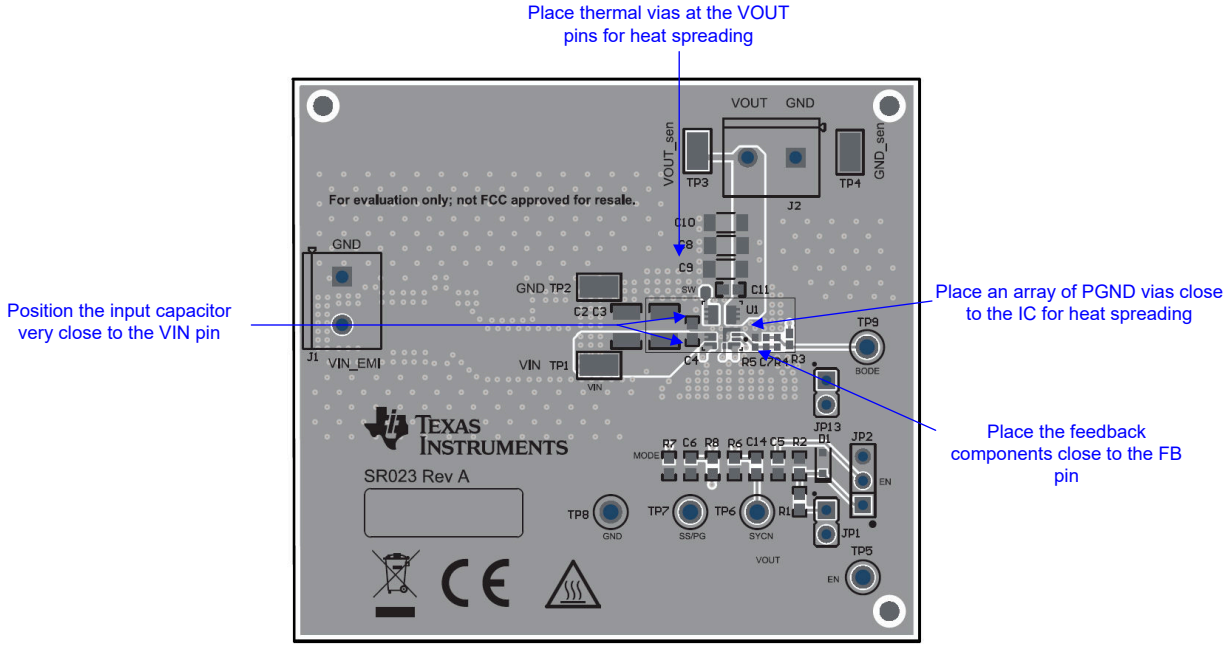

Figure 7-9. TPSM843321 Top Layout Example

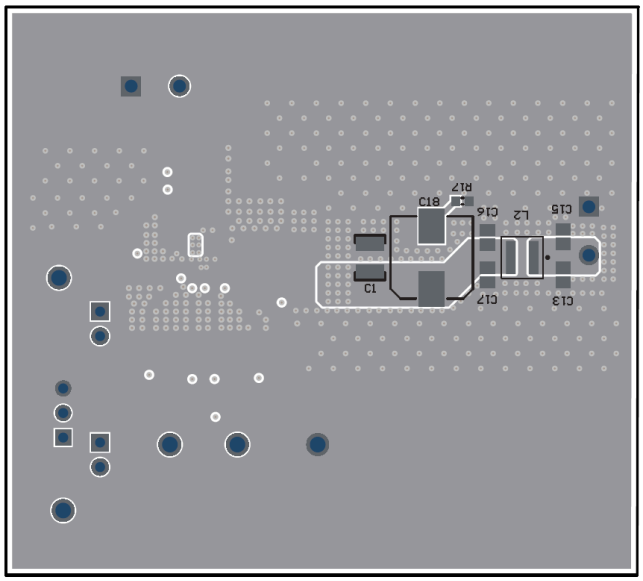

Figure 7-10. TPSM843321 Bottom Layout Example

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.1.2 Development Support

8.1.2.1 Custom Design With WEBENCH® Tools

Create a custom design with the TPSM843321 using the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

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In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *AN-2162 Simple Success with Conducted EMI from DCDC Converters* application note
- Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

DATE	REVISION	NOTES
March 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM843321RCJR	Active	Production	null (null) |	3000 | LARGE T&R	In-Work	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M843321
TPSM843321RCJR.A	Active	Production	QFN-FCMOD (RCJ) | 9	3000 | LARGE T&R	In-Work	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M843321

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

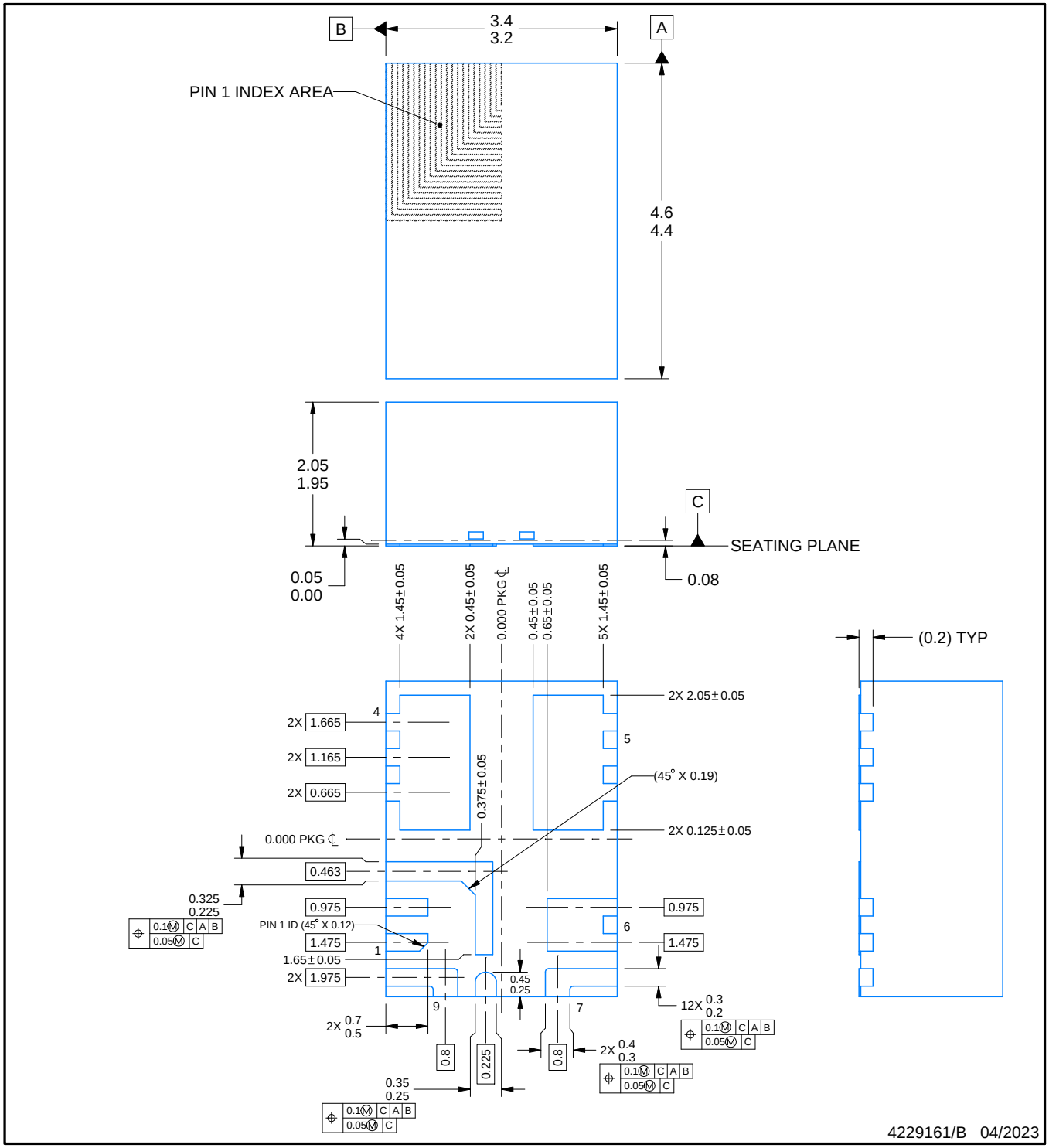
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RCJ0009A

QFN-FCMOD - 2.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

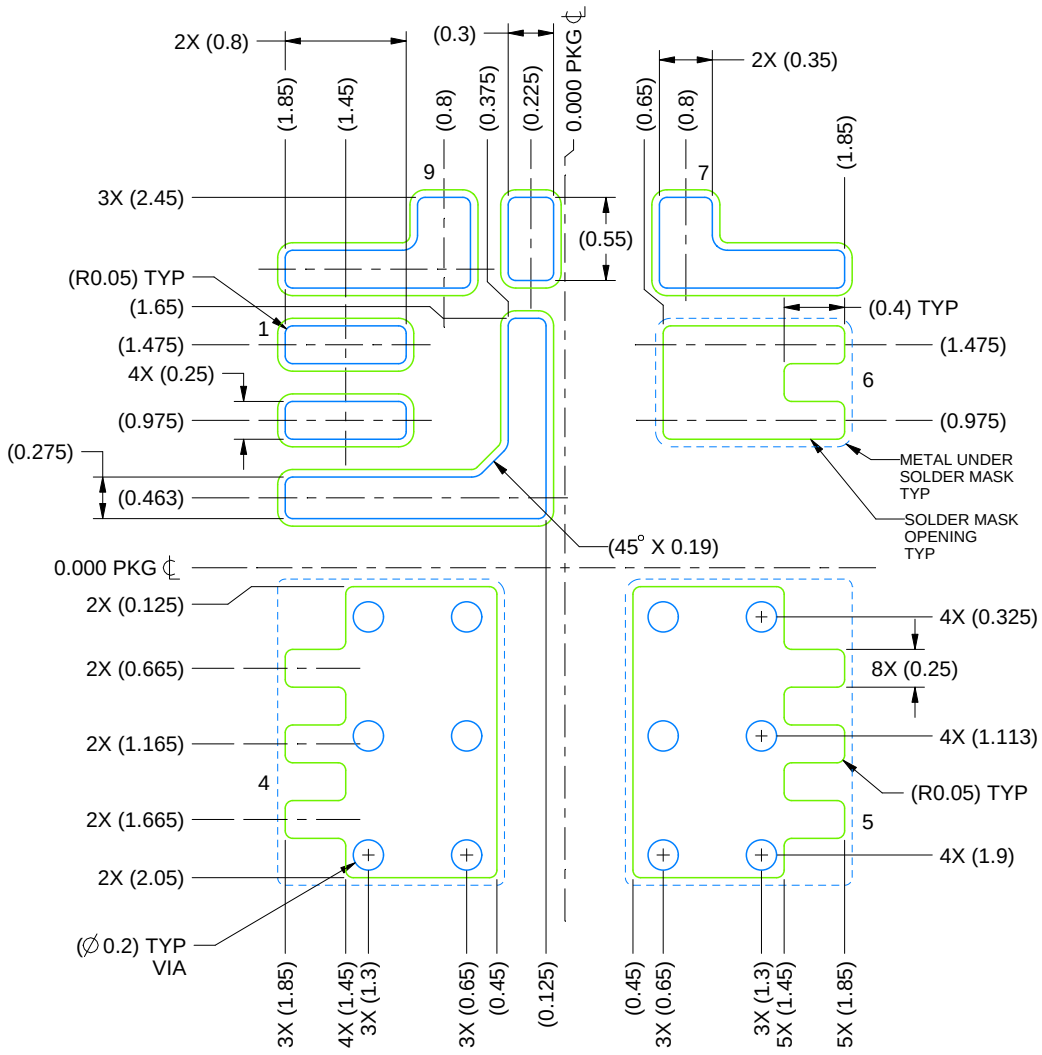
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

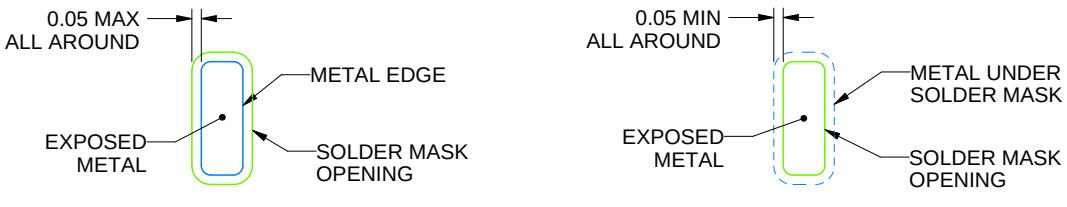
RCJ0009A

QFN-FCMOD - 2.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 20X



NON SOLDER MASK DEFINED PADS:1-3 & 7-9

SOLDER MASK DEFINED PADS: 4-6

SOLDER MASK DETAILS

4229161/B 04/2023

NOTES: (continued)

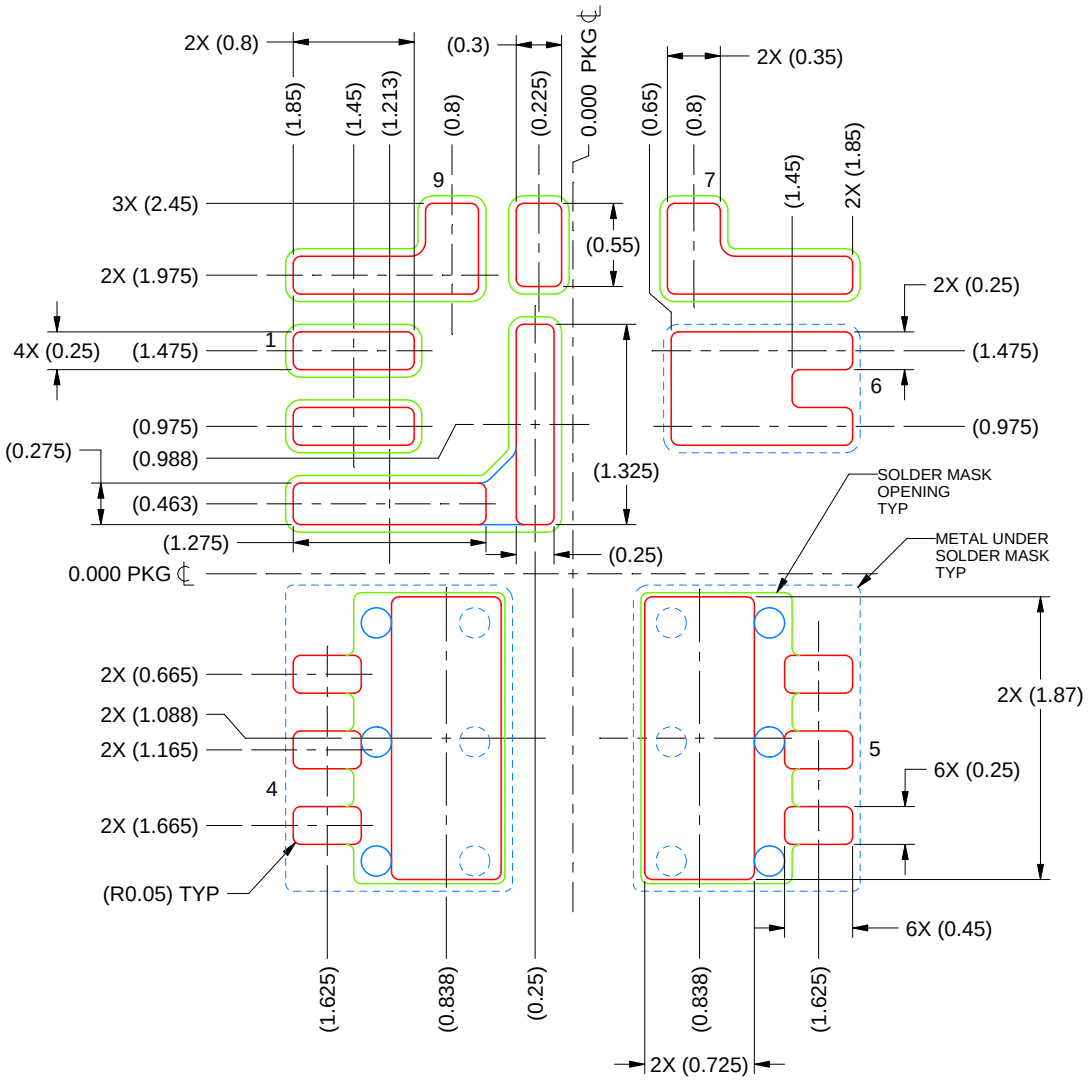
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RCJ0009A

QFN-FCMOD - 2.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 3: 91%
PADS 4 & 5: 76%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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