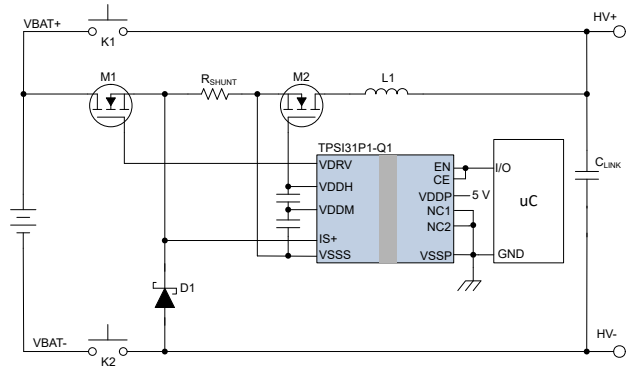
TPSI31P1-Q1 Automotive Active Pre-charge Controller With 17V Isolated Gate Driver and Bias Supply

1 Features

- Replaces large, high power pre-charge resistors using a switched converter architecture
- Improved thermal performance compared to passive pre-charge solutions
- Hysteretic current control for linear charging of downstream capacitance
- Drives external power transistors such as Si, SiC MOSFET, or IGBT
- Integrated isolated secondary supply for gate bias
- 17V gate drive, 1.5A and 2.5A peak source and sink current
- AEC Q-100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Safety-related certifications
  - Planned: 7070V_{PK} reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - Planned: 5kV_{RMS} isolation for 1 minute per UL 1577

2 Applications

- Battery management system



TPSI31P1-Q1 Simplified Application

3 Description

The TPSI31P1-Q1 is designed to be used in automotive pre-charge systems as an alternative to traditional passive pre-charge architectures that typically include costly electromechanical relays (EMR), along with bulky, high power resistors. The TPSI31P1-Q1, combined with external power switches, power inductor and diode, forms an active pre-charge solution. The inductor current is continuously monitored and controlled in a hysteretic mode of operation by the TPSI31P1-Q1 to linearly charge the large capacitance of the downstream system. The TPSI31P1-Q1 is an isolated switch driver that generates its own secondary bias supply from power received on its primary side, therefore no isolated secondary supply is required. With a gate drive voltage of 17V with 1.5A and 2.5A peak source and sink current, a large availability of power switches can be used including SiC FET and IGBT.

The TPSI31P1-Q1 integrates a communication back-channel that transfers status information from the secondary side to the primary side via open-drain output, PGOOD (Power Good) and indicates when the secondary power is valid.

The TPSI31P1-Q1 reinforced isolation is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than those found in optocouplers. Replacing the EMR and power resistor with a solid state solution can lead to reduced cost and form factor, while providing higher reliability.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPSI31P1-Q1 (3)	DVX (SSOP, 16)	5.85mm ×10.3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product preview.

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4 Pin Configuration and Functions

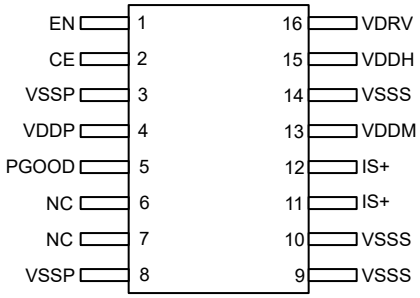

Figure 4-1. TPSI31P1-Q1 DVX Package, 16-Pin SSOP (Top View)

PIN		I/O	TYPE[1]	DESCRIPTION
NO.	NAME			
1	EN	I	—	Active high pre-charge enable. Internal 500kΩ pull-down to VSSP.
2	CE	I	—	Active high chip enable. When asserted low, device is disabled. Tie to VDDP or EN when not used. Internal 500kΩ pull-down to VSSP.
4	VDDP	—	P	Power supply for the primary side.
5	PGOOD	O	—	Power good indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
11, 12	IS+	I	—	Resistor shunt positive. When voltage across shunt resistor exceeds internal reference voltage (1.23V), VDRV is asserted low and remains low until voltage across shunt resistor falls below internal reference (160mV). Internal 3MΩ pull-down to VSSS.
13	VDDM	—	P	Generated mid-supply, nominal 5V.
15	VDDH	—	P	Generated high supply, nominal 17V.
16	VDRV	O	—	Active high driver output.
6,7	NC	NC	—	No connect. Leave floating or connect to VSSP.
3, 8	VSSP	—	GND	Ground supply for the primary side. All VSSP pins must be connected to the primary side ground.
9, 10, 14	VSSS	—	GND	Ground supply for the secondary side. All VSSS pins must be connected to the secondary side ground.

(1) P = power, GND = ground, NC = no connect

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER(1)		MIN	MAX	UNIT
Primary side supply(2)	VDDP, EN, CE, PGOOD	–0.3	6	V
Secondary side supply(3)	IS+	–3	6	V
Secondary side supply(3)	VDRV	–0.3	18	V
	VDDH	–0.3	18	V
	VDDM	–0.3	6	V
	VDDH-VDDM	–0.3	13	V
Junction temperature, T_J	Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute MaximumRatings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSSP.
(3) All voltage values are with respect to VSSS.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 8, 9, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDP	Primary side supply voltage(1)	4.5		5.5	V
EN	Enable pre-charge (1)	0		5.5	V
CE	Chip enable(1)	0		5.5	V
PGOOD	Power good indicator(4) (1)	0		5.5	V
C_{VDDP}	Decoupling capacitance on VDDP and VSSP(3)	1		20	µF
C_{DIV1} (2)	Decoupling capacitance across VDDH and VDDM(3)	0.003		15	µF
C_{DIV2} (2)	Decoupling capacitance across VDDM and VSSS(3)	0.1		40	µF
T_A	Ambient operating temperature	–40		125	°C
T_J	Operating junction temperature	–40		150	°C

(1) All voltage values are with respect to VSSP.
(2) C_{DIV1} and C_{DIV2} should be of same type and tolerance. C_{DIV2} capacitance value should be at least three times the capacitance value of C_{DIV1} i.e. $C_{DIV2} \geq 3 \times C_{DIV1}$.
(3) All capacitance values are absolute. Derating should be applied where necessary.
(4) Open-drain fail-safe output. When being used, an external pull-up resistor greater than 20kΩ to VDDP is recommended. When not being used, float pin or connect to VSSP.

5.4 Thermal Information

THERMAL METRIC(1)		DEVICE DVX (SSOP) 16 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	82.5	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	39.3	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	42.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation, VDDP.	T_A = 25°C, V_{VDDP} = 5.0V, f_{EN} = 1kHz square wave, C_{VDRV} = 1nF			250	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CREEPAGE AND TRACKING				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	≥ 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	≥ 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	

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PARAMETER		TEST CONDITIONS	VALUE	UNIT
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1697	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave)	1200	V_{RMS}
		DC voltage	1697	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60s (qualification test)	7070	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$; t = 1s (100% production test)	8484	V_{PK}
V_{IMP}	Maximum impulse voltage(2)	Tested in air; 1.2/50µs waveform per IEC 62638-1	9230	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Tested in oil (qualification test); 1.2/50µs waveform per IEC 62638-1	12000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2036V_{PK}$, t_m = 10s.	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2715V_{PK}$, t_m = 10s.	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3139V_{PK}$, t_m = 1s.	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1MHz	3	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S =150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000V_{RMS}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000V_{RMS}$, t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air to determine the intrinsic surge immunity of the package.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety-Related Certifications

VDE	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 Component Recognition Program
Reinforced insulation; Maximum transient isolation voltage, $7070V_{PK}$; Maximum repetitive peak isolation voltage, $1697V_{PK}$; Maximum surge isolation voltage, $12000V_{PK}$	Single protection, $5000V_{RMS}$
Certificate planned	Certificate planned

5.8 Safety Limiting Values

PARAMETER(1) (2)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 82.5°C/W, V_{VDDP} = 5.5V, T_J = 150°C, T_A = 25°C			275	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ =82.5°C/W, T_J = 150°C, T_A = 25°C			1.52	W
T_S	Maximum safety temperature				150	°C

(1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

(2) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

5.9 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. 50kΩ pull-up from PGOOD to VDDP.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
CMTI	Common-mode transient immunity, static.	$\|V_{CM}\|$ = 1000V, V_{EN} = 0V or V_{EN} = 5V.	100			V/ns
TSD	Temperature shutdown	V_{VDDP} = 5V		173		°C
TSDH	Temperature shutdown hysteresis	V_{VDDP} = 5V		32		°C
SUPPLY						
I_{VDDP_STBY}	VDDP current in standby	V_{VDDP} = 5V, EN = 0V, CE = 0V. Measure average current.		25	45	µA
I_{VDDP}	VDDP average current in steady state	V_{VDDP} = 5V, EN = CE = 5V. V_{VDDH} in steady state, measure I_{VDDP}.		37		mA
V_{VDDH}	VDDH output voltage	V_{VDDP} = 5V, EN = CE = 5V.	16	17	18	V
V_{VDDM}	Average VDDM voltage when not sourcing current.	V_{VDDP} = 5V, EN = CE = 5V.	4.8	5.0	5.2	V
SUPERVISORY						
$V_{VDDP\_UV\_R}$	VDDP under-voltage threshold rising	VDDP rising.	3.9	4.1	4.35	V
$V_{VDDP\_UV\_F}$	VDDP under-voltage threshold falling	VDDP falling	3.8	3.9	4.25	V
$V_{VDDP\_UV\_HYS}$	VDDP under-voltage threshold hysteresis			170		mV
$V_{VDDH\_UV\_R}$	VDDH under-voltage threshold rising	VDDH rising.	12.3	13	13.6	V
$V_{VDDH\_UV\_F}$	VDDH under-voltage threshold falling.	VDDH falling.	9.9	10.4	11	V
$V_{VDDH\_UV\_HYS}$	VDDH under-voltage threshold hysteresis.			2.5		V
$V_{VDDM\_UV\_R}$	VDDM under-voltage threshold rising	VDDM rising.	3.4	3.7	3.9	V
$V_{VDDM\_UV\_F}$	VDDM under-voltage threshold falling.	VDDM falling.	3.1	3.4	3.7	V

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over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. 50kΩ pull-up from PGOOD to VDDP.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDDM\_UV\_HYS}$	VDDM under-voltage threshold hysteresis.			0.3		V
DRIVER						
V_{VDRV_H}	VDRV output voltage driven high	V_{VDDP} = 5V, EN = 5V. V_{VDDH} in steady state.	16	17	18	V
V_{VDRV_L}	VDRV output voltage driven low	V_{VDDP} = 5V, EN = 0V, V_{VDDH} in steady state, VDRV sinking 10mA.			0.1	V
I_{VDRV_PEAK}	VDRV peak output current during rise	V_{VDDP} = 5V, EN = 0V → 5V, V_{VDDH} in steady state, measure peak current.		1.5		A
	VDRV peak output current during fall	V_{VDDP} = 5V, EN = 5V → 0V, V_{VDDH} in steady state, measure peak current.		2.5		A
V_{ACT_CLAMP}	Active clamp voltage when engaged.	V_{VDDP} = 0V. Sink I_{VDRV} = 300mA. Measure VDRV.		1.9	2.5	V
DIGITAL INPUT/OUTPUT						
$V_{IT\_+(EN)}$	Input threshold voltage rising on EN.	V_{VDDP} = 5V	2.3	2.5	2.7	V
$V_{IT\_-(EN)}$	Input threshold voltage falling on EN.	V_{VDDP} = 5V	1.7	1.9	2.0	V
$V_{IT\_HYS(EN)}$	Input threshold voltage hysteresis on EN.	V_{VDDP} = 5V		0.5		V
$V_{IT\_+(CE)}$	Input threshold voltage rising on CE.	V_{VDDP} = 5V	2.3	2.5	2.7	V
$V_{IT\_-(CE)}$	Input threshold voltage falling on CE.	V_{VDDP} = 5V	1.7	1.9	2.0	V
$V_{IT\_HYS(CE)}$	Input threshold voltage hysteresis on CE.	V_{VDDP} = 5V		0.5		V
V_{OL}	Low level output voltage. PGOOD	V_{VDDP} = 4.5V to 5.5V, I_{OL} = 2mA. Output enabled.			0.4	V
I_{OL}	Low level output current. PGOOD	V_{VDDP} = 4.5V to 5.5V, V_{OL} = 0.4V. Output enabled.	-2			mA
I_{LKG}	Leakage current. PGOOD	V_{VDDP} = 4.5V to 5.5V, Output disabled.			2	µA
$R_{EN\_PULLDOWN}$	Internal resistor pull-down on EN.	V_{VDDP} = 5V	400	500	640	kΩ
$R_{CE\_PULLDOWN}$	Internal resistor pull-down on CE.	V_{VDDP} = 5V	400	500	640	kΩ

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over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. 50kΩ pull-up from PGOOD to VDDP.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{REF+}	Peak current reference voltage.	T_A = 25°C		1.23		V
V_{REF-}	Valley current reference voltage.	T_A = 25°C		0.16		V
V_{REF_TOL}	Internal reference voltage tolerance.		-1.5		1.5	%
COMPARATORS						
$R_{CMP\_PULLDOWN}$	Internal resistor pull-down. IS+		1.3	2.8	3.8	MΩ

5.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. 50kΩ pull-up from PGOOD to VDDP.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER and DRIVER						
t_{LO_EN}	Low time of EN.	V_{VDDH} = steady state.	5			µs
t_{HI_EN}	High time of EN.	V_{VDDH} = steady state.	5			µs
t_{PER_EN}	Period of EN.	V_{VDDH} = steady state.	10			µs
t_{LH_VDDH}	Propagation delay time from VDDP rising to VDDH at 50% level.	EN = 0V, V_{VDDP} = 0V → 5V at 1V/µs, V_{VDDH} = 7.5V.		145		µs
t_{LH_VDRV}	Propagation delay time from EN rising to VDRV at 90% level	V_{VDDP} = 5V, V_{VDDH} steady state, EN = 0V → 5V, V_{VDRV} = 13.5V.		3	4.5	µs
t_{HL_VDRV}	Propagation delay time from EN falling to VDRV at 10% level	V_{VDDP} = 5V, V_{VDDH} steady state, EN = 5V → 0V, V_{VDRV} = 1.5V.		2.5	3.0	µs
$t_{HL\_VDRV\_PD}$	Propagation delay time from VDDP falling to VDRV at 10% level. Timeout mechanism due to loss of power on primary supply.	EN = 5V, V_{VDDP} = 5V → 0V at -1V/µs, V_{VDRV} = 1.5V.		140	160	µs
$t_{LH\_VDRV\_CE}$	Propagation delay time from CE rising to VDRV at 10% level	V_{VDDP} = 5V, VDDH and VDDM fully discharged. EN = CE = 0V → 5V, V_{VDRV} = 1.5V.		185		µs
$t_{HL\_VDRV\_CE}$	Propagation delay time from CE falling to VDRV at 10% level	V_{VDDP} = 5V, V_{VDDH} steady state, EN = 5V, CE= 5V → 0V, V_{VDRV} = 1.5V.		3	4	µs
t_{R_VDRV}	VDRV rise time from EN rising to VDRV from 15% to 85% level	V_{VDDP} = 5V, V_{VDDH} steady state, EN = 0V → 5V, V_{VDRV} = 2.25V to 12.75V.		10		ns
t_{F_VDRV}	VDRV fall time from EN falling to VDRV from 85% to 15% level	V_{VDDP} = xV, V_{VDDH} steady state, EN = xV → 0V, V_{VDRV} = 12.75V to 2.25V.		10		ns
COMPARATORS						

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over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. 50kΩ pull-up from PGOOD to VDDP.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD\_CMP\_VDRV}$	Propagation delay time, comparator input to VDRV asserted low or high.	EN = CE = VDDP V_{UD} = 100mV V_{OD} = 30mV Measure V_{IS+} crossing V_{REF+}, V_{REF-} to 50% V_{VDRV}.	320	395	460	ns

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5.11 Insulation Characteristic Curves

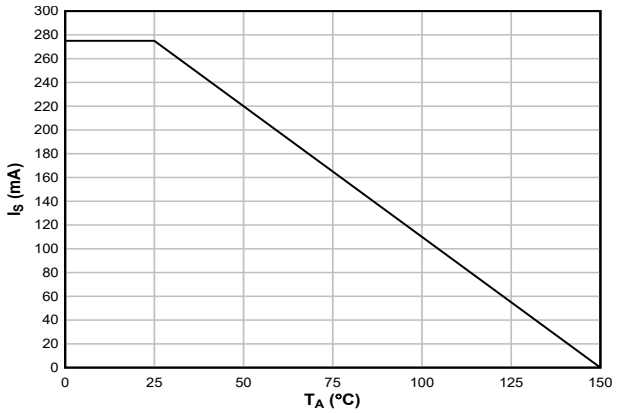

Figure 5-1. Thermal Derating Curve for Limiting Current per VDE and IEC

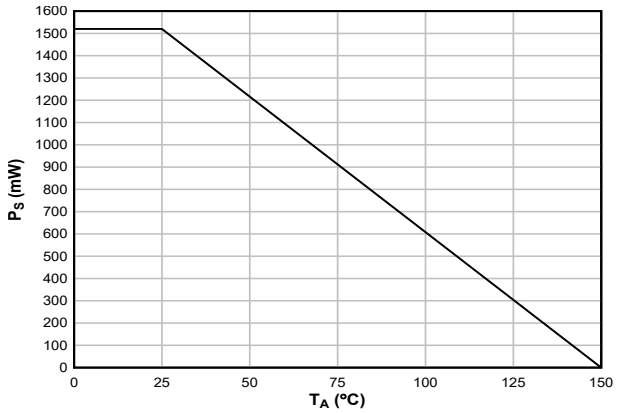

Figure 5-2. Thermal Derating Curve for Limiting Power per VDE and IEC

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6 Detailed Description

6.1 Overview

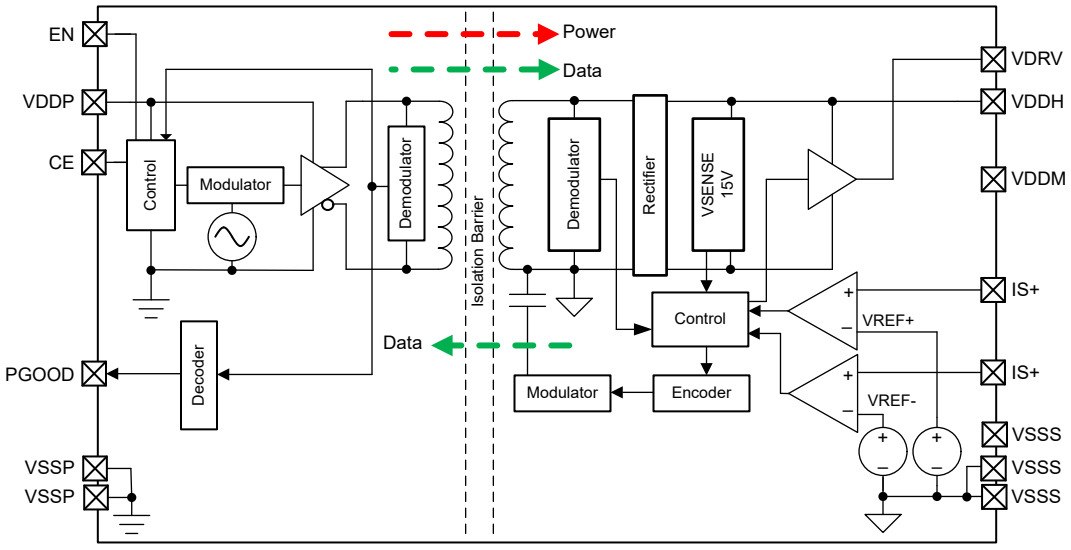
The TPSI31P1-Q1 is designed to be used in automotive pre-charge systems as an alternative to traditional passive pre-charge architectures that typically include costly electromechanical relays (EMR), along with bulky, high power resistors. The TPSI31P1-Q1, combined with external power switches, power inductor and diode, forms an active pre-charge solution. The inductor current is continuously monitored and controlled in a hysteretic mode of operation by the TPSI31P1-Q1 to linearly charge the large capacitance of the downstream system. The TPSI31P1-Q1 is an isolated switch driver that generates its own secondary bias supply from power received on its primary side, therefore no isolated secondary supply is required. With a gate drive voltage of 17V with 1.5 and 2.5A peak source and sink current, a large availability of power switches can be used including SiC FET and IGBT.

The TPSI31P1-Q1 integrates a communication back-channel that transfers status information from the secondary side to the primary side via open-drain output, PGOOD (Power Good) and indicates when the secondary power is valid.

The Functional Block Diagram shows the primary side includes a transmitter that drives an alternating current into the primary winding of an integrated transformer which transfers power from the primary side to the secondary side. The transmitter operates at high frequency (80MHz, nominal) to optimally drive the transformer to its peak efficiency. In addition, the transmitter utilizes spread spectrum techniques to greatly improve EMI performance allowing many applications to achieve CISPR 25 - Class 5. During transmission, data information is transferred to the secondary side alongside with the power. On the secondary side, the voltage induced on the secondary winding of the transformer, is rectified and multiplied, and is regulated to the voltage level of VDDH. Lastly, the demodulator decodes the received data information and drives VDRV high or low, respective of the logic state of the EN pin.

During each transfer of power from the primary side to the secondary side, back-channel state information is automatically sampled, encoded, and sent from the secondary side back to the primary side where it is decoded.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Transmission of the Enable State

The TPSI31P1-Q1 uses a modulation scheme to transmit the pre-charge enable (EN) state information across the isolation barrier. The transmitter modulates the EN signal with an internally generated, high frequency carrier, and differentially drives the primary winding of the isolation transformer. The receiver on the secondary side demodulates the received signal high or low, enabling or disabling the pre-charge function, respectively.

6.3.2 Power Transmission

The TPSI31P1-Q1 does not utilize a secondary side isolated bias supply for its power. The secondary side power is obtained by the transferring of the primary side input power from VDDP across the isolation transformer. The modulation scheme uses spread spectrum techniques to improve EMI performance assisting applications in meeting the CISPR 25 Class 5 standards.

6.3.3 Gate Driver

The TPSI31P1-Q1 has an integrated gate driver that provides a nominal 17V with 1.5 and 2.5A peak source and sink current sufficient for driving many power transistors. When driving external power transistors, TI recommends bypass capacitors ($C_{DIV2} \geq 3 * C_{DIV1}$) from VDDH to VDDM and VDDM to VSSS with an equivalent series capacitance of minimum of 30 times the equivalent gate capacitance. This minimizes the voltage droop on the supplies due to charging the external gate capacitance of the external power transistors.

6.3.4 Chip Enable (CE)

The TPSI31P1-Q1 has an active high chip enable, CE. When CE is asserted high and VDDP is present, the device enters its active mode of operation and power transfer occurs from the primary side to the secondary side. When CE is asserted low while VDDP is present, the device enters standby and no power transfer occurs from primary side to the secondary side and VDRV will be asserted low. Over time, VDDH and VDDM fully discharges depending on the amount of loading present on these rails.

6.3.5 Comparators

The TPSI31P1-Q1 includes two identical isolated comparators. A simplified block diagram is shown in Figure 6-1. The positive input of each comparator monitors the voltage on the IS+ pins referenced to VSSS. One comparator has an integrated reference, VREF+, at the comparator negative input terminal. The second comparator has an integrated reference, VREF-, at the comparator negative input terminal. Both references have an overall accuracy of ±1.5% over voltage and temperature. The reference voltages are not available externally.

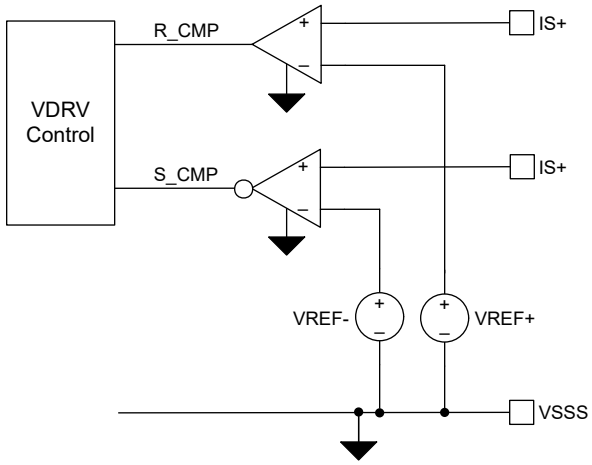


Figure 6-1. Comparator Block Diagram

The outputs of the comparators, R_CMP and S_CMP, interface to logic that controls the state of VDRV based on the output state of each comparator as shown in VDRV Control Logic

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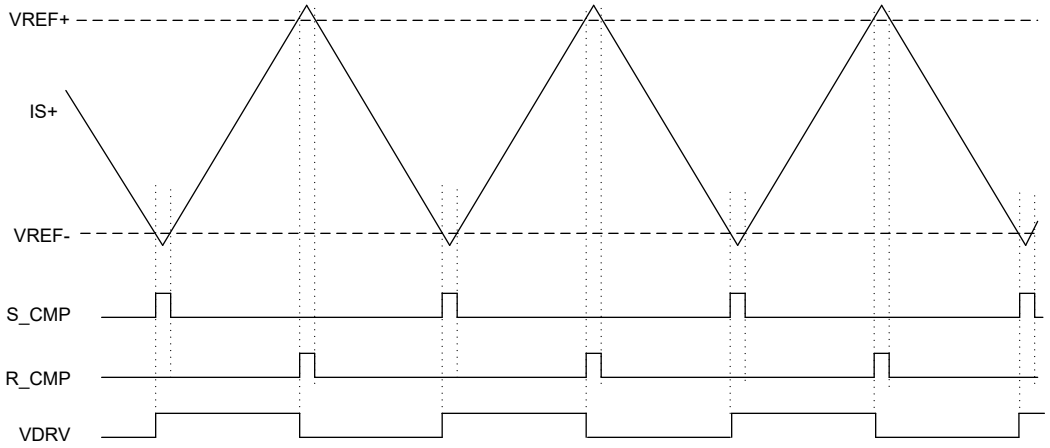

Figure 6-2. VDRV Control Logic

6.3.6 VDDP, VDDH, and VDDM Under-voltage Lockout (UVLO)

The TPSI31P1-Q1 implements an internal UVLO protection feature for both input (VDDP) and output power supplies (VDDM and VDDH). The device remains disabled until VDDP exceeds its rising UVLO threshold. When the VDDP supply voltage falls below its falling threshold voltage, the device attempts to send data information to quickly assert VDRV low, regardless of the state of EN. This depends on the rate of VDDP loss. If VDDP collapses too fast to send the information, a timeout mechanism ensures VDRV is asserted low within $t_{HL\_VDRV\_PD}$. A VDDP ULVO event causes PGOOD to assert low.

The VDDH and VDDM UVLO circuits monitor the voltage on VDDH and VDDM, respectively. VDRV is only asserted high if both the VDDH and VDDM UVLO rising thresholds are surpassed. If either VDDH or VDDM fall below their respective UVLO falling thresholds, VDRV is immediately asserted low. The UVLO protection blocks feature hysteresis, which helps to improve the noise immunity of the power supply. During turn on and turn off, the driver sources and sinks a peak transient current, which can result in voltage drop of the VDDH and VDDM power supplies. The UVLO protection circuits ignores the associated noise during these normal switching transients.

6.3.7 Keep-off Circuitry

The TPSI31P1-Q1 contains keep-off circuitry on the output driver. The purpose of the keep-off circuitry is to clamp the gate voltage below an acceptable level to prevent the external power switch from turning on when no power is present on the secondary rails. The keep-off circuitry can be used to replace or greatly reduce the requirements of an external bleed-off resistor on the external power switch.

Figure 6-3 shows a simplified schematic of the keep-off circuitry. Transistors MP1 and MN1 form the driver that provides the gate current to drive the external power switch (M1). When no power is available on the secondary, the 1MΩ resistor, is connected from the drain to gate of MN1, forming an NMOS diode configuration. Any external coupling into the VDRV signal, via the M1 parasitic gate-to-drain and gate-to-source capacitances, can cause the VDRV signal to rise. The diode configuration of MN1 sinks this current to keep VDRV from rising too high, clamping VDRV to V_{ACT_CLAMP} . This is sufficient to keep most power switches off. If desired, an additional resistance can also be placed (on the order of 250kΩ or higher) across the gate-to-source of M1. Note that any resistance applied requires power from the secondary supply in normal operation and must be accounted for in the overall power budget.

In addition to the MN1 diode clamp, the body diode of MP1 can also help absorb any coupling into VDRV. The equivalent capacitance, C_{eq}, which is the series combination of C_{DIV1} and C_{DIV2} is typically on the order of 100's of nanofarads for most applications. If power transfer has ceased for some time, this capacitance is fully discharged to VSSS and clamps VDRV a diode above VSSS via the body diode of MP1 connected to VDDH. Any external coupling into the VDRV signal, via the M1 parasitic gate-to-drain and gate-to-source capacitances, is absorbed by C_{eq}, minimizing the voltage rise on VDRV.

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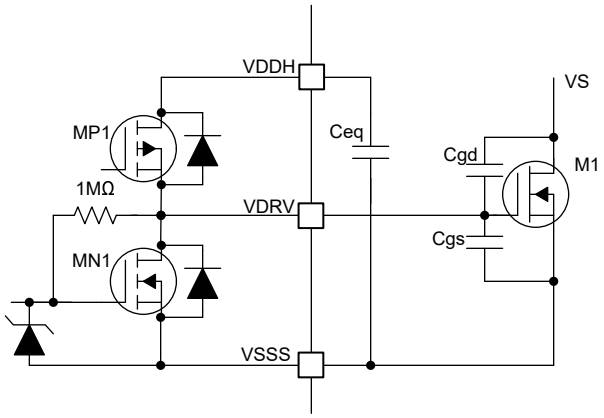

Figure 6-3. Keep-off Circuitry

6.3.8 Thermal Shutdown

The TPSI31P1-Q1 has an integrated temperature sensor. The sensor monitors its local temperature. When the sensor reaches its threshold, it automatically disables power transfer from the primary side to the secondary side, and sends data information to disable the driver, VDRV. The power transfer and driver are disabled until the local temperature reduces enough to re-engage.

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6.4 Device Functional Modes

Table 6-1 summarizes the functional modes for the TPSI31P1-Q1.

Table 6-1. TPSI31P1-Q1 Functional Modes (1)

CE	VDDP	VDDH, VDDM	EN	VDRV	PGOOD	COMMENTS
X	Powered Down(3)	Powered Down(5)	X	L	L	Powered Down: VDRV output disabled, keep off circuitry applied.
L	Powered Up(2)	Powered Down(5)	X	L	L	Disabled Operation: When CE is asserted low, power transfer to the secondary ceases. VDDH and VDDM rails discharge pending loading. VDRV output disabled, keep off circuitry applied.
H	Powered Up(2)	Powered Up(4)	L	L	H	VDRV asserted low. PGOOD indicates secondary supply status. Power transfer occurs to the VDDH and VDDM rails.
H	Powered Up(2)	Powered Up(4)	H	L or H	H	Pre-charge Operation: VDRV output state controlled by comparator outputs, R_CMP and S_CMP. PGOOD indicates secondary supply status.

(1) X: do-not-care.
(2) V_{VDDP} ≥ VDDP_UVLO threshold.
(3) V_{VDDP} < VDDP_UVLO threshold.
(4) V_{VDDH} ≥ VDDH_UVLO threshold and V_{VDDM} ≥ VDDM_UVLO threshold.
(5) V_{VDDH} <VDDH_UVLO threshold or V_{VDDM} < VDDM_UVLO threshold.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPSI31P1-Q1 is designed to be used in automotive pre-charge systems as an alternative to traditional passive pre-charge architectures that typically include costly electromechanical relays (EMR), along with the bulky, large, high power resistors. The TPSI31P1-Q1, combined with external power switches, power inductor and diode, forms an active pre-charge solution. The inductor current is monitored and controlled in a hysteretic mode of operation by the TPSI31P1-Q1 to linearly charge the large capacitance of the downstream system. The TPSI31P1-Q1 is an isolated switch driver that generates its own secondary bias supply from power received on its primary side, therefore no isolated secondary supply is required. With a gate drive voltage of 17V with 1.5 and 2.5A peak source and sink current, a large availability of power switches can be used including SiC and IGBTs.

7.2 Typical Application

The simplified circuit diagram shown in Figure 7-1 is a typical active pre-charge application using the TPSI31P1-Q1. The TPSI31P1-Q1 interfaces to a microcontroller residing on the primary side of the TPSI31P1-Q1. The external power inductor, L1, along with power diode, D1, and power FET, M1, form a buck converter topology. M2 is an optional power FET and allows for reverse blocking. M2 is statically enabled during pre-charge. The shunt resistor, R_{SHUNT}, is used to monitor the current in L1 by forming a voltage across IS+ relatively to VSSS.

With power applied to VDDP and CE high, the pre-charge cycle is initiated by asserting EN high. If IS+ is below VREF-, VDRV is asserted high by the TPSI31P1-Q1 to enable M1, which begins to store energy in L1.Once the current in L1 reaches its set peak level, which occurs when IS+ reaches VREF+, VDRV is asserted low to disable M1. At this point, stored energy in L1 is released into the capacitance, C_{LINK}. As the inductor current decreases, the voltage on IS+ falls to VREF-, and M1 is enabled again. This process continues throughout the entire pre-charge cycle.

The TPSI31P1-Q1 keeps VDRV asserted high upon pre-charge completion while EN state is high.

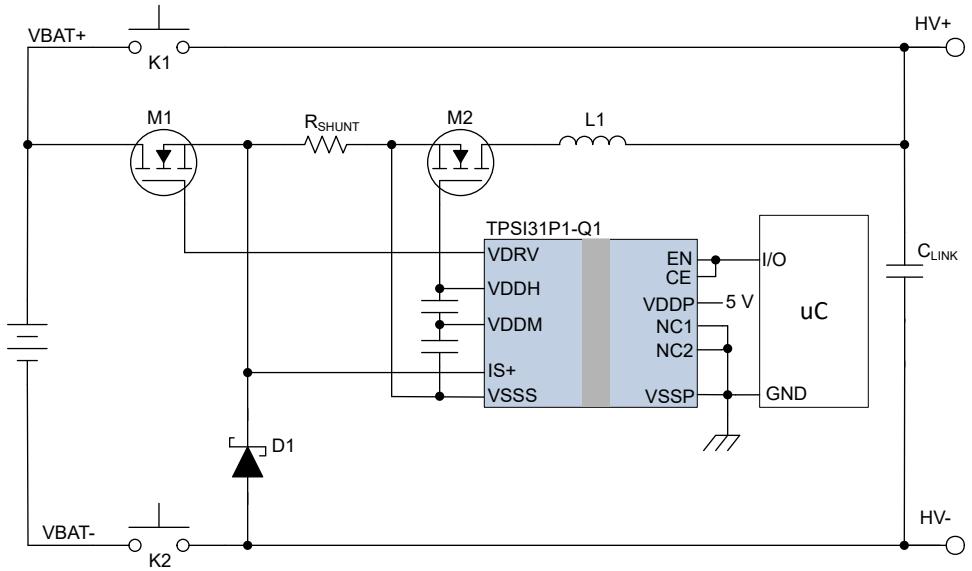

Figure 7-1. Typical Active Pre-Charge Application

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7.2.1 Design Requirements

Table 7-1 lists the design requirements for an active pre-charge system.

Table 7-1. TPSI31P1-Q1 Design Requirements

DESIGN PARAMETERS	
Link capacitance	2mF
Pre-charge time	800ms
Battery voltage	800V
Peak inductor current	< 5A

7.2.2 Detailed Design Procedure

The battery voltage (V_{BAT}), link capacitance (C_{DC_LINK}), along with the target pre-charge time determines the average charging current (I_{AVG}) required. This may be computed as follows:

$$I_{AVG} \geq \frac{C_{DC_{LINK}} \times V_{BAT}}{t_{CHARGE}} = \frac{2mF \times 800V}{800ms} = 2A \quad (1)$$

The average current is defined as:

$$I_{AVG} = \frac{I_{PEAK} + I_{MIN}}{2} \quad (2)$$

The peak current, I_{PEAK}, represents the maximum current through the inductor, and is defined by:

$$I_{PEAK} = \frac{V_{REF+}}{R_{SENSE}} \quad (3)$$

Similarly, the minimum current, I_{MIN}, represents the minimum current through the inductor, and is defined by:

$$I_{MIN} = \frac{V_{REF-}}{R_{SENSE}} \quad (4)$$

Therefore, to find the shunt resistor, R_{SENSE}, required to properly set the inductor current, the following equation can be used:

$$R_{SENSE} = \frac{V_{REF+} + V_{REF-}}{2I_{AVG}} = \frac{1.23V + 0.16V}{2 \times 2A} = 348m\Omega \quad (5)$$

For this design, R_{SENSE} was selected as 300mΩ.

The peak inductor current is computed as:

$$I_{PEAK} = \frac{1.23V}{300m\Omega} = 4.1A \quad (6)$$

The minimum inductor current is computed as:

$$I_{MIN} = \frac{0.16V}{300m\Omega} = 0.53\ A \quad (7)$$

The average inductor current is computed as:

$$I_{AVG} = \frac{I_{PEAK} + I_{MIN}}{2} = \frac{4.1A + 0.53A}{2} = 2.32A \quad (8)$$

During pre-charge, due to the hysteretic control, the switching frequency of the FET changes over time as the voltage on the link capacitance increases from fully discharged to fully pre-charged. The maximum switching

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frequency, $f_{SW\_MAX\_FET}$, occurs when the voltage on the link capacitance reaches its midpoint value, $V_{BAT}/2$. This occurs at half the total pre-charge time.

The minimum power transfer of the TPSI31P1-Q1 is limited to 42mW at 85 °C. Since the FET is switching during pre-charge, the total gate charge of the FET must be fully charged and discharged each switching cycle. This minimum power transfer constrains the maximum frequency the TPSI31P1-Q1 can switch the FET. The FET selected has a total gate charge, Q_{TOTAL}, of 30nC. Assuming V_{GS} = 15V to ensure full enhancement of the FET, the maximum switching frequency is:

$$f_{SW\ MAX\ FET} = \frac{P}{V_{GS} \times Q_{TOTAL}} = \frac{42mW}{15V \times 30nC} = 93.3kHz \quad (9)$$

Based on the maximum switching frequency, the minimum inductance, L_{MIN}, can be computed:

$$L_{MIN} \geq \frac{V_{BAT}}{4 \times F_{SW\ MAX\ FET} \times \Delta I} \quad (10)$$

$$L_{MIN} \geq \frac{800V}{4 \times 93.3kHz \times (4.1A - 0.53A)} \geq 600.5\mu H \quad (11)$$

For this design, two inductors connected in series with a total value of 940µH was selected which reduces the maximum switching frequency to 61.3kHz, well within the power transfer capabilities of the TPSI31P1-Q1. It is important that an inductor be chosen that can support the average and peak currents required. Higher inductor and ΔI values reduce the switching frequency and power requirements.

7.2.2.1 C_{DIV1}, C_{DIV2} Capacitance

The C_{DIV1} and C_{DIV2} capacitors required depends on the amount of drop that can be tolerated on the VDDH rail during switching of the external load. The charge stored on the C_{DIV1} and C_{DIV2} capacitors is used to provide the current to the load during switching. During switching, charge sharing occurs and the voltage on VDDH drops. At a minimum, TI recommends that the total capacitance formed by the series combination of C_{DIV1} and C_{DIV2} be sized to be at least 30 times the total gate capacitance to be switched. This sizing results in an approximate 0.5V drop of the VDDH supply rail that is used to supply power to the VDRV signal. Equation 12 and Equation 13 can be to used to calculate the amount of capacitance required for a specified voltage drop.

C_{DIV1} and C_{DIV2} must be of the same type and tolerance.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V},\ n \geq 3.0 \quad (12)$$

$$C_{DIV2} = n \times C_{DIV1},\ n \geq 3.0 \quad (13)$$

where

- n is a real number greater than or equal to 3.0.
- C_{DIV1} is the external capacitor from VDDH to VDDM.
- C_{DIV2} is the external capacitor from VDDM to VSSS.
- Q_{LOAD} is the total charge of the load from VDRV to VSSS.
- ΔV is the voltage drop on VDDH when switching the load.

Note

C_{DIV1} and C_{DIV2} represent absolute capacitor and components selected must be adjusted for tolerances and any derating necessary to achieve the required capacitance.

Larger values of ΔV can be used in the application, but excessive droop can cause the VDDH under-voltage lockout falling threshold ($V_{VDDH\_UVLO\_F}$) to be reached and cause VDRV to be asserted low. Note that as the series combination of C_{DIV1} and C_{DIV2} capacitance increases relative to Q_{LOAD}, the VDDH supply voltage drop decreases, but the initial charging of the VDDH supply voltage during power up increases.

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For this design, a total gate charge for switching FET is 30nC. For a ΔV = 0.5V,

$$C_{DIV1} = \left(\frac{3+1}{3}\right) \times \frac{30nC}{0.5V} = 80nF \quad (14)$$

$$C_{DIV2} = 3 \times 80nF = 240nF \quad (15)$$

To reduce ΔV further, capacitances for this design were selected as:

$$C_{DIV1} = 330nF \quad (16)$$

$$C_{DIV2} = 1\mu F \quad (17)$$

7.2.3 Application Curves

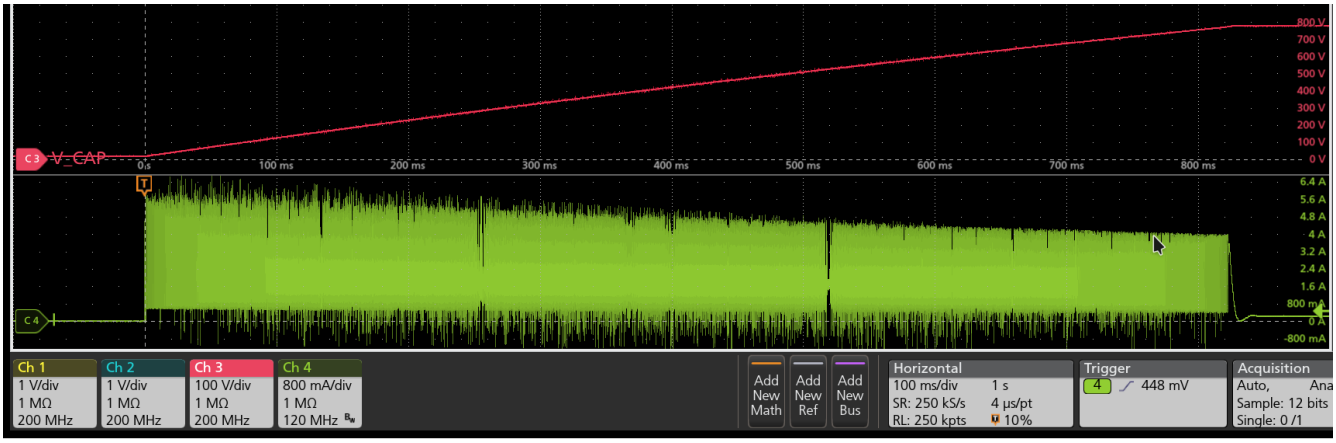

Figure 7-2. Typical Active Pre-charge Waveforms

7.2.4 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 7-3 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

Figure 7-4 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is $1200V_{RMS}$ with a lifetime of 101 years.

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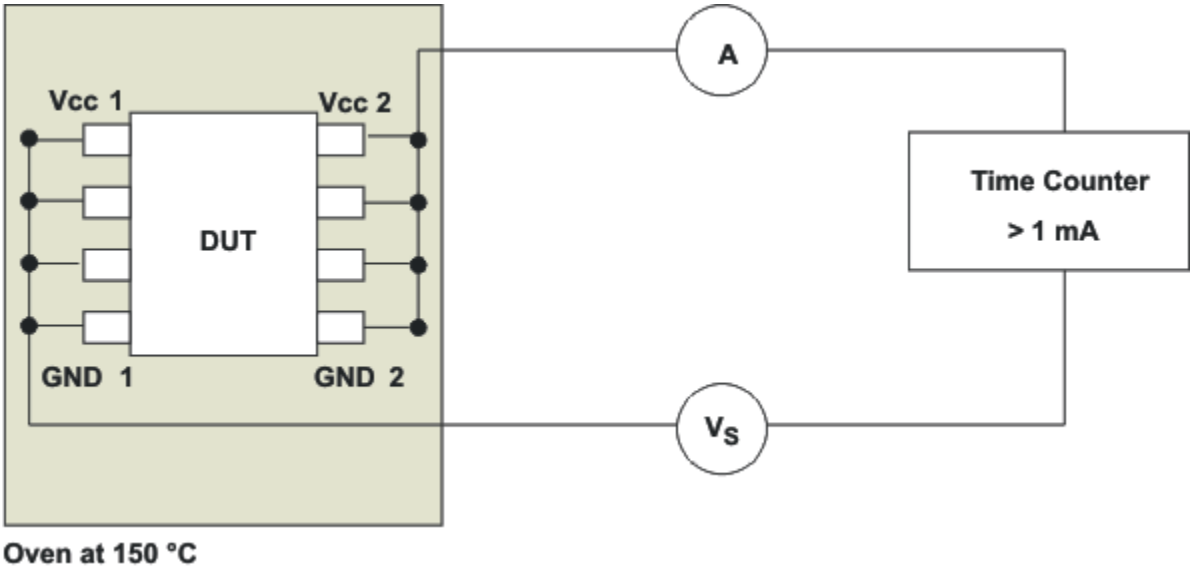

Figure 7-3. Test Setup for Insulation Lifetime Measurement

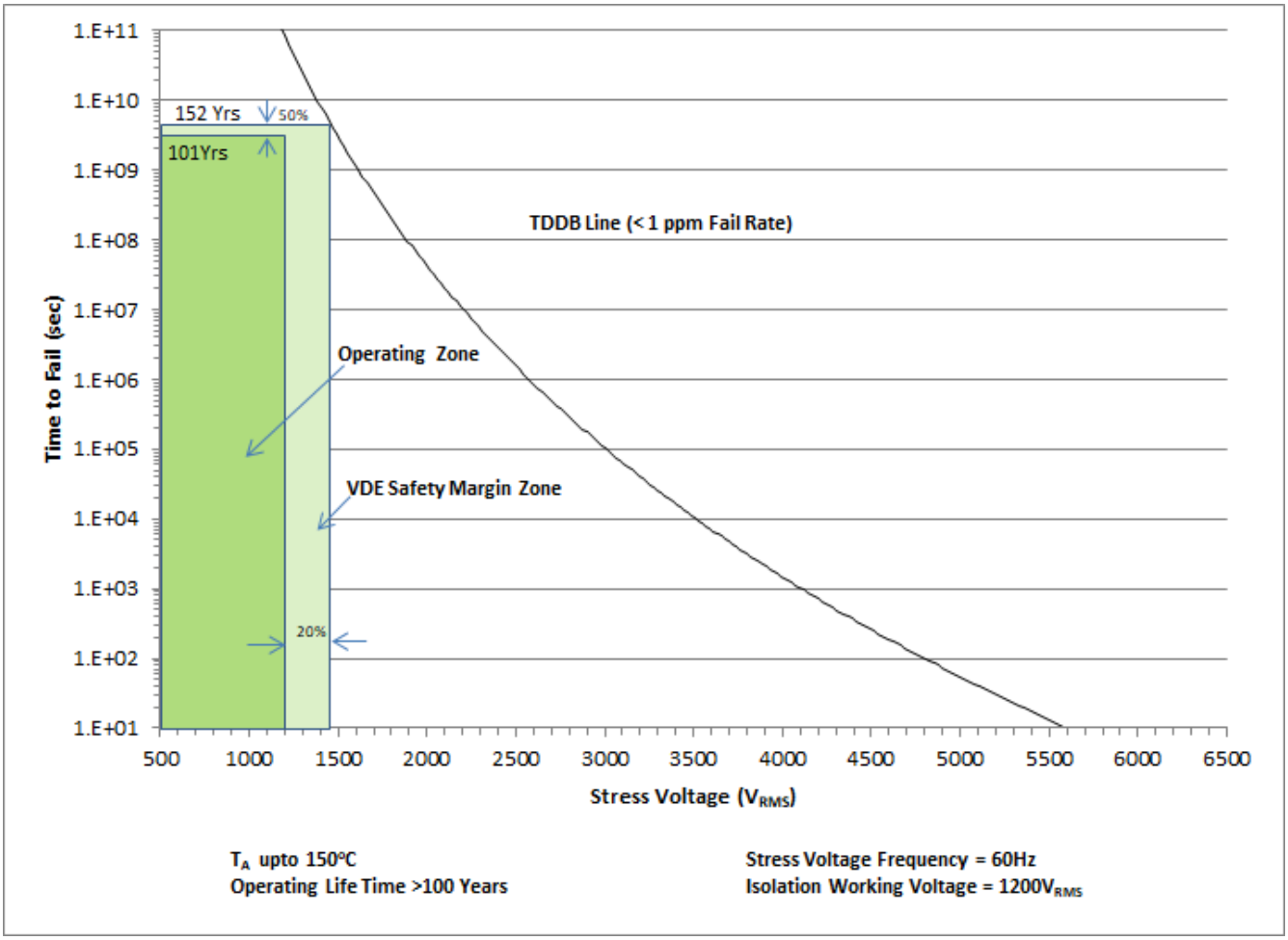

Figure 7-4. Insulation Lifetime Projection Data

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7.3 Power Supply Recommendations

To help ensure a reliable supply voltage, TI recommends that the C_{VDDP} capacitance from VDDP to VSSP consists of a 0.1µF bypass capacitor for high frequency decoupling in parallel with a 1µF for low frequency decoupling. Low-ESR and low-ESL capacitors must be connected close to the device between the VDDP and VSSP pins.

7.4 Layout

7.4.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the TPSI31P1-Q1. Some key guidelines are:

- Component placement:
  - Place the driver as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDH and VDDM pins and the VDDM and VSSS pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDP and VSSP pins.
  - Minimize parasitic capacitance on the RESP pin.
- Grounding considerations:
  - Limit the high peak currents that charge and discharge the transistor gates to a minimal physical area. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. Place the gate driver as close as possible to the transistors.
  - Connect the driver VSSS to the Kelvin connection of MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, connect the VSSS pin as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- EMI considerations:

  The TPSI31P1-Q1 employs spread spectrum modulation (SSM), and in some systems, no additional system design considerations are required to meet the EMI performance needs. However, the system designer may choose to take additional measures to minimize EMI depending on the system requirements and safety preferences of the system designer. The measures listed below reduce emissions by providing a capacitive return path from the secondary side to the primary side or by increasing the common mode loop impedance with an inductive component on the primary side.

  - Inductive components: A pair of ferrite beads or a common mode choke with a high frequency impedance on the order of TBD kΩ can be placed in series with VDDP supply and VSSP ground.
  - Capacitive components: Most system designs already employ discrete Y capacitors or contain an amount of parasitic Y capacitance between the high voltage and low voltage domains. If this Y capacitance is located on the same board as the TPSI31P1-Q1, they act as a capacitive return path.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. TI recommends a PCB cutout or groove to prevent contamination that can compromise the isolation performance.
- Thermal considerations:
  - Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - If the system has multiple layers, TI also recommends connecting the VDDH and VSSS pins to internal ground or power planes through multiple vias of adequate size. These vias must be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

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7.4.2 Layout Example

Figure 7-5 shows a PCB layout example with the signals and key components labeled.

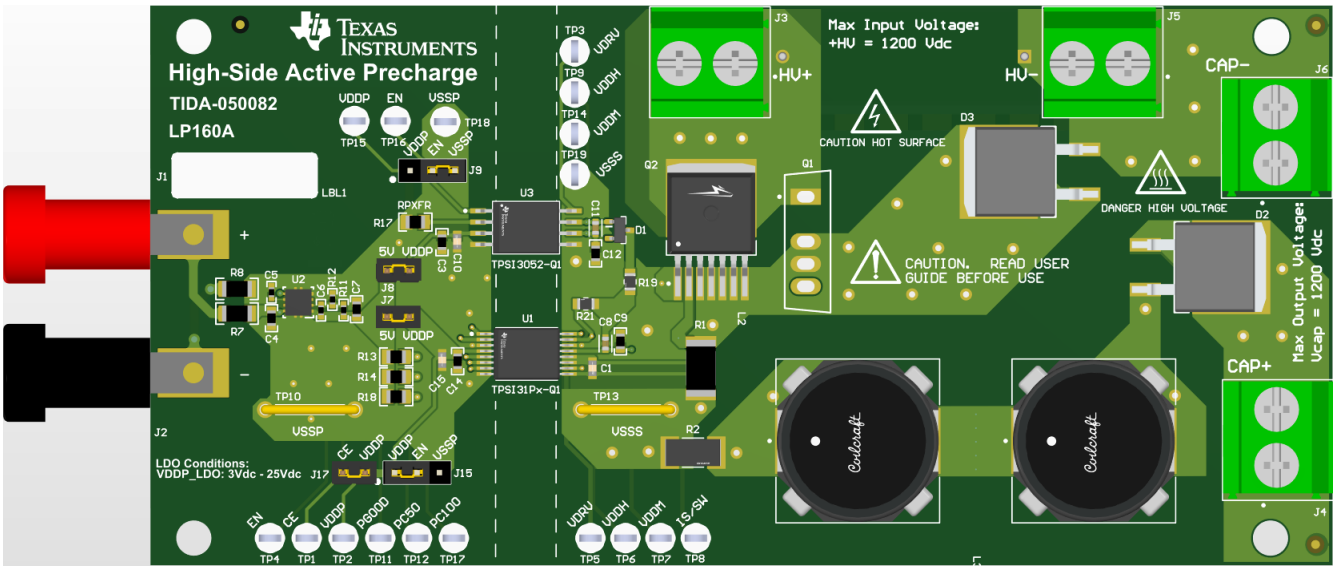

Figure 7-5. 3-D PCB View

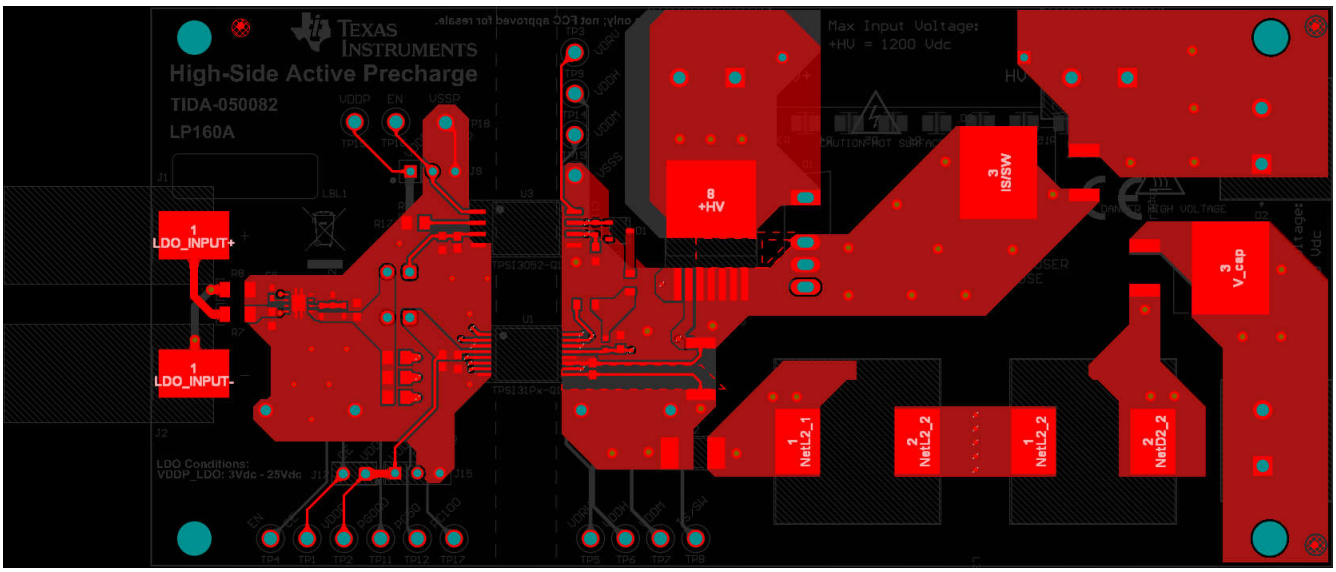

Figure 7-6. Top Layer

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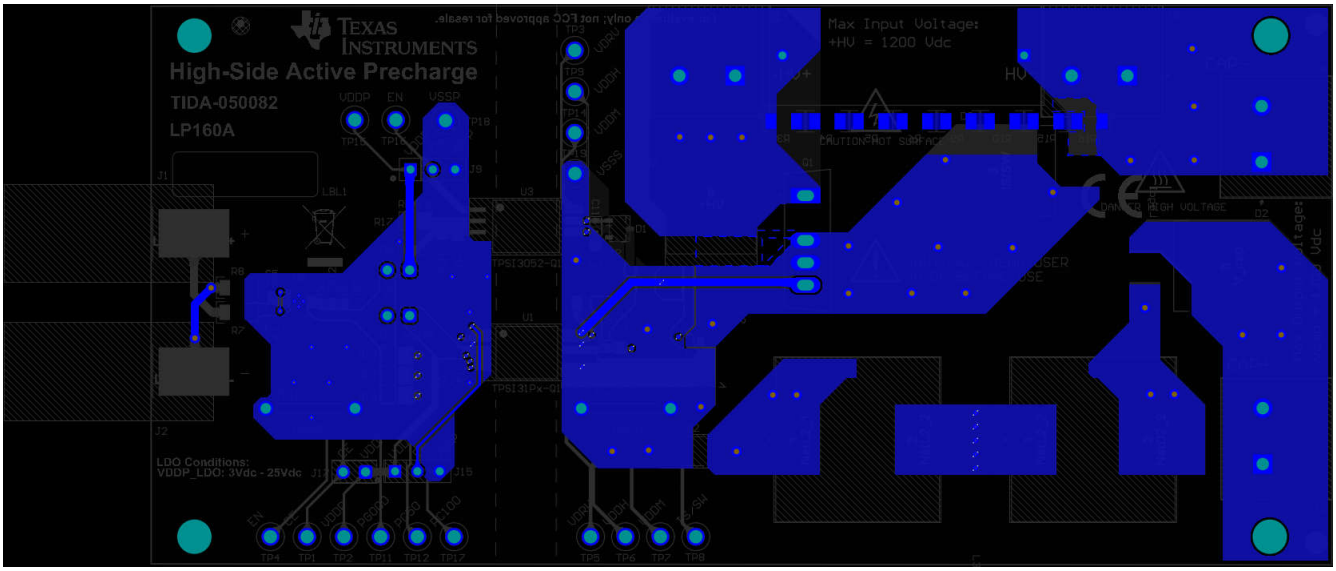

Figure 7-7. Bottom Layer

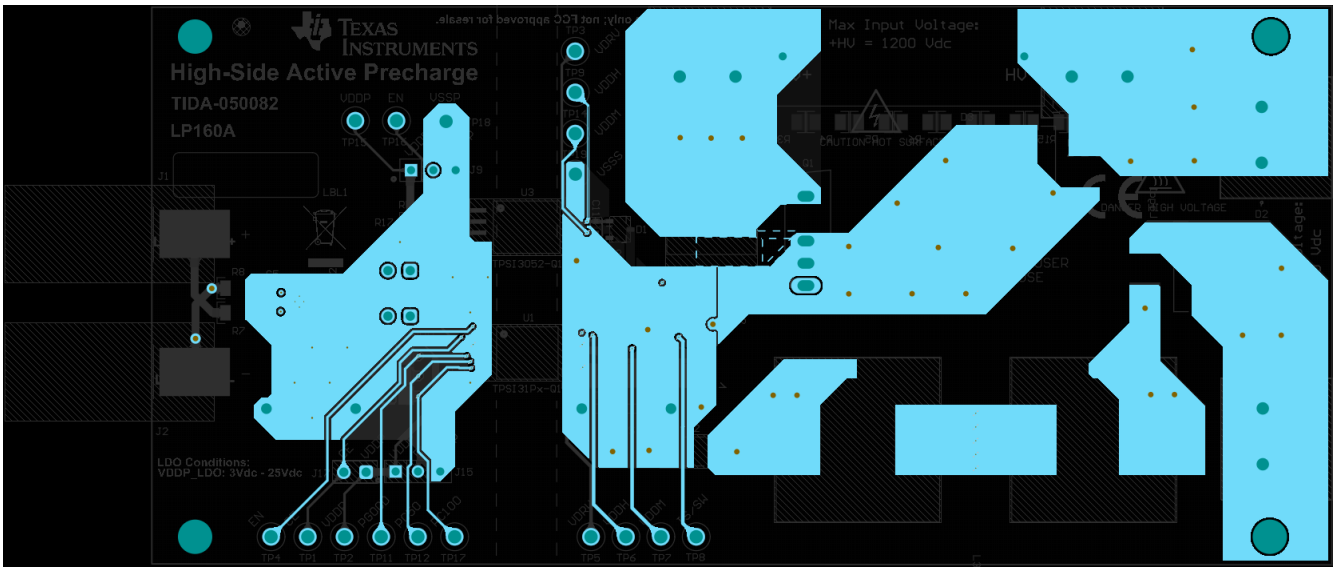

Figure 7-8. Signal Layer 1

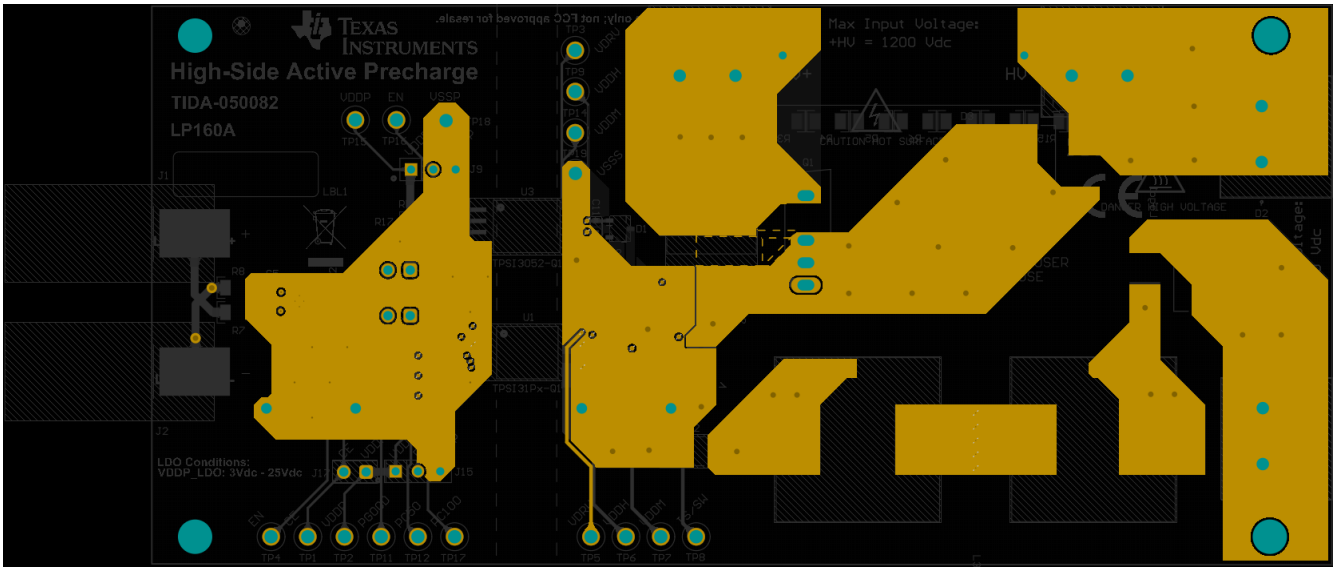

Figure 7-9. Signal Layer 2

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

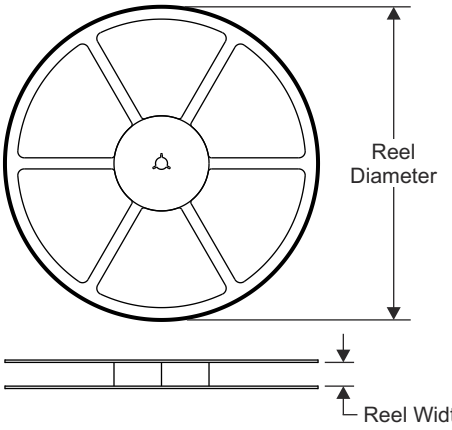
DATE	REVISION	NOTES
October 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

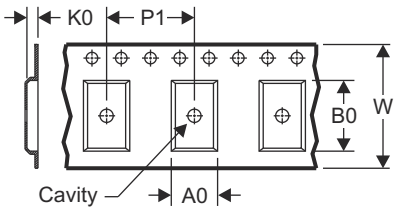
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

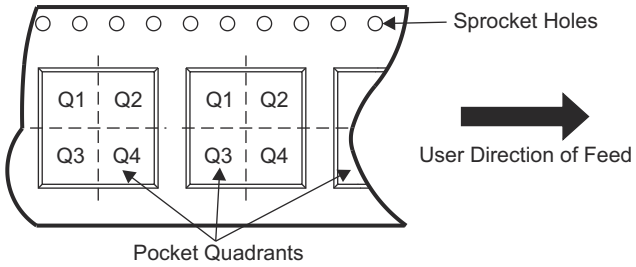


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

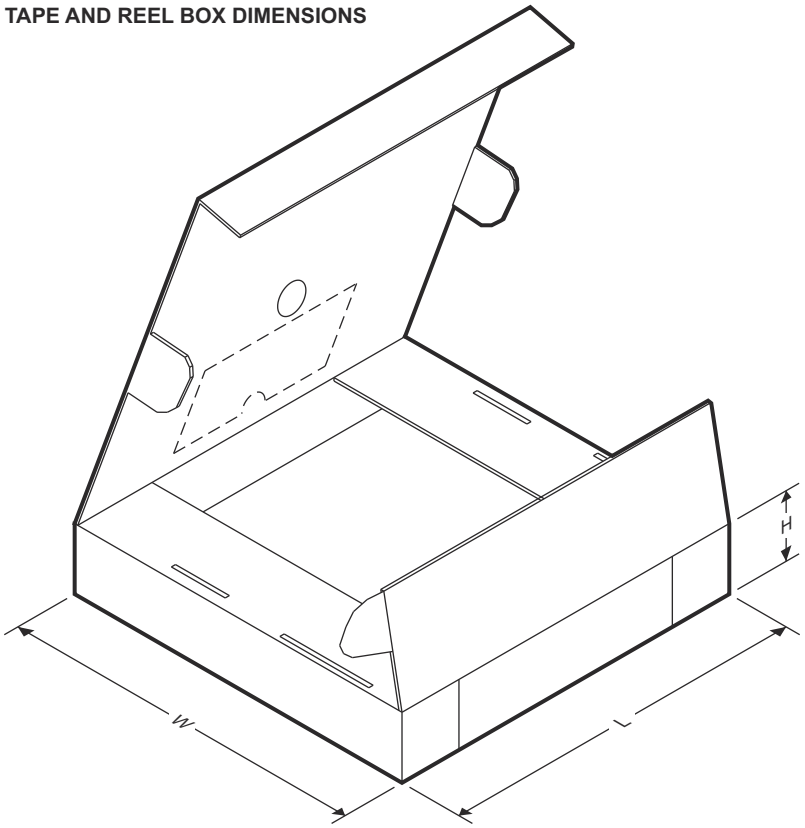


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPSI31P1QDVXRQ1	SSOP	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



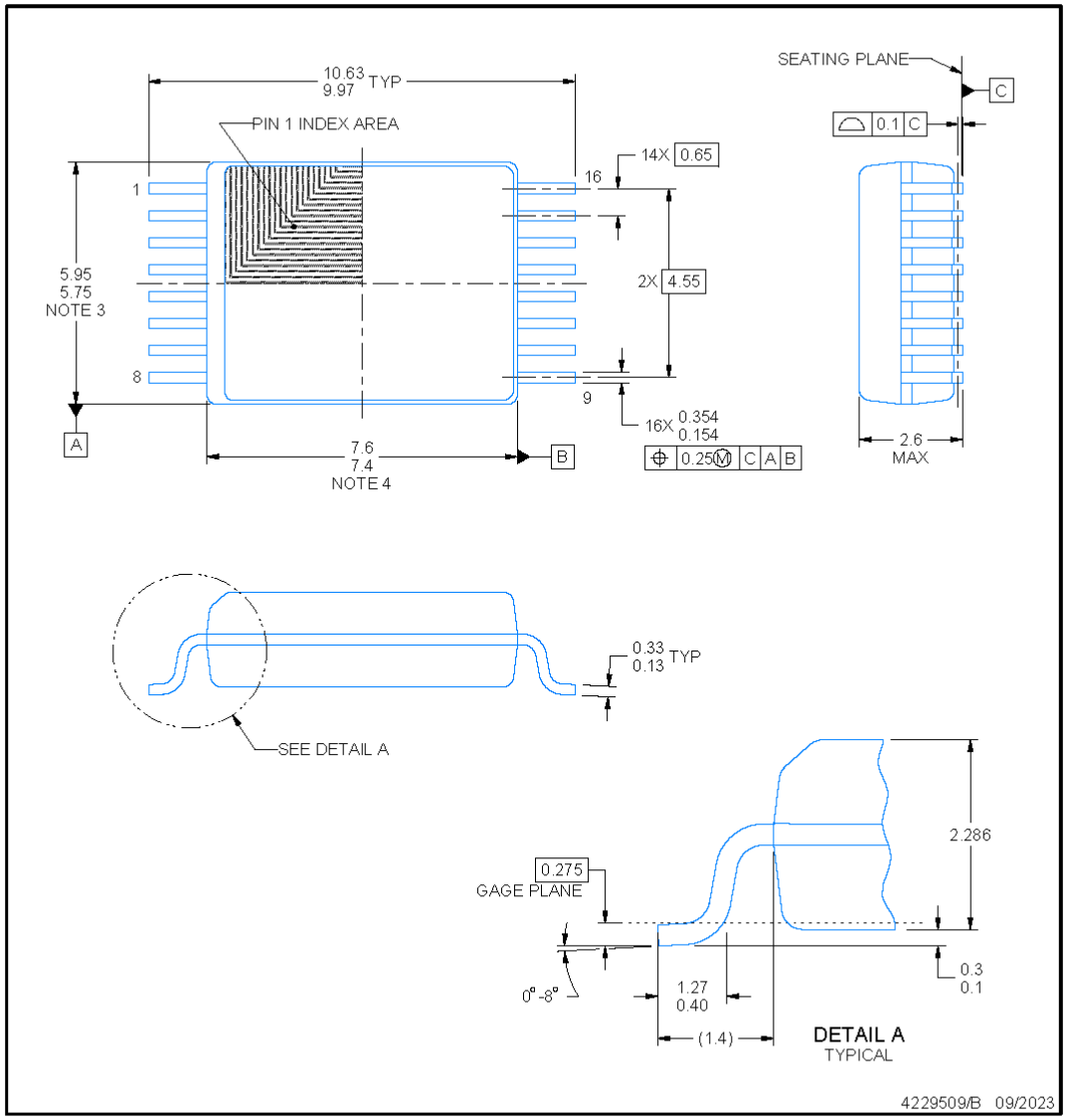
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPSI31P1QDVXRQ1	SSOP	DVX	16	1000	350.0	350.0	43.0

PACKAGE OUTLINE

DVX0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

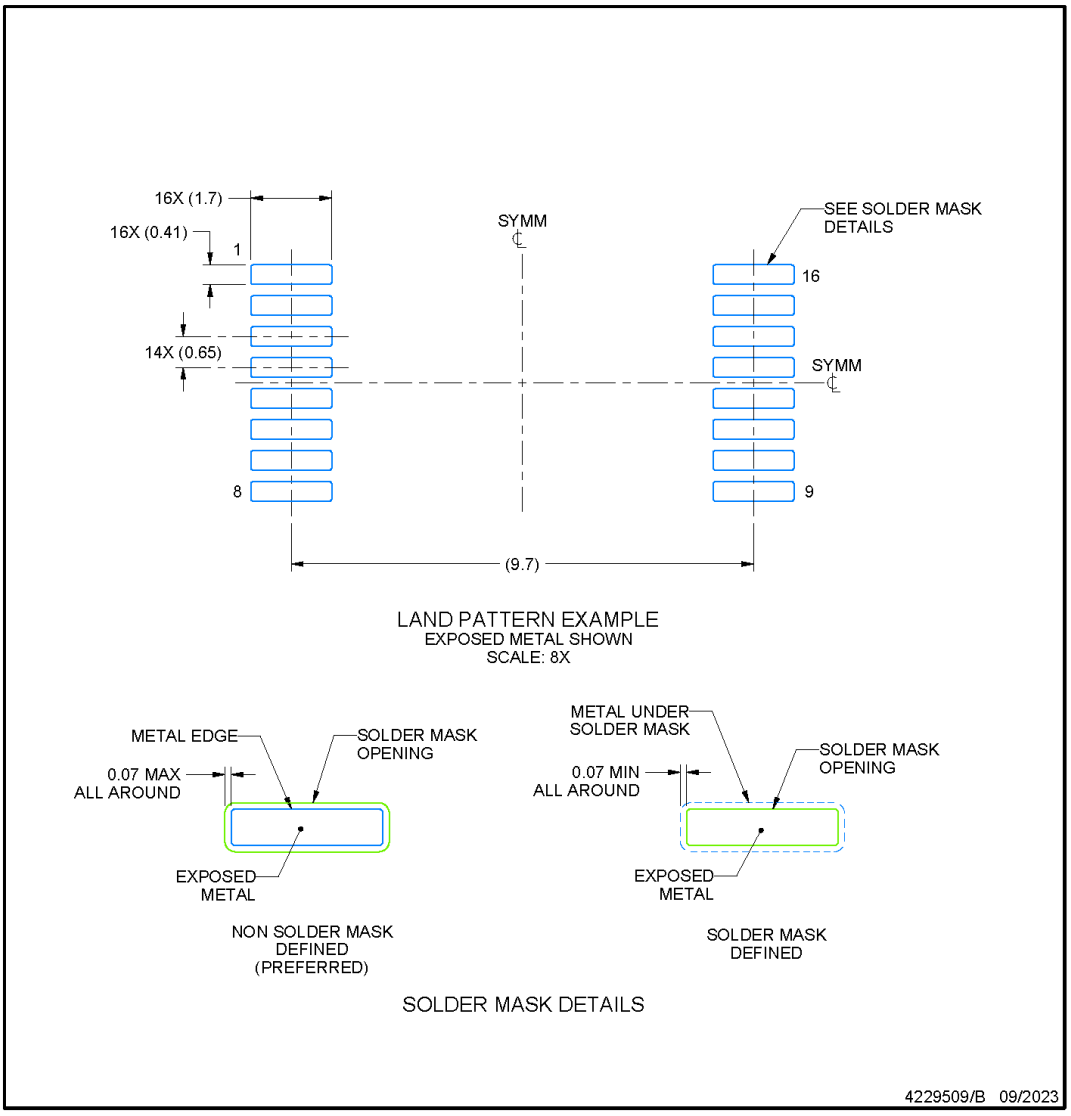
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DVX0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



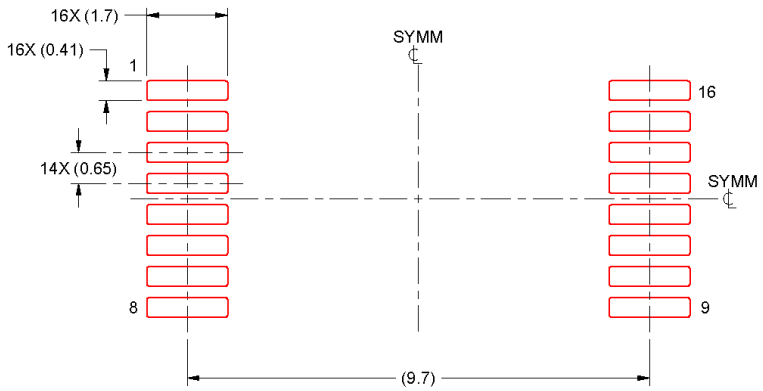
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DVX0016A — **SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

DWG_NO:3/REV:3 MM_YYYY:3

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPSI31P1QDVXRQ1	Active	Preproduction	SO-MOD (DVX) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPSI31P1QDVXRQ1.A	Active	Preproduction	SO-MOD (DVX) | 16	1000 | LARGE T&R	-	Call TI	Call TI	See PTPSI31P1QDVXRQ1	
PTPSI31P1QDVXRQ1.B	Active	Preproduction	SO-MOD (DVX) | 16	1000 | LARGE T&R	-	Call TI	Call TI	See PTPSI31P1QDVXRQ1	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

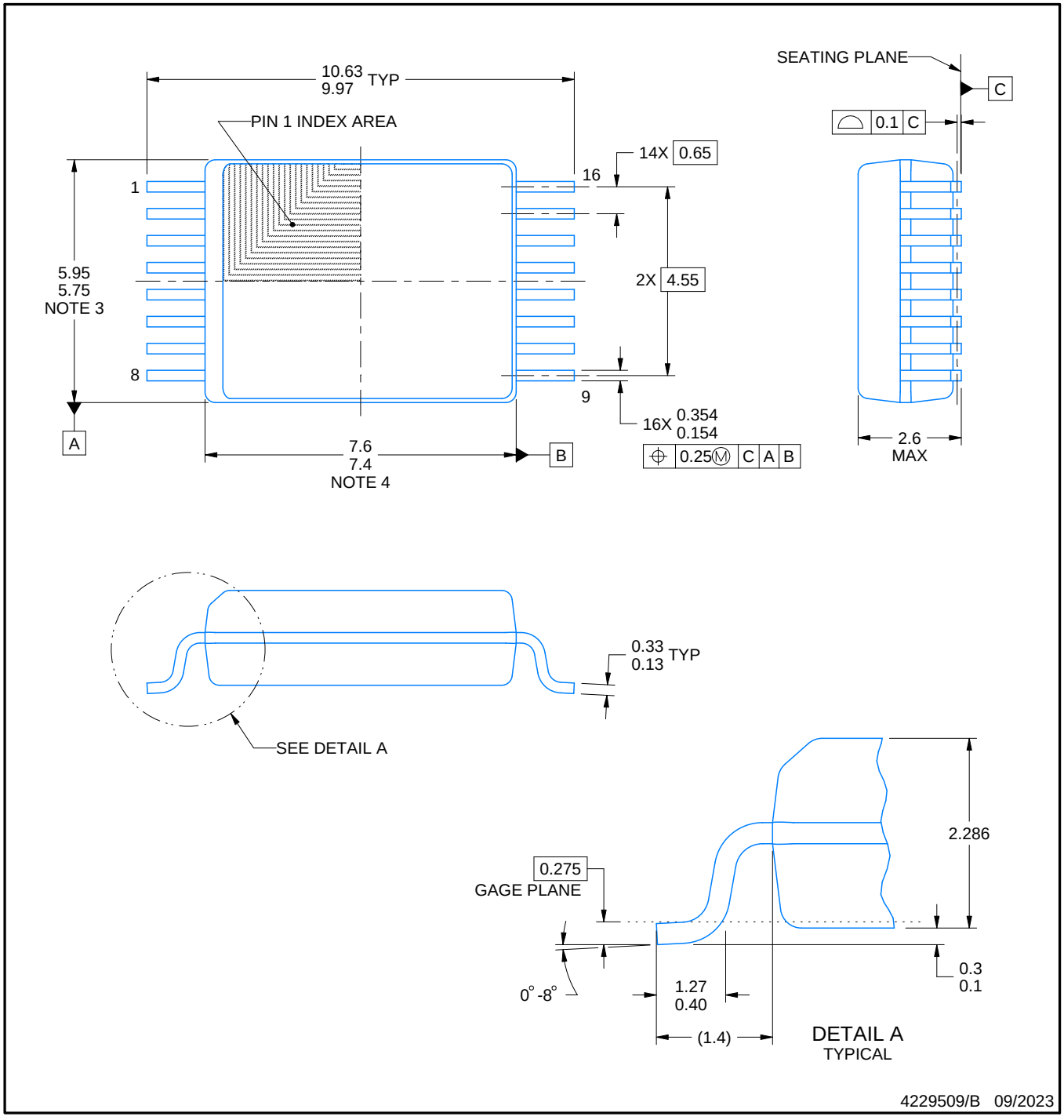
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DVX0016A

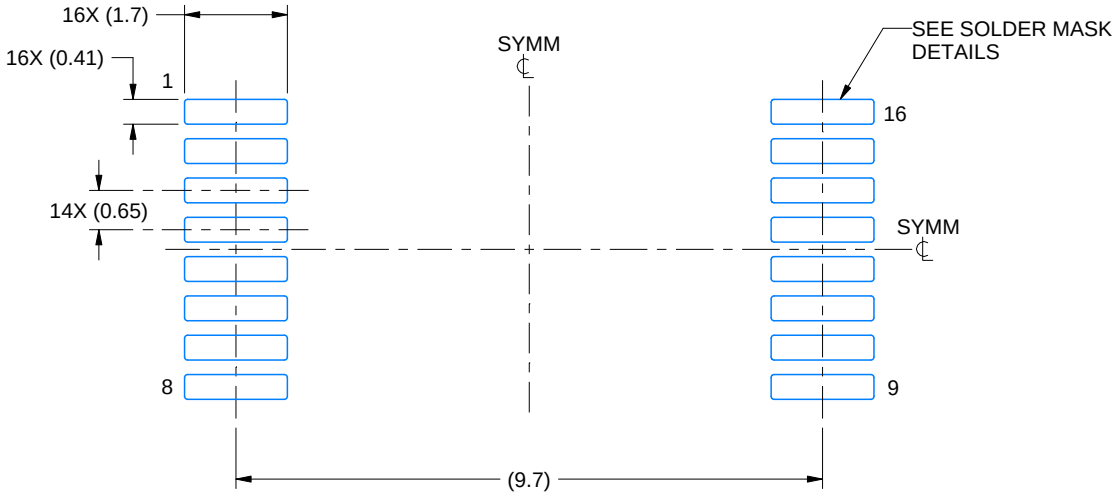
SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE

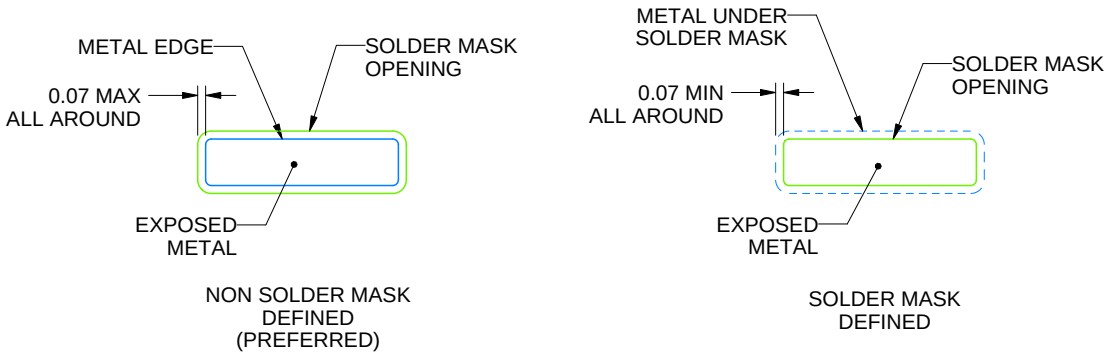


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4229509/B 09/2023

NOTES: (continued)

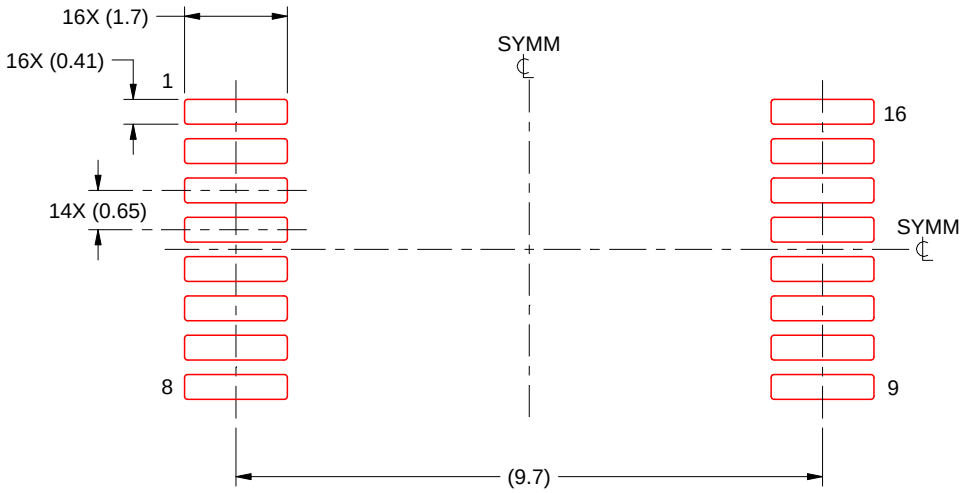
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DVX0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

DWG_NO:3/REV:3 MM_YYYY:3

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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