TPS929160-Q1 16-Channel, Automotive, 40V, High-Side (O)LED Driver With FlexWire™ Interface

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- 16-channel precision high-side current output:
  - Device supply voltage 4.5V to 40V
  - LED supply voltage 4V to 36V
  - Up to 100mA channel current set by resistor
  - 2-bit global, 6-bit independent current setting
  - High-current accuracy < ±5% at 5mA to 100mA
  - Low voltage drop 750mV at 100mA
  - 12-bit independent PWM dimming
  - Programmable PWM frequency up to 20kHz
  - Phase-shift PWM dimming
  - Ultra low quiescent in sleep mode supported by EN and NSTB pin
  - Linear and exponential dimming method
- FlexWire™ control interface
  - Up to 1MHz clock frequency
  - Maximum 16 devices on one FlexWire bus
  - Up to 24 bytes data transaction in one frame
  - 5V LDO output to supply CAN transceiver
- Diagnostic and protection:
  - Programmable FAIL-SAFE state
  - LED open-circuit detection
  - LED short-circuit detection
  - Single-LED short-circuit diagnostic
  - Programmable low-supply detection
  - Open-drain $\overline{\text{ERR}}$ for fault indication
  - Watchdog and CRC for FlexWire interface
  - 8-bit ADC for pin voltage measurement
  - Overtemperature protection

2 Applications

- Automotive exterior rear light
- Automotive exterior headlight
- Automotive interior ambient light
- Automotive cluster display

3 Description

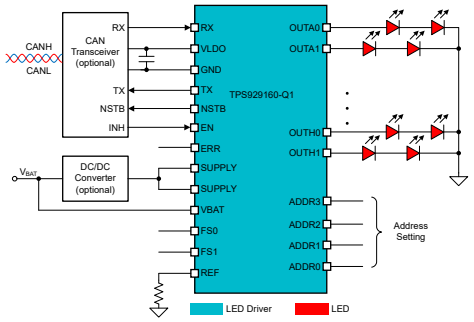
With the increasing demand for animation in automotive lighting, LEDs must be controlled independently. Therefore, LED drivers with digital interfaces are essential to effectively drive pixel-controlled lighting applications. In exterior lighting, multiple lamp functions are typically located on different PCB boards with off-board wires connected to each other. It is difficult for a traditional single-ended interface to meet the strict EMC requirements. By using an industrial-standard CAN physical layer, the UART-based FlexWire interface of the TPS929160-Q1 easily accomplishes long distance off-board communication without impacting EMC.

The TPS929160-Q1 is a 16-channel, 40V high-side LED driver that controls the 8-bit output current and 12-bit PWM duty cycles. The device meets multiple regulation requirements with LED open-circuit, short-to-ground, and single LED short-circuit diagnostics. A configurable watchdog also automatically sets FAIL-SAFE states when the MCU connection is lost, and, with programmable EEPROM, TPS929160-Q1 can flexibly be set for different application scenarios.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS929160-Q1	DCP (HTSSOP, 38)	9.70mm × 4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Diagram

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4 Pin Configuration and Functions

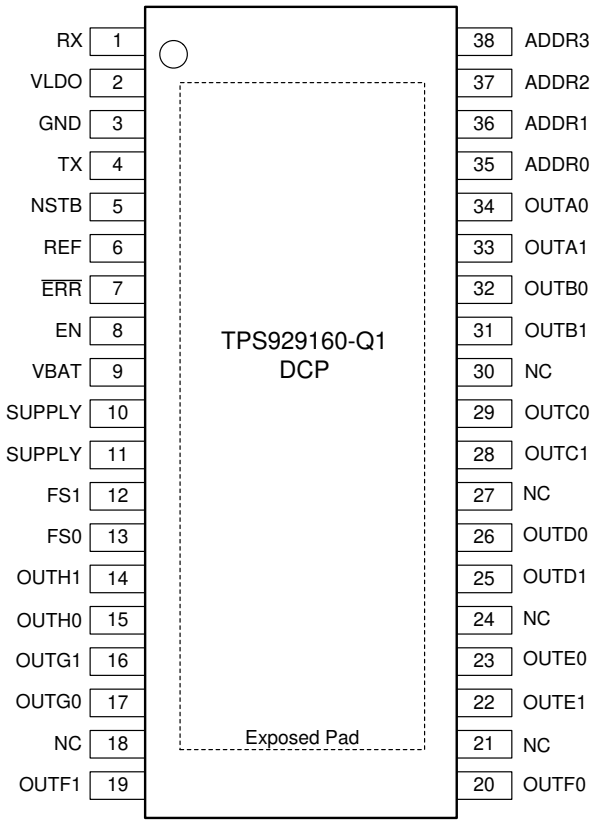


Figure 4-1. DCP Package 38-Pin HTSSOP with PowerPAD™ Integrated Circuit Package Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	RX	I	FlexWire RX
2	VLDO	Power	5V regulator output
3	GND	–	Ground
4	TX	O	FlexWire TX
5	NSTB	O	FlexWire NSTB Output
6	REF	I/O	Device current reference setting
7	$\overline{\text{ERR}}$	I/O	Open-drain error indication
8	EN	I	Device Enable Pin
9	VBAT	Power	Power supply for analog and digital circuit
10	SUPPLY	Power	Power supply for current output channels
11	SUPPLY	Power	Power supply for current output channels
12	FS1	I	Fail-safe input 1
13	FS0	I	Fail-safe input 0
14	OUTH1	O	Current output channel H1
15	OUTH0	O	Current output channel H0
16	OUTG1	O	Current output channel G1
17	OUTG0	O	Current output channel G0
18	NC	–	No Connection
19	OUTF1	O	Current output channel F1
20	OUTF0	O	Current output channel F0
21	NC	–	No Connection
22	OUTE1	O	Current output channel E1
23	OUTE0	O	Current output channel E0
24	NC	–	No Connection
25	OUTD1	O	Current output channel D1
26	OUTD0	O	Current output channel D0
27	NC	–	No Connection
28	OUTC1	O	Current output channel C1
29	OUTC0	O	Current output channel C0
30	NC	–	No Connection
31	OUTB1	O	Current output channel B1
32	OUTB0	O	Current output channel B0
33	OUTA1	O	Current output channel A1
34	OUTA0	O	Current output channel A0
35	ADDR0	I	Device address setting (Bit0)
36	ADDR1	I	Device address setting (Bit1)
37	ADDR2	I	Device address setting (Bit2)
38	ADDR3	I	Device address setting (Bit3)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
SUPPLY, VBAT	Device supply voltage	–0.3	45	V
FS0, FS1, EN	High-voltage input	–0.3	$V_{(VBAT)}$ + 0.3	V
OUTXn	High-voltage outputs	–0.3	$V_{(SUPPLY)}$ + 0.3	V
$\overline{ERR}$	High-voltage output	–0.3	22	V
ADDR3, ADDR2, ADDR1, ADDR0, REF, RX	Low-voltage input	–0.3	5.5	V
VLDO, TX, NSTB	Low-voltage output	–0.3	5.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD classification level 1C		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins (RX, ADDR3, OUTF0, OUTF1)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VBAT	Device supply voltage	4.5		40	V
SUPPLY	Power supply for output current channel	4		36	V
IOUTXn	Channel output current	0.5		100	mA
FS0, FS1	External fail-safe selection input	0		$V_{(BAT)}$	V
TX	FlexWire TX output	0		5	V
RX	FlexWire RX input	0		5	V
VLDO	Internal 5-V LDO output	0		5	V
$I_{(VLDO)}$	LDO external current load	0		80	mA
ADDR3, ADDR2, ADDR1, ADDR0	Device address selection	0		5	V
REF	Current reference setting	0		5	V
$\overline{ERR}$	Error feedback open-drain output	0		20	V
$t_{(r\_RX)}$	RX risetime			$5\%/f_{CLK}$	
$t_{(f\_RX)}$	RX falltime			$5\%/f_{CLK}$	
f_{CLK}	FlexWire frequency	10		1000	kHz
D_{SYNC}	Synchronization pulse dutycycle	45	50	55	%
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS929160-Q1 HTSSOP (DCP) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

T_J = –40°C to 150°C, $V_{(VBAT)}$ = 4.5-40 V, $V_{(SUPPLY)}$ = 4-36 V, for digital outputs, $C_{(LOAD)}$ = 20 pF, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS						
$V_{(VBAT)}$	Operating input voltage		4.5	12	40	V
$I_{SD(VBAT)}$	Shutdown current, VBAT pin	$V_{(VBAT)}$ = 12V, EN = L		5	10	µA
$I_{Q(VBAT)}$	Quiescent current, all-channels-off, VBAT pin	$V_{(VBAT)}$ = 12V, EN = H, $R_{(REF)}$ = 8.45kΩ, REFRANGE = 11b, all-output OFF		1.6	2.0	mA
	Quiescent current, all-channels-on, VBAT pin	$V_{(VBAT)}$ = 12V, EN = H, $R_{(REF)}$ = 8.45kΩ, REFRANGE = 11b, PWMOUTXn = 0, all-output ON		2.8	4.0	mA
$I_{Q(SUPPLY)}$	Quiescent current, all-channels-off, SUPPLY pin	$V_{(VBAT)}$ = 12V, $V_{(SUPPLY)}$ = 12V, EN = H, $R_{(REF)}$ = 8.45kΩ, REFRANGE = 11b, all-output OFF		4.9	10	µA
	Quiescent current, all-channels-on, SUPPLY pin	$V_{(VBAT)}$ = 12V, $V_{(SUPPLY)}$ = 12V, EN = H, $R_{(REF)}$ = 8.45kΩ, REFRANGE = 11b, PWMOUTXn = 0, all-output ON		5.2	8.0	mA
$I_{FAULT(VBAT)}$	Quiescent current, fail-safe state fault mode, VBAT pin	$V_{(VBAT)}$ = 12V, $V_{(SUPPLY)}$ = 12V, fail-safe state, all-output OFF, $\overline{ERR}$ = LOW		1.3	2.0	mA
$I_{FAULT(SUPPLY)}$	Quiescent current, fail-safe state fault mode, SUPPLY pin	$V_{(VBAT)}$ = 12V, $V_{(SUPPLY)}$ = 12V, fail-safe state, all-output OFF, $\overline{ERR}$ = LOW		5	10	µA
$I_{LKG(SUPPLY)}$	Supply leakage current	$V_{(SUPPLY)}$ = 36V, EN = L		0.08	5	µA
$V_{(POR\_rising)}$	Power-on-reset rising threshold		4	4.2	4.4	V
$V_{(POR\_falling)}$	Power-on-reset falling threshold		3.8	4	4.2	V
$V_{(LDO)}$	LDO output voltage	$V_{(VBAT)}$ > 5.6V, $I_{(LDO)}$ = 80mA	4.75	5	5.25	V
$I_{(LDO)}$	LDO output current capability				80	mA
$I_{(LDO\_LIMIT)}$	LDO output current limit		110			mA
$V_{(LDO\_DROP)}$	LDO maximum dropout voltage	$I_{(LDO)}$ = 80mA		0.5	0.9	V
$V_{(LDO\_DROP)}$	LDO maximum dropout voltage	$I_{(LDO)}$ = 50mA		0.3	0.6	V
$V_{(LDO\_POR\_rising)}$	LDO power-on-reset rising threshold		2.75	3.00	3.25	V
$V_{(LDO\_POR\_falling)}$	LDO power-on-reset falling threshold		2.5	2.75	3	V
$C_{(LDO)}$	Supported LDO loading capacitance range		1		10	µF
$f_{(OSC)}$	Internal oscillator frequency		-2.5%	32.15	+2.5%	MHz
ERR, NSTB						
$V_{IL(\overline{ERR})}$	Input logic low voltage, $\overline{ERR}$		1.045	1.1	1.155	V
$V_{IH(\overline{ERR})}$	Input logic high voltage, $\overline{ERR}$		1.14	1.2	1.26	V
$I_{PD(\overline{ERR})}$	$\overline{ERR}$ pull-down current capability	$V_{(\overline{ERR})}$ = 0.4V	3	5	9	mA
$I_{LKG(\overline{ERR})}$	$\overline{ERR}$ leakage current			0.02	1	µA
$\Delta V_{(NSTB)}$	High level voltage drop NSTB with respect to $V_{(LDO)}$	$I_{(NSTB)}$ = 1mA		40	100	mV
$R_{PD(NSTB)}$	NSTB pull-down resistor			1	2	MΩ
$I_{LKG(NSTB)}$	NSTB leakage current	$V_{(NSTB)}$ = 0V	-4		4	µA
FLEXWIRE INTERFACE						
$V_{IL(RX)}$	Input logic low voltage, RX				0.7	V
$V_{IH(RX)}$	Input logic high voltage, RX		2			V
$V_{OL(TX)}$	Low-level output voltage, TX	I_{sink} = 5mA,	0	0.04	0.3	V
$V_{OH(TX)}$	High-level output voltage, TX	I_{source} = 5mA, $V_{pull-up}$ = 5V	4.7	4.9	5.0	V
I_{lkg}	TX, RX		–1		1	µA

T_J = –40°C to 150°C, $V_{(VBAT)}$ = 4.5-40 V, $V_{(SUPPLY)}$ = 4-36 V, for digital outputs, $C_{(LOAD)}$ = 20 pF, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN, ADDRESS, FS						
$V_{IL(ADDR)}$	Input logic low voltage, EN, ADDR3, ADDR2, ADDR1, ADDR0				0.7	V
$V_{IH(ADDR)}$	Input logic high voltage, EN, ADDR3, ADDR2, ADDR1, ADDR0		2			V
$V_{IL(IO)}$	Input logic low voltage FS1, FS0		1.045	1.1	1.155	V
$V_{IH(IO)}$	Input logic high voltage, FS1, FS0		1.14	1.2	1.26	V
$R_{PD(ADDR)}$	Internal pull down resistance, ADDR3, ADDR2, ADDR1, ADDR0		200	240	300	kΩ
ADC						
DNL	Differential nonlinearity		–1(1)		1(1)	LSB
INL	Integral nonlinearity		–2(1)		2(1)	LSB
OUTPUT DRIVERS						
$f_{(PWM\_200)}$		200Hz selection		200		Hz
$f_{(PWM\_1000)}$		1kHz selection		1000		Hz
$\Delta I_{(OUT\_d2d)}$	Device-to-device accuracy $\Delta I_{(OUT\_d2d)}$ = 1- $I_{avg(OUT)}$ / $I_{ideal(OUT)}$	$R_{(REF)}$ = 8.45kOhm, REFRANGE = 11b, DC = 63	–5	0	5	%
		$R_{(REF)}$ = 8.45kΩ, REFRANGE = 10b, DC = 63	–5	0	5	
		$R_{(REF)}$ = 8.45kΩ, REFRANGE = 01b, DC = 63	–5	0	5	
		$R_{(REF)}$ = 8.45kΩ, REFRANGE = 00b, DC = 63	–5	0	5	
$\Delta I_{(OUT\_c2c)}$	Channel-to-channel accuracy $\Delta I_{(OUT\_c2c)}$ = 1- $I_{(OUTx)}$ / $I_{avg(OUT)}$	$R_{(REF)}$ = 8.45kΩ, REFRANGE = 11b, DC = 63	–3	0	3	%
		$R_{(REF)}$ = 8.45kΩ, REFRANGE = 10b, DC = 31	–3	0	3	
		$R_{(REF)}$ = 8.45kΩ, REFRANGE = 01b, DC = 15	–5	0	5	
		$R_{(REF)}$ = 31.6kΩ, REFRANGE = 01b, DC = 12	–7	0	7	
$I_{(OUT\_100mA)}$		$R_{(REF)}$ = 6.34kΩ, REFRANGE = 11b, DC = 63		100		mA
$I_{(OUT\_75mA)}$		$R_{(REF)}$ = 8.45kΩ, REFRANGE = 11b, DC = 63		75		mA
$I_{(OUT\_50mA)}$		$R_{(REF)}$ = 12.7kΩ, REFRANGE = 11b, DC = 63		50		mA
$I_{(OUT\_20mA)}$		$R_{(REF)}$ = 31.6kΩ, REFRANGE = 11b, DC = 63		20		mA
$I_{(OUT\_1mA)}$		$R_{(REF)}$ = 31.6kΩ, REFRANGE = 01b, DC = 12		1		mA
$V_{(OUT\_drop)}$	Output dropout voltage	$R_{(REF)}$ = 8.45kΩ, REFRANGE = 11b, DC = 38, $I_{(OUTx)}$ = 45mA		450	700	mV
		$R_{(REF)}$ = 8.45kΩ, REFRANGE = 11b, DC = 63, $I_{(OUTx)}$ = 75mA		600	1000	mV
		$R_{(REF)}$ = 6.34kΩ, REFRANGE = 11b, DC = 63, $I_{(OUTx)}$ = 100mA		750	1200	mV
$R_{(REF)}$			1		50	kΩ
$C_{(REF)}$			0		4.7	nF
$V_{(REF)}$			1.228	1.235	1.242	V
$K_{(REF\_11)}$		REFRANGE = 11b		512		

T_J = –40°C to 150°C, $V_{(VBAT)}$ = 4.5-40 V, $V_{(SUPPLY)}$ = 4-36 V, for digital outputs, $C_{(LOAD)}$ = 20 pF, (unless otherwise noted).

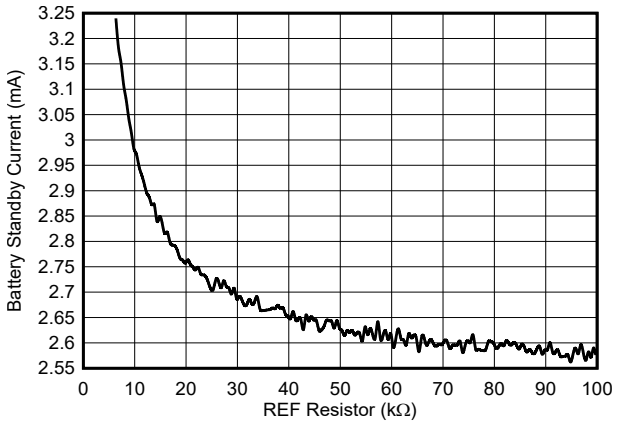
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$K_{(REF\_10)}$		REFRANGE = 10b		256		
$K_{(REF\_01)}$		REFRANGE = 01b		128		
$K_{(REF\_00)}$		REFRANGE = 00b		64		
$I_{(REF\_OPEN\_th)}$			7	8.5	10	µA
$I_{(REF\_OPEN\_th\_hyst)}$				4		uA
$V_{(REF\_SHORT\_th)}$			0.54	0.565	0.59	V
DIAGNOSTICS						
$V_{(SUPUV\_th\_rising)}$	SUPPLY undervoltage rising threshold		2.73	2.875	3.02	V
$V_{(SUPUV\_th\_falling)}$	SUPPLY undervoltage falling threshold		2.49	2.625	2.76	V
$V_{(SUPUV\_th\_hyst)}$	SUPPLY undervoltage hysteresis			250		mV
$V_{(SUPLOW\_th\_rising)}$	SUPPLY low rising threshold, LOWSUPTH = 0		4.05	4.25	4.45	V
$V_{(SUPLOW\_th\_falling)}$	SUPPLY low falling threshold, LOWSUPTH = 0		3.8	4.0	4.2	V
$V_{(SUPLOW\_th\_hyst)}$	SUPPLY low hysteresis, LOWSUPTH = 0			250		mV
$V_{(OPEN\_th\_rising)}$	LED open rising threshold	$V_{(SUPPLY)}$ - $V_{(OUTx)}$	200	400	600	mV
$V_{(OPEN\_th\_falling)}$	LED open falling threshold	$V_{(SUPPLY)}$ - $V_{(OUTx)}$	300	500	700	mV
$V_{(OPEN\_th\_hyst)}$				100		mV
$V_{(SG\_th\_rising)}$	Short-to-ground rising threshold		0.8	0.9	1	V
$V_{(SG\_th\_falling)}$	Short-to-ground falling threshold		1.1	1.2	1.3	V
$V_{(SG\_th\_hyst)}$	Short-to-ground hysteresis			0.3		V
$V_{(SLS\_th\_rising)}$	Single-LED short rising threshold, SLSTHx = 0		2.35	2.5	2.65	V
$V_{(SLS\_th\_falling)}$	Single-LED short falling threshold, SLSTHx = 0		2.65	2.85	3.05	V
$V_{(SLS\_th\_hyst)}$	Single-LED short hysteresis, SLSTHx = 0			275		mV
EEPROM						
$N_{(EEP)}$	Number of programming cycles	$V_{(VBAT)}$ = 12V	1000			
TEMPERATURE						
$T_{(PRETSD)}$	Pre-thermal warning threshold			135		ºC
$T_{(PRETSD\_HYS)}$	Pre-thermal warning hysteresis			5		ºC
$T_{(TSD1)}$	Over-temperature protection threshold		160	175	190	ºC
$T_{(TSD2)}$	Over-temperature shutdown threshold			185		ºC
$T_{(TSD1\_HYS)}$	Over-temperature protection hysteresis			15		ºC
$T_{(TSD2\_HYS)}$	Over-temperature shutdown hysteresis			15		ºC

(1) Specified by design only

5.6 Timing Requirements

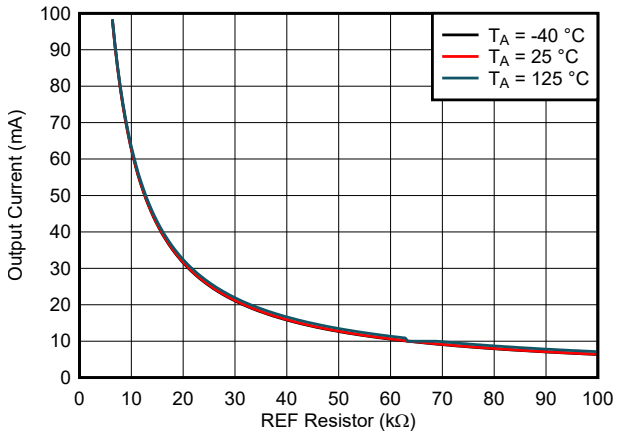
		MIN	NOM	MAX	UNIT
$t_{(BLANK)}$	Diagnostics pulse-width, BLANK = 0h		100		µs
$t_{(SUPLOW\_deg)}$	Low supply deglitch timer		96		µs
$t_{(SUPUV\_deg)}$	Supply undervoltage deglitch timer		96		µs
$t_{(CONV)}$	time needed to complete one AD conversion		57		µs
$t_{(OPEN\_deg)}$	Open-circuit deglitch timer		8		µs
$t_{(SHORT\_deg)}$	Short-circuit deglitch timer		8		µs
$t_{(SLS\_deg)}$	Single-LED short-circuit deglitch timer		8		µs
$t_{(SLS\_retry)}$	Fault retry timer		10		ms

5.7 Typical Characteristics



REFRANGE = 11b
PWMOUTXn=0, all-output ON

Figure 5-1. Standby Current vs REF Resistor



REFRANGE = 11b
IOUTXn[5:0]=3Fh

Figure 5-2. Output Current vs REF Resistor

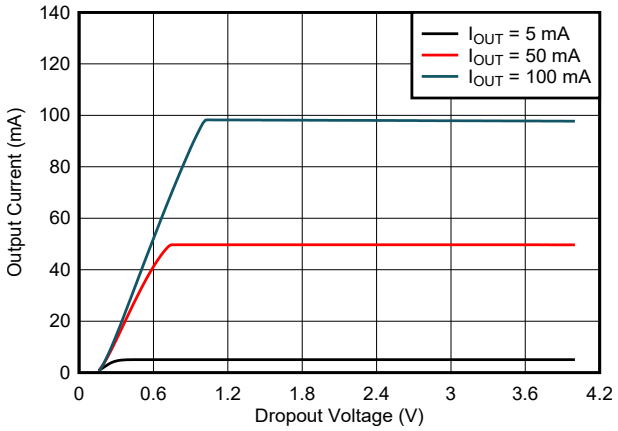


Figure 5-3. Output Current vs Dropout Voltage

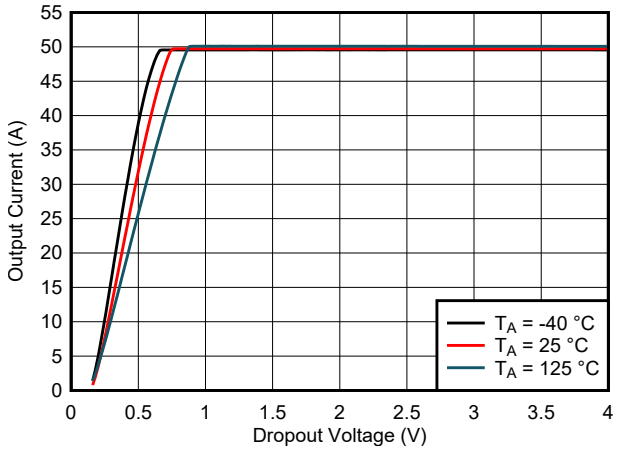


Figure 5-4. Output Current vs Dropout Voltage

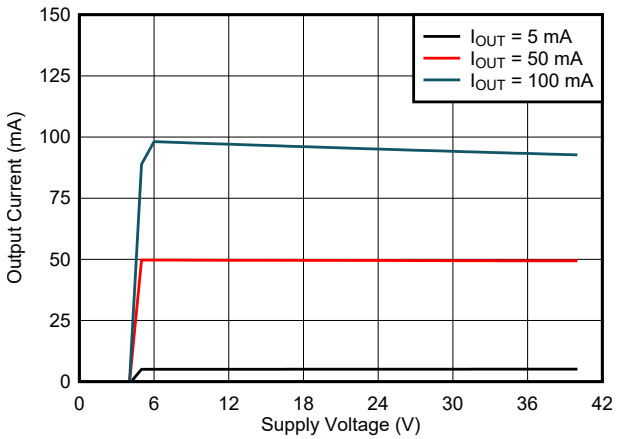


Figure 5-5. Output Current vs Supply Voltage

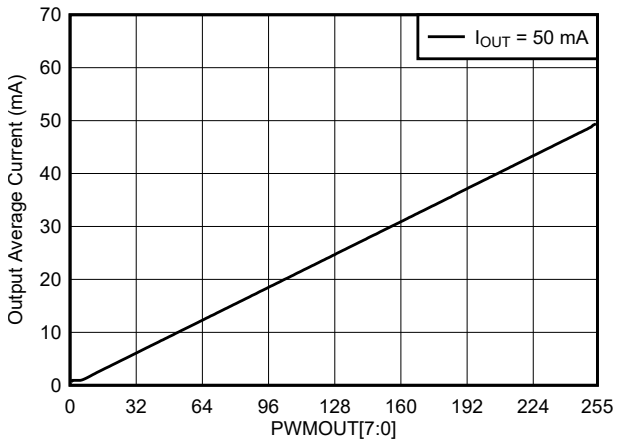


Figure 5-6. Average Current vs PWMOUT[7:0]

5.7 Typical Characteristics (continued)

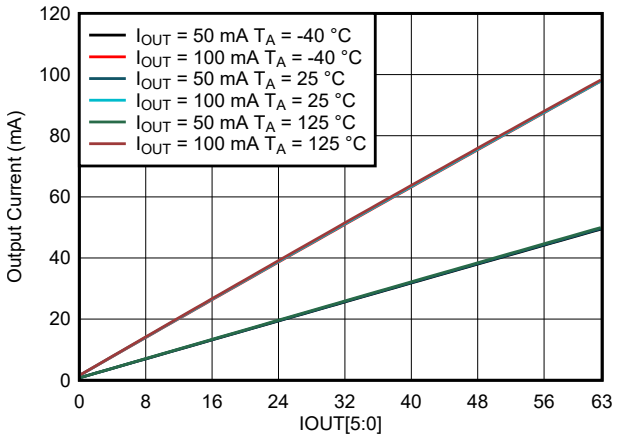


Figure 5-7. Output DC Current vs IOUT[5:0]

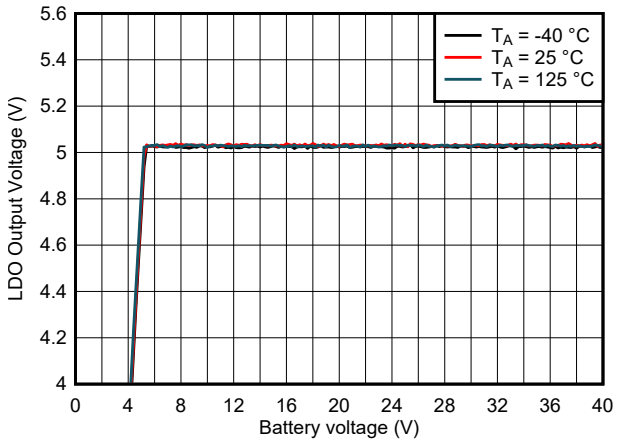


Figure 5-8. LDO Output Line Regulation

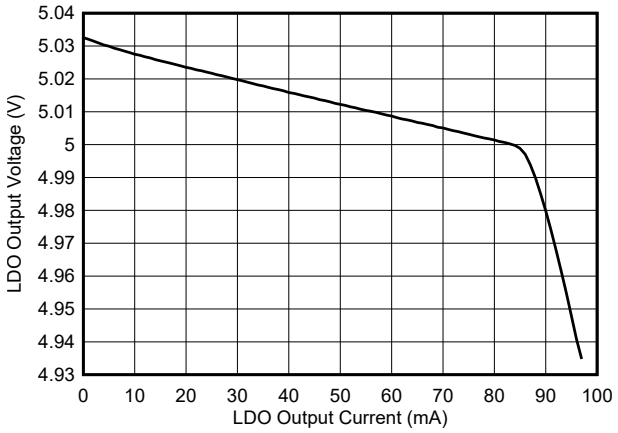


Figure 5-9. LDO Output Load Regulation

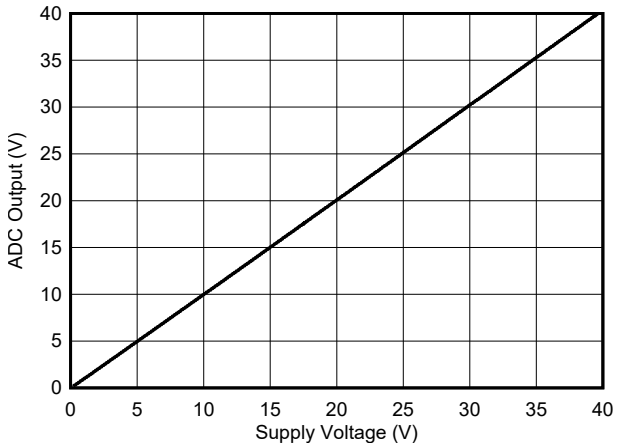


Figure 5-10. ADC Sampling Result vs Sampled Supply Voltage

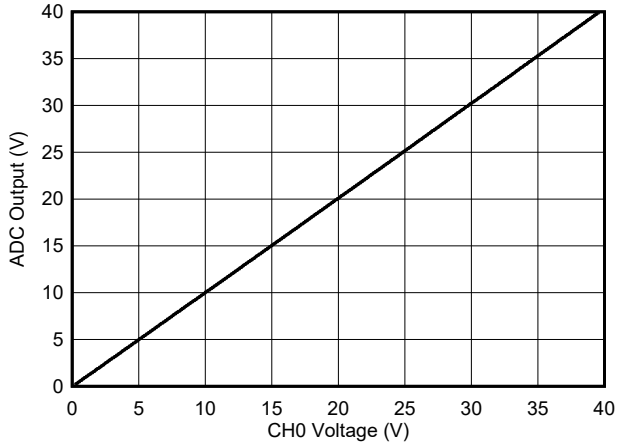
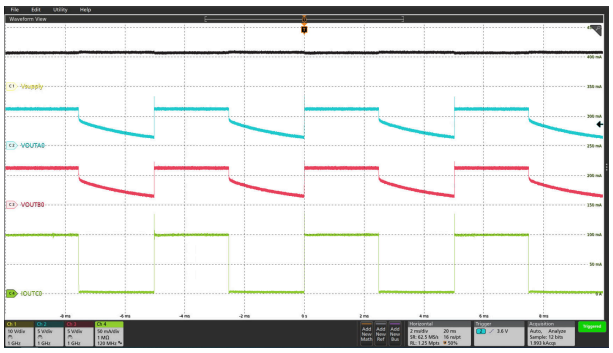


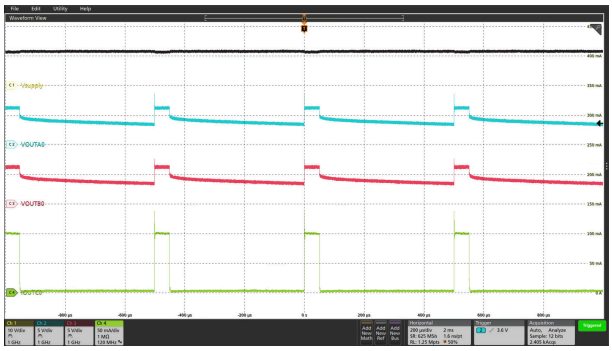
Figure 5-11. ADC Sampling Result vs Sampled Channel Voltage

5.7 Typical Characteristics (continued)



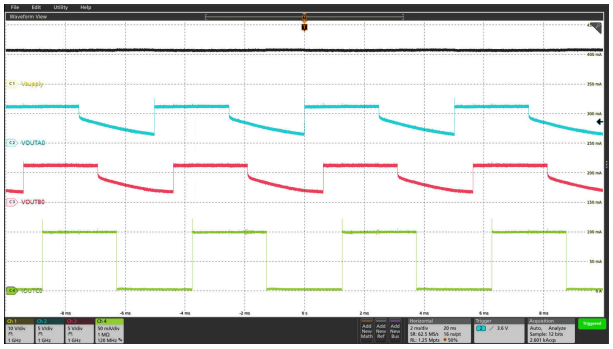
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUTA0)}$ Ch3 = $V_{(OUTB0)}$
Ch4 = $I_{(OUTC0)}$

Figure 5-12. PWM Dimming at 200Hz



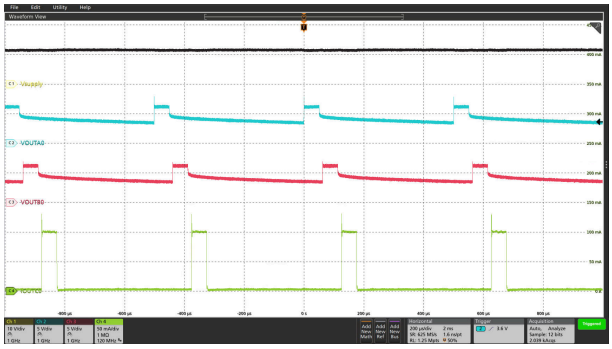
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUTA0)}$ Ch3 = $V_{(OUTB0)}$
Ch4 = $I_{(OUTC0)}$

Figure 5-13. PWM Dimming at 2000Hz



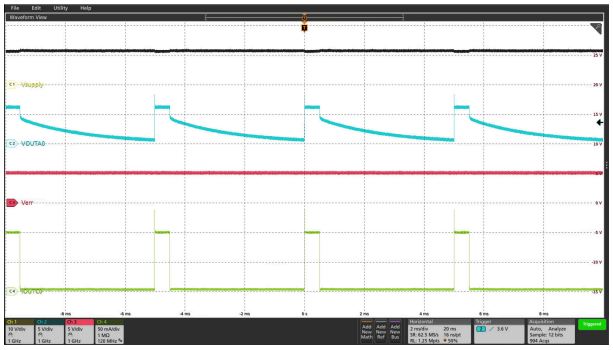
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUTA0)}$ Ch3 = $V_{(OUTB0)}$
Ch4 = $I_{(OUTC0)}$

Figure 5-14. Phase Shift PWM Dimming at 200Hz



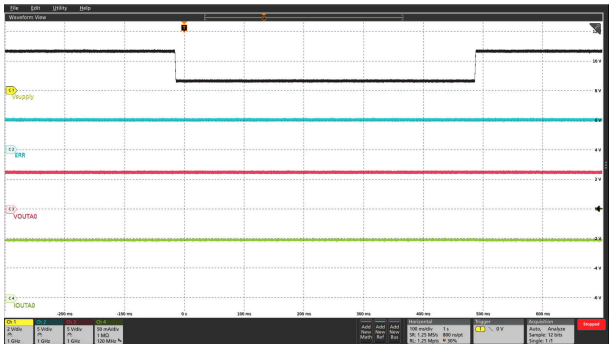
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUTA0)}$ Ch3 = $V_{(OUTB0)}$
Ch4 = $I_{(OUTC0)}$

Figure 5-15. Phase Shift PWM Dimming at 2000Hz



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUTA0)}$ Ch3 = $V_{(\overline{ERR})}$
Ch4 = $I_{(OUTC0)}$

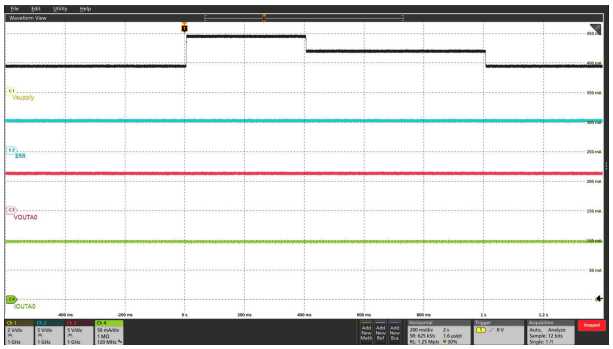
Figure 5-16. Supply Dimming in FAIL-SAFE Mode at 200Hz



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

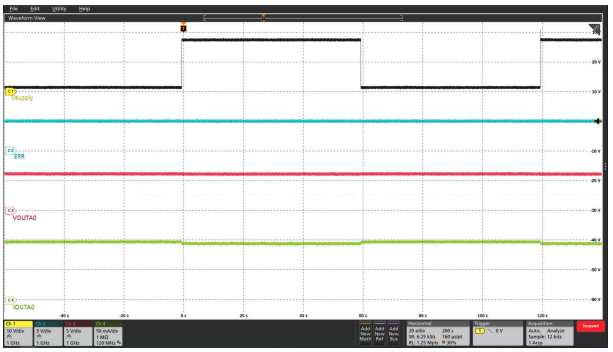
Figure 5-17. Transient Undervoltage

5.7 Typical Characteristics (continued)



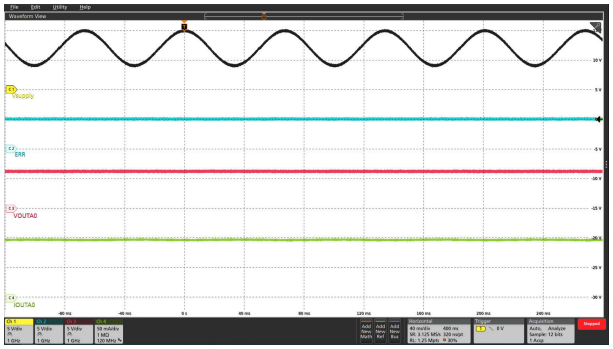
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-18. Transient Overvoltage



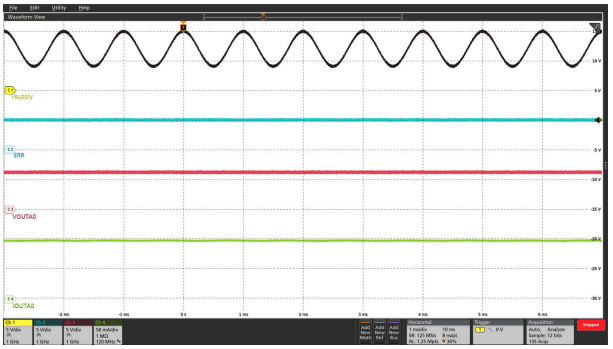
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-19. Jump Start



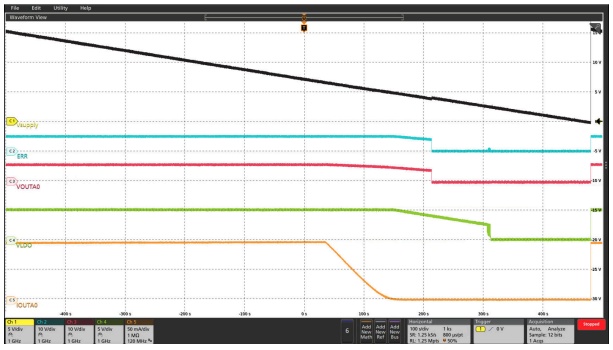
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-20. Superimposed Alternating Voltage 15Hz



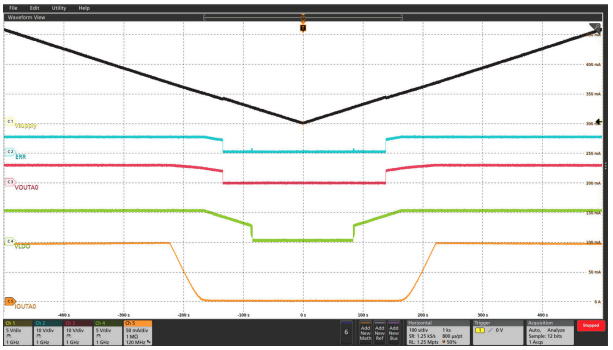
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-21. Superimposed Alternating Voltage 1 kHz



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $V_{(LDO)}$ Ch5 = $I_{(OUTA0)}$

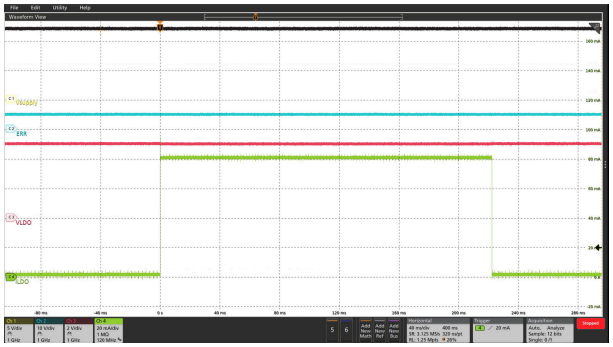
Figure 5-22. Slow Decrease and Quick Increase of Supply Voltage



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $V_{(LDO)}$ Ch5 = $I_{(OUTA0)}$

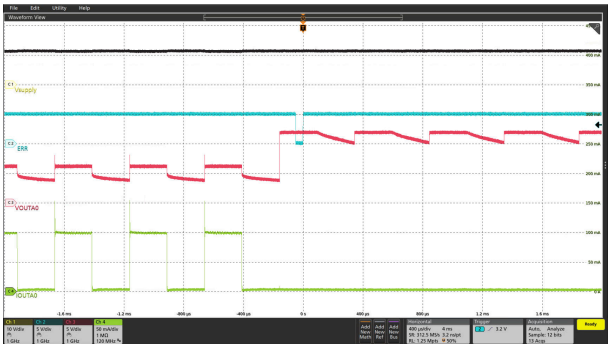
Figure 5-23. Slow Decrease and Slow Increase of Supply Voltage

5.7 Typical Characteristics (continued)



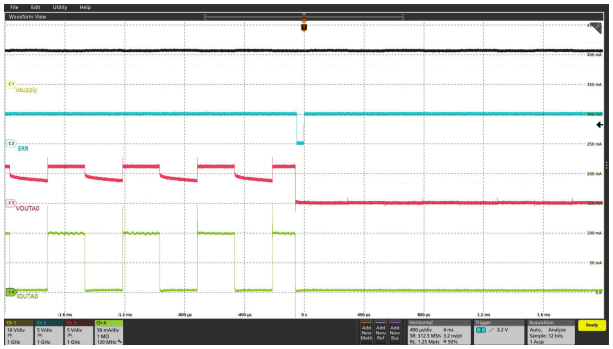
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(LDO)}$
Ch4 = $I_{(LDO)}$

Figure 5-24. LDO Output Load Transient



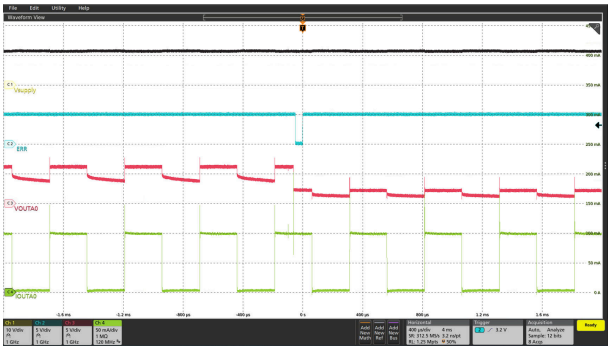
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-25. LED Open-Circuit Detection in Normal Mode



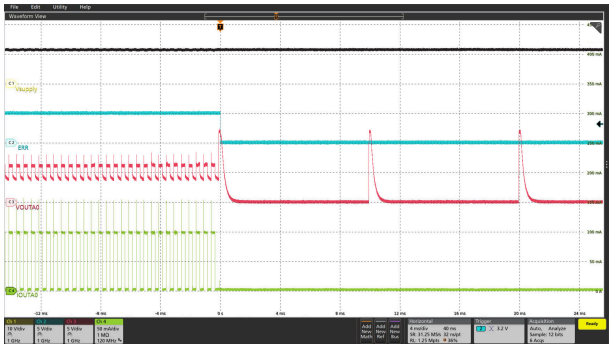
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-26. LED Short-Circuit Detection in Normal Mode



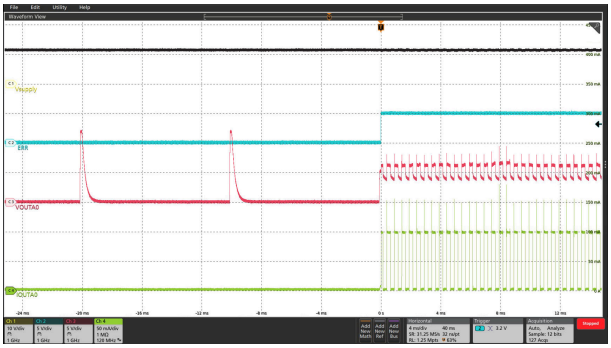
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-27. Single-LED Short-Circuit Detection in Normal Mode



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

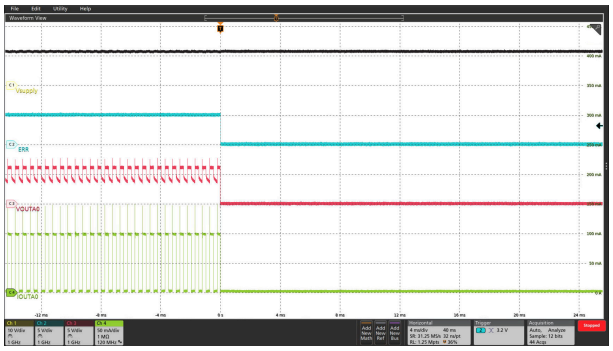
Figure 5-28. LED Open-Circuit Detection in FS Mode



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

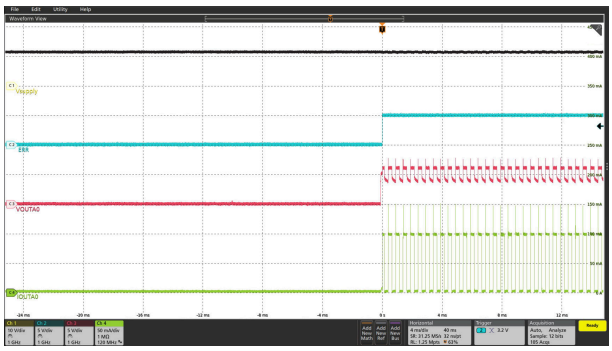
Figure 5-29. LED Open-Circuit Recovery in FS Mode

5.7 Typical Characteristics (continued)



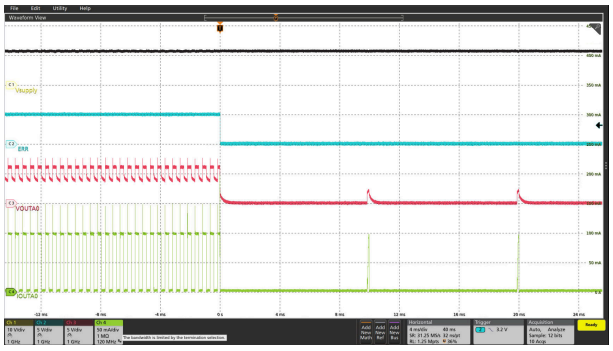
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-30. LED Short-Circuit Detection in Fail-Safe Mode



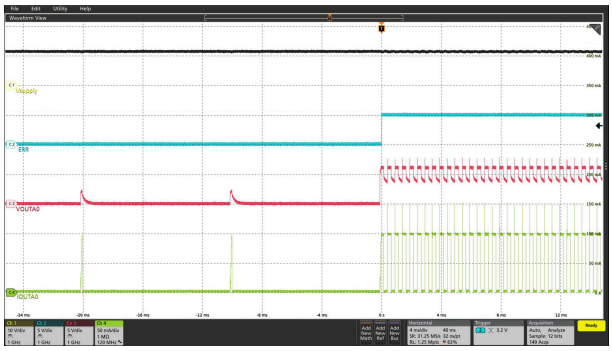
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-31. LED Short-Circuit Recovery in Fail-Safe Mode



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-32. Single-LED Short-Circuit Detection in Fail-Safe Mode



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(\overline{ERR})}$ Ch3 = $V_{(OUTA0)}$
Ch4 = $I_{(OUTA0)}$

Figure 5-33. Single-LED Short-Circuit Recovery in Fail-Safe Mode

6 Detailed Description

6.1 Overview

TPS929160-Q1 is an automotive, 16-channel LED driver with FlexWire interface to address increasing requirements for individual control of each LED string. Each of the device channels can support both analog dimming and pulse-width-modulation (PWM) dimming, configured through its FlexWire serial interface. The internal electrically erasable programmable read-only memory (EEPROM) allows users to configure device in the scenario of communication loss to fulfill system level safety requirements.

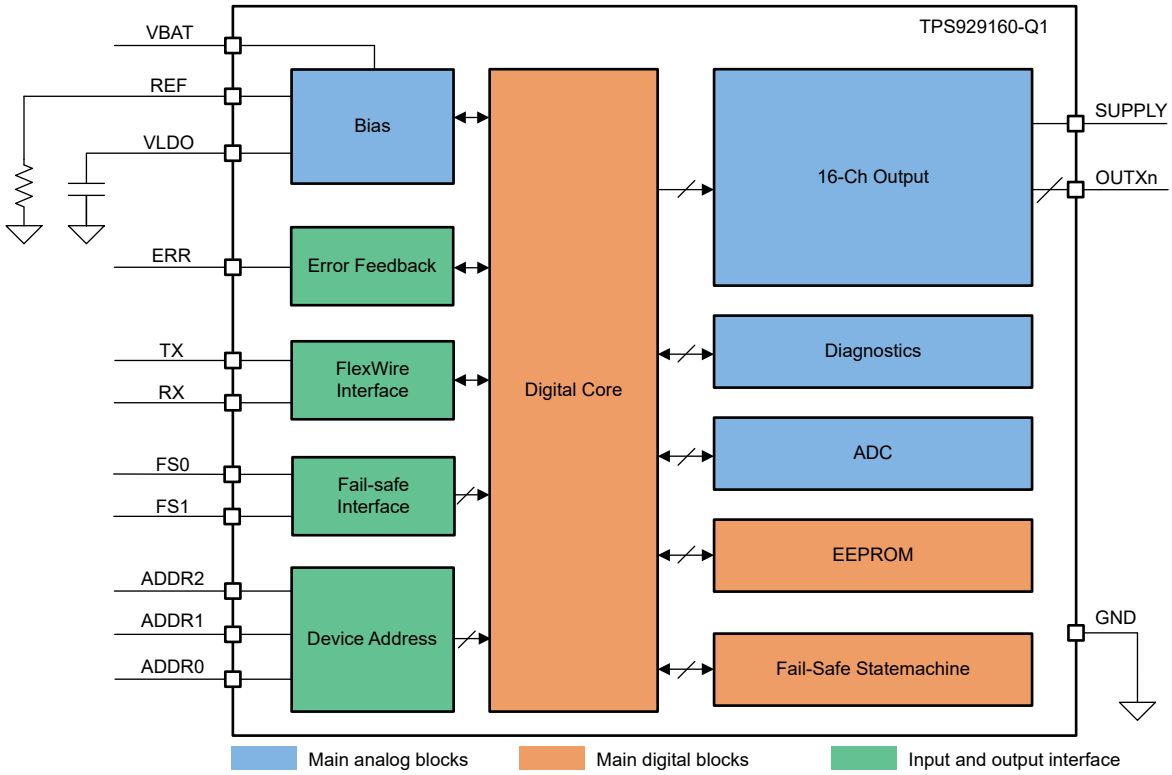
The FlexWire interface is a robust address-based master-slave interface with flexible baud rate. The interface is based on multi-frame universal, asynchronous, receiver-transmitter (UART) protocol. The unique synchronization frame of FlexWire reduces system cost by saving external crystal oscillators. It also supports various physical layer with the help of external physical layer transceiver such as CAN or LIN transceivers. The embedded CRC correction is able to ensure robust communication in automotive environments. The FlexWire interface is easily supported by most of MCUs in the markets.

Each output is a constant current source with individually programmable current output and PWM duty cycle. PWM phase shift is supported for the output channels to improve the EMC performance and reduce the output noise. Each channel features various diagnostics including LED open-circuit, short-circuit and single-LED short-circuit detection. The on-chip analog-digital convertor (ADC) allows the controller to real-time monitor loading conditions.

To further increase robustness, the unique fail-safe of the device state machine allows automatic switching to FAIL-SAFE states in the case of communication loss, for example, MCU failure. The device supports programming fail-safe settings with user-programmable EEPROM. In FAIL-SAFE states, the device supports different configurations if output fails, such as one-fails-all-fail or one-fails-others-on. Each channel can be independently programmed as on or off in FAIL-SAFE states. The FAIL-SAFE state machine also allows the system to function with pre-programmed EEPROM settings without presence of any controller in the system, also known as stand-alone operation.

The microcontroller can access each of the devices through the FlexWire interface. By setting and reading back the registers, the master, which is the microcontroller, has full control over the device and LEDs. All EEPROMs are pre-programmed to default values. TI recommends that users program the EEPROM at the end-of-line for application-specific settings and FAIL-SAFE configurations.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Device Bias and Power

6.3.1.1 Power Bias (VBAT)

The TPS929160-Q1 is AEC-Q100 qualified for automotive applications. The bias voltage input to the device through VBAT pin can be low to 4.5V and up to 40V for automotive battery directly powered systems. All the internal analog and digital circuits except for the current output channels are powered by VBAT.

6.3.1.2 Enable and Shutdown (EN)

The TPS929160-Q1 device has an enable input. When EN is low, the device is in sleep mode with ultra low quiescent current $I_{(SD)}$. This low current helps to save system-level current consumption in applications where battery voltage directly connects to the device without high-side switches.

When the EN voltage rises above $V_{IL(EN)}$ and $V_{(VBAT)}$ is above $V_{(POR\_rising)}$, the TPS929160-Q1 immediately starts up the internal voltage regulator to provide a stable VLDO, 5V bias to internal analog and digital circuit. When the EN voltage falls below $V_{IL(EN)}$ and $V_{(VBAT)}$ is above $V_{(POR\_rising)}$, the TPS929160-Q1 shuts down all current output immediately.

6.3.1.3 5V Low-Drop-Out Linear Regulator (VLDO)

The TPS929160-Q1 has an integrated low-drop-out linear regulator to provide power supply to external CAN transceivers, such as TCAN1042-Q1. The internal LDO powered by input voltage $V_{(VBAT)}$ provides a stable 5-V output with up to 80mA constant current capability. TI recommends a ceramic capacitor from 1µF to 10µF on the VLDO pin. The LDO has an internal current limit $I_{(LDO\_LIMIT)}$ for protection and soft start. The capacitor charging time must be considered to total start-up time period, because the device is held in POR state if the capacitor voltage is not charged to above UVLO threshold.

6.3.1.4 Undervoltage Lockout (UVLO) and Power-On-Reset (POR)

To ensure clean start-up, the TPS929160-Q1 uses UVLO and POR circuitry to clear its internal registers upon power up and to reset registers with its default values.

The TPS929160-Q1 has internal UVLO circuits so that when either input voltage $V_{(VBAT)}$ or LDO output voltage $V_{(LDO)}$ is lower than its UVLO threshold, POR is triggered. In POR state, the device resets digital core and all registers to default value. FLAG_POR and FLAG_ERR register are set to 1 for each POR cycle to indicate the POR history.

Before both powers are above UVLO thresholds, the TPS929160-Q1 stays in POR state with all outputs off and $\overline{ERR}$ pulled down. Once both power supplies are above UVLO threshold, the device enters INIT mode for initialization releasing $\overline{ERR}$ pulldown. A programmable timer starts counting in INIT state, the timer length can be set by EEPROM register INITTIMER. When the timer is completed, the device switches to NORMAL state. In INIT state, setting CLRPOR to 1 clears FLAG_POR, disables the timer, and sets the device to NORMAL state.

Upon powering up, the TPS929160-Q1 automatically loads all settings stored in EEPROM to correlated registers and sets the other registers to default value which don't have correlated EEPROM. All channels are powered up in OFF state by default to avoid unwanted blinking.

Writing 1 to REGDEFAULT manually loads EEPROM setting to the correlated registers and set the other registers to default value. After REGDEFAULT is set, the FLAG_POR is cleared to 0. Writing 1 to CLRPOR also resets the FLAG_POR register to 0. TI recommends setting REGDEFAULT to 1 to clear the internal registers every time after POR. The REGDEFAULT automatically resets to 0.

6.3.1.5 Power Supply (SUPPLY)

The TPS929160-Q1 has two additional SUPPLY input pins for powering all 16 high-side current output channels. The supply voltage input to the device through two SUPPLY pin can be low to 3.5V and up to 36V for either automotive battery directly powered systems or an external DC-to-DC converter output. An external DC-to-DC converter can provide a regulated voltage for required LED output forward voltage from wide automotive battery voltage range.

The TPS929160-Q1 has an internal undervoltage detection circuit for SUPPLY input. When the SUPPLY input voltage is lower than its undervoltage threshold, $V_{(SUPUV\_th\_falling)}$, all 16 current output channels are disabled with $\overline{ERR}$ pin constantly pulled low and register flags set to 1 including FLAG_ERR bit and FLAG_SUPUV bit. Table 6-6 shows the detailed fault behavior in NORMAL state.

6.3.1.6 Programmable Low Supply Warning

The TPS929160-Q1 uses its internal comparator to monitor supply voltage $V_{(SUPPLY)}$. If the supply is below allowable working threshold, the output voltage can be insufficient to keep the LED operating with desired brightness output as expected. The supply voltage is automatically compared with threshold set by register LOWSUPTH. When the supply voltage is below threshold, the device sets warning flag register FLAG_LOWSUP and FLAG_ERR to 1 in the status register. CLRFAULT is able to clear the FLAG_LOWSUP as well as other fault registers. Low-supply warning will clear LED open and single-LED short fault. In addition, the LED open-circuit and single LED short-circuit detection is disabled if the supply voltage is below threshold to avoid LED open circuit and to prevent the single LED short-circuit fault from being mis-triggered. The 5-bit register LOWSUPTH has a total of 32 options covering from 4V to 35V at 1V interval.

6.3.2 Constant Current Output

6.3.2.1 Reference Current with External Resistor (REF)

The TPS929160-Q1 must have an external resistor $R_{(REF)}$ to set the internal current reference $I_{(REF)}$ as shown in Figure 6-1.

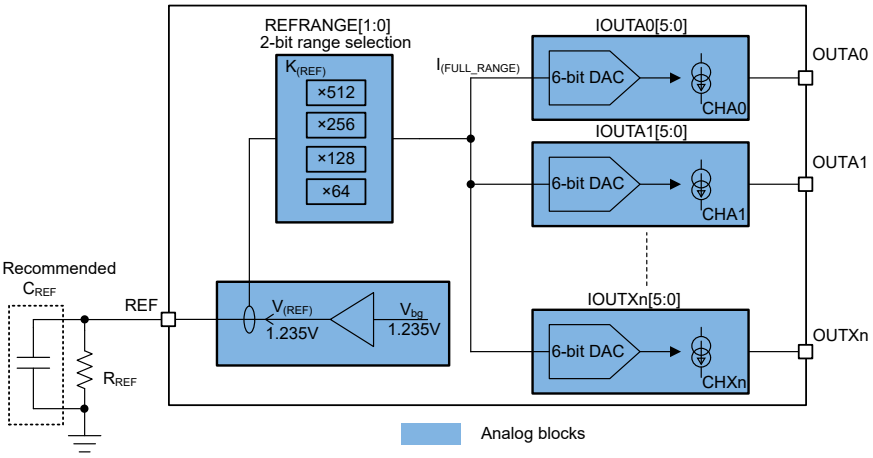


Figure 6-1. Output Current Setting

The internal current reference, $I_{(FULL\_RANGE)}$, is generated based on the $I_{(REF)}$ multiplied by factor $K_{(REF)}$ to provide the full range current reference for each OUTXn channel. The $K_{(REF)}$ is programmable by 2-bit register REFRANGE with four different options. Use the following equation to calculate the $I_{(FULL\_RANGE)}$.

$$I_{(FULL\_RANGE)} = \frac{V_{(REF)}}{R_{(REF)}} \times K_{(REF)} \quad (1)$$

where

- $V_{(REF)}$ = 1.235V typically
- $K_{(REF)}$ = 64, 128, 256, or 512 (default)

The following table lists the recommended resistor values of $R_{(REF)}$ and amplifier ratios of $K_{(REF)}$.

Table 6-1. Reference Current Range Setting

REFRANGE	$K_{(REF)}$	FULL RANGE CURRENT (mA)			
		$R_{(REF)}$ = 6.3kΩ	$R_{(REF)}$ = 8.45kΩ	$R_{(REF)}$ = 12.7kΩ	$R_{(REF)}$ = 31.6kΩ
11b(default)	512	100	75	50	20
10b	256	50	37.5	25	10
01b	128	25	18.75	12.5	5
00b	64	12.5	9.375	6.25	2.5

Place the $R_{(REF)}$ resistor as close as possible to the REF pin with an up to 2.2-nF ceramic capacitor in parallel to improve the noise immunity. The off-board $R_{(REF)}$ setup is not allowed due to the concern of instability reference current. TI recommends a 1-nF ceramic capacitor in parallel with $R_{(REF)}$.

6.3.2.2 64-Step Programmable High-Side Constant-Current Output

TPS929160-Q1 has 16 channels of high-side current sources. Each channel has its own enable configuration register ENOUTXn. Setting ENOUTXn to 1 enables the channel output; clearing the register to 0 disables the channel output. To completely turn off the channel current, the user can clear channel enable bit ENOUTXn to 0. Upon power up, ENOUTXn is automatically reset to 0 to avoid unwanted blinking.

Each OUTXn channel supports individual 64-step programmable current setting, also known as dot correction (DC). The DC feature can be used to set binning values for output LEDs or to calibrate the LEDs to achieve high brightness homogeneity based on external visual system to further save binning cost. The 6-bit register IOUTXn sets the current independently, where X is the channel group from A to H, n is the channel number 0 or 1 in each group. Use the following equation to calculate the OUTXn current.

$$I_{(OUTXn)} = \frac{IOUTXn + 1}{64} \times I_{(FULL\_RANGE)} \quad (2)$$

where

- IOUTXn is programmable from 0 to 63.
- X is from A to H, n is 0 or 1 for different output channel.
- Use Equation 1 to calculate $I_{(FULL\_RANGE)}$.

6.3.3 PWM Dimming

TPS929160-Q1 integrates independent 12-bit PWM generators for each OUTXn channel. The current output for each OUTXn channel is turned on and off controlled by the integrated PWM generator. The average current of each OUTXn can be adjusted by PWM duty cycle independently, therefore, to control the brightness for LEDs in each channel.

6.3.3.1 PWM Generator

The 12-bit PWM generator constructs the cyclical PWM output based on a 12-bit digital binary input to control the output current ON and OFF. Basically the PWM generator counts 4096 pulses at base high frequency for PWM output cycle period and counts number of pulses determined by 12-bit binary input at the same frequency for PWM ON period. The base high frequency is generated by internal oscillator, which is 4096 times of the frequency programmable by PWMFREQ. Figure 6-2 is the signal path diagram for the PWM generator.

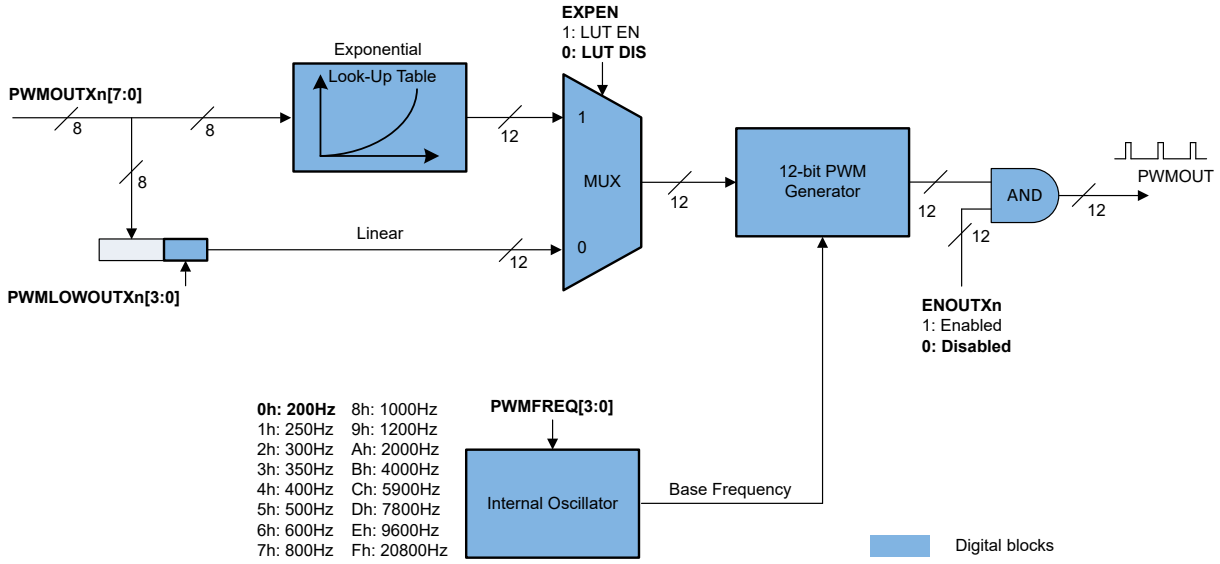


Figure 6-2. PWM Generator Path Diagram

6.3.3.2 PWM Dimming Frequency

The frequency for PWM dimming is programmable by 4-bit register PWMFREQ with 16 options covering from 200Hz to 20.8kHz. Select the frequency for PWM dimming based on the minimum brightness requirement in application. TPS929160-Q1 supports down to 1µs minimum pulse current for all 16 channel outputs.

6.3.3.3 Blank Time

Because the TPS929160-Q1 supports PWM control for adjusting LED brightness, the voltage on OUTXn is like a pulse waveform. The output voltage and current ramp up to the target value in a certain period of time after the channel is turned on depending on the value of capacitor on the OUTXn pin. The ramping up period is proportional to the capacitance value of the capacitor. To avoid the output voltage of each OUTXn is measured in the ramping up transient period, the TPS929160-Q1 integrates a $t_{(BLANK)}$ timer which is programmable by a 4-bit register BLANK to setup the blanking time for all OUTXn. The device does not start the OUTXn diagnostics and ADC measurement until the $t_{(BLANK)}$ timer is overflow. The $t_{(BLANK)}$ timer is programmable from 20 µs to 4 ms as described in the Table 6-2. TI recommends to set the $t_{(BLANK)}$ less than the PWM dimming period which is programmable by PWMFREQ register, otherwise the OUTXn diagnostics and ADC measurement only operates properly when PWM duty cycle is set to 100%.

Table 6-2. Blank Time

	Blank Time															
Binary Code	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
$t_{(BLANK)}$ (µs)	100	20	30	50	80	150	200	300	500	800	1000	1200	1500	2000	3000	4000

6.3.3.4 Phase Shift PWM Dimming

The TPS929160-Q1 supports both PWM dimming method and phase shift PWM dimming method. In PWM dimming mode, all 16 current output channels are turned on and off together at the same time at PWM dimming frequency set by PWMFREQ register as the following figure illustrates.

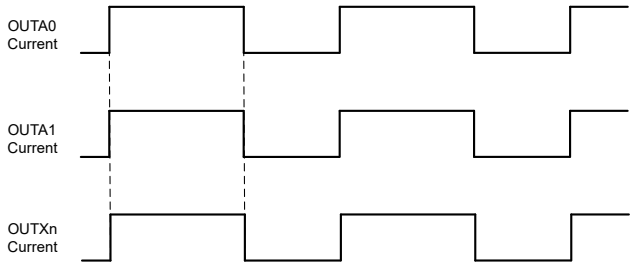


Figure 6-3. PWM Dimming Mode

The phase shift PWM dimming mode is enabled by setting PSEN to 1. In phase shift PWM dimming mode, every three current output channels are formed as one group, so a total of eight current output groups are turned on and off at PWM dimming frequency set by PWMFREQ register with a constant delay as the following figure illustrates. The detailed group information is also listed in the below table.

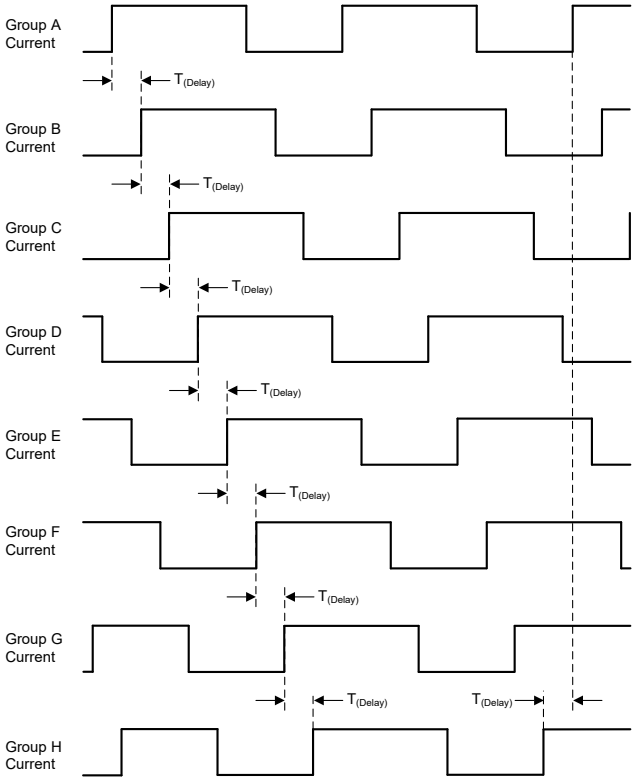


Figure 6-4. Phase Shift Dimming Mode

Table 6-3. Phase Shift Dimming Groups

Phase	Groups	Output Channels	
Phase 0	Group A	OUTA0	OUTA1
Phase 1	Group B	OUTB0	OUTB1
Phase 2	Group C	OUTC0	OUTC1
Phase 3	Group D	OUTD0	OUTD1
Phase 4	Group E	OUTE0	OUTE1
Phase 5	Group F	OUTF0	OUTF1
Phase 6	Group G	OUTG0	OUTG1
Phase 7	Group H	OUTH0	OUTH1

The phase delay interval is 1/8 of PWM dimming cycle time between two neighboring groups. The phase delay can be calculated with the below equation.

$$T_{(Delay)} = \frac{1}{8 \times F_{(PWM)}} \quad (3)$$

where

- $F_{(PWM)}$ is PWM dimming frequency set by PWMFREQ.

6.3.3.5 Linear Brightness Control

When register EXPEN is set to 0, the MSB 8 bits of 12-bit binary input to PWM generator are directly copied from 8-bit register PWMOUTXn, and the LSB 4 bits are directly copied from 4-bit register PWMLOWOUTXn. The PWM output duty cycle can be calculated with the following equation. The PWM output duty cycle is linearly controlled by the register PWMOUTXn and PWMLOWOUTXn, which provides the linear brightness control to each channel output. When PWMOUTXn is FFh, and PWMLOWOUTXn is Fh, the duty cycle is 100% exceptionally.

$$D_{(OUTXn)} = \frac{(16 \times PWMOUTXn + PWMLOWOUTXn)}{4096} \times 100\% \quad (4)$$

where

- PWMOUTXn is decimal number from 0 to 255.
- PWMLOWOUTXn is decimal number from 0 to 15.
- X is from A to H, n is 0 or 1 for different output channel.

Because the 12-bit PWM duty cycles require 2 bytes of write operation to update the completed data, the output PWM duty cycle is not changed in between of the two bytes data transmission. TPS929160-Q1 only updates PWM duty cycle of any output when its high 8-bit PWMOUTXn is written. When very fast brightness change is needed, for example, fade-in and fade-out effects, simultaneous PWM duty cycle change of all channels is required. Setting SHAREPWM to 1 enables all channels using the PWM duty cycle setting of channel A0 to save communication latency. When disabling the SHAREPWM, PWM outputs of all the channels remain unchanged until the corresponding PWM duty cycle setting registers are modified.

To reduce the data transmission for large quantity of the LED pixel control, 8-bit PWM duty cyle resolution can be adopted by writing 0 to 12BIT in DIM register. The master only needs to update high 8-bit PWMOUTXn register to change the brightness of target output channel. The low 4-bit registers PWMLOWOUTXn are ignored. The PWM duty-cycle calculation is shown in he below equation. When PWMOUTXn is FFh, the duty cycle is 100% exceptionally.

$$D_{(OUTXn)} = \frac{PWMOUTXn}{256} \times 100\% \quad (5)$$

where

- PWMOUTXn is decimal number from 0 to 255.
- X is from A to H, n is 0 or 1 for different output channel.

6.3.3.6 Exponential Brightness Control

The TPS929160-Q1 can also generate PWM duty-cycle output following exponential curve. EXPEN bit selects the dimming method between linear or exponential. When register EXPEN is set to 1, the integrated look-up table provides a one-to-one conversion from 8-bit register PWMOUTXn to 12-bit binary code following exponential increment, as the following figure illustrates. When exponential control path is selected, the PWMLOWOUTXn data is neglected. By using the exponential brightness control, LED brightness change by one LSB is invisible to human eyes especially at low brightness range.

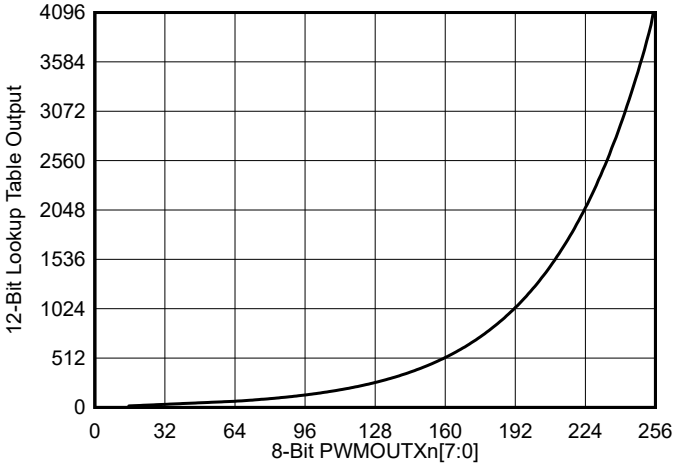


Figure 6-5. PWM Duty Cycle vs 8-Bit Code for Exponential Dimming

During power up or in FAIL-SAFE state, the registers EXPEN, and PWMFREQ are automatically reset to their default values stored in their corresponding EEPROM. Both PWMOUTXn and PWMLOWOUTXn are reset to 00h during power up, but load their EEPROM content in FAIL-SAFE state.

6.3.4 FAIL-SAFE State Operation

The TPS929160-Q1 supports independent channel brightness control through the FlexWire interface. The brightness of each channel is adjustable according to its DC current register IOUTXn, PWM duty cycle register PWMOUTXn/PWMLOWOUTXn and channel enable register ENOUTXn setting. The brightness of each channel reflects to its register setting value immediately after register is successfully updated through the FlexWire interface by master unit. However, the master unit loses the control for all current channels if the FlexWire communication fails between master unit and the TPS929160-Q1. For example, the interface cable is broken by accident. As a consequence, the brightness for all output channels of the TPS929160-Q1 are stuck and the ON and OFF control for all output channels are missed too. To keep the basic ON and OFF control for each output channels, the TPS929160-Q1 provides a FAIL-SAFE state when the communication to master is lost. For detailed description for FAIL-SAFE state entering and quitting criteria, refer to *Device Functional Modes*.

When the TPS929160-Q1 is entering FAIL-SAFE state, all the registers are set to default value or reloaded from EEPROM including IOUTXn, PWMOUTXn, PWMLOWOUTXn and ENOUTXn. The pre-programmed settings in the EEPROM are loaded and the corresponding registers are reset to the default values. The TPS929160-Q1 provides two hardware input pins, FS0 and FS1 to turn on or off corresponding current output channels in FAIL-SAFE state. Each current output channel has its own register, FSOUTXn to set the mapping to FS0 or FS1. When FSOUTXn is set to 0, the corresponding current output channel is controlled by FS0 input, otherwise it is controlled by FS1 input. If the voltage of FSx input is higher than its high threshold, $V_{IH(IO)}$, all current output channels mapped to FSx input are turned on. When the voltage of FSx input drops below low threshold, $V_{IL(IO)}$, all current out channels mapped to FSx input are turned off. The flag register FLAG_EXTFSx shows the FSx input level at real-time. If FSx pin input voltage is logic high, the FLAG_EXTFSx is set to 1. All FSOUTXn registers load their corresponding EEPROM data when the TPS929160-Q1 enters FAIL-SAFE state.

The PWM generator and phase shift dimming are both supported in FAIL-SAFE state. Figure 6-6 is the signal path diagram for PWM generator in FAIL-SAFE state.

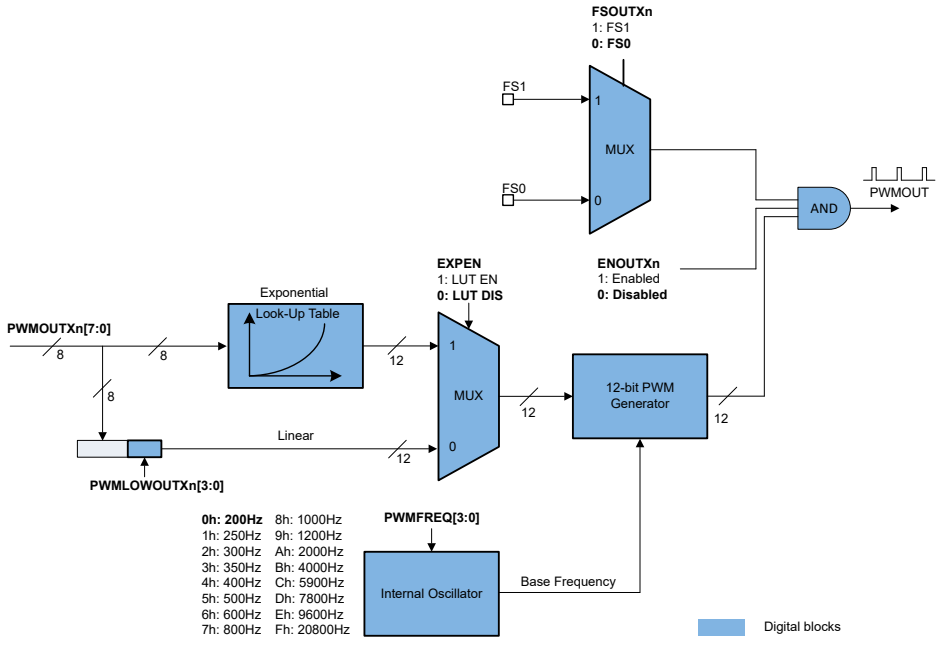


Figure 6-6. Output Current Control Path in FAIL-SAFE State

The FAIL-SAFE state also allows the TPS929160-Q1 operating as a standalone device without master controlling in the system. The $\overline{ERR}$ pin is used as a fault indicator to achieve one-fails-all-fail or one-fails-others-on diagnostics requirement. When low quiescent current in fault mode is required, the device must be set as one-fails-all-fail. In this case, if fault is triggered, the device goes into low current fault mode.

6.3.5 On-Chip, 8-Bit, Analog-to-Digital Converter (ADC)

The TPS929160-Q1 has integrated a successive-approximation-register (SAR) ADC for diagnostics.

To manually read the voltage of an ADC channel as listed in the below table, the user must write the 5-bit register ADCCHSEL to select channel. After ADCCHSEL register is written, the one-time ADC conversion starts and clears FLAG_ADCDONE register. As long as the ADC conversion is completed, the ADC result is available in an 8-bit register ADC_OUT and sets FLAG_ADCDONE to 1. Reading the ADC_OUT register also clears FLAG_ADCDONE and starts a new ADC conversion. The FLAG_ADCDONE is set to 0 after reading completion. TI recommends to write the ADCCHSEL register after turning on or changing current output duty cycle at assigned OUTXn with delay of one PWM cycle time which is set by the PWMFREQ register.

The analog value can be calculated based on the read back binary code with the below equation and table.

$$\text{Analog Value} = a + k \times (\text{ADC\_OUT}) \tag{6}$$

where

- ADC_OUT is a decimal number from 0 to 255.

Table 6-4. ADC Channel

CHANNEL NO.	ADCCHSEL	NAME	ADC CALCULATION PARAMETER (a)	ADC CALCULATION PARAMETER (k)	COMMENT
0	00h	REF	0.007V	0.0101V/LSB	Reference voltage
1	01h	SUPPLY	0.1346V	0.1608V/LSB	SUPPLY voltage
2	02h	VLDO	0.0465V	0.022V/LSB	5V LDO output voltage
3	03h	TEMPSNS	–270.312°C	2.688°C/LSB	Internal temperature sensor
4	04h	IREF	0.9969µA	0.9969µA/LSB	Reference current
5	05h	VBAT	0.1346V	0.1608V/LSB	VBAT Voltage
6	06h	MAXOUT	0.1346V	0.1608V/LSB	Maximum channel output voltage
7	07h	RESERVED	RESERVED	RESERVED	RESERVED
8	08h	OUTA0	0.1346V	0.1608V/LSB	Output voltage channel A0
9	09h	OUTA1	0.1346V	0.1608V/LSB	Output voltage channel A1
10	0Ah	RESERVED			RESERVED
11	0Bh	OUTB0	0.1346V	0.1608V/LSB	Output voltage channel B0
12	0Ch	OUTB1	0.1346V	0.1608V/LSB	Output voltage channel B1
13	0Dh	RESERVED	RESERVED	RESERVED	RESERVED
14	0Eh	OUTC0	0.1346V	0.1608V/LSB	Output voltage channel C0
15	0Fh	OUTC1	0.1346V	0.1608V/LSB	Output voltage channel C1
16	10h	RESERVED	RESERVED	RESERVED	RESERVED
17	11h	OUTD0	0.1346V	0.1608V/LSB	Output voltage channel D0
18	12h	OUTD1	0.1346V	0.1608V/LSB	Output voltage channel D1
19	13h	RESERVED	RESERVED	RESERVED	RESERVED
20	14h	OUTE0	0.1346V	0.1608V/LSB	Output voltage channel E0
21	15h	OUTE1	0.1346V	0.1608V/LSB	Output voltage channel E1
22	16h	RESERVED	RESERVED	RESERVED	RESERVED
23	17h	OUTF0	0.1346V	0.1608V/LSB	Output voltage channel F0
24	18h	OUTF1	0.1346V	0.1608V/LSB	Output voltage channel F1
25	19h	RESERVED	RESERVED	RESERVED	RESERVED
26	1Ah	OUTG0	0.1346V	0.1608V/LSB	Output voltage channel G0

Table 6-4. ADC Channel (continued)

CHANNEL NO.	ADCCHSEL	NAME	ADC CALCULATION PARAMETER (a)	ADC CALCULATION PARAMETER (k)	COMMENT
27	1Bh	OUTG1	0.1346V	0.1608V/LSB	Output voltage channel G1
28	1Ch	RESERVED	RESERVED	RESERVED	RESERVED
29	1Dh	OUTH0	0.1346V	0.1608V/LSB	Output voltage channel H0
30	1Eh	OUTH1	0.1346V	0.1608V/LSB	Output voltage channel H1
31	1Fh	RESERVED	RESERVED	RESERVED	RESERVED

6.3.5.1 Minimum On Time for ADC Measurement

Because the TPS929160-Q1 supports PWM control for adjusting LED brightness, the voltage on OUTXn is like a pulse waveform. When the current output is enabled by setting ENOUTXn to 1, the ADC measures the voltage on assigned OUTXn after the output is turned on with $t_{(BLANK)}$ delay time, which is programmable by 4-bit register BLANK. The minimum current output pulse on assigned OUTXn must be longer than $t_{(BLANK)} + 3 \times t_{(CONV)}$ to make sure the correct measured result for OUTXn at ON state. When the output is disabled by setting ENOUTXn to 0, the ADC samples the voltage on assigned OUTXn at OFF state.

TI recommends to set 100% duty cycle on assigned OUTXn for ADC measurement by writing FFh to PWMOUTXn and 0Fh to PWMLOWOUTXn register when the PWM dimming period $t_{(DIM\_cycle)}$ has to be less than $t_{(BLANK)} + 3 \times t_{(CONV)}$.

6.3.5.2 ADC Auto Scan

In ADC auto scan mode, If the MAXOUT channel is selected by writing 06h to ADCCHSEL, the maximum voltage of OUTXn is recorded into ADC_OUT register. The maximum channel output voltage is available after at least nine output PWM cycles are completed. The ADC measures every two outputs as one group when the group is turned on and move to measure the next group in next PWM dimming cycle until all eight groups are completed no matter in PWM dimming mode or phase shift PWM dimming mode. The device sets FLAG_ADCDONE to 1 and stops ADC auto scan after the measurements for all eight groups are done. The FLAG_ADCDONE is cleared to 0 by reading the ADC_OUT, and ADC auto scan restarts again if the data of ADCCHSEL is still 06h. FLAG_ADCDONE is also cleared to 0 by writing ADCCHSEL register, and ADC restarts after FLAG_ADCDONE is cleared. The minimum current pulse for each output must be longer than $t_{(BLANK)} + 3 \times t_{(CONV)}$ in auto scan mode. The channel is skipped if it is disabled in auto scan mode.

Based on the measured maximum output voltage and supply voltage, the microcontroller is able to regulate supply voltage from previous power stage to minimize the power consumption on the TPS929160-Q1. Basically, the microcontroller must program the output voltage of previous power stage to be just higher than the measured maximum channel output voltage plus the required dropout voltage $V_{(OUT\_drop)}$ of the TPS929160-Q1. In this way, the TPS929160-Q1 takes minimum power consumption, and overall power efficiency optimizes.

6.3.5.3 ADC Error

The TPS929160-Q1 integrates a digital comparator to measure the PWM dimming period $t_{(DIM\_cycle)}$ and $t_{(BLANK)} + 3 \times t_{(CONV)}$ at real time when ADC is started by writing ADCCHSEL register or reading ADC_OUT register. The device stops the ADC measurement and sets the FLAG_ADCERR register to 1 if the $t_{(DIM\_cycle)}$ time is measured less than $t_{(BLANK)} + 3 \times t_{(CONV)}$ time. The FLAG_ADCERR register is cleared to 0 by writing 1 to the CLRFAULT register.

6.3.6 NSTB Output

The TPS929160-Q1 device provides a NSTB output to control external CAN transciever enter into sleep mode. The NSTB ouput is an open drain structure with internal pulling up path to VLDO, and it is recommended to be pulled down to GND through an external 100kΩ resistor. The internal pull up of NSTB output is turned on by default and only turned off when NSTB register is set to 1h. The pulling up path is turned on again when the NSTB register is set to 0h. Which means that the NSTB output always exhibits VLDO voltage output after device

is enabled by pulling high EN pin, and it goes to low once the NSTB register is set to 1h or the TPS929160-Q1 is disabled.

With this NSTB output, the TPS929160-Q1 can set an external CAN transciever such as TCAN1043-Q1 into sleep mode by controlling the nSTB input pin of TCAN1043-Q1 to minimize the power consumption. The TCAN1043-Q1 can also remove the pulling up of the EN pin of TPS929160-Q1 by its INH output to shutdown the TPS929160-Q1 after entering the sleep mode. The TCAN1043-Q1 can be waked up again by a specified WUP pattern and release INH output to turn on the TPS929160-Q1 as well. Figure 6-7 and Figure 6-8 are the typical application and timing diagram for TPS929160-Q1 cooperating with TCAN1043-Q1 to achieve the low current consumption in sleep mode.

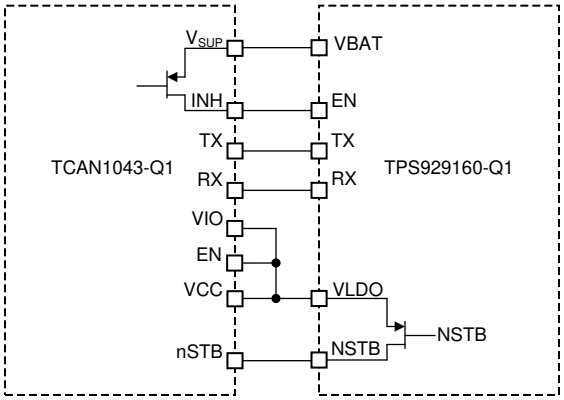


Figure 6-7. Sleep Mode Typical Application Diagram

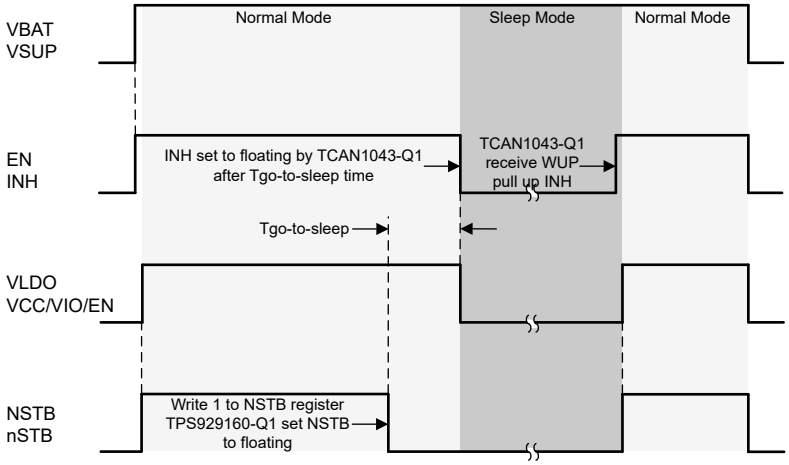


Figure 6-8. Sleep Mode Access and Exit Timing Diagram

6.3.7 Diagnostic and Protection in NORMAL State

The TPS929160-Q1 has full-diagnostics coverage for supply voltage, current output, and junction temperature.

In NORMAL state, the device detects all failures and reports the status out through the $\overline{\text{ERR}}$ or FLAG registers, without any actions taken by the device except VBAT UVLO, supply undervoltage and overtemperature protection. The master controller must handle all fault actions, for example, retry several times and shut down the outputs if the error still exists. The fault behavior in NORMAL state can be found in Table 6-6.

6.3.7.1 VBAT Undervoltage Lockout Diagnostics in NORMAL state

When VBAT or VLDO voltage drops below its UVLO threshold, the device enters POR state. Upon voltage recovery, the device automatically switches to INIT state with FLAG_POR and FLAG_ERR set to 1. The master

controller can write 1 to register CLRPOR to clear the FLAG_POR and FLAG_ERR, and the CLRPOR bit automatically returns to 0.

6.3.7.2 Low-Supply Warning Diagnostics in NORMAL State

The TPS929160-Q1 continuously monitors the SUPPLY voltage and compares the results with internal threshold $V_{(LOWSUPTH)}$ set by LOWSUPTH for low-supply voltage warning.

If the supply voltage is lower than threshold, the device pulls $\overline{ERR}$ pin down with one pulsed current sink for 50 µs to report the fault and set flag registers including FLAG_LOWSUP and FLAG_ERR to 1.

The fault is latched in flag registers. When the supply voltage rises above low-supply warning threshold, the master controller must write 1 to register CLRFAULT to clear FLAG_LOWSUP and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

The low-supply warning is also used to disable the LED open-circuit detection and single-LED short-circuit detection. When the voltage applied on SUPPLY pin is higher than the threshold $V_{(LOWSUPTH)}$, the TPS929160-Q1 enables LED open-circuit and single-LED short-circuit diagnosis. When $V_{(SUPPLY)}$ is lower than the threshold $V_{(LOWSUPTH)}$, the device disables LED-open-circuit detection and single-LED short-circuit diagnosis. Because when $V_{(SUPPLY)}$ drops below the maximum total LED forward voltage plus required $V_{(OUT\_drop)}$ at required current, the TPS929160-Q1 is not able to deliver sufficient current output. The device pulls the voltage of each output channel as close as possible to the $V_{(SUPPLY)}$. In this condition, the LED open-circuit fault or single-LED short-circuit fault can be detected and reported by mistake. Setting the low-supply warning threshold high enough can avoid the LED open-circuit and single LED short-circuit fault being detected when $V_{(SUPPLY)}$ drops to low. The $V_{(LOWSUPTH)}$ is programmable from 4 V to 35 V at 1-V interval.

6.3.7.3 Supply Undervoltage Diagnostics in NORMAL State

The TPS929160-Q1 provides internal analog comparator to monitor the supply voltage for undervoltage protection.

If the supply voltage falls below the internal threshold, $V_{(SUPUV\_th\_falling)}$, the device pulls the $\overline{ERR}$ pin low with constant current sink to report the fault and set flag registers including FLAG_SUPUV and FLAG_ERR to 1.

The supply undervoltage detection is used to disable all current output. When the voltage applied on the SUPPLY pin is higher than the threshold $V_{(SUPUV\_th\_rising)}$, the TPS929160-Q1 enables all current outputs. When $V_{(SUPPLY)}$ is lower than the threshold $V_{(SUPUV\_th\_falling)}$, the device disables every output to avoid the unwanted LED flickering or output fault triggered improperly.

The fault is latched in flag registers. When the supply voltage rises above $V_{(SUPUV\_th\_rising)}$, the master controller must write register CLRFAULT to 1 to clear FLAG_SUPUV and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

6.3.7.4 Reference Diagnostics in NORMAL state

The TPS929160-Q1 integrates diagnostics for REF resistor open and short fault. The device monitors the reference current $I_{(REF)}$ set by external resistor $R_{(REF)}$. The $I_{(REF)}$ can be calculated with the following equation.

$$I_{(REF)} = \frac{V_{(REF)}}{R_{(REF)}} \tag{7}$$

where

- $V_{(REF)}$ = 1.235 V typically

If the current output from REF pin $I_{(REF)}$ is lower than $I_{(REF\_OPEN\_th)}$, the reference resistor open-circuit fault is reported. The reference resistor short-circuit fault is reported if the voltage of REF pin $V_{(REF)}$ is lower than $V_{(REF\_SHORT\_th)}$. The device pulls the $\overline{ERR}$ pin down with constant current sink and set flag registers including FLAG_REF and FLAG_ERR to 1.

The fault is latched in flag registers. After the REF pin $I_{(REF)}$ and $V_{(REF)}$ recover to normal, the device releases $\overline{ERR}$ pin pulldown automatically and the master controller must send CLRFAULT to clear FLAG_REF and FLAG_ERR. The CLRFAULT automatically returns to 0.

In NORMAL state, the device does not perform any actions automatically when the reference resistor fault is detected. However, the output can not work properly and the output current can be operating at high current level. TI recommends for master controller to shut down the device outputs and report error to upper level control system such as Body Control Module (BCM).

6.3.7.5 Pre-Thermal Warning in NORMAL state

The TPS929160-Q1 has pre-thermal warning at typical 135°C.

When the junction temperature, $T_{(J)}$, of TPS929160-Q1 rises above pre-thermal warning threshold, the device reports pre-thermal warning, pull $\overline{ERR}$ pin with pulsed current sink for 50 µs and sets the flag registers including FLAG_PRETSD and FLAG_ERR to 1.

The fault is latched in flag registers. When the junction temperature of TPS929160-Q1 falls below pre-thermal warning threshold, the master controller must write 1 to CLRFAULT register to clear FLAG_PRETSD and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

When more accurate thermal measurement on LED unit is required, one current output channel can be sacrificed to provide current bias to external thermal resistor such as PTC or NTC. The voltage of external thermal resistor can be measured by integrated ADC to acquire the temperature information of thermal resistor located area. The master controller can determine actions based on the acquired temperature information to turn off or reduce current output.

6.3.7.6 Overtemperature Protection in NORMAL state

The TPS929160-Q1 has overtemperature protection at $T_{(TSD1)}$, typical 175°C.

When device junction temperature $T_{(J)}$ further rises above overtemperature protection threshold, the device turns off all output drivers, pulls the $\overline{ERR}$ pin low with constant current sink to report fault, and sets the flag registers including FLAG_TSD and FLAG_ERR to 1.

The fault is latched in flag registers. When the junction temperature falls below $T_{(TSD1)} – T_{(TSD1\_HYS)}$, the device resumes all outputs and releases $\overline{ERR}$ pin pulldown. The master controller must write 1 to CLRFAULT to clear FLAG_TSD and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

6.3.7.7 Overtemperature Shutdown in NORMAL state

When the $T_{(J)}$ rises too high above $T_{(TSD2)}$, 180°C typically, the TPS929160-Q1 turns off the internal linear regulator, VLDO output to shutdown all the analog and digital circuit. The $\overline{ERR}$ pin is pulled down by constant current sink to report the fault, and the FLAG_POR and FLAG_ERR are all set to 1.

When the $T_{(J)}$ drops below $T_{(TSD2)} – T_{(TSD2\_HYS)}$, the TPS929160-Q1 restarts from POR state with all the registers cleared to default value and $\overline{ERR}$ pin released. The master controller must write 1 to CLRPOR to clear both FLAG_POR and FLAG_ERR after fault removal. The CLRPOR bit automatically returns to 0.

6.3.7.8 LED Open-Circuit Diagnostics in NORMAL state

The TPS929160-Q1 integrates LED open-circuit diagnostics to allow users to monitor LED status real time. The device monitors voltage difference between SUPPLY and OUTXn to judge if there is any open-circuit failure. The SUPPLY voltage is also monitored in parallel with programmable threshold to determine if supply voltage is high enough for open-circuit diagnostics.

The open-circuit monitor is only effective during PWM-ON state with programmable minimal pulse width greater than $t_{(BLANK)} + t_{(OPEN\_deg)}$. The $t_{(BLANK)}$ is programmed by register BLANK. If PWM on-time is less than $t_{(BLANK)} + t_{(OPEN\_deg)}$, the device does not report any open-circuit fault. When the device supply voltage $V_{(SUPPLY)}$ is below the threshold $V_{(LOWSUPTH)}$ set by register LOWSUPTH, the LED open-circuit is not detected nor reported.

When the voltage difference $V_{(SUPPLY)}$ – $V_{(OUTXn)}$ is below threshold $V_{(OPEN\_th\_rising)}$ with duration longer than $t_{(BLANK)}$ + $t_{(OPEN\_deg)}$, and the device supply voltage $V_{(SUPPLY)}$ is above the threshold $V_{(LOWSUPTH)}$ set by register LOWSUPTH, the TPS929160-Q1 pulls the $\overline{ERR}$ pin down with one pulsed current sink for 50 µs to report fault and set flag registers including FLAG_OPENOUTXn, FLAG_OUT and FLAG_ERR to 1. In NORMAL state, the device does not take any actions in response the LED open-circuit fault and waits for the master controller to determine the protection behavior.

The fault is latched in flag registers. When the voltage difference $V_{(SUPPLY)}$ – $V_{(OUTXn)}$ rises above threshold $V_{(OPEN\_th\_rising)}$ with duration longer than $t_{(BLANK)}$ + $t_{(OPEN\_deg)}$, or the device supply voltage $V_{(SUPPLY)}$ is below the threshold $V_{(LOWSUPTH)}$, the master controller must write 1 to CLRFAULT to clear FLAG_OPENOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

6.3.7.9 LED Short-Circuit Diagnostics in NORMAL state

The TPS929160-Q1 has internal analog comparators to monitor all channel outputs with respect to a fixed threshold for reporting OUTXn short to GND fault.

The short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of $t_{(BLANK)}$ + $t_{(SHORT\_deg)}$. The $t_{(BLANK)}$ is programmable by register BLANK. If PWM on-time is less than $t_{(BLANK)}$ + $t_{(SHORT\_deg)}$, the device can not report any short-circuit fault.

When the voltage $V_{(OUTXn)}$ is below threshold $V_{(SG\_th\_rising)}$ with duration longer than deglitch timer length of $t_{(BLANK)}$ + $t_{(SHORT\_deg)}$, the device pulls the $\overline{ERR}$ pin down with pulsed current sink for 50 µs to report fault and set flag registers including FLAG_SHORTOUTXn, FLAG_OUT and FLAG_ERR. In NORMAL state, the device does not take any actions in response the LED short-circuit fault and waits for the master controller to determine the protection behavior.

The fault is latched in flag registers. When the voltage $V_{(OUTXn)}$ rises above threshold $V_{(SG\_th\_falling)}$ with duration longer than deglitch timer length of $t_{(BLANK)}$ + $t_{(SHORT\_deg)}$, the master controller must write 1 to CLRFAULT to clear FLAG_SHORTOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

6.3.7.10 Single-LED Short-Circuit Detection in NORMAL state

The TPS929160-Q1 also integrates analog comparators to monitor all outputs with respect to two alternative threshold for single-LED short-circuit diagnostic. Setting the register SLSEN to 1 enables the single-LED short-circuit detection.

The single-LED, short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of $t_{(BLANK)}$ + $t_{(SLS\_deg)}$. The $t_{(BLANK)}$ is programmable by register BLANK. If PWM on-time is less than $t_{(BLANK)}$ + $t_{(SLS\_deg)}$, the device cannot report any single-LED short-circuit fault. When the device supply voltage $V_{(SUPPLY)}$ is below the threshold $V_{(LOWSUPTH)}$ set by register LOWSUPTH, the single-LED short-circuit is not detected nor reported.

When the voltage $V_{(OUTXn)}$ is below threshold $V_{(SLSTHx)}$ with duration longer than deglitch timer length of $t_{(BLANK)}$ + $t_{(SLS\_deg)}$, and the device supply voltage $V_{(SUPPLY)}$ is above the threshold $V_{(LOWSUPTH)}$ set by register LOWSUPTH, the device pulls the $\overline{ERR}$ pin down with pulsed current sink for 50 µs to report fault and set flag registers including FLAG_SLSOUTXn, FLAG_OUT and FLAG_ERR. The TPS929160-Q1 provides two alternative thresholds $V_{(SLSTH0)}$ and $V_{(SLSTH1)}$ for single-LED short-circuit detection selected by SLSTHOUTXn independently for each current output. The $V_{(SLSTH0)}$ is selected for current OUTXn when SLSTHOUTXn is set to 0, however $V_{(SLSTH1)}$ is selected when SLSLTHOUTXn is set to 1. The actual voltage value for $V_{(SLSTH0)}$ and $V_{(SLSTH1)}$ is programmable by two 8-bit registers SLSTH0 and SLSTH1 from 2.5 V to 34.375 V at 125-mV interval. In NORMAL state, the device does not take any actions in response the single-LED short-circuit fault and waits for the master controller to determine the protection behavior.

The fault is latched in flag registers. When the voltage $V_{(OUTXn)}$ rises above threshold $V_{(SLSTHx)}$ + 275 mV with duration longer than deglitch timer length of $t_{(BLANK)}$ + $t_{(SLS\_deg)}$, or the device supply voltage $V_{(SUPPLY)}$ is below the threshold $V_{(LOWSUPTH)}$, the master controller must write 1 to register CLRFAULT to clear FLAG_SLSOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT automatically returns to 0.

6.3.7.11 EEPROM CRC Error in NORMAL state

The TPS929160-Q1 implements a EEPROM CRC check after loading the EEPROM code to configuration register in NORMAL state.

The calculated CRC result is sent to register CALC_EEPCRC and compared to the data in register EEPCRC, which stores the CRC code for all EEPROM registers except for DIM-R reserved register. The reserved DIM-R register value is not included in the EEPCRC calculation. The TPS929160-Q1 *EEPROM configuration tool* are available on *ti.com* to help calculate the EEPCRC value. If the code in register CALC_EEPCRC is not matched to the code in register EEPCRC, the TPS929160-Q1 pulls the $\overline{ERR}$ pin down with pulsed current sink for 50 µs to report the fault and set the registers including FLAG_EEPCRC and FLAG_ERR to 1. The TPS929160-Q1 only loads EEPROM to corresponding registers one time during initialization state. Parity check is used to detect whether the internal configuration parameters are correctly loaded from trim EEPROM or not. When there is internal trim EEPROM error, the FLAG_EEPPAR is set to 1. The master controller can write 1 to REGDEFAULT to reset all the regiters to default value and reload the EEPROM to corresponding registers in NORMAL state. Reloading the EEPROM triggers the EEPROM CRC check.

The master controller must write CLRFAULT to 1 to clear the fault flags, and the CLRFAULT bit automatically returns to 0.

The CRC code for all the EEPROM registers must be burnt into EEPROM register of EEPCRC in the end of production line. The CRC code algorithm for multiple bytes of binary data is based on the polynomial, $X^8 + X^5 + X^4 + 1$. The CRC code contain 8 bits binary code, and the initial value is FFh. As described in the below figure, all bits code shift to MSB direction for 1 bit with three exclusive-OR calculation. A new CRC code for one byte input canbe generated after repeating the 1 bit shift and three exclusive-OR calculation for eight times. Based on this logic, the CRC code can be calculated for all the EEPROM register byte. When the EEPROM design for production is finalized, the corresponding CRC code based on the calculation must be burnt to EEPROM register EEPCRC together with other EEPROM registers in the end of production line. If the DC current for each output channel must be calibrated in the end of production for different LED brightness bin, the CRC code for each production devices must be calculated independent and burnt during the calibration. The CRC algorithm must be implemented into the LED calibration system in the end of production line.

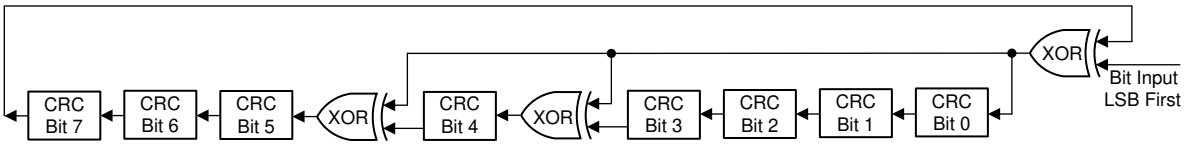


Figure 6-9. CRC Algorithm Diagram

6.3.7.12 Communication Loss Diagnostic in NORMAL state

The TPS929160-Q1 monitors the FlexWire interface for the communication with an internal watchdog timer.

Any successful non-broadcast communication with correct CRC and address matching target device automatically resets the timer. The watchdog timer starts to count when UART bus is idle. If the watchdog timer overflows, device automatically switches to FAIL-SAFE state and sets the FLAG_FS to 1. The master controller can access the TPS929160-Q1 and write 1 to CLRFS to set the device to NORMAL state again when the communication recovers.

The watchdog timer is programmable by 4-bit register WDTIMER. The TPS929160-Q1 can directly enter FAIL-SAFE states from NORMAL state by burning EEPROM of WDTIMER to Fh. Disabling the watchdog timer by setting WDTIMER to 0h prevents the device from getting into FAIL-SAFE state.

6.3.7.13 Fault Masking in NORMAL state

The TPS929160-Q1 provides fault masking capability using masking registers. The device is capable of masking faults by channels or by fault types. The fault masking does not disable diagnostics features but only prevents fault reporting to FLAG_OUT register, FLAG_ERR register, and $\overline{ERR}$ output. The below table lists the detailed description for each fault mask register in NORMAL state.

To disable diagnostics on a single channel, setting DIAGENOUTXn registers to 0 disables open-circuit, LED short-circuit and single-LED short circuit diagnostics of channel x and thus no fault of this channel is reported to FLAG_OPENOUTXn, FLAG_SHORTOUTXn, FLAG_SLSOUTXn, FLAG_OUT or FLAG_ERR registers, or to the $\overline{\text{ERR}}$ output.

Table 6-5. Fault Masking in NORMAL state

Fault Detected	Mask Register	FLAG Name	$\overline{\text{ERR}}$ PIN
Low-supply warning	MASKLOWSUP = 1	FLAG_LOWSUP = 1 FLAG_ERR = 0	No action
	MASKLOWSUP = 0	FLAG_LOWSUP = 1 FLAG_ERR = 1	One pulse pulled down for 50 µs
Supply undervoltage	MASKSUPUV = 1	FLAG_SUPUV = 1 FLAG_ERR = 0	No action
	MASKSUPUV = 0	FLAG_SUPUV = 1 FLAG_ERR = 1	Constant pulled down
Reference fault	MASKREF = 1	FLAG_REF = 1 FLAG_ERR = 0	No action
	MASKREF = 0	FLAG_REF = 1 FLAG_ERR = 1	Constant pulled down
Pre-thermal warning	MASKPRETSD = 1	FLAG_PRETSD = 1 FLAG_ERR = 0	No action
	MASKPRETSD = 0	FLAG_PRETSD = 1 FLAG_ERR = 1	One pulse pulled down for 50 µs
Overtemperature protection	MASKTSD = 1	FLAG_TSD = 1 FLAG_ERR = 0	No action
	MASKTSD = 0	FLAG_TSD = 1 FLAG_ERR = 1	Constant pulled down
EEPROM CRC error	MASKEEPCRC = 1	FLAG_EEPCRC = 1 FLAG_ERR = 0	No action
	MASKEEPCRC = 0	FLAG_EEPCRC = 1 FLAG_ERR = 1	One pulse pulled down for 50 µs
LED open-circuit fault	MASKOPEN = 1	FLAG_OPENOUTXn = 1 FLAG_OUT = 0 FLAG_ERR = 0	No action
	MASKOPEN = 0	FLAG_OPENOUTXn = 1 FLAG_OUT = 1 FLAG_ERR = 1	One pulse pulled down for 50 µs
LED short-circuit fault	MASKSHORT = 1	FLAG_SHORTOUTXn = 1 FLAG_OUT = 0 FLAG_ERR = 0	No action
	MASKSHORT = 0	FLAG_SHORTOUTXn = 1 FLAG_OUT = 1 FLAG_ERR = 1	One pulse pulled down for 50 µs
Single LED short-circuit fault	MASKSLS = 1	FLAG_SLSOUTXn = 1 FLAG_OUT = 0 FLAG_ERR = 0	No action
	MASKSLS = 0	FLAG_SLSOUTXn = 1 FLAG_OUT = 1 FLAG_ERR = 1	One pulse pulled down for 50 µs

Table 6-6. Diagnostics Table in NORMAL State

FAULT TYPE	DETECTION CRITERIA	CONDITIONS	FAULT ACTIONS	FAULT OUTPUT	$\overline{ERR}$ PIN	RECOVERY
VBAT UVLO	$V_{(VBAT)} < V_{(POR\_falling)}$ or $V_{(LDO)} < V_{(LDO\_POR\_falling)}$		Device switch to POR state	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLRPOR.
Low-supply warning	$V_{(SUPPLY)} < V_{(LOWSUPTH)}$		Disable fault type *	FLAG_LOWSUP FLAG_ERR (maskable)	One pulse pulled down for 50 µs	Automatically recovery upon fault removal. Clear fault flag with CLRFAULT.
Supply undervoltage	$V_{(SUPPLY)} < V_{(SUPUV\_th\_falling)}$		Turn off all outputs	FLAG_SUPUV FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recovery and release $\overline{ERR}$ pin upon fault removal. Clear fault flag with CLRFAULT.
Reference fault	$V_{(REF)} < V_{(REF\_SHORT\_th)}$ or $I_{(REF)} < I_{(REF\_OPEN\_th)}$		No action	FLAG_REF FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically release $\overline{ERR}$ pin upon fault removal. Clear fault flag with CLRFAULT.
Pre-thermal warning	$T_{(J)} > T_{(PRETSD)}$		No action	FLAG_PRETSD FLAG_ERR(maskable)	One pulse pulled down for 50 µs	Clear fault flag with CLRFAULT
Overtemperature protection	$T_{(J)} > T_{(TSD1)}$		Turn off all outputs	FLAG_TSD FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover upon fault removal. Clear fault flag with CLRFAULT.
Overtemperature shutdown	$T_{(J)} > T_{(TSD2)}$		Turn off LDO	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLRPOR.
LED open-circuit fault *	$V_{(SUPPLY)} - V_{(OUTXn)} < V_{(OPEN\_th\_rising)}$ and $V_{(SUPPLY)} > V_{(LOWSUPTH)}$	PWM pulse width greater than $t_{(BLANK)} + t_{(OPEN\_deg)}$ ENOUTXn = 1 DIAGENOUTXn = 1	No action	FLAG_OPENOUTXn FLAG_OUT (maskable) FLAG_ERR (maskable)	One pulse pulled down for 50 µs (maskable)	Clear fault flag with CLRFAULT
LED short-circuit fault	$V_{(OUTXn)} < V_{(SG\_th\_rising)}$	PWM pulse width greater than $t_{(BLANK)} + t_{(SHORT\_deg)}$ ENOUTXn = 1 DIAGENOUTXn = 1	No action	FLAG_SHORTOUTXn FLAG_OUT (maskable) FLAG_ERR (maskable)	One pulse pulled down for 50 µs (maskable)	Clear fault flag with CLRFAULT
Single-LED short circuit *	$V_{(OUTXn)} < V_{(SLSTH)}$ and $V_{(SUPPLY)} > V_{(LOWSUPTH)}$	PWM pulse width greater than $t_{(BLANK)} + t_{(SLS\_deg)}$ ENOUTXn = 1 DIAGENOUTXn = 1 SLSEN = 1	No action	FLAG_SLSOUTXn FLAG_OUT FLAG_ERR (maskable)	One pulse pulled down for 50 µs	Clear fault flag with CLRFAULT
EEPROM CRC error	CALC_EEPCRC is different EEPCRC		No action	FLAG_EEPCRC FLAG_ERR (maskable)	One pulse pulled down for 50 µs (maskable)	Clear fault flag with CLRFAULT
Communication loss fault	$T_{(WDTIMER)}$ overflows		Enter FAIL-SAFE states	FLAG_FS	No action	Set CLRFS to 1 to set the device to NORMAL state

6.3.8 Diagnostic and Protection in FAIL-SAFE states

In FAIL-SAFE state, the TPS929160-Q1 also detects all failures and reports the status out by $\overline{ERR}$ or FLAG registers. Table 6-8 lists the summary of the fault detection criteria and the device behavior after the fault is detected. Basically, the TPS929160-Q1 actively takes the action to turn off the failed output channels, retry on the failed channels, or restart the device to keep device operating without controlled by master. The EEPROM register OFAF can be used to set the fault behavior for LED open-circuit, LED short-circuit and single-LED short-circuit faults. The one-fails-all-fail behavior is selected when the register OFAF is burnt to 1; otherwise, the one-fails-others-on behavior is chosen. The TPS929160-Q1 turns off all output channels when any type of LED fault is detected on any one of output channels for one-fails-all-fail behavior. On the other hand, the TPS929160-Q1 only turns off the failed channel and keeps all other normal channels on.

In FAIL-SAFE state, the fault flag registers of TPS929160-Q1 still can be accessed again through FlexWire interface in case the communication is rebuilt.

6.3.8.1 Supply Undervoltage Lockout Diagnostics in FAIL-SAFE states

When VBAT or VLDO voltage drops below its UVLO threshold, the device enters POR state. Upon voltage recovery, the device automatically switches to INIT state with FLAG_POR and FLAG_ERR set to 1. The master controller can write 1 to register CLRPOR to clear the FLAG_POR and FLAG_ERR, and the CLRPOR bit automatically returns to 0.

6.3.8.2 Low-Supply Warning Diagnostics in FAIL-SAFE states

The TPS929160-Q1 continuously monitors the SUPPLY voltage and compares the results with internal threshold $V_{(LOWSUPTH)}$ set by LOWSUPTH for low-supply voltage warning.

If the supply voltage is lower than threshold, the device sets flag registers including FLAG_LOWSUP and FLAG_ERR to 1.

The fault is latched in flag registers. When the supply voltage rises above low-supply warning threshold, the master controller must write register CLRFAULT to 1 to reset FLAG_LOWSUP and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

The low-supply warning is also used to disable the LED open-circuit detection and single-LED short-circuit detection. When the voltage applied on SUPPLY pin is higher than the threshold $V_{(LOWSUPTH)}$, the TPS929160-Q1 enables LED open-circuit and single-LED short-circuit diagnosis. When $V_{(SUPPLY)}$ is lower than the threshold $V_{(LOWSUPTH)}$, the device disables LED-open-circuit detection and single-LED short-circuit diagnosis. Because when $V_{(SUPPLY)}$ drops below the maximum total LED forward voltage plus required $V_{(OUT\_drop)}$ at required current, the TPS929160-Q1 is not able to deliver sufficient current output to pull the voltage of each output channel as close as possible to the $V_{(SUPPLY)}$. In this condition, the LED open-circuit fault or single-LED short-circuit fault might be detected and reported by mistake. Setting the low-supply warning threshold high enough can avoid the LED open-circuit and single LED short-circuit fault being detected when $V_{(SUPPLY)}$ drops to low. The $V_{(LOWSUPTH)}$ is programmable from 4 V to 35 V at 1-V interval.

6.3.8.3 Supply Undervoltage Diagnostics in FAIL-SAFE State

The TPS929160-Q1 provides internal analog comparator to monitor the supply voltage for undervoltage protection in FAIL-SAFE state.

If the supply voltage falls below the internal threshold, $V_{(SUPUV\_th\_falling)}$, the device pulls the $\overline{ERR}$ pin low with constant current sink to report the fault and set flag registers including FLAG_SUPUV and FLAG_ERR to 1.

The supply undervoltage detection is used to disable all current output. When $V_{(SUPPLY)}$ is lower than the threshold $V_{(SUPUV\_th\_falling)}$, the device disables every outputs to avoid the unwanted LED flickering or output fault triggered improperly. When the voltage applied on SUPPLY pin rises above the threshold $V_{(SUPUV\_th\_rising)}$, the TPS929160-Q1 enables all current outputs automatically.

The fault is latched in flag registers. When the supply voltage rises above $V_{(SUPUV\_th\_rising)}$, the TPS929160-Q1 releases $\overline{ERR}$ pin and the master controller must write register CLRFAULT to 1 to clear FLAG_SUPUV and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

6.3.8.4 Reference Diagnostics in FAIL-SAFE states

The TPS929160-Q1 integrates diagnostics for REF resistor open and short fault in FAIL-SAFE state. The device monitors the reference current $I_{(REF)}$ set by external resistor $R_{(REF)}$. Use Equation 7 to calculate the $I_{(REF)}$.

If the current output from REF pin $I_{(REF)}$ is lower than $I_{(REF\_OPEN\_th)}$, the reference resistor open-circuit fault is reported. The reference resistor short-circuit fault is reported if the voltage of REF pin $V_{(REF)}$ is lower than $V_{(REF\_SHORT\_th)}$. The device pulls the $\overline{ERR}$ pin down with constant current sink and sets flag registers including FLAG_REF and FLAG_ERR to 1.

The fault is latched in flag registers. After the REF pin $I_{(REF)}$ and $V_{(REF\_SHORT\_th)}$ recover to normal, the device releases $\overline{ERR}$ pin pulldown automatically and the master controller must send CLRFAULT to clear FLAG_REF and FLAG_ERR. The CLRFAULT automatically returns to 0.

In FAIL-SAFE state, the device turns off all output channels when reference fault is detected. The device automatically recovers and turns on all enabled channel after fault removal.

6.3.8.5 Pre-Thermal Warning in FAIL-SAFE state

The TPS929160-Q1 has pre-thermal warning at typical 135°C in FAIL-SAFE state.

When the junction temperature $T_{(J)}$ of TPS929160-Q1 rises above pre-thermal warning threshold, the device reports pre-thermal warning and sets the flag registers including FLAG_PRETSD and FLAG_ERR to 1.

The fault is latched in flag registers. When the junction temperature of TPS929160-Q1 falls below pre-thermal warning threshold, the master controller must write 1 to CLRFAULT register to clear FLAG_PRETSD and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

6.3.8.6 Overtemperature Protection in FAIL-SAFE state

The TPS929160-Q1 has overtemperature protection at $T_{(TSD1)}$, typical 175°C in FAIL-SAFE state.

When device junction temperature $T_{(J)}$ further rises above overtemperature protection threshold, the device turns off all output drivers, pulls the $\overline{ERR}$ pin low with constant current sink to report fault, and sets the flag registers including FLAG_TSD and FLAG_ERR to 1.

The fault is latched in flag registers. When the junction temperature falls below $T_{(TSD1)} – T_{(TSD1\_HYS)}$, the device resumes all outputs and releases $\overline{ERR}$ pin pulldown. The master controller must write 1 to CLRFAULT to clear FLAG_TSD and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

6.3.8.7 Overtemperature Shutdown in FAIL-SAFE state

When the $T_{(J)}$ rises too high above $T_{(TSD2)}$, typical 180°C typically, the TPS929160-Q1 turns off the internal linear regulator, VLDO output to shutdown all the analog and digital circuit. The $\overline{ERR}$ pin is pulled down by constant current sink to report the fault, and the FLAG_POR and FLAG_ERR are all set to 1.

When the $T_{(J)}$ drops below $T_{(TSD2)} – T_{(TSD2\_HYS)}$, the TPS929160-Q1 restarts from POR state with all the registers cleared to default value and $\overline{ERR}$ pin released. The master controller must write 1 to CLRPOR to clear both FLAG_POR and FLAG_ERR after fault removal. The CLRPOR bit automatically returns to 0.

6.3.8.8 LED Open-Circuit Diagnostics in FAIL-SAFE state

The TPS929160-Q1 integrates LED open-circuit diagnostics to allow users to monitor LED status real time in FAIL-SAFE state. The device monitors voltage difference between SUPPLY and OUTXn to judge if there is any open-circuit failure. The SUPPLY voltage is also monitored in parallel with programmable threshold to determine if supply voltage is high enough for open-circuit diagnostics.

The open-circuit monitor is only effective during PWM-ON state with programmable minimal pulse width greater than $t_{(BLANK)} + t_{(OPEN\_deg)}$. The $t_{(BLANK)}$ is programmed by register BLANK. If PWM on-time is less than $t_{(BLANK)} + t_{(OPEN\_deg)}$, the device does not report any open-circuit fault. When the device supply voltage $V_{(SUPPLY)}$ is below the threshold $V_{(LOWSUPTH)}$ set by register LOWSUPTH, the LED open-circuit fault is not detected nor reported.

When the voltage difference $V_{(SUPPLY)} – V_{(OUTXn)}$ is below threshold $V_{(OPEN\_th\_rising)}$ with duration longer than $t_{(BLANK)} + t_{(OPEN\_deg)}$, and the device supply voltage $V_{(SUPPLY)}$ is above the threshold $V_{(LOWSUPTH)}$, the

TPS929160-Q1 pulls the $\overline{ERR}$ pin down with constant current sink to report fault and set flag registers including FLAG_OPENOUTXn, FLAG_OUT and FLAG_ERR to 1. In FAIL-SAFE state, the TPS929160-Q1 shuts down the normal current regulation and PWM dutycycle for the error output, then the device sources a current $I_{(RETRY)}$ to faulty output every $t_{(SLS\_Retry)}$, 10 ms for retrying. $I_{(RETRY)}$ is programed by IRETRY register. The current $I_{(RETRY)}$ can be calculated with the below equation. When the voltage difference $V_{(SUPPLY)} - V_{(OUTXn)}$ of error output rises above threshold $V_{(OPEN\_th\_rising)}$ with duration longer than $t_{(BLANK)} + t_{(OPEN\_deg)}$, or the supply voltage $V_{(SUPPLY)}$ is above the threshold $V_{(LOWSUPTH)}$, the device automatically resumes the normal current and PWM duty cycle setup and releases the $\overline{ERR}$ pin.

$$I_{(RETRY)} = \frac{IRETRY \times 4 + 4}{64} \times I_{(FULL\_RANGE)} \quad (8)$$

where

- IRETRY is programmable from 0 to 15.
- Use Equation 1 to calculate $I_{(FULL\_RANGE)}$.

The fault is latched in flag registers. When the open-circuit failure is removed, the master controller must write 1 to CLRFAULT to clear FLAG_OPENOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

6.3.8.9 LED Short-Circuit Diagnostics in FAIL-SAFE state

The TPS929160-Q1 has internal analog comparators to monitor all channel outputs with respect to a fixed threshold for reporting OUTXn short to GND fault in FAIL-SAFE state.

The short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of $t_{(BLANK)} + t_{(SHORT\_deg)}$. The $t_{(BLANK)}$ is programmable by register BLANK. If PWM on-time is less than $t_{(BLANK)} + t_{(SHORT\_deg)}$, the device cannot report any short-circuit fault.

When the voltage $V_{(OUTXn)}$ is below threshold $V_{(SG\_th\_rising)}$ with duration longer than deglitch timer length of $t_{(BLANK)} + t_{(SHORT\_deg)}$, the device pulls $\overline{ERR}$ pin down with constant current sink to report fault and set flag registers including FLAG_SHORTOUTXn, FLAG_OUT and FLAG_ERR. In FAIL-SAFE state, the TPS929160-Q1 shuts down the normal current regulation and PWM duty cycle for the faulty output, then the device sources a pulse current to faulty output every $t_{(SLS\_Retry)}$, 10 ms for retrying. $I_{(RETRY)}$ is programed by IRETRY register. Use Equation 8 to calculate the current, $I_{(RETRY)}$. When the voltage $V_{(OUTXn)}$ of error output rises above threshold $V_{(SG\_th\_falling)}$ with duration longer than $t_{(BLANK)} + t_{(SHORT\_deg)}$, the device automatically resumes the normal current and PWM dutycycle setup and releases the $\overline{ERR}$ pin.

The fault is latched in flag registers. When the short-circuit failure is removed, the master controller must write 1 to CLRFAULT to clear FLAG_OPENOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

6.3.8.10 Single-LED Short-Circuit Detection in FAIL-SAFE state

The TPS929160-Q1 also integrates analog comparators to monitor all outputs with respect to two alternative threshold for single-LED short-circuit diagnostic in FAIL-SAFE state. Setting the register SLSEN to 1 enables the single-LED short-circuit detection.

The single-LED short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of $t_{(BLANK)} + t_{(SLS\_deg)}$. The $t_{(BLANK)}$ is programmable by register BLANK. If PWM on-time is less than $t_{(BLANK)} + t_{(SLS\_deg)}$, the device cannot report any single-LED short-circuit fault. When the device supply voltage $V_{(SUPPLY)}$ is below the threshold $V_{(LOWSUPTH)}$ set by register LOWSUPTH, the single-LED short-circuit is not detected nor reported.

When the voltage $V_{(OUTXn)}$ is below threshold $V_{(SLSTHx)}$ with duration longer than deglitch timer length of $t_{(BLANK)} + t_{(SLS\_deg)}$, and the device supply voltage $V_{(SUPPLY)}$ is above the threshold $V_{(LOWSUPTH)}$, the device pulls the $\overline{ERR}$ pin down with constant current sink to report fault and set flag registers including FLAG_SLSOUTXn, FLAG_OUT and FLAG_ERR. The TPS929160-Q1 provides two alternative threshold $V_{(SLSTH0)}$ and $V_{(SLSTH1)}$

for single-LED short-circuit detection selected by SLSTHOUTXn independently for each current output. The $V_{(SLSTH0)}$ is selected for current OUTXn when LSTHOUTXn is set to 0, however $V_{(SLSTH1)}$ is selected when SLSLTHOUTXn is set to 1. The actual voltage value for $V_{(SLSTH0)}$ and $V_{(SLSTH1)}$ is programmable by two 8-bit registers SLSTH0 and SLSTH1 from 2.5 V to 34.375 V at 125-mV interval. In FAIL-SAFE state, the TPS929160-Q1 shuts down the normal current regulation and PWM duty cycle for the faulty output, then the device sources a pulse current, $I_{(OUTXn)}$ programed by IOUTXn register to the faulty output every $t_{(SLS\_Retry)}$, 10 ms for retrying. When the voltage $V_{(OUTXn)}$ of error output rises above threshold $V_{(SLSTHx)}$ + 275 mV with duration longer than $t_{(BLANK)}$ + $t_{(SLS\_deg)}$ during retrying, or the supply voltage $V_{(SUPPLY)}$ is below the threshold $V_{(LOWSUPTH)}$, the device automatically resumes the normal current and PWM dutycycle setup and releases the $\overline{ERR}$ pin.

The fault is latched in flag registers. When the single-LED short-circuit fault is removed, the master controller must write 1 to register CLRFAULT to clear FLAG_SLSOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT automatically returns to 0.

6.3.8.11 EEPROM CRC Error in FAIL-SAFE state

The TPS929160-Q1 automatically reloads all EEPROM code into the corresponding configuration registers every time after entering the FAIL-SAFE state. The TPS929160-Q1 implements a EEPROM CRC check after loading the EEPROM code to configuration register in FAIL-SAFE state. The calculated CRC results are sent to register CALC_EEPCRC and compared to the data in EEPROM register EEPCRC, which stores the CRC code for all EEPROM registers except for DIM-R reserved register. The reserved DIM-R register value is not included in the EEPCRC calculation. The TPS929160-Q1 *EEPROM configuration tool* are available on *ti.com* to help calculate the EEPCRC value. If the code in register CALC_EEPCRC is not matched to the code in register EEPCRC, the TPS929160-Q1 turns off all channels output, pulls the $\overline{ERR}$ pin down with constant current sink to report the fault, and sets the registers including FLAG_EEPCRC and FLAG_ERR to 1. The CRC code for all the EEPROM registers must be burnt into EEPROM register EEPCRC in the end of production line. The CRC code algorithm is described in *EEPROM CRC Error in NORMAL state*.

6.3.8.12 Fault Masking in FAIL-SAFE state

The TPS929160-Q1 provides fault masking capability using masking registers. The device is capable of masking faults by channels or by fault types. The fault masking does not disable diagnostics features but only prevents fault reporting to FLAG_OUT register, FLAG_ERR register, and $\overline{ERR}$ output. The below table gives the detailed description for each fault mask register in NORMAL state.

To disable diagnostics on a single channel in FAIL-SAFE state, burning EEPROM of DIAGENOUTXn registers to 0 disables open-circuit, LED short-circuit and single-LED short-circuit diagnostics of channel x, and thus no fault of this channel is reported to FLAG_OPENOUTXn, FLAG_SHORTOUTXn, FLAG_SLSOUTXn, FLAG_OUT or FLAG_ERR registers, or to the $\overline{ERR}$ output.

Table 6-7. Fault Masking in FAIL-SAFE State

Fault Detected	Mask Register	FLAG Name	$\overline{ERR}$ PIN
Low-supply warning	MASKLOWSUP = 1	FLAG_LOWSUP = 1 FLAG_ERR = 0	No action
	MASKLOWSUP = 0	FLAG_LOWSUP = 1 FLAG_ERR = 1	No action
Supply undervoltage	MASKSUPUV = 1	FLAG_SUPUV = 1 FLAG_ERR = 0	No action
	MASKSUPUV = 0	FLAG_SUPUV = 1 FLAG_ERR = 1	Constant pulled down
Reference fault	MASKREF = 1	FLAG_REF = 1 FLAG_ERR = 0	No action
	MASKREF = 0	FLAG_REF = 1 FLAG_ERR = 1	Constant pulled down
Pre-thermal warning	MASKPRETSD = 1	FLAG_PRETSD = 1 FLAG_ERR = 0	No action
	MASKPRETSD = 0	FLAG_PRETSD = 1 FLAG_ERR = 1	No action

Table 6-7. Fault Masking in FAIL-SAFE State (continued)

Fault Detected	Mask Register	FLAG Name	$\overline{\text{ERR}}$ PIN
Overtemperature protection	MASKTSD = 1	FLAG_TSD = 1 FLAG_ERR = 0	No action
	MASKTSD = 0	FLAG_TSD = 1 FLAG_ERR = 1	Constant pulled down
EEPROM CRC error	MASKEEPCRC = 1	FLAG_EEPCRC = 1 FLAG_ERR = 0	No action
	MASKEEPCRC = 0	FLAG_EEPCRC = 1 FLAG_ERR = 1	Constant pulled down
LED open-circuit fault	MASKOPEN = 1	FLAG_OPENOUTXn = 1 FLAG_OUT = 0 FLAG_ERR = 0	No action
	MASKOPEN = 0	FLAG_OPENOUTXn = 1 FLAG_OUT = 1 FLAG_ERR = 1	Constant pulled down
LED short-circuit fault	MASKSHORT = 1	FLAG_SHORTOUTXn = 1 FLAG_OUT = 0 FLAG_ERR = 0	No action
	MASKSHORT = 0	FLAG_SHORTOUTXn = 1 FLAG_OUT = 1 FLAG_ERR = 1	Constant pulled down
Single LED short-circuit fault	MASKSLS = 1	FLAG_SLSOUTXn = 1 FLAG_OUT = 0 FLAG_ERR = 0	No action
	MASKSLS = 0	FLAG_SLSOUTXn = 1 FLAG_OUT = 1 FLAG_ERR = 1	Constant pulled down

Table 6-8. Diagnostics Table in FAIL-SAFE state

FAULT TYPE	DETECTION CRITERIA	CONDITIONS	FAULT ACTIONS	FAULT OUTPUT	$\overline{ERR}$ PIN	RECOVERY
VBAT UVLO	$V_{(VBAT)} < V_{(POR\_falling)}$ or $V_{(LDO)} < V_{(LDO\_POR\_falling)}$		Device switch to POR state	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLRPOR.
Low-supply warning	$V_{(SUPPLY)} < V_{(LOWSUPTH)}$		Disable fault type *	FLAG_LOWSUP FLAG_ERR (maskable)	No action	Automatically recovery upon fault removal. Clear fault flag with CLRFAULT.
Supply undervoltage	$V_{(SUPPLY)} < V_{(SUPUV\_th\_falling)}$		Turn off all outputs	FLAG_SUPUV FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recovery and release $\overline{ERR}$ pin upon fault removal. Clear fault flag with CLRFAULT.
Reference fault	$V_{(REF)} < V_{(REF\_SHORT\_th)}$ or $I_{(REF)} < I_{(REF\_OPEN\_th)}$		Turn off all outputs	FLAG_REF FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover and release $\overline{ERR}$ pin upon fault removal. Clear fault flags with CLRFAULT.
Pre-thermal warning	$T_{(J)} > T_{(PRETSD)}$		No action	FLAG_PRETSD FLAG_ERR(maskable)	No action	Clear fault flag with CLRFAULT
Overtemperature protection	$T_{(J)} > T_{(TSD1)}$		Turn off all outputs	FLAG_TSD FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover and release $\overline{ERR}$ pin upon fault removal. Clear fault flags with CLRFAULT.
Overtemperature shutdown	$T_{(J)} > T_{(TSD2)}$		Turn off LDO	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLRPOR.
LED open-circuit fault *	$V_{(SUPPLY)} - V_{(OUTXn)} < V_{(OPEN\_th\_rising)}$ and $V_{(SUPPLY)} > V_{(LOWSUPTH)}$	PWM pulse width greater than $t_{(BLANK)} + t_{(OPEN\_deg)}$ ENOUTXn = 1 DIAGENOUTXn = 1	Turn off the failed outputs and retry every 10 ms	FLAG_OPENOUTXn FLAG_OUT (maskable) FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover and release $\overline{ERR}$ pin upon fault removal. Clear fault flags with CLRFAULT.
LED short-circuit fault	$V_{(OUTXn)} < V_{(SG\_th\_rising)}$	PWM pulse width greater than $t_{(BLANK)} + t_{(SHORT\_deg)}$ ENOUTXn = 1 DIAGENOUTXn = 1	Turn off the failed outputs and retry every 10 ms	FLAG_SHORTOUTXn FLAG_OUT (maskable) FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover and release $\overline{ERR}$ pin upon fault removal. Clear fault flags with CLRFAULT.
Auto single-LED short-circuit *	$V_{(OUTXn)} < V_{(SLSTHx)}$ and $V_{(SUPPLY)} > V_{(LOWSUPTH)}$	PWM pulse width greater than $t_{(BLANK)} + t_{(SLS\_deg)}$ ENOUTXn = 1 DIAGENOUTXn = 1 SLSEN = 1	Turn off the failed outputs and retry every 10 ms	FLAG_SLSOUTXn FLAG_OUT (Maskable) FLAG_ERR (Maskable)	Constant pulled down	Automatically recover and release $\overline{ERR}$ pin upon fault removal. Clear fault flags with CLRFAULT.
EEPROM CRC error	CALC_EEPCRC is different EEPCRC		Turn off all outputs	FLAG_EEPCRC FLAG_ERR (maskable)	Constant pulled down (maskable)	Clear fault flag with CLRFAULT

6.3.9 OFAF Setup In FAIL-SAFE state

The TPS929160-Q1 has a unique setup for failure behavior in FAIL-SAFE state. If there is a failure detected in FAIL-SAFE state, the TPS929160-Q1 automatically reacts to the failure. The register OFAF determines whether the result behavior of output failure is one-fails-all-fail or one-fails-others-on.

In FAIL-SAFE state, the TPS929160-Q1 shuts down all enabled current outputs except the faulty output when OFAF is set to 1. Otherwise the TPS929160-Q1 keeps regulation for all enable current outputs except the faulty output when OFAF is set to 0. Table 6-9 provides details.

6.3.10 $\overline{\text{ERR}}$ Output

The $\overline{\text{ERR}}$ pin is a programmable fault indicator pin. This pin can be used as an interrupt output to master controller in case there is any fault in NORMAL state. In FAIL-SAFE states, the $\overline{\text{ERR}}$ pin can be used as an output to other $\overline{\text{ERR}}$ pin of other TPS929160-Q1 to achieve one-fails-all-fail at system level. The $\overline{\text{ERR}}$ pin is an open-drain output with current limit up to $I_{PD(\overline{ERR})}$. TI recommends a < 10-kΩ external pullup resistor from the $\overline{\text{ERR}}$ pin to the same IO voltage of the master controller.

In NORMAL state, when a fault is triggered, depending on the fault type, the $\overline{\text{ERR}}$ pin is either pulled down constantly or pulled down for a single pulse. After an $\overline{\text{ERR}}$ output is triggered, the master controller must take action to deal with the failure and reset the fault flag. For non-critical faults, the TPS929160-Q1 pulls down the $\overline{\text{ERR}}$ pin with a duration of 50 µs and release; for critical faults, device constantly pulls down $\overline{\text{ERR}}$ as described in Table 6-6. In NORMAL state, basically, the TPS929160-Q1 only reports the faults to the master controller for most of the failure and takes no actions except supply or LDO UVLO, reference fault, and overtemperature. The master controller determines what action to take according to the type of the failure.

The TPS929160-Q1 provides a forced-error feature to validate the error feedback-loop integrity in NORMAL state. In NORMAL state, if the microcontroller sets FORCEERR to 1, the FLAG_ERR is set 1 and pulls down $\overline{\text{ERR}}$ output with a pulse of 50 µs accordingly. The FORCEERR automatically returns to 0.

In FAIL-SAFE states, the $\overline{\text{ERR}}$ pin is used as fault bus. When there is any output failure reported, the $\overline{\text{ERR}}$ is pulled down by internal current sink $I_{PD(\overline{ERR})}$. The TPS929160-Q1 monitors the voltage of the $\overline{\text{ERR}}$ pin. If the one-fails-all-fail diagnostics is enabled by setting register OFAF to 1, all current output channels are turned off, as well as diagnostics, when the $\overline{\text{ERR}}$ pin voltage is low. If register OFAF is 0, the device only turns off the failed channel with alive channels diagnostics enabled.

Table 6-9. One-Fails-All-Fail Feature in Fail-Safe State

	OFAF = 1	OFAF = 0
$\overline{\text{ERR}}$ pulled low internally	All OUT channel OFF except failure detected OUT retries every 10 ms	Only failure detected OUT OFF
$\overline{\text{ERR}}$ pulled low externally	All OUT channel OFF	All OUT channel ON

If multiple TPS929160-Q1 devices are used in one application, tying the $\overline{\text{ERR}}$ pins together achieves the one-fails-all-fail behavior in FAIL-SAFE states without master controlling. Any one of TPS929160-Q1 reports fault by pulling the $\overline{\text{ERR}}$ pin to low, and the low voltage on $\overline{\text{ERR}}$ bus is detected by other TPS929160-Q1 as Figure 6-10 illustrated. If the register OFAF is set to 1 for all TPS929160-Q1 devices having the $\overline{\text{ERR}}$ pins tied together, all TPS929160-Q1 devices turn off current for all output channels.

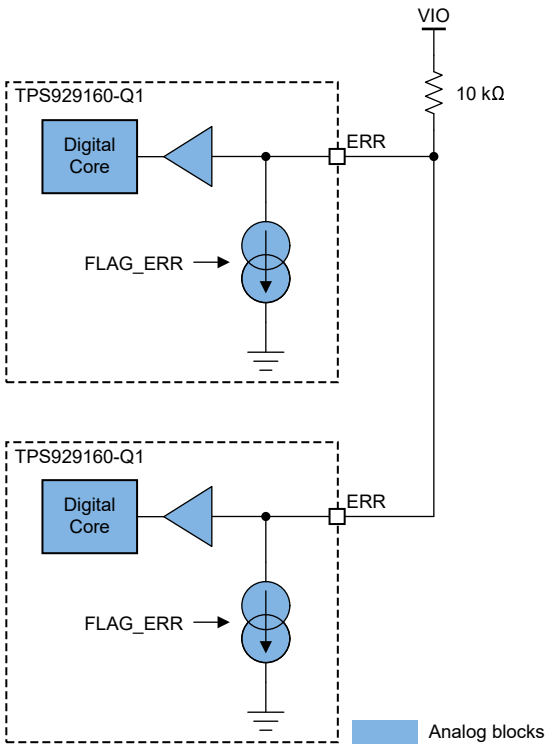


Figure 6-10. $\overline{\text{ERR}}$ Internal Block Diagram

6.4 Device Functional Modes

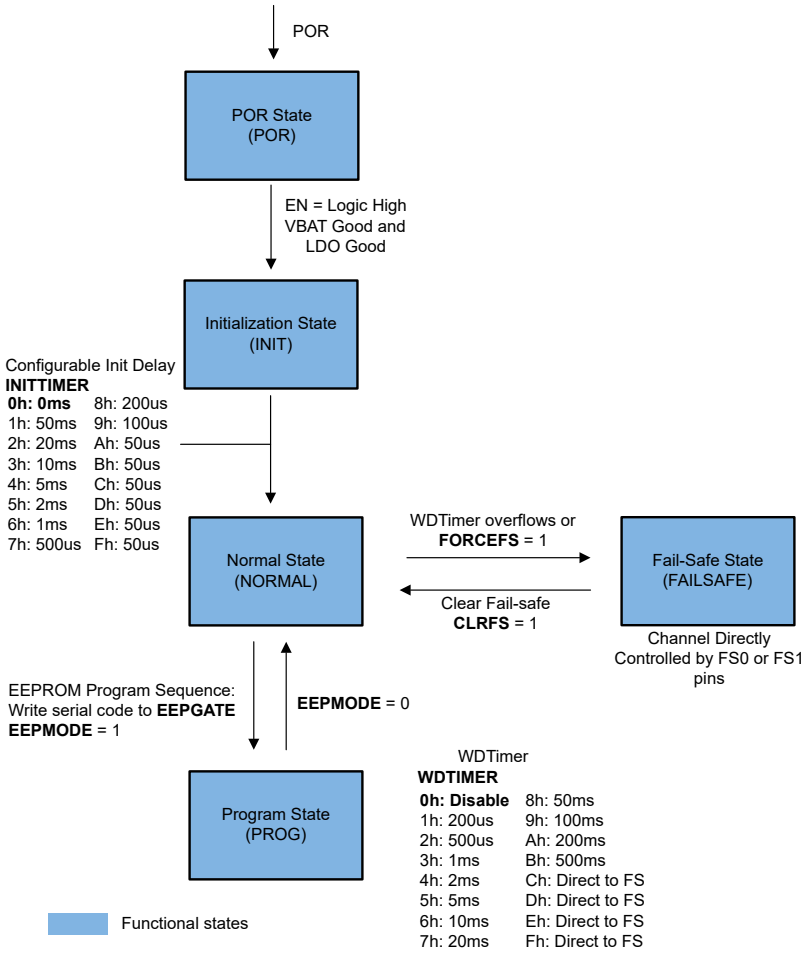


Figure 6-11. Device Functional Mode Statemachine

6.4.1 POR State

Upon power up, the TPS929160-Q1 enters POWER_ON_RESET (POR) state. In this state, registers are cleared to default value, outputs are disabled, and the device cannot be accessed through the FlexWire interface.

After both the VBAT input and the LDO output are above their UVLO threshold, the device switches to INITIALIZATION state (INIT). If any of the supply fails below UVLO threshold or EN pin is pulled low in other states, the device immediately switches to POR state.

6.4.2 INITIALIZATION state

The INITIALIZATION state is designed to allow master controller to have enough time to power up before the device automatically gets into FAIL-SAFE states. INIT mode has a configurable delay programmed by 4-bit register INITTIMER. After the delay counter is reached, the device changes to NORMAL state. In INIT state, the communication between master controller and the TPS929160-Q1 is enabled through FlexWire interface. In INITIALIZATION state, device automatically load register map default values, which can be programmed in corresponding EEPROM. The master controller sets CLRPOR to 1 in INITIALIZATION state, the device immediately switches to NORMAL state. Only write CLRPOR to TPS929160-Q1 in INITIALIZATION state.

6.4.3 NORMAL state

After the TPS929160-Q1 is in NORMAL state, the device operates under master control for LED animation and diagnostics using a FlexWire interface. The TPS929160-Q1 integrates a watchdog timer to monitor the communication on FlexWire. The watchdog timer is programmable by a 4-bit register WDTIMER for 13 options. The timer in TPS929160-Q1 starts to count when there is no instruction received from the master controller. The TPS929160-Q1 enters FAIL-SAFE states when the timer overflows. The device can be also forced into FAIL-SAFE states anytime in NORMAL state by setting FORCEFS to 1. The FORCEFS register automatically returns to 0.

6.4.4 FAIL-SAFE state

When the TPS929160-Q1 is entering FAIL-SAFE state from NORMAL state, all the registers are set to default value or reloaded from EEPROM.

The Flexwire interface keeps alive in FAIL-SAFE state. Setting FORCEFS to 1 forces the device into FAIL-SAFE state from NORMAL state. The TPS929160-Q1 can quit from FAIL-SAFE state to NORMAL state by setting CLRFS to 1 with FLAG_FS register cleared.

6.4.5 PROGRAM state

The TPS929160-Q1 can enter EEPROM PROGRAM state by writing multiple configuration registers to EEPGATE and setting 1 to EEPMODE. For details of getting into PROGRAM state, refer to *EEPROM Programming*.

6.5 Programming

6.5.1 FlexWire Protocol

6.5.1.1 Protocol Overview

The FlexWire is a UART-based protocol supported by most microcontroller units (MCU). Each frame contains multiple bytes started with a synchronization byte. The synchronization byte allows LED drivers to synchronize with master MCU frequency, therefore saving the extra cost on high precision oscillators that are commonly used in UART / CAN interfaces. Each byte has 1 start bit, 8 data bits, 1 stop bit, no parity check. The LSB data follows the start bit as the below figure describes. The FlexWire supports adaptive communication frequency ranging from 10kHz to 1MHz. The protocol supports master-slave with star-connected topology.

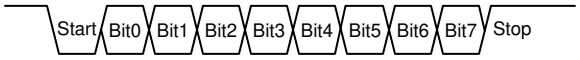


Figure 6-12. One Byte Data Structure

The FlexWire is designed robust for automotive environment. After the slave device receives a communication frame, it firstly verifies its CRC byte. When CRC is verified, the slave device sends out response frame and clears the watchdog timer. In addition, if one communication frame is interrupted in the middle without any bus toggling for a period longer than timeout timer $t_{(DBWTIMER)}$, the TPS929160-Q1 resets the communication and waits for next communication starting from synchronization byte. It is also required for idle period between bytes within $t_{(DBWTIMER)}$. The timeout timer $t_{(DBWTIMER)}$ is programmable by configuration register DBWTIMER. TI recommends using a longer timeout setting for low baud rate communication to avoid unintended timeout and using a shorter timeout setting for high baud rate communication.

If communication CRC check fails, the TPS929160-Q1 ignores the message without sending the feedback. The master does not receive any feedback if the communication is unsuccessful. In this case, the communication can be reset by keeping communication bus idle for $t_{(DBWTIMER)}$, which forces the TPS929160-Q1 to clear its cache and be ready for new communication.

FlexWire supports both write and readback. Both write or readback communication supports burst mode for high throughput and single-byte mode. Figure 6-13 describes the frame structure of a typical single-byte write action. The master frame consists of SYNC, DEV_ADDR, REG_ADDR, DATA and CRC bytes. After CRC is verified, the slave immediately feeds back ACK byte. Figure 6-14 describes the frame structure of a typical single-byte readback action. The master frame consists of SYNC, DEV_ADDR, REG_ADDR, and CRC bytes. After CRC is verified, the slave immediately feeds back DATA and ACK bytes.

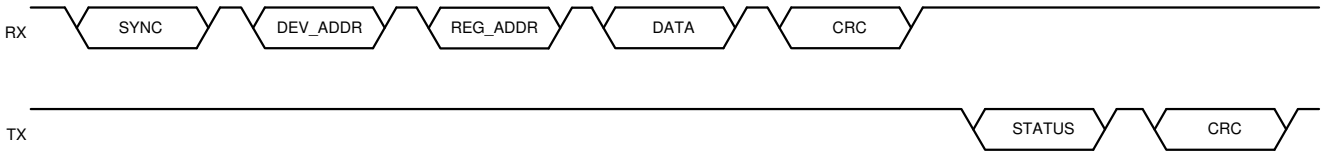


Figure 6-13. Single-Byte Write Command with Status Feedback

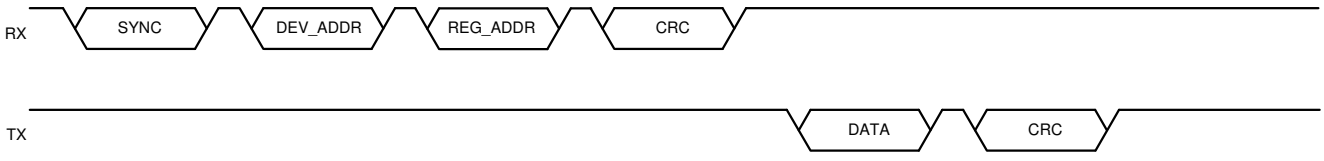


Figure 6-14. Single-Byte Readback Command

Table 6-10. Frame-Byte Description

BYTE NAME	LENGTH (byte)	DESCRIPTION
SYNC	1	Synchronization byte from master
DEV_ADDR	1	Device address bit, r/w, broadcast, burst mode
REG_ADDR	1	Register address
DATA_N	Variable (1, 4, 16, 24)	N-th byte data content
CRC	1	Cyclic redundancy check (CRC) for DEV_ADDR, REG_ADDR and all DATA bytes
STATUS	1	Acknowledgment (Return FLAG_ERR register value)

6.5.1.2 UART Interface Address Setting

Each FlexWire bus supports maximum 16 slave devices. The TPS929160-Q1 has three pinouts including ADDR3, ADDR2, ADDR1, and ADDR0 for slave address configuration. There are additional 4-bit EEPROM register to program the slave address of the TPS929160-Q1. The register INTADDR sets the device slave address by either address pins setup or internal EEPROM register code.

If INTADDR is 1, the device uses the binary code in register DEVADDR[3:0] as slave address as shown in the below table.

If INTADDR is 0, the device uses external inputs on ADDR3, ADDR2, ADDR1 and ADDR0 as shown in Table 6-11 and ignore DEVADDR[3:0] code.

The address 0h to Fh can be used as slave address for up to 16 pieces of TPS929160-Q1 in the same FlexWire bus. Do not have two TPS929160-Q1 sharing the same slave address either setting by internal register DEVADDR or address pins configuration on ADDR3, ADDR2, ADDR1 and ADDR0.

The default value for DEVADDR[3:0] is 0h.

Table 6-11. Device Address Setting

Address(HEX)	INTERNAL ADDRESS SETTING				EXTERNAL ADDRESS SETTING			
	BIT3	BIT2	BIT1	BIT0	BIT3	BIT2	BIT1	BIT0
	DEVADDR[3]	DEVADDR[2]	DEVADDR[1]	DEVADDR[0]	ADDR3	ADDR2	ADDR1	ADDR0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	0	0	1
A	1	0	1	0	1	0	1	0
B	1	0	1	1	1	0	1	1
C	1	1	0	0	1	1	0	0
D	1	1	0	1	1	1	0	1
E	1	1	1	0	1	1	1	0
F	1	1	1	1	1	1	1	1

6.5.1.3 Status Response

When the TPS929160-Q1 as a slave device receives a non-broadcast frame, it first verifies the CRC byte. After CRC check is succeeded, the TPS929160-Q1 sends out the device status of FLAG_ERR register byte followed by CRC byte. The response is disabled by setting register ACKEN to 0. The response sent from TPS929160-Q1 is enabled by default.

Every communication requires CRC verification to make sure the integrity for the data transaction. In broadcast mode, TPS929160-Q1 does not send out a response.

6.5.1.4 Synchronization Byte

The first byte data sent from master controller to TPS929160-Q1 is synchronization frame (SYNC). The master controller sends the clock signal to TPS929160-Q1 through outputting 01010101 binary code in first frame. The TPS929160-Q1 adaptively uses the same clock to communicate with master by synchronization of internal high frequency clock. To avoid clock drift over time, the synchronization byte is always required for each new instruction transaction on FlexWire interface. With this approach, the communication reliability is improved, and the cost for external crystal oscillator is saved. Figure 6-15 is the timing diagram for synchronization frame and device address frame.

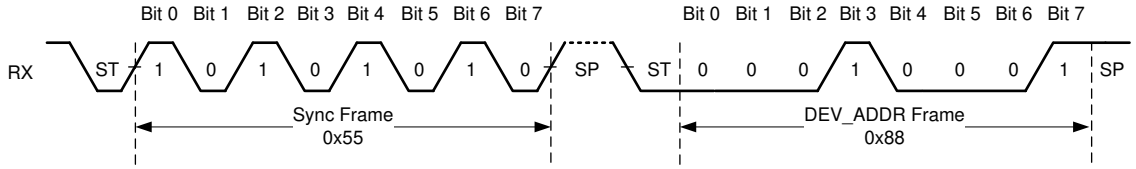


Figure 6-15. Synchronization Byte

6.5.1.5 Device Address Byte

The device address byte, DEV_ADDR frame follows the SYNC frame. There are total 8 bits binary code in the device address byte. The below table provides detailed definition for each bit function. The DEVICE_ADDR register is required to set to 0000b for broadcast mode, otherwise the broadcast mode cannot be enabled. The broadcast mode is only effective for writing mode. The READ/WRITE bit must be 1 for broadcast mode.

Table 6-12. DEV_ADDR Byte

BIT	FIELD	DESCRIPTION
3-0	DEVICE_ADDR	Target device address
5-4	DATA_LENGTH	00b: Single-byte mode with 1 byte of data; 01b: Bust mode with 4 bytes of data; 10b: Burst mode with 16 bytes of data; 11b: Burst mode with 24 bytes of data
6	BROADCAST	Broadcast mode. 1: Broadcast (DEVICE_ADDR =0000b); 0: Single-device only
7	READ/WRITE	Read / Write mode. 1: Write mode; 0: Read mode

6.5.1.6 Register Address Byte

The register address byte, REG_ADDR frame follows the device address frame. There are total 8 bits binary code in register address byte. The maximum allowed register address is 255. The below figure is the timing diagram for register address frame and data frame.

Table 6-13. REG_ADDR Byte

BIT	FIELD	DESCRIPTION
0 - 7	REG_ADDR	Register address

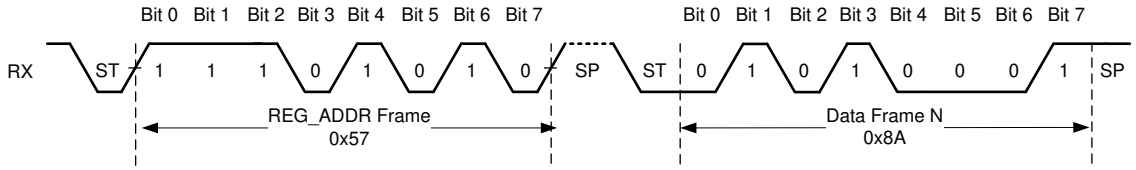


Figure 6-16. Address and Data Bytes

6.5.1.7 Data Frame

The data bytes, data frame follows the register address byte. The TPS929160-Q1 supports single-data-byte, or multiple-data-byte writing in one time data transaction. The number of data byte is defined in the device address byte as introduced in Table 6-12. There are four options including 1 data byte, 4, 16, or 24 data bytes.

Table 6-14. DATA Byte

BIT	FIELD	DESCRIPTION
0 - 7	DATA	Data

6.5.1.8 CRC Frame

The CRC data byte follows the data byte as the final byte in the end of one data transaction to ensure the TPS929160-Q1 correctly receiving all the data bytes from master controller. The master controller must calculate the CRC value for all bytes binary code including device address byte, register address byte, data bytes and sends it to TPS929160-Q1 to end the one time communication. The TPS929160-Q1 receives all bytes data, calculates the CRC and compares the calculated CRC code with received CRC code. If two CRC codes do not match each other, the TPS929160-Q1 ignores the data transaction and waits for the next data transaction without reset FlexWire watchdog timer, WDTIMER. The CRC algorithm is the same to the EEPROM CRC diagnostics as described in *EEPROM CRC Error in NORMAL state*. The initial code for CRC is FFh as well.

Table 6-15. CRC Byte

BIT	FIELD	DESCRIPTION
0 - 7	CRC	CRC Residual

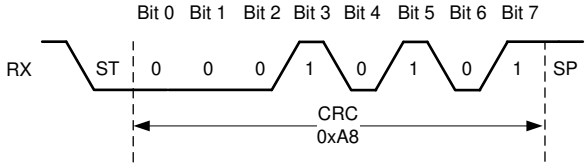


Figure 6-17. CRC Byte

6.5.1.9 Burst Mode

The TPS929160-Q1 with FlexWire protocol supports burst mode for multiple data bytes writing and reading in one data transaction cycle to accelerate the communication between the master controller and slaves. Figure 6-18 shows the data format for multiple data bytes write, and Figure 6-19 shows the data format for multiple data bytes read. The DATA_1 is written to the register in REG_ADDR address, and the following DATA_2 to DATA_N are written to the registers in REG_ADDR+1 to REG_ADDR+N address sequentially for multiple bytes write. For multiple data read, the DATA_1 is read from the register in REG_ADDR address, and the following DATA_2 to DATA_N are read from the registers in REG_ADDR+1 to REG_ADDR+N address sequentially.

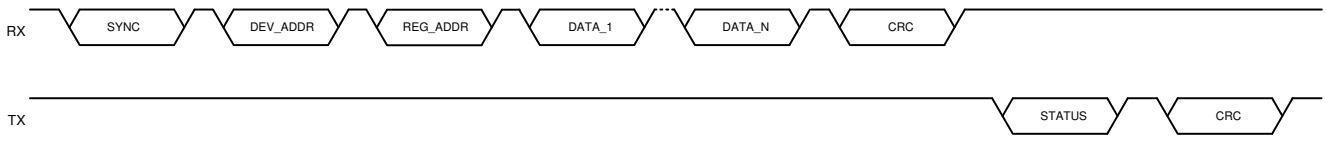


Figure 6-18. Multiple Data Bytes Write in Burst Mode

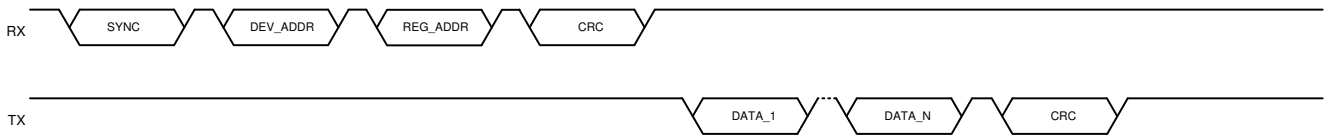


Figure 6-19. Multiple Data Bytes Read in Burst Mode

6.5.2 Registers Lock

The TPS929160-Q1 provides registers content lock feature to prevent unintended modification of registers. There are four register lock bits for different type of registers covering all registers as the below table illustrates. TI recommends locking the register after register writing operations.

Table 6-16. Registers Lock Table

Register IP Name	Address	Lock Register Name	Lock Register Default
BRT (PWMMx)	00h~17h	BRTLOCK	0 (unlock)
BRT (PWMLx)	20h~37h		
BRT	40h~44h		
IOUT	50h~67h	IOUTLOCK	1 (lock)
CONF	70h~83h	CONFLOCK	1 (lock)
CONF	84h~87h	Always locked except in EEPROM program state	
CTRL (ADCCH and CLR)	90h and 91h	No Lock Register	
CTRL	92h~95h	Unlock by sending serial code to CTRLGATE register	
CTRL (CTRLGATE)	96h	No Lock Register	
CTRL (EEP)	97h	Unlock by sending serial code to EEPGATE register	
CTRL (EEPGATE)	98h	No Lock Register	

The below instruction is required to access and exit the CTRL (92h to 95h) register.

- Write 43h, 4Fh, 44h, 45h to 8-bit register CTRLGATE one-byte by one-byte sequentially to access.
- Write any 8-bit data to register CTRLGATE to exit active mode of the CTRL register.
- Write any data to register CTRLGATE also reset LOCK register (93h) to default value.

The below instruction is required to access and exit the EEP (97h) register.

- Write 00h, 04h, 02h, 09h, 02h, 09h to 8-bit register EEPGATE one-byte by one-byte sequentially to access.
- Keep accessible state until write any 8-bit data to register EEPGATE to exit.

6.5.3 Register Default Data

The TPS929160-Q1 has three types of registers. The register IP name BRT with address between 00h to 17h, 20h to 37h and 40h to 44h, have the same set of EEPROM. These registers reset to 00h from POR, EN toggling or setting 1 to REGDEFAULT, and they load the code from the corresponding EEPROM value by the following operations:

- The TPS929160-Q1 enters FAIL-SAFE state by watchdog timer overflow.
- Writing FORCEFS to 1 to force TPS929160-Q1 into FAIL-SAFE state.
- Writing EEPLOAD to 1 to load all corresponding EEPROM content.
- Writing EEPMODE to 1 to enter EEPROM program state.

The register IP name IOUT and CONF with address between 50h to approximately 67h and 70h to approximately 87h, have the same set of EEPROM. These registers always load EEPROM value by the following operation:

- The TPS929160-Q1 starts from POR.
- The TPS929160-Q1 restarts from EN toggled.
- The TPS929160-Q1 restarts from VBAT or LDO UVLO triggered.
- The TPS929160-Q1 enters FAIL-SAFE state by watchdog timer overflow.

- Writing FORCEFS to 1 to force TPS929160-Q1 into FAIL-SAFE state.
- Writing EEPLOAD to 1 to load all corresponding EEPROM content.
- Writing REGDEFAULT to 1 to reset all registers to default code.
- Writing EEPMODE to 1 to enter EEPROM program state.

The register IP name CTRL and FLAG with address between 90h to 98h and A0h to approximately AFh, have no corresponding EEPROM cells. These registers always set to manufacture default value by the following operation:

- The TPS929160-Q1 starts from POR.
- The TPS929160-Q1 restarts from EN toggled.
- The TPS929160-Q1 restarts from VBAT or LDO UVLO triggered.

Table 6-17. Registers Default Value Table

Register IP Name	Register Address	POR Default and SOFTRESET	REGDEFAULT	EEPLOAD	FAIL-SAFE state	EEPMODE
BRT (PWMMx)	00h~17h	00h	00h	Load EEPROM	Load EEPROM	Load EEPROM
BRT (PWMLx)	20h~37h	00h	00h	Load EEPROM	Load EEPROM	Load EEPROM
BRT	40h~44h	00h	00h	Load EEPROM	Load EEPROM	Load EEPROM
IOUT	50~67h	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM
CONF	70h~87h	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM
CTRL	90h~98h	Manufacture default	No action	No action	Only reset 93h to default, no action on other registers	Set 93h to 00h
FLAG	A0~AFh	Manufacture default	Only clear FLAG_POR to 0h and no action on other registers	No action	No action	No action

6.5.4 EEPROM Programming

The TPS929160-Q1 has a user-programmable EEPROM with high reliability for automotive applications. All the EEPROM registers can be burnt through writing the target data into its corresponding register. The TPS929160-Q1 supports two solutions for individual chip selection through pulling the REF pin high or through device address configuration by address pin.

6.5.4.1 Chip Selection by Pulling REF Pin High

The TPS929160-Q1 supports using REF pin as chip-select during EEPROM programming. Considering multiple TPS929160-Q1 devices connected on one FlexWire bus before burning EEPROM, the slave address for all TPS929160-Q1 are all same before programming in case internal EEPROM register DEVADDR is used for slave address setup. The EEPROM burning instruction can be sent to target TPS929160-Q1 by pulling the REF pin of the target TPS929160-Q1 to 5 V. After the REF pin is pulled up to 5 V, the TPS929160-Q1 ignores the device address setup by ADDR3/ADDR2/ADDR1/ADDR0 pins or EEPROM programmed device address in EEP_DEVADDR. The master controller must send out data to target TPS929160-Q1 with device address as 0h and not in broadcast mode.

6.5.4.2 Chip Selection by ADDR Pins Configuration

The TPS929160-Q1 also supports using configuration on ADDR3/ADDR2/ADDR1/ADDR0 pins to determine the slave address for TPS929160-Q1 if multiple TPS929160-Q1 devices are connected on the same FlexWire interface. TI recommends to use this approach for applications of multiple TPS929160-Q1 in the same FlexWire interface. The master controller can send out register data to target TPS929160-Q1 with device address matched to the ADDR3/ADDR2/ADDR1/ADDR0 pins configuration and not in broadcast mode.

6.5.4.3 EEPROM Register Access and Burn

After selecting the target TPS929160-Q1 for EEPROM burning, the master controller must send a serial data bytes to register EEPGATE and set 1 to register EEPMODE one by one in below sequence to finally enable the EEPROM register access. Each data written must be a single-byte operation instead of burst-mode operation.

The chip is selected by pulling REF pin high, below instruction is required to access the EEPROM register.

- Write 09h, 02h, 09h, 02h, 04h, 00h to 8-bit register EEPGATE one-byte by one-byte sequentially.
- Write 1 to 1-bit register EEPMODE

The chip is selected by ADDR pins configuration. The below instruction is required to access the EEPROM register.

- Write 00h, 04h, 02h, 09h, 02h, 09h to 8-bit register EEPGATE one-byte by one-byte sequentially.
- Write 1 to 1-bit register EEPMODE.

The EEPROM registers of the TPS929160-Q1 can be overwritten after the access enabled. The TPS929160-Q1 first loads all data stored in EEPROM to corresponding registers right after entering EEPROM program state. Then the master controller must write the target EEPROM value and the correlated CRC value into its corresponding registers and set EEPPROG to 1 to start the burning of all the EEPROM registers. If DEVADDR[3] or DEVADDR[3:0] is used for addressing and is modified during the EEPROM registers writing process, the device address will be updated immediately. The master should use the new device address for the next frame communication. It is not needed to write target EEPROM value to its corresponding register if the target value EEPROM value is same to its present value, because the EEPROM present value is automatically loaded into its corresponding register after entering the EEPROM PROGRAM state. The data is lost after POR cycle if it is not burnt to EEPROM cell. The EEPPROG automatically returns to 0 at the next clock cycle. The programming takes around 200 ms and flag register FLAG_PROGDONE is 0 during programming. Keep the device power supply stable for at least 200 ms after writing 1 to EEPPROG to make sure solid and robust burning. After programming is done, the FLAG_PROGDONE is automatically set to 1. Figure 6-20 lists the detailed flow chart. The EEPMODE and EEPPROG registers are not writable if the serial codes are not written to EEPGATE one-byte by one-byte sequentially.

The EEPROM cells for TPS929160-Q1 can be overwritten and burnt for up to 1000 times. The one time EEPROM burning is counted after the register EEPPROG is set to 1 even though the EEPROM data is not changed at all.

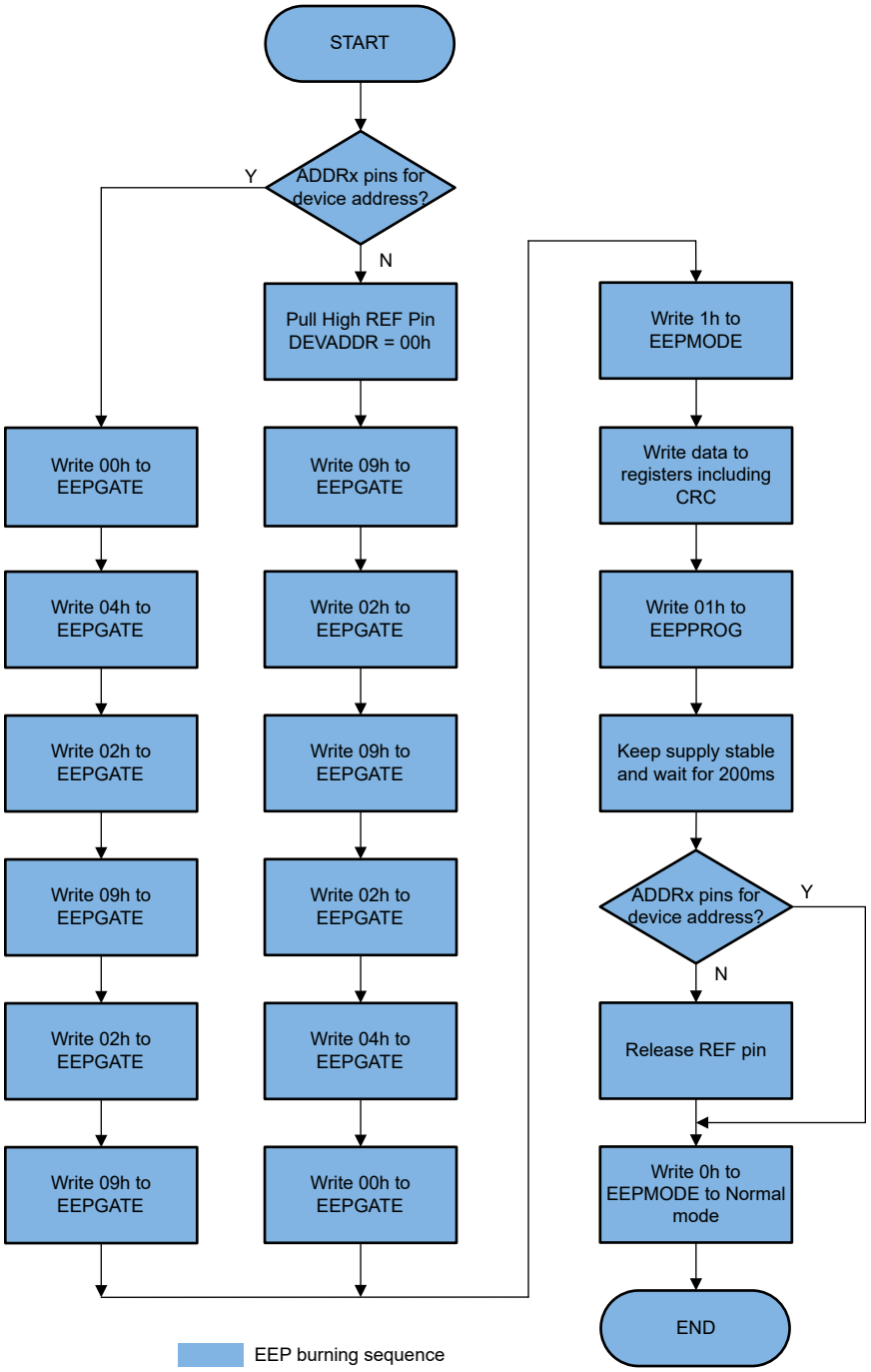


Figure 6-20. Programming Sequence

6.5.4.4 EEPROM PROGRAM state Exit

The REF pin can be released after EEPROM burning if it is pulled high to 5 V for chip selection. The REF pin must be kept high during all of EEPROM PROGRAM state.

The TPS929160-Q1 can quit the EEPROM PROGRAM state to NORMAL state after burning by writing 0 to register EEPMODE. TI recommends reloading the EEPROM data to the registers after EEPROM burning by set 1 to REGDEFAULT.

6.6 Register Maps

CAUTION

All the RESERVED bits in register are set to 0b in TI manufacture. All the RESERVED bits in regester must be written to 0b in case of unavoidable register writing.

Table 6-18. Register Map

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT	EEPROM DEFAULT
00h	PWMMA0	PWMOUTA0								00h	FFh
01h	PWMMA1	PWMOUTA1								00h	FFh
02h	PWMMB0	PWMOUTB0								00h	FFh
03h	PWMMB1	PWMOUTB1								00h	FFh
04h	PWMMC0	PWMOUTC0								00h	FFh
05h	PWMMC1	PWMOUTC1								00h	FFh
06h	PWMMD0	PWMOUTD0								00h	FFh
07h	PWMMD1	PWMOUTD1								00h	FFh
08h	PWMME0	PWMOUTE0								00h	FFh
09h	PWMME1	PWMOUTE1								00h	FFh
0Ah	PWMMF0	PWMOUTF0								00h	FFh
0Bh	PWMMF1	PWMOUTF1								00h	FFh
0Ch	PWMMG0	PWMOUTG0								00h	FFh
0Dh	PWMMG1	PWMOUTG1								00h	FFh
0Eh	PWMMH0	PWMOUTH0								00h	FFh
0Fh	PWMMH1	PWMOUTH1								00h	FFh
10h	PWMMR0	RESERVED								00h	00h
11h	PWMMR1	RESERVED								00h	00h
12h	PWMMR2	RESERVED								00h	00h
13h	PWMMR3	RESERVED								00h	00h
14h	PWMMR4	RESERVED								00h	00h
15h	PWMMR5	RESERVED								00h	00h
16h	PWMMR6	RESERVED								00h	00h
17h	PWMMR7	RESERVED								00h	00h
20h	PWMLA0	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTA0				00h	0Fh

Table 6-18. Register Map (continued)

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT	EEPROM DEFAULT
21h	PWMLA1	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTA1				00h	0Fh
22h	PWMLB0	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTB0				00h	0Fh
23h	PWMLB1	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTB1				00h	0Fh
24h	PWMLC0	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTC0				00h	0Fh
25h	PWMLC1	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTC1				00h	0Fh
26h	PWMLD0	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTD0				00h	0Fh
27h	PWMLD1	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTD1				00h	0Fh
28h	PWMLE0	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTE0				00h	0Fh
29h	PWMLE1	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTE1				00h	0Fh
2Ah	PWMLF0	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTF0				00h	0Fh
2Bh	PWMLF1	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTF1				00h	0Fh
2Ch	PWMLG0	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTG0				00h	0Fh
2Dh	PWMLG1	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTG1				00h	0Fh
2Eh	PWMLH0	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTH0				00h	0Fh
2Fh	PWMLH1	RESERVED	RESERVED	RESERVED	RESERVED	PWMLOWOUTH1				00h	0Fh
30h	PWMLR0	RESERVED								00h	00h
31h	PWMLR1	RESERVED								00h	00h
32h	PWMLR2	RESERVED								00h	00h
33h	PWMLR3	RESERVED								00h	00h
34h	PWMLR4	RESERVED								00h	00h
35h	PWMLR5	RESERVED								00h	00h
36h	PWMLR6	RESERVED								00h	00h
37h	PWMLR7	RESERVED								00h	00h
40h	OUTEN0	RESERVED	RESERVED	ENOUTB1	ENOUTB0	RESERVED	RESERVED	ENOUTA1	ENOUTA0	00h	33h
41h	OUTEN1	RESERVED	RESERVED	ENOUTD1	ENOUTD0	RESERVED	RESERVED	ENOUTC1	ENOUTC0	00h	33h
42h	OUTEN2	RESERVED	RESERVED	ENOUTF1	ENOUTF0	RESERVED	RESERVED	ENOUTE1	ENOUTE0	00h	33h
43h	OUTEN3	RESERVED	RESERVED	ENOUTH1	ENOUTH0	RESERVED	RESERVED	ENOUTG1	ENOUTG0	00h	33h
44h	PWMSHARE	RESERVED	RESERVED	RESERVED	RESERVED	SHAREPWM				00h	00h
50h	IOUTA0	RESERVED	RESERVED	IOUTA0						EEPROM	3Fh
51h	IOUTA1	RESERVED	RESERVED	IOUTA1						EEPROM	3Fh
52h	IOUTB0	RESERVED	RESERVED	IOUTB0						EEPROM	3Fh

Table 6-18. Register Map (continued)

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT	EEPROM DEFAULT
53h	IOUTB1	RESERVED	RESERVED	IOUTB1						EEPROM	3Fh
54h	IOUTC0	RESERVED	RESERVED	IOUTC0						EEPROM	3Fh
55h	IOUTC1	RESERVED	RESERVED	IOUTC1						EEPROM	3Fh
56h	IOUTD0	RESERVED	RESERVED	IOUTD0						EEPROM	3Fh
57h	IOUTD1	RESERVED	RESERVED	IOUTD1						EEPROM	3Fh
58h	IOUTE0	RESERVED	RESERVED	IOUTE0						EEPROM	3Fh
59h	IOUTE1	RESERVED	RESERVED	IOUTE1						EEPROM	3Fh
5Ah	IOUTF0	RESERVED	RESERVED	IOUTF0						EEPROM	3Fh
5Bh	IOUTF1	RESERVED	RESERVED	IOUTF1						EEPROM	3Fh
5Ch	IOUTG0	RESERVED	RESERVED	IOUTG0						EEPROM	3Fh
5Dh	IOUTG1	RESERVED	RESERVED	IOUTG1						EEPROM	3Fh
5Eh	IOUTH0	RESERVED	RESERVED	IOUTH0						EEPROM	3Fh
5Fh	IOUTH1	RESERVED	RESERVED	IOUTH1						EEPROM	3Fh
60h	IOUTAR	RESERVED								EEPROM	00h
61h	IOUTBR	RESERVED								EEPROM	00h
62h	IOUTCR	RESERVED								EEPROM	00h
63h	IOUTDR	RESERVED								EEPROM	00h
64h	IOUTER	RESERVED								EEPROM	00h
65h	IOUTFR	RESERVED								EEPROM	00h
66h	IOUTGR	RESERVED								EEPROM	00h
67h	IOUTHR	RESERVED								EEPROM	00h
70h	DIAGEN0	RESERVED	RESERVED	DIAGENOUTB1	DIAGENOUTB0	RESERVED	RESERVED	DIAGENOUTA1	DIAGENOUTA0	EEPROM	33h
71h	DIAGEN1	RESERVED	RESERVED	DIAGENOUTD1	DIAGENOUTD0	RESERVED	RESERVED	DIAGENOUTC1	DIAGENOUTC0	EEPROM	33h
72h	DIAGEN2	RESERVED	RESERVED	DIAGENOUTF1	DIAGENOUTF0	RESERVED	RESERVED	DIAGENOUTE1	DIAGENOUTE0	EEPROM	33h
73h	DIAGEN3	RESERVED	RESERVED	DIAGENOUTH1	DIAGENOUTH0	RESERVED	RESERVED	DIAGENOUTG1	DIAGENOUTG0	EEPROM	33h
74h	SLSTHSEL0	RESERVED	RESERVED	SLSTHOUTB1	SLSTHOUTB0	RESERVED	RESERVED	SLSTHOUTA1	SLSTHOUTA0	EEPROM	00h
75h	SLSTHSEL1	RESERVED	RESERVED	SLSTHOUTD1	SLSTHOUTD0	RESERVED	RESERVED	SLSTHOUTC1	SLSTHOUTC0	EEPROM	00h
76h	SLSTHSEL2	RESERVED	RESERVED	SLSTHOUTF1	SLSTHOUTF0	RESERVED	RESERVED	SLSTHOUTE1	SLSTHOUTE0	EEPROM	00h
77h	SLSTHSEL3	RESERVED	RESERVED	SLSTHOUTH1	SLSTHOUTH0	RESERVED	RESERVED	SLSTHOUTG1	SLSTHOUTG0	EEPROM	00h

Table 6-18. Register Map (continued)

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT	EEPROM DEFAULT
78h	SLSDAC0	SLSTH0								EEPROM	00h
79h	SLSDAC1	SLSTH1								EEPROM	00h
7Ah	REFERENCE	SLSEN	REFRANGE		LOWSUPTH					EEPROM	60h
7Bh	DIAG	IRETRY				BLANK				EEPROM	00h
7Ch	DIAGMASK	MASKLOWSUP	MASKSUPUV	MASKREF	MASKPRETSD	MASKTSD	MASKEEPCRC	RESERVED	RESERVED	EEPROM	00h
7Dh	OUTMASK	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MASKOPEN	MASKSHORT	MASKSLS	EEPROM	00h
7Eh	DIM	EXPEN	PSEN	12BIT	PSMEN	PWMFREQ				EEPROM	30h
7Fh	DIM-R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	EEPROM	00h
80h	FSMAP0	RESERVED	RESERVED	FSOUTB1	FSOUTB0	RESERVED	RESERVED	FSOUTA1	FSOUTA0	EEPROM	00h
81h	FSMAP1	RESERVED	RESERVED	FSOUTD1	FSOUTD0	RESERVED	RESERVED	FSOUTC1	FSOUTC0	EEPROM	00h
82h	FSMAP2	RESERVED	RESERVED	FSOUTF1	FSOUTF0	RESERVED	RESERVED	FSOUTE1	FSOUTE0	EEPROM	00h
83h	FSMAP3	RESERVED	RESERVED	FSOUTH1	FSOUTH0	RESERVED	RESERVED	FSOUTG1	FSOUTG0	EEPROM	00h
84h	FLEXWIRE0	WDTIMER				DBWTIMER			ACKEN	EEPROM	01h
85h	FLEXWIRE1	RESERVED	RESERVED	RESERVED	INTADDR	DEVADDR				EEPROM	00h
86h	FLEXWIRE2	RESERVED	RESERVED	RESERVED	OFAF	INITTIMER				EEPROM	10h
87h	CRC	EEPCRC								EEPROM	81h
90h	ADCCH	RESERVED	RESERVED	RESERVED	ADCCHSEL					00h	
91h	CLR	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CLRFS	CLRFAULT	CLRPOR	00h	
92h	DEBUG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FORCEFS	FORCEERR	00h	
93h	LOCK	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BRTLOCK	CONFLOCK	IOUTLOCK	03h	
94h	CLRREG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SOFTRESET	EEPLOAD	REGDEFAULT	00h	
95h	NSTB	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	NSTB	00h	
96h	CTRLGATE	CTRLGATE								00h	
97h	EEP	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	EEPPROG	EEPMODE	00h	
98h	EEPGATE	EEPGATE								00h	
A0h	FLAG_ERR	FLAG_LOWSUP	FLAG_SUPUV	FLAG_REF	FLAG_PRETSD	FLAG_TSD	FLAG_EEPCRC	FLAG_OUT	FLAG_ERR	01h	
A1h	FLAG_STATUS	FLAG_EEPPAR	FLAG_EXTFS1	FLAG_EXTFS0	FLAG_PROGDONE	FLAG_FS	FLAG_ADCDONE	FLAG_ADCERR	FLAG_POR	01h	
A2h	FLAG_ADC	ADC_OUT								00h	

Table 6-18. Register Map (continued)

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT	EEPROM DEFAULT
A3h	FLAG_SLS0	RESERVED	RESERVED	FLAG_SLSOUTB1	FLAG_SLSOUTB0	RESERVED	RESERVED	FLAG_SLSOUTA1	FLAG_SLSOUTA0	00h	
A4h	FLAG_SLS1	RESERVED	RESERVED	FLAG_SLSOUTD1	FLAG_SLSOUTD0	RESERVED	RESERVED	FLAG_SLSOUTC1	FLAG_SLSOUTC0	00h	
A5h	FLAG_SLS2	RESERVED	RESERVED	FLAG_SLSOUTF1	FLAG_SLSOUTF0	RESERVED	RESERVED	FLAG_SLSOUTE1	FLAG_SLSOUTE0	00h	
A6h	FLAG_SLS3	RESERVED	RESERVED	FLAG_SLSOUTH1	FLAG_SLSOUTH0	RESERVED	RESERVED	FLAG_SLSOUTG1	FLAG_SLSOUTG0	00h	
A7h	FLAG_OPEN0	RESERVED	RESERVED	FLAG_OPENOUTB1	FLAG_OPENOUTB0	RESERVED	RESERVED	FLAG_OPENOUTA1	FLAG_OPENOUTA0	00h	
A8h	FLAG_OPEN1	RESERVED	RESERVED	FLAG_OPENOUTD1	FLAG_OPENOUTD0	RESERVED	RESERVED	FLAG_OPENOUTC1	FLAG_OPENOUTC0	00h	
A9h	FLAG_OPEN2	RESERVED	RESERVED	FLAG_OPENOUTF1	FLAG_OPENOUTF0	RESERVED	RESERVED	FLAG_OPENOUTE1	FLAG_OPENOUTE0	00h	
AAh	FLAG_OPEN3	RESERVED	RESERVED	FLAG_OPENOUTH1	FLAG_OPENOUTH0	RESERVED	RESERVED	FLAG_OPENOUTG1	FLAG_OPENOUTG0	00h	
ABh	FLAG_SHORT0	RESERVED	RESERVED	FLAG_SHORTOUTB1	FLAG_SHORTOUTB0	RESERVED	RESERVED	FLAG_SHORTOUTA1	FLAG_SHORTOUTA0	00h	
ACh	FLAG_SHORT1	RESERVED	RESERVED	FLAG_SHORTOUTD1	FLAG_SHORTOUTD0	RESERVED	RESERVED	FLAG_SHORTOUTC1	FLAG_SHORTOUTC0	00h	
ADh	FLAG_SHORT2	RESERVED	RESERVED	FLAG_SHORTOUTF1	FLAG_SHORTOUTF0	RESERVED	RESERVED	FLAG_SHORTOUTE1	FLAG_SHORTOUTE0	00h	
AEh	FLAG_SHORT3	RESERVED	RESERVED	FLAG_SHORTOUTH1	FLAG_SHORTOUTH0	RESERVED	RESERVED	FLAG_SHORTOUTG1	FLAG_SHORTOUTG0	00h	
AFh	FLAG_EEPCRC	CALC_EEPCRC								00h	

6.6.1 BRT Registers

Table 6-19 lists the memory-mapped registers for the BRT registers. All register offset addresses not listed in Table 6-19 should be considered as reserved locations and the register contents should not be modified.

Control Register

Table 6-19. BRT Registers

Offset	Acronym	Register Name	Section
0h	PWMMA0	8-MSB Output PWM Duty-cycle Setting for OUTA0	Go
1h	PWMMA1	8-MSB Output PWM Duty-cycle Setting for OUTA1	Go
2h	PWMMB0	8-MSB Output PWM Duty-cycle Setting for OUTB0	Go
3h	PWMMB1	8-MSB Output PWM Duty-cycle Setting for OUTB1	Go
4h	PWMMC0	8-MSB Output PWM Duty-cycle Setting for OUTC0	Go
5h	PWMMC1	8-MSB Output PWM Duty-cycle Setting for OUTC1	Go
6h	PWMMD0	8-MSB Output PWM Duty-cycle Setting for OUTD0	Go
7h	PWMMD1	8-MSB Output PWM Duty-cycle Setting for OUTD1	Go
8h	PWMME0	8-MSB Output PWM Duty-cycle Setting for OUTE0	Go
9h	PWMME1	8-MSB Output PWM Duty-cycle Setting for OUTE1	Go
Ah	PWMMF0	8-MSB Output PWM Duty-cycle Setting for OUTF0	Go
Bh	PWMMF1	8-MSB Output PWM Duty-cycle Setting for OUTF1	Go
Ch	PWMMG0	8-MSB Output PWM Duty-cycle Setting for OUTG0	Go
Dh	PWMMG1	8-MSB Output PWM Duty-cycle Setting for OUTG1	Go
Eh	PWMMH0	8-MSB Output PWM Duty-cycle Setting for OUTH0	Go
Fh	PWMMH1	8-MSB Output PWM Duty-cycle Setting for OUTH1	Go
10h	PWMMR0	Reserved Register	Go
11h	PWMMR1	Reserved Register	Go
12h	PWMMR2	Reserved Register	Go
13h	PWMMR3	Reserved Register	Go
14h	PWMMR4	Reserved Register	Go
15h	PWMMR5	Reserved Register	Go
16h	PWMMR6	Reserved Register	Go
17h	PWMMR7	Reserved Register	Go
20h	PWMLA0	4-LSB Output PWM Duty-cycle Setting for OUTA0	Go
21h	PWMLA1	4-LSB Output PWM Duty-cycle Setting for OUTA1	Go
22h	PWMLB0	4-LSB Output PWM Duty-cycle Setting for OUTB0	Go
23h	PWMLB1	4-LSB Output PWM Duty-cycle Setting for OUTB1	Go
24h	PWMLC0	4-LSB Output PWM Duty-cycle Setting for OUTC0	Go
25h	PWMLC1	4-LSB Output PWM Duty-cycle Setting for OUTC1	Go
26h	PWMLD0	4-LSB Output PWM Duty-cycle Setting for OUTD0	Go
27h	PWMLD1	4-LSB Output PWM Duty-cycle Setting for OUTD1	Go
28h	PWMLE0	4-LSB Output PWM Duty-cycle Setting for OUTE0	Go
29h	PWMLE1	4-LSB Output PWM Duty-cycle Setting for OUTE1	Go
2Ah	PWMLF0	4-LSB Output PWM Duty-cycle Setting for OUTF0	Go
2Bh	PWMLF1	4-LSB Output PWM Duty-cycle Setting for OUTF1	Go
2Ch	PWMLG0	4-LSB Output PWM Duty-cycle Setting for OUTG0	Go
2Dh	PWMLG1	4-LSB Output PWM Duty-cycle Setting for OUTG1	Go
2Eh	PWMLH0	4-LSB Output PWM Duty-cycle Setting for OUTH0	Go
2Fh	PWMLH1	4-LSB Output PWM Duty-cycle Setting for OUTH1	Go

Table 6-19. BRT Registers (continued)

Offset	Acronym	Register Name	Section
30h	PWMLR0	Reserved Register	Go
31h	PWMLR1	Reserved Register	Go
32h	PWMLR2	Reserved Register	Go
33h	PWMLR3	Reserved Register	Go
34h	PWMLR4	Reserved Register	Go
35h	PWMLR5	Reserved Register	Go
36h	PWMLR6	Reserved Register	Go
37h	PWMLR7	Reserved Register	Go
40h	OUTEN0	OUTAn, OUTBn Enable Setting	Go
41h	OUTEN1	OUTCn, OUTDn Enable Setting	Go
42h	OUTEN2	OUTEn, OUTFn Enable Setting	Go
43h	OUTEN3	OUTGn, OUTHn Enable Setting	Go
44h	PWMSHARE	PWM Duty-cycle Sharing for All Enabled Output	Go

Complex bit access types are encoded to fit into small table cells. Table 6-20 shows the codes that are used for access types in this section.

Table 6-20. BRT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.1.1 PWMMA0 Register (Offset = 0h) [Reset = 00h]

PWMMA0 is shown in Figure 6-21 and described in Table 6-21.

Return to the Summary Table.

Figure 6-21. PWMMA0 Register

7	6	5	4	3	2	1	0
PWMOUTA0							
R/W-0h							

Table 6-21. PWMMA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTA0	R/W	0h	8-MSB output PWM duty-cycle setting for OUTA0

6.6.1.2 PWMMA1 Register (Offset = 1h) [Reset = 00h]

PWMMA1 is shown in Figure 6-22 and described in Table 6-22.

Return to the Summary Table.

Figure 6-22. PWMMA1 Register

7	6	5	4	3	2	1	0

Figure 6-22. PWMMA1 Register (continued)

PWMOUTA1
R/W-0h

Table 6-22. PWMMA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTA1	R/W	0h	8-MSB output PWM duty-cycle setting for OUTA1

6.6.1.3 PWMMB0 Register (Offset = 2h) [Reset = 00h]

PWMMB0 is shown in Figure 6-23 and described in Table 6-23.

Return to the Summary Table.

Figure 6-23. PWMMB0 Register

7	6	5	4	3	2	1	0
PWMOUTB0							
R/W-0h							

Table 6-23. PWMMB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTB0	R/W	0h	8-MSB output PWM duty-cycle setting for OUTB0

6.6.1.4 PWMMB1 Register (Offset = 3h) [Reset = 00h]

PWMMB1 is shown in Figure 6-24 and described in Table 6-24.

Return to the Summary Table.

Figure 6-24. PWMMB1 Register

7	6	5	4	3	2	1	0
PWMOUTB1							
R/W-0h							

Table 6-24. PWMMB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTB1	R/W	0h	8-MSB output PWM duty-cycle setting for OUTB1

6.6.1.5 PWMMC0 Register (Offset = 4h) [Reset = 00h]

PWMMC0 is shown in Figure 6-25 and described in Table 6-25.

Return to the Summary Table.

Figure 6-25. PWMMC0 Register

7	6	5	4	3	2	1	0
PWMOUTC0							
R/W-0h							

Table 6-25. PWMMC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTC0	R/W	0h	8-MSB output PWM duty-cycle setting for OUTC0

6.6.1.6 PWMMC1 Register (Offset = 5h) [Reset = 00h]

PWMMC1 is shown in Figure 6-26 and described in Table 6-26.

Return to the Summary Table.

Figure 6-26. PWMMC1 Register

7	6	5	4	3	2	1	0
PWMOUTC1							
R/W-0h							

Table 6-26. PWMMC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTC1	R/W	0h	8-MSB output PWM duty-cycle setting for OUTC1

6.6.1.7 PWMMD0 Register (Offset = 6h) [Reset = 00h]

PWMMD0 is shown in Figure 6-27 and described in Table 6-27.

Return to the Summary Table.

Figure 6-27. PWMMD0 Register

7	6	5	4	3	2	1	0
PWMOUTD0							
R/W-0h							

Table 6-27. PWMMD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTD0	R/W	0h	8-MSB output PWM duty-cycle setting for OUTD0

6.6.1.8 PWMMD1 Register (Offset = 7h) [Reset = 00h]

PWMMD1 is shown in Figure 6-28 and described in Table 6-28.

Return to the Summary Table.

Figure 6-28. PWMMD1 Register

7	6	5	4	3	2	1	0
PWMOUTD1							
R/W-0h							

Table 6-28. PWMMD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTD1	R/W	0h	8-MSB output PWM duty-cycle setting for OUTD1

6.6.1.9 PWMME0 Register (Offset = 8h) [Reset = 00h]

PWMME0 is shown in Figure 6-29 and described in Table 6-29.

Return to the Summary Table.

Figure 6-29. PWMME0 Register

7	6	5	4	3	2	1	0
PWMOUTE0							

Figure 6-29. PWMME0 Register (continued)

R/W-0h

Table 6-29. PWMME0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTE0	R/W	0h	8-MSB output PWM duty-cycle setting for OUTE0

6.6.1.10 PWMME1 Register (Offset = 9h) [Reset = 00h]

PWMME1 is shown in Figure 6-30 and described in Table 6-30.

Return to the Summary Table.

Figure 6-30. PWMME1 Register

7	6	5	4	3	2	1	0
PWMOUTE1							
R/W-0h							

Table 6-30. PWMME1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTE1	R/W	0h	8-MSB output PWM duty-cycle setting for OUTE1

6.6.1.11 PWMMF0 Register (Offset = Ah) [Reset = 00h]

PWMMF0 is shown in Figure 6-31 and described in Table 6-31.

Return to the Summary Table.

Figure 6-31. PWMMF0 Register

7	6	5	4	3	2	1	0
PWMOUTF0							
R/W-0h							

Table 6-31. PWMMF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTF0	R/W	0h	8-MSB output PWM duty-cycle setting for OUTF0

6.6.1.12 PWMMF1 Register (Offset = Bh) [Reset = 00h]

PWMMF1 is shown in Figure 6-32 and described in Table 6-32.

Return to the Summary Table.

Figure 6-32. PWMMF1 Register

7	6	5	4	3	2	1	0
PWMOUTF1							
R/W-0h							

Table 6-32. PWMMF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTF1	R/W	0h	8-MSB output PWM duty-cycle setting for OUTF1

6.6.1.13 PWMMG0 Register (Offset = Ch) [Reset = 00h]

PWMMG0 is shown in Figure 6-33 and described in Table 6-33.

Return to the Summary Table.

Figure 6-33. PWMMG0 Register

7	6	5	4	3	2	1	0
PWMOUTG0							
R/W-0h							

Table 6-33. PWMMG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTG0	R/W	0h	8-MSB output PWM duty-cycle setting for OUTG0

6.6.1.14 PWMMG1 Register (Offset = Dh) [Reset = 00h]

PWMMG1 is shown in Figure 6-34 and described in Table 6-34.

Return to the Summary Table.

Figure 6-34. PWMMG1 Register

7	6	5	4	3	2	1	0
PWMOUTG1							
R/W-0h							

Table 6-34. PWMMG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTG1	R/W	0h	8-MSB output PWM duty-cycle setting for OUTG1

6.6.1.15 PWMMH0 Register (Offset = Eh) [Reset = 00h]

PWMMH0 is shown in Figure 6-35 and described in Table 6-35.

Return to the Summary Table.

Figure 6-35. PWMMH0 Register

7	6	5	4	3	2	1	0
PWMOUTH0							
R/W-0h							

Table 6-35. PWMMH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTH0	R/W	0h	8-MSB output PWM duty-cycle setting for OUTH0

6.6.1.16 PWMMH1 Register (Offset = Fh) [Reset = 00h]

PWMMH1 is shown in Figure 6-36 and described in Table 6-36.

Return to the Summary Table.

Figure 6-36. PWMMH1 Register

7	6	5	4	3	2	1	0
PWMOUTH1							

Figure 6-36. PWMMH1 Register (continued)

R/W-0h

Table 6-36. PWMMH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWMOUTH1	R/W	0h	8-MSB output PWM duty-cycle setting for OUTH1

6.6.1.17 PWMMR0 Register (Offset = 10h) [Reset = 00h]

PWMMR0 is shown in Figure 6-37 and described in Table 6-37.

Return to the Summary Table.

Figure 6-37. PWMMR0 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-37. PWMMR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.18 PWMMR1 Register (Offset = 11h) [Reset = 00h]

PWMMR1 is shown in Figure 6-38 and described in Table 6-38.

Return to the Summary Table.

Figure 6-38. PWMMR1 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-38. PWMMR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.19 PWMMR2 Register (Offset = 12h) [Reset = 00h]

PWMMR2 is shown in Figure 6-39 and described in Table 6-39.

Return to the Summary Table.

Figure 6-39. PWMMR2 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-39. PWMMR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.20 PWMMR3 Register (Offset = 13h) [Reset = 00h]

PWMMR3 is shown in Figure 6-40 and described in Table 6-40.

Return to the Summary Table.

Figure 6-40. PWMMR3 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-40. PWMMR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.21 PWMMR4 Register (Offset = 14h) [Reset = 00h]

PWMMR4 is shown in Figure 6-41 and described in Table 6-41.

Return to the Summary Table.

Figure 6-41. PWMMR4 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-41. PWMMR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.22 PWMMR5 Register (Offset = 15h) [Reset = 00h]

PWMMR5 is shown in Figure 6-42 and described in Table 6-42.

Return to the Summary Table.

Figure 6-42. PWMMR5 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-42. PWMMR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.23 PWMMR6 Register (Offset = 16h) [Reset = 00h]

PWMMR6 is shown in Figure 6-43 and described in Table 6-43.

Return to the Summary Table.

Figure 6-43. PWMMR6 Register

7	6	5	4	3	2	1	0
RESERVED							

Figure 6-43. PWMMR6 Register (continued)

R-0h

Table 6-43. PWMMR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.24 PWMMR7 Register (Offset = 17h) [Reset = 00h]

PWMMR7 is shown in Figure 6-44 and described in Table 6-44.

Return to the Summary Table.

Figure 6-44. PWMMR7 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-44. PWMMR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.25 PWMLA0 Register (Offset = 20h) [Reset = 00h]

PWMLA0 is shown in Figure 6-45 and described in Table 6-45.

Return to the Summary Table.

Figure 6-45. PWMLA0 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTA0			
R-0h				R/W-0h			

Table 6-45. PWMLA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTA0	R/W	0h	4-LSB output PWM duty-cycle setting for OUTA0

6.6.1.26 PWMLA1 Register (Offset = 21h) [Reset = 00h]

PWMLA1 is shown in Figure 6-46 and described in Table 6-46.

Return to the Summary Table.

Figure 6-46. PWMLA1 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTA1			
R-0h				R/W-0h			

Table 6-46. PWMLA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved

Table 6-46. PWMLA1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	PWMLOWOUTA1	R/W	0h	4-LSB output PWM duty-cycle setting for OUTA1

6.6.1.27 PWMLB0 Register (Offset = 22h) [Reset = 00h]

PWMLB0 is shown in Figure 6-47 and described in Table 6-47.

Return to the Summary Table.

Figure 6-47. PWMLB0 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTB0			
R-0h				R/W-0h			

Table 6-47. PWMLB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTB0	R/W	0h	4-LSB output PWM duty-cycle setting for OUTB0

6.6.1.28 PWMLB1 Register (Offset = 23h) [Reset = 00h]

PWMLB1 is shown in Figure 6-48 and described in Table 6-48.

Return to the Summary Table.

Figure 6-48. PWMLB1 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTB1			
R-0h				R/W-0h			

Table 6-48. PWMLB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTB1	R/W	0h	4-LSB output PWM duty-cycle setting for OUTB1

6.6.1.29 PWMLC0 Register (Offset = 24h) [Reset = 00h]

PWMLC0 is shown in Figure 6-49 and described in Table 6-49.

Return to the Summary Table.

Figure 6-49. PWMLC0 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTC0			
R-0h				R/W-0h			

Table 6-49. PWMLC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTC0	R/W	0h	4-LSB output PWM duty-cycle setting for OUTC0

6.6.1.30 PWMLC1 Register (Offset = 25h) [Reset = 00h]

PWMLC1 is shown in Figure 6-50 and described in Table 6-50.

Return to the Summary Table.

Figure 6-50. PWMLC1 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTC1			
R-0h				R/W-0h			

Table 6-50. PWMLC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTC1	R/W	0h	4-LSB output PWM duty-cycle setting for OUTC1

6.6.1.31 PWMLD0 Register (Offset = 26h) [Reset = 00h]

PWMLD0 is shown in Figure 6-51 and described in Table 6-51.

Return to the Summary Table.

Figure 6-51. PWMLD0 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTD0			
R-0h				R/W-0h			

Table 6-51. PWMLD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTD0	R/W	0h	4-LSB output PWM duty-cycle setting for OUTD0

6.6.1.32 PWMLD1 Register (Offset = 27h) [Reset = 00h]

PWMLD1 is shown in Figure 6-52 and described in Table 6-52.

Return to the Summary Table.

Figure 6-52. PWMLD1 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTD1			
R-0h				R/W-0h			

Table 6-52. PWMLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTD1	R/W	0h	4-LSB output PWM duty-cycle setting for OUTD1

6.6.1.33 PWMLE0 Register (Offset = 28h) [Reset = 00h]

PWMLE0 is shown in Figure 6-53 and described in Table 6-53.

Return to the Summary Table.

Figure 6-53. PWMLE0 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTE0			
R-0h				R/W-0h			

Table 6-53. PWMLE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTE0	R/W	0h	4-LSB output PWM duty-cycle setting for OUTE0

6.6.1.34 PWMLE1 Register (Offset = 29h) [Reset = 00h]

PWMLE1 is shown in Figure 6-54 and described in Table 6-54.

Return to the Summary Table.

Figure 6-54. PWMLE1 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTE1			
R-0h				R/W-0h			

Table 6-54. PWMLE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTE1	R/W	0h	4-LSB output PWM duty-cycle setting for OUTE1

6.6.1.35 PWMLF0 Register (Offset = 2Ah) [Reset = 00h]

PWMLF0 is shown in Figure 6-55 and described in Table 6-55.

Return to the Summary Table.

Figure 6-55. PWMLF0 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTF0			
R-0h				R/W-0h			

Table 6-55. PWMLF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTF0	R/W	0h	4-LSB output PWM duty-cycle setting for OUTF0

6.6.1.36 PWMLF1 Register (Offset = 2Bh) [Reset = 00h]

PWMLF1 is shown in Figure 6-56 and described in Table 6-56.

Return to the Summary Table.

Figure 6-56. PWMLF1 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTF1			
R-0h				R/W-0h			

Figure 6-56. PWMLF1 Register (continued)

Table 6-56. PWMLF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTF1	R/W	0h	4-LSB output PWM duty-cycle setting for OUTF1

6.6.1.37 PWMLG0 Register (Offset = 2Ch) [Reset = 00h]

PWMLG0 is shown in Figure 6-57 and described in Table 6-57.

Return to the Summary Table.

Figure 6-57. PWMLG0 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTG0			
R-0h				R/W-0h			

Table 6-57. PWMLG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTG0	R/W	0h	4-LSB output PWM duty-cycle setting for OUTG0

6.6.1.38 PWMLG1 Register (Offset = 2Dh) [Reset = 00h]

PWMLG1 is shown in Figure 6-58 and described in Table 6-58.

Return to the Summary Table.

Figure 6-58. PWMLG1 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTG1			
R-0h				R/W-0h			

Table 6-58. PWMLG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTG1	R/W	0h	4-LSB output PWM duty-cycle setting for OUTG1

6.6.1.39 PWMLH0 Register (Offset = 2Eh) [Reset = 00h]

PWMLH0 is shown in Figure 6-59 and described in Table 6-59.

Return to the Summary Table.

Figure 6-59. PWMLH0 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTH0			
R-0h				R/W-0h			

Table 6-59. PWMLH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved

Table 6-59. PWMLH0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	PWMLOWOUTH0	R/W	0h	4-LSB output PWM duty-cycle setting for OUTH0

6.6.1.40 PWMLH1 Register (Offset = 2Fh) [Reset = 00h]

PWMLH1 is shown in Figure 6-60 and described in Table 6-60.

Return to the Summary Table.

Figure 6-60. PWMLH1 Register

7	6	5	4	3	2	1	0
RESERVED				PWMLOWOUTH1			
R-0h				R/W-0h			

Table 6-60. PWMLH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	PWMLOWOUTH1	R/W	0h	4-LSB output PWM duty-cycle setting for OUTH1

6.6.1.41 PWMLR0 Register (Offset = 30h) [Reset = 00h]

PWMLR0 is shown in Figure 6-61 and described in Table 6-61.

Return to the Summary Table.

Figure 6-61. PWMLR0 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-61. PWMLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.42 PWMLR1 Register (Offset = 31h) [Reset = 00h]

PWMLR1 is shown in Figure 6-62 and described in Table 6-62.

Return to the Summary Table.

Figure 6-62. PWMLR1 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-62. PWMLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.43 PWMLR2 Register (Offset = 32h) [Reset = 00h]

PWMLR2 is shown in Figure 6-63 and described in Table 6-63.

Return to the Summary Table.

Figure 6-63. PWMLR2 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-63. PWMLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.44 PWMLR3 Register (Offset = 33h) [Reset = 00h]

PWMLR3 is shown in Figure 6-64 and described in Table 6-64.

Return to the Summary Table.

Figure 6-64. PWMLR3 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-64. PWMLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.45 PWMLR4 Register (Offset = 34h) [Reset = 00h]

PWMLR4 is shown in Figure 6-65 and described in Table 6-65.

Return to the Summary Table.

Figure 6-65. PWMLR4 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-65. PWMLR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.46 PWMLR5 Register (Offset = 35h) [Reset = 00h]

PWMLR5 is shown in Figure 6-66 and described in Table 6-66.

Return to the Summary Table.

Figure 6-66. PWMLR5 Register

7	6	5	4	3	2	1	0
RESERVED							

Figure 6-66. PWMLR5 Register (continued)

R-0h

Table 6-66. PWMLR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.47 PWMLR6 Register (Offset = 36h) [Reset = 00h]

PWMLR6 is shown in Figure 6-67 and described in Table 6-67.

Return to the Summary Table.

Figure 6-67. PWMLR6 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-67. PWMLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.48 PWMLR7 Register (Offset = 37h) [Reset = 00h]

PWMLR7 is shown in Figure 6-68 and described in Table 6-68.

Return to the Summary Table.

Figure 6-68. PWMLR7 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-68. PWMLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.1.49 OUTEN0 Register (Offset = 40h) [Reset = 00h]

OUTEN0 is shown in Figure 6-69 and described in Table 6-69.

Return to the Summary Table.

Figure 6-69. OUTEN0 Register

7	6	5	4	3	2	1	0
RESERVED		ENOUTB1	ENOUTB0	RESERVED		ENOUTA1	ENOUTA0
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 6-69. OUTEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved

Table 6-69. OUTEN0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ENOUTB1	R/W	0h	Enable register for OUTB1 0h = Disabled 1h = Enabled
4	ENOUTB0	R/W	0h	Enable register for OUTB0 0h = Disabled 1h = Enabled
3-2	RESERVED	R	0h	Reserved
1	ENOUTA1	R/W	0h	Enable register for OUTA1 0h = Disabled 1h = Enabled
0	ENOUTA0	R/W	0h	Enable register for OUTA0 0h = Disabled 1h = Enabled

6.6.1.50 OUTEN1 Register (Offset = 41h) [Reset = 00h]

OUTEN1 is shown in Figure 6-70 and described in Table 6-70.

Return to the Summary Table.

Figure 6-70. OUTEN1 Register

7	6	5	4	3	2	1	0
RESERVED		ENOUTD1	ENOUTD0	RESERVED		ENOUTC1	ENOUTC0
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 6-70. OUTEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	ENOUTD1	R/W	0h	Enable register for OUTD1 0h = Disabled 1h = Enabled
4	ENOUTD0	R/W	0h	Enable register for OUTD0 0h = Disabled 1h = Enabled
3-2	RESERVED	R	0h	Reserved
1	ENOUTC1	R/W	0h	Enable register for OUTC1 0h = Disabled 1h = Enabled
0	ENOUTC0	R/W	0h	Enable register for OUTC0 0h = Disabled 1h = Enabled

6.6.1.51 OUTEN2 Register (Offset = 42h) [Reset = 00h]

OUTEN2 is shown in Figure 6-71 and described in Table 6-71.

Return to the Summary Table.

Figure 6-71. OUTEN2 Register

7	6	5	4	3	2	1	0
RESERVED		ENOUTF1	ENOUTF0	RESERVED		ENOUTE1	ENOUTE0
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 6-71. OUTEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	ENOUTF1	R/W	0h	Enable register for OUTF1 0h = Disabled 1h = Enabled
4	ENOUTF0	R/W	0h	Enable register for OUTF0 0h = Disabled 1h = Enabled
3-2	RESERVED	R	0h	Reserved
1	ENOUTE1	R/W	0h	Enable register for OUTE1 0h = Disabled 1h = Enabled
0	ENOUTE0	R/W	0h	Enable register for OUTE0 0h = Disabled 1h = Enabled

6.6.1.52 OUTEN3 Register (Offset = 43h) [Reset = 00h]

OUTEN3 is shown in Figure 6-72 and described in Table 6-72.

Return to the Summary Table.

Figure 6-72. OUTEN3 Register

7	6	5	4	3	2	1	0
RESERVED		ENOUTH1	ENOUTH0	RESERVED		ENOUTG1	ENOUTG0
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 6-72. OUTEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	ENOUTH1	R/W	0h	Enable register for OUTH1 0h = Disabled 1h = Enabled
4	ENOUTH0	R/W	0h	Enable register for OUTH0 0h = Disabled 1h = Enabled
3-2	RESERVED	R	0h	Reserved
1	ENOUTG1	R/W	0h	Enable register for OUTG1 0h = Disabled 1h = Enabled
0	ENOUTG0	R/W	0h	Enable register for OUTG0 0h = Disabled 1h = Enabled

6.6.1.53 PWMSHARE Register (Offset = 44h) [Reset = 00h]

PWMSHARE is shown in Figure 6-73 and described in Table 6-73.

Return to the Summary Table.

Figure 6-73. PWMSHARE Register

7	6	5	4	3	2	1	0
RESERVED				SHAREPWM			
R-0h				R/W-0h			

Figure 6-73. PWMSHARE Register (continued)

Table 6-73. PWMSHARE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	SHAREPWM	R/W	0h	Set all Output PWM duty-cyce same to OUTA0 0~Eh = Each output PWM duty-cycle is set independently Fh = All output PWM duty-cycle set to same to OUTA0

6.6.2 IOUT Registers

Table 6-74 lists the memory-mapped registers for the IOUT registers. All register offset addresses not listed in Table 6-74 should be considered as reserved locations and the register contents should not be modified.

Output Current Setting

Table 6-74. IOUT Registers

Offset	Acronym	Register Name	Section
50h	IOUTA0	Output Current Setting for OUTA0	Go
51h	IOUTA1	Output Current Setting for OUTA1	Go
52h	IOUTB0	Output Current Setting for OUTB0	Go
53h	IOUTB1	Output Current Setting for OUTB1	Go
54h	IOUTC0	Output Current Setting for OUTC0	Go
55h	IOUTC1	Output Current Setting for OUTC1	Go
56h	IOUTD0	Output Current Setting for OUTD0	Go
57h	IOUTD1	Output Current Setting for OUTD1	Go
58h	IOUTE0	Output Current Setting for OUTE0	Go
59h	IOUTE1	Output Current Setting for OUTE1	Go
5Ah	IOUTF0	Output Current Setting for OUTF0	Go
5Bh	IOUTF1	Output Current Setting for OUTF1	Go
5Ch	IOUTG0	Output Current Setting for OUTG0	Go
5Dh	IOUTG1	Output Current Setting for OUTG1	Go
5Eh	IOUTH0	Output Current Setting for OUTH0	Go
5Fh	IOUTH1	Output Current Setting for OUTH1	Go
60h	IOUTAR	Reserved Register	Go
61h	IOUTBR	Reserved Register	Go
62h	IOUTCR	Reserved Register	Go
63h	IOUTDR	Reserved Register	Go
64h	IOUTER	Reserved Register	Go
65h	IOUTFR	Reserved Register	Go
66h	IOUTGR	Reserved Register	Go
67h	IOUTHR	Reserved Register	Go

Complex bit access types are encoded to fit into small table cells. Table 6-75 shows the codes that are used for access types in this section.

Table 6-75. IOUT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.2.1 IOUTA0 Register (Offset = 50h) [Reset = X]

IOUTA0 is shown in Figure 6-74 and described in Table 6-76.

Return to the Summary Table.

Figure 6-74. IOUTA0 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTA0			
R-0h				R/W-X			

Table 6-76. IOUTA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTA0	R/W	X	Output current setting for OUTA0 Load EEPROM register data when reset

6.6.2.2 IOUTA1 Register (Offset = 51h) [Reset = X]

IOUTA1 is shown in Figure 6-75 and described in Table 6-77.

Return to the Summary Table.

Figure 6-75. IOUTA1 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTA1			
R-0h				R/W-X			

Table 6-77. IOUTA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTA1	R/W	X	Output current setting for OUTA1 Load EEPROM register data when reset

6.6.2.3 IOUTB0 Register (Offset = 52h) [Reset = X]

IOUTB0 is shown in Figure 6-76 and described in Table 6-78.

Return to the Summary Table.

Figure 6-76. IOUTB0 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTB0			
R-0h				R/W-X			

Table 6-78. IOUTB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTB0	R/W	X	Output current setting for OUTB0 Load EEPROM register data when reset

6.6.2.4 IOUTB1 Register (Offset = 53h) [Reset = X]

IOUTB1 is shown in Figure 6-77 and described in Table 6-79.

Return to the Summary Table.

Figure 6-77. IOUTB1 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTB1			
R-0h				R/W-X			

Table 6-79. IOUTB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTB1	R/W	X	Output current setting for OUTB1 Load EEPROM register data when reset

6.6.2.5 IOUTC0 Register (Offset = 54h) [Reset = X]

IOUTC0 is shown in Figure 6-78 and described in Table 6-80.

Return to the Summary Table.

Figure 6-78. IOUTC0 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTC0			
R-0h				R/W-X			

Table 6-80. IOUTC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTC0	R/W	X	Output current setting for OUTC0 Load EEPROM register data when reset

6.6.2.6 IOUTC1 Register (Offset = 55h) [Reset = X]

IOUTC1 is shown in Figure 6-79 and described in Table 6-81.

Return to the Summary Table.

Figure 6-79. IOUTC1 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTC1			
R-0h				R/W-X			

Table 6-81. IOUTC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTC1	R/W	X	Output current setting for OUTC1 Load EEPROM register data when reset

6.6.2.7 IOUTD0 Register (Offset = 56h) [Reset = X]

IOUTD0 is shown in Figure 6-80 and described in Table 6-82.

Return to the Summary Table.

Figure 6-80. IOUTD0 Register

7	6	5	4	3	2	1	0

Figure 6-80. IOUTD0 Register (continued)

RESERVED	IOUTD0
R-0h	R/W-X

Table 6-82. IOUTD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTD0	R/W	X	Output current setting for OUTD0 Load EEPROM register data when reset

6.6.2.8 IOUTD1 Register (Offset = 57h) [Reset = X]

IOUTD1 is shown in Figure 6-81 and described in Table 6-83.

Return to the Summary Table.

Figure 6-81. IOUTD1 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTD1			
R-0h				R/W-X			

Table 6-83. IOUTD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTD1	R/W	X	Output current setting for OUTD1 Load EEPROM register data when reset

6.6.2.9 IOUTE0 Register (Offset = 58h) [Reset = X]

IOUTE0 is shown in Figure 6-82 and described in Table 6-84.

Return to the Summary Table.

Figure 6-82. IOUTE0 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTE0			
R-0h				R/W-X			

Table 6-84. IOUTE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTE0	R/W	X	Output current setting for OUTE0 Load EEPROM register data when reset

6.6.2.10 IOUTE1 Register (Offset = 59h) [Reset = X]

IOUTE1 is shown in Figure 6-83 and described in Table 6-85.

Return to the Summary Table.

Figure 6-83. IOUTE1 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTE1			

Figure 6-83. IOUTE1 Register (continued)

R-0h	R/W-X

Table 6-85. IOUTE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTE1	R/W	X	Output current setting for OUTE1 Load EEPROM register data when reset

6.6.2.11 IOUTF0 Register (Offset = 5Ah) [Reset = X]

IOUTF0 is shown in Figure 6-84 and described in Table 6-86.

Return to the Summary Table.

Figure 6-84. IOUTF0 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTF0			
R-0h				R/W-X			

Table 6-86. IOUTF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTF0	R/W	X	Output current setting for OUTF0 Load EEPROM register data when reset

6.6.2.12 IOUTF1 Register (Offset = 5Bh) [Reset = X]

IOUTF1 is shown in Figure 6-85 and described in Table 6-87.

Return to the Summary Table.

Figure 6-85. IOUTF1 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTF1			
R-0h				R/W-X			

Table 6-87. IOUTF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTF1	R/W	X	Output current setting for OUTF1 Load EEPROM register data when reset

6.6.2.13 IOUTG0 Register (Offset = 5Ch) [Reset = X]

IOUTG0 is shown in Figure 6-86 and described in Table 6-88.

Return to the Summary Table.

Figure 6-86. IOUTG0 Register

7	6	5	4	3	2	1	0
RESERVED				IOUTG0			
R-0h				R/W-X			

Figure 6-86. IOUTG0 Register (continued)

Table 6-88. IOUTG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTG0	R/W	X	Output current setting for OUTG0 Load EEPROM register data when reset

6.6.2.14 IOUTG1 Register (Offset = 5Dh) [Reset = X]

IOUTG1 is shown in Figure 6-87 and described in Table 6-89.

Return to the Summary Table.

Figure 6-87. IOUTG1 Register

7	6	5	4	3	2	1	0
RESERVED		IOUTG1					
R-0h		R/W-X					

Table 6-89. IOUTG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTG1	R/W	X	Output current setting for OUTG1 Load EEPROM register data when reset

6.6.2.15 IOUTH0 Register (Offset = 5Eh) [Reset = X]

IOUTH0 is shown in Figure 6-88 and described in Table 6-90.

Return to the Summary Table.

Figure 6-88. IOUTH0 Register

7	6	5	4	3	2	1	0
RESERVED		IOUTH0					
R-0h		R/W-X					

Table 6-90. IOUTH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTH0	R/W	X	Output current setting for OUTH0 Load EEPROM register data when reset

6.6.2.16 IOUTH1 Register (Offset = 5Fh) [Reset = X]

IOUTH1 is shown in Figure 6-89 and described in Table 6-91.

Return to the Summary Table.

Figure 6-89. IOUTH1 Register

7	6	5	4	3	2	1	0
RESERVED		IOUTH1					
R-0h		R/W-X					

Table 6-91. IOUTH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	IOUTH1	R/W	X	Output current setting for OUTH1 Load EEPROM register data when reset

6.6.2.17 IOUTAR Register (Offset = 60h) [Reset = 00h]

IOUTAR is shown in Figure 6-90 and described in Table 6-92.

Return to the Summary Table.

Figure 6-90. IOUTAR Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-92. IOUTAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.2.18 IOUTBR Register (Offset = 61h) [Reset = 00h]

IOUTBR is shown in Figure 6-91 and described in Table 6-93.

Return to the Summary Table.

Figure 6-91. IOUTBR Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-93. IOUTBR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.2.19 IOUTCR Register (Offset = 62h) [Reset = 00h]

IOUTCR is shown in Figure 6-92 and described in Table 6-94.

Return to the Summary Table.

Figure 6-92. IOUTCR Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-94. IOUTCR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.2.20 IOUTDR Register (Offset = 63h) [Reset = 00h]

IOUTDR is shown in Figure 6-93 and described in Table 6-95.

Return to the Summary Table.

Figure 6-93. IOUTDR Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-95. IOUTDR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.2.21 IOUTER Register (Offset = 64h) [Reset = 00h]

IOUTER is shown in Figure 6-94 and described in Table 6-96.

Return to the Summary Table.

Figure 6-94. IOUTER Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-96. IOUTER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.2.22 IOUTFR Register (Offset = 65h) [Reset = 00h]

IOUTFR is shown in Figure 6-95 and described in Table 6-97.

Return to the Summary Table.

Figure 6-95. IOUTFR Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-97. IOUTFR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.2.23 IOUTGR Register (Offset = 66h) [Reset = 00h]

IOUTGR is shown in Figure 6-96 and described in Table 6-98.

Return to the Summary Table.

Figure 6-96. IOUTGR Register

7	6	5	4	3	2	1	0
RESERVED							

Figure 6-96. IOUTGR Register (continued)

R-0h

Table 6-98. IOUTGR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.2.24 IOUTHR Register (Offset = 67h) [Reset = 00h]

IOUTHR is shown in Figure 6-97 and described in Table 6-99.

Return to the Summary Table.

Figure 6-97. IOUTHR Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-99. IOUTHR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.3 CONF Registers

Table 6-100 lists the memory-mapped registers for the CONF registers. All register offset addresses not listed in Table 6-100 should be considered as reserved locations and the register contents should not be modified.

Configuration Register

Table 6-100. CONF Registers

Offset	Acronym	Register Name	Section
70h	DIAGEN0	OUTAn, OUTBn Diagnostics Enable Setting	Go
71h	DIAGEN1	OUTCn, OUTDn Diagnostics Enable Setting	Go
72h	DIAGEN2	OUTEn, OUTFn Diagnostics Enable Setting	Go
73h	DIAGEN3	OUTGn, OUTHn Diagnostics Enable Setting	Go
74h	SLSTHSEL0	OUTAn, OUTBn Single-LED Short Threshold Selecting	Go
75h	SLSTHSEL1	OUTCn, OUTDn Single-LED Short Threshold Selecting	Go
76h	SLSTHSEL2	OUTEn, OUTFn Single-LED Short Threshold Selecting	Go
77h	SLSTHSEL3	OUTGn, OUTHn Single-LED Short Threshold Selecting	Go
78h	SLSDAC0	Single-LED Short Threshold0 Setting	Go
79h	SLSDAC1	Single-LED Short Threshold1 Setting	Go
7Ah	REFERENCE	Reference Setting	Go
7Bh	DIAG	Diagnostics Setting	Go
7Ch	DIAGMASK	Diagnostics Mask Setting	Go
7Dh	OUTMASK	OUTXn Diagnostics Mask Setting	Go
7Eh	DIM	Dimming Parameter Setting	Go
7Fh	DIM-R	Reserved Register	Go
80h	FSMAP0	OUTAn, OUTBn Fail-safe Mapping Setting	Go
81h	FSMAP1	OUTCn, OUTDn Fail-safe Mapping Setting	Go
82h	FSMAP2	OUTEn, OUTFn Fail-safe Mapping Setting	Go
83h	FSMAP3	OUTGn, OUTHn Fail-safe Mapping Setting	Go
84h	FLEXWIRE0	FlewWire Parameter Setting	Go
85h	FLEXWIRE1	FlewWire Parameter Setting	Go
86h	FLEXWIRE2	FlewWire Parameter Setting	Go
87h	CRC	EEPROM CRC	Go

Complex bit access types are encoded to fit into small table cells. Table 6-101 shows the codes that are used for access types in this section.

Table 6-101. CONF Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.3.1 DIAGEN0 Register (Offset = 70h) [Reset = X]

DIAGEN0 is shown in Figure 6-98 and described in Table 6-102.

Return to the Summary Table.

Figure 6-98. DIAGEN0 Register

7	6	5	4	3	2	1	0
RESERVED		DIAGENOUTB1	DIAGENOUTB0	RESERVED		DIAGENOUTA1	DIAGENOUTA0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-102. DIAGEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	DIAGENOUTB1	R/W	X	Diagnostics enable register for OUTB1 Load EEPROM data when reset 0h = Disabled 1h = Enabled
4	DIAGENOUTB0	R/W	X	Diagnostics enable register for OUTB0 Load EEPROM data when reset 0h = Disabled 1h = Enabled
3-2	RESERVED	R	0h	Reserved
1	DIAGENOUTA1	R/W	X	Diagnostics enable register for OUTA1 Load EEPROM data when reset 0h = Disabled 1h = Enabled
0	DIAGENOUTA0	R/W	X	Diagnostics enable register for OUTA0 Load EEPROM data when reset 0h = Disabled 1h = Enabled

6.6.3.2 DIAGEN1 Register (Offset = 71h) [Reset = X]

DIAGEN1 is shown in Figure 6-99 and described in Table 6-103.

Return to the Summary Table.

Figure 6-99. DIAGEN1 Register

7	6	5	4	3	2	1	0
RESERVED		DIAGENOUTD1	DIAGENOUTD0	RESERVED		DIAGENOUTC1	DIAGENOUTC0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-103. DIAGEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	DIAGENOUTD1	R/W	X	Diagnostics enable register for OUTD1 Load EEPROM data when reset 0h = Disabled 1h = Enabled
4	DIAGENOUTD0	R/W	X	Diagnostics enable register for OUTD0 Load EEPROM data when reset 0h = Disabled 1h = Enabled
3-2	RESERVED	R	0h	Reserved
1	DIAGENOUTC1	R/W	X	Diagnostics enable register for OUTC1 Load EEPROM data when reset 0h = Disabled 1h = Enabled

Table 6-103. DIAGEN1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DIAGENOUTC0	R/W	X	Diagnostics enable register for OUTC0 Load EEPROM data when reset 0h = Disabled 1h = Enabled

6.6.3.3 DIAGEN2 Register (Offset = 72h) [Reset = X]

DIAGEN2 is shown in Figure 6-100 and described in Table 6-104.

Return to the Summary Table.

Figure 6-100. DIAGEN2 Register

7	6	5	4	3	2	1	0
RESERVED		DIAGENOUTF1	DIAGENOUTF0	RESERVED		DIAGENOUTE1	DIAGENOUTE0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-104. DIAGEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	DIAGENOUTF1	R/W	X	Diagnostics enable register for OUTF1 Load EEPROM data when reset 0h = Disabled 1h = Enabled
4	DIAGENOUTF0	R/W	X	Diagnostics enable register for OUTF0 Load EEPROM data when reset 0h = Disabled 1h = Enabled
3-2	RESERVED	R	0h	Reserved
1	DIAGENOUTE1	R/W	X	Diagnostics enable register for OUTE1 Load EEPROM data when reset 0h = Disabled 1h = Enabled
0	DIAGENOUTE0	R/W	X	Diagnostics enable register for OUTE0 Load EEPROM data when reset 0h = Disabled 1h = Enabled

6.6.3.4 DIAGEN3 Register (Offset = 73h) [Reset = X]

DIAGEN3 is shown in Figure 6-101 and described in Table 6-105.

Return to the Summary Table.

Figure 6-101. DIAGEN3 Register

7	6	5	4	3	2	1	0
RESERVED		DIAGENOUTH1	DIAGENOUTH0	RESERVED		DIAGENOUTG1	DIAGENOUTG0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-105. DIAGEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved

Table 6-105. DIAGEN3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DIAGENOUTH1	R/W	X	Diagnostics enable register for OUTH1 Load EEPROM data when reset 0h = Disabled 1h = Enabled
4	DIAGENOUTH0	R/W	X	Diagnostics enable register for OUTH0 Load EEPROM data when reset 0h = Disabled 1h = Enabled
3-2	RESERVED	R	0h	Reserved
1	DIAGENOUTG1	R/W	X	Diagnostics enable register for OUTG1 Load EEPROM data when reset 0h = Disabled 1h = Enabled
0	DIAGENOUTG0	R/W	X	Diagnostics enable register for OUTG0 Load EEPROM data when reset 0h = Disabled 1h = Enabled

6.6.3.5 SLSTHSEL0 Register (Offset = 74h) [Reset = X]

SLSTHSEL0 is shown in Figure 6-102 and described in Table 6-106.

Return to the Summary Table.

Figure 6-102. SLSTHSEL0 Register

7	6	5	4	3	2	1	0
RESERVED		SLSTHOUTB1	SLSTHOUTB0	RESERVED		SLSTHOUTA1	SLSTHOUTA0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-106. SLSTHSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	SLSTHOUTB1	R/W	X	Single-LED short-circuit threshold selection register for OUTB1 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
4	SLSTHOUTB0	R/W	X	Single-LED short-circuit threshold selection register for OUTB0 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
3-2	RESERVED	R	0h	Reserved
1	SLSTHOUTA1	R/W	X	Single-LED short-circuit threshold selection register for OUTA1 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
0	SLSTHOUTA0	R/W	X	Single-LED short-circuit threshold selection register for OUTA0 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected

6.6.3.6 SLSTHSEL1 Register (Offset = 75h) [Reset = X]

SLSTHSEL1 is shown in Figure 6-103 and described in Table 6-107.

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Figure 6-103. SLSTHSEL1 Register

7	6	5	4	3	2	1	0
RESERVED		SLSTHOUTD1	SLSTHOUTD0	RESERVED		SLSTHOUTC1	SLSTHOUTC0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-107. SLSTHSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	SLSTHOUTD1	R/W	X	Single-LED short-circuit threshold selection register for OUTD1 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
4	SLSTHOUTD0	R/W	X	Single-LED short-circuit threshold selection register for OUTD0 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
3-2	RESERVED	R	0h	Reserved
1	SLSTHOUTC1	R/W	X	Single-LED short-circuit threshold selection register for OUTC1 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
0	SLSTHOUTC0	R/W	X	Single-LED short-circuit threshold selection register for OUTC0 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected

6.6.3.7 SLSTHSEL2 Register (Offset = 76h) [Reset = X]

SLSTHSEL2 is shown in Figure 6-104 and described in Table 6-108.

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Figure 6-104. SLSTHSEL2 Register

7	6	5	4	3	2	1	0
RESERVED		SLSTHOUTF1	SLSTHOUTF0	RESERVED		SLSTHOUTE1	SLSTHOUTE0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-108. SLSTHSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	SLSTHOUTF1	R/W	X	Single-LED short-circuit threshold selection register for OUTF1 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
4	SLSTHOUTF0	R/W	X	Single-LED short-circuit threshold selection register for OUTF0 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
3-2	RESERVED	R	0h	Reserved
1	SLSTHOUTE1	R/W	X	Single-LED short-circuit threshold selection register for OUTE1 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected

Table 6-108. SLSTHSEL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SLSTHOUTE0	R/W	X	Single-LED short-circuit threshold selection register for OUTE0 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected

6.6.3.8 SLSTHSEL3 Register (Offset = 77h) [Reset = X]

SLSTHSEL3 is shown in Figure 6-105 and described in Table 6-109.

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Figure 6-105. SLSTHSEL3 Register

7	6	5	4	3	2	1	0
RESERVED		SLSTHOUTH1	SLSTHOUTH0	RESERVED		SLSTHOUTG1	SLSTHOUTG0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-109. SLSTHSEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	SLSTHOUTH1	R/W	X	Single-LED short-circuit threshold selection register for OUTH1 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
4	SLSTHOUTH0	R/W	X	Single-LED short-circuit threshold selection register for OUTH0 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
3-2	RESERVED	R	0h	Reserved
1	SLSTHOUTG1	R/W	X	Single-LED short-circuit threshold selection register for OUTG1 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected
0	SLSTHOUTG0	R/W	X	Single-LED short-circuit threshold selection register for OUTG0 Load EEPROM data when reset 0h = SLSTH0 is selected 1h = SLSTH1 is selected

6.6.3.9 SLSDAC0 Register (Offset = 78h) [Reset = X]

SLSDAC0 is shown in Figure 6-106 and described in Table 6-110.

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Figure 6-106. SLSDAC0 Register

7	6	5	4	3	2	1	0
SLSTH0							
R/W-X							

Table 6-110. SLSDAC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SLSTH0	R/W	X	Single-LED short-circuit setting register for SLSTH0 Load EEPROM data when reset V(SLSTH0) = SLSTH0*0.125V + 2.5V

6.6.3.10 SLSDAC1 Register (Offset = 79h) [Reset = X]

SLSDAC1 is shown in Figure 6-107 and described in Table 6-111.

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Figure 6-107. SLSDAC1 Register

7	6	5	4	3	2	1	0
SLSTH1							
R/W-X							

Table 6-111. SLSDAC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SLSTH1	R/W	X	Single-LED short-circuit setting register for SLSTH1 Load EEPROM data when reset V(SLSTH1) = SLSTH1*0.125V + 2.5V

6.6.3.11 REFERENCE Register (Offset = 7Ah) [Reset = X]

REFERENCE is shown in Figure 6-108 and described in Table 6-112.

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Figure 6-108. REFERENCE Register

7	6	5	4	3	2	1	0
SLSEN	REFRANGE		LOWSUPTH				
R/W-X	R/W-X		R/W-X				

Table 6-112. REFERENCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLSEN	R/W	X	Enable register for single-LED short-ciruit diagnostics Load EEPROM data when reset 0h = Disabled 1h = Enabled
6-5	REFRANGE	R/W	X	Reference current ratio setting register Load EEPROM data when reset 0h = 64 1h = 128 2h = 256 3h = 512
4-0	LOWSUPTH	R/W	X	Supply low threshold setting register Load EEPROM data when reset V(LOWSUPTH) = LOWSUPTH*1V + 4V

6.6.3.12 DIAG Register (Offset = 7Bh) [Reset = X]

DIAG is shown in Figure 6-109 and described in Table 6-113.

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Figure 6-109. DIAG Register

7	6	5	4	3	2	1	0
IRETRY				BLANK			
R/W-X				R/W-X			

Table 6-113. DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IRETRY	R/W	X	LED open-circuit and short-circuit retry current setting register I(RETRY) = (IRETRY*4 + 4)/64*I(FULL_RANGE) Load EEPROM data when reset
3-0	BLANK	R/W	X	Diagnostics blank time setting register Load EEPROM data when reset 0h = 100µs 1h = 20µs 2h = 30µs 3h = 50µs 4h = 80µs 5h = 150µs 6h = 200µs 7h = 300µs 8h = 500µs 9h = 800µs Ah = 1ms Bh = 1.2ms Ch = 1.5ms Dh = 2ms Eh = 3ms Fh = 4ms

6.6.3.13 DIAGMASK Register (Offset = 7Ch) [Reset = X]

DIAGMASK is shown in Figure 6-110 and described in Table 6-114.

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Figure 6-110. DIAGMASK Register

7	6	5	4	3	2	1	0
MASKLOWSUP	MASKSUPUV	MASKREF	MASKPRETSD	MASKTSD	MASKEEPCRC	RESERVED	
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R-0h	

Table 6-114. DIAGMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASKLOWSUP	R/W	X	Supply low fault mask register Load EEPROM data when reset 0h = Fault report is enabled 1h = Fault report is disabled
6	MASKSUPUV	R/W	X	Supply undervoltage fault mask register Load EEPROM data when reset 0h = Fault report is enabled 1h = Fault report is disabled
5	MASKREF	R/W	X	REF pin fault mask register Load EEPROM data when reset 0h = Fault report is enabled 1h = Fault report is disabled
4	MASKPRETSD	R/W	X	Thermal pre-warning fault mask register Load EEPROM data when reset 0h = Fault report is enabled 1h = Fault report is disabled
3	MASKTSD	R/W	X	Thermal shutdown fault mask register Load EEPROM data when reset 0h = Fault report is enabled 1h = Fault report is disabled

Table 6-114. DIAGMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MASKEEPCRC	R/W	X	EEPROM CRC fault mask register Load EEPROM data when reset 0h = Fault report is enabled 1h = Fault report is disabled
1-0	RESERVED	R	0h	Reserved

6.6.3.14 OUTMASK Register (Offset = 7Dh) [Reset = X]

OUTMASK is shown in Figure 6-111 and described in Table 6-115.

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Figure 6-111. OUTMASK Register

7	6	5	4	3	2	1	0
RESERVED					MASKOPEN	MASKSHORT	MASKSLS
R-0h					R/W-X	R/W-X	R/W-X

Table 6-115. OUTMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	MASKOPEN	R/W	X	Output open-circuit fault mask register Load EEPROM data when reset 0h = Fault report is enabled 1h = Fault report is disabled
1	MASKSHORT	R/W	X	Output short-circuit fault mask register Load EEPROM data when reset 0h = Fault report is enabled 1h = Fault report is disabled
0	MASKSLS	R/W	X	Single-LED short-circuit fault mask register Load EEPROM data when reset 0h = Fault report is enabled 1h = Fault report is disabled

6.6.3.15 DIM Register (Offset = 7Eh) [Reset = X]

DIM is shown in Figure 6-112 and described in Table 6-116.

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Figure 6-112. DIM Register

7	6	5	4	3	2	1	0
EXPEN	PSEN	12BIT	PSMEN	PWMFREQ			
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X			

Table 6-116. DIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EXPEN	R/W	X	Enable register for exponential dimming curve Load EEPROM data when reset 0h = Disabled 1h = Enabled
6	PSEN	R/W	X	Enable register for phase shift dimming Load EEPROM data when reset 0h = Disabled 1h = Enabled

Table 6-116. DIM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	12BIT	R/W	X	Enable register for 12-bit dimming resolution diagnostics Load EEPROM data when reset 0h = Disabled 1h = Enabled
4	PSMEN	R/W	X	Enable register for digital power save mode Load EEPROM data when reset 0h = Disabled 1h = Enabled
3-0	PWMFREQ	R/W	X	PWM dimming frequency setting register Load EEPROM data when reset 0h = 200Hz 1h = 250Hz 2h = 300Hz 3h = 350Hz 4h = 400Hz 5h = 500Hz 6h = 600Hz 7h = 800Hz 8h = 1000Hz 9h = 1200Hz Ah = 2000Hz Bh = 4000Hz Ch = 5900Hz Dh = 7800Hz Eh = 9600Hz Fh = 20800Hz

6.6.3.16 DIM-R Register (Offset = 7Fh) [Reset = 00h]

DIM-R is shown in Figure 6-113 and described in Table 6-117.

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Figure 6-113. DIM-R Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 6-117. DIM-R Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

6.6.3.17 FSMAP0 Register (Offset = 80h) [Reset = X]

FSMAP0 is shown in Figure 6-114 and described in Table 6-118.

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Figure 6-114. FSMAP0 Register

7	6	5	4	3	2	1	0
RESERVED		FSOUTB1	FSOUTB0	RESERVED		FSOUTA1	FSOUTA0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-118. FSMAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved

Table 6-118. FSMAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FSOUTB1	R/W	X	Fail-safe state control input mapping for OUTB1 Load EEPROM data when reset 0h = OUTB1 is mapped to FS0 in fail-safe state 1h = OUTB1 is mapped to FS1 in fail-safe state
4	FSOUTB0	R/W	X	Fail-safe state control input mapping for OUTB0 Load EEPROM data when reset 0h = OUTB0 is mapped to FS0 in fail-safe state 1h = OUTB0 is mapped to FS1 in fail-safe state
3-2	RESERVED	R	0h	Reserved
1	FSOUTA1	R/W	X	Fail-safe state control input mapping for OUTA1 Load EEPROM data when reset 0h = OUTA1 is mapped to FS0 in fail-safe state 1h = OUTA1 is mapped to FS1 in fail-safe state
0	FSOUTA0	R/W	X	Fail-safe state control input mapping for OUTA0 Load EEPROM data when reset 0h = OUTA0 is mapped to FS0 in fail-safe state 1h = OUTA0 is mapped to FS1 in fail-safe state

6.6.3.18 FSMAP1 Register (Offset = 81h) [Reset = X]

FSMAP1 is shown in Figure 6-115 and described in Table 6-119.

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Figure 6-115. FSMAP1 Register

7	6	5	4	3	2	1	0
RESERVED		FSOUTD1	FSOUTD0	RESERVED		FSOUTC1	FSOUTC0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-119. FSMAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FSOUTD1	R/W	X	Fail-safe state control input mapping for OUTD1 Load EEPROM data when reset 0h = OUTD1 is mapped to FS0 in fail-safe state 1h = OUTD1 is mapped to FS1 in fail-safe state
4	FSOUTD0	R/W	X	Fail-safe state control input mapping for OUTC2 Load EEPROM data when reset 0h = OUTD0 is mapped to FS0 in fail-safe state 1h = OUTD0 is mapped to FS1 in fail-safe state
3-2	RESERVED	R	0h	Reserved
1	FSOUTC1	R/W	X	Fail-safe state control input mapping for OUTC1 Load EEPROM data when reset 0h = OUTC1 is mapped to FS0 in fail-safe state 1h = OUTC1 is mapped to FS1 in fail-safe state
0	FSOUTC0	R/W	X	Fail-safe state control input mapping for OUTC0 Load EEPROM data when reset 0h = OUTC0 is mapped to FS0 in fail-safe state 1h = OUTC0 is mapped to FS1 in fail-safe state

6.6.3.19 FSMAP2 Register (Offset = 82h) [Reset = X]

FSMAP2 is shown in Figure 6-116 and described in Table 6-120.

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Figure 6-116. FSMAP2 Register

7	6	5	4	3	2	1	0
RESERVED		FSOUTF1	FSOUTF0	RESERVED		FSOUTE1	FSOUTE0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-120. FSMAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FSOUTF1	R/W	X	Fail-safe state control input mapping for OUTF1 Load EEPROM data when reset 0h = OUTF1 is mapped to FS0 in fail-safe state 1h = OUTF1 is mapped to FS1 in fail-safe state
4	FSOUTF0	R/W	X	Fail-safe state control input mapping for OUTF0 Load EEPROM data when reset 0h = OUTF0 is mapped to FS0 in fail-safe state 1h = OUTF0 is mapped to FS1 in fail-safe state
3-2	RESERVED	R	0h	Reserved
1	FSOUTE1	R/W	X	Fail-safe state control input mapping for OUTE1 Load EEPROM data when reset 0h = OUTE1 is mapped to FS0 in fail-safe state 1h = OUTE1 is mapped to FS1 in fail-safe state
0	FSOUTE0	R/W	X	Fail-safe state control input mapping for OUTE0 Load EEPROM data when reset 0h = OUTE0 is mapped to FS0 in fail-safe state 1h = OUTE0 is mapped to FS1 in fail-safe state

6.6.3.20 FSMAP3 Register (Offset = 83h) [Reset = X]

FSMAP3 is shown in Figure 6-117 and described in Table 6-121.

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Figure 6-117. FSMAP3 Register

7	6	5	4	3	2	1	0
RESERVED		FSOUTH1	FSOUTH0	RESERVED		FSOUTG1	FSOUTG0
R-0h		R/W-X	R/W-X	R-0h		R/W-X	R/W-X

Table 6-121. FSMAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FSOUTH1	R/W	X	Fail-safe state control input mapping for OUTH1 Load EEPROM data when reset 0h = OUTH1 is mapped to FS0 in fail-safe state 1h = OUTH1 is mapped to FS1 in fail-safe state
4	FSOUTH0	R/W	X	Fail-safe state control input mapping for OUTH0 Load EEPROM data when reset 0h = OUTH0 is mapped to FS0 in fail-safe state 1h = OUTH0 is mapped to FS1 in fail-safe state
3-2	RESERVED	R	0h	Reserved
1	FSOUTG1	R/W	X	Fail-safe state control input mapping for OUTG1 Load EEPROM data when reset 0h = OUTG1 is mapped to FS0 in fail-safe state 1h = OUTG1 is mapped to FS1 in fail-safe state

Table 6-121. FSMAP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FSOUTG0	R/W	X	Fail-safe state control input mapping for OUTG0 Load EEPROM data when reset 0h = OUTG0 is mapped to FS0 in fail-safe state 1h = OUTG0 is mapped to FS1 in fail-safe state

6.6.3.21 FLEXWIRE0 Register (Offset = 84h) [Reset = X]

FLEXWIRE0 is shown in Figure 6-118 and described in Table 6-122.

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Figure 6-118. FLEXWIRE0 Register

7	6	5	4	3	2	1	0
WDTIMER				DBWTIMER			ACKEN
R/W-X				R/W-X			R/W-X

Table 6-122. FLEXWIRE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	WDTIMER	R/W	X	Communication watchdog timer setting register Load EEPROM data when reset 0h = Disabled, do not automatically enter fail-safe state 1h = 200µs 2h = 500µs 3h = 1ms 4h = 2ms 5h = 5ms 6h = 10ms 7h = 20ms 8h = 50ms 9h = 100ms Ah = 200ms Bh = 500ms Ch = 0µs, directly enter fail-safe state Dh = 0µs, directly enter fail-safe state Eh = 0µs, directly enter fail-safe state Fh = 0µs, directly enter fail-safe state
3-1	DBWTIMER	R/W	X	Data transaction break waiting timer setting register Load EEPROM data when reset 0h = 1ms 1h = 125µs 2h = 250µs 3h = 500µs 4h = 1.25ms 5h = 2.5ms 6h = 5ms 7h = 5ms
0	ACKEN	R/W	X	Enable register for acknowledgement Load EEPROM data when reset 0h = Disabled 1h = Enabled

6.6.3.22 FLEXWIRE1 Register (Offset = 85h) [Reset = X]

FLEXWIRE1 is shown in Figure 6-119 and described in Table 6-123.

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Figure 6-119. FLEXWIRE1 Register

7	6	5	4	3	2	1	0
RESERVED			INTADDR	DEVADDR			
R-0h			R/W-X	R/W-X			

Table 6-123. FLEXWIRE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	INTADDR	R/W	X	Devce address selection register Load EEPROM data when reset 0h = Device address set by ADDR2/ADDR1 and ADDR0 pins 1h = Device address set by DEVADDR
3-0	DEVADDR	R/W	X	Device address setting register Load EEPROM data when reset 0h = slave address is 0000b 1h = slave address is 0001b 2h = slave address is 0010b 3h = slave address is 0011b 4h = slave address is 0100b 5h = slave address is 0101b 6h = slave address is 0110b 7h = slave address is 0111b 8h = slave address is 1000b 9h = slave address is 1001b Ah = slave address is 1010b Bh = slave address is 1011b Ch = slave address is 1100b Dh = slave address is 1101b Eh = slave address is 1110b Fh = slave address is 1111b

6.6.3.23 FLEXWIRE2 Register (Offset = 86h) [Reset = X]

FLEXWIRE2 is shown in Figure 6-120 and described in Table 6-124.

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Figure 6-120. FLEXWIRE2 Register

7	6	5	4	3	2	1	0
RESERVED			OFAF	INITTIMER			
R-0h			R/W-X	R/W-X			

Table 6-124. FLEXWIRE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OFAF	R/W	X	Output one-fail-all-fail setting register in fail-safe state Load EEPROM data when reset 0h = OFAF Disabled 1h = OFAF Enabled

Table 6-124. FLEXWIRE2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	INITTIMER	R/W	X	Initialization timer setting register Load EEPROM data when reset 0h = 0ms 1h = 50ms 2h = 20ms 3h = 10ms 4h = 5ms 5h = 2ms 6h = 1ms 7h = 500µs 8h = 200µs 9h = 100µs Ah = 50µs Bh = 50µs Ch = 50µs Dh = 50µs Eh = 50µs Fh = 50µs

6.6.3.24 CRC Register (Offset = 87h) [Reset = X]

CRC is shown in Figure 6-121 and described in Table 6-125.

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Figure 6-121. CRC Register

7	6	5	4	3	2	1	0
EEPCRC							
R/W-X							

Table 6-125. CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEPCRC	R/W	X	CRC reference for all EEPROM registers including RESERVED registers, manufacture default CRC result is 81h Load EEPROM data when reset

6.6.4 CTRL Registers

Table 6-126 lists the memory-mapped registers for the CTRL registers. All register offset addresses not listed in Table 6-126 should be considered as reserved locations and the register contents should not be modified.

Control Register

Table 6-126. CTRL Registers

Offset	Acronym	Register Name	Section
90h	ADCCH	ADC Channel Selection Setting	Go
91h	CLR	Control Register for Clear	Go
92h	DEBUG	Control Register for Debug	Go
93h	LOCK	Control Register for Register Lock	Go
94h	CLRREG	Control Register for Clear Register	Go
95h	NSTB	Control Register for NSTB	Go
96h	CTRLGATE	Gate Register for MISC and LOCK	Go
97h	EEP	Control Register for EEP Operation	Go
98h	EEPGATE	Gate Register for EEP	Go

Complex bit access types are encoded to fit into small table cells. Table 6-127 shows the codes that are used for access types in this section.

Table 6-127. CTRL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.4.1 ADCCH Register (Offset = 90h) [Reset = 00h]

ADCCH is shown in Figure 6-122 and described in Table 6-128.

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Figure 6-122. ADCCH Register

7	6	5	4	3	2	1	0
RESERVED				ADCCHSEL			
R-0h				R/W-0h			

Table 6-128. ADCCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	ADCCHSEL	R/W	0h	Channel selection setting for ADC voltage measurement, write this register automatically initiates the ADC conversion

6.6.4.2 CLR Register (Offset = 91h) [Reset = 00h]

CLR is shown in Figure 6-123 and described in Table 6-129.

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Figure 6-123. CLR Register

7	6	5	4	3	2	1	0
RESERVED					CLRFS	CLRFAULT	CLRPOR
R-0h					R/W-0h	R/W-0h	R/W-0h

Table 6-129. CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	CLRFS	R/W	0h	Write 1 to force device to exit fail-safe state to normal state, automatically returns to 0
1	CLRFAULT	R/W	0h	Write 1 to clear all fault flags, automatically returns to 0
0	CLRPOR	R/W	0h	Write 1 to clear POR fault flag, automatically returns to 0

6.6.4.3 DEBUG Register (Offset = 92h) [Reset = 00h]

DEBUG is shown in Figure 6-124 and described in Table 6-130.

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Figure 6-124. DEBUG Register

7	6	5	4	3	2	1	0
RESERVED						FORCEFS	FPRCEERR
R-0h						R/W-0h	R/W-0h

Table 6-130. DEBUG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	FORCEFS	R/W	0h	Write 1 to force device to fail-safe state, automatically returns to 0
0	FPRCEERR	R/W	0h	Write 1 to set FLAG_ERR to 1 and $\overline{\text{ERR}}$ output pulled down for 50µs in normal state, automatically returns to 0

6.6.4.4 LOCK Register (Offset = 93h) [Reset = 03h]

LOCK is shown in Figure 6-125 and described in Table 6-131.

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Figure 6-125. LOCK Register

7	6	5	4	3	2	1	0
RESERVED					BRTLOCK	CONFLOCK	IOUTLOCK
R-0h					R/W-0h	R/W-1h	R/W-1h

Table 6-131. LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	BRTLOCK	R/W	0h	BRT register lock 0h = Write protection is disabled 1h = Write protection is enabled
1	CONFLOCK	R/W	1h	CONF register lock 0h = Write protection is disabled 1h = Write protection is enabled

Table 6-131. LOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IOUTLOCK	R/W	1h	IOUT register lock 0h = Write protection is disabled 1h = Write protection is enabled

6.6.4.5 CLRREG Register (Offset = 94h) [Reset = 00h]

CLRREG is shown in Figure 6-126 and described in Table 6-132.

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Figure 6-126. CLRREG Register

7	6	5	4	3	2	1	0
RESERVED					SOFTRESET	EEPLOAD	REGDEFAULT
R-0h					R/W-0h	R/W-0h	R/W-0h

Table 6-132. CLRREG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	SOFTRESET	R/W	0h	Write 1 to reset all state machine and all registers, automatically returns to 0
1	EEPLOAD	R/W	0h	Write 1 to load EEP data to corresponding registers, automatically returns to 0
0	REGDEFAULT	R/W	0h	Write 1 to set all registers to default value, automatically returns to 0

6.6.4.6 NSTB Register (Offset = 95h) [Reset = 00h]

NSTB is shown in Figure 6-127 and described in Table 6-133.

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Figure 6-127. NSTB Register

7	6	5	4	3	2	1	0
RESERVED							NSTB
R-0h							R/W-0h

Table 6-133. NSTB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	NSTB	R/W	0h	NSTB output internal pulling up control register 0h = Pulling up is enabled 1h = Pulling up is disabled

6.6.4.7 CTRLGATE Register (Offset = 96h) [Reset = 00h]

CTRLGATE is shown in Figure 6-128 and described in Table 6-134.

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Figure 6-128. CTRLGATE Register

7	6	5	4	3	2	1	0
CTRLGATE							
R/W-0h							

Figure 6-128. CTRLGATE Register (continued)

Table 6-134. CTRLGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CTRLGATE	R/W	0h	Gate register for DEBUG, LOCK and CLRREG registers access, write 43h, 4Fh, 44h and 45h one-byte by one-byte

6.6.4.8 EEP Register (Offset = 97h) [Reset = 00h]

EEP is shown in Figure 6-129 and described in Table 6-135.

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Figure 6-129. EEP Register

7	6	5	4	3	2	1	0
RESERVED						EEPPROG	EEPMODE
R-0h						R/W-0h	R/W-0h

Table 6-135. EEP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	EEPPROG	R/W	0h	EEPROM burning starts in EEPROM programming state only, automatically returns to 0
0	EEPMODE	R/W	0h	EEPROM programming state setting 0h = Disabled 1h = Enabled

6.6.4.9 EEPGATE Register (Offset = 98h) [Reset = 00h]

EEPGATE is shown in Figure 6-130 and described in Table 6-136.

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Figure 6-130. EEPGATE Register

7	6	5	4	3	2	1	0
EEPGATE							
R/W-0h							

Table 6-136. EEPGATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEPGATE	R/W	0h	Gate register for EEP registers access, write 00h, 04h, 02h, 09h, 02h and 09h one-byte by one-byte

6.6.5 FLAG Registers

Table 6-137 lists the memory-mapped registers for the FLAG registers. All register offset addresses not listed in Table 6-137 should be considered as reserved locations and the register contents should not be modified.

FLAG Register

Table 6-137. FLAG Registers

Offset	Acronym	Register Name	Section
A0h	FLAG_ERR	Device Error Flag Register	Go
A1h	FLAG_STATUS	Device Status Flag Register	Go
A2h	FLAG_ADC	Selected Channel ADC Measurement Result	Go
A3h	FLAG_SLS0	OUTAn, OUTBn Single-LED Short Error FLAG	Go
A4h	FLAG_SLS1	OUTCn, OUTDn Single-LED Short Error FLAG	Go
A5h	FLAG_SLS2	OUTEn, OUTFn Single-LED Short Error FLAG	Go
A6h	FLAG_SLS3	OUTGn, OUTHn Single-LED Short Error FLAG	Go
A7h	FLAG_OPEN0	OUTAn, OUTBn LED Open Error FLAG	Go
A8h	FLAG_OPEN1	OUTCn, OUTDn LED Open Error FLAG	Go
A9h	FLAG_OPEN2	OUTEn, OUTFn LED Open Error FLAG	Go
AAh	FLAG_OPEN3	OUTGn, OUTHn LED Open Error FLAG	Go
ABh	FLAG_SHORT0	OUTAn, OUTBn Short-to-GND Error FLAG	Go
ACh	FLAG_SHORT1	OUTCn, OUTDn Short-to-GND Error FLAG	Go
ADh	FLAG_SHORT2	OUTEn, OUTFn Short-to-GND Error FLAG	Go
AEh	FLAG_SHORT3	OUTGn, OUTHn Short-to-GND Error FLAG	Go
AFh	FLAG_EEPCRC	EEPROM Calculated CRC	Go

Complex bit access types are encoded to fit into small table cells. Table 6-138 shows the codes that are used for access types in this section.

Table 6-138. FLAG Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

6.6.5.1 FLAG_ERR Register (Offset = A0h) [Reset = 01h]

FLAG_ERR is shown in Figure 6-131 and described in Table 6-139.

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Figure 6-131. FLAG_ERR Register

7	6	5	4	3	2	1	0
FLAG_LOWSUP	FLAG_SUPUV	FLAG_REF	FLAG_PRETSD	FLAG_TSD	FLAG_EEPCRC	FLAG_OUT	FLAG_ERR
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h

Table 6-139. FLAG_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FLAG_LOWSUP	R	0h	Supply voltage low flag 0h = Supply voltage is above preset threshold. 1h = Supply voltage is below preset threshold.
6	FLAG_SUPUV	R	0h	Supply undervoltage fault flag 0h = No supply undervoltage fault is detected. 1h = Device has supply undervoltage fault detected.
5	FLAG_REF	R	0h	REF pin fault flag 0h = No REF pin fault is detected. 1h = Device has REF pin fault detected.
4	FLAG_PRETSD	R	0h	Overtemperature Pre warning flag 0h = No overtemperature pre-warning is detected. 1h = Device has triggered overtemperature pre-warning threshold.
3	FLAG_TSD	R	0h	Thermal shutdown flag 0h = No thermal shutdown fault is triggered. 1h = Device has triggered thermal shutdown fault.
2	FLAG_EEPCRC	R	0h	EEPROM CRC failure flag 0h = EEPROM CRC passes. 1h = EEPROM CRC fails.
1	FLAG_OUT	R	0h	Output fault flag 0h = No output fault is detected. 1h = Device has at least one fault detected on output channels.
0	FLAG_ERR	R	1h	Error flag 0h = No error flag. 1h = Device has at least one error flag.

6.6.5.2 FLAG_STATUS Register (Offset = A1h) [Reset = 01h]

FLAG_STATUS is shown in Figure 6-132 and described in Table 6-140.

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Figure 6-132. FLAG_STATUS Register

7	6	5	4	3	2	1	0
FLAG_EEPPAR	FLAG_EXTFS1	FLAG_EXTFS0	FLAG_PROGDONE	FLAG_FS	FLAG_ADCDONE	FLAG_ADCERR	FLAG_POR
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h

Table 6-140. FLAG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FLAG_EEPPAR	R	0h	EEPROM parity error flag 0h = No internal EEPROM parity error is triggered. 1h = Internal EEPROM parity error is triggered.
6	FLAG_EXTFS1	R	0h	FS1 input status flag 0h = FS1 input is logic low. 1h = FS1 input is logic high.
5	FLAG_EXTFS0	R	0h	FS0 input status flag 0h = FS0 input is logic low. 1h = FS0 input is logic high.
4	FLAG_PROGDONE	R	0h	EEPROM program completition flag 0h = EEPROM burning is not completed or not started. 1h = EEPROM burning is completed.
3	FLAG_FS	R	0h	FS state flag 0h = Device is not in Fail-safe state. 1h = Device is in Fail-safe state.

Table 6-140. FLAG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	FLAG_ADCDONE	R	0h	ADC measurement completition flag 0h = ADC measurement result is not available. 1h = ADC measurement result is available, read ADC_OUT or write ADCCHSEL to clear FLAG_ADCDONE.
1	FLAG_ADCERR	R	0h	ADC error flag 0h = No ADC error is triggered. 1h = ADC error is triggered.
0	FLAG_POR	R	1h	Power-On-Reset flag 0h = No POR is triggered. 1h = Device has triggered POR.

6.6.5.3 FLAG_ADC Register (Offset = A2h) [Reset = 00h]

FLAG_ADC is shown in Figure 6-133 and described in Table 6-141.

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Figure 6-133. FLAG_ADC Register

7	6	5	4	3	2	1	0
ADC_OUT							
R-0h							

Table 6-141. FLAG_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADC_OUT	R	0h	ADC measurement result for selected channel

6.6.5.4 FLAG_SLS0 Register (Offset = A3h) [Reset = 00h]

FLAG_SLS0 is shown in Figure 6-134 and described in Table 6-142.

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Figure 6-134. FLAG_SLS0 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_SLSOUTB1	FLAG_SLSOUTB0	RESERVED		FLAG_SLSOUTA1	FLAG_SLSOUTA0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-142. FLAG_SLS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_SLSOUTB1	R	0h	Single-LED short-circuit fault flag for OUTB1 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
4	FLAG_SLSOUTB0	R	0h	Single-LED short-circuit fault flag for OUTB0 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_SLSOUTA1	R	0h	Single-LED short-circuit fault flag for OUTA1 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.

Table 6-142. FLAG_SLS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FLAG_SLSOUTA0	R	0h	Single-LED short-circuit fault flag for OUTA0 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.

6.6.5.5 FLAG_SLS1 Register (Offset = A4h) [Reset = 00h]

FLAG_SLS1 is shown in Figure 6-135 and described in Table 6-143.

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Figure 6-135. FLAG_SLS1 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_SLSOUTD1	FLAG_SLSOUTD0	RESERVED		FLAG_SLSOUTC1	FLAG_SLSOUTC0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-143. FLAG_SLS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_SLSOUTD1	R	0h	Single-LED short-circuit fault flag for OUTD1 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
4	FLAG_SLSOUTD0	R	0h	Single-LED short-circuit fault flag for OUTD0 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_SLSOUTC1	R	0h	Single-LED short-circuit fault flag for OUTC1 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
0	FLAG_SLSOUTC0	R	0h	Single-LED short-circuit fault flag for OUTC0 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.

6.6.5.6 FLAG_SLS2 Register (Offset = A5h) [Reset = 00h]

FLAG_SLS2 is shown in Figure 6-136 and described in Table 6-144.

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Figure 6-136. FLAG_SLS2 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_SLSOUTF1	FLAG_SLSOUTF0	RESERVED		FLAG_SLSOUTE1	FLAG_SLSOUTE0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-144. FLAG_SLS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_SLSOUTF1	R	0h	Single-LED short-circuit fault flag for OUTF1 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
4	FLAG_SLSOUTF0	R	0h	Single-LED short-circuit fault flag for OUTF0 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.

Table 6-144. FLAG_SLS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	RESERVED	R	0h	Reserved
1	FLAG_SLSOUTE1	R	0h	Single-LED short-circuit fault flag for OUTE1 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
0	FLAG_SLSOUTE0	R	0h	Single-LED short-circuit fault flag for OUTE0 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.

6.6.5.7 FLAG_SLS3 Register (Offset = A6h) [Reset = 00h]

FLAG_SLS3 is shown in Figure 6-137 and described in Table 6-145.

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Figure 6-137. FLAG_SLS3 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_SLSOUTH1	FLAG_SLSOUTH0	RESERVED		FLAG_SLSOUTG1	FLAG_SLSOUTG0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-145. FLAG_SLS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_SLSOUTH1	R	0h	Single-LED short-circuit fault flag for OUTH1 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
4	FLAG_SLSOUTH0	R	0h	Single-LED short-circuit fault flag for OUTH0 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_SLSOUTG1	R	0h	Single-LED short-circuit fault flag for OUTG1 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.
0	FLAG_SLSOUTG0	R	0h	Single-LED short-circuit fault flag for OUTG0 0h = Single-LED short-circuit fault is not detected. 1h = Single-LED short-circuit fault is detected.

6.6.5.8 FLAG_OPEN0 Register (Offset = A7h) [Reset = 00h]

FLAG_OPEN0 is shown in Figure 6-138 and described in Table 6-146.

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Figure 6-138. FLAG_OPEN0 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_OPENOUTB1	FLAG_OPENOUTB0	RESERVED		FLAG_OPENOUTA1	FLAG_OPENOUTA0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-146. FLAG_OPEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved

Table 6-146. FLAG_OPEN0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FLAG_OPENOUTB1	R	0h	Output open-circuit fault flag for OUTB1 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
4	FLAG_OPENOUTB0	R	0h	Output open-circuit fault flag for OUTB0 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_OPENOUTA1	R	0h	Output open-circuit fault flag for OUTA1 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
0	FLAG_OPENOUTA0	R	0h	Output open-circuit fault flag for OUTA0 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.

6.6.5.9 FLAG_OPEN1 Register (Offset = A8h) [Reset = 00h]

FLAG_OPEN1 is shown in Figure 6-139 and described in Table 6-147.

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Figure 6-139. FLAG_OPEN1 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_OPENOUTD1	FLAG_OPENOUTD0	RESERVED		FLAG_OPENOUTC1	FLAG_OPENOUTC0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-147. FLAG_OPEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_OPENOUTD1	R	0h	Output open-circuit fault flag for OUTD1 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
4	FLAG_OPENOUTD0	R	0h	Output open-circuit fault flag for OUTD0 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_OPENOUTC1	R	0h	Output open-circuit fault flag for OUTC1 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
0	FLAG_OPENOUTC0	R	0h	Output open-circuit fault flag for OUTC0 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.

6.6.5.10 FLAG_OPEN2 Register (Offset = A9h) [Reset = 00h]

FLAG_OPEN2 is shown in Figure 6-140 and described in Table 6-148.

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Figure 6-140. FLAG_OPEN2 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_OPENOUTF1	FLAG_OPENOUTF0	RESERVED		FLAG_OPENOUTE1	FLAG_OPENOUTE0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Figure 6-140. FLAG_OPEN2 Register (continued)

Table 6-148. FLAG_OPEN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_OPENOUTF1	R	0h	Output open-circuit fault flag for OUTF1 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
4	FLAG_OPENOUTF0	R	0h	Output open-circuit fault flag for OUTF0 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_OPENOUTE1	R	0h	Output open-circuit fault flag for OUTE1 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
0	FLAG_OPENOUTE0	R	0h	Output open-circuit fault flag for OUTE0 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.

6.6.5.11 FLAG_OPEN3 Register (Offset = AAh) [Reset = 00h]

FLAG_OPEN3 is shown in Figure 6-141 and described in Table 6-149.

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Figure 6-141. FLAG_OPEN3 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_OPENOUTH1	FLAG_OPENOUTH0	RESERVED		FLAG_OPENOUTG1	FLAG_OPENOUTG0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-149. FLAG_OPEN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_OPENOUTH1	R	0h	Output open-circuit fault flag for OUTH1 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
4	FLAG_OPENOUTH0	R	0h	Output open-circuit fault flag for OUTH0 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_OPENOUTG1	R	0h	Output open-circuit fault flag for OUTG1 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.
0	FLAG_OPENOUTG0	R	0h	Output open-circuit fault flag for OUTG0 0h = Output open-circuit fault is not detected. 1h = Output open-circuit fault is detected.

6.6.5.12 FLAG_SHORT0 Register (Offset = ABh) [Reset = 00h]

FLAG_SHORT0 is shown in Figure 6-142 and described in Table 6-150.

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Figure 6-142. FLAG_SHORT0 Register

7	6	5	4	3	2	1	0

Figure 6-142. FLAG_SHORT0 Register (continued)

RESERVED	FLAG_SHORT OUTB1	FLAG_SHORT OUTB0	RESERVED	FLAG_SHORT OUTA1	FLAG_SHORT OUTA0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 6-150. FLAG_SHORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_SHORTOUTB1	R	0h	Output short-circuit fault flag for OUTB1 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
4	FLAG_SHORTOUTB0	R	0h	Output short-circuit fault flag for OUTB0 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_SHORTOUTA1	R	0h	Output short-circuit fault flag for OUTA1 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
0	FLAG_SHORTOUTA0	R	0h	Output short-circuit fault flag for OUTA0 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.

6.6.5.13 FLAG_SHORT1 Register (Offset = ACh) [Reset = 00h]

FLAG_SHORT1 is shown in Figure 6-143 and described in Table 6-151.

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Figure 6-143. FLAG_SHORT1 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_SHORT OUTD1	FLAG_SHORT OUTD0	RESERVED		FLAG_SHORT OUTC1	FLAG_SHORT OUTC0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-151. FLAG_SHORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_SHORTOUTD1	R	0h	Output short-circuit fault flag for OUTD1 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
4	FLAG_SHORTOUTD0	R	0h	Output short-circuit fault flag for OUTD0 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_SHORTOUTC1	R	0h	Output short-circuit fault flag for OUTC1 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
0	FLAG_SHORTOUTC0	R	0h	Output short-circuit fault flag for OUTC0 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.

6.6.5.14 FLAG_SHORT2 Register (Offset = ADh) [Reset = 00h]

FLAG_SHORT2 is shown in Figure 6-144 and described in Table 6-152.

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Figure 6-144. FLAG_SHORT2 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_SHORTOUTF1	FLAG_SHORTOUTF0	RESERVED		FLAG_SHORTOUTE1	FLAG_SHORTOUTE0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-152. FLAG_SHORT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_SHORTOUTF1	R	0h	Output short-circuit fault flag for OUTF1 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
4	FLAG_SHORTOUTF0	R	0h	Output short-circuit fault flag for OUTF0 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_SHORTOUTE1	R	0h	Output short-circuit fault flag for OUTE1 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
0	FLAG_SHORTOUTE0	R	0h	Output short-circuit fault flag for OUTE0 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.

6.6.5.15 FLAG_SHORT3 Register (Offset = AEh) [Reset = 00h]

FLAG_SHORT3 is shown in Figure 6-145 and described in Table 6-153.

Return to the Summary Table.

Figure 6-145. FLAG_SHORT3 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_SHORTOUTH1	FLAG_SHORTOUTH0	RESERVED		FLAG_SHORTOUTG1	FLAG_SHORTOUTG0
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 6-153. FLAG_SHORT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	FLAG_SHORTOUTH1	R	0h	Output short-circuit fault flag for OUTH1 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
4	FLAG_SHORTOUTH0	R	0h	Output short-circuit fault flag for OUTH0 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
3-2	RESERVED	R	0h	Reserved
1	FLAG_SHORTOUTG1	R	0h	Output short-circuit fault flag for OUTG1 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.
0	FLAG_SHORTOUTG0	R	0h	Output short-circuit fault flag for OUTG0 0h = Output short-circuit fault is not detected. 1h = Output short-circuit fault is detected.

6.6.5.16 FLAG_EEPCRC Register (Offset = AFh) [Reset = 00h]

FLAG_EEPCRC is shown in Figure 6-146 and described in Table 6-154.

Return to the Summary Table.

Figure 6-146. FLAG_EEPCRC Register

7	6	5	4	3	2	1	0
CALC_EEPCRC							
R-0h							

Table 6-154. FLAG_EEPCRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CALC_EEPCRC	R	0h	Calculated CRC result for all EEPROM

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS929160-Q1 device with FlexWire interface easily generates independent brightness and ON and OFF control for large amount LED units. The device allows each single LED as a pixel in large LED array or string to display a complicated pattern or animation under accurate control. The FlexWire interface also supports to use the CAN physical layer through external CAN transceiver for data transmission between master microcontroller (MCU) and TPS929160-Q1, which allows the TPS929160-Q1 to be controlled by control module far away in long distance. With these features, the single TPS929160-Q1 or multiple TPS929160-Q1 devices can drive large volume LEDs with digital control interface for automotive lighting applications. The long distance, reliable off-board communication with high EMC performance simplifies the system design in lower cost for automotive application.

The TPS929160-Q1 can also operate as a standalone LED driver without master MCU. The FAIL-SAFE state is designed to ensure the TPS929160-Q1 keeps operating in case the communication is lost or the master MCU is damaged. TPS929160-Q1 can also use the FAIL-SAFE state without master MCU design for traditional automotive lighting applications.

7.2 Typical Application

7.2.1 Smart Rear Lamp with Distributed LED Drivers

Use multiple TPS929160-Q1 devices to control large number of LED pixels for rear-lamp animation.

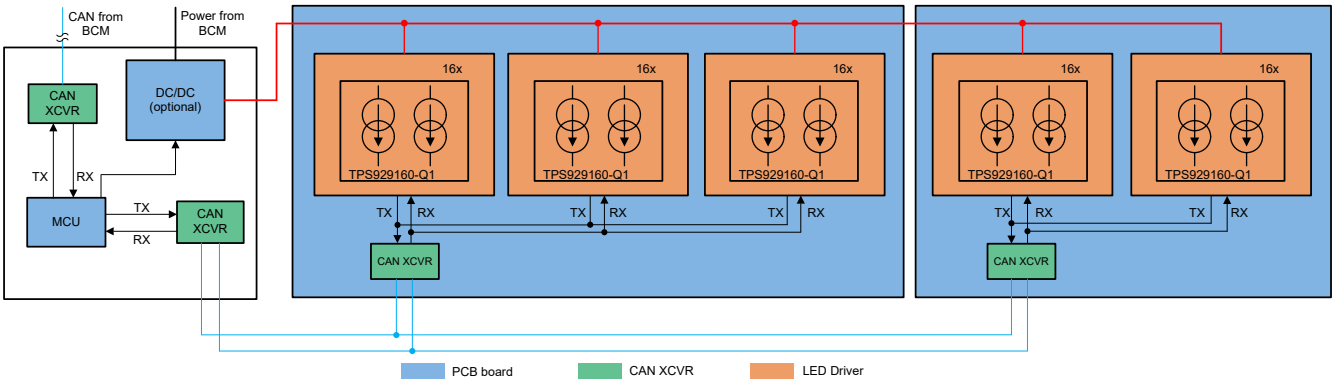


Figure 7-1. System Block Diagram

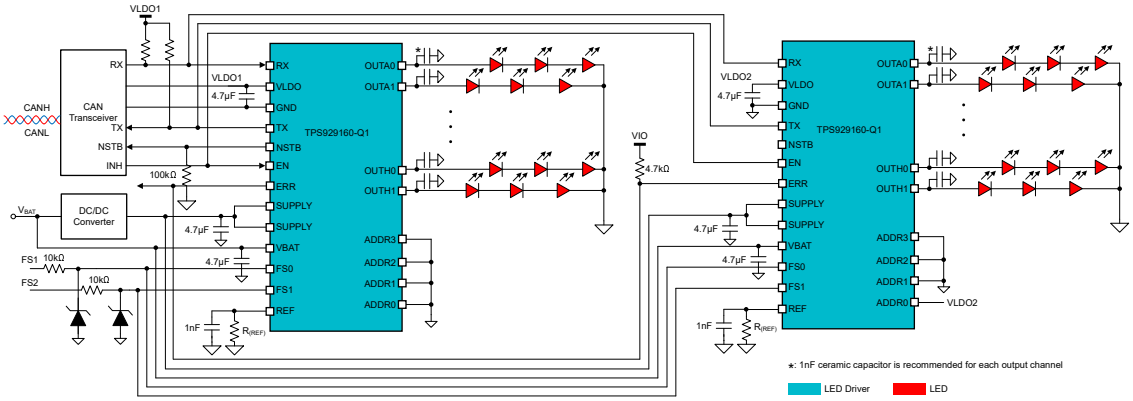


Figure 7-2. Typical Application Schematic

7.2.2 Design Requirements

Input voltage ranges from 9V to 16V, and a total of 80 LED strings with 3 LEDs in each string are required in one rear-lamp housing. The 80 LED strings must be controlled independently to achieve the animation effect. The maximum forward voltage of single LED $V_{(F\_MAX)}$ = 2.6V, minimum forward voltage $V_{(F\_MIN)}$ = 2.3V, and each string current $I_{(LED)}$ = 50mA. The 48 strings of LED, and 32 strings of LED and MCU must be placed in three different boards due to the shape of the rear-lamp housing.

7.2.3 Detailed Design Procedure

STEP 1: Determine the architecture at system level.

Because MCU is located in a separate board, the CAN physical layer must be used for off-board long distance communication between LED driver boards and MCU board. The overall system block diagram is shown in Figure 7-1 and the typical schematic for 48 strings of LED board is shown in Figure 7-2. The pullup resistors for RX and TX interface can or cannot required, depending on the model of the CAN transceiver. Normally the pullup resistor value for RX and TX must be about 10kΩ. TI recommends putting a 4.7μF ceramic capacitor on the VLDO output to keep the voltage stable. Because only one CAN transceiver is required per one PCB board, the CAN transceiver must only be powered by one LDO output of the TPS929160-Q1. *Do not* tie the LDO outputs for all TPS929160-Q1 in one PCB board. TI also recommends placing a 4.7μF decoupling ceramic capacitor close to the VBAT and the SUPPLY pin of each TPS929160-Q1 to obtain good EMC performance.

STEP 2: Thermal analysis for the worst application conditions.

Normally the thermal analysis is necessary for linear LED-driver applications to ensure that the operation junction temperature of TPS929160-Q1 is well managed. The total power consumption on the TPS929160-Q1 itself is one important factor determining operation junction temperature, and it can be calculated by using the following equation.

$$P_{(MAX)} = \left(V_{(SUPPLY\_MAX)} - V_{(LED\_MIN)}\right) \times I_{(CH)} \times N_{(CH)} \tag{9}$$

where

- $V_{(SPPLY\_MAX)}$ is maximum supply voltage.
- $V_{(LED\_MIN)}$ is minimum output voltage.
- $I_{(CH)}$ is channel current.
- $N_{(CH)}$ is number of used channels.

Based on the worst-case analysis for maximum power consumption on device, either optimizing PCB layout for better power dissipation as *Layout Example* describes or implementing a DC-to-DC converter in previous stage on MCU board can be considered. The DC-to-DC such as a buck converter or buck-boost converter can regulate the battery voltage to be a stable supply for the TPS929160-Q1 with sufficient headroom. A properly designed supply voltage is helpful to minimize the power consumption on the TPS929160-Q1 itself as well as the whole system. In this application, the DC-to-DC converter with 8.6V output voltage can make sure current output on each output channel of TPS929160-Q1 is stable. The calculated maximum power dissipation on the device is 1.36 W as show in the below equation.

$$\begin{aligned} P_{(MAX)} &= (V_{(SUPPLY\_MAX)} - V_{(LED\_MIN)}) \times I_{(CH)} \times N_{(CH)} \\ &= (8.6 - 2.3 \times 3) \times 0.05 \times 16 = 1.36\ W \end{aligned} \tag{10}$$

where

- $V_{(SPPLY\_MAX)}$ is maximum supply voltage.
- $V_{(LED\_MIN)}$ is minimum output voltage.
- $I_{(CH)}$ is channel current.
- $N_{(CH)}$ is number of used channels.

STEP 3: Set up the slave address for individual TPS929160-Q1.

The slave address of TPS929160-Q1 can be configured by ADDR3/ADDR2/ADDR1/ADDR0 pins or DEVADDR[3:0] selected by INTADDR. The detailed description is explained in *UART Interface Address Setting*.

STEP 4: DC current setup for each LED string.

The DC current for all output channel can be programmed by an external resistor, $R_{(REF)}$, and internal register REFRANGE. The resistor value can be calculated by using Equation 11. The manufacturer default value for

$K_{(REF)}$ is 512. If the other number rather than 512 is chosen for DC current setting, the selected code needs to be burnt into EEPROM to change the default value for REFRANGE. A 1nF ceramic capacitor is recommended to be placed in parallel with $R_{(REF)}$ resistor to improve the noise immunity. The 6-bit register IOUTXn can be used to program DC current for each output channel independently mainly for dot correction purpose. The code setting for IOUTXn registers must be decided in the end of production line according to the LED calibration result. The detailed calculation is described in *64-Step Programmable High-Side Constant-Current Output*.

$$R_{(REF)} = \frac{V_{(REF)}}{I_{(FULL\_RANGE)}} \times K_{(REF)} \tag{11}$$

where

- $V_{(REF)}$ = 1.235V typically.
- $K_{(REF)}$ = 64, 128, 256 or 512 (default).

Table 7-1. Reference Current Range Setting

CURRENT (mA)	REFRANGE	$K_{(REF)}$	REF RESISTOR VALUE (kΩ)
50	11b	512	12.7
	10b	256	6.34
	01b	128	3.16
	00b	64	1.58

TI recommends placing a 1nF ceramic capacitor on each of output channels to achieve good EMC performance.

STEP 5: Design the configuration for PWM generator. Basically, there are three main parameters for PWM generator that must be considered, including:

- PWM frequency is set by PWMFREQ. The detailed calculation and description is explained in *PWM Dimming Frequency*. The default value of PWMFREQ can be changed by burning the target value to EEPROM.
- PWM duty cycle is set by PWMOUTXn and PWMLOWOUTXn. The detailed calculation and description are explained in *Linear Brightness Control*. The default value of PWMOUTXn and PWMLOWOUTXn can be changed by burning the target value to EEPROM.
- PWM dimming method set by EXPEN. The detailed calculation and description are explained in *Exponential Brightness Control*. The default value of EXPEN can be changed by burning the target value to EEPROM.

STEP 6: Design the diagnostics configuration. The diagnostics configuration for both NORMAL state and FAIL-SAFE states must be set up properly based on the system requirements. The following configuration registers must be designed:

- Low-supply warning threshold set by LOWSUPTH. The detail calculation and description are explained in *Low-Supply Warning Diagnostics in NORMAL State*. The default value of LOWSUPTH can be changed by burning the target value to EEPROM.
- Diagnostics enabling setup for each channel by CONF_DIAGENCHx. The diagnostics for each channel can be enabled or disabled by DIAGENOUTXn register. The detailed description is explained in *Fault Masking*. The default value of DIAGENOUTXn can be changed by burning the target value to EEPROM.
- Single-LED short-circuit configuration by SLSEN, SLSTHOUTXn, SLSTH0 and SLSTH1. The detailed calculation and description are explained in *Single-LED Short-Circuit Detection in NORMAL state*. The default value of SLSEN, SLSTHOUTXn, SLSTH0 and SLSTH1 can be changed by burning the target value to EEPROM.
- FAIL-SAFE state access watchdog timer setup by WDTIMER. The detailed calculation and description are explained in *NORMAL state*. The default value of WDTIMER can be changed by burning the target value to EEPROM.
- Channel setup in FAIL-SAFE state. In FAIL-SAFE state, the FS pin can be used as control signal to turn on or turn off the corresponding channel. Each current output channel has its own register, FSOUTXn to set the mapping to FS0 or FS1. When FSOUTXn is set to 0, the corresponding current output channel is controlled

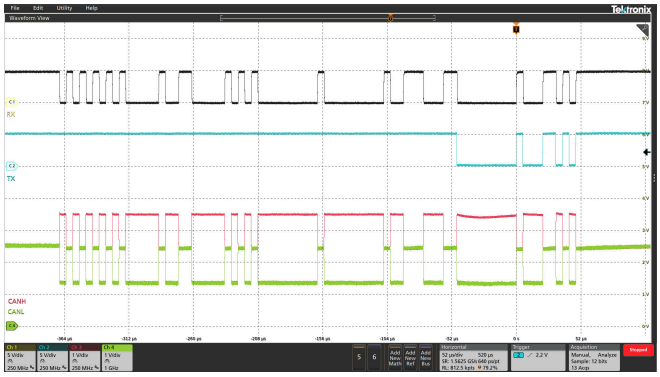
by FS0 input, otherwise it is controlled by FS1 input. The detailed calculation and description are explained in *FAIL-SAFE State Operation*.

- One-fails-all-fail setup by OFAF. If the one-fails-all-fail can be enabled by burning 1 to OFAF according to system requirements. Tie the $\overline{ERR}$ pins for all TPS929160-Q1 in the system together with a single 4.7kΩ pullup resistor to realize the one-fails-all-fail feature. The detailed calculation and description is explained in *OFAF Setup In FAIL-SAFE State*.
- CRC check reference calculation for EEPCRC. After all the EEPROM register values are designed, the CRC reference value for all EEPROM register must be calculated and burnt into EEPCRC. The detailed calculation and description are explained in *EEPROM CRC Error in NORMAL state*.

STEP 7: EEPROM burning solution design.

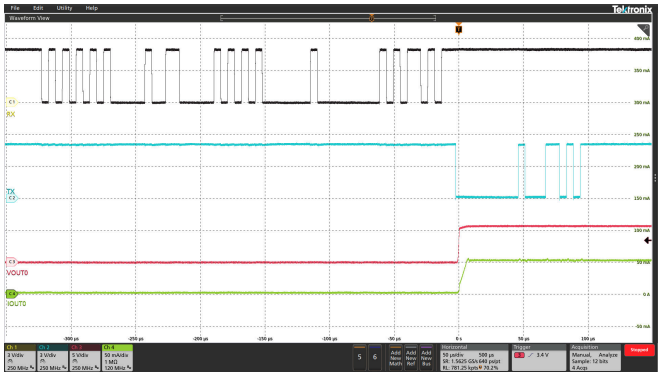
TI recommends that the EEPROM burning be done in the end of production line. The detailed flow is introduced in *EEPROM Register Access and Burn* .

7.2.4 Application Curves



CH1 = RX CH2 = TC CH3 = CANH
CH4 = CANL

Figure 7-3. CAN Transceiver Operating



CH1 = RX CH2 = TX CH3 = $V_{(OUT0)}$
CH4 = $I_{(OUT0)}$

Figure 7-4. Output Control by FlexWire Interface

7.3 Power Supply Recommendations

The TPS929160-Q1 is designed to operate from an automobile electrical power system within the range specified in *Power Supply (SUPPLY)* and *Power Bias (VBAT)*. The $V_{(SUPPLY)}$ input must be protected from the reverse voltage and the voltage dump condition over 40V. The impedance of the input supply voltage source must be low enough that the input current transient does not cause the input voltage at the supply pin of device to drop below LED string required forward voltage. If the input supply is connected with long wires, additional bulk capacitance is required in addition to normal input capacitor.

7.4 Layout

7.4.1 Layout Guidelines

Thermal dissipation is the primary consideration for TPS929160-Q1 layout. TI recommends that a large thermal dissipation area should be connected to the thermal pads with multiple thermal vias. Place the capacitor for SUPPLY input, VBAT input and VLDO output as close as possible to the pins. The $R_{(REF)}$ resistor must also be placed as close as possible to the REF pin together with 1-nF capacitor for enhanced noise immunity. A 1nF ceramic capacitor is recommended to be put closely to each of output channels to achieve good EMC performance.

7.4.2 Layout Example

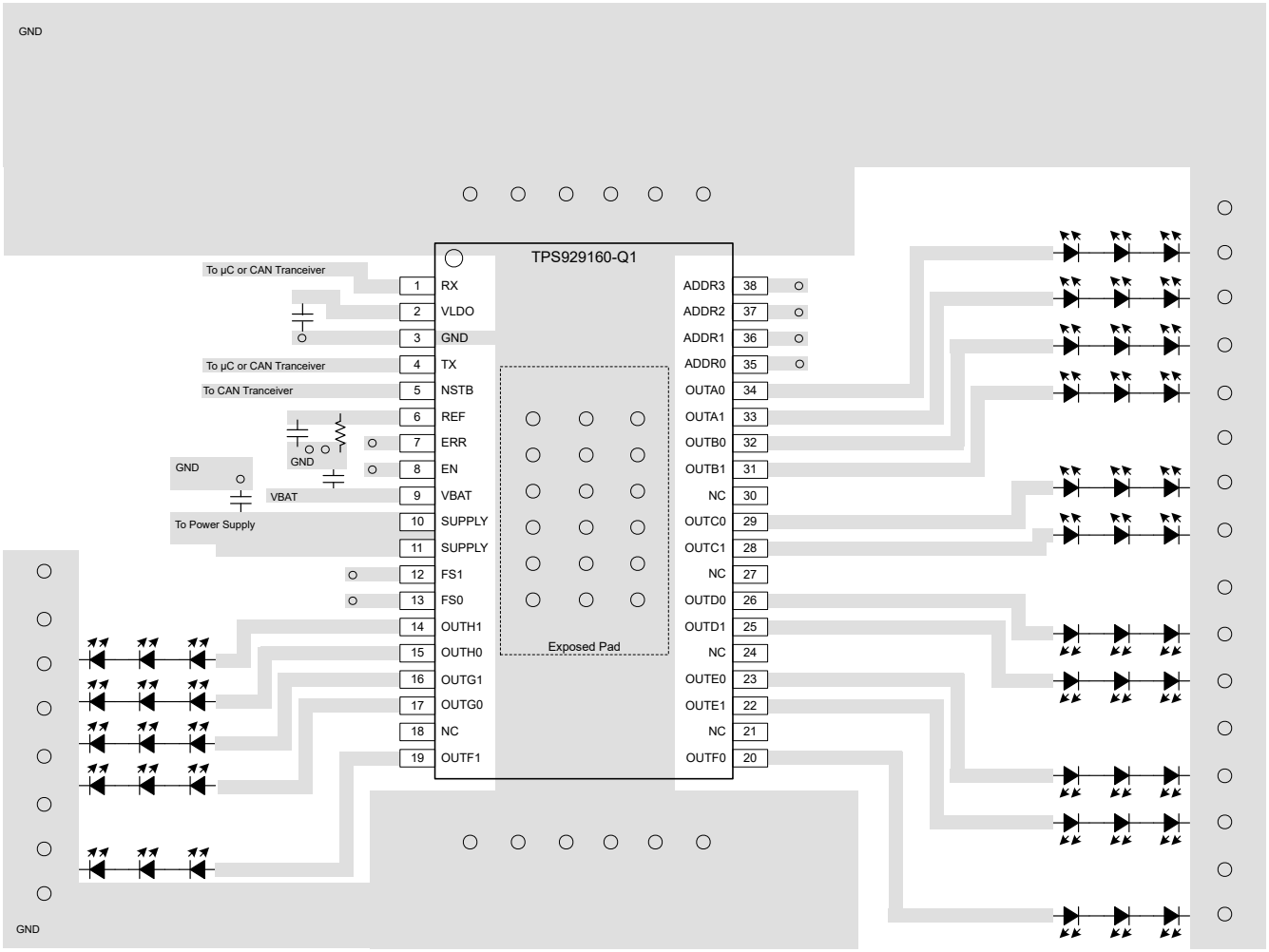


Figure 7-5. TPS929160-Q1 Layout

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2023) to Revision A (April 2024)	Page
• Updated Communication Loss Diagnostic in NORMAL state	33
• Updated Protocol Overview	46

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS929160QDCPRQ1	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	929160Q
TPS929160QDCPRQ1.A	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	929160Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

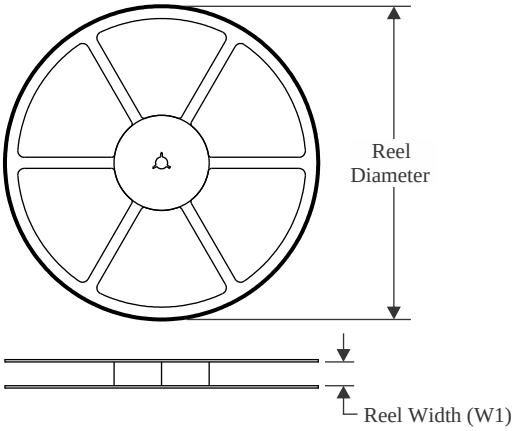
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

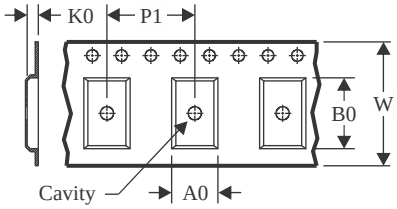
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

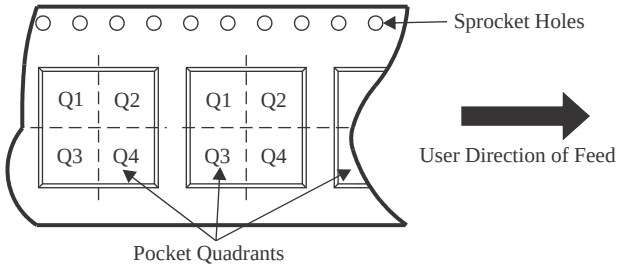


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

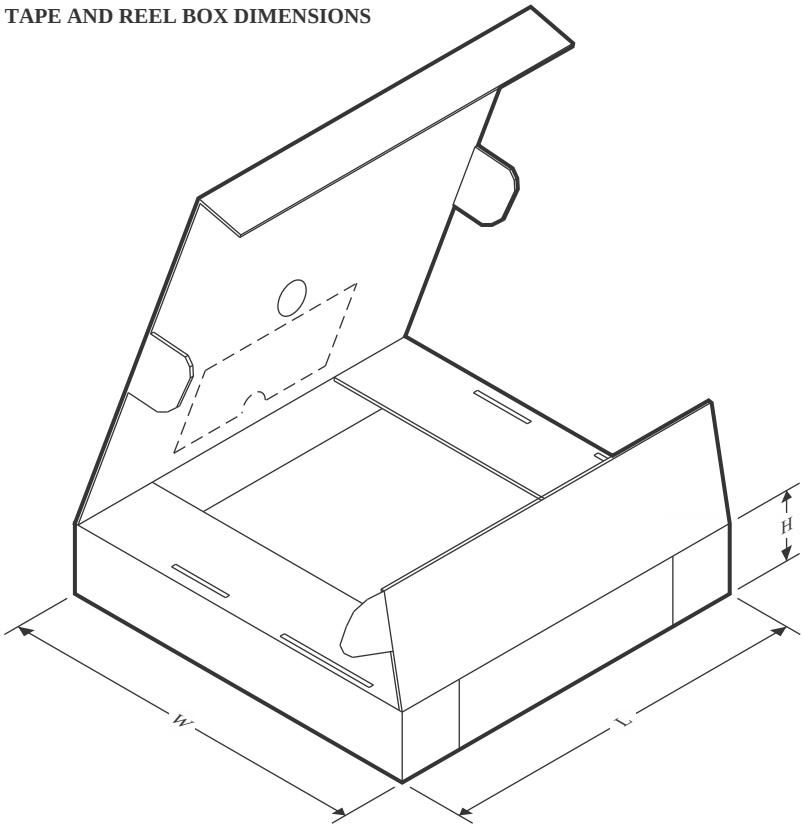
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS929160QDCPRQ1	HTSSOP	DCP	38	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS929160QDCPRQ1	HTSSOP	DCP	38	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

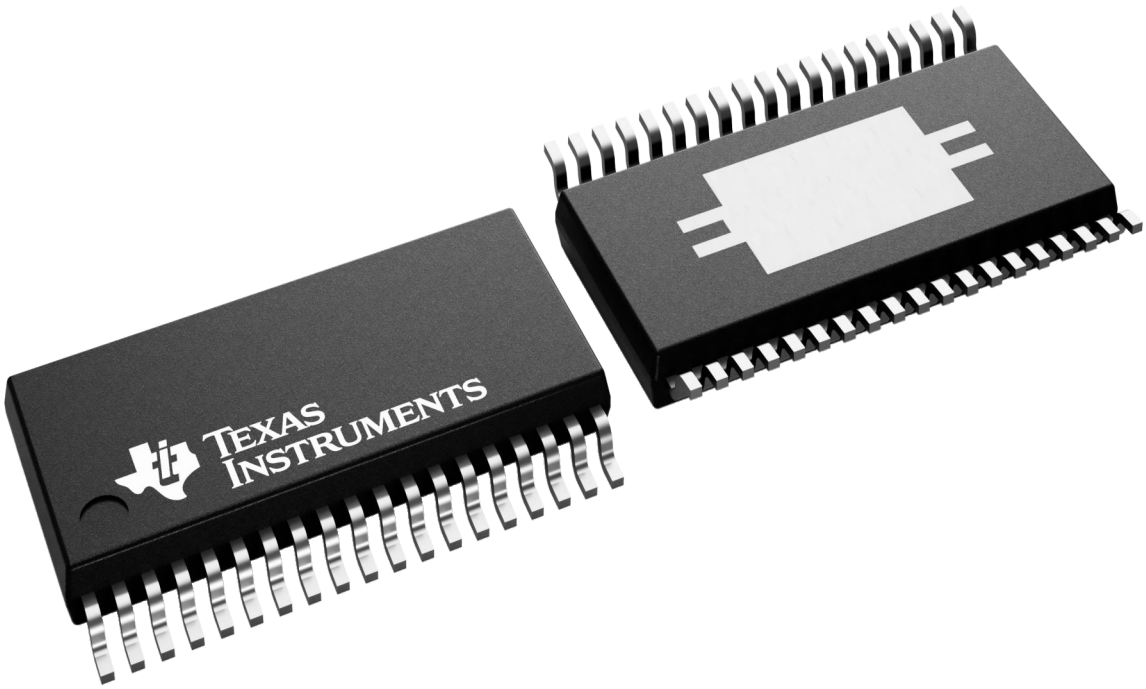
DCP 38

PowerPAD TSSOP - 1.2 mm max height

4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

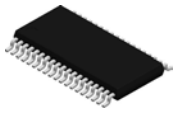
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224560/B

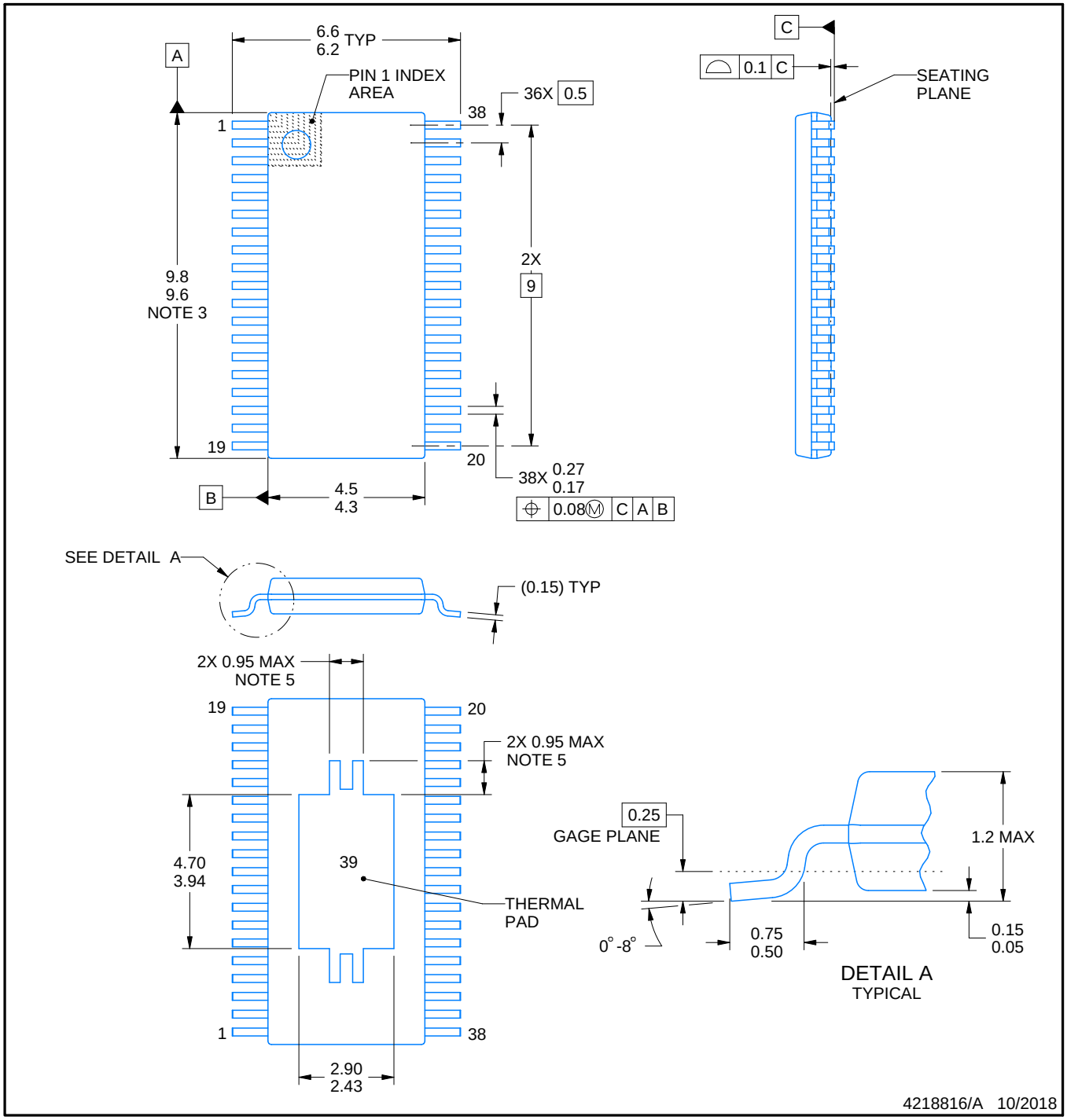
PACKAGE OUTLINE

DCP0038A



PowerPAD™ TSSOP - 1.2 mm max height

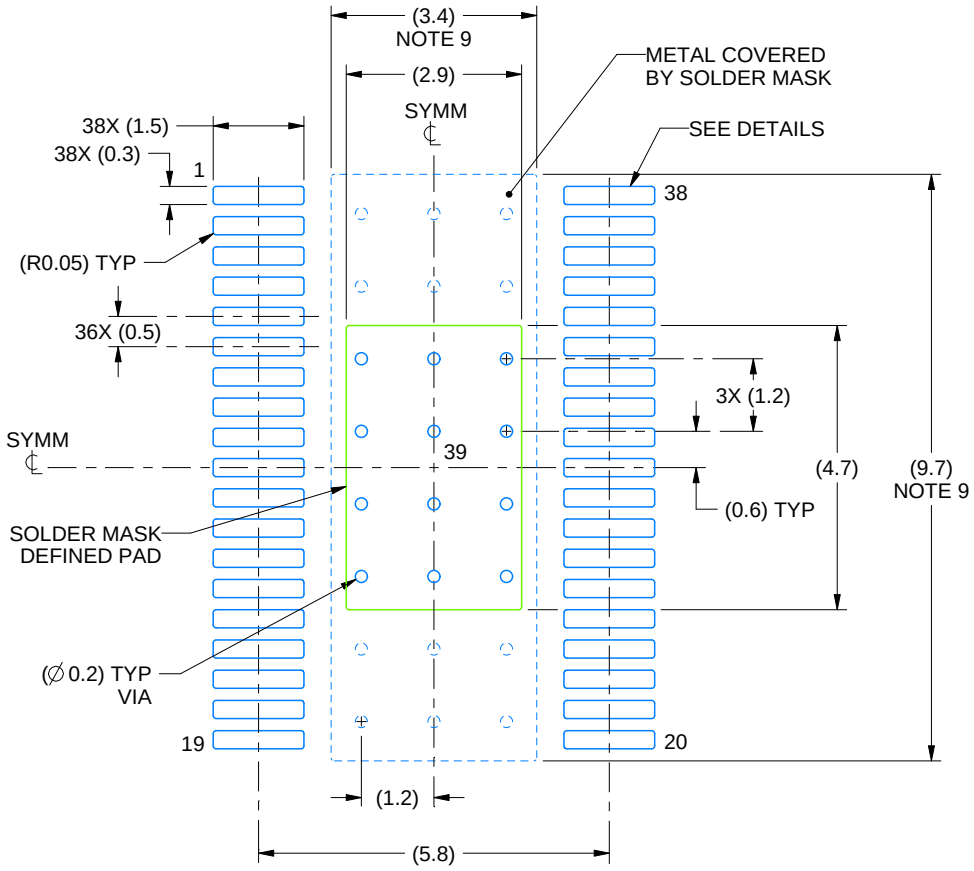
SMALL OUTLINE PACKAGE



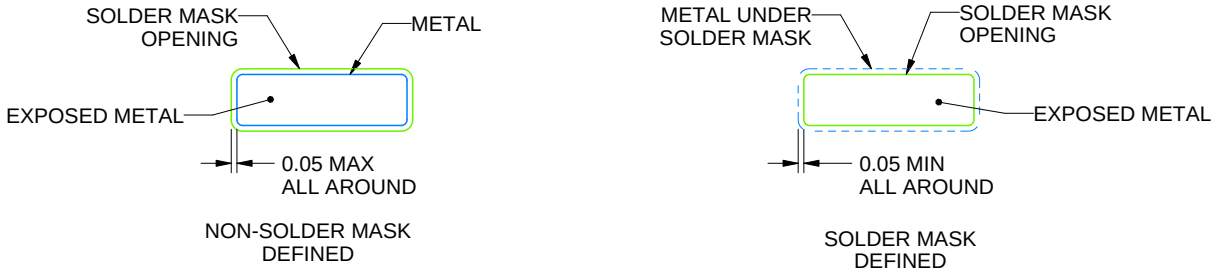
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

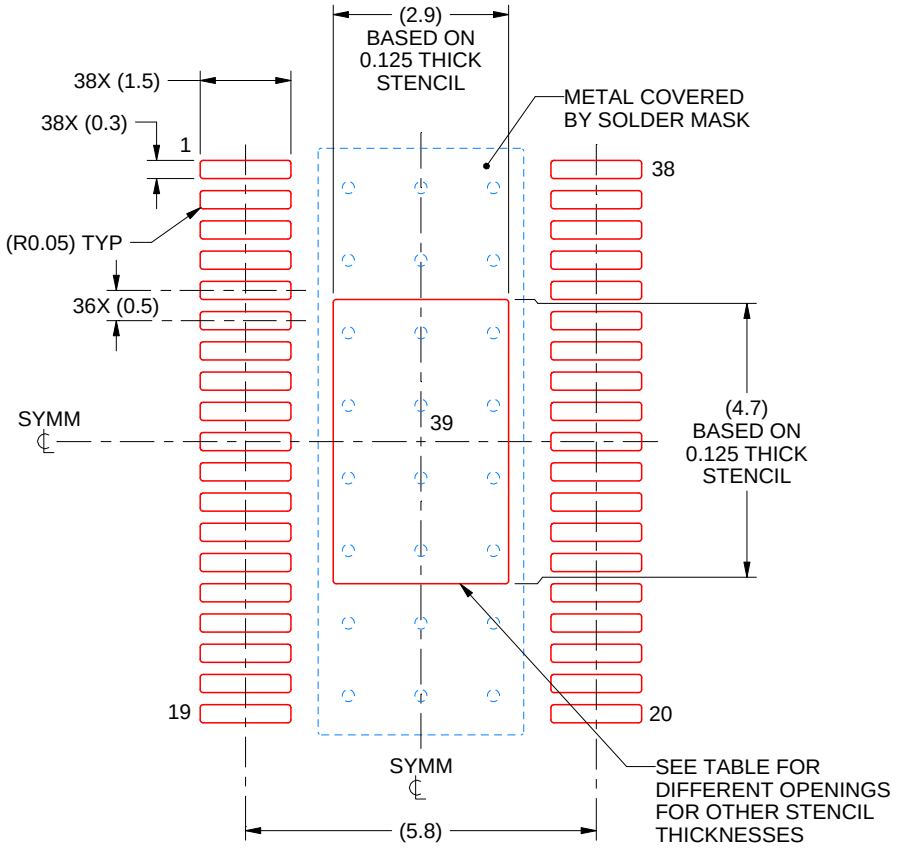


SOLDER MASK DETAILS

4218816/A 10/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

4218816/A 10/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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