





**TPS82130** 

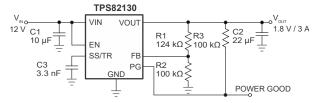
# TPS82130 17-V Input 3-A Step-Down Converter MicroSiP™ Power Module with **Integrated Inductor**

#### 1 Features

- 3-mm × 2.8-mm × 1.5-mm MicroSiP package
- 3-V to 17-V input range
- 3-A continuous output current
- DCS-Control topology
- Power save mode for light-load efficiency
- 20-µA operating quiescent current
- 0.9-V to 6-V adjustable output voltage
- 100% duty cycle for lowest dropout
- Power-good output
- Programmable soft start-up with tracking
- Thermal shutdown protection
- -40°C to 125°C operating temperature range
- Mandarin data sheet available
- Create a custom design using the TPS82130 with the WEBENCH® Power Designer

# 2 Applications

- Industrial applications
- Telecom and networking applications
- Solid state drives



Simplified Schematic 1.8-V Output Application

# 3 Description

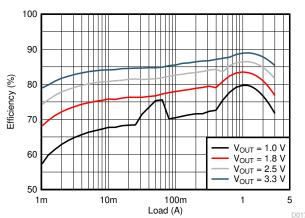
The TPS82130 is a 17-V input 3-A step-down converter MicroSiP power module optimized for small solution size and high efficiency. The module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components, and save PCB area. The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 2 MHz and automatically enters power save mode operation at light load currents. In power save mode, the device operates with 20-µA (typical) quiescent current. Using the DCS-Control topology, the device achieves excellent load transient performance and accurate output voltage regulation.

#### **Package Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
TPS82130	SIL (µSiL, 8)	3.00 mm × 2.80 mm

For all available packages, see the orderable addendum at the end of the data sheet.



12-V Input Voltage Efficiency



# **Table of Contents**

1 Features1	7.4 Device Functional Modes	9
2 Applications1	8 Application and Implementation	11
3 Description1	8.1 Application Information	
4 Revision History2	8.2 Typical Applications	
5 Pin Configuration and Functions3	8.3 Power Supply Recommendations	
6 Specifications4	8.4 Layout	. 17
6.1 Absolute Maximum Ratings4	9 Device and Documentation Support	
6.2 ESD Ratings4	9.1 Device Support	. 18
6.3 Recommend Operating Conditions4	9.2 Documentation Support	
6.4 Thermal Information4	9.3 Receiving Notification of Documentation Updates	18
6.5 Electrical Characteristics5	9.4 Support Resources	. 18
6.6 Typical Characteristics6	9.5 Trademarks	18
7 Detailed Description7	9.6 Glossary	18
7.1 Overview7	9.7 Electrostatic Discharge Caution	
7.2 Functional Block Diagram7	10 Mechanical, Packaging, and Orderable	
7.3 Feature Description7	Information	. 20

# **4 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

•	'	•			
Changes f	rom Revision E (Octo	ber 2021) to Revisi	on F (January 202	3)	Page
<ul> <li>Added a</li> </ul>	a hyperlink to the trans	lated mandarin data	sheet		1
<ul> <li>Updated</li> </ul>	d trademark information	n			1
	Documentation Suppor				
Changes f	rom Revision D (Nov	ember 2018) to Rev	ision E (October 2	2021)	Page
• Updated	d the numbering forma	t for tables, figures, a	and cross-reference	s throughout the de	ocument1

# **5 Pin Configuration and Functions**

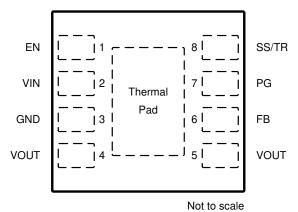


Figure 5-1. SIL 8-Pin µSiL Package (SIL0008C Top View)

**Table 5-1. Pin Functions** 

	DIN				
PIN		I/O	DESCRIPTION		
NAME	NO.		DECOM! HOW		
EN	1	I	Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pulldown resistor of typically 400 k $\Omega$ when the device is disabled.		
VIN	2	PWR	Input pin		
GND	3		Ground pin		
VOUT	4, 5	PWR	Output pin		
FB	6	I	Feedback reference pin. An external resistor divider connected to this pin programs the output voltage.		
PG	7	0	Power-good open-drain output pin. A pullup resistor can be connected to any voltage less than 6 V. Leave this pin open if it is not used.		
SS/TR	8	I	Soft start-up and voltage tracking pin. An external capacitor connected to this pin sets the internal reference voltage rising time.		
Exposed Therr	mal Pad		The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.		

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# **6 Specifications**

# **6.1 Absolute Maximum Ratings**

		MIN	MAX	UNIT
	VIN	-0.3	20	
Voltage at pins <sup>(1)</sup> (2)	EN, SS/TR	-0.3	V <sub>IN</sub> + 0.3	V
voltage at pins (**/ (=*/	PG, FB	-0.3	7	V
	VOUT	0	7	
Sink current <sup>(1)</sup>	PG		10	mA
Module operating temp	erature <sup>(1)</sup>	-40	125	°C
Storage temperature <sup>(1)</sup>		<b>-</b> 55	125	°C

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

# **6.3 Recommend Operating Conditions**

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	3	17	V
$V_{PG}$	Power good pull-up resistor voltage		6	V
V <sub>OUT</sub>	Output voltage	0.9	6	V
I <sub>OUT</sub>	Output current	0	3	Α
TJ	Module operating temperature range for 100,000 hours lifetime <sup>(1)</sup>	-40	110	°C

<sup>(1)</sup> The module operating temperature range includes module self temperature rise and IC junction temperature rise. In applications where high power dissipation is present, the maximum operating temperature or maximum output current must be derated. For applications where the module operates continuously at 125 °C temperature, the maximum lifetime is reduced to 50,000 hours.

## 6.4 Thermal Information

	THERMAL METRIC(1)	TPS82130 (JEDEC 51-5)	TPS82130EVM-720	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.2	46.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	9.4	9.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	14.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.9	0.9	°C/W
ΨЈВ	Junction-to-board characterization parameter	14.2	14.0	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	21.3	21.3	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the <u>Semiconductor and IC Package Thermal Metrics</u> application report. Theta-JA can be improved with a custom PCB design containing thermal vias where possible.

Product Folder Links: TPS82130

<sup>(2)</sup> All voltage values are with respect to network ground pin.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



# **6.5 Electrical Characteristics**

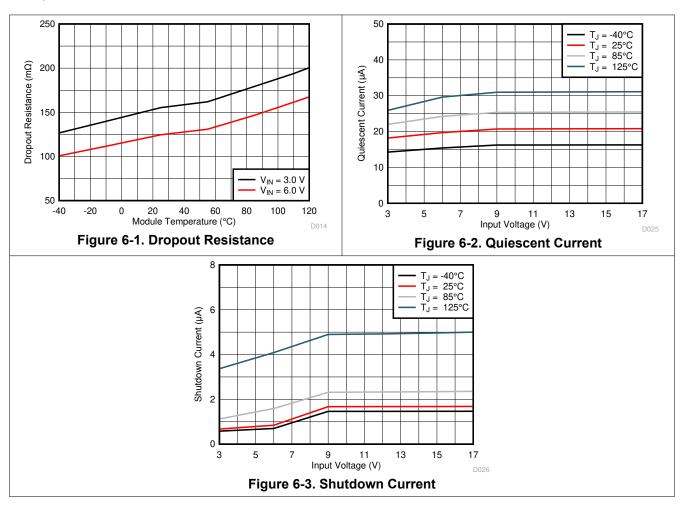
 $T_J$  = -40°C to 125°C and  $V_{IN}$  = 3.0 V to 17 V. Typical values are at  $T_J$  = 25°C and  $V_{IN}$  = 12 V, unless otherwise noted.

-	PARAMETER		TEST CONDITIONS			MAX	UNIT
SUPPL	Y						
IQ	Quiescent current into VIN	No load, device no	ot switching		20	35	μA
I <sub>SD</sub>	Shutdown current into VIN	EN = Low			1.5	7.4	μA
.,		V <sub>IN</sub> falling	IN falling		2.7	2.8	V
$V_{UVLO}$	Undervoltage lockout threshold	V <sub>IN</sub> rising		2.8	2.9	3.0	V
т	Thermal shutdown threshold	T <sub>J</sub> rising			160		°C
$T_{JSD}$	Thermal shutdown threshold	T <sub>J</sub> falling			140		°C
LOGIC	INTERFACE (EN)			·			
$V_{\text{IH}}$	High-level input voltage			0.9	0.65		V
$V_{IL}$	Low-level input voltage				0.45	0.3	V
$I_{lkg(EN)}$	Input leakage current into the EN pin	EN = High			0.01	1	μΑ
CONTR	ROL (SS/TR, PG)	1		· · · · · · · · · · · · · · · · · · ·			
I <sub>SS/TR</sub>	SS/TR pin source current			2.1	2.5	2.8	μΑ
\/	Dower good threshold	V <sub>OUT</sub> rising, refere	nced to V <sub>OUT</sub> nominal	92%	95%	99%	
$V_{PG}$	Power-good threshold	V <sub>OUT</sub> falling, refere	enced to V <sub>OUT</sub> nominal	87%	90%	94%	
$V_{PG,OL}$	Power-good low-level voltage	I <sub>sink</sub> = 2 mA	I <sub>sink</sub> = 2 mA		0.1	0.3	V
I <sub>lkg(PG)</sub>	Input leakage current into the PG pin	V <sub>PG</sub> = 1.8 V			1	400	nA
OUTPL	JT						
	Feedback regulation voltage	PWM mode		785	800	815	mV
V		1 WWW IIIOGE	$T_J = 0$ °C to 85°C	788	800	812	
$V_{FB}$		PSM	C <sub>OUT</sub> = 22 μF	785	800	823	
		1 SIVI	$C_{OUT} = 2 \times 22 \mu F$ , $T_{J} = 0^{\circ}C$ to 85°C	788	800	815	
$I_{lkg(FB)}$	Feedback input leakage current	V <sub>FB</sub> = 0.8 V			1	100	nA
	Line regulation	I <sub>OUT</sub> = 1 A, V <sub>OUT</sub> =	1.8 V		0.002		%/V
	Load regulation	$I_{OUT} = 0.5 A \text{ to } 3 A$	a, V <sub>OUT</sub> = 1.8 V		0.12		%/A
POWE	R SWITCH						
	High-side FET on-resistance	$I_{SW}$ = 500 mA, $V_{IN}$	≥ 6 V		90	170	
R <sub>DS(on</sub>	riigii-side i E i Oil-lesistance	I <sub>SW</sub> = 500 mA, V <sub>IN</sub> = 3 V			120		mΩ
)	Low-side FET on-resistance	I <sub>SW</sub> = 500 mA, V <sub>IN</sub> ≥ 6 V			40	70	
	Low-side i E i on-resistance	I <sub>SW</sub> = 500 mA, V <sub>IN</sub> = 3 V			50		
Ros	Dronout resistance	100% mode, V <sub>IN</sub> ≥ 6 V			125		mΩ
R <sub>DP</sub>	Dropout resistance	100% mode, V <sub>IN</sub> = 3 V			160		11122
I <sub>LIMF</sub>	High-side FET switch current limit	$V_{IN} = 6 \text{ V}, T_A = 25^{\circ}$	°C	3.6	4.2	4.9	Α
f <sub>SW</sub>	PWM switching frequency	I <sub>OUT</sub> = 1 A, V <sub>OUT</sub> =	1.8 V		2.0		MHz

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# **6.6 Typical Characteristics**



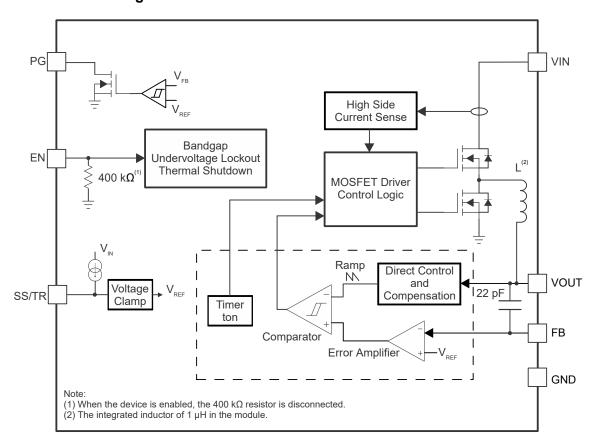
# 7 Detailed Description

#### 7.1 Overview

The TPS82130 synchronous step-down converter MicroSiP power module is based on DCS-Control (Direct Control with Seamless transition into power save mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in PSM (power save mode) at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.0 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the quiescent current of the IC to achieve high efficiency over the entire load current range. DCS-Control supports both operation modes using a single building block and therefore has a seamless transition from PWM to PSM without effects on the output voltage. The TPS82130 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

## 7.2 Functional Block Diagram



# 7.3 Feature Description

## 7.3.1 PWM and PSM Operation

The TPS82130 includes an on-time ( $t_{ON}$ ) circuitry.  $t_{ON}$ , in steady-state operation in PWM and PSM modes, is estimated as:

$$t_{ON} = 500 \text{ns} \times \frac{V_{OUT}}{V_{IN}} \tag{1}$$

In PWM mode, the TPS82130 operates with pulse width modulation in continuous conduction mode (CCM) with a  $t_{ON}$  shown in Equation 1 at medium and heavy load currents. A PWM switching frequency of typically 2.0 MHz



is achieved by this  $t_{ON}$  circuitry. The device operates in PWM mode as long as the output current is higher than half of the ripple current of the inductor estimated by Equation 2.

$$\Delta I_{L} = t_{ON} \times \frac{V_{IN} - V_{OUT}}{L} \tag{2}$$

To maintain high efficiency at light loads, the device enters power save mode seamlessly when the load current decreases. This happens when the load current becomes smaller than half of the ripple current of the inductor. In PSM, the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency. PSM is also based on the ton circuitry. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}}$$
(3)

In PSM, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance. The output voltage accuracy in PSM operation is reflected in Section 6.5 and given for a  $22-\mu F$  output capacitor.

For very small output voltages, an absolute minimum on time of approximately 80 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also, the off time can reach its minimum value at high duty cycles. The output voltage remains regulated in such cases.

When  $V_{IN}$  decreases to typically 15% above  $V_{OUT}$ , the TPS82130 cannot enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

# 7.3.2 Low Dropout Operation (100% Duty Cycle)

The TPS82130 offers a low input to output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP}$$
(4)

where

- R<sub>DP</sub> = Resistance from V<sub>IN</sub> to V<sub>OUT</sub>, including high-side FET on-resistance and DC resistance of the inductor
- V<sub>OUT(min)</sub> = Minimum output voltage the load can accept

#### 7.3.3 Switch Current Limit

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a heavy load/shorted output circuit condition. If the inductor peak current reaches the switch current limit after a propagation delay of typically 30 ns, the high-side FET is turned off and the low-side FET is turned on to ramp down the inductor current.

#### 7.3.4 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is implemented, which shuts down the device at voltages lower than  $V_{UVLO}$  with a hysteresis of 200 mV.

#### 7.3.5 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T<sub>JSD</sub>. After the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

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#### 7.4 Device Functional Modes

#### 7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic High. Accordingly, shutdown mode is forced if the EN pin is pulled Low with a shutdown current of typically 1.5 µA.

An internal 400-k $\Omega$  pulldown resistor is connected to the EN pin when the EN pin is Low. The pulldown resistor is disconnected when the EN pin is High.

#### 7.4.2 Soft Start-Up (SS/TR)

The internal voltage clamp controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output voltage rise time. When the EN pin is pulled high, the device starts switching after a delay of typically 55 µs and the output voltage rises with a slope controlled by an external capacitor connected to the SS/TR pin. Using a very small capacitor or leaving the SS/TR pin floating provides the fastest start-up time.

The TPS82130 is able to start into a pre-biased output capacitor. During the pre-biased start-up, both the power MOSFETs are not allowed to turn on until the internal voltage clamp sets an output voltage above the pre-bias voltage.

When the device is in shutdown, undervoltage lockout, or thermal shutdown, the capacitor connected to the SS/TR pin is discharged by an internal resistor. Returning from those states causes a new start-up sequence.

## 7.4.3 Voltage Tracking (SS/TR)

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in Figure 7-1.

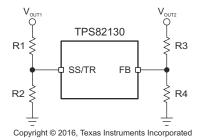


Figure 7-1. Output Voltage Tracking

When the SS/TR pin voltage is between 50 mV and 1.2 V, the VOUT2 tracks the VOUT1 as described in Equation 5.

$$\frac{V_{OUT2}}{V_{OUT1}} \approx 0.64 \times \frac{R2}{R1 + R2} \times \frac{R3 + R4}{R4}$$
(5)

When the SS/TR pin voltage is above 1.2 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.8 V. To decrease the SS/TR pin voltage, the device does not sink current from the output, so the resulting decreases of the output voltage can be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is VIN + 0.3 V.

Details about tracking and sequencing circuits are found in the Sequencing and Tracking With the TPS621-Family and TPS821-Family Application Report.

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# 7.4.4 Power-Good Output (PG)

The device has a power-good (PG) output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 2 mA. The power good output requires a pullup resistor connecting to any voltage rail less than 6 V.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin floating when it is not used. Table 7-1 shows the PG pin logic.

Table 7-1. Power Good Pin Logic

DEVICE	STATE	PG LOGIC STATUS		
DEVICE	SIAIE	HIGH IMPEDANCE	LOW	
Enable (EN=High)	V <sub>FB</sub> ≥ V <sub>TH_PG</sub>	V		
Enable (EN-Figh)	V <sub>FB</sub> ≤ V <sub>TH_PG</sub>		$\sqrt{}$	
Shutdown (EN = Low)			$\sqrt{}$	
UVLO	0.7 V < V <sub>IN</sub> < V <sub>UVLO</sub>		$\sqrt{}$	
Thermal Shutdown	T <sub>J</sub> > T <sub>SD</sub>		$\sqrt{}$	
Power Supply Removal	V <sub>IN</sub> < 0.7 V	√ V		

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# 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The output voltage of the TPS82130 is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

# 8.2 Typical Applications

## 8.2.1 1.8-V Output Application

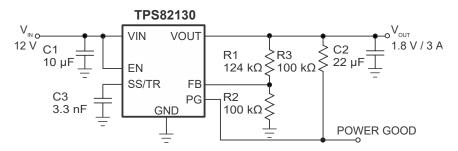


Figure 8-1. 1.8-V Output Application

# 8.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12 V
Output voltage	1.8 V
Output ripple voltage	< 20 mV
Output current rating	3 A

The components used for measurements are given in the following table.

**Table 8-2. List of Components** 

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 μF, 25 V, X7R, ±20%, size 1206, C3216X7R1E106M160AE	TDK
C2	22 μF, 10 V, ±20%, X7S, size 0805, C2012X7S1A226M125AC	TDK
C3	3300 pF, 50 V, ±5%, C0G/NP0, size 0603, GRM1885C1H332JA01D	Murata
R1, R2, R3	Standard	

#### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS82130 device with the WEBENCH Power Designer.

- 1. Start by entering your V<sub>IN</sub>, V<sub>OUT</sub>, and I<sub>OUT</sub> requirements.
- 2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
- 3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
- 4. In most cases, you will also be able to:
  - Run electrical simulations to see important waveforms and circuit performance
  - · Run thermal simulations to understand the thermal performance of your board
  - · Export your customized schematic and layout into popular CAD formats
  - · Print PDF reports for the design, and share your design with colleagues
- 5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 8.2.1.2.2 Setting the Output Voltage

The output voltage is set by an external resistor divider according to Equation 6:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8 \text{ V} \times \left(1 + \frac{R1}{R2}\right)$$
 (6)

R2 must not be higher than 100 k $\Omega$  to achieve high efficiency at light load while providing acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. Figure 8-1 shows the external resistor divider value for a 1.8-V output. Choose appropriate resistor values for other outputs.

In case the FB pin gets opened, the device clamps the output voltage at the VOUT pin internally to approximately 7 V.

#### 8.2.1.2.3 Input and Output Capacitor Selection

For the best output and input voltage filtering, low-ESR ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. A 10- $\mu$ F or larger input capacitor is required. The output capacitor value can range from 22  $\mu$ F up to more than 400  $\mu$ F. Higher values are possible as well and can be evaluated through the transient response. TI recommends larger soft start times for higher output capacitances.

High capacitance ceramic capacitors have a DC bias effect, which have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

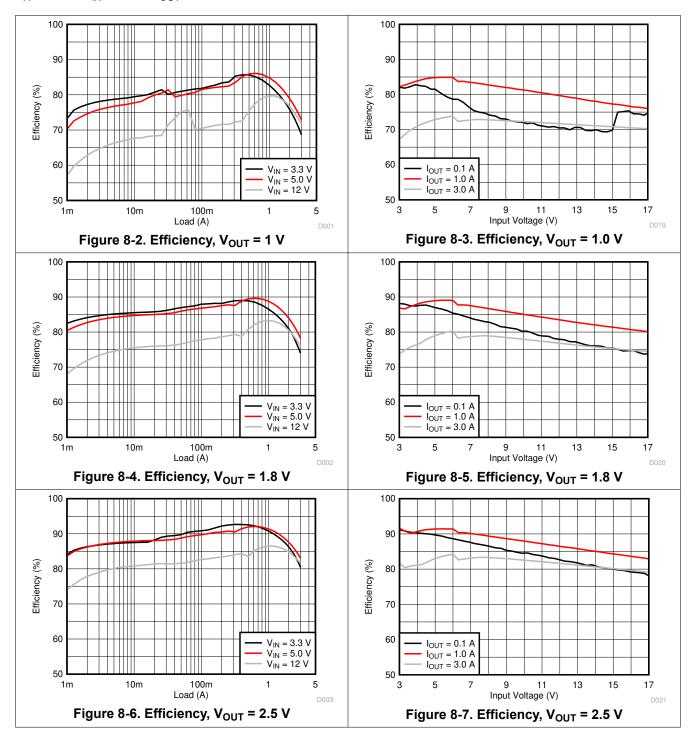
#### 8.2.1.2.4 Soft Start-Up Capacitor Selection

A capacitance connected between the SS/TR pin and the GND allows programming the start-up slope of the output voltage. A constant current of  $2.5~\mu A$  charges the external capacitor. The capacitance required for a given soft start-up time for the output voltage is given by:

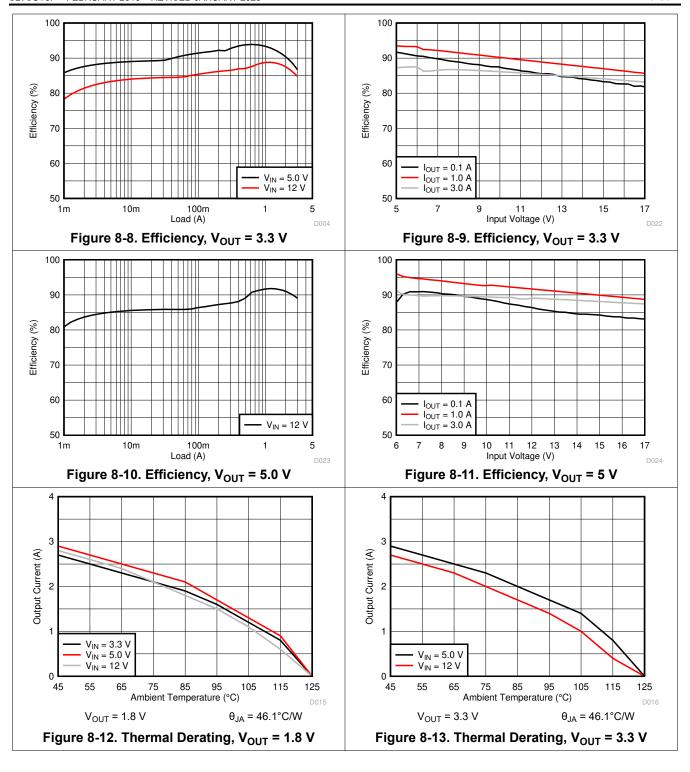
$$C_{SS/TR} = t_{SS/TR} \times \frac{I_{SS/TR}}{1.25V}$$
(7)

# 8.2.1.3 Application Performance Curves

 $T_A = 25$ °C,  $V_{IN} = 12$  V,  $V_{OUT} = 1.8$  V, unless otherwise noted.







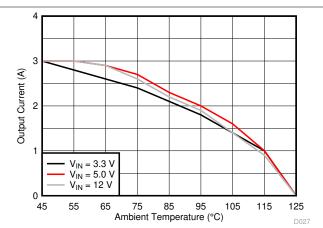


Figure 8-14. Thermal Derating, V<sub>OUT</sub> = 1.0 V

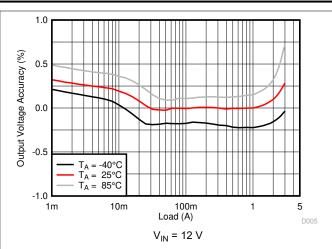


Figure 8-15. Load Regulation

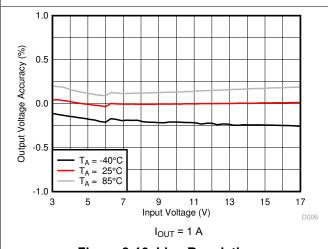


Figure 8-16. Line Regulation

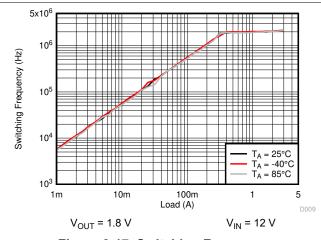


Figure 8-17. Switching Frequency

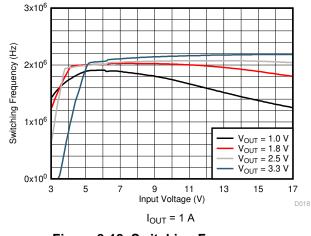


Figure 8-18. Switching Frequency

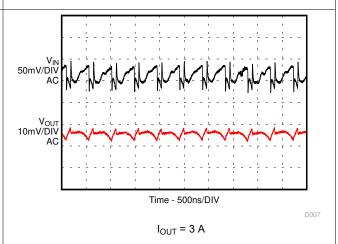
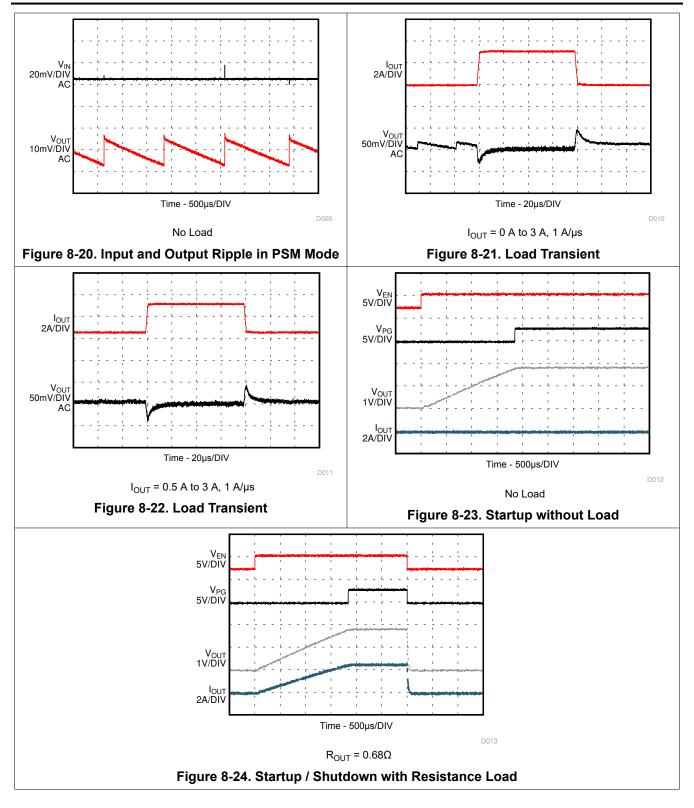


Figure 8-19. Input and Output Ripple in PWM Mode





# 8.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3 V and 17 V. The average input current of the TPS82130 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}}$$
(8)

Ensure that the power supply has a sufficient current rating for the applications.

#### 8.4 Layout

# 8.4.1 Layout Guidelines

- TI recommends placing all components as close as possible to the IC. The input capacitor placement specifically must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- To enhance heat dissipation of the device, the exposed thermal pad must be connected to bottom or internal layer ground planes using vias.
- Refer to Figure 8-25 for an example of component placement, routing, and thermal design.

#### 8.4.2 Layout Example

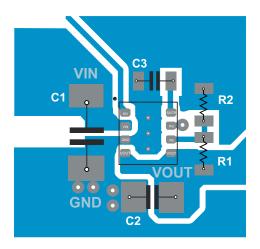


Figure 8-25. TPS82130 PCB Layout

#### 8.4.3 Thermal Consideration

The output current of the TPS82130 must be derated when the device operates in a high ambient temperature or delivers high output power. The amount of current derating is dependent upon the input voltage, output power, PCB layout design, and environmental thermal condition. Care must especially be taken in applications where the localized PCB temperature exceeds 65°C.

The TPS82130 module temperature must be kept less than the maximum rating of 125°C. Three basic approaches for enhancing thermal performance are below:

- · Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the TPS82130 to the PCB.
- Introduce airflow into the system.

To estimate approximate module temperature of TPS82130, apply the typical efficiency stated in this data sheet to the desired application condition to find the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application report* and *Semiconductor and IC Package Thermal Metrics application report*.

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# 9 Device and Documentation Support

# 9.1 Device Support

#### 9.1.1 Development Support

# 9.1.1.1 Third-Party Products Disclaimer

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#### 9.1.1.2 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS82130 device with the WEBENCH Power Designer.

- 1. Start by entering your V<sub>IN</sub>, V<sub>OUT</sub>, and I<sub>OUT</sub> requirements.
- 2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
- 3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
- 4. In most cases, you will also be able to:
  - Run electrical simulations to see important waveforms and circuit performance
  - Run thermal simulations to understand the thermal performance of your board
  - Export your customized schematic and layout into popular CAD formats
  - · Print PDF reports for the design, and share your design with colleagues
- 5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

# 9.2 Documentation Support

#### 9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application report
- · Texas Instruments, Sequencing and Tracking With the TPS621-Family and TPS821-Family application report

#### 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 9.4 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 9.5 Trademarks

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#### 9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.



# 9.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: TPS82130

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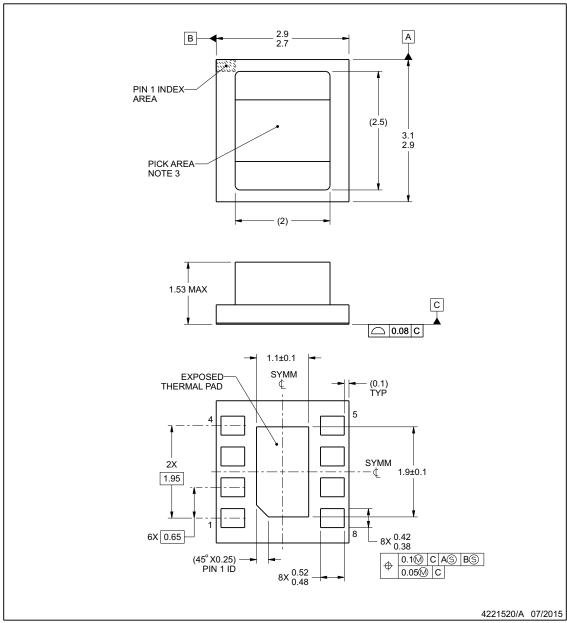
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SIL0008D

# **PACKAGE OUTLINE**

# MicroSiP™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



# NOTES:

MicroSiP is a trademark of Texas Instruments

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
   This drawing is subject to change without notice.
   Pick and place nozzle Ø1.3 mm or smaller recommended.
   The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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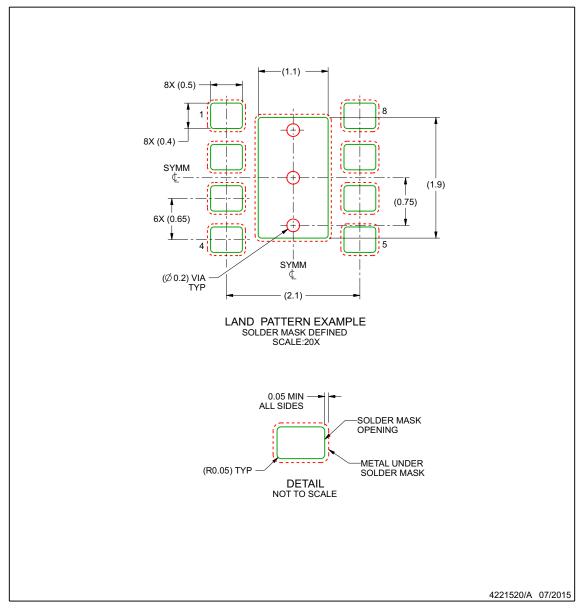


# **EXAMPLE BOARD LAYOUT**

# **SIL0008D**

MicroSiP <sup>™</sup> - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

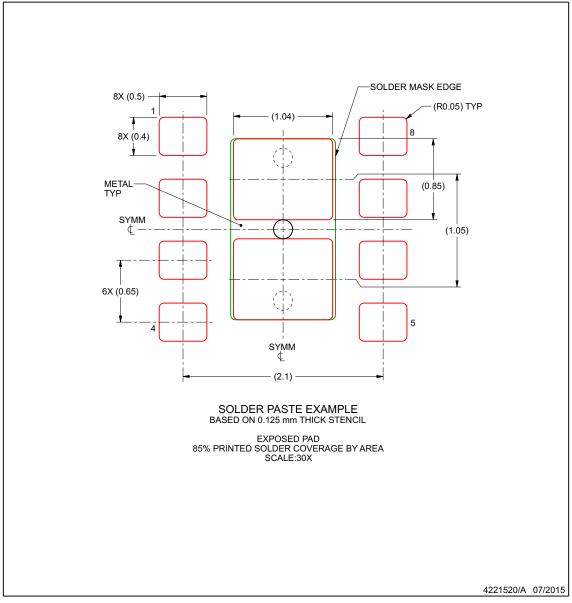
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# **EXAMPLE STENCIL DESIGN**

# **SIL0008D**

# MicroSiP <sup>™</sup> - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TPS82130SILR	Active	Production	uSiP (SIL)   8	3000   LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILR.A	Active	Production	uSiP (SIL)   8	3000   LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILR.B	Active	Production	uSiP (SIL)   8	3000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS82130SILT	Active	Production	uSiP (SIL)   8	250   SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILT.A	Active	Production	uSiP (SIL)   8	250   SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILT.B	Active	Production	uSiP (SIL)   8	250   SMALL T&R	-	Call TI	Call TI	-40 to 125	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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# **PACKAGE MATERIALS INFORMATION**

www.ti.com 6-Jun-2025

# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82130SILR	uSiP	SIL	8	3000	330.0	12.4	3.05	3.25	1.68	8.0	12.0	Q1
TPS82130SILT	uSiP	SIL	8	250	178.0	13.2	3.05	3.25	1.68	8.0	12.0	Q1

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 6-Jun-2025



## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82130SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
TPS82130SILT	uSiP	SIL	8	250	223.0	194.0	35.0

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