TPS7N41Q1 Low-Noise, High-PSRR 1A LDO

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C
  - Junction temperature: –40°C to +150°C
- Adjustable Output Voltage: 0.8V to 5.5V
- Input Voltage Range: 1.9V to 6.0V
- High PSRR:
  - 75dB at 1kHz
  - 50dB at 100kHz
  - 50dB at 1MHz
- Low Noise: 8μV_{RMS}, no NR capacitor needed
- Low Dropout Voltage: 250mV at 1A
- 2% Accuracy over Load, Line, Temperature
- Stable with 4.7µF output capacitor
- Excellent Load and Line Transient Response
- Over-Current and Over-Temperature Protection
- Packages:
  - 3mm × 3mm Wettable Flanks SON-8

2 Applications

- Automotive Head Units
- Instrument Clusters
- Automotive Radar
- Telematics

3 Description

The TPS7N41Q1 low-dropout linear regulator (LDO) offers very good noise and power-supply rejection ratio (PSRR) performance. This LDO uses an advanced BiCMOS process and a PMOSFET pass device to achieve excellent noise, transient response, and PSRR performance.

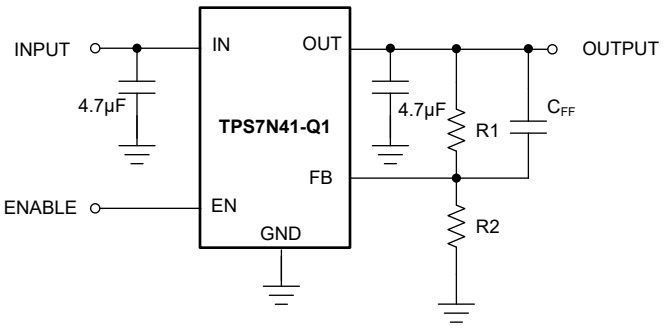
The TPS7N41Q1 is stable with an output capacitor of 4.7µF. A precision voltage reference and feedback loop help the LDO to achieve an accuracy of ±2% over all load, line, process, and temperature variations.

The LDO is specified over the operating junction temperature range from −40°C to +150°C. The device is available in a 3mm × 3mm SON-8 package with wettable flanks.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7N41Q1	DRB (SON, 8)	3mm × 3mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configuration and Functions

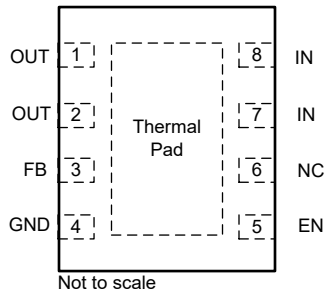


Figure 4-1. DRB Package, 3mm × 3mm, 8-Pin SON (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	DRB		
EN	5	I	Enable input. A low voltage (< $V_{IL(EN)}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage (> $V_{IH(EN)}$) on this pin enables the regulator output.
FB	3	I	Feedback input. Connect the midpoint of the external feedback resistor divider to this input.
GND	4	G	Ground.
IN	7, 8	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground; see the *Recommended Operating Conditions* . Place the input capacitor as close to the IN and GND pins of the device as possible.
NC	6	—	No internal electrical connection. Connect to GND for improved thermal performance.
OUT	1, 2	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *Recommended Operating Conditions* . Place the output capacitor as close to the OUT and GND pins of the device as possible.
Thermal Pad	5	—	Thermal pad for the DRB package. Connect the thermal pad to a large-area ground plane for best thermal performance. If not connected to GND, the thermal pad can be disconnected. Do not connect to any potential other than GND.

(1) I = input, O = output, I/O = input or output, and G = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, EN	–0.3	6.5	V
Voltage	OUT	–0.3	V_{IN} + 0.3(2)	V
Voltage	FB	–0.3	3.6	V
Current	OUT	Internally limited	Internally limited	A
T_J	Operating junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3V or 6.5V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 500V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.9		6.0	V
V_{OUT}	Output voltage range(1)	0.8		5.5	V
V_{EN}	Enable voltage range	0		6.0	V
V_{FB}	Feedback pin voltage		0.8		V
R_2	Bottom resistor value in feedback network for adjustable operation		10	15(2)	kΩ
I_{OUT}	Output current	0		1	A
C_{IN}	Input capacitor	4.7(3)			µF
C_{OUT}	Output capacitor	4.7(4)		100	µF
C_{FF}	Feed-forward capacitor	10	470		nF
ESR	Output capacitor effective resistance			50	mΩ
T_J	Operating junction temperature	–40		150	°C

(1) This output voltage range does not include device accuracy or accuracy of the feedback resistors.
(2) The upper limit for the R_2 resistor is to verify accuracy by making the current through the feedback network much larger than the leakage current into the feedback node.
(3) An input capacitor is not required for LDO stability. However, an input capacitor at least equal to the output capacitor value is recommended to counteract the effect of source resistance and inductance, which in some cases causes symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(4) Effective output capacitance of 2.2µF minimum and 100µF maximum over all temperature and voltage conditions is required for stability. Assuming 50% de-rating for a typical capacitor, COUT has a nominal value of 4.7µF or greater.

5.4 Thermal Information

THERMAL METRIC[1]		DEVICE DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	26.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to +150°C), V_{IN} = 1.9V or V_{IN} = $V_{OUT(NOM)}$ + 0.5V (whichever is greater), $V_{OUT(NOM)}$ = 0.8V, I_{OUT} = 1mA, V_{EN} = 1.0V, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, and C_{FF} = 10nF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage				0.8		V
ΔV_{OUT}	Output voltage tolerance[1]	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 6.0V	V_{IN} ≥ 1.9V, 1mA ≤ I_{OUT} ≤ 500mA	-2		2	%
			V_{IN} ≥ 2.2V, 1mA ≤ I_{OUT} ≤ 1A	-2		2	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 6.0V	V_{IN} ≥ 1.9V, I_{OUT} = 1mA		460		µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	1mA ≤ I_{OUT} ≤ 1A, V_{IN} ≥ 1.9V			4		mV/A
V_{DO}	Dropout voltage	V_{FB} = GND, I_{OUT} = 1A	1.9V ≤ V_{IN} < 2.5V		500	1000	mV
			2.5V ≤ V_{IN} < 3.0V		260	500	mV
			V_{IN} ≥ 3.0V		250	400	mV
I_{CL}	Output current limit	V_{OUT} = 0.85 × $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2.2V, whichever is greater.		1.1	2.0	2.7	A
I_{SC}	Short-circuit current limit	R_{LOAD} = 20mΩ			0.95		
I_{GND}	GND pin current	I_{OUT} = 0mA, V_{IN} = V_{EN} = 6.0V			30	59	µA
I_{GND}	GND pin current	I_{OUT} = 1A			3000	4700	
I_{SD}	GND pin current in shutdown	V_{IN} = 6.0V, V_{EN} = 0V, R_L = 1kΩ			0.8	19	
I_{FB}	FB pin leakage current	V_{IN} = 6.0V, V_{FB} = 0.8V				100	nA
PSRR	Power-supply rejection ratio	V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{FF} = 470nF, C_{OUT} = 10µF, I_{OUT} = 750mA	f = 1kHz		75		dB
			f = 10kHz		70		
			f = 100kHz		50		
			f = 1MHz		50		
V_n	Output noise voltage	Bandwidth = 10Hz to 100kHz, I_{OUT} = 750mA, C_{FF} = 470nF, C_{OUT} = 10µF	V_{IN} = 2.2V, V_{OUT} = 0.8V		8		μV_{RMS}
			V_{IN} = 4.3V, V_{OUT} = 3.3V		9		
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)			0.95		6.0	V
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)			0		0.23	V
I_{EN}	EN pin current	V_{IN} = 6.0V, V_{EN} = 0V and 6.0V				1	µA

5.5 Electrical Characteristics (continued)

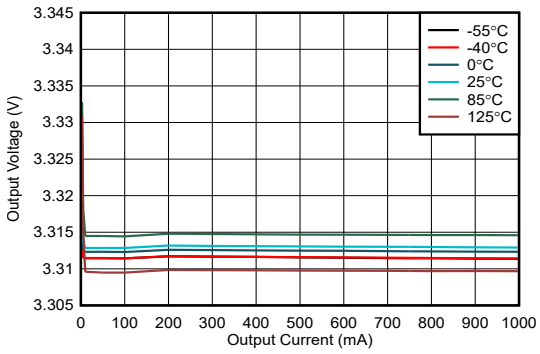
Over operating junction temperature range (T_J = –40°C to +150°C), V_{IN} = 1.9V or V_{IN} = $V_{OUT(NOM)}$ + 0.5V (whichever is greater), $V_{OUT(NOM)}$ = 0.8V, I_{OUT} = 1mA, V_{EN} = 1.0V, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, and C_{FF} = 10nF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO+}	Undervoltage lockout threshold	V_{IN} rising	0.99	1.39	1.81	V
V_{UVLO-}		V_{IN} falling	0.96	1.34	1.75	
$V_{UVLO(HYST)}$	Undervoltage lockout hysteresis			45		mV
T_{sd+}	Thermal shutdown temperature increasing	Shutdown, temperature increasing		165		°C
T_{sd-}	Thermal shutdown temperature decreasing	Reset, temperature decreasing		140		°C
t_{ST}	Start-up time	$V_{OUT(nom)}$ = 3.3V, C_{FF} = 10nF, time from EN > V_{IL} to V_{OUT} = 90% $V_{OUT(nom)}$		800		µs

(1) External resistor tolerances are not included. V_{OUT} = 0.8V, 4.5V ≤ V_I ≤ 6.0V and 750mA ≤ I_{OUT} ≤ 1A are not tested because the power dissipation is greater than the maximum rating of the package.

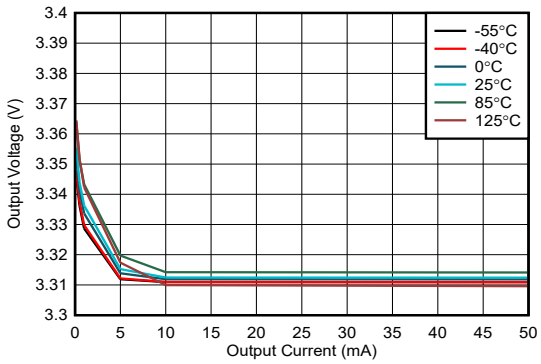
5.6 Typical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.9V (whichever is greater), $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1V, I_{OUT} = 1mA, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, C_{FF} = 10nF, and T_A = 25°C (unless otherwise noted)



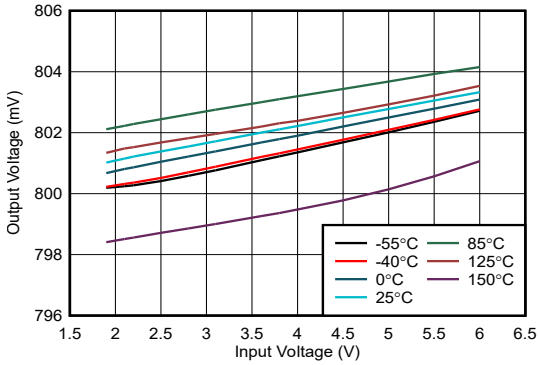
$V_{OUT(NOM)}$ = 3.3V

Figure 5-1. Load Regulation



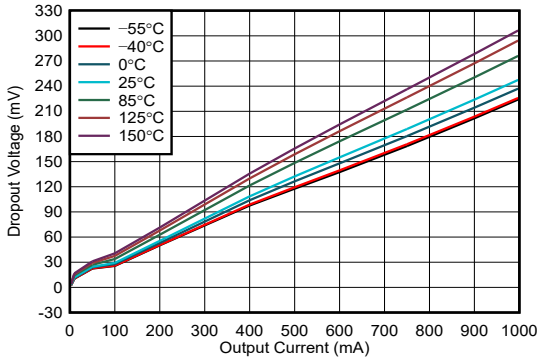
$V_{OUT(NOM)}$ = 3.3V

Figure 5-2. Load Regulation Under Light Loads



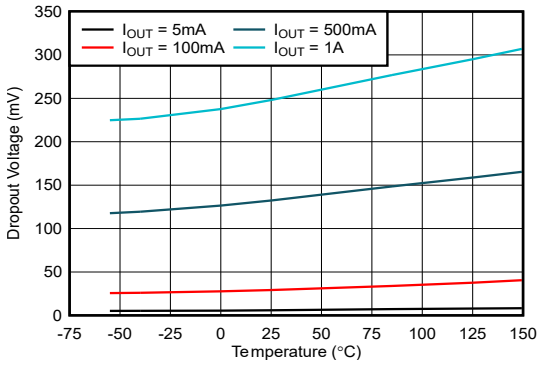
I_{OUT} = 5mA

Figure 5-3. Line Regulation



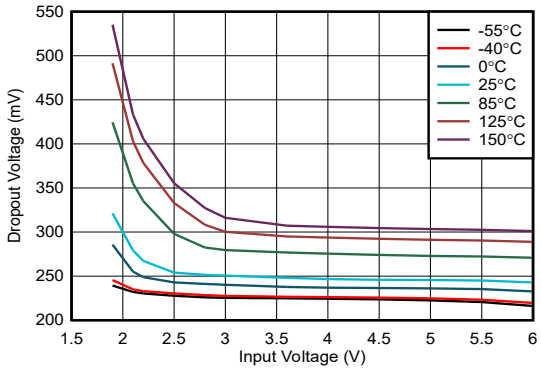
V_{IN} = 3.6V, I_{OUT} = 1A, V_{FB} = 0V

Figure 5-4. Dropout Voltage vs Load Current



V_{IN} = 3.6, V_{FB} = 0V

Figure 5-5. Dropout Voltage vs Temperature

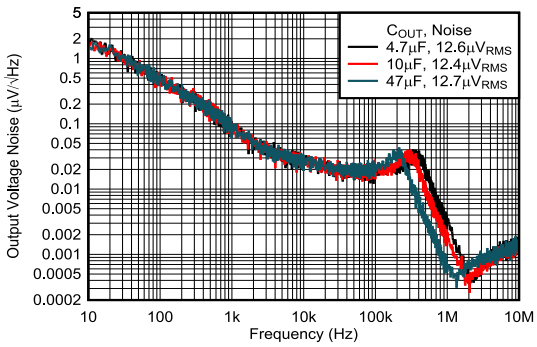


I_{OUT} = 1A, V_{FB} = 0V

Figure 5-6. Dropout Voltage vs Input Voltage

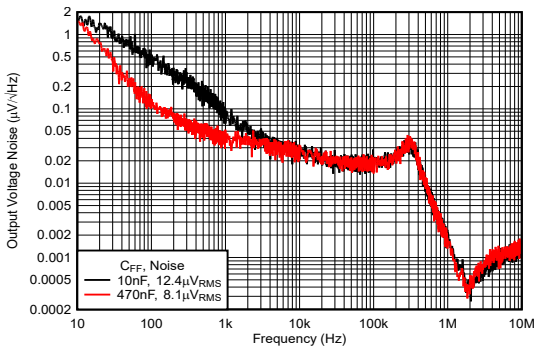
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.9V (whichever is greater), $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1V, I_{OUT} = 1mA, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, C_{FF} = 10nF, and T_A = 25°C (unless otherwise noted)



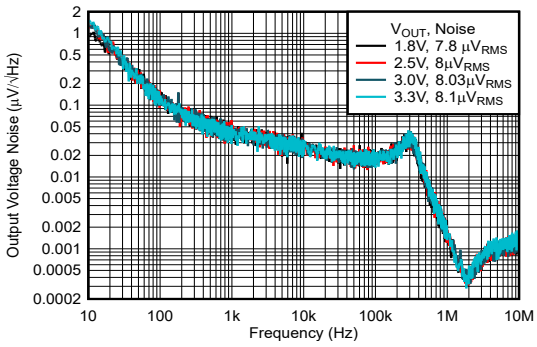
C_{IN} = 10µF, I_{OUT} = 100mA, $V_{OUT(NOM)}$ = 3.3V

Figure 5-7. Output Noise Spectral Density vs Frequency



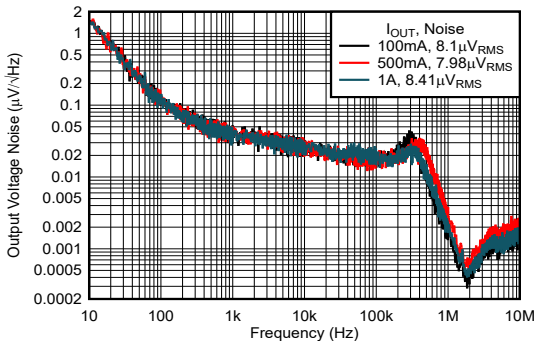
C_{IN} = C_{OUT} = 10µF, I_{OUT} = 100mA, $V_{OUT(NOM)}$ = 3.3V

Figure 5-8. Output Noise Spectral Density vs Frequency



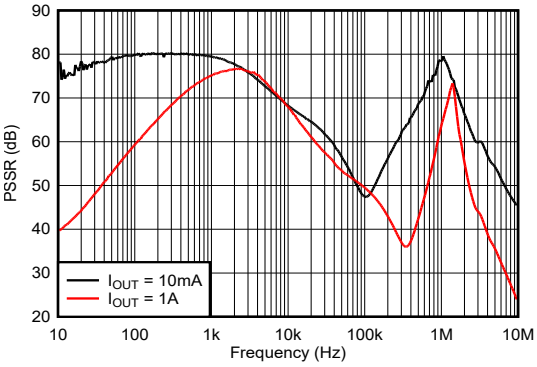
C_{IN} = C_{OUT} = 10µF, C_{FF} = 470nF, I_{OUT} = 100mA

Figure 5-9. Output Noise Spectral Density vs Frequency



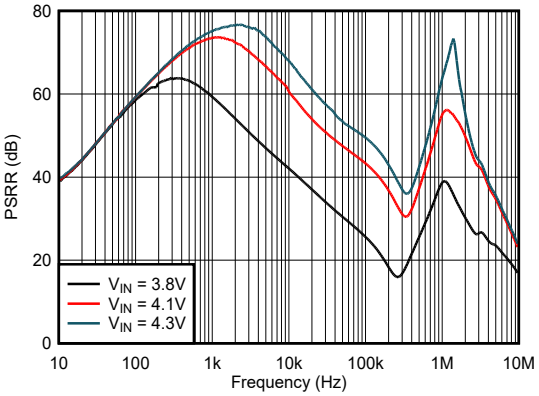
C_{IN} = C_{OUT} = 10µF, C_{FF} = 470nF, $V_{OUT(NOM)}$ = 3.3V

Figure 5-10. Output Noise Spectral Density vs Frequency



C_{OUT} = 10µF, C_{FF} = 470nF, V_{IN} = 4.3V, $V_{OUT(NOM)}$ = 3.3V

Figure 5-11. PSRR vs Frequency

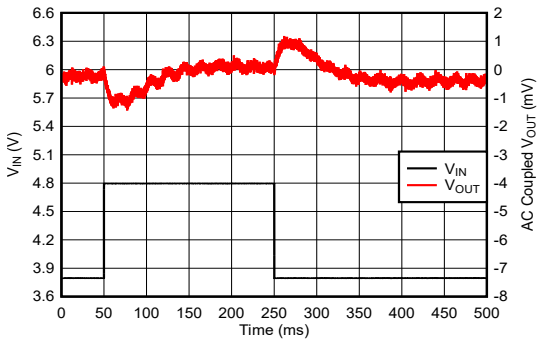


C_{OUT} = 10µF, C_{FF} = 470nF, I_{OUT} = 1A, $V_{OUT(NOM)}$ = 3.3V

Figure 5-12. PSRR vs Frequency

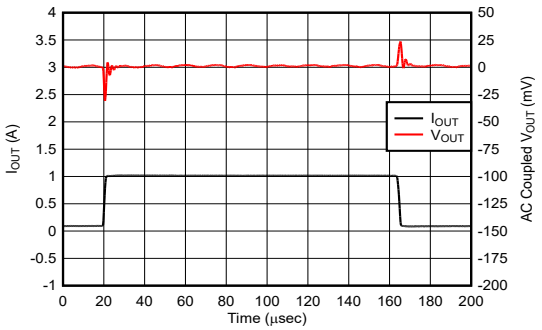
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.9V (whichever is greater), $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1V, I_{OUT} = 1mA, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, C_{FF} = 10nF, and T_A = 25°C (unless otherwise noted)



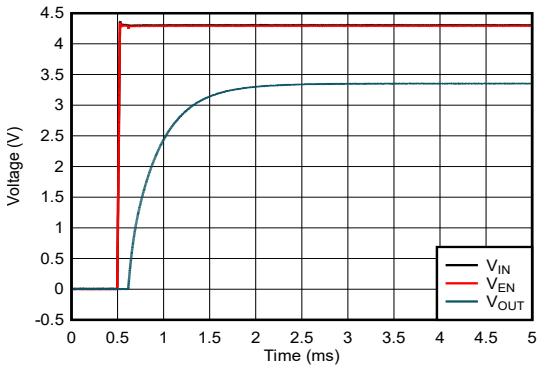
$V_{OUT(NOM)}$ = 3.3V, I_{OUT} = 500mA, C_{FF} = 470nF, T_R = T_F = 5µs

Figure 5-13. Line Transient Response



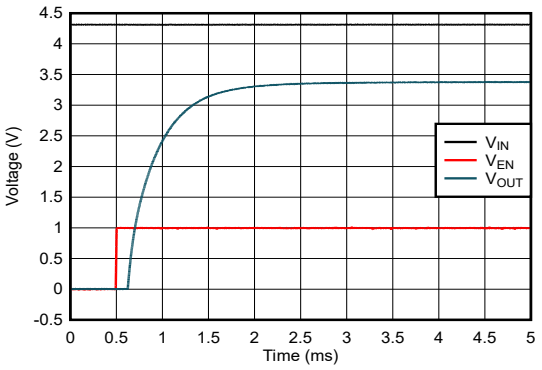
$V_{OUT(NOM)}$ = 3.3V, I_{OUT} = 100mA → 1A → 100mA, C_{FF} = 470nF, T_R = T_F = 1µs

Figure 5-14. Load Transient Response



$V_{OUT(NOM)}$ = 3.3V

Figure 5-15. Startup With Enable Tied to VIN



$V_{OUT(NOM)}$ = 3.3V

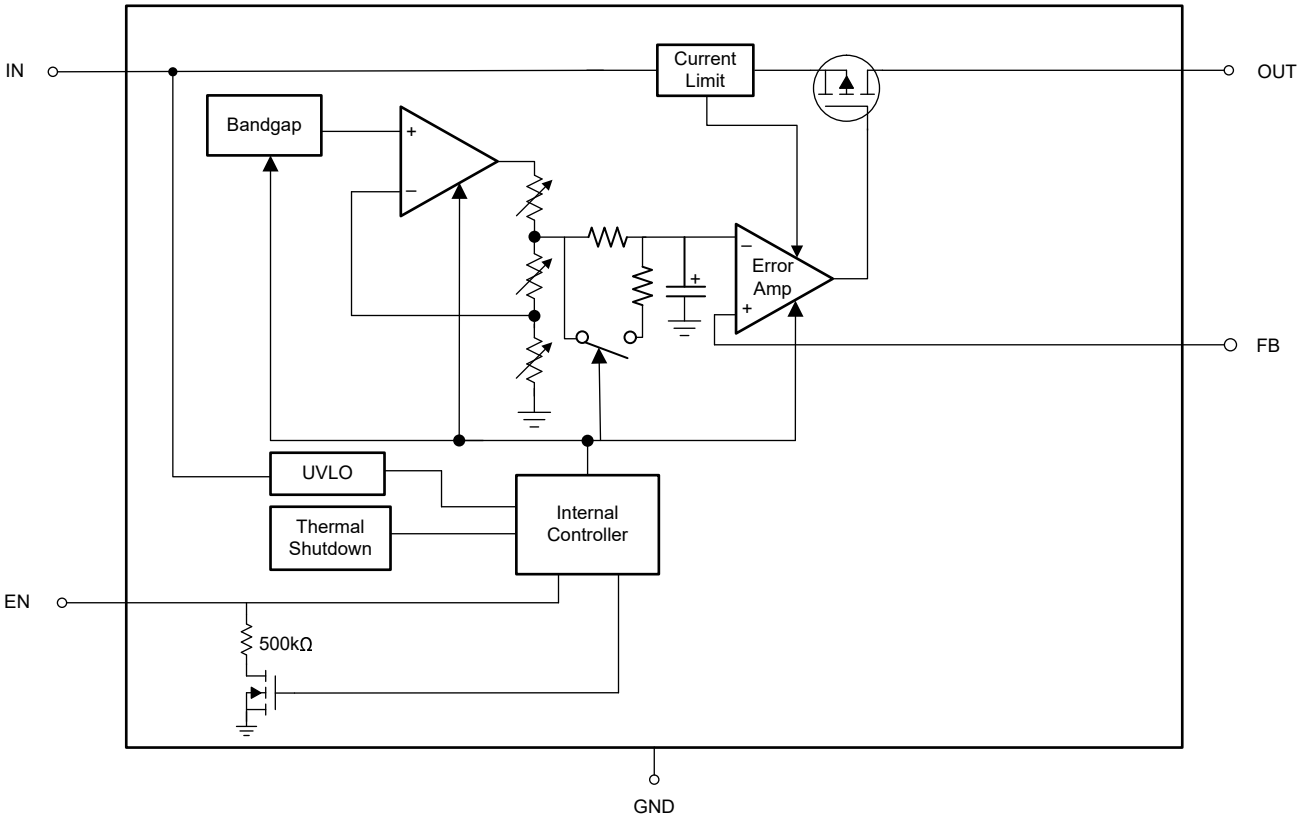
Figure 5-16. Startup With Enable

6 Detailed Description

6.1 Overview

The TPS7N41Q1 provides up to 1A of output current with high PSRR and low quiescent current. Low noise is achieved without the need for a noise-reduction capacitor. This family of regulators offers sub-bandgap output voltages, current-limit, and thermal protection, and is specified for operation over the –40°C to 150°C temperature range.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.2 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current termed the *short-circuit current limit (I_{SC})*. I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-1 shows a diagram of the foldback current limit.

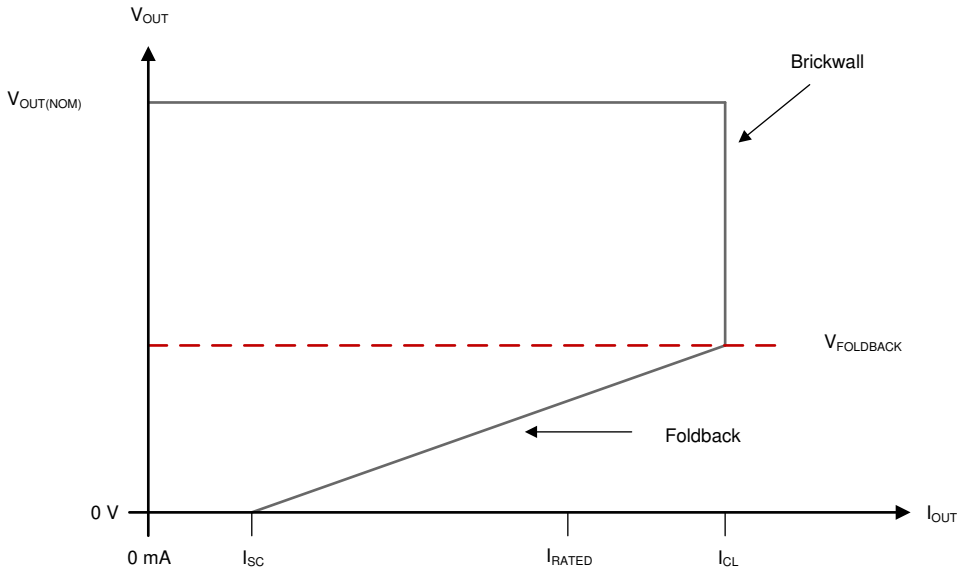


Figure 6-1. Foldback Current Limit

6.3.3 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to T_{SD+} (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to T_{SD-} (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational

specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{IL(EN)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven fully on. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the regulator exits dropout, the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$. During this time, the output voltage potentially overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage. During dropout exit, the device pulls the pass transistor back from being driven fully on.

6.4.3 Disabled

Shut down the LDO by forcing the EN input voltage to less than the maximum EN low-level input voltage. When disabled, the pass transistor turns off and the internal circuits shut down.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. For typical operation of the TPS7N41-Q1, connect a 4.7µF capacitor to the input. Use a higher value capacitor if large, fast rise-time, load, or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability. Make sure that the minimum derated output capacitance is equal to or greater than 2.2µF (4.7µF nominal). When the output voltage is ramping up, the inrush current depends on the size of the output capacitance. During start-up, the output current is potentially as high as the current limit value for larger output capacitors.

7.1.3 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3V$:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. Figure 7-1 shows one approach of protecting the device.

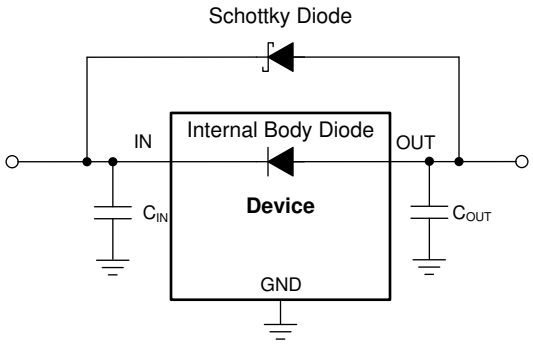


Figure 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.4 Dropout Voltage

The TPS7N41Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

7.2 Typical Application

7.2.1 Application

Figure 7-2 shows a typical application circuit for the TPS7N41-Q1.

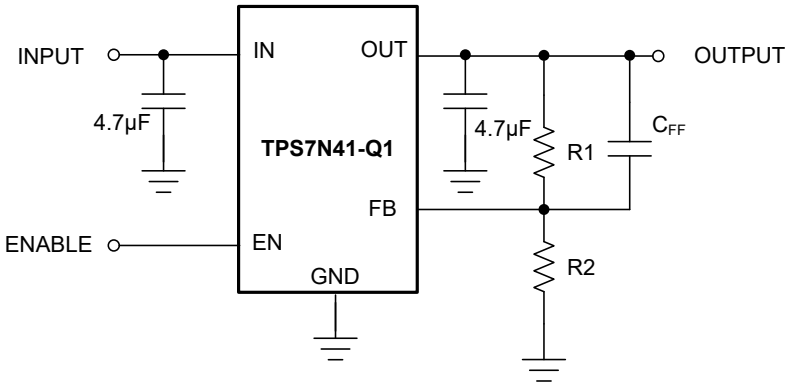


Figure 7-2. TPS7N41-Q1 Typical Application

The output voltage is determined by the feedback node voltage and the values of resistors R1 and R2. Use this equation to calculate the output voltage based on the values of R1 and R2.

$$V_O = \frac{(R1 + R2)}{R2} \times 0.8 \quad (2)$$

The values of the feedback resistors affect the output voltage accuracy, so use resistors with appropriate tolerance values. The input current of the FB pin is supplied by the feedback network, so verify that the resistor values are low enough that the input current of the FB pin does not introduce significant output voltage error. It is recommended to use a value of 10kΩ for R2 for this reason.

7.2.2 Design Requirements

Table 7-1 summarizes the design requirements for Figure 7-2.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range	4.0V ±5%
Output voltage	3.3V
Output current	600mA
Maximum ambient temperature	100°C

7.2.3 Detailed Design Procedure

For this design example, a nominal 4.0V input supply is assumed. Use a minimum 4.7µF input capacitor to minimize the effect of resistance and inductance between the 4.0V source and LDO input. Use a nominal 4.7µF (minimum 2.2µF) output capacitance for stability and good load transient response. Use a value of 10kΩ for R2, and 31.2kΩ for R1 to achieve the 3.3V nominal output voltage. The dropout voltage (V_{DO}) is less than 300mV maximum at a 3.3V output voltage and 600mA output current, so there are no dropout issues.

7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.9V to 6.0V. Make sure the input is well regulated and free of spurious noise, so the regulator provides a well regulated output with optimum dynamic performance. Set the input supply to at least $V_{OUT(nom)}$ + 0.5V or 1.9V, whichever is greater.

Use a 4.7µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.

7.4.2 Layout Examples

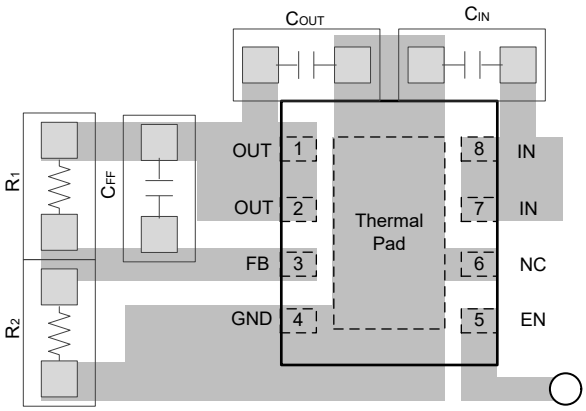


Figure 7-3. Typical Layout

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT(1)	DESCRIPTION
TPS7N41**01Q(W)yyyzQ1**	**01** indicates that the output voltage of the LDO is adjustable. **Q** indicates that this device is a Grade-1 device in accordance with the AEC-Q100 standard. **W** (when present) indicates the package has wettable flanks. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces). **Q1** indicates that this is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Know Your Limits* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7N4101QWDRBRQ1	Active	Production	SON (DRB) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7N4101

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

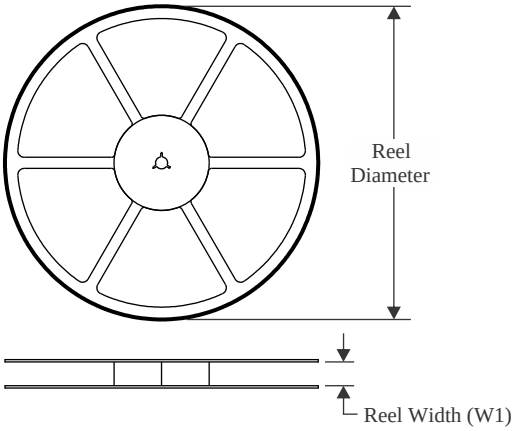
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

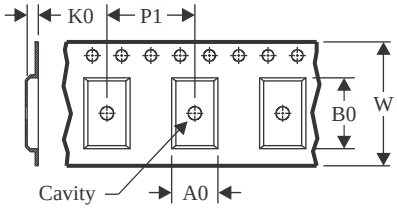
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

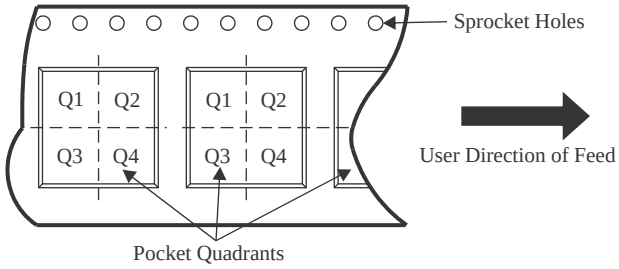


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

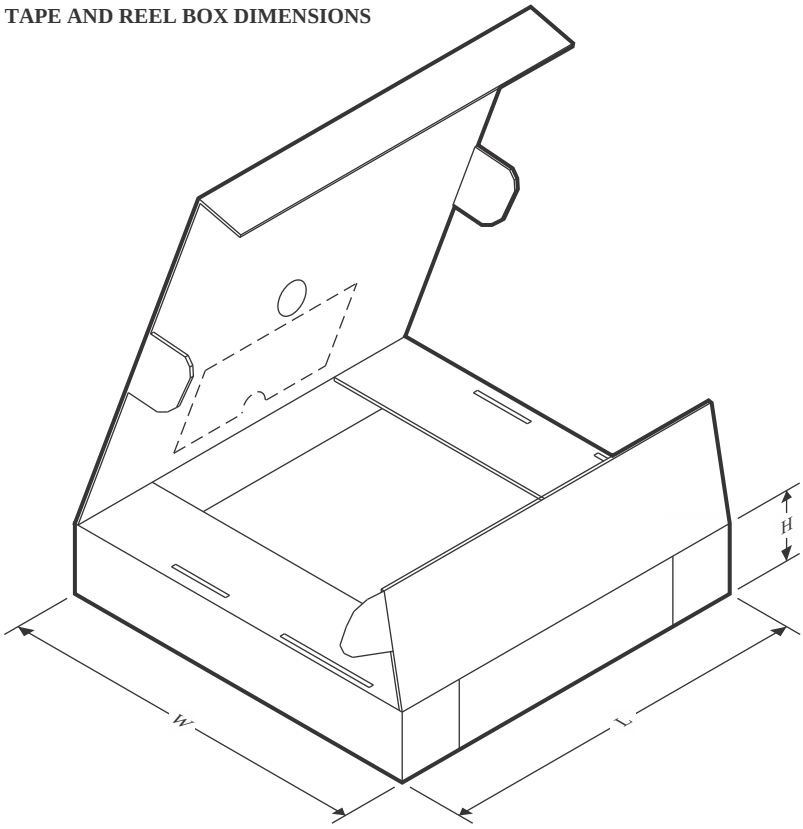
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7N4101QWDRBRQ1	SON	DRB	8	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7N4101QWDRBRQ1	SON	DRB	8	5000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

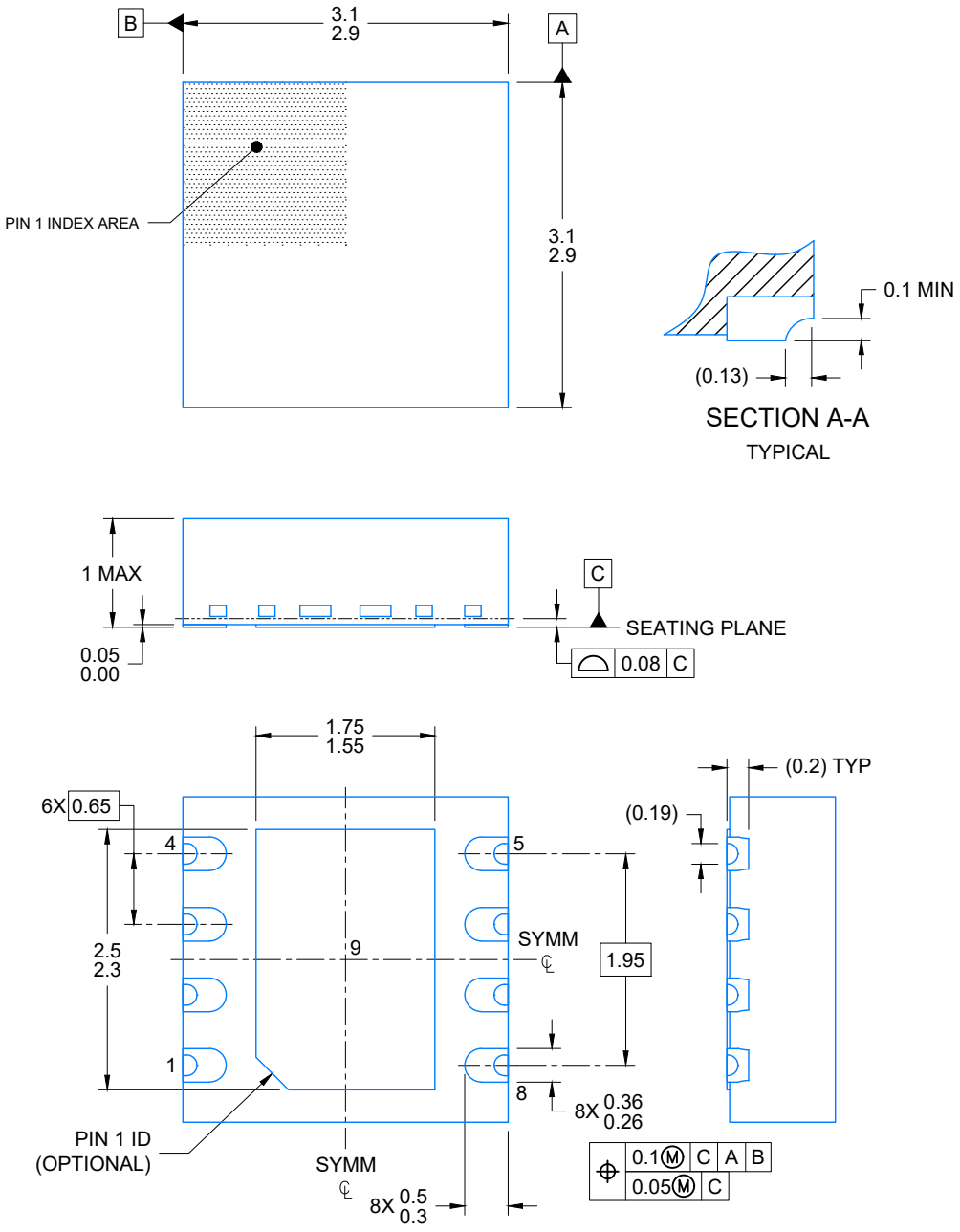
4203482/L

PACKAGE OUTLINE

DRB0008J

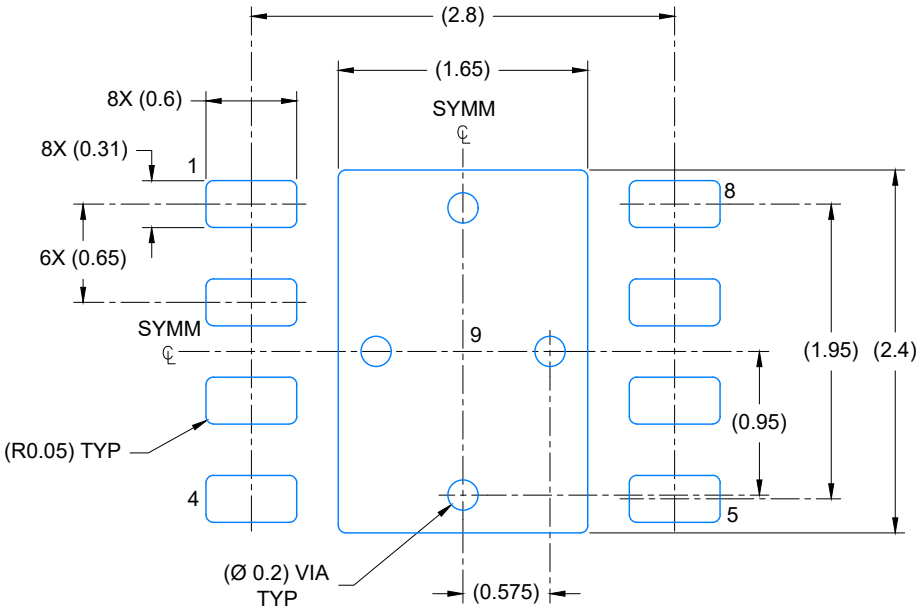
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

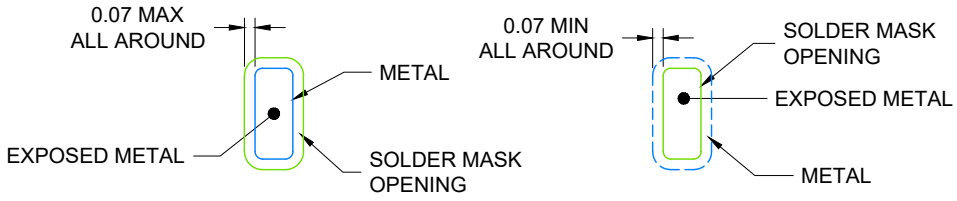


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

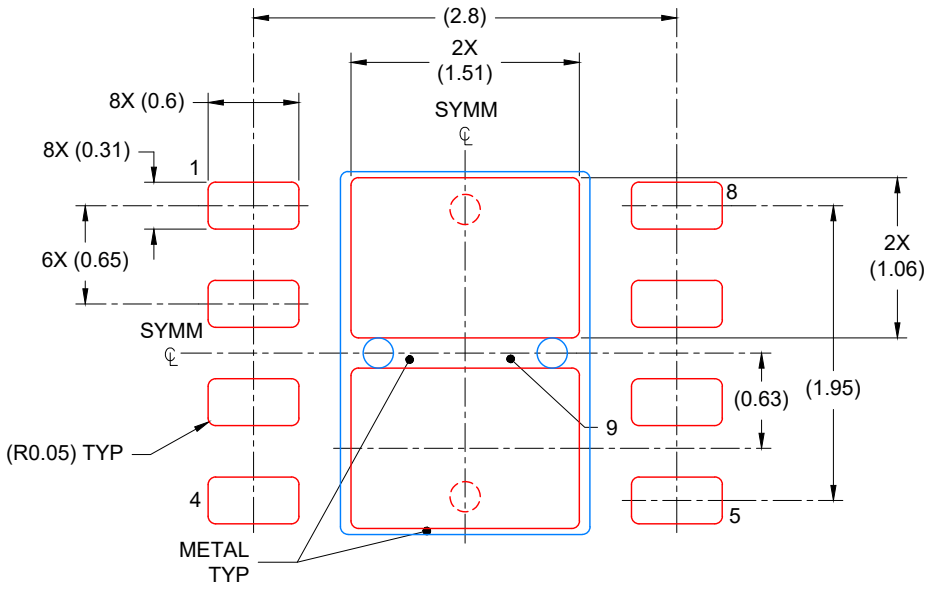
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025