TPS7H6101-SEP 200V, 10A GaN Half Bridge Power Stage

1 Features

- Radiation performance:
  - Radiation lot acceptance tested (RLAT) to total ionizing dose (TID) of 50krad(Si)
  - Single-event transient (SET), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 43MeV-cm^2/mg
  - Single-event transient (SET) and single-event fault interrupt (SEFI) characterized up to (LET) = 43MeV-cm^2/mg
- 200V e-mode GaN FET half bridge
  - 15mΩ$R_{DS(ON)}$ (typ)
  - 100kHz to 2MHz operation
- LGA package:
  - Thermally optimized 12mm × 9mm LGA package with thermal pads
  - Integrated gate drive resistors
  - Low common source inductance packaging
  - Electrically isolated high-side and low-side
- Flexible control for various half-bridge and two switch power supply topologies
  - Low propagation delay
  - Two operational modes
    - Single PWM input with adjustable dead time
    - Two independent inputs
  - Programmable dead time control
  - Selectable input interlock protection in independent input mode
  - 5V gate drive supply for robust FET operation

2 Applications

- Satellite electrical power system (EPS)
- Motor drives

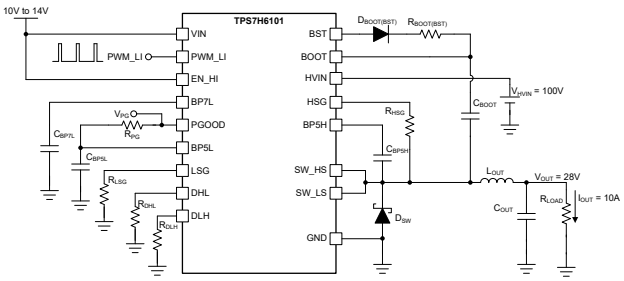
3 Description

The TPS7H6101 is a radiation-tolerant 200V e-mode GaN power-FET half bridge with integrated gate driver; integration of the e-mode GaN FETs and gate driver simplifies design, reduces component count, and reduces board space. Support for half-bridge and two independent switch topologies, configurable dead time, and configurable shoot through interlock protection facilitates support for a wide variety of applications and implementations.

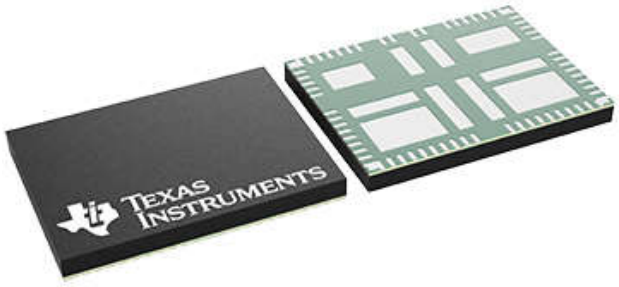
Device Information

PART NUMBER(1)	GRADE	BODY SIZE(2)
TPS7H6101MNPRNSEP	SEP	NPR (LGA, 64) 12.00mm × 9.00mm Mass = 264mg(3)

(1) For additional information view the *Device Options Table*.
(2) The body size (length × width) is a nominal value and does not include pins.
(3) Mass is a nominal value.



Typical Application Circuit



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4 Device Options Table

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H6101-SEP	TID of 50krad(Si) RLAT, DSEE free to 48MeV-cm^2/mg	Space Enhanced Plastic	64-Pin NPR	TPS7H6101MNPRNSEP

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view SLYB235.

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5 Pin Configuration and Functions

NPR Package
64-Pin LGA
(Top View)

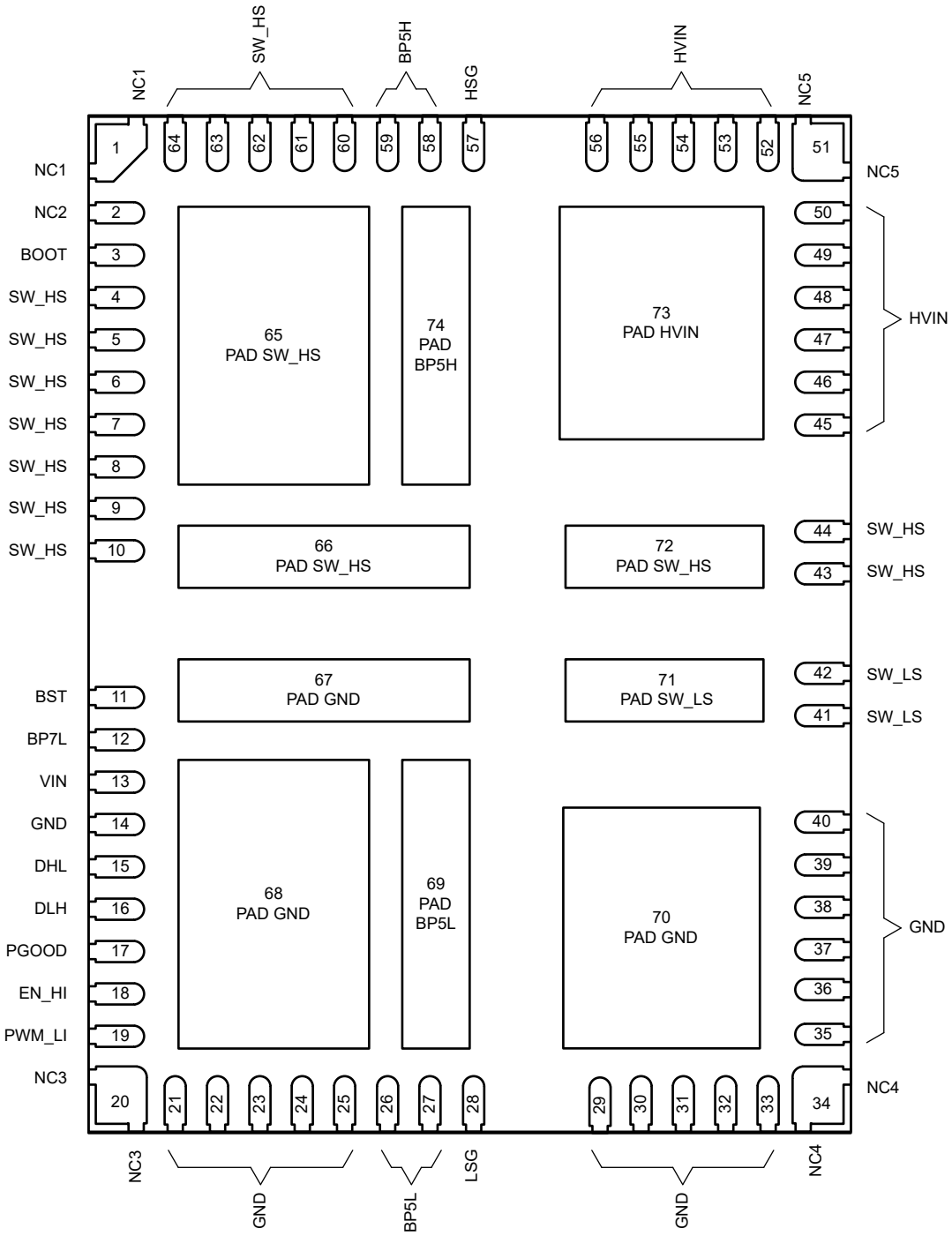

Table 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
BOOT	3	I	Input voltage supply of the high-side linear regulator. The external bootstrap capacitor is placed between BOOT and SW_HS. The cathode of the external bootstrap diode is connected to this pin. A Zener diode clamp between BOOT and SW_HS provides supplemental protection from exceeding the maximum electrical rating.
BP5H	58–59	P	High-side 5V linear regulator output. Connect a 1µF ceramic capacitor as close as possible to the package from BP5H and SW, with a wide PCB trace connecting BP5H and PAD PB5H. When mounting on the opposite side of the PCB, position capacitor under PAD BP5H and use multiple in pad vias to minimize parasitic inductance.
BP5L	26–27	P	Low-side 5V linear regulator output. Connect a 1µF ceramic capacitor as close as possible to the package from BP5L and GND, with a wide PCB trace connecting BP5L and PAD PB5L. When mounting on the opposite side of the PCB, position capacitor under PAD BP5L and use multiple in pad vias to minimize parasitic inductance.
BP7L	12	P	Low-side 7V linear regulator output. A minimum of 1uF capacitance is required from BP7L to GND.
BST	11	O	For bootstrap charging that utilizes the internal bootstrap switch, this pin serves as the bootstrap diode anode connection point. The external high-side bootstrap capacitor can be charged through this pin using the input voltage applied to VIN, internal bootstrap switch, and external bootstrap diode.
DLH	16	I	Low-side to high-side dead time set. In PWM mode, a resistor from DLH to GND sets the dead time between the low-side turn-off and high-side turn-on. For half-bridge applications in PWM mode, connect a 35.7kΩ R_{DLH} to GND. Alternate R_{DLH} values can be configured, but additional testing and analysis is required to verify proper switching behavior. In independent input mode (IIM), DLH is used to configure the input interlock protection of the driver. A resistor valued between 100kΩ and 220kΩ is connected from DLH to GND for IIM with interlock enabled. DLH is connected to BP5L in IIM with interlock disabled.
DHL	15	I	High-side to low-side dead time set. In PWM mode, a resistor from DHL to AGND sets the dead time between the high-side turn-off and low-side turn-on. For half-bridge applications in PWM mode, connect a 57.6kΩ R_{DHL} to GND. Alternate R_{DHL} values can be configured, but additional testing and analysis is required to verify proper switching behavior. In independent input mode (IIM), DHL is used to configure the input interlock protection of the driver. DHL is connected to BP5L in IIM with interlock enabled. A resistor valued between 100kΩ and 220kΩ is connected from DHL to GND for IIM with interlock disabled.
EN_HI	18	I	Enable input or high-side driver control input. In PWM mode this is used as an enable pin. In independent input mode (IIM) this serves as the control input for the high-side driver.
GND	14, 21–25, 29–33, 35–40	—	Low-side driver signal return. Internally connected to PAD GND 67, 68 & 70. Pins 14, 21-25, and 29 are not directly in the high current path; pins 29-33, and 35-40 are in the high current path.
HSG	57	NC	High-side gate pin. This pin provides access to the gate of the high-side GaN FET for debugging and testing purposes. When configured in a half-bridge topology, connect a 10kΩ resistor from HSG to SW.
HVIN	45–50, 52–56	P	Internally connected to PAD HVIN (67-68) and the high-side GaN FETs drain terminal; the pins are directly in the high current path.
LSG	28	NC	Low-side gate pin. This pin provides access to the gate of the low-side GaN FET for debugging and testing purposes. When configured in a half-bridge topology, connect a 10kΩ resistor from LSG to GND.
NC1	1	NC	Used to anchor the package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are solder mask defined pads; this pin is not internally connected and is recommended to be connected to the high side reference voltage (SW_LS).
NC2	2	NC	No connect. This pin is not connected internally. Connection of pin NC2 to SW_HS is recommended to prevent charge buildup; however, this pin can also be left open.
NC3	20	NC	Used to anchor the package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are solder mask defined pads; this pin is not internally connected and is recommended to be connected ground (GND) to prevent charge build up; however this pin can also be left open.

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Table 5-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
NC4	34	NC	Used to anchor the the package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are solder mask defined pads; this pin is not internally connected and is recommended to be connected ground (GND) to prevent charge build up; however this pin can also be left open.
NC5	51	NC	Used to anchor the the package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are solder mask defined pads; this pin is not internally connected and is recommended to be connected to high voltage input (HVIN) to prevent charge build up; however this pin can also be left open.
PAD BP5H	74	P	The BP5H pad provides a low electrical resistance path for the high side regulator, BP5H; PAD BP5H is internally connected to the BP5H pins (58-59).
PAD BP5L	69	P	The BP5L pad provides a low electrical resistance path for the high side regulator, BP5L; PAD BP5L is internally connected to the BP5L pins 26-27.
PAD_GND	67, 68, 70	—	Power GND pad utilized as the high current path, connected to the high-side GaN FET drain terminal for low-side driver signal return. PAD_GND pin 70 is internally connected to the low side FET source terminal and is to be used as the primary heat extraction path for the low side switch.
PAD HVIN	73	—	Power HVIN pad utilized as the high current path, connected to the high-side GaN FET source terminal for thermal heat extraction. PAD HVIN is internally connected to HVIN pins 45-50, 52-56.
PAD SW_HS	65, 66, 72	—	Power SW_HS pad utilized as the high current path, connected to the high-side GaN FET drain terminal. Also internally connected to pins SW_HS 9-10, 44-45, and 60-64. The TPS7H6101-SP has two electrically isolated GaN FETs and drivers; to form a half-bridge configuration, connect to SW_LS pad and pins.
PAD SW_LS	71	—	Power SW_LS pad utilized as the high current path, connected to the low-side GaN FET source terminal. Internally connected to pins SW_LS(41-42). The TPS7H6101-SP has two electrically isolated GaN FETs and drivers; to form a half-bridge, connect to SW_HS pad and pins.
PGOOD	17	O	Power good pin. Asserts low when any of the low-side internal linear regulators or VIN goes into undervoltage lockout. Requires a 10kΩ pull-up resistor to BP5L.
PWM_LI	19	I	PWM input or low-side driver control input. In PWM mode this is used as the PWM input to the gate driver. In independent input mode (IIM) this serves as the control input for the low-side driver.
SW_HS	4–10, 44–45, 60–64	P	High side driver signal return. SW_HS is internally connected to PAD SW_HS (65, 66 & 72). Pins 4-10 and pins 60-64 are not directly part of the high current path; pins 44-45 are in the high current path.
SW_LS	41–42	P	Internally connected to PAD SW_LS and the low-side GaN FETs drain terminal; connect to SW_LS on the PCB; these pins are part of the high current path.
VIN	13	I	Gate driver input voltage supply. Input voltage range is from 10V to 14V. This pin serves as the input to the low-side linear regulators and the internal bootstrap switch. For bootstrap charging directly from the input voltage, VIN also serves as the bootstrap diode anode connection point.

(1) I = Input, O = Output, G = Ground, P = Power, NC = No Connect, — = Other

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Breakdown voltage	High side drain-source breakdown voltage (HVIN to SW_HS) voltage, $BV_{DS(HS)}$	200		V
	Low side drain-source breakdown voltage (SW_LS to GND) voltage, $BV_{DS(LS)}$	200		V
Input voltage	HVIN	–0.3	200	V
	VIN, EN_HI, PWM_LI, DLH, DHL	–0.3	16	
	BOOT	0	216	
Output voltage	PGOOD	–0.3	5.5	V
	BP7L	–0.3	8	
	BP5L	–0.3	7	
	SW_HS	–10	200	
	SW_LS	–10	200	
	BST	–0.3	16	
Input voltage (Referenced to SW_HS)	BOOT	–0.3	V_{SW_HS} + 16	V
	HVIN	–10	200	
Output voltage (Referenced to SW_HS)	BP5H	–0.3	7	V
Sink current	Continuous drain-source current, $I_{OUT(CONT)}$		18	A
	Single-pulse drain current $t_p \le 80$ µs, $T_A = 25$°C, $I_{OUT(PULSE)}$		72	A
	BST current (3-µs transient pulse, non-repetitive), I_{BST}		4	A
Operating junction temperature		–55	150	°C
Storage temperature, T_{stg}		–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Input voltage	HVIN			150	V
	VIN	10		14	
	EN_HI,PWM_LI	0		14	
	BOOT to SW_HS	V_{SW_HS} + 8		V_{SW_HS} + 14	
Output voltage	SW_HS	–10		150	V
	SW_LS	–10		150	
	Low side drain-source voltage (SW_LS to GND)			150	
	High side drain-source voltage (HVIN to SW_HS)			150	
Output current	Continuous output current, I_{OUT}			10	A
Slew rate	Vin slew rate, SR_{VIN}			0.03	V/ns
	SW slew rate, SR_{SW}			100	
	PWM_LI slew rate, SR_{PWM_LI}	2			V/µs
	EN_HI slew rate, SR_{EN_HI}	2			
Operating junction temperature	T_J	–55		125	°C

6.4 Thermal Information

THERMAL METRIC		TPS7H6101-SP LGA 74 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	°C/W
$R_{\theta JC(HS)}$	Junction-to-case High Side FET (PAD HVIN)	2.4	°C/W
$R_{\theta JC(LS)}$	Junction-to-case Low Side FET (PAD GND)	4.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5	°C/W
$\Psi_{\theta JT}$	Junction-to-top characterization parameter	5.1	°C/W
$\Psi_{\theta JB}$	Junction-to-board characterization parameter	4.9	°C/W

6.5 Electrical Characteristics

Over ambient temperature operating range T_A = –55°C to 125°C, VIN = 10V to 14V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GAN POWER FETs							
$R_{DS(on)(ls)}$	Drain-source on resistance - low side	V_{PWM_LI} = 5V, $I_{D(LS)}$ = 2A	T_A = -55℃		12		mΩ
			T_A = 25℃		16		
			T_A = 125℃		24		
$V_{SD(ls)}$	Low side source-drain (GND to SW_LS) third quadrant voltage	$I_{D(LS)}$ = -0.5A			1.8		V
		$I_{D(LS)}$ = -1A			2		
$I_{DSS(ls)}$	Low side drain (SW_LS to GND) leakage current	$V_{DS(LS)}$ = 150V, V_{PWM_LI} = 0V	T_A = 25℃		15	150	µA
			T_A = 125℃			300	
$R_{DS(on)(hs)}$	Drain-source on resistance - high side	V_{EN_HI} = 5V, $I_{D(HS)}$ = 2A	T_A = -55℃		12		mΩ
			T_A = 25℃		16		
			T_A = 125℃		24		
$V_{SD(hs)}$	High side source-drain (SW_HS to HVIN) third quadrant voltage	$I_{D(HS)}$ = 0.5A			1.8		V
		$I_{D(HS)}$ = 1A			2		
$I_{DSS(hs)}$	High side drain (HVIN to SW_HS) leakage current	$V_{DS(HS)}$ = 150V, V_{EN_HI} = 0V	T_A = 25℃		15	150	µA
			T_A = 125℃			300	
SUPPLY CURRENTS							
I_{Q_LS}	Low side shutdown current (measured on VIN)	EN = 0V, VIN = 12V, BOOT = 10V	MODE = PWM		5	6.8	mA
			MODE = IIM		5	8	
I_{Q_HS}	High side shut down current (measured on BOOT)	EN = 0V, VIN = 12V, BOOT = 10V	MODE = PWM		5	6.3	mA
		EN = 0V, VIN = 12V, BOOT = 10V	MODE = IIM		5	6.3	mA
I_{Q_BG}	BOOT to GND shutdown leakage current	V_{SW_HS} = V_{SW_LS} = 100V, BOOT = 110V				50	µA
I_{OP_BG}	BOOT to GND operating leakage current	V_{SW_HS} = V_{SW_LS} = 100V, BOOT = 110V				50	µA
I_{OP_LS}	Low side operating current	MODE = PWM	f = 500kHz		9	12	mA
			f = 1Mhz		13	16	
			f = 2Mhz		21	25	
		MODE = IIM	f = 500kHz		9	12	
			f = 1Mhz		13	16	
			f = 2Mhz		21	25	
I_{OP_HS}	High side operating current	MODE = PWM	f =500kHz		9	12	mA
			f = 1Mhz		13	16	
			f = 2Mhz		21	25	
		MODE = IIM	f = 500kHz		9	12	
			f = 1Mhz		13	16	
			f = 2Mhz		21	25	
INTERNAL REGULATORS							
V_{BP5L}	Low side 5V regulator output voltage	C_{BP5L} = 1µF		4.75	5.0	5.175	V
V_{BP5H}	High side 5V regulator output voltage	C_{BP5H} = 1µF		4.75	5.0	5.175	V
V_{BP7L}	7V regulator output voltage	C_{BP7L} = 1µF		6.65	7	7.35	V

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6.5 Electrical Characteristics (continued)

Over ambient temperature operating range T_A = –55°C to 125°C, VIN = 10V to 14V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
UNDERVOLTAGE PROTECTION							
$BP5H_R$	BP5H UVLO rising threshold	C_{BP5H} = 1µF			4.1		V
$BP5H_F$	BP5H UVLO falling threshold				3.9		V
$BP5H_H$	BP5H UVLO hysteresis				0.25		V
$BP5L_R$	BP5L UVLO rising threshold	C_{BP5L} = 1µF			4.1		V
$BP5L_F$	BP5L UVLO falling threshold				3.9		V
$BP5L_H$	BP5L UVLO hysteresis				0.25		V
$BP7L_R$	BP7L UVLO rising threshold	C_{BP7L} = 1µF			6.4		V
$BP7L_F$	BP7L UVLO falling threshold				6.1		V
$BP7L_H$	BP7L UVLO hysteresis				0.3		V
VIN_R	VIN UVLO rising threshold			8.0	8.6	9.0	V
VIN_F	VIN UVLO falling threshold			7.5	8.1	8.5	V
VIN_H	VIN UVLO hysteresis				0.5		V
$BOOT_R$	BOOT UVLO rising threshold			6.6	7.1	7.4	V
$BOOT_F$	BOOT UVLO falling threshold			6.2	6.65	7	V
$BOOT_H$	BOOT UVLO hysteresis				0.45		V
INPUT PINS (EN_HI, PWM_LI)							
V_{IR}	Input rising edge threshold			1.9		2.7	V
V_{IF}	Input falling edge threshold			1.20		1.85	V
V_{IHYS}	Input hysteresis				0.7		V
R_{PD}	Input pull-down resistance	V = 2.15V applied at input (EN_HI or PWM_LI)		100		400	kΩ
PROGRAMMBLE DEAD TIME							
t_{DLH}	Dead time low side falling to high side(1)	MODE = PWM From V_{LSG} = 0.48V to V_{HSG} = 0.48V 100kHz < f ≤ 2MHz	RLH = 35.7kΩ	20	30	37	ns
t_{DHL}	Dead time high side falling to low side(1)	MODE = PWM From V_{HSG} = 0.48V to V_{LSG} = 0.48V 100kHz< f ≤ 2MHz	RHL = 57.6kΩ	36	44	53	
BOOTSTRAP DIODE SWITCH							
R_{BST_SW}	Bootstrap diode switch resistance	I_{BST_SW} = 100mA			0.3		Ω
	Bootstrap diode switch parallel resistance	I_{BST_RP} = 1mA		0.8	1	1.2	kΩ
POWER GOOD							
V_{PG_OL}	Logic-low output	I_{FLT} = 1mA				0.4	V
R_{PG}	PGOOD internal resistance	BP5L = 5V, BP7L = 7V, VIN = 12V		0.6	1	1.8	MΩ
$V_{BP7I\_MIN\_PG}$	Minimum BP7L voltage for valid PGOOD				3	3.6	V

(1) Refer to Deadtime Measurement diagram.

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6.6 Switching Characteristics

Over ambient temperature operating range T_A = -55°C to 125°C, VIN = 10V to 14V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).

PARAMETER		Test Conditions		MIN	TYP	MAX	UNIT
GATE DRIVE TIMING							
$t_{p(off)(ls)}$	Low side turn-off propagation delay(1)	From V_{PWM_LI} = V_{IR} to V_{LSG} = 2.5V, I_D = 400mA	Mode = PWM		41	51	ns
		From V_{PWM_LI} = V_{IF} to V_{LSG} = 2.5V, I_D = 400mA	Mode = IIM		33	42	
$t_{p(on)(ls)}$	Low side turn-on gate drive propagation delay(1)	From V_{PWM_LI} = V_{IR} to V_{LSG} = 2.5V, I_D = 400mA	Mode = IIM		33	42	ns
$t_{p(off)(hs)}$	High side turn-off propagation delay(1)	From V_{PWM_LI} = V_{IF} to V_{HSG} = 2.5V, I_D = 400mA	Mode = PWM		35	50	ns
		From V_{EN_HI} = V_{IF} to V_{HSG} = 2.5V, I_D = 400mA	Mode = IIM		35	45	
$t_{p(on)(hs)}$	High side turn-on propagation delay(1)	From V_{EN_HI} = V_{IR} to V_{HSG} = 2.5V, I_D = 400mA	Mode = IIM		35	50	ns
$t_{d(on)(ls)}$	Low side turn-on delay(1)	From V_{PWM_LI} = V_{IF} to $V_{DS(ls)}$ = 4V, I_D = 400mA	Mode = PWM		45	60	ns
		From V_{PWM_LI} = V_{IR} to $V_{DS(ls)}$ = 4V, I_D = 400mA	Mode = IIM		45	60	
$t_{d(off)(ls)}$	Low side turn-off delay(1)	From V_{PWM_LI} = V_{IR} to $V_{DS(ls)}$ = 1V, I_D = 400mA	Mode = PWM		51	79	ns
		From V_{PWM_LI} = V_{IF} to $V_{DS(ls)}$ = 1V, I_D = 400mA	Mode = IIM		45	60	
$t_{d(on)(hs)}$	High side turn-on delay(1)	From V_{PWM_LI} = V_{IR} to $V_{DS(hs)}$ = 1V, I_D = 400mA	Mode = PWM		39	65	ns
		From V_{EN_HI} = V_{IR} to $V_{DS(hs)}$ = 1V, I_D = 400mA	Mode = IIM		39	65	
$t_{d(off)(hs)}$	High side turn-off delay(1)	From V_{PWM_LI} = V_{IF} to $V_{DS(hs)}$ = 4V, I_D = 400mA	Mode = PWM		45	65	ns
		From V_{EN_HI} = V_{IF} to $V_{DS(hs)}$ = 4V, I_D = 400mA	Mode = IIM		45	65	
t_{MON}	Delay matching low side on and high side off(2)	Mode = IIM			5	8	ns
t_{MOFF}	Delay matching low side off and high side on(2)	MODE = IIM			5	8	ns
$t_{PW(IIM)}$	Minimum input pulse width (turn-on)	MODE = IIM			5	8	ns
$t_{PW(IIM)(OFF)}$	Minimum input pulse width (turn-off)	MODE = IIM			12	16	ns
$t_{PW(PWM)}$	Minimum required input pulse width for targeted dead time	MODE = PWM, RHL = 57.6kΩ, RLH = 35.7kΩ, DT reduction ≤ 0.5ns			12		ns
$t_{PW(PWM)}$	Minimum required input pulse width for targeted dead time	MODE = PWM, RHL = 57.6kΩ, RLH = 35.7kΩ, DT reduction ≤ 3ns			30		ns
GAN FET							
$C_{OSS(ls)}$	Output capacitance - low side	f = 1MHz, V_{SW_LS} = 100V, V_{PWM_LI} = 0V			250		pF
$C_{OSS(hs)}$	Output capacitance - high side	f = 1MHz, V_{HVIN} = 100V, V_{EN_HI} = 0V			250		pF

(1) Refer to Timing Measurement section for measurement configuration and waveform diagrams.
(2) Specification limits for this parameter are respresented as an absolute value.

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6.7 Typical Characteristics

Over ambient temperature operating range T_A = 25°C , VIN = 10V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).

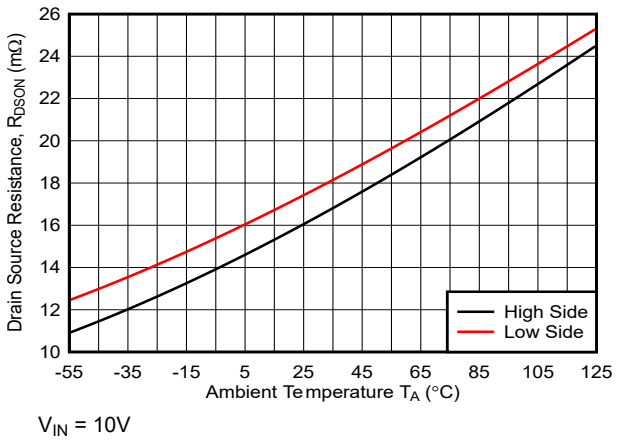

Figure 6-1. On-Resistance vs Junction Temperature (High-Side and Low-Side)

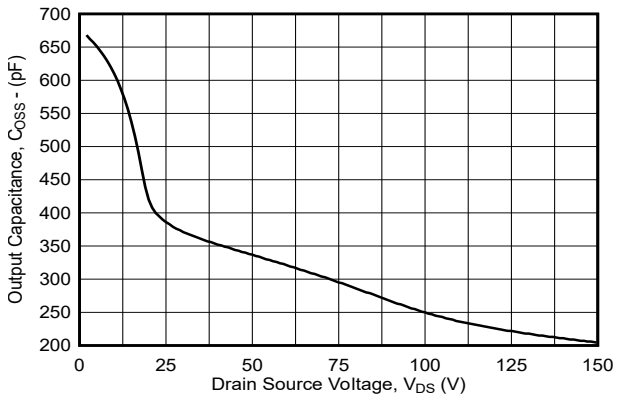

Figure 6-2. High-Side and Low-Side Output Capacitance vs Drain-Source Voltage

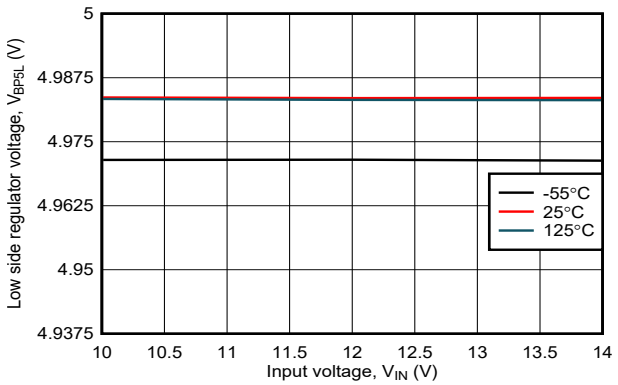

Figure 6-3. Low-Side Regulator, BP5L Output Voltage vs VIN Voltage

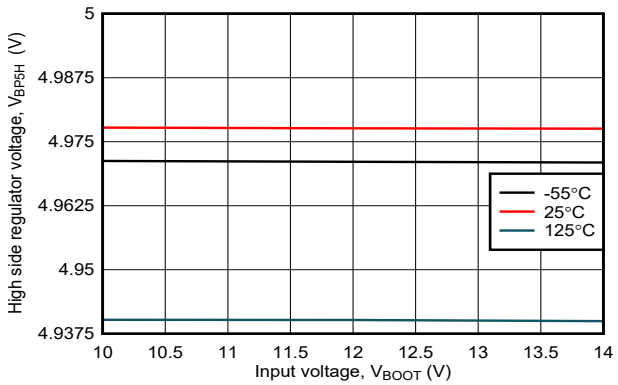

Figure 6-4. High-Side Regulator, BP5H Output Voltage vs VIN Voltage

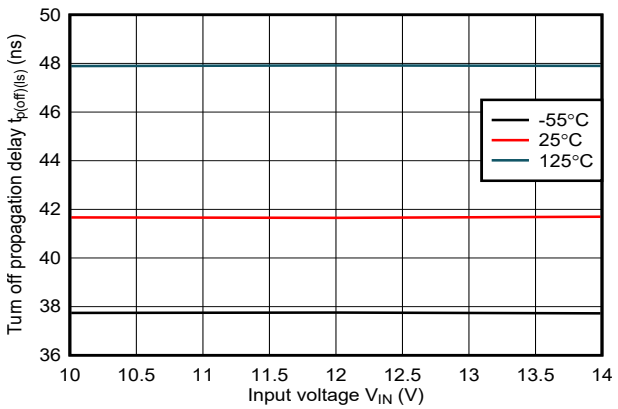

Figure 6-5. Low-Side Turn Off Propagation Delay vs VIN Voltage (PWM Mode)

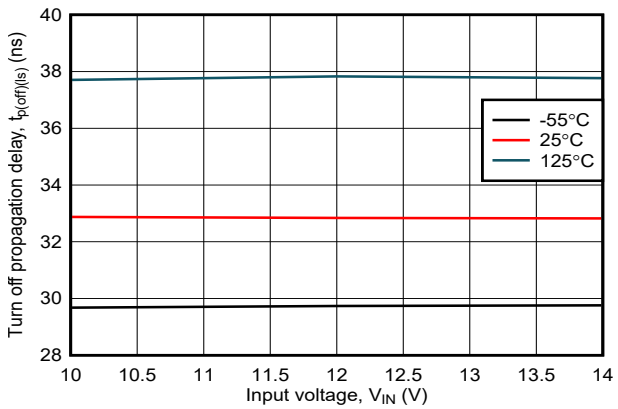

Figure 6-6. Low-Side Turn Off Propagation Delay vs VIN Voltage (IIM)

6.7 Typical Characteristics (continued)

Over ambient temperature operating range T_A = 25°C , VIN = 10V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).

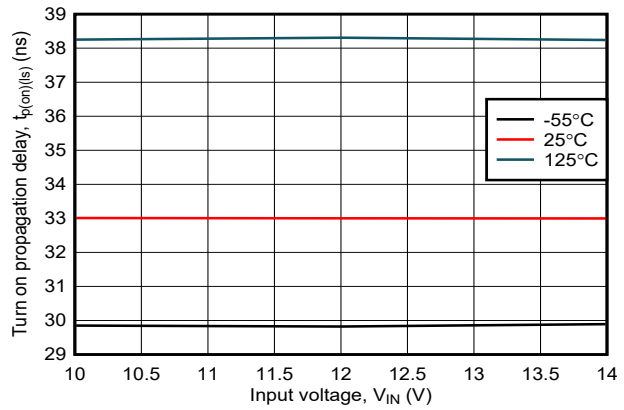

Figure 6-7. Low-Side Turn On Propagation Delay vs VIN Voltage (IIM)

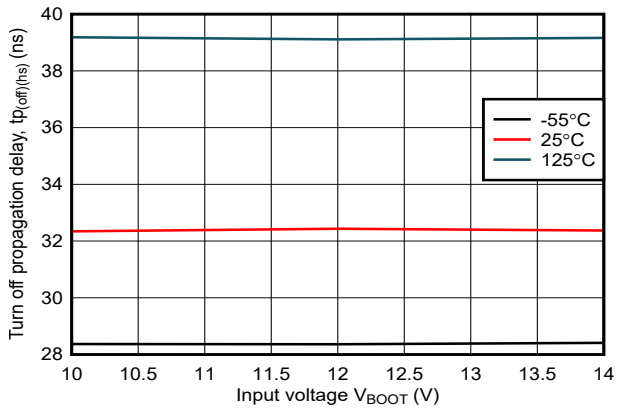

Figure 6-8. High-Side Turn Off Propagation Delay vs VIN Voltage (PWM)

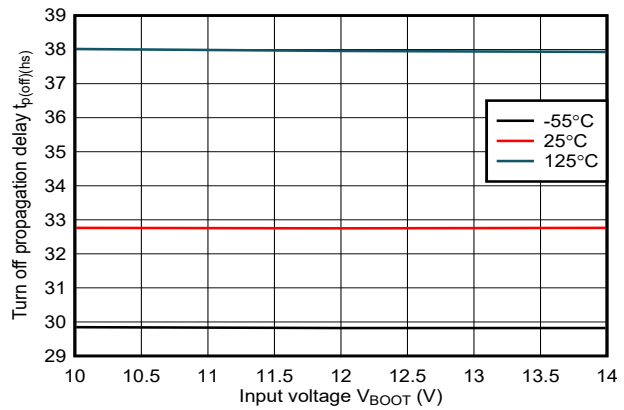

Figure 6-9. High-Side Turn Off Propagation Delay vs VIN Voltage (IIM)

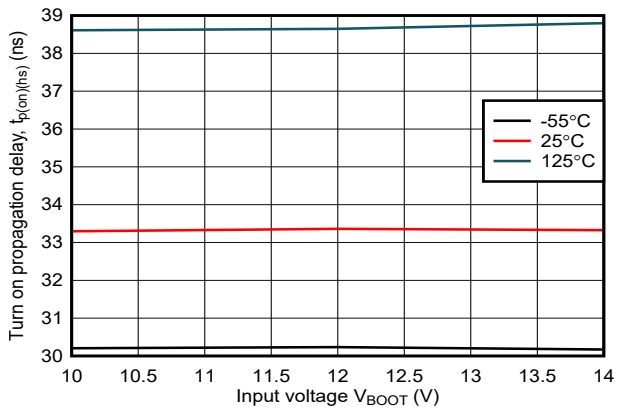

Figure 6-10. High-Side Turn On Propagation Delay vs VIN Voltage (IIM)

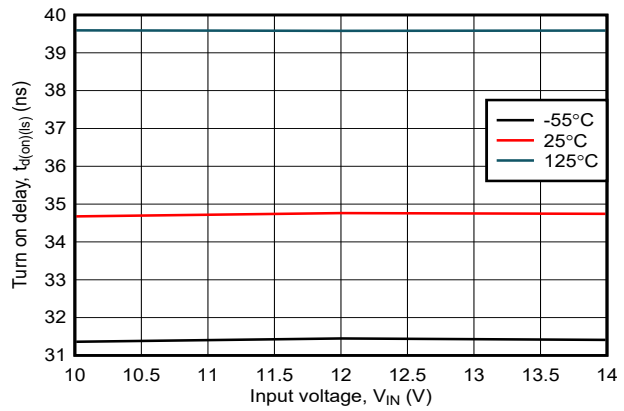

Figure 6-11. Low-Side Turn On Delay vs Input Voltage VIN (IIM)

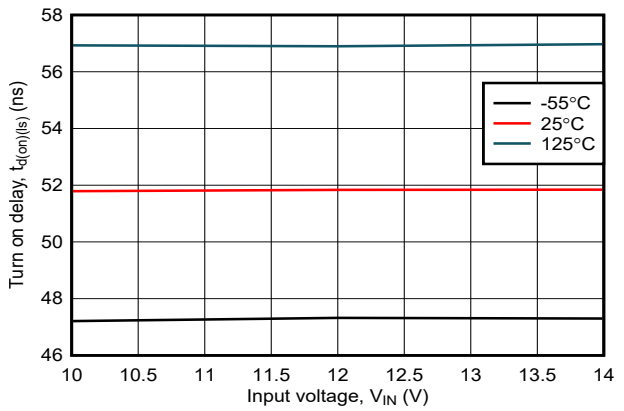

Figure 6-12. Low-Side Turn On Delay vs Input Voltage VIN (PWM)

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6.7 Typical Characteristics (continued)

Over ambient temperature operating range T_A = 25°C , VIN = 10V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).

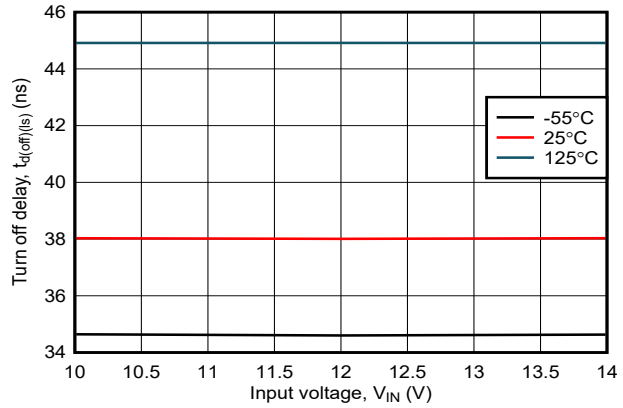

Figure 6-13. Low-Side Turn Off Delay vs Input Voltage VIN (IIM)

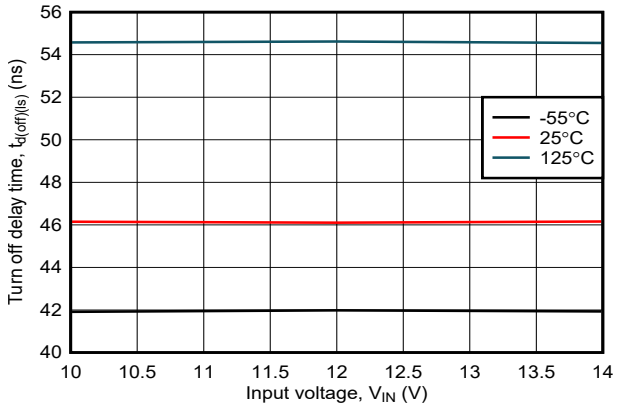

Figure 6-14. Low-Side Turn Off Delay vs Input Voltage VIN (PWM)

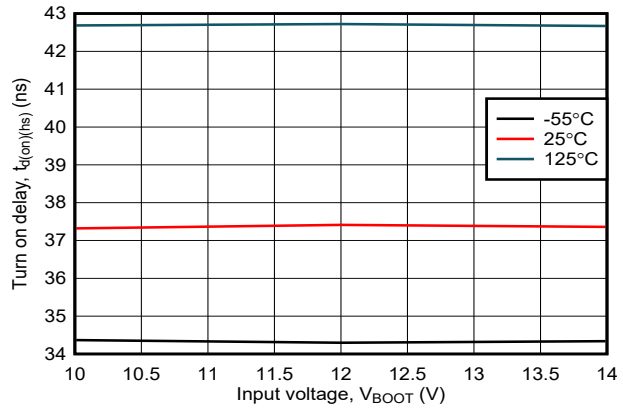

Figure 6-15. High-Side Turn On Delay vs Input Voltage (IIM)

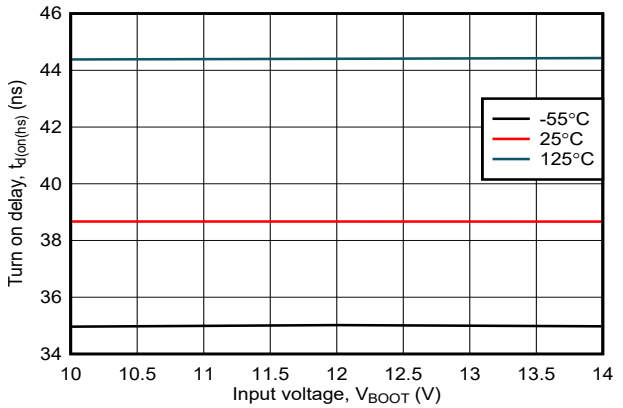

Figure 6-16. High-Side Turn On Delay vs Input Voltage (PWM)

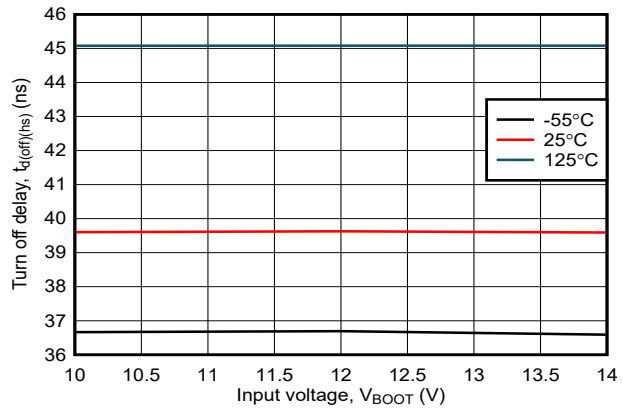

Figure 6-17. High-Side Turn Off Delay vs Input Voltage (IIM)

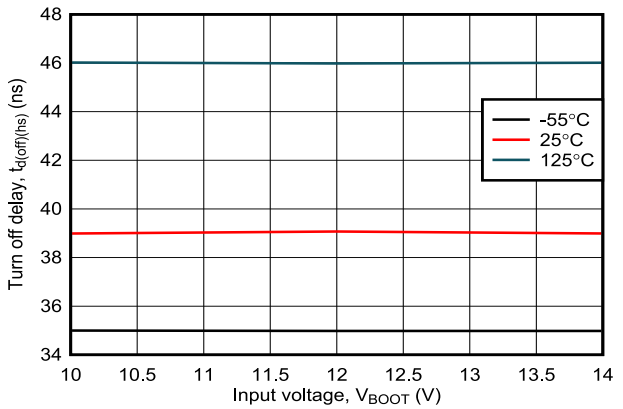

Figure 6-18. High-Side Turn Off Delay Voltage vs Input Voltage (PWM)

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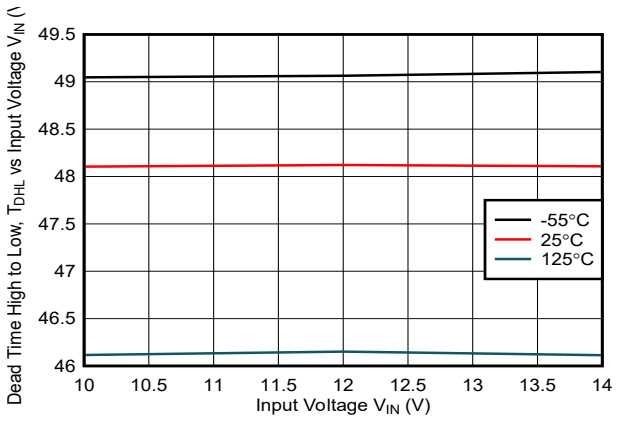
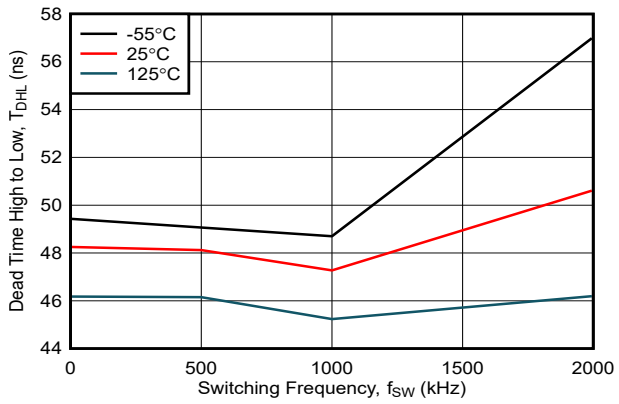
6.7 Typical Characteristics (continued)

Over ambient temperature operating range T_A = 25°C , VIN = 10V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).



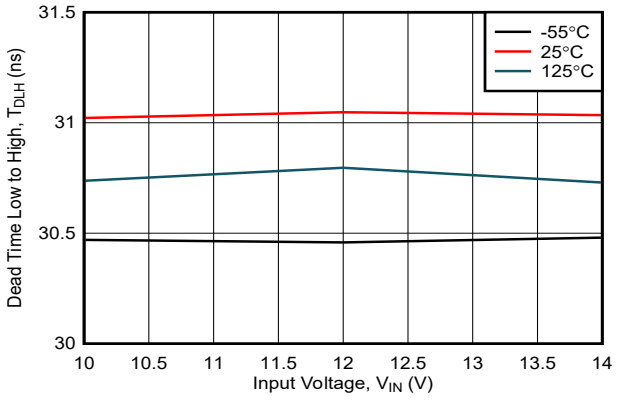
RLH = 57.6kΩ F_{SW} = 500kHz

Figure 6-19. Dead Time High to Low, T_{DHL} vs VIN Voltage



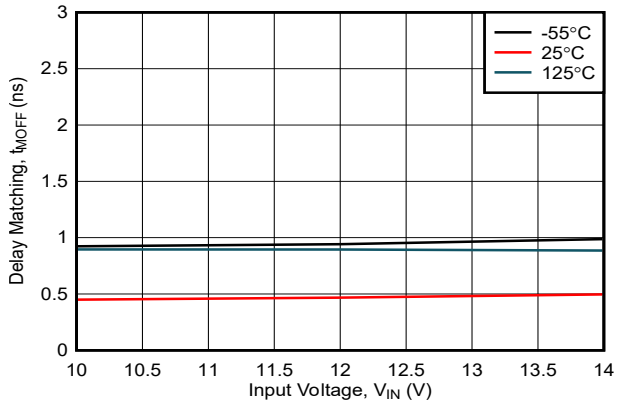
RHL = 57.6kΩ V_{IN} = 10V

Figure 6-20. Dead Time High to Low, T_{DHL} vs Switching Frequency



RLH = 35.7kΩ F_{SW} = 500kHz

Figure 6-21. Dead Time Low to High, T_{DLH} vs VIN Voltage



IIM Mode F_{SW} = 500kHz

Figure 6-22. Delay Matching Low-Side Off and High-Side On vs Input Voltage

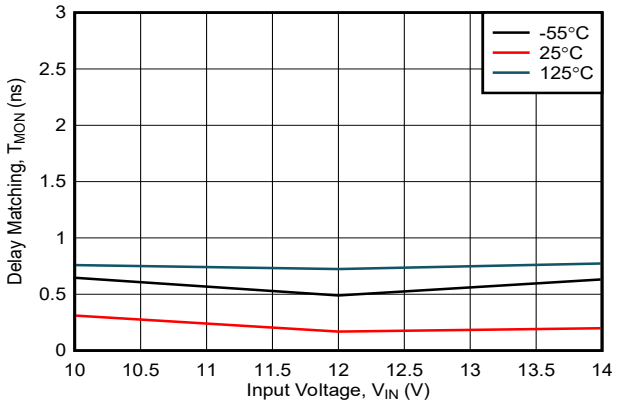
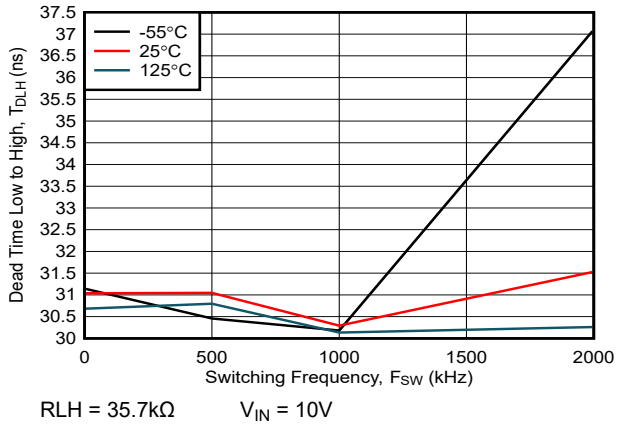


Figure 6-23. Delay Matching Low-Side On and High-Side Off vs Input Voltage



RLH = 35.7kΩ V_{IN} = 10V

Figure 6-24. Dead Time Low to High vs Switching Frequency

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6.7 Typical Characteristics (continued)

Over ambient temperature operating range T_A = 25°C , VIN = 10V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).

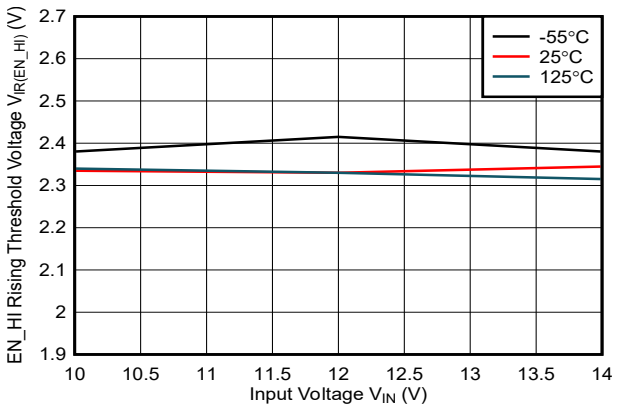

Figure 6-25. Input Rising Edge Threshold vs Input Voltage (EN_HI)

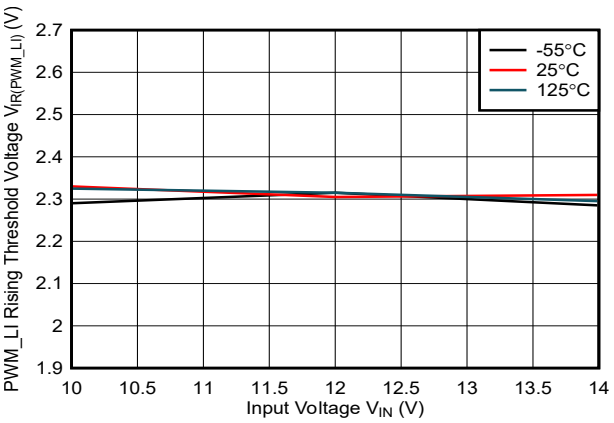

Figure 6-26. Input Rising Edge Threshold vs Input Voltage (PWM_LI)

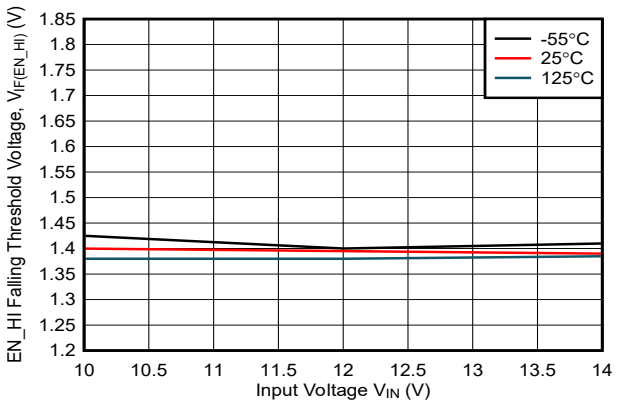

Figure 6-27. Input Falling Edge Threshold vs Input Voltage (EN_HI)

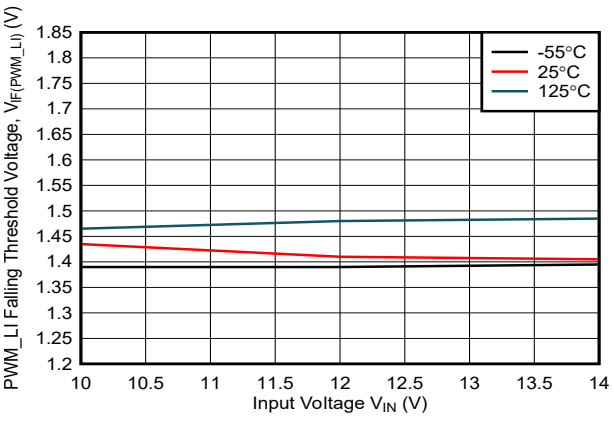

Figure 6-28. Input Falling Edge Threshold vs Input Voltage (PWM_LI)

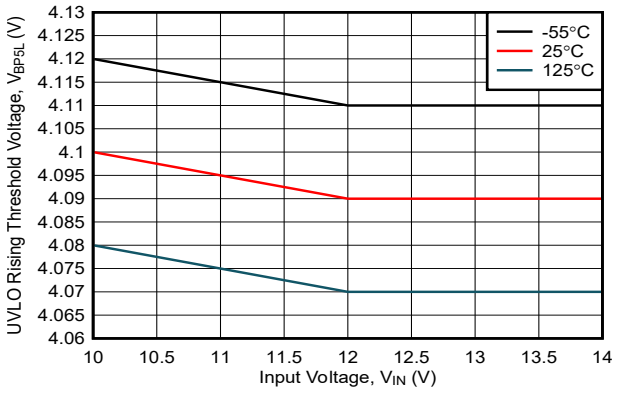

Figure 6-29. BP5L UVLO Rising Threshold vs VIN Voltage

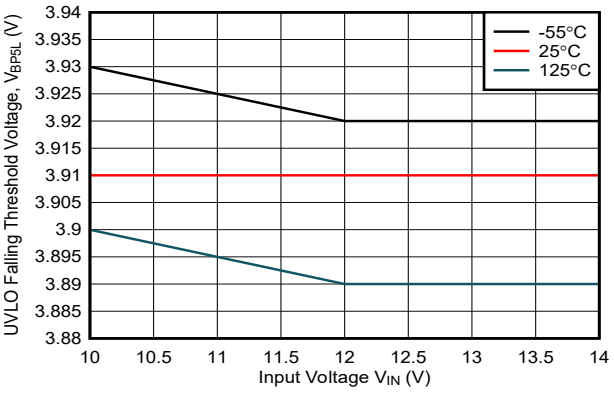

Figure 6-30. BP5L UVLO Falling Threshold vs VIN Voltage

6.7 Typical Characteristics (continued)

Over ambient temperature operating range T_A = 25°C , VIN = 10V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).

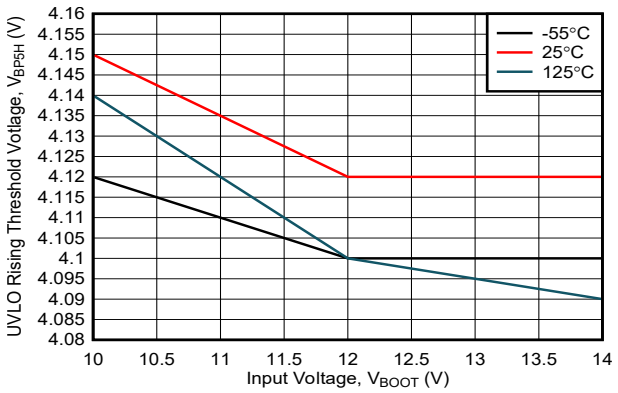

Figure 6-31. BP5H UVLO Rising Threshold vs BOOT Voltage

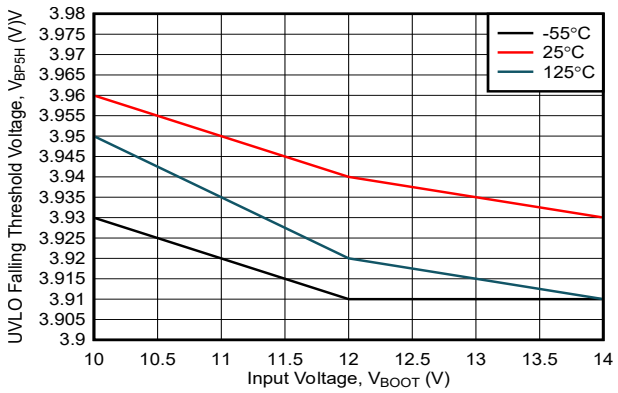

Figure 6-32. BP5H UVLO Falling Threshold vs BOOT Voltage

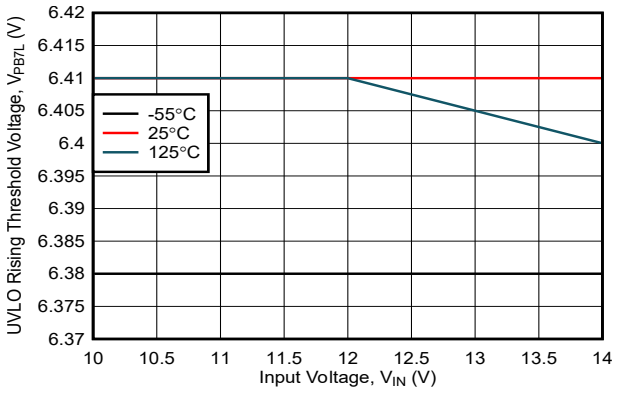

Figure 6-33. BP7L UVLO Rising Threshold vs VIN Voltage

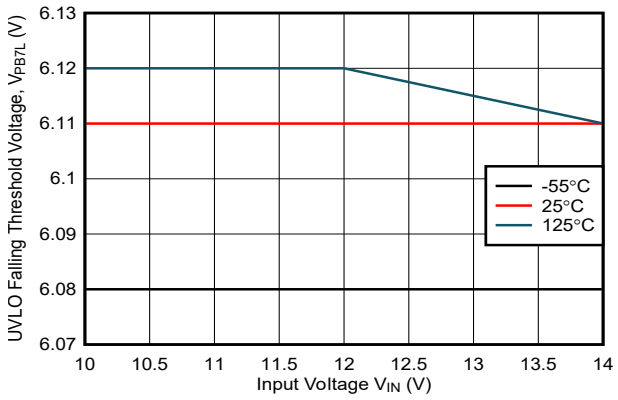

Figure 6-34. BP7L UVLO Falling Threshold vs VIN Voltage

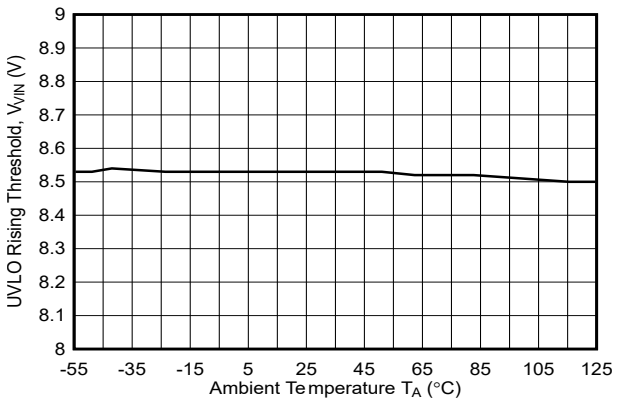

Figure 6-35. VIN UVLO Rising Threshold vs Temperature

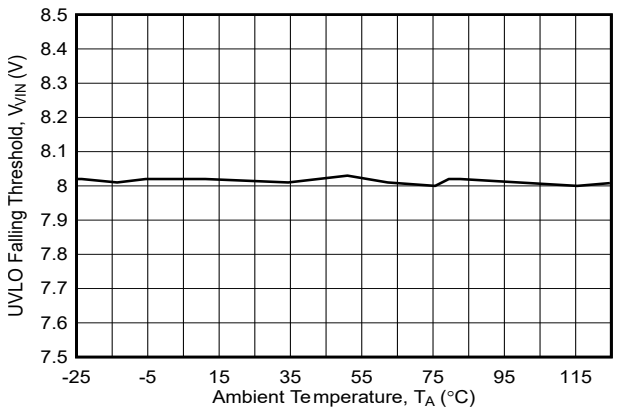

Figure 6-36. VIN UVLO Falling Threshold vs Temperature

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6.7 Typical Characteristics (continued)

Over ambient temperature operating range T_A = 25°C , VIN = 10V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).

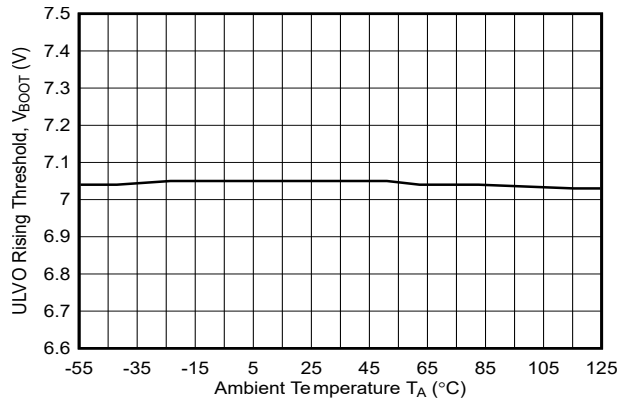


Figure 6-37. BOOT UVLO Rising Threshold vs Temperature

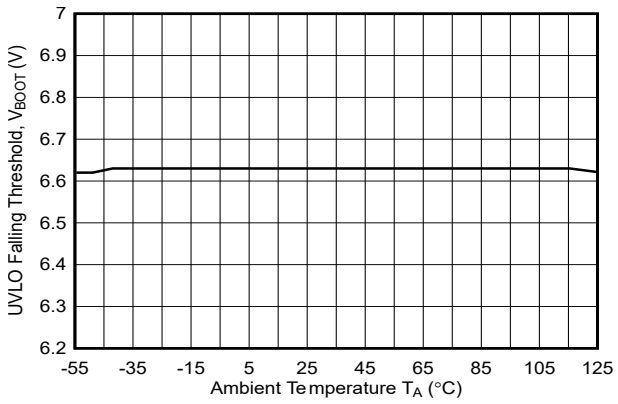


Figure 6-38. BOOT UVLO Falling Threshold vs Temperature

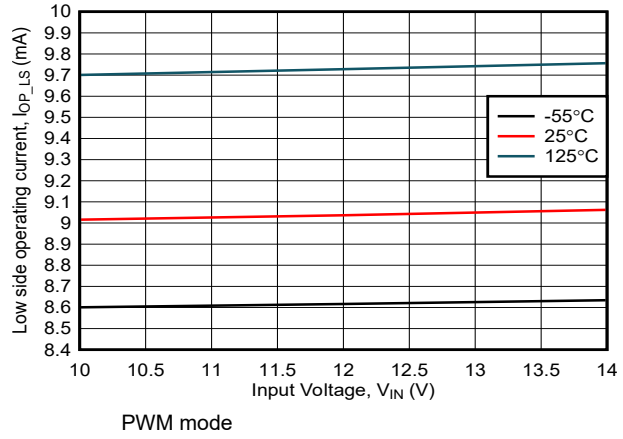


Figure 6-39. Low-Side Operating Current vs Input Voltage

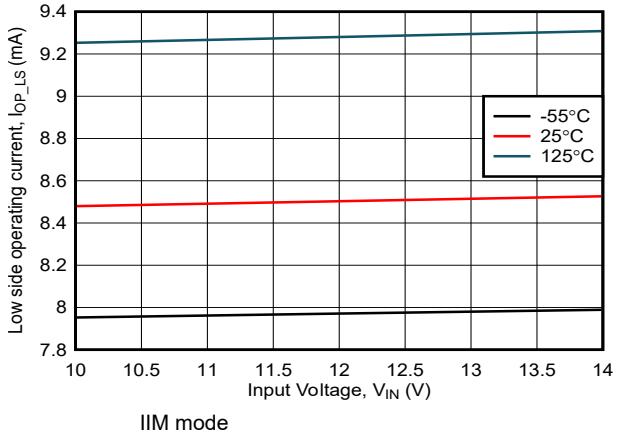


Figure 6-40. Low-Side Operating Current vs Input Voltage

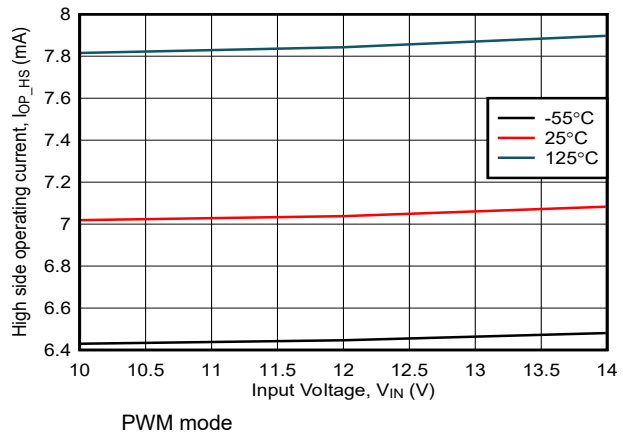


Figure 6-41. High-Side Operating Current vs Input Voltage

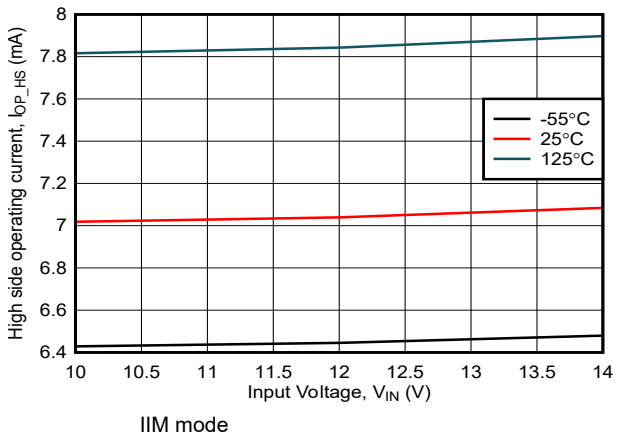
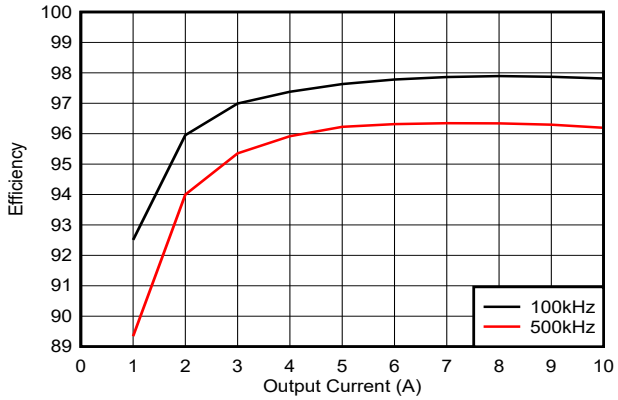


Figure 6-42. High-Side Operating Current vs Input Voltage

6.7 Typical Characteristics (continued)

Over ambient temperature operating range T_A = 25°C , VIN = 10V, HVIN = V_{SW_LS} = 5V, V_{SW_HS} = GND = 0V, $I_{DS(HS)}$ = $I_{DS(LS)}$ = 1mA (unless otherwise noted).



Synchronous half-bridge buck regulator

L = 22µH DCR_L = 2.64mΩ

Figure 6-43. 100V to 28V Efficiency

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7 Parameter Measurement Information

7.1 Timing Measurement

Figure 7-1 shows the circuit configuration used to measure the timing characteristics when in PWM Mode; when in PWM Mode, the FETs are configured in a "dual low-side" topology with independent test supplies. Figure 7-2 and Figure 7-3 show the measurement waveforms for propagation, turn-on and turn-off delays when configured in PWM Mode.

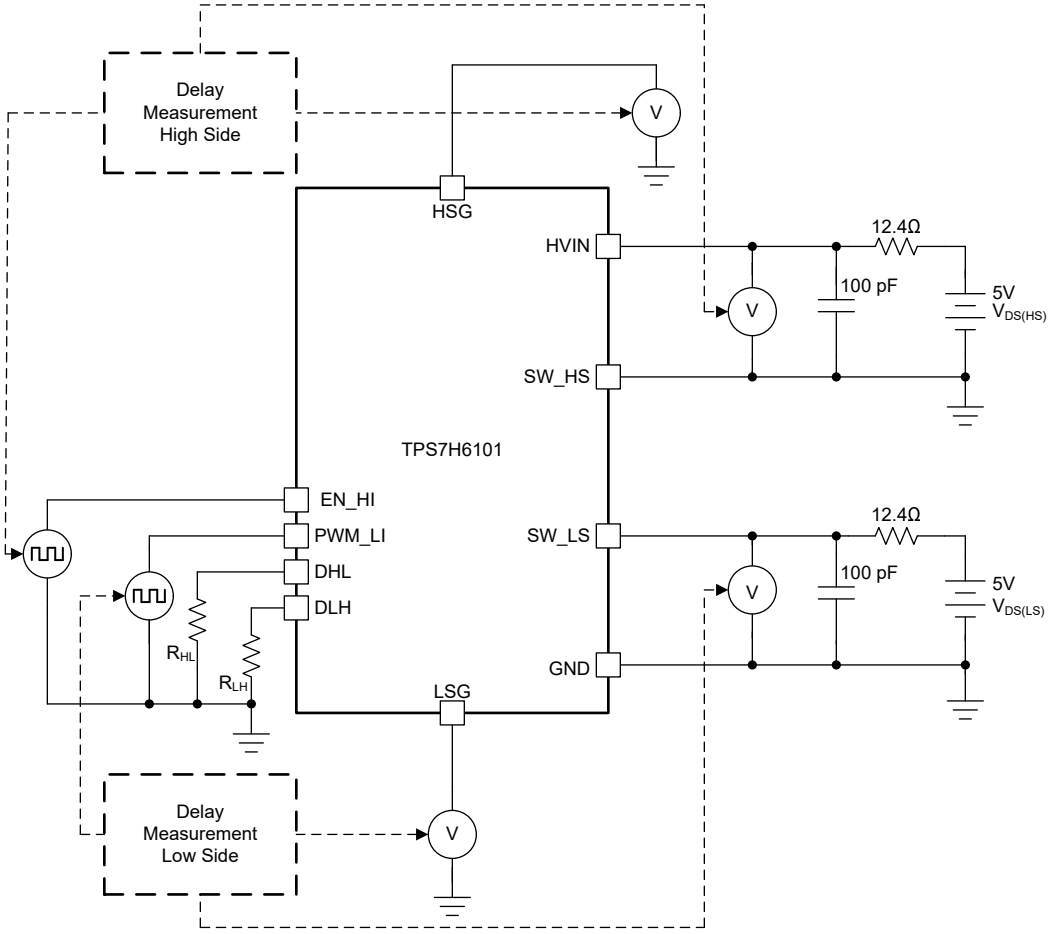

Figure 7-1. Timing Measurement: PWM Mode

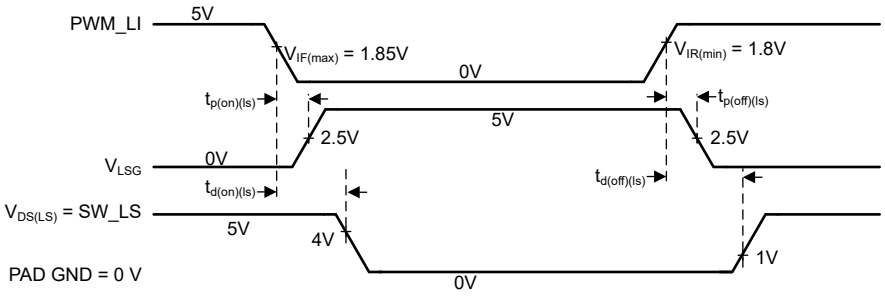

Figure 7-2. Low Side Timing Measurement Waveform: PWM Mode

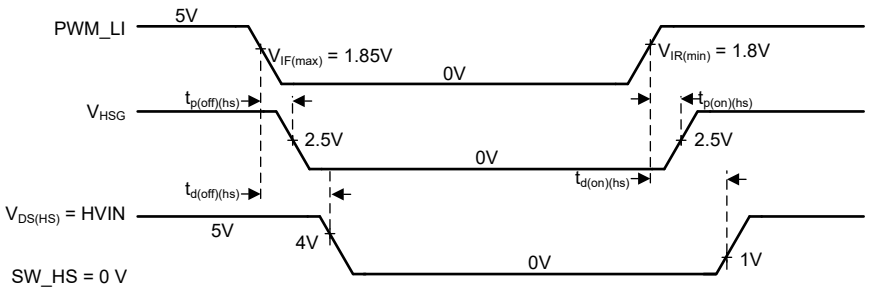

Figure 7-3. High Side Timing Measurement Waveform: PWM Mode

Figure 7-4shows the circuit configuration used to measure the timing characteristics when in Independent Input Mode (IIM); when in IIM Mode, the FETs are configured in a "dual low-side" topology with independent test supplies. Figure 7-5 and Figure 7-6 show the measurement waveforms for propagation, turn-on and turn-off delays when configured in IIM.

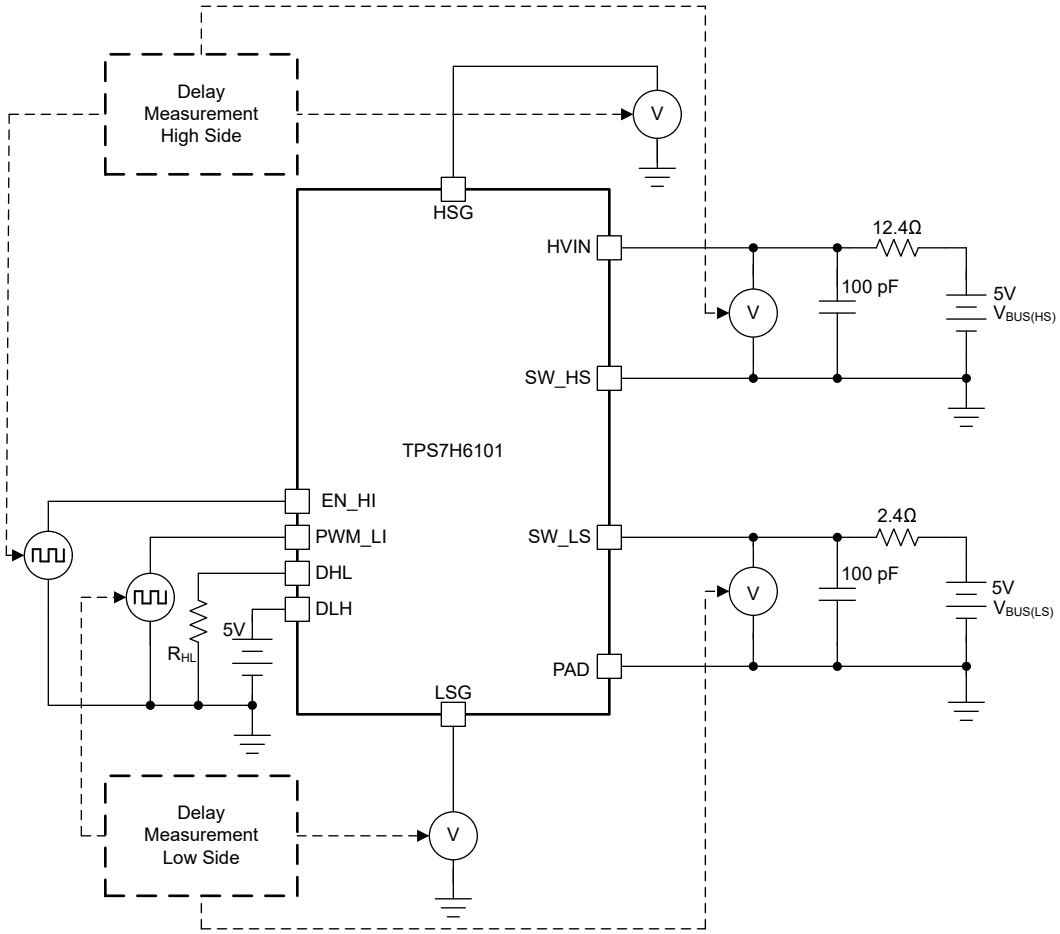

Figure 7-4. Timing Measurement: IIM

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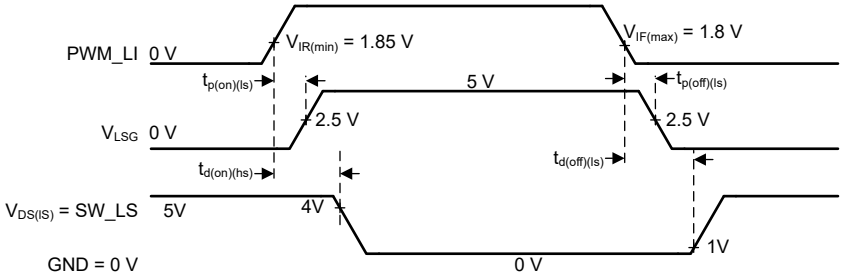

Figure 7-5. Low Side Timing Measurement Waveform: IIM

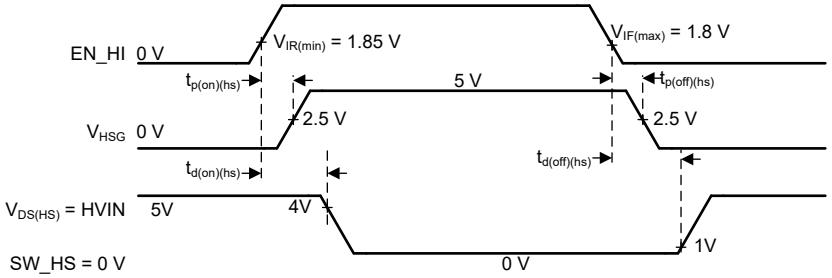

Figure 7-6. High Side Timing Measurement Waveform: IIM

7.2 Deadtime Measurement Information

When configured in PWM Mode the configurable dead times are measured per the figure below.

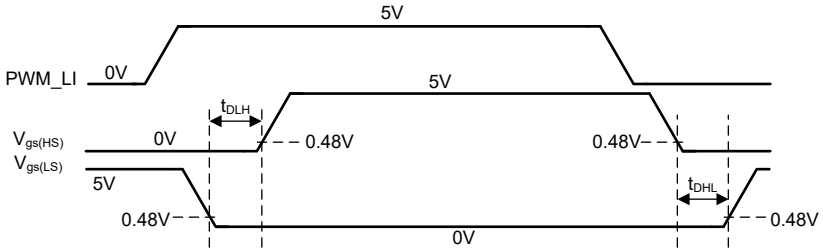

Figure 7-7. Dead Time Timing Measurement

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8 Detailed Description

8.1 Overview

The TPS7H6101 is a highly-integrated 200V e-mode GaN power-FET half bridge intended for use in synchronous buck converters, dual low-side topologies, and motor drives. The TPS7H6101 combines the half-bridge power FETs and isolated gate drivers in a 12mm by 9mm LGA package that minimizes junction-to-case thermal resistances, parasitic common mode inductance, and ohmic losses.

The driver can operate up to 2MHz, which enables use in high frequency, high efficiency GaN based power converter designs. The driver is designed to have a propagation delay of 35ns (typical) as well as 5.5ns (typical) high-side to low-side delay matching.

An external bootstrap diode is required for the gate driver and as such, the user has the ability to optimize the diode based on the application. The driver contains an internal switch in series with the bootstrap diode that can be used to prevent overcharging of the bootstrap capacitor and decreases reverse recovery losses in the diode.

The gate driver has two modes of operation: PWM mode and Independent Input Mode (IIM). The dual mode operation allows for the gate driver to be used with a wide number of PWM controllers to enable both synchronous rectifier control and GaN FET compatibility. The user also has the option to enable input interlock protection in IIM, allowing for anti-shoot through protection in synchronous buck and half-bridge topologies.

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8.2 Functional Block Diagram

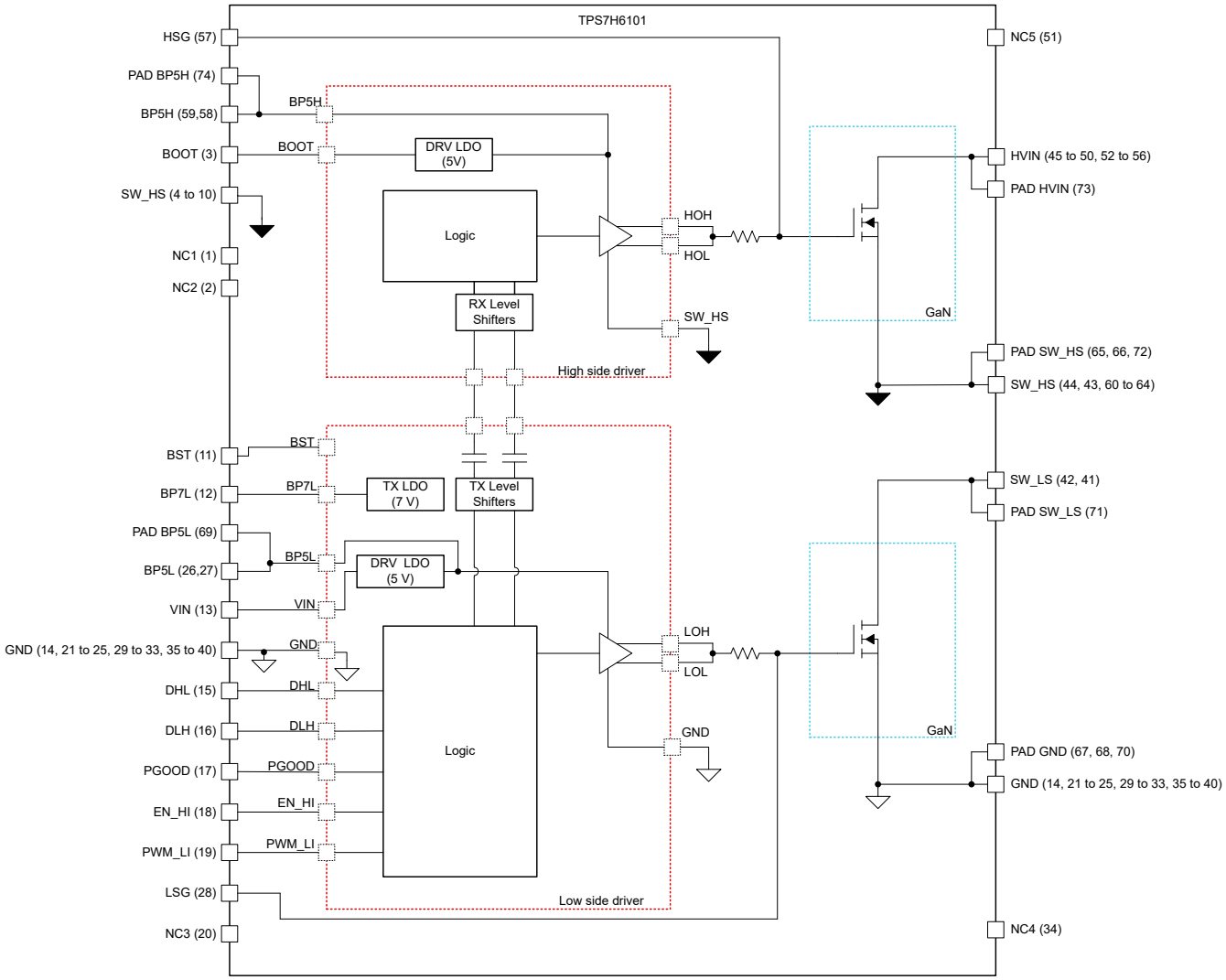

Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Gate Drive Input Voltage

During steady state operation, the input voltage of the gate drive for the TPS7H6101 must be between 10V and 14V. This voltage serves as the input to the two low-side linear regulators, BP5L and BP7L. The external high-side bootstrap capacitor is also charged from VIN (see *Bootstrap Charging*). For best performance, add a bypass capacitor from VIN to AGND. Place this bypass capacitor as close to the gate driver as possible.

8.3.2 Linear Regulator Operation

The TPS7H6101 contains three internal linear regulators: BP5L, BP7L, and BP5H. BP5L and BP7L are included on the low side of the driver. These linear regulators provide 5V and 7V, respectively, as the nominal output voltages.

BP5L is used to power the low-side logic circuitry as well as the low-side gate drive voltage. The BP5L regulator has an accuracy of 5V +3.5% /-5% to provide the proper voltage for driving GaN FETs.

BP7L powers the low-side transmitters within the driver. A minimum capacitor of 1µF is also required from the BP7L pin to GND and PAD GND must be externally connected and placed as close as possible to the package TPS7H6101-SP.

On the high side, the voltage on BOOT serves as the input to the high side linear regulator BP5H. Similar to BP5L on the low-side, this regulator is used to power the high-side logic circuitry while providing the 5V +3.5%/-5% high-side gate voltage to the high side FET. A minimum capacitor of 1µF is required from BP5H to SW_HS. The recommendation for all internal linear regulators is that these not be externally loaded other than where indicated within this document.

8.3.3 Bootstrap Operation

To generate the power for the high-side gate driver circuitry when used in a half-bridge configuration, the gate driver requires the use of a bootstrap circuit. The selection of the TPS7H6101 bootstrap components is critical for proper gate driver operation. There are also various methods for bootstrap capacitor charging that can be utilized for this device.

8.3.3.1 Bootstrap Charging Methods

The TPS7H6101 provides the user several options for charging the bootstrap capacitor. The flexibility is to allow for operation with a wide range of PWM controllers, and also to allow the user to select an option with trade-offs that are most desirable for the specific application. In both instances, a bootstrap resistor is recommended to limit the bootstrap current during initial startup. The bootstrap resistor and capacitor need to be chosen such that sufficient time is allowed for the re-charge of the capacitor for the specific application.

The first option is to allow for charging of the bootstrap capacitor through the internal bootstrap switch of the driver. This switch is internally connected between VIN and BST pins and the bootstrap diode is connected externally between BST (anode) and BOOT (cathode). The bootstrap switch is only on when the low side driver output is on. By disallowing bootstrap charging during the converter dead times, the maximum voltage across the bootstrap capacitor can be reduced. The internal bootstrap switch has a parallel resistance of 1kΩ that allows for slow charging the bootstrap capacitor at start-up before low-side FET turn-on.

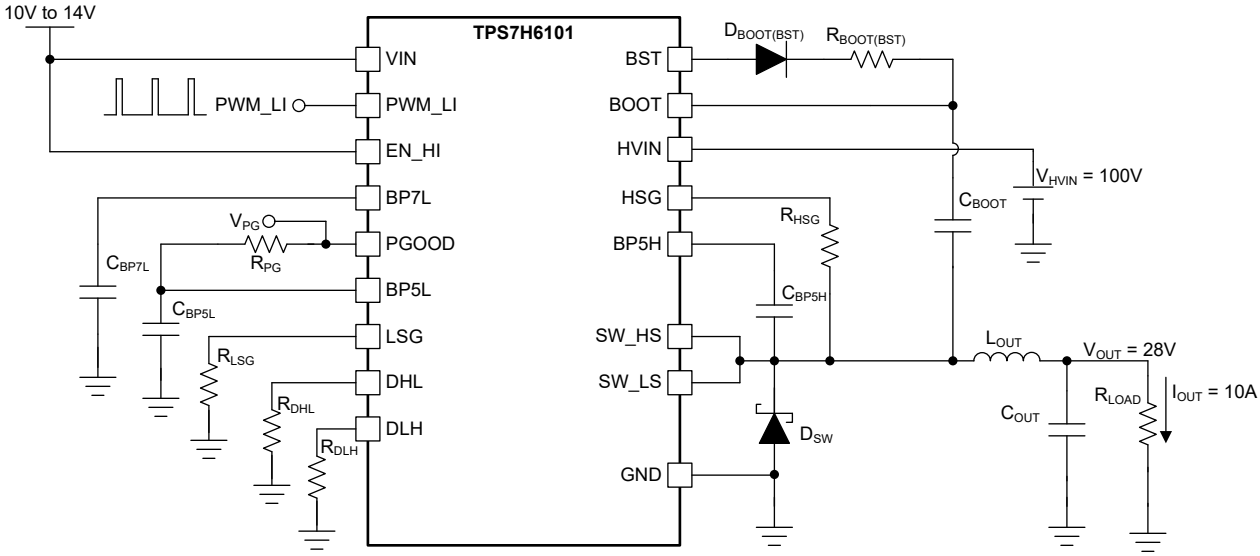

Figure 8-2. Internal Switch Bootstrap Charging Configuration

Another option is to charge the bootstrap capacitor directly from VIN. This is a more conventional method used with half-bridge drivers. This option can be considered in a number of use cases, but is particularly helpful in instances where the low-side FET turn-on is not immediate. This is the case when using the TPS7H6101 with one of the three controllers in the TPS7H500x-SP family that have integrated synchronous rectification outputs. The synchronous rectification outputs are disabled during soft-start, and as such, when implementing a synchronous buck topology the bootstrap capacitor cannot be charged through the internal bootstrap switch of the driver. The bootstrap switch does have the parallel resistor for slow-charging, but sequencing and/or startup requirements for the converter can potentially dictate that the charging need to occur more rapidly. When using the direct VIN charging, the options for preventing overcharging of the bootstrap capacitor are to add a resistor in series with the bootstrap capacitor, to add a Zener diode in parallel with the bootstrap capacitor, or a combination of both. A consideration that must be made if using the Zener diode is that has an associated leakage current during normal operation, which contributes to the overall converter losses.

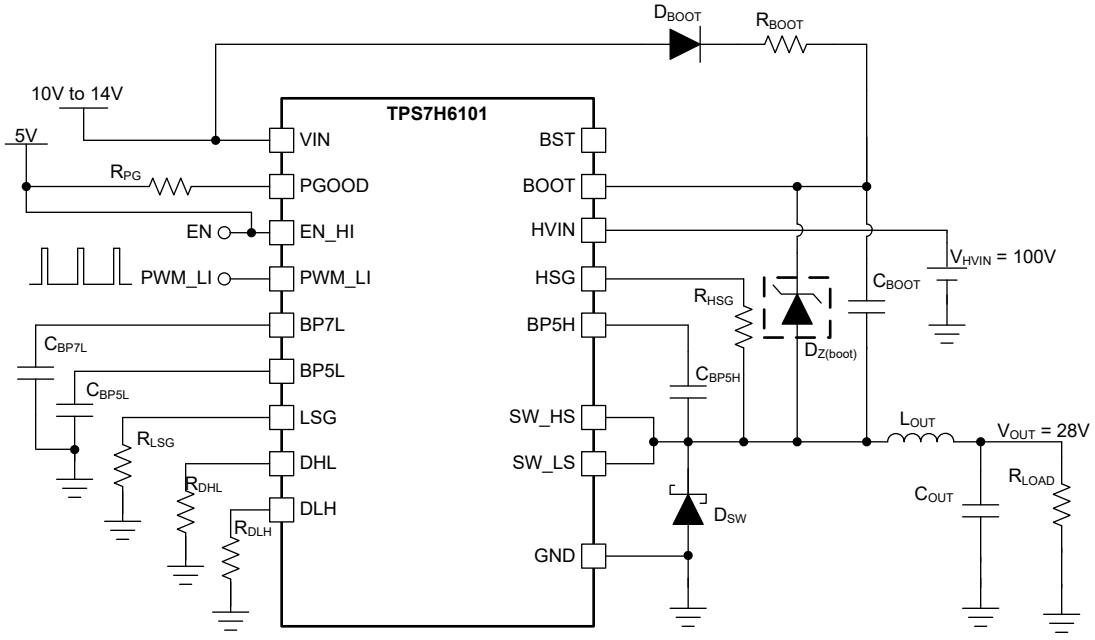

Figure 8-3. Direct V_{IN} Bootstrap Charging Configuration

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A dual-charging option can be considered, which is a combination of the bootstrap switch and direct VIN charging methods. This method offers the benefit of circumventing any potential bootstrap charging issues during startup due to the low-side FET not turning on, while also taking advantage of the reduction of bootstrap voltage during normal operation offered by the internal switch. The series resistor used with the bootstrap diode in the direct VIN charging path must be higher than the resistance of the internal bootstrap switch to make sure that the charging is via the bootstrap switch during normal operation. This higher resistor value also effectively reduces the Zener current during normal operation. The trade-off for this configuration is the additional part count.

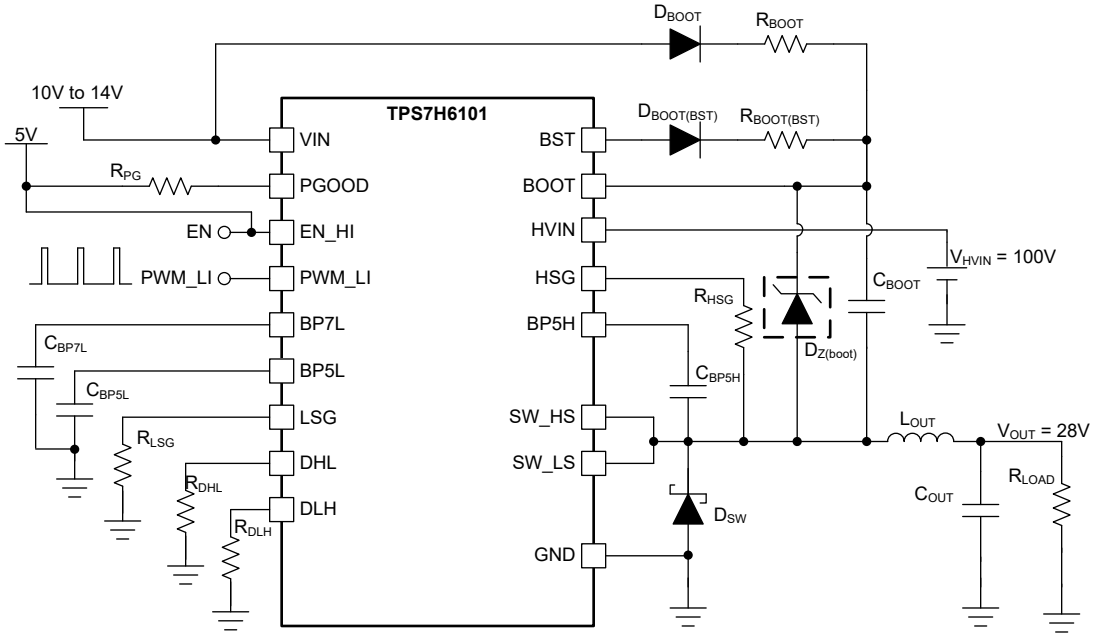

Figure 8-4. Dual Bootstrap Charging Configuration

For two independent switch topologies, in which SW_HS and GND are referenced to a common ground,(e.g. push-pull topology); the following configuration for the BOOT and BST pins is recommended.

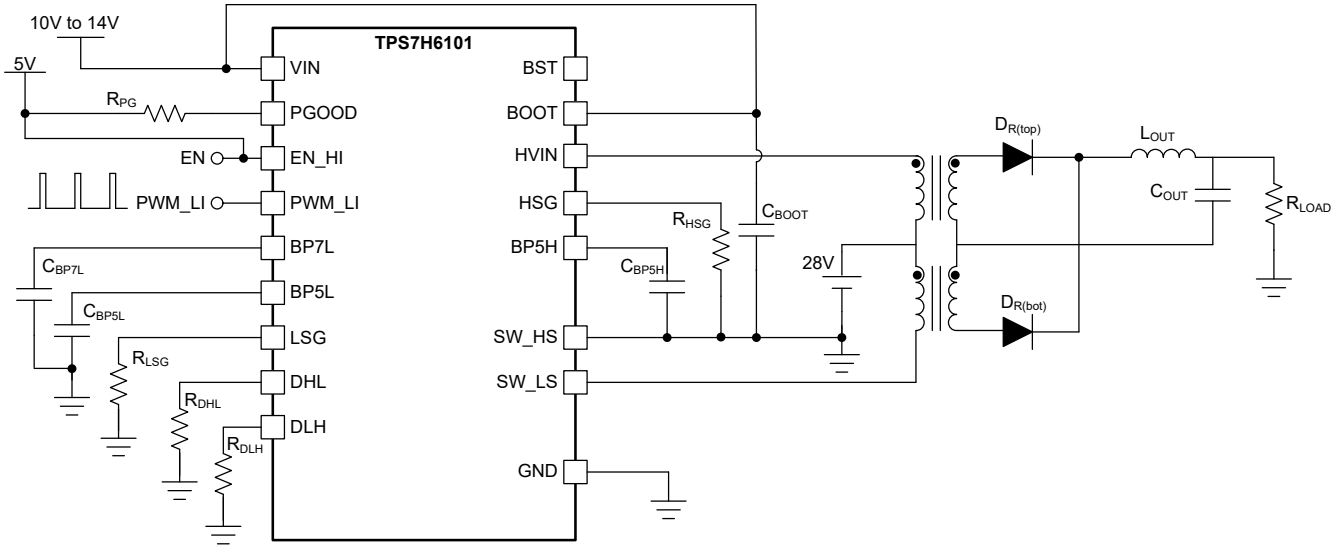

Figure 8-5. Common Ground Referenced Bootstrap Configuration

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8.3.3.2 Bootstrap Capacitor

The external bootstrap capacitor that is required for the driver is connected between BOOT and SW_LS. The bootstrap capacitor voltage serves as the input to the high-side linear regulator BP5H that provides the gate drive voltage for the high-side GaN FET. A general guideline for bootstrap capacitor selection is to specify the capacitance at least 10× greater than the gate capacitance of the high-side GaN FET that is being driven:

Selecting a C_{BOOT} cap value of 1µF satisfies Equation 1.

$$C_{BOOT} \geq 10 \times C_{ISS} \tag{1}$$

where:

- C_{ISS} = 600pF (typ), gate capacitance for the high-side GaN FET

A more detailed calculation of the minimum bootstrap capacitance needed is show below using Equation 3:

$$C_{BOOT} \geq \frac{Q_{total}}{\Delta V_{BOOT}} \tag{2}$$

$$Q_{total} = Q_G + I_{QBG} \times \frac{D_{MAX}}{f_{SW}} + \frac{I_{QHS}}{f_{SW}} \tag{3}$$

where:

- Q_g = 5nC (typ), total gate charge for the high-side GaN FET
- I_{QBG} is the BOOT to GND quiescent current
- D_{MAX} is the maximum duty cycle
- I_{QHS} is the high-side quiescent current
- f_{SW} is the switching frequency

and ΔV_{BOOT} is the maximum allowable drop on BOOT for proper operation:

$$\Delta V_{BOOT} = VIN - (n \times V_F) - (I_{BOOT} \times (R_{BOOT} + R_{SW})) - V_{BOOT\_UVLO} \tag{4}$$

where:

- VIN is the gate driver input voltage
- I_{BOOT} is the bootstrap charging current
- R_{SW} is the resistance of the internal bootstrap switch
- R_{BOOT} is resistance of the external bootstrap resistor
- n is the number of external bootstrap diodes placed in series
- V_F is the forward voltage drop of the bootstrap diode
- V_{BOOT_UVLO} is the falling undervoltage lockout threshold of BOOT (6.4V typical)

For applications where the internal bootstrap switch is not used, omit the R_{SW} term from the calculation. Selection of a bootstrap capacitor with low ESR and ESL is recommended. Include in the voltage rating of the bootstrap capacitor sufficient margin above the maximum expected bootstrap voltage.

8.3.3.3 Bootstrap Diode

Regardless of the method of charging the bootstrap capacitor, the TPS7H6101 requires an external bootstrap diode rated to withstand the input voltage that is applied to the converter power stage in the half-bridge configuration. Care must be taken when selecting the external bootstrap diode. The bootstrap diode needs to be capable of handling peak transient currents that occur during the startup period. Select fast recovery diodes in the bootstrap circuit. The user needs to examine the I-V characteristics of the selected diode to verify that the forward voltage under the intended operating conditions does not become too large to trigger the undervoltage lockout of the BP5H regulator. Overall, the user needs to meet the conditions of Equation 5:

$$VIN - (n \times V_F) - (I_{BOOT} \times (R_{BOOT} + R_{SW})) \geq V_{BOOT\_UVLO} \tag{5}$$

where:

- VIN is the gate driver input voltage
- I_{BOOT} is the bootstrap charging current
- R_{BOOT} is the resistance of the external bootstrap resistor
- R_{SW} is the resistance of the internal bootstrap switch
- n is the number of external bootstrap diodes placed in series
- V_F is the forward voltage drop of the bootstrap diode
- V_{BOOT_UVLO} is the falling undervoltage lockout threshold of BOOT (6.4V typical)

For applications where the internal bootstrap switch is not used, omit the R_{SW} term from the calculation.

8.3.3.4 Bootstrap Resistor

The bootstrap resistor is used to (1) limit the peak current during gate driver startup and (2) control the slew rate (dv/dt) at BOOT. The peak current through the bootstrap diode, and through the BST switch if utilized, can become excessively high during the initial charging period. Furthermore, excessive slew rates at BOOT can cause a slight overshoot of the BP5H voltage during startup. To mitigate these issues a bootstrap resistor of at least 2Ω is recommended.

While the bootstrap resistor does alleviate peak current and slew rate issues, this resistor in conjunction with the bootstrap capacitor introduces a time constant τ:

$$\tau = \frac{R_{BOOT} \times C_{BOOT}}{D} \quad (6)$$

where:

- R_{BOOT} is the value of the bootstrap resistor in ohms
- C_{BOOT} is the value of bootstrap capacitor in Farads
- D is the duty cycle of the switching converter

The time required to charge and refresh the charge of the bootstrap capacitor needs to be checked against the time constant. Lastly, the resistor can experience high power dissipation during the initial charging period. Select a resistor that can handle the energy during this charging period:

$$E = \frac{1}{2} \times C_{BOOT} \times V_{BOOT}^2 \quad (7)$$

where:

- C_{BOOT} is the value of bootstrap capacitor in Farads
- V_{BOOT} is the final voltage of the bootstrap capacitor

8.3.4 High-Side Driver Startup

For proper startup up of the high side, the BOOT to SW voltage must be greater than the BOOT UVLO rising threshold value of 6.65V (typical). In half-bridge converter configurations that have a pre-bias voltage present at the output, the bootstrap capacitor is unable to adequately charge from VIN until the output voltage is sufficiently discharged. This same behavior can be seen during a brownout of VIN in which the input voltage temporarily decreases below the VIN UVLO falling threshold. Upon recovery, the low-side driver initiates resumption of normal operation, but the turn-on of the high-side driver is delayed due to the output voltage that is present on the converter. This is a problem that is inherent in half-bridge gate drivers. Discharge circuits at the converter output can help alleviate the problem by forcing the output to a low voltage, only after which gate drive startup is attempted.

8.3.5 PWM_LI and EN_HI

The input pins of the TPS7H6101 are PWM_LI and EN_HI. Each of these pins has an internal pull-down resistance of approximately 200kΩ (typical). The functions of these pins vary depending on the selected mode of operation of the gate driver as described in Device Functional Modes. In PWM mode, PWM_LI serves as the input pin for the single PWM control signal into the driver and EN_HI is an enable pin for the driver. In

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independent input mode, PWM_LI serves as the low-side input and EN_HI serves as the high-side input. The inputs are capable of withstanding voltages up to 14V, which allows them to be directly connected to the outputs of an analog PWM controller with a power supply voltage less than or equal to 14V. If operating in independent input mode and either of the two input channels PWM_LI or EN_HI is not used then connect the unused input to GND.

8.3.6 Dead Time

When operating in PWM mode, resistors to GND are required on both DLH and DHL to program the dead time. The DHL resistor sets the dead time between high-side gate (V_{HSG}) turn-off to low-side gate (V_{LSG}) output turn-on. Likewise, the resistor on DLH sets the dead-time between low-side gate (V_{HSG}) turn-off to high-side (V_{LSG}) turn-on. The resistor can be used to set the dead time from a minimum value of roughly 0.8ns up to 100ns. The resistor must be populated on both pins to operate the device in this mode. Refer to Figure 7-7 diagram.

The dead time values selected are critical as these directly impact that losses that occur in the converter during these periods. The dead time is carefully chosen to avoid cross-conduction between the high-side FET and low-side FET, while also minimizing the third-quadrant conduction time for the GaN FETs. T_{DLH} and T_{DHL} have been selected to minimize third quadrant time and avoid cross conduction events.

Equation 8 and Equation 9 can be used to obtain typical deadtime resistor values with the nearest E192 resistor value selected below.

R_{DHL}:

$$\mathrm{RHL} = 1.246 \times \mathrm{T_{DHL}} + 5.13 = (1.246 \times 42.5\mathrm{ns}) + 5.13 = 58.05\mathrm{k\Omega} \quad (8)$$

A value of 57.6kΩ is selected for RHL.

R_{DLH}:

$$\mathrm{RLH} = 1.046 \times \mathrm{T_{DLH}} - 1.355 = (1.064 \times 35\mathrm{ns}) - 1.355 = 35.3\mathrm{k\Omega} \quad (9)$$

A resistor value of 35.7kΩ was used for RLH.

8.3.7 Input Interlock Protection

The TPS7H6101 can be configured to have input interlock protection in independent input mode (IIM). To activate the input interlock protection in IIM, DHL must be connected to 5V while DLH has a resistor (valued between 100kΩ and 220kΩ) connected between the pin and GND. This protection is intended to improve the robustness and reliability of the power stage with which the driver is being used by preventing shoot-through of the GaN FETs in a half-bridge configuration. In any instance when the protection is enabled and both inputs are logic high, the internal logic turns both of the outputs off. Both outputs remain off until one of the inputs goes low, in which case the outputs resume following the input logic. There is no fixed time deglitching for this feature that does not impact the propagation delay and dead time of the driver. Small filters at the inputs of the driver can be utilized to improve robustness in noise prone applications.

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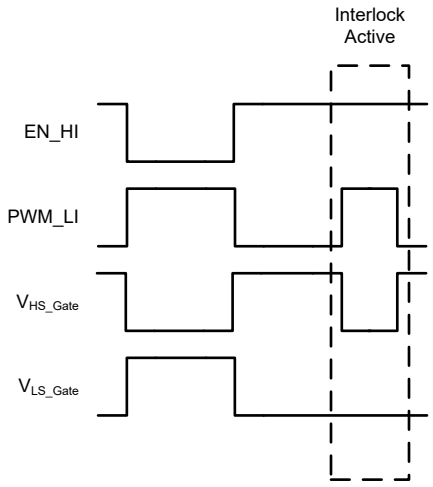

Figure 8-6. Interlock Input Protect

8.3.8 Undervoltage Lockout and Power Good (PGOOD)

The TPS7H6101 has undervoltage lockout (UVLO) on BP5L, BP7L, BP5H, BOOT, and VIN. When the output voltage on any of the low-side linear regulators or VIN falls below the UVLO threshold (4.05V for the BP5L linear regulator, 6.25V for the BP7L linear regulator, and 8V for VIN), the PWM inputs are ignored to prevent the GaN FETs from partial turn-on. In this scenario, the UVLO actively pulls the Low Side Gate and High Side Gate low. When the low-side regulators and VIN are each above the respective UVLO threshold but one of the high-side UVLOs is triggered (4.05V for BP5H and/or 6.4V for BOOT), then only High Side Gate is pulled low.

The gate driver also has a power good (PGOOD) pin, which indicates when any of the low-side linear regulators have entered undervoltage lockout. The pin enters the logic-high state when all low-side regulators and VIN each have surpassed the respective rising UVLO threshold. The pin goes, or remains, logic-low if any one of these linear regulators or VIN falls below the corresponding falling UVLO threshold. The PGOOD pin has an internal pull-down resistance of 1MΩ when the pin is in the logic-high state. A pull-up of 10kΩ connected from PGOOD to BP5L is recommended.

8.3.9 Negative SW Voltage Transients

Though enhancement mode GaN FETs do not contain a body diode like silicon FETs, the devices are capable of reverse conduction due to the symmetrical device structure. During the reverse conduction periods, the source-drain voltage of the integrated GaN FET is typically 2.1V, which is higher than what is encountered with a traditional silicon FET. As such, the switch node pins of the driver (SW_HS and SW_LS are externally tied together and are collectively referred to as SW) have a negative voltage present. This negative transient can lead to an excessive bootstrap voltage, since BOOT is always referenced to SW. Furthermore, the printed circuit board layout and device parasitic inductances can further intensify the negative voltage transients. The recommended implementation of the bootstrap circuity aids in reducing the likelihood of excessive negative BOOT to SW voltage. Operating at a bootstrap voltage above the absolute maximum of 16V can be detrimental to the gate driver, so care must be taken to make sure that the maximum BOOT to SW voltage differential is not exceeded. Generally, BOOT follows SW instantaneously so that the BOOT to SW voltage does not overshoot significantly. However, to further increase assurance that excessive voltage is not present at the Boot pin, an external Zener diode can be used between BOOT and SW to clamp the bootstrap voltage to acceptable values during operation.

8.3.10 Level Shifter

The integrated TX and RX level shifters interface between the inputs on the low-side to the high-side driver stage which is referenced to the high voltage switch node (ASW). The level shifters allow control of the High Side Gate output. The level shifters in both the high-side and low-side signal paths are identical and provide excellent delay matching (5ns typical).

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8.4 Device Functional Modes

The mode of operation for the TPS7H6101 is determined by the state of the DHL and DLH pins. The configuration of these pins cannot be changed during device operation. There are two different operational modes: PWM and independent input mode. In PWM mode, the EN_HI pin is used to enable the device and a single PWM input signal is required on PWM_LI and the internal gate driver generates the complementary output signals for the low side and high side. Since the primary application of this mode is a synchronous buck converter, the high side switch generates the main output and low side switch performs the synchronous rectification. Resistors are connected from DHL to GND and DLH to GND to program the dead time between the high-side and low-side outputs. For acceptable resistor values to use in PWM mode, refer to the Dead Time detailed description section.

In independent input mode (IIM), separate PWM input signals are required on PWM_LI and EN_HI. The corresponding outputs of the TPS7H6101 are driven directly from these inputs. In IIM with interlock disabled, DLH is tied to BP5L and DHL has a resistor connected to GND. For operation in IIM with interlock enabled, connect a resistor between DLH and GND while connecting DHL to BP5L. For both operating mode options in IIM, resistors used must be valued between 100kΩ and 220kΩ.

Table 8-1 shows the configuration for each operating mode. Note that these are the only valid operating modes for the driver, and the connections for DLH and DHL must adhere to one of these configurations for proper operation.

Table 8-1. TPS7H6101 Operating Mode Selection

Operating Mode	DLH	DHL
PWM	Resistor to GND	Resistor to GND
Independent input mode - input interlock disabled	BP5L	Resistor to GND (100kΩ to 220kΩ)
Independent input mode - input interlock enabled	Resistor to GND (100kΩ to 220kΩ)	BP5L

TPS7H6101-SEP Truth Table shows the truth table for each functional mode of the TPS7H6101-SP.

Table 8-2. TPS7H6101-SEP Truth Table

Inputs		PWM Mode		IIM - Interlock Disabled		IIM - Interlock Enabled	
EN_HI	PWM_LI	HS Gate	LS Gate	HS Gate	LS Gate	HS Gate	LS Gate
0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	1
1	0	0	1	1	0	1	0
1	1	1	0	1	1	0	0

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H6101 is a rad-tolerant GaN FET half bridge power stage with electrically isolated high side and low side gate drive and GaN FETs. A typical application example shows the TPS7H6101 as a step down converter taking a 100V main bus to a 28V rail with 10A output current; the following example is an open-loop example, however a closed loop implementation can be achieved with the addition of a PWM controller shuch as the TPS7H5005-SEP.

9.2 Typical Application

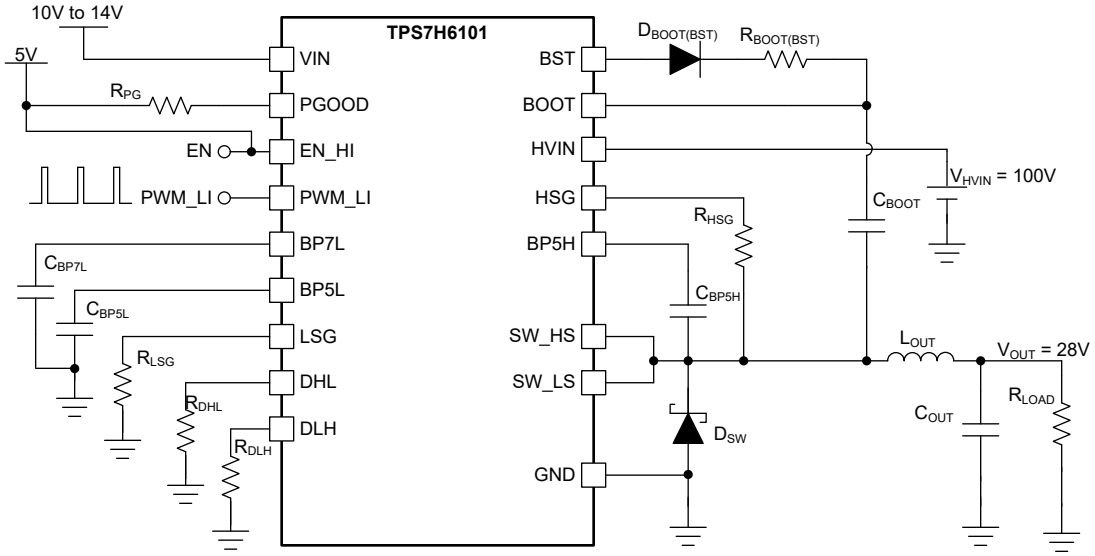

Figure 9-1. 100V to 28V 10A Satellite Bus Application

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9.2.1 Design Requirements

Table 9-1. Electrical Performance Specifications

DESIGN PARAMETER	DESIGN VALUE
INPUT CHARACTERISTICS	
Input Voltage, V_{IN}	100V
OUTPUT CHARACTERISTICS	
Output voltage, V_{OUT}	28V
Output current, I_{OUT}	10A
SYSTEM CHARACTERISTICS	
Switching Frequency, F_{SW}	100kHz
Full-load efficiency, η_{FL_28} (V_O = 28V,V_{IN} = 100V, I_O = 10A)	90%

9.2.2 Detailed Design Procedure

A 100V to 28V satellite bus is depicted in Figure 9-1; the following design procedure provides guidance for bootstrap diode selection, dead time resistor selection and the utilization of pull down resistor on LSG and HSG pins.

9.2.2.1 Bootstrap and Bypass Capacitor

The external bootstrap capacitor needs to maintain operation above the BOOT UVLO falling threshold during normal operation. As a best design practice, size the capacitor to allow for substantial margin this threshold. The first step in determining the bootstrap capacitor value is calculating for ΔV_{BOOT}. This is the maximum allowable drop on the bootstrap capacitor:

$$\Delta V_{BOOT} \approx VIN - (n \times V_F) - V_{BOOT\_UVLO} = 12V - (1 \times 0.9V) - 6.65V = 4.35V \quad (10)$$

where:

- n is the number of bootstrap diodes used in series
- V_F is the voltage drop of the bootstrap diode chosen
- V_{BOOT_UVLO} is the BOOT UVLO falling threshold voltage

To maintain significant margin and account for any additional voltage drop across the bootstrap resistor used and also for load transients, the capacitor is calculated for ΔV_{BOOT} of 1.5V. Referring to the Bootstrap Capacitor section, the value of Q_{total} needs to first be determined, and then C_{BOOT} can subsequently be calculated:

$$Q_{total} = Q_g + I_{QBG} \times \frac{D_{MAX}}{f_{SW}} + \frac{I_{QHS}}{f_{SW}} = 5nC + 50\mu A \times \frac{0.28}{100kHz} + \frac{5mA}{100kHz} = 55nC \quad (11)$$

$$C_{BOOT} \geq \frac{Q_{total}}{\Delta V_{BOOT}} = \frac{55nC}{1.5V} = 36.7nF \quad (12)$$

A minimum value of 36.7nF is needed for the design. However, given the potential for capacitance changes with temperature and applied voltage, as well as unexpected circuit behavior such as load transients that impact the bootstrap charging time, a 100nF X7R capacitor is selected.

The VIN capacitor selected must be larger than the bootstrap capacitor. The general recommendation is that this capacitor is at least ten times the bootstrap capacitor value, which gives 1µF capacitor in this instance. For the evaluation setup, three 3.3µF and nine 100µF capacitors were used at VIN, both ceramic X7R type capacitors. The recommendation is to place these capacitors and the bootstrap capacitors as close the respective pins as possible. Select capacitors with voltage ratings that are sufficiently larger than the maximum applied voltage (i.e. greater than two times if possible).

Lastly, as detailed in Linear Regulator Operation section, select high-quality 1µF X7R ceramic capacitors for use at BP5H, BP5L, and BP7L outputs. Place these capacitors in close proximity to the respective pins.

ADVANCE INFORMATION

9.2.2.2 Bootstrap Diode

The bootstrap diode needs to have sufficient voltage rating to block the power stage input voltage of the power converter for the synchronous buck application. Depending on the type of diode selected, series diodes are required if the power stage input voltage is high. As mentioned in Bootstrap Diode detailed description, the diode also needs to be able to handle the peak current during the gate driver startup, and exhibit a low forward voltage drop, low junction capacitance, and fast recovery time. For high frequency applications, consider using a Schottky diode. A 150V, 5A rated Schottky diode with 100pF junction capacitance is selected for the evaluation setup. Note that the diode selected for use in the evaluation is for laboratory testing only, and TI recommends selection of a diode that meets all of the system performance and radiation needs.

9.2.3 Application Results

100V to 28V Efficiency plot shows the resulting efficiency performance of the TPS7H6101 with switching frequencies of 100kHz and 500kHz; both configurations show efficiencies greater than 95%.

Figure 9-2 is shown below from the TPS7H6101EVM; a sharp transintion with a 20V overshoot is well within the recommended operating condition of the TPS7H6101.

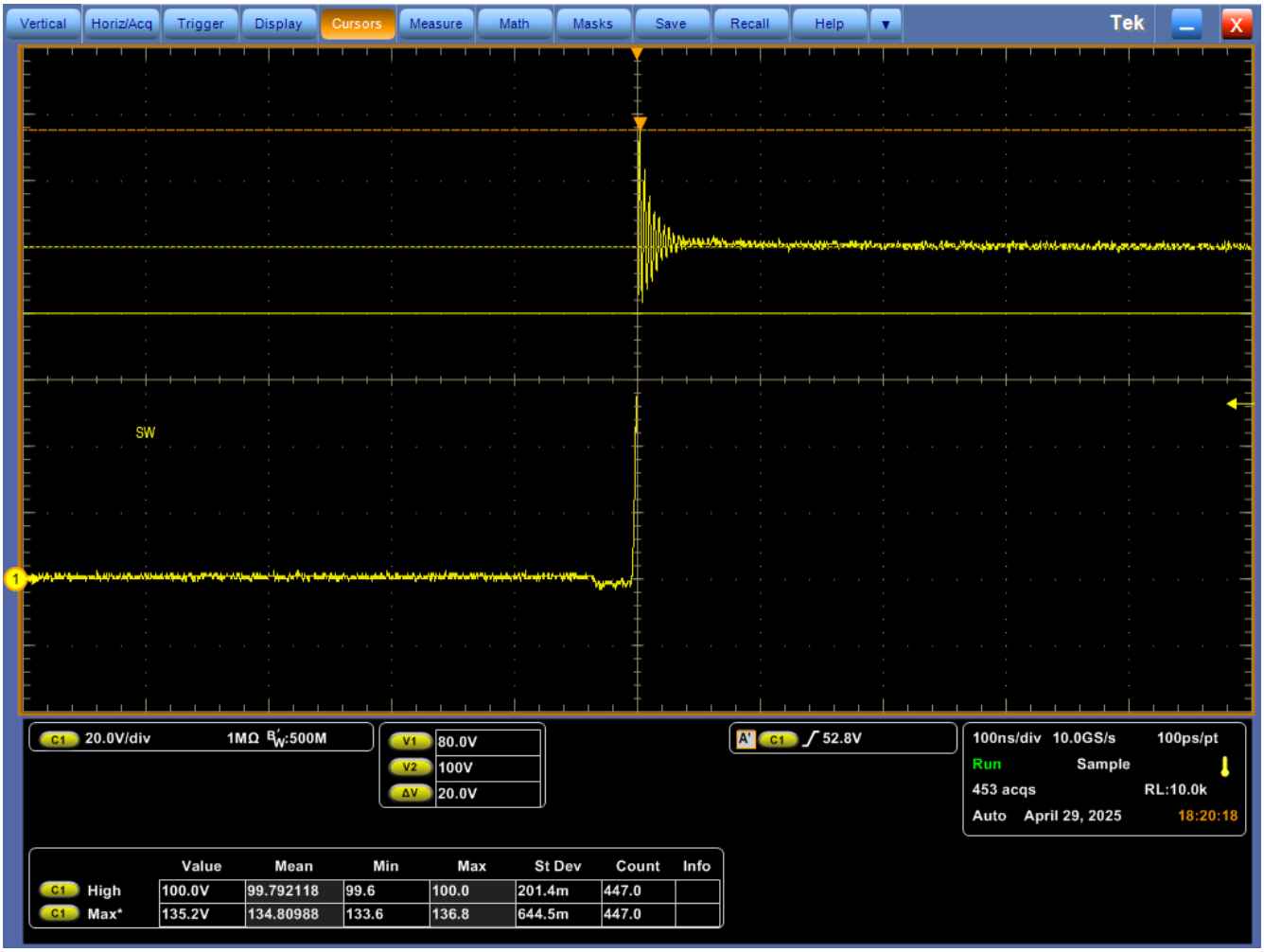

Figure 9-2. Switch Node Rising Transition

ADVANCE INFORMATION

9.3 Power Supply Recommendations

The recommended bias supply voltage range for TPS7H6101 is from 10V to 14V. The TPS7H6101 is designed for use with a well regulated input voltage. The BOOT voltage which supplies the high-side driver is required to be between 8V to 14V. Minimizing the voltage drop along the bootstrap charging path is essential to prevent the high-side driver from inadvertently entering into undervoltage lockout at any time during normal operation.

A local bypass capacitor must be placed between the VIN and GND pins. Place the bootstrap capacitor in as close proximity to the device as permissible. TI recommends a low-ESR, low-ESL, ceramic, surface-mount capacitors (X7R or better) for the connections at VIN and BOOT.

9.4 Layout

9.4.1 Layout Guidelines

To maximize the efficiency benefits of fast switching, optimize the board layout such that the power loop impedance is minimal. When using a multilayer board (more than 2 layers), power loop parasitic impedance is minimized by having the return path to the input capacitor (between VIN and GND), small and directly underneath the first layer. Refer to TPS7H6101EVM for an actual layout of these recommendations.

9.4.2 Layout Example

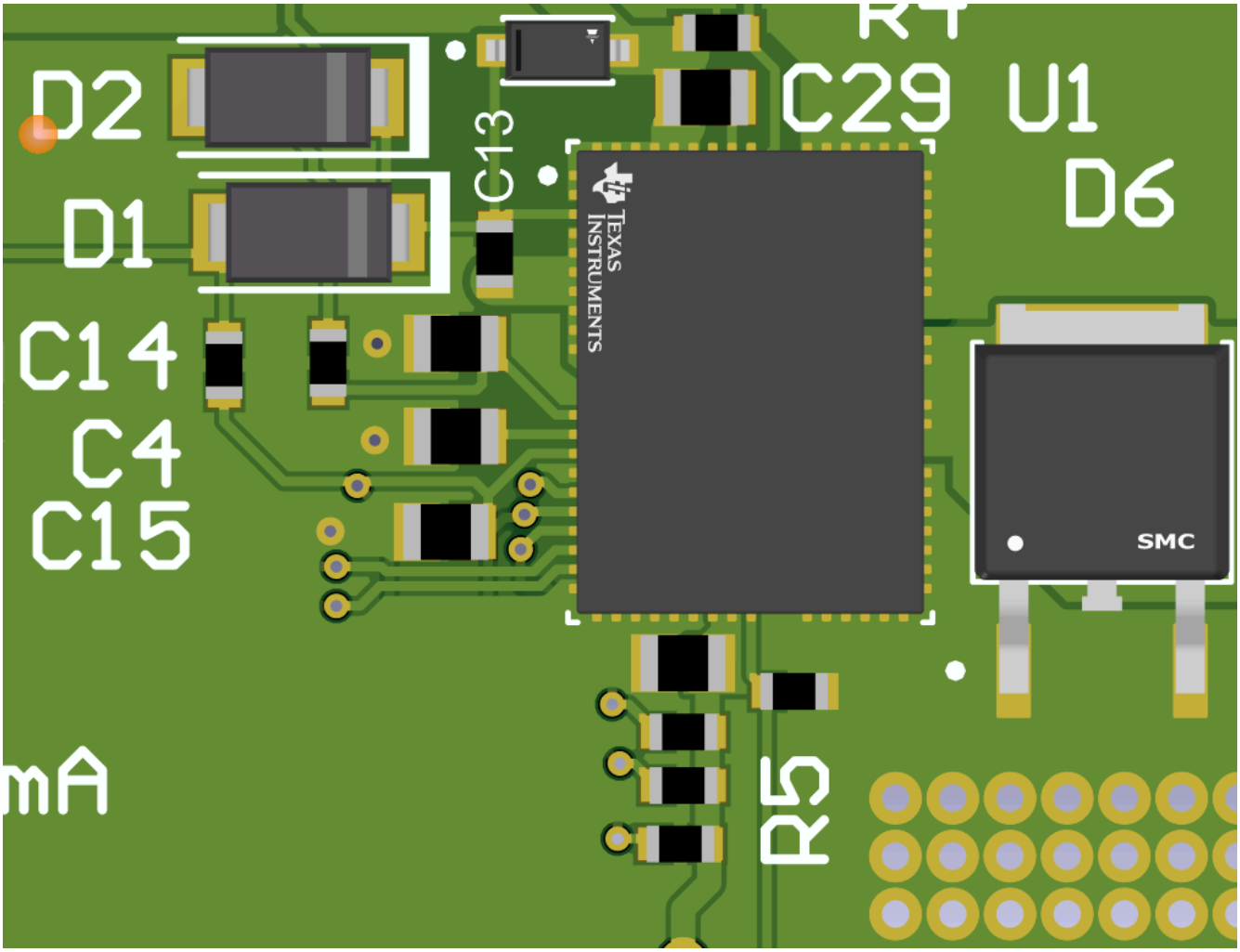

Figure 9-3. 3D View From TPS7H6101EVM

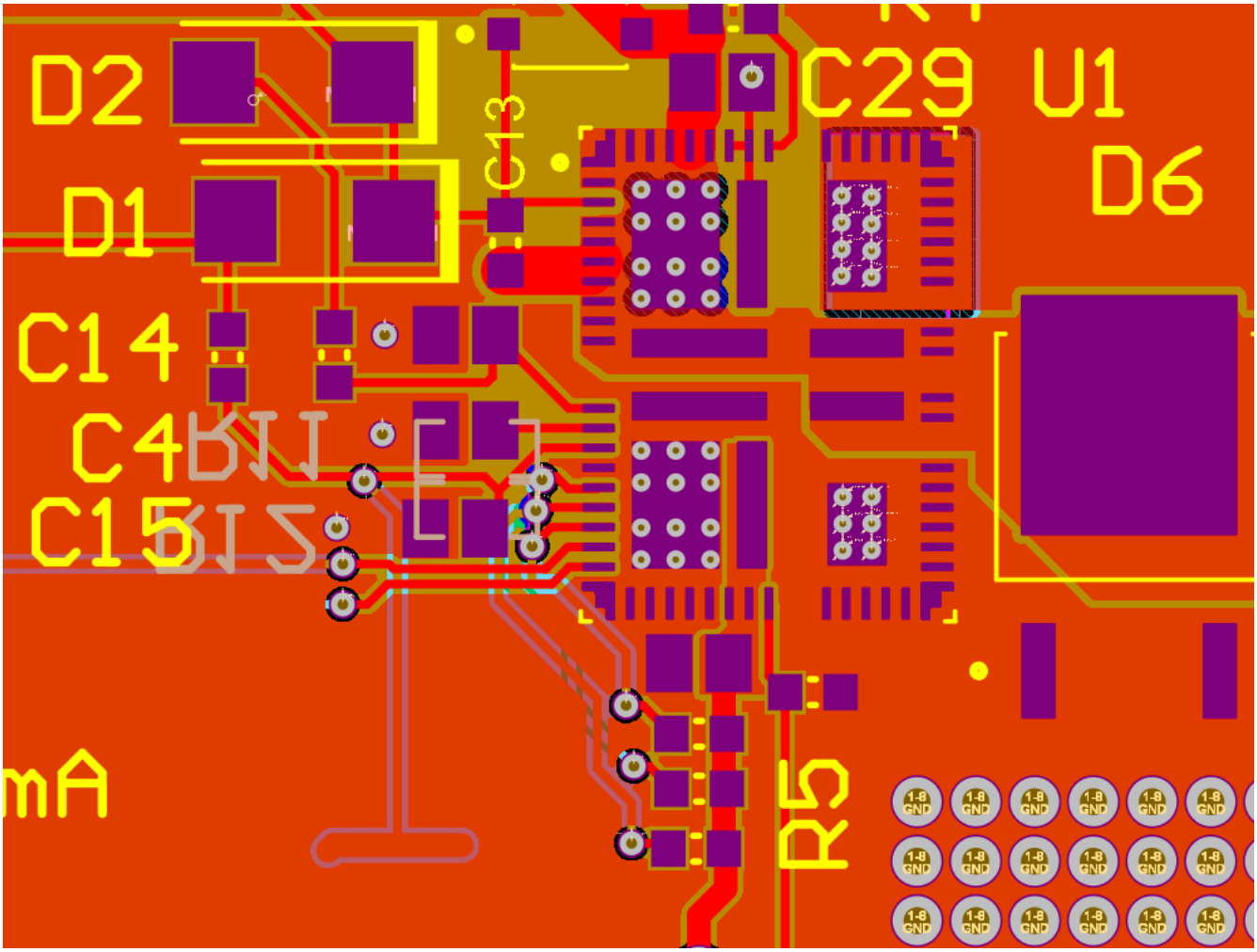

Figure 9-4. Layout Example From TPS7H6101EVM

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

- TPS7H6101EVM Evaluation Module and user's guide
- TPS7H6101-SEP Total Ionizing Dose (TID) report
- TPS7H6005-SEP Total Ionizing Dose (TID) Report
- TPS7H6005-SEP, TPS7H6015-SEP and TPS7H6025-SEP Neutron Displacement Damage (NDD) Characterization Report
- TPS7H60X5-SEP Single-Event Effects (SEE) Report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

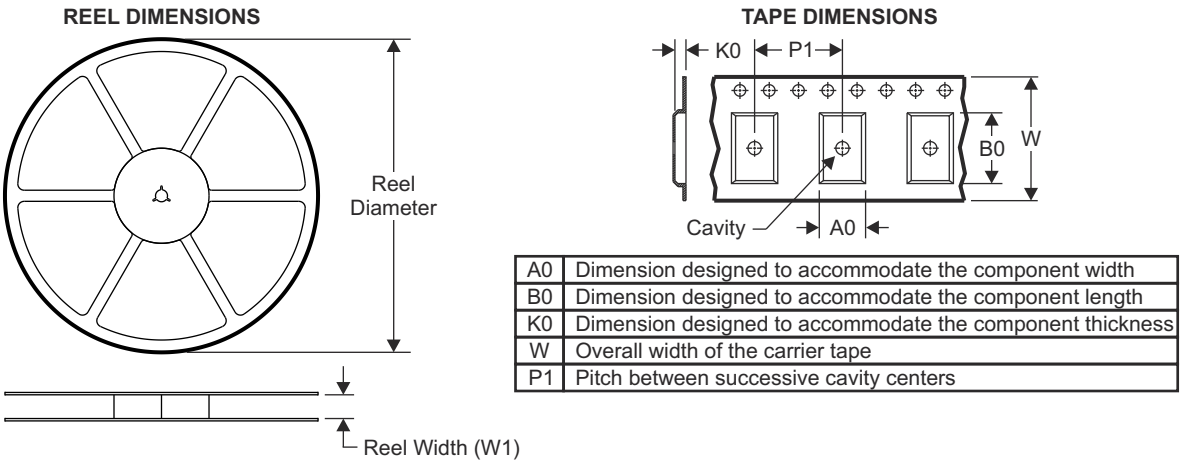
ADVANCE INFORMATION

ADVANCE INFORMATION

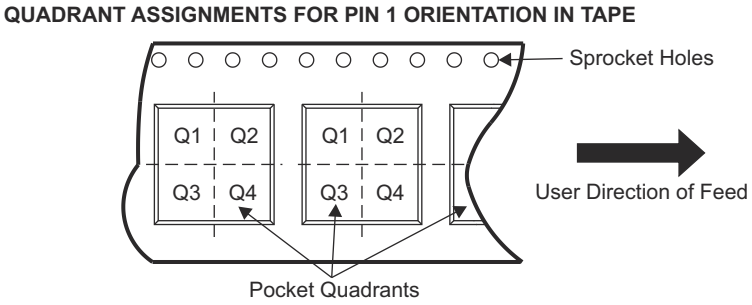
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

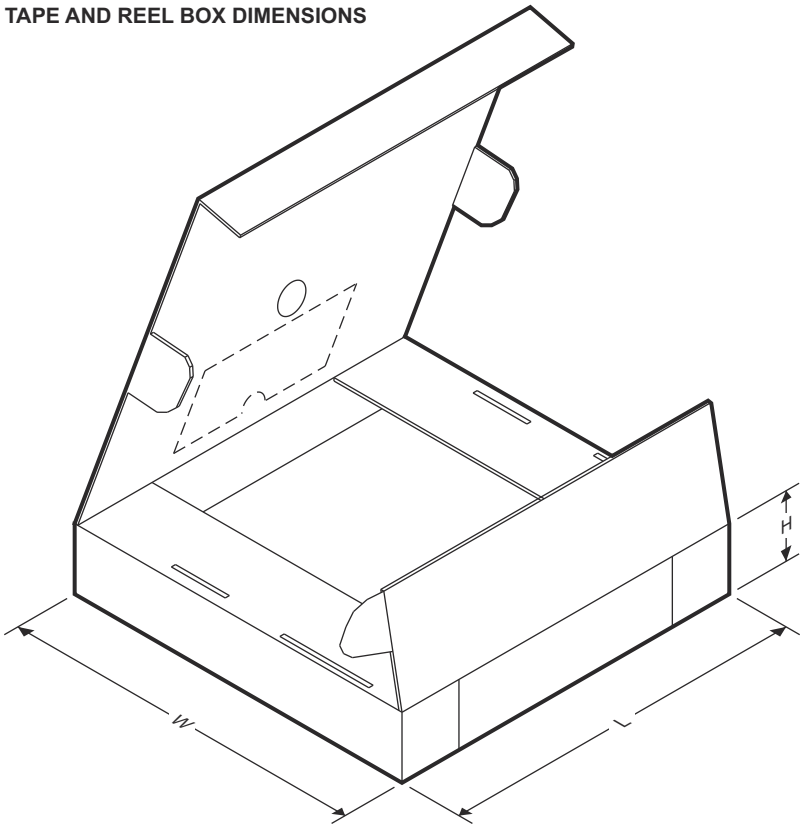


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7H6101MNPRNSEPQ1	LGA	NPR	64	250	178.0	24.4	9.4	12.9	1.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7H6101MNPRNSEPQ1	LGA	NPR	64	250	213.0	191.0	55.0

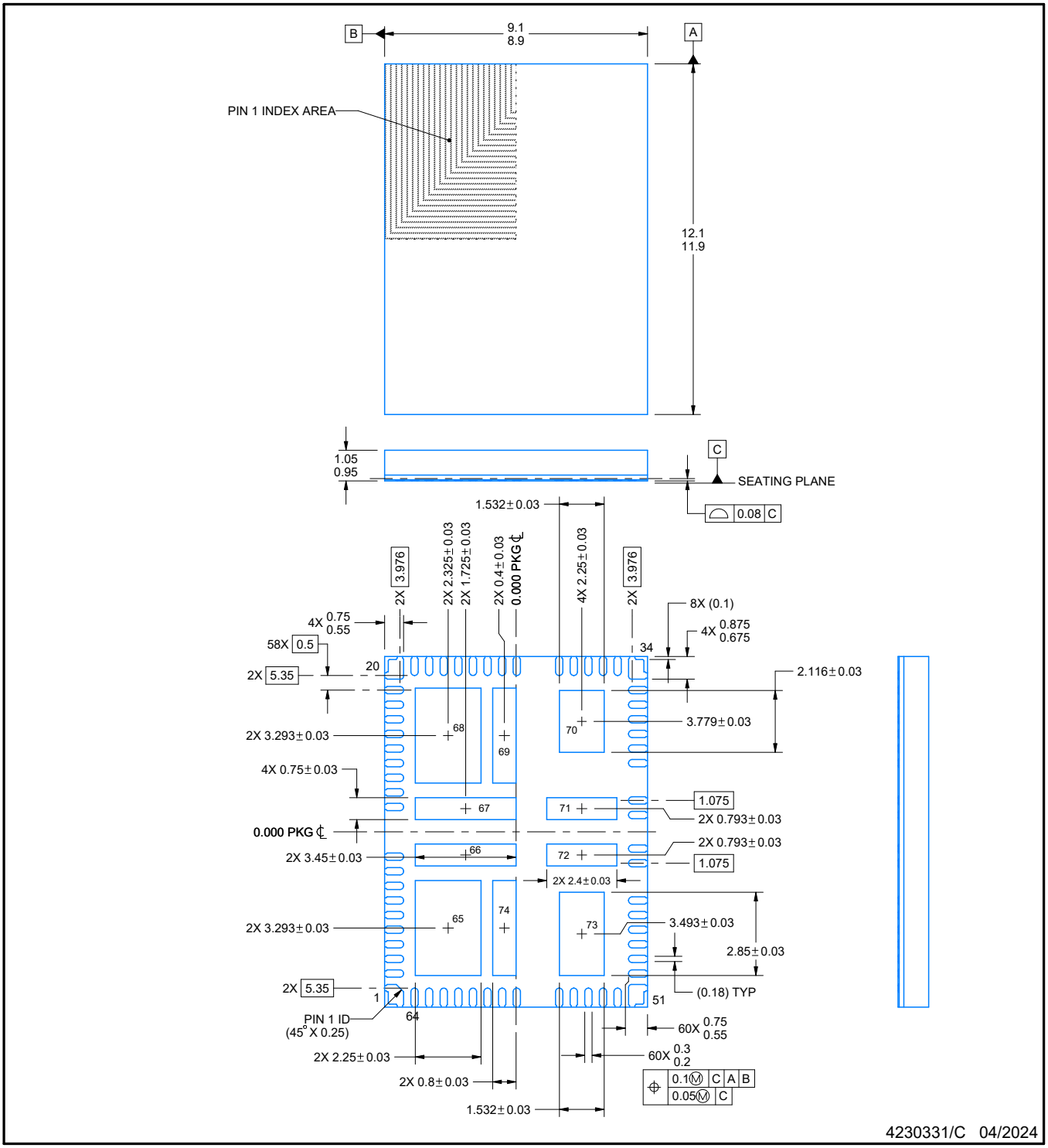
ADVANCE INFORMATION

PACKAGE OUTLINE

NPR0064A

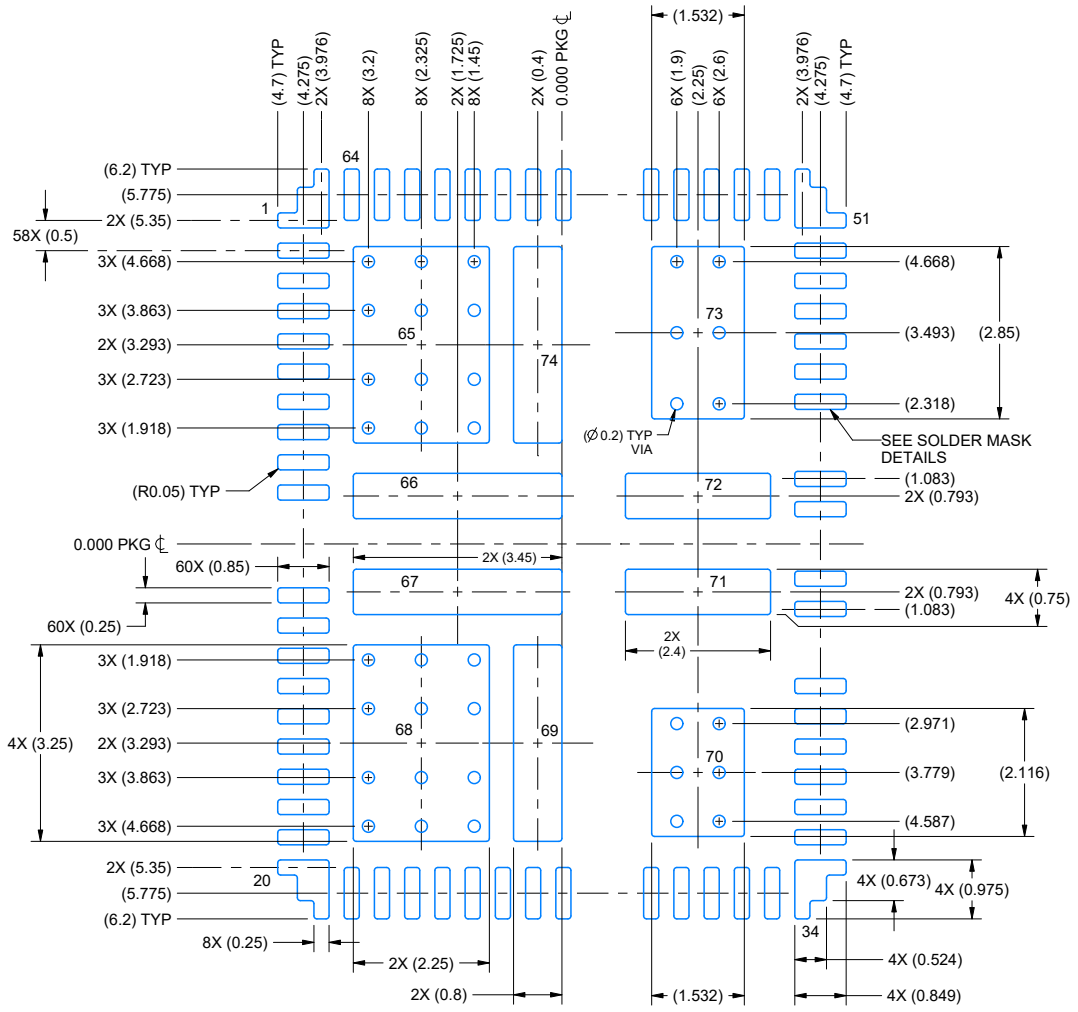
LGA - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

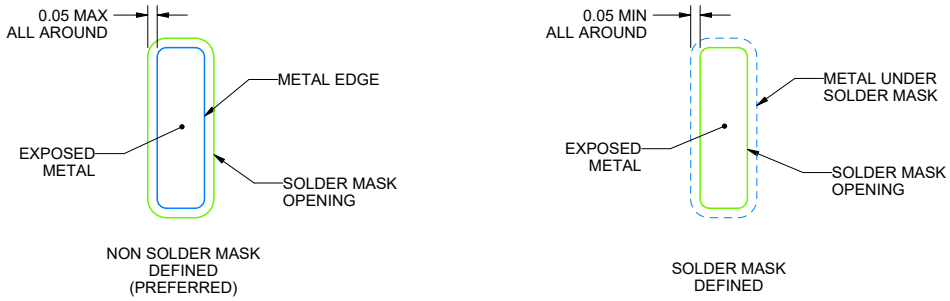


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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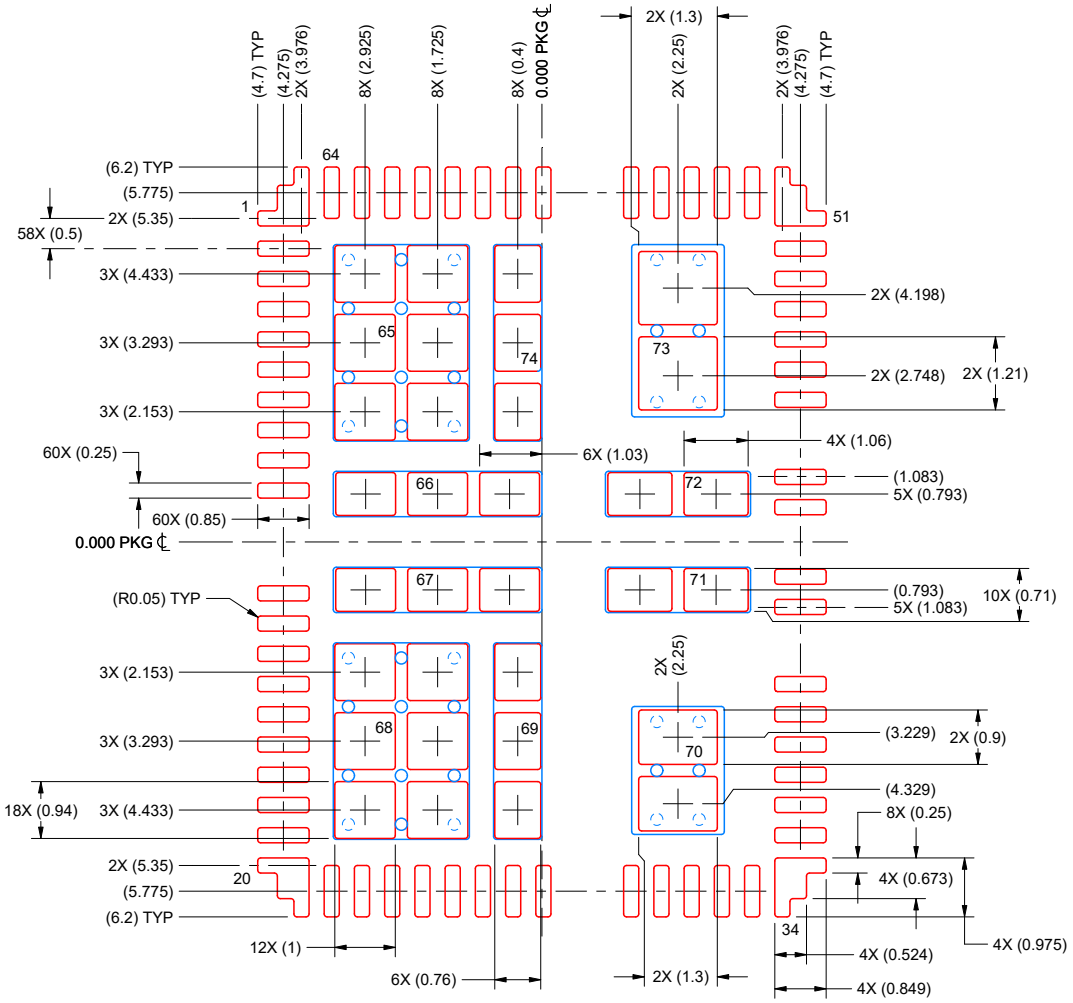
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 65 & 68: 77%
PADS 66 & 67: 85%
PADS 69 & 74: 82%
PADS 70 & 73: 72%
PADS 71 & 72: 84%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7H6101MNPRNSEP	Active	Preproduction	LGA (NPR) | 64	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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