TPS7H401x-SP and TPS7H401x-SEP 4.5V to 14V Input, 3A and 6A, Radiation Hardened Synchronous Buck Converter

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1 Features

- Total ionizing dose (TID) characterized
  - Radiation hardness assurance (RHA) availability of up to 100krad(Si)
- Single-Event Effects (SEE) characterized
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 75MeV-cm^2/mg
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 75MeV-cm^2/mg
- Input voltage range from 4.5V to 14V
- 6A (TPS7H4012) or 3A (TPS7H4013) maximum output current
- High efficiency (typical values for VIN = 12V, VOUT = 3.3V, f_{SW} = 500kHz)
  - 88% at 1A
  - 92% at 3A
  - 91% at 6A
- Integrated 33mΩ (HS) and 27mΩ (LS) MOSFETs (typ at 12V)
- Flexible switching frequency options:
  - 100kHz to 1MHz, accurate (±15% or better), adjustable internal oscillator
  - 100kHz to 1MHz external sync capability
- 0.6V ± 0.83% voltage reference over line, temperature, and radiation
- Supports start-up into prebiased outputs
- Adjustable slope compensation and soft-start
- Adjustable input enable and power-good output for power sequencing
- Power-good output monitor for undervoltage and overvoltage
- Supports inverting buck-boost topology
- Plastic packages outgas tested per ASTM E595
- Available in military (–55°C to 125°C) temperature range

2 Applications

- Space satellite point of load supply
- Satellite electrical power systems (EPS)
- Communications payload
- Radar imaging payload
- Radiation hardened power supplies

3 Description

The TPS7H401x devices are 14V synchronous buck converters optimized for use in a space environment. The TPS7H4012 is a 6A device and the TPS7H4013 is a 3A device. The peak current mode converter obtains high efficiency with good transient performance and reduced component count.

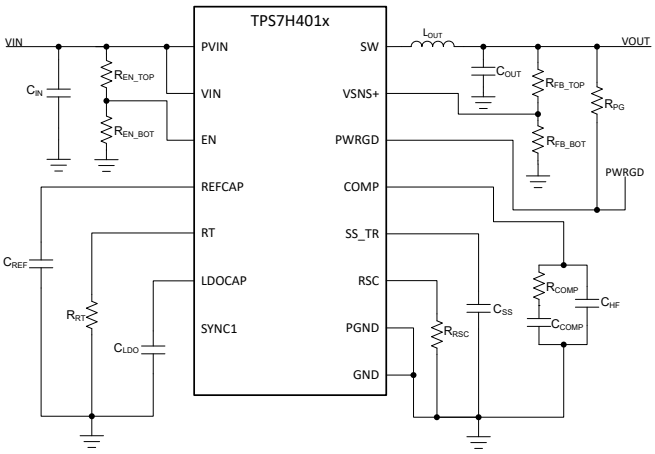
The wide voltage range of the TPS7H401x enables it to be used as a point of load regulator to convert directly from a 12V or 5V rail. The output voltage start-up ramp is controlled by the SS_TR pin. Power sequencing is possible with the EN and PWRGD pins.

Additionally, various features are included such as an optimized current limit for each device, a flexible switching frequency, and configurable compensation.

Device Information

PART NUMBER(1)	GRADE	PACKAGE(2)
5962R2122105VZC(3)	QMLV-RHA	20-pin ceramic 7.84mm × 12.93mm Mass = TBD
5962R2122106VZC(3)		
TPS7H4012HLC/EM(3)	Engineering sample	
TPS7H4013HLC/EM(3)		
5962R2122103PYE(3)	QMLP-RHA	44-pin plastic 6.10mm × 14.00mm Mass = 218mg
5962R2122104PYE(3)		
TPS7H4012MDDWTSEP	SEP	
TPS7H4013MDDWTSEP		

(1) For additional information view the Device Options Table.
(2) Dimension and mass values are nominal.
(3) Product preview.



Simplified Schematic

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4 Device Comparison Table

MAXIMUM OUTPUT CURRENT	DEVICE	RADIATION	DIFFERENTIAL REMOTE SENSE	FLEXIBLE SYNCHRONIZATION	SELECTABLE CURRENT LIMIT	FAULT INPUT PIN
12A	TPS7H4011-SP	Rad-hard	Yes	Yes	Yes	Yes
	TPS7H4011-SEP	Rad-tolerant				
6A	TPS7H4012-SP	Rad-hard	No	No	No	No
	TPS7H4012-SEP	Rad-tolerant				
3A	TPS7H4013-SP	Rad-hard	No	No	No	No
	TPS7H4013-SEP	Rad-tolerant				

5 Device Options Table

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H4012-SP	TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLV-RHA	20-pin CFP HLC	5962R2122105VZC(4)
		QMLP-RHA	44-pin HTSSOP DDW	5962R2122103PYE(4)
	None	Engineering model(3)	20-pin CFP HLC	TPS7H4012HLC/EM(4)
TPS7H4012-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV-cm^2/mg	Space Enhanced Plastic	44-pin HTSSOP DDW	TPS7H4012MDDWTSEP
TPS7H4013-SP	TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLV-RHA	20-pin CFP HLC	5962R2122106VZC(4)
		QMLP-RHA	44-pin HTSSOP DDW	5962R2122104PYE(4)
	None	Engineering model(3)	20-pin CFP HLC	TPS7H4013HLC/EM(4)
TPS7H4013-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV-cm^2/mg	Space Enhanced Plastic	44-pin HTSSOP DDW	TPS7H4013MDDWTSEP
SN0020HLC	N/A	Mechanical "dummy" package (no die)	20-pin CFP HLC	SN0020HLC

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view SLYB235.
(3) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.
(4) Product preview.

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6 Pin Configuration and Functions

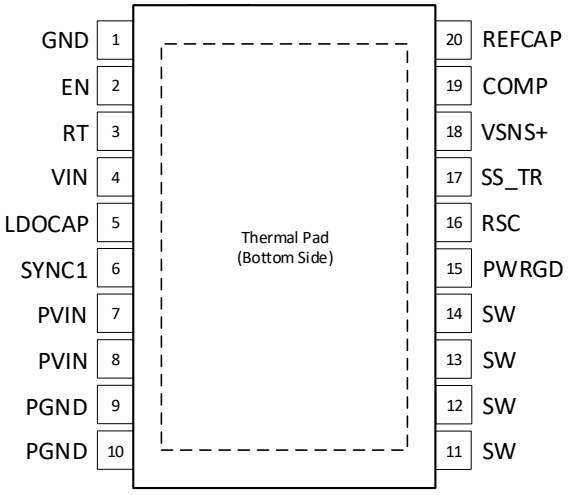

Figure 6-1. HLC Package, 20-Pin CFP (Top View)

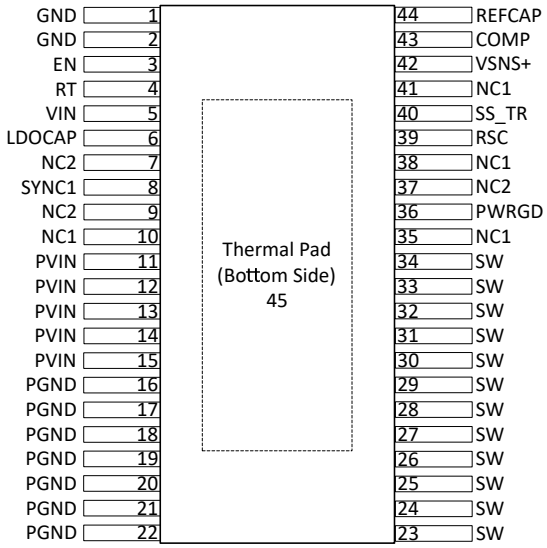

Figure 6-2. DDW Package, 44-Pin HTSSOP (Top View)

Table 6-1. Pin Functions

PIN			I/O[1]	DESCRIPTION
NAME	CFP (20)	HTSSOP (44)		
GND	1	1, 2	—	Ground. Return for control circuitry.
EN	2	3	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. A resistor divider from VIN to GND may be used to set the device turn-on level.
RT	3	4	I/O	A resistor connected between RT and GND sets the switching frequency of the converter. The switching frequency range is 100kHz to 1MHz. If the device is configured to utilize an external clock, this pin may be left floating or a resistor may be used to provide a backup frequency if the external clock is lost.
VIN	4	5	I	Input voltage. Power for the control circuitry of the switching regulator. It must be the same voltage as PVIN and is therefore recommended to externally connect VIN to PVIN.
LDOCAP	5	6	O	Linear regulator output capacitor pin. A 1µF capacitor must be placed on this pin for the internal linear regulator. The output voltage, AVDD, is nominally 5V. Do not load this pin with any additional external circuitry.
SYNC1	6	8	I	Synchronization pin 1. This pin is used as an input for an external clock. It will set the switching frequency 180° out of phase with SYNC1. If an external clock is not used, it is recommended to connect SYNC1 to GND to prevent noise coupling into the pin.
PVIN	7–8	11–15	I	Power stage input voltage. Power for the output stage of the switching regulator.
PGND	9–10	16–22	—	Power stage ground. Return for low-side power MOSFET. Connect to GND on the PCB.
SW	11–14	23–34	O	Switching node pins. Switch node output. A Schottky diode may be connected from SW to PGND for potential improvement in internal device noise and efficiency.
PWRGD	15	36	O	Power Good pin. This is an open-drain pin. Use a pull-up resistor to pull this pin up to VOUT (assuming VOUT is under 7V) or the desired logic level. PWRGD is asserted when the output voltage is within 5% (typ) of its programmed value. PWRGD is deasserted when the output voltages is outside 8% (typ) of its programmed value or when there is a fault condition (such as thermal shutdown).
RSC	16	39	I/O	Slope compensation pin. A resistor from RSC to GND sets the desired slope compensation.

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Table 6-1. Pin Functions (continued)

PIN			I/O[1]	DESCRIPTION
NAME	CFP (20)	HTSSOP (44)		
SS_TR	17	40	I/O	Soft-start and tracking. An external capacitor connected between this pin and VSNS- slows down the rise time of the internal reference. It can also be used for tracking and sequencing.
VSNS+	18	42	I	Positive voltage sense. This is the feedback pin that will be set to a nominal 0.6V by selecting the appropriate resistor divider network.
COMP	19	43	I/O	Compensation pin. This is the operational transconductance (OTA) error amplifier output and input to the switch current comparator. Connect frequency compensation to this pin.
REFCAP	20	44	O	Reference capacitor pin. A 470nF external capacitor is required for the internal bandgap reference. The voltage, V_{BG}, is nominally 1.2V. Do not connect external circuitry to this pin.
NC1	N/A	10, 35, 38,41	—	No connect 1. These pins are not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
NC2	N/A	7, 9, 37	—	No connect 2. These pins are internally connected. Do not externally connect these pins (they must be left electrically floating). They will internally be pulled to a voltage between GND and LDOCAP.
THERMAL PAD	21	45	—	Thermal pad internally connected to GND. Connect to a large ground plane for thermal dissipation. While it is recommended to electrically connect to GND or PGND; it may be left electrically disconnected if desired.
Metal lid	Lid	N/A	—	Internally connected to GND.

(1) I = Input, O = Output, I/O = Input or Output, — = Other

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN, PVIN	–0.3	16	V
	EN, PWRGD, SYNC1	–0.3	7.5	
	VSNS+	–0.3	3.6	
Output voltage	SW	–1	16	V
	SW, 80ns transient	–3	20	
	LDOCAP	–0.3	7.5	
	RSC, COMP, RT, SS_TR	–0.3	3.6	
	REFCAP	–0.3	1.9	
Vdiff	(GND to exposed thermal pad)	–0.2	0.2	V
Source current	SW		Current limit	A
	PVIN		Current limit	
	PGND		Current limit	
	RT	–100	100	µA
Sink current	SW		Current limit	A
	PGND		Current limit	
	COMP	–200	200	µA
	PWRGD	–0.1	5	mA
Operating junction temperature		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN, PVIN(1)	4.5		14	V
	EN, PWRGD	0		7	
	SYNC1(2)	0		5.3	
		0		VIN	
	VSNS+	0	0.6	1	
Output voltage	SW	0		14	V
	RSC, COMP, RT	0		3.3	
	SS_TR	0	0.6	1	
Output current	$SW_{(avg)}$, TPS7H4012	0		6	A
	$SW_{(avg)}$, TPS7H4013	0		3	A
	RT	–100		100	µA
Input current	COMP	–200		200	µA
	PWRGD	0		2	mA
Operating junction temperature	T_J	–55		125	°C

(1) VIN must be equal to PVIN and startup at the same time. Normally this is achieved by tying them to the same voltage rail.
(2) The SYNC1 maximum input voltage must be set to the lower of VIN and 5.3V.

7.4 Thermal Information

THERMAL METRIC(1)		TPS7H4012-SP TPS7H4013-SP	TPS7H4012-SP, -SEP TPS7H4013-SP, -SEP	UNIT
		CFP HLC	DDW (HTSSOP)	
		20 PINS	44 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.3	21.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	4.0	8.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.31	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.8	4.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.8	4.4	°C/W

(1) For more information about the traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).

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7.5 Electrical Characteristics

Over 4.5V ≤ VIN ≤ 14V, PVIN = VIN, open loop configuration, I_{OUT} = 0A, over operating temperature range (T_A = –55°C to 125°C), unless otherwise noted; includes RLAT at T_A = 25°C if sub-group number is present for QML RHA and SEP devices(1) Note the parts are advanced information and specifications are subject to change.

PARAMETER		TEST CONDITIONS		SUB-GROUP(2)	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
V_{UVLOR_PVIN}	PVIN internal UVLO rising threshold			1, 2, 3	3.2	3.4	3.6	V
$V_{UVLOHYST_PVIN}$	PVIN internal UVLO hysteresis			1, 2, 3	425	450	500	mV
V_{UVLOR_VIN}	VIN internal UVLO rising threshold			1, 2, 3	3.4	3.6	3.8	V
$V_{UVLOHYST_VIN}$	VIN internal UVLO hysteresis			1, 2, 3	140	155	170	mV
I_{SHDN_VIN}	VIN shutdown supply current	V_{EN} = 0V	VIN = 4.5V	1, 2, 3		2	2.9	mA
			VIN = 14V	1, 2, 3		2	3	
I_{SHDN_PVIN}	PVIN shutdown supply current	V_{EN} = 0V	PVIN = 4.5V	1, 2, 3		2.6	3.5	mA
			PVIN = 14V	1, 2, 3		3.5	4.7	
I_{Q_VIN}	VIN operating quiescent current (non switching)	V_{EN} = 7V, VSNS+ = 1V		1, 2, 3		2.6	5	mA
ENABLE								
$V_{EN(rising)}$	Enable rising threshold (turn-on)			1, 2, 3	0.555	0.61	0.655	V
$V_{EN(falling)}$	Enable falling threshold (turn-off)			1, 2, 3	0.455	0.51	0.554	
$t_{EN(delay)}$	Enable propogation delay	EN high to SW high, SS pin open		1, 2, 3		52	100	µs
$I_{EN(LKG)}$	Enable input leakage current	V_{EN} = 7V		1, 2, 3		2	100	nA
VOLTAGE REFERENCE AND SENSE								
V_{REF}	Internal voltage reference (including error amplifier V_{IO})	see (3)	T_A = –55°C	3	0.594	0.598	0.603	V
			T_A = 25°C	1	0.596	0.6	0.603	
			T_A = 125°C	2	0.597	0.6	0.604	
$V_{REF(internal)}$	Internal voltage reference (without error amplifier included)	$V_{REF(internal)}$ = V_{SS_TR}		1, 2, 3	0.593	0.6	0.606	V
V_{BG}	Bandgap voltage (voltage at the REFCAP pin)	C_{REFCAP} = 470nF		1, 2, 3	1.184	1.2	1.222	V
$I_{VSNS+(LKG)}$	VSNS+ input leakage current	VSNS+ = 0.6V		1, 2, 3		10	30	nA
ERROR AMPLIFIER								
V_{IO}	Error amplifier input offset voltage	VSNS+ = 0.6V		1, 2, 3	–2.9		2.9	mV
g_{mEA}	Error amplifier transconductance	–10µA < I_{COMP} < 10µA, V_{COMP} = 1V	T_A = –55°C	11	1400	2050	2700	µS
			T_A = 25°C	9	1200	1650	2100	
			T_A = 125°C	10	1000	1250	1500	
EA_{DC}	Error amplifier DC gain	VSNS+ = 0.6V				11500		V/V
EA_{ISRC}	Error amplifier source	V_{COMP} = 1V, 100mV input overdrive		1, 2, 3	90	125	200	µA
EA_{ISNK}	Error amplifier sink				90	125	200	
EA_{Ro}	Error amplifier output resistance					7		MΩ
EA_{BW}	Error amplifier bandwidth					9		MHz
g_{mps}	Power stage transconductance	V_{COMP} = 0.7V	TPS7H4012, HTSSOP	1, 2, 3	8	11.2	14.5	S
		V_{COMP} = 0.7V	TPS7H4012, CFP			11		
		V_{COMP} = 0.75V	TPS7H4013, HTSSOP	1, 2, 3	3.5	6.2	9.2	
		V_{COMP} = 0.75V	TPS7H4013, CFP			7.2		
OVERCURRENT PROTECTION								
I_{OC_HS1}	High-side switch current limit threshold 1(4)	R_{SHORT} = 100mΩ	TPS7H4012, HTSSOP	1, 2, 3		9.7	12.2	A
			TPS7H4012, CFP			9.5		
			TPS7H4013, HTSSOP	1, 2, 3		5.6	7.7	
			TPS7H4013, CFP			5.5		

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7.5 Electrical Characteristics (continued)

Over 4.5V ≤ VIN ≤ 14V, PVIN = VIN, open loop configuration, I_{OUT} = 0A, over operating temperature range (T_A = –55°C to 125°C), unless otherwise noted; includes RLAT at T_A = 25°C if sub-group number is present for QML RHA and SEP devices[1] Note the parts are advanced information and specifications are subject to change.

PARAMETER		TEST CONDITIONS		SUB-GROUP[2]	MIN	TYP	MAX	UNIT
I_{OC_HS2}	High-side switch current limit threshold 2	VIN = 12V, R_{SHORT} ≈ 4mΩ	TPS7H4012, HTSSOP	1, 2, 3		11.8		A
			TPS7H4012, CFP			11.5		
			TPS7H4013, HTSSOP	1, 2, 3		6.8		
			TPS7H4013, CFP			6.6		
$I_{OC_LS(sink)}$	Low-side switch sinking overcurrent threshold	T_A = –55°C		3	1.6	2.3	3.6	A
		T_A = 25°C		1	1.5	2.2	3.3	
		T_A = 125°C		2	1.4	2	2.8	
$COMP_{SHDN}$	COMP shutdown voltage			1, 2, 3	1.7	1.9	2.1	V
$t_{COMP(delay)}$	COMP shutdown delay					30		µs
SOFT START AND TRACKING								
t_{SS}	Soft start time	V_{SS_TR} from 10% to 90%, $V_{OUT(set)}$ = 3.3V	C_{SS} = 5.6nF	9, 10, 11		1.5		ms
			C_{SS} = 22nF	9, 10, 11	4.7	5.8	7.3	
			C_{SS} = 100nF	9, 10, 11		24.7		
$R_{SS(discharge)}$	Soft start discharge pull-down resistor			1, 2, 3	200	442	700	Ω
$SS_{startup}$	Maximum voltage on SS before startup[5]					20		mV
SLOPE COMPENSATION								
SC	Slope compensation, TPS74012	f_{SW} = 100kHz, VIN = 12V	R_{SC} = 499kΩ			–0.8		A/µs
			R_{SC} = 1.5MΩ			–0.3		
		f_{SW} = 500kHz, VIN = 12V	R_{SC} = 100kΩ			–4.4		
			R_{SC} = 499kΩ			–1.6		
			R_{SC} = 1.5MΩ			–1.2		
		f_{SW} = 1000kHz, VIN = 12V	R_{SC} = 100kΩ			–6.1		
			R_{SC} = 499kΩ			–3.2		
			R_{SC} = 1.5MΩ			–2.9		
SC	Slope compensation, TPS74013	f_{SW} = 100kHz, VIN = 12V	R_{SC} = 499kΩ			–0.6		A/µs
			R_{SC} = 1.5MΩ			–0.2		
		f_{SW} = 500kHz, VIN = 12V	R_{SC} = 100kΩ			–4.0		
			R_{SC} = 499kΩ			–1.4		
			R_{SC} = 1.5MΩ			–1.0		
		f_{SW} = 1000kHz, VIN = 12V	R_{SC} = 100kΩ			–5.5		
			R_{SC} = 499kΩ			–2.8		
			R_{SC} = 1.5MΩ			–2.1		
MINIMUM ON TIME AND DEAD TIME								
$t_{on(min)}$	Minimum on time	50% to 50% of VIN, I_{SW} = 2A	VIN = 4.5V	9, 10, 11		210	235	ns
			VIN = 5V	9, 10, 11		213	250	
			VIN = 12V	9, 10, 11		199	250	
			VIN = 14V	9, 10, 11		199	250	
$t_{off(min)}$	Minimum off time	I_{SW} = 2A				306		ns
t_{dead}	Dead time					70		ns

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7.5 Electrical Characteristics (continued)

Over 4.5V ≤ VIN ≤ 14V, PVIN = VIN, open loop configuration, I_{OUT} = 0A, over operating temperature range (T_A = –55°C to 125°C), unless otherwise noted; includes RLAT at T_A = 25°C if sub-group number is present for QML RHA and SEP devices(1) Note the parts are advanced information and specifications are subject to change.

PARAMETER		TEST CONDITIONS		SUB-GROUP(2)	MIN	TYP	MAX	UNIT
SWITCHING FREQUENCY AND SYNCHRONIZATION								
f_{SW}	RT programmed switching frequency	R_{RT} = 511kΩ		4, 5, 6	90	100	120	kHz
		R_{RT} = 90.9kΩ		4, 5, 6	450	500	550	
		R_{RT} = 40.2kΩ	VIN = 4.5V	4, 5, 6	850	1000	1150	
			5 ≤ VIN ≤ 14	4, 5, 6	870	1000	1170	
t_{SYNC_D}	SYNC1 to SW delay	SYNC1 input, see Figure 8-2	VIN = 4.5V	9, 10, 11	150	256	390	ns
			5V ≤ VIN ≤ 14V	9, 10, 11	140	240	300	
			VIN = 12V, IOUT = 12A			246		
$V_{SYNC1(IH)}$	SYNC1 input high threshold			1, 2, 3			1.7	V
$V_{SYNC1(IL)}$	SYNC1 input low threshold			1, 2, 3	0.7			
f_{SYNC}	SYNC1 input frequency range			4, 5, 6	100		1000	kHz
D_{SYNC}	SYNC1 input duty cycle range	External clock duty cycle		4, 5, 6	40%		60%	
$t_{CLK_E_I}$	External clock to internal clock detection time	RT populated		9, 10, 11		2	5	$(1/f_{sw})$ s
$t_{CLK_I_E}$	Internal clock to external clock detection time	RT populated		9, 10, 11		1	2	$(1/f_{sw})$ s
POWER GOOD AND THERMAL SHUTDOWN								
$PWRGD_{LOW_F\%}$	PWRGD falling threshold (fault), low	Threshold for PWRGD (VSNS+ as percent of V_{REF})	VSNS+ falling	1, 2, 3	90%	92%	95%	
$PWRGD_{LOW_R\%}$	PWRGD rising threshold (good), low		VSNS+ rising	1, 2, 3	93%	95%	98%	
$PWRGD_{HIGH_R\%}$	PWRGD rising threshold (fault), high		VSNS+ rising	1, 2, 3	106%	108%	112%	
$PWRGD_{HIGH_F\%}$	PWRGD falling threshold (good), high		VSNS+ falling	1, 2, 3	103%	105%	109%	
$I_{PWRGD(LKG)}$	Output high leakage	VSNS+ = V_{REF}, V_{PWRGD} = 7V		1, 2, 3		50	500	nA
$V_{PWRGD\ (OL)}$	Power good output low	$I_{PWRGD\ (SINK)}$ = 0mA to 2mA		1, 2, 3		250	300	mV
VIN_{MIN_PWRGD}	Minimum VIN for valid PWRGD output	Measured when V_{PWRGD} ≤ 0.5V at 100µA		1, 2, 3		1	2	V
$T_{SD(enter)}$	Thermal shutdown enter temperature					175		°C
$T_{SD(exit)}$	Thermal shutdown exit temperature					140		
$T_{SD(HYS)}$	Thermal shutdown hysteresis					35		
MOSFET								
$R_{DS_ON_HS}$	High-side switch resistance at I_{HS} = 6A, TPS7H4012, HTSSOP	PVIN = 4.5V	T_A = –55°C	3		29	42	mΩ
			T_A = 25°C	1		37	48	
			T_A = 125°C	2		47	63	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		26	38	
			T_A = 25°C	1		33	46	
			T_A = 125°C	2		41	56	
$R_{DS_ON_LS}$	Low-side switch resistance at I_{LS} = 6A, TPS7H4012, HTSSOP	PVIN = 4.5V	T_A = –55°C	3		20	31	mΩ
			T_A = 25°C	1		28	39	
			T_A = 125°C	2		41	50	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		20	29	
			T_A = 25°C	1		27	37	
			T_A = 125°C	2		39	48	

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7.5 Electrical Characteristics (continued)

Over 4.5V ≤ VIN ≤ 14V, PVIN = VIN, open loop configuration, I_{OUT} = 0A, over operating temperature range (T_A = –55°C to 125°C), unless otherwise noted; includes RLAT at T_A = 25°C if sub-group number is present for QML RHA and SEP devices(1) Note the parts are advanced information and specifications are subject to change.

PARAMETER		TEST CONDITIONS		SUB-GROUP(2)	MIN	TYP	MAX	UNIT
$R_{DS_ON_HS}$	High-side switch resistance at I_{HS} = 6A, TPS7H4012, CFP(6)	PVIN = 4.5V	T_A = –55°C	3		43	58	mΩ
			T_A = 25°C	1		55	66	
			T_A = 125°C	2		69	84	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		41	55	
			T_A = 25°C	1		53	65	
			T_A = 125°C	2		67	78	
$R_{DS_ON_LS}$	Low-side switch resistance at I_{LS} = 6A, TPS7H4012, CFP(6)	PVIN = 4.5V	T_A = –55°C	3		30	45	mΩ
			T_A = 25°C	1		40	56	
			T_A = 125°C	2		56	66	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		28	40	
			T_A = 25°C	1		38	50	
			T_A = 125°C	2		53	61	
$R_{DS_ON_HS}$	High-side switch resistance at I_{HS} = 3A, TPS7H4013, HTSSOP	PVIN = 4.5V	T_A = –55°C	3		28	41	mΩ
			T_A = 25°C	1		36	47	
			T_A = 125°C	2		46	62	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		26	38	
			T_A = 25°C	1		33	46	
			T_A = 125°C	2		41	56	
$R_{DS_ON_LS}$	Low-side switch resistance at I_{LS} = 3A, TPS7H4013, HTSSOP	PVIN = 4.5V	T_A = –55°C	3		20	31	mΩ
			T_A = 25°C	1		28	39	
			T_A = 125°C	2		41	50	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		20	29	
			T_A = 25°C	1		27	37	
			T_A = 125°C	2		39	48	
$R_{DS_ON_HS}$	High-side switch resistance at I_{HS} = 3A, TPS7H4013, CFP(6)	PVIN = 4.5V	T_A = –55°C	3		42	57	mΩ
			T_A = 25°C	1		54	65	
			T_A = 125°C	2		68	83	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		40	54	
			T_A = 25°C	1		52	64	
			T_A = 125°C	2		66	77	
$R_{DS_ON_LS}$	Low-side switch resistance at I_{LS} = 3A, TPS7H4013, CFP(6)	PVIN = 4.5V	T_A = –55°C	3		29	44	mΩ
			T_A = 25°C	1		39	55	
			T_A = 125°C	2		55	65	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		27	39	
			T_A = 25°C	1		37	49	
			T_A = 125°C	2		52	60	

(1) See the 5962R21221 SMD for additional information on the QML RHA devices and see the VID for additional information on the SEP devices.
(2) Subgroups are applicable for QML parts. For subgroup definitions, see the Quality Conformance Inspection table.
(3) Use this V_{REF} value to set the output voltage. Measured in a non-switching configuration as shown in Figure 8-1
(4) See Section 9.3.8.1.1 for additional information.
(5) The device will not begin startup until the voltage on SS discharges below $SS_{startup}$ in order to ensure proper soft start functionality.
(6) Measured at pins with lead length ≈ 3mm.

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7.6 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

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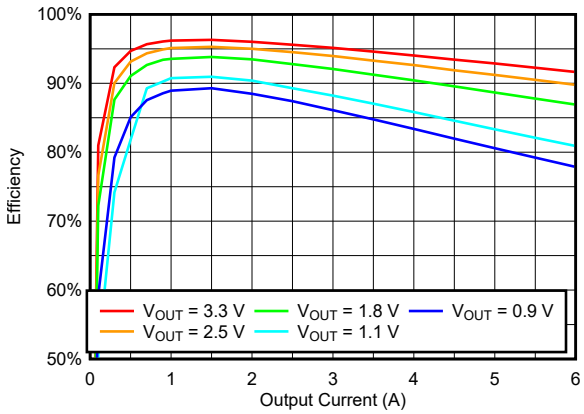
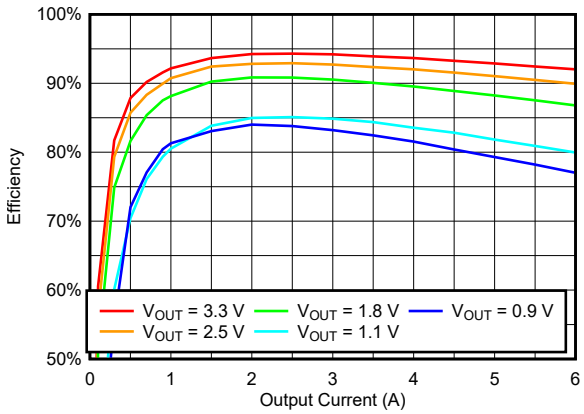
7.7 Typical Characteristics

TPS7H4012 44-pin HTSSOP (DDW) package, VIN = PVIN, VIN = 12V, C_{SS} = 22nF, Kemet MPXV1D2213L series inductor and SS10P4-M3/87A Schottky diode for efficiency tests, T_A = 25°C, unless otherwise noted.



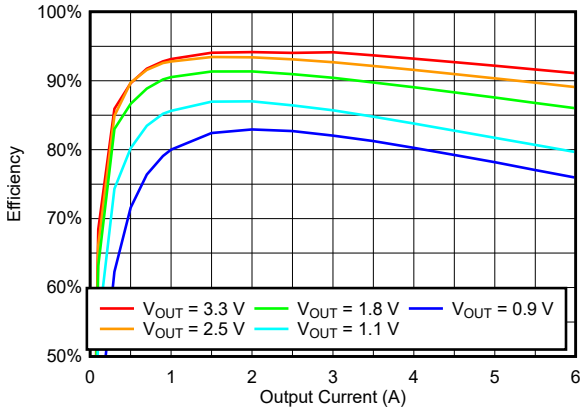
L_{OUT} = 15µH

Figure 7-1. Efficiency vs Load Across VOUT at VIN = 5V, 100kHz



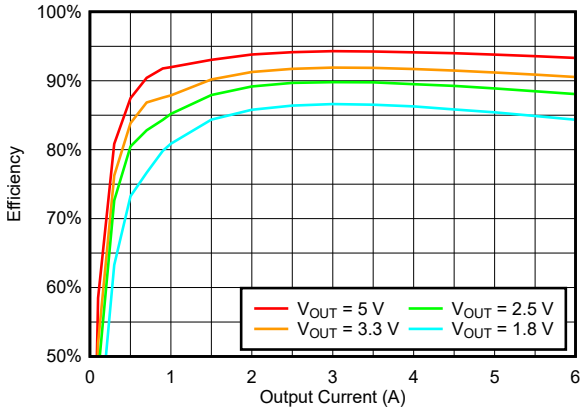
A. L_{OUT} = 15µH

Figure 7-2. Efficiency vs Load Across VOUT at VIN = 12V, 100kHz



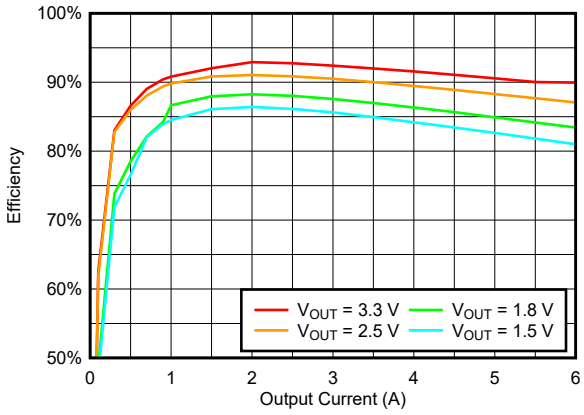
L_{OUT} = 2.2µH

Figure 7-3. Efficiency vs Load Across VOUT at VIN = 5V, 500kHz



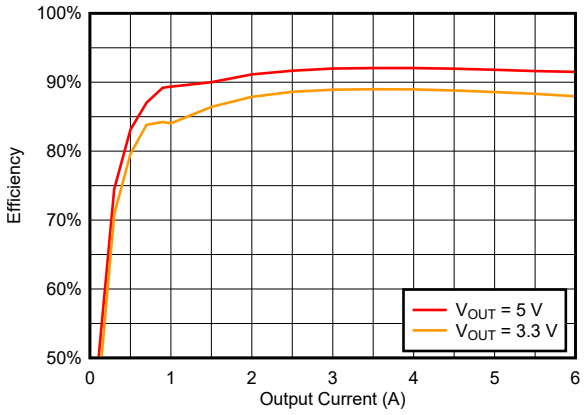
L_{OUT} = 2.2µH

Figure 7-4. Efficiency vs Load Across VOUT at VIN = 12V, 500kHz



L_{OUT} = 1µH

Figure 7-5. Efficiency vs Load Across VOUT at VIN = 5V, 1MHz



L_{OUT} = 1µH

Figure 7-6. Efficiency vs Load Across VOUT at VIN = 12V, 1MHz

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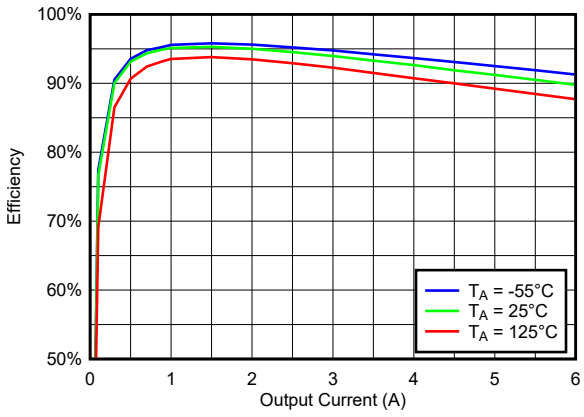
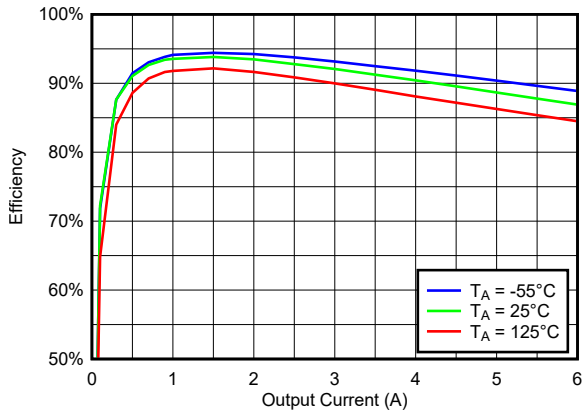
7.7 Typical Characteristics (continued)

TPS7H4012 44-pin HTSSOP (DDW) package, VIN = PVIN, VIN = 12V, C_{SS} = 22nF, Kemet MPXV1D2213L series inductor and SS10P4-M3/87A Schottky diode for efficiency tests, T_A = 25°C, unless otherwise noted.



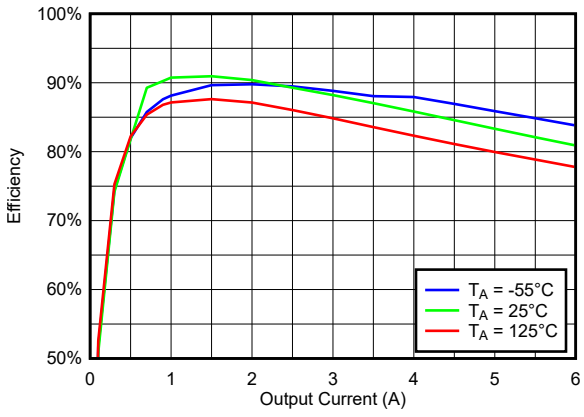
L_{OUT} = 15µH

Figure 7-7. Efficiency vs Load Across Temperature at 100kHz, VIN = 5V, VOUT = 2.5V



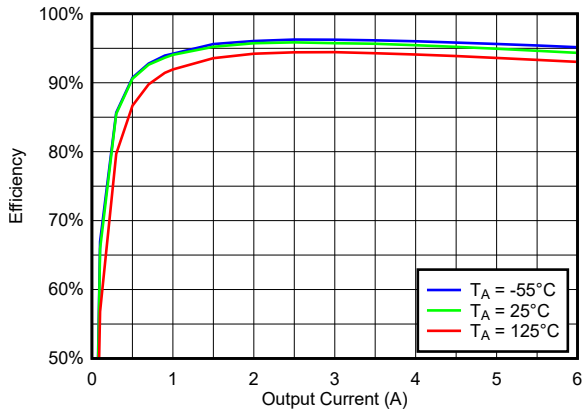
L_{OUT} = 15µH

Figure 7-8. Efficiency vs Load Across Temperature at 100kHz, VIN = 5V, VOUT = 1.8V



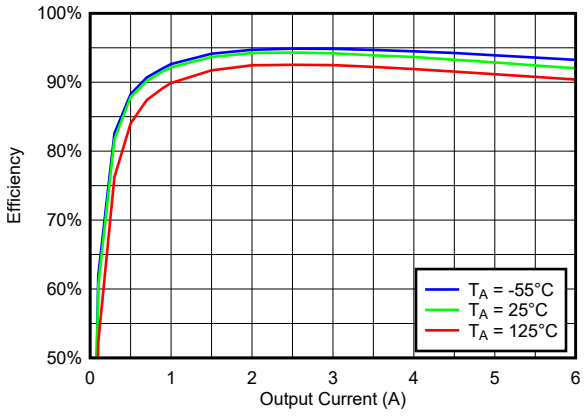
L_{OUT} = 15µH

Figure 7-9. Efficiency vs Load Across Temperature at 100kHz, VIN = 5V, VOUT = 1.1V



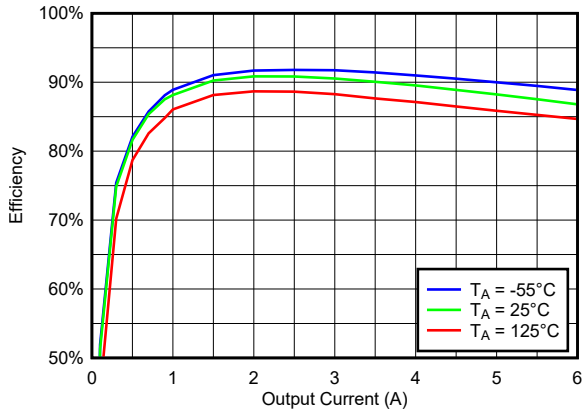
L_{OUT} = 15µH

Figure 7-10. Efficiency vs Load Across Temperature at 100kHz, VIN = 12V, VOUT = 5V



L_{OUT} = 15µH

Figure 7-11. Efficiency vs Load Across Temperature at 100kHz, VIN = 12V, VOUT = 3.3V



L_{OUT} = 15µH

Figure 7-12. Efficiency vs Load Across Temperature at 100kHz, VIN = 12V, VOUT = 1.8V

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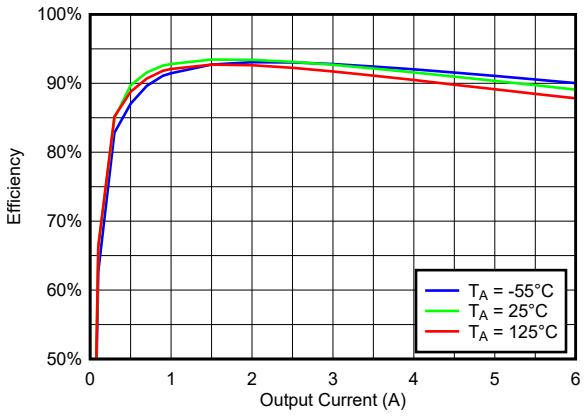
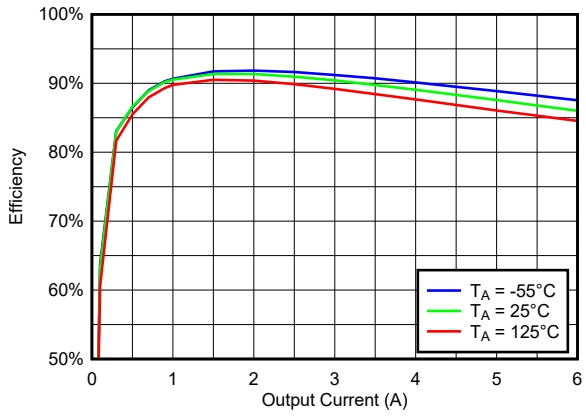
7.7 Typical Characteristics (continued)

TPS7H4012 44-pin HTSSOP (DDW) package, VIN = PVIN, VIN = 12V, C_{SS} = 22nF, Kemet MPXV1D2213L series inductor and SS10P4-M3/87A Schottky diode for efficiency tests, T_A = 25°C, unless otherwise noted.



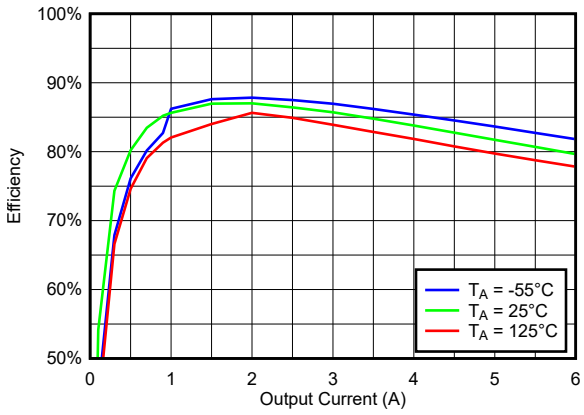
L_{OUT} = 2.2µH

Figure 7-13. Efficiency vs Load Across Temperature at 500kHz, VIN = 5V, VOUT = 2.5V



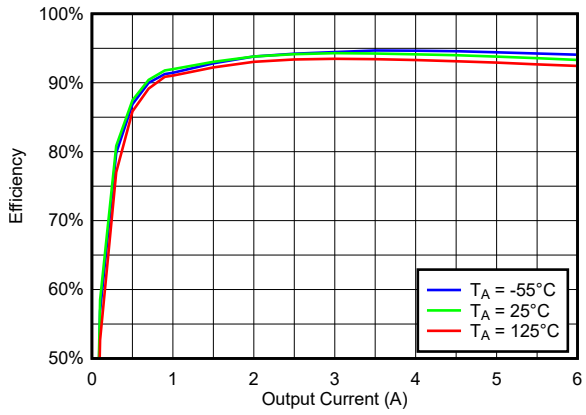
L_{OUT} = 2.2µH

Figure 7-14. Efficiency vs Load Across Temperature at 500kHz, VIN = 5V, VOUT = 1.8V



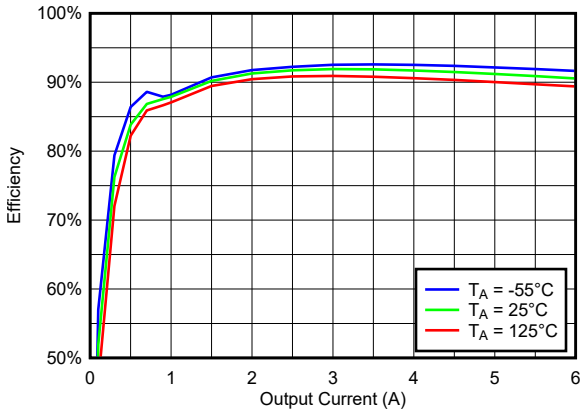
L_{OUT} = 2.2µH

Figure 7-15. Efficiency vs Load Across Temperature at 500kHz, VIN = 5V, VOUT = 1.1V



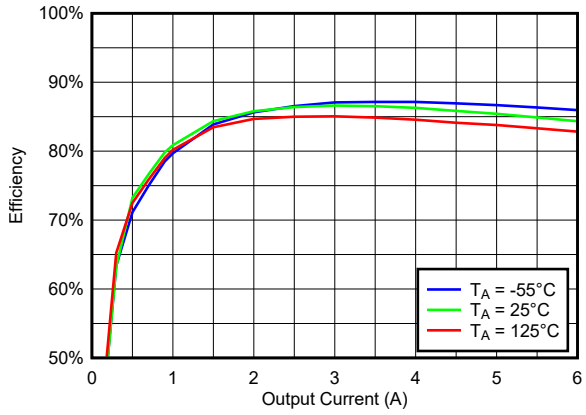
L_{OUT} = 2.2µH

Figure 7-16. Efficiency vs Load Across Temperature at 500kHz, VIN = 12V, VOUT = 5V



L_{OUT} = 2.2µH

Figure 7-17. Efficiency vs Load Across Temperature at 500kHz, VIN = 12V, VOUT = 3.3V



L_{OUT} = 2.2µH

Figure 7-18. Efficiency vs Load Across Temperature at 500kHz, VIN = 12V, VOUT = 1.8V

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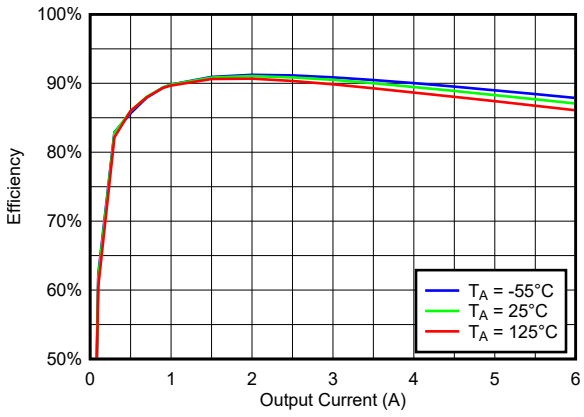
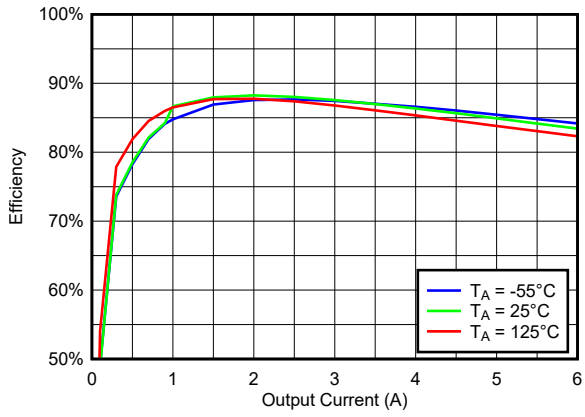
7.7 Typical Characteristics (continued)

TPS7H4012 44-pin HTSSOP (DDW) package, VIN = PVIN, VIN = 12V, C_{SS} = 22nF, Kemet MPXV1D2213L series inductor and SS10P4-M3/87A Schottky diode for efficiency tests, T_A = 25°C, unless otherwise noted.



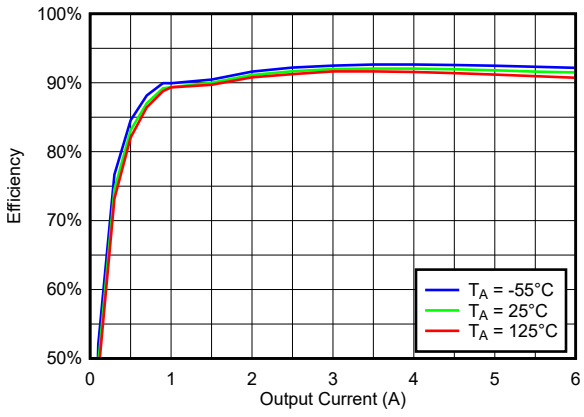
L_{OUT} = 1µH

Figure 7-19. Efficiency vs Load Across Temperature at 1MHz, VIN = 5V, VOUT = 2.5V



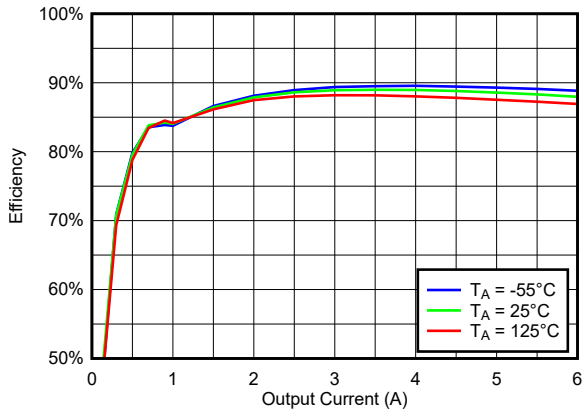
L_{OUT} = 1µH

Figure 7-20. Efficiency vs Load Across Temperature at 1MHz, VIN = 5V, VOUT = 1.8V



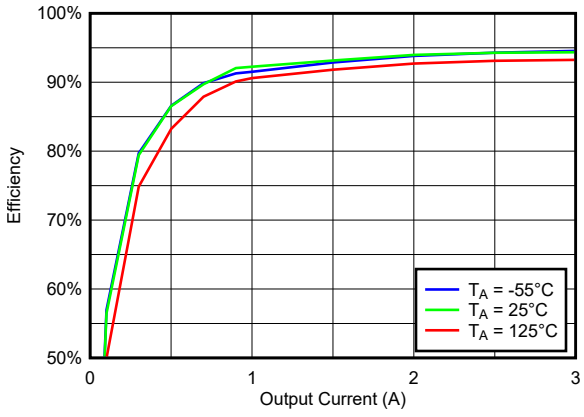
L_{OUT} = 1µH

Figure 7-21. Efficiency vs Load Across Temperature at 1MHz, VIN = 12V, VOUT = 5V



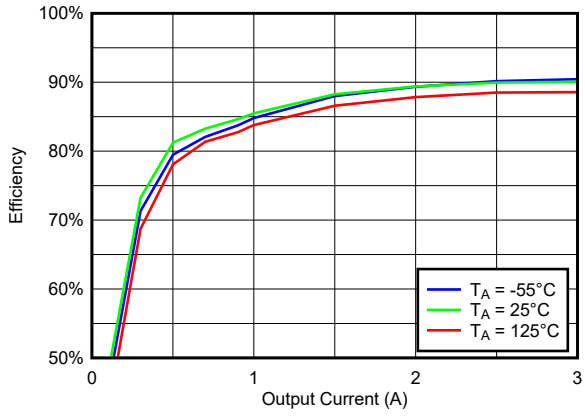
L_{OUT} = 1µH

Figure 7-22. Efficiency vs Load Across Temperature at 1MHz, VIN = 12V, VOUT = 3.3V



L_{OUT} = 2.2µH, TPS7H4013

Figure 7-23. Efficiency vs Load Across Temperature at 500kHz, VIN = 12V, VOUT = 5V for TPS7H4013



L_{OUT} = 2.2µH, TPS7H4013

Figure 7-24. Efficiency vs Load Across Temperature at 500kHz, VIN = 12V, VOUT = 2.5V for TPS7H4013

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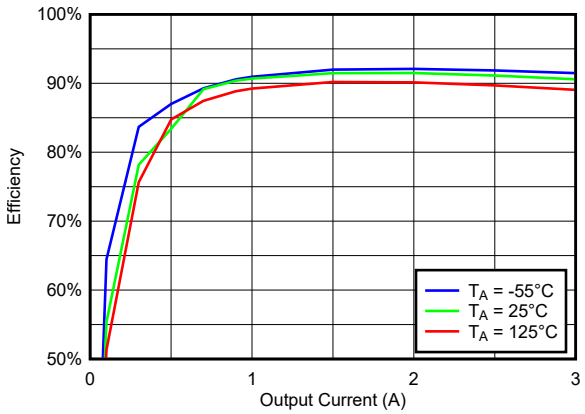
7.7 Typical Characteristics (continued)

TPS7H4012 44-pin HTSSOP (DDW) package, VIN = PVIN, VIN = 12V, C_{SS} = 22nF, Kemet MPXV1D2213L series inductor and SS10P4-M3/87A Schottky diode for efficiency tests, T_A = 25°C, unless otherwise noted.



L_{OUT} = 2.2µH, TPS7H4013

Figure 7-25. Efficiency vs Load Across Temperature at 500kHz, VIN = 5V, VOUT = 1.8V for TPS7H4013

Graph Placeholder

L_{OUT} = 2.2µH

Figure 7-26. VSNS+ vs Output Current at 500kHz

Graph Placeholder

L_{OUT} = 1µH

Figure 7-27. VSNS+ vs Output Current at 1MHz

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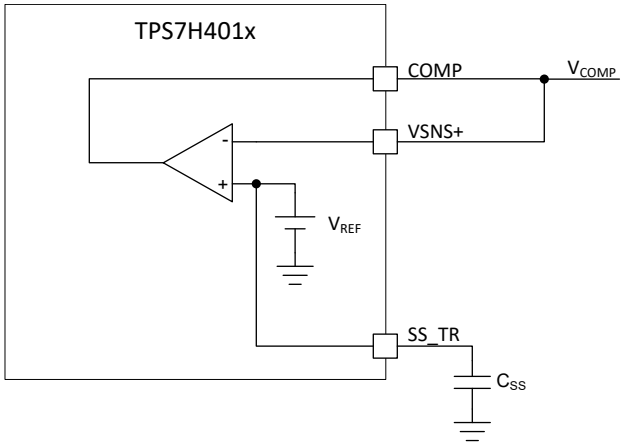
8 Parameter Measurement Information



A. V_{REF} = V_{COMP}. This accurate reference voltage value includes the error amplifier offset, V_{IO}. Use this value to set the output voltage.

Figure 8-1. Reference Voltage Measurement

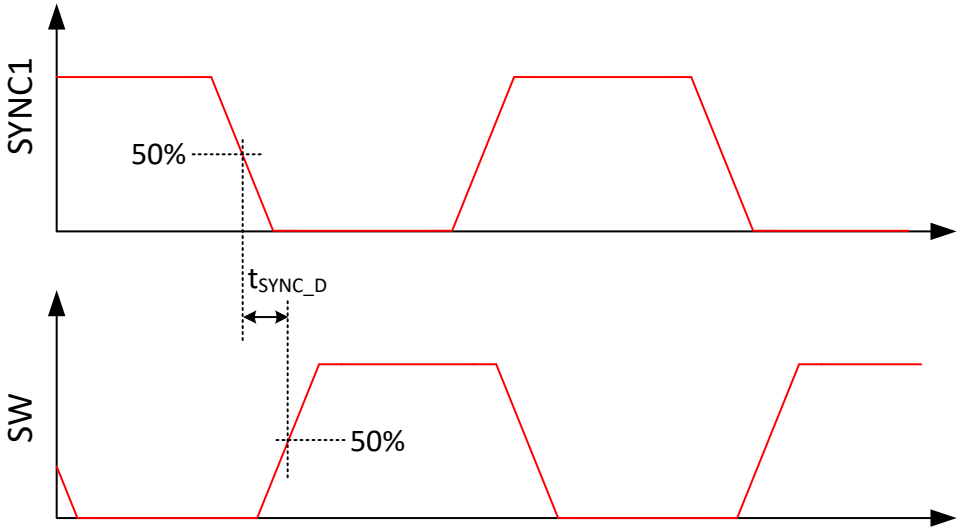


Figure 8-2. SYNC1 to SW Delay: Inverted Sync

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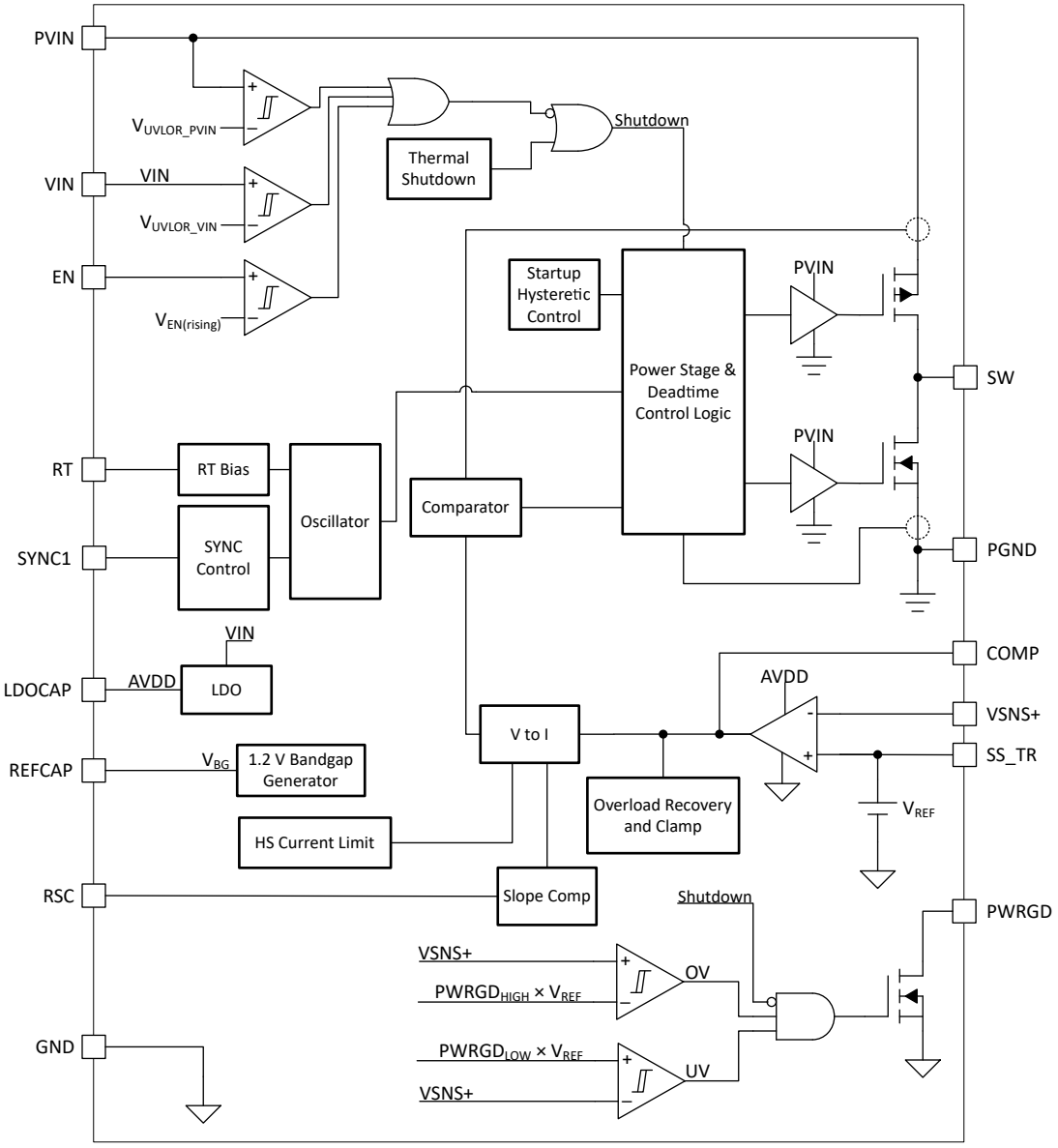
9 Detailed Description

9.1 Overview

The TPS7H4012 and TPS7H4013 are 14V, 6A and 3A synchronous step-down (buck) converter with two integrated MOSFETs; a PMOS for the high side and an NMOS for the low side. To improve performance during line and load transients, the device implements a constant frequency, peak current mode control, which also simplifies external frequency compensation. The wide switching frequency range, 100kHz to 1MHz, allows for efficiency and size optimization when selecting the output filter components. The integrated MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 6A. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 VIN and Power VIN Pins (VIN and PVIN)

The VIN pin provides power to internal control circuitry. The PVIN pins and PVIN pad provide the input voltage to the internal high side FET. Both pins have an input voltage range of 4.5V to 14V. The pins must be the same nominal voltage and they must power up and power down at the same time. Generally this is achieved by providing them from the same voltage source.

Both VIN and PVIN have individual UVLO (undervoltage lockout) rising thresholds, V_{UVLOR_VIN} and V_{UVLOR_PVIN} respectively. This is to ensure the device internal circuitry remains in a known off condition until a minimum voltage is reached. Additionally, VIN and PVIN have individual UVLO falling thresholds, V_{UVLOF_VIN} and V_{UVLOF_PVIN} respectively. If the voltage falls and these values are reached, the device will turn-off.

As described in Section 9.3.4, a voltage divider connected to the EN pin can be utilized to configure the effective device UVLO.

9.3.2 Voltage Reference

The device generates an internal nominal 1.2V bandgap reference voltage, V_{BG}. This is the voltage present on the REFCAP pin during steady state operation. A 470nF capacitor to ground is required at the REFCAP pin for proper electrical operation as well as to ensure robust SET performance of the device. This bandgap voltage is used to derive the nominal 0.6V reference voltage for the error amplifier, $V_{REF(internal)}$.

The reference voltage that is fed into the error amplifier is utilized to set the output voltage. However, error amplifiers have intrinsic offset, V_{IO}, which contribute to the overall accuracy error. Therefore, the voltage that is actually used to set the output voltage is $V_{REF(internal)}$ + V_{IO}. This combined value is defined as V_{REF} and is designed to be the accurate value to set the output voltage. V_{REF} is specified across line, temperature, and TID in the Electrical Characteristics. Because V_{REF} is measured in an open loop configuration, the effects of switching frequency and load on V_{REF} are not included in the specification. See typical graphs Figure 7-26 and Figure 7-27 which show the minimal affect of current and switching frequency on the output sense voltage. See Section 10.2.2.8 for more details on calculating the output voltage accuracy.

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9.3.3 Voltage Sensing and Setting VOUT

The TPS7H401x features a VSNS+ pin for remote sensing. During steady state operation, VSNS+ will be equal to the reference voltage, V_{REF} (0.6V typical). By appropriately setting the resistor divider for VSNS+, the output voltage value across the load, V_{LOAD}, can be set using as shown in Figure 9-1. By connecting VSNS+ to the load, $R_{parasitic1}$ is accounted for and remote sensing is achieved. Note a good ground connection is recommended to avoid offset due to differences in ground between the load and the TPS7H401x.

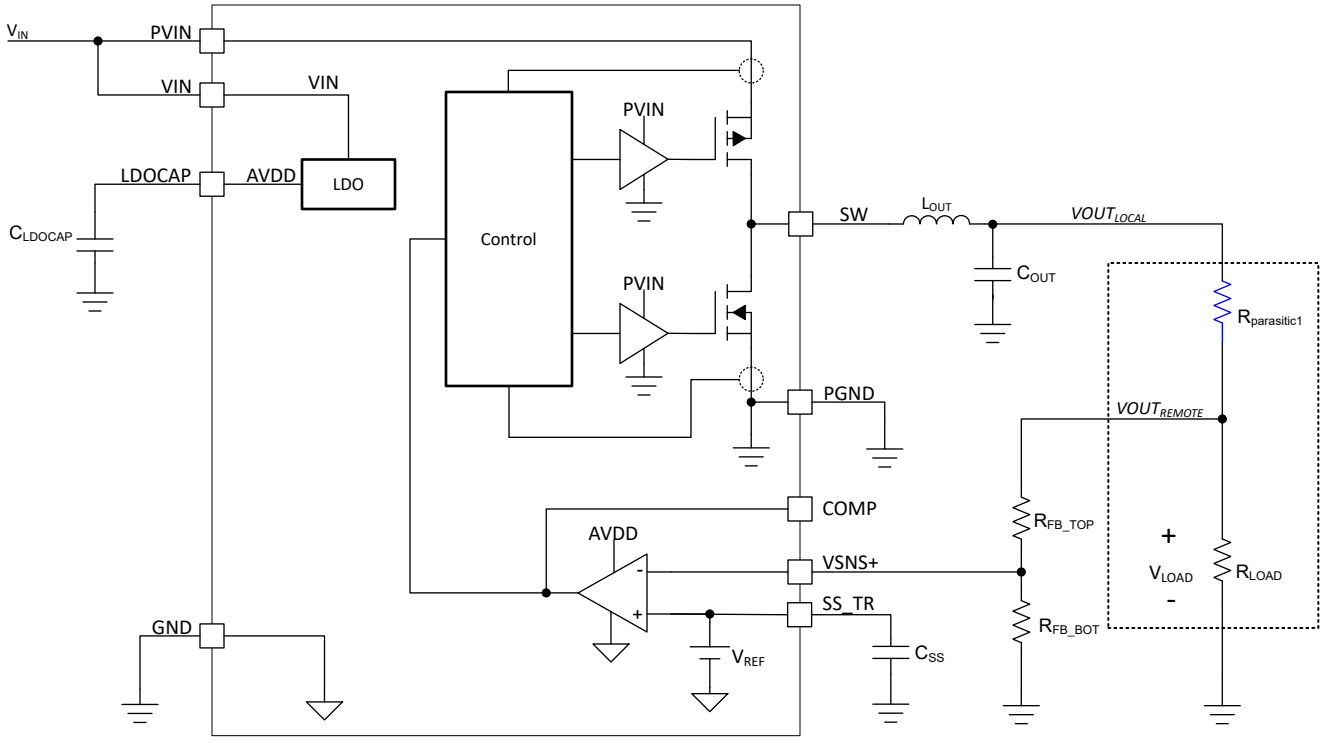

Figure 9-1. Voltage Sense Diagram

TI recommends 1% tolerance or better resistors. Start with a 10kΩ for R_{FB_TOP} and use Equation 1 to calculate R_{FB_BOT}. To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors.

$$R_{FB_BOT} = \frac{V_{REF}}{V_{OUT(set)} - V_{REF}} \times R_{FB_TOP} \quad (1)$$

where

- V_{REF} = 0.6V (typ)
- $V_{OUT(set)}$ = voltage set point; this is the voltage regulated across the load

9.3.3.1 Minimum Output Voltage

Like all current-mode control buck converters, there is a minimum configurable output voltage. First, the output voltage can never be lower than the internal voltage reference of 0.6V (typ). Additionally, the minimum on time, $t_{on(min)}$, will limit the minimum output voltage. $t_{on(min)}$ is specified as 250ns (max). See the Electrical Characteristics for more information. The minimum output voltage is approximated by Equation 2.

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$$VOUT_{(min)} \approx V_{IN} \times t_{ON(\min)} \times f_{SW} \quad (2)$$

In this equation:

- $VOUT_{(min)}$ is the minimum possible output voltage
- VIN is the input voltage for the application
- $t_{on(min)}$ is the minimum on-time; use the maximum $t_{on(min)}$ value for the worst case calculation
- f_{SW} is the switching frequency; use the maximum possible f_{SW} for the worst case calculation

Table 9-1 shows calculated minimum output voltages for selected values of f_{SW} and VIN assuming $t_{on(min)}$ = 250ns.

Table 9-1. Calculated Minimum Output Voltages

f_{SW}	VIN	$VOUT_{(min)}$
100kHz	5V	0.6V(1)
	12V	0.6V(1)
	14V	0.6V(1)
500kHz	5V	0.625V
	12V	1.5V
	14V	1.75V
1MHz	5V	1.25V
	12V	3V
	14V	3.5V

(1) The calculated value is lower, but the minimum is limited to V_{REF} itself which is typically 0.6V.

9.3.3.2 Maximum Output Voltage

The TPS7H401x has a maximum output voltage due to the minimum off time, $t_{off(min)}$. This minimum off time is not due to an internal charge pump like some buck regulators. Instead, the minimum off time is to ensure switching noise and internal circuitry behavior does not cause excessive duty cycle jitter. The maximum output voltage is approximated by Equation 2.

$$VOUT_{(max)} \approx V_{IN} \times \left(1 - t_{OFF(\min)} \times f_{SW}\right) \quad (3)$$

In this equation:

- $VOUT_{(max)}$ is the maximum possible output voltage
- VIN is the input voltage for the application
- $t_{off(min)}$ is the minimum off-time
- f_{SW} is the switching frequency

Table 9-2 shows calculated maximum output voltages for selected values of f_{SW} and VIN assuming $t_{off(min)}$ = 306ns.

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Table 9-2. Calculated Maximum Output Voltages

f_{SW}	VIN	$VOUT_{(max)}$
100kHz	5V	4.85V
	12V	11.63V
	14V	13.57V
500kHz	5V	4.24V
	12V	10.16V
	14V	11.86V
1MHz	5V	3.47V
	12V	8.33V
	14V	9.72V

9.3.4 Enable

When the enable pin is low, the device will enter shutdown mode and not regulate the output voltage. Normally, an external resistor divider from VIN to GND is used to feed EN. The resistors can be appropriately sized to turn on the device when a desired preset input voltage is reached as shown in Equation 4. This can be used to create an adjustable UVLO to compliment the default internal UVLO voltage on the VIN and PVIN pins.

$$R_{EN_BOT} = \frac{V_{EN(rising)}}{VIN_{(rising)} - V_{EN(rising)}} \times R_{EN_TOP} \quad (4)$$

where

- $VIN_{(rising)}$ = the VIN value that will cause EN to go high
- $V_{EN(rising)}$ = 0.61V (typ)
- R_{EN_TOP} = feedback resistor from VIN to EN
- R_{EN_BOT} = feedback resistor from EN to GND

The EN pin has 100mV (typ) of hysteresis. Therefore, Equation 5 can be used to calculate the $VIN_{(falling)}$ voltage.

$$VIN_{(falling)} = V_{EN(falling)} \times \frac{R_{EN_TOP} + R_{EN_BOT}}{R_{EN_BOT}} \quad (5)$$

where

- $VIN_{(falling)}$ = the VIN value that will cause EN to go low and turn-off the TPS7H401x
- $V_{EN(falling)}$ = 0.51V (typ)

Alternatively, the EN pin may be driven directly from a microcontroller or FPGA. The low voltage threshold of the enable pin aids in support of 1.1, 1.8, 2.5, and 3.3V logic levels.

9.3.5 Power Good (PWRGD)

The PWRGD pin is an open-drain output that is asserted when the output voltage reaches an appropriate range. The PWRGD pin may be pulled-up through a resistor to VOUT or to another voltage level within the device recommended operating conditions. Select the resistor size to keep the maximum current sunk by PWRGD to under the recommended operating condition current maximum of 2mA. Generally a pull up resistor of 10kΩ is sufficient. Using a larger value resistor will minimize power dissipation but may allow switching noise to couple into the PWRGD signal due to the weaker pull-up.

PWRGD will be asserted or deasserted when VOUT is within a certain percentage of its programmed value. This is accomplished by comparing the voltage on VSNS+ to V_{REF}. For example, when VSNS+ reaches $PWRGD_{LOW_R\%}$ (typically 95%) of its final value, PWRGD is asserted. When VSNS+ falls below $PWRGD_{LOW_F\%}$ (typically 92%), PWRGD is deasserted. See Figure 9-2 for these waveforms.

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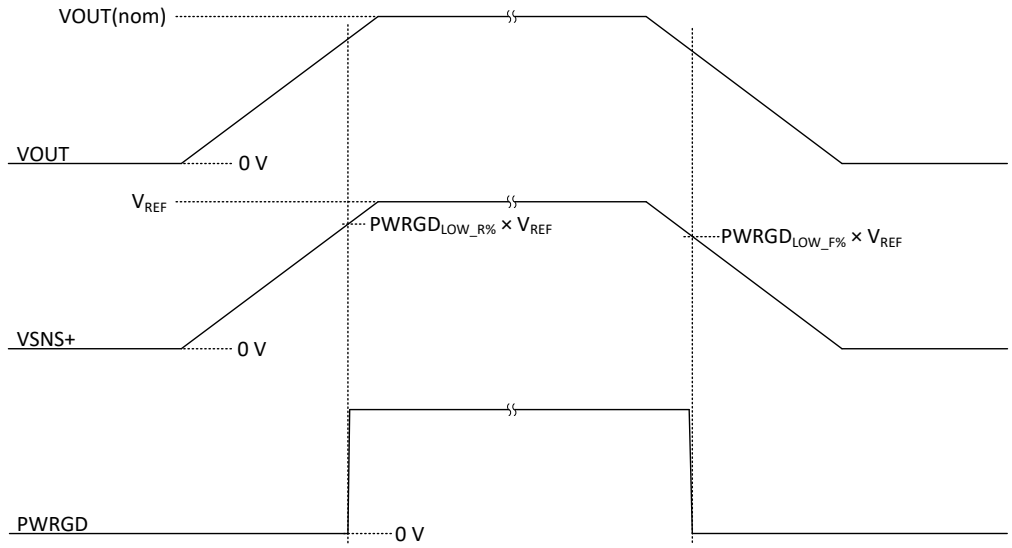

Figure 9-2. Power Good Low Thresholds

Power good also has a threshold if an overvoltage event occurs on VOUT. For example, when VSNS+ reaches $PWRGD_{HIGH_R\%}$ (typically 108%) of its final value, PWRGD is deasserted. When VSNS+ falls below $PWRGD_{HIGH_F\%}$ (typically 105%), PWRGD is asserted. See Figure 9-3 for these waveforms.

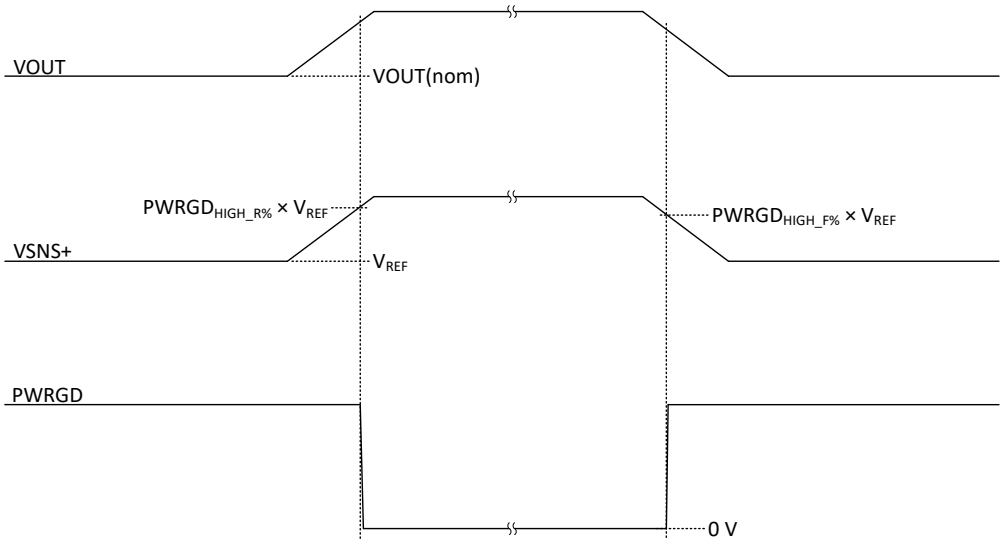

Figure 9-3. Power Good High Thresholds

The PWRGD is in a defined state when the VIN input voltage is greater than 2V but has reduced current sinking capability. The PWRGD achieves full current sinking capability by the time VIN reaches 4.5V. See VIN_{MIN_PWRGD} in the Electrical Characteristics.

In addition to the description of PWRGD above, PWRGD is deasserted during other conditions that cause regulation to stop such as:

- VIN or PVIN are in UVLO
- The device is in thermal shutdown
- The device EN pin is deasserted
- the COMP pin reaches the $COMP_{SHDN}$ threshold (1.9V typical)

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9.3.6 Adjustable Switching Frequency and Synchronization

There are multiple clocking mode options to enable use of both the programmable internal clock and an externally synchronized clock. This allows flexibility to synchronize devices to a system clock . The modes are listed in Table 9-3.

Table 9-3. Clock Modes

MODE	RT	SYNC1 INPUT
Internal clock	Resistor from RT to GND	None
External clock: default f_{SW}	Resistor from RT to GND	Input f_{SW} 180° out of phase
External clock: no default f_{SW}	Float	Input f_{SW} 180° out of phase

9.3.6.1 Internal Clock Mode

The TPS7H401x is configured for internal clock mode if the RT pin is populated and no external clock is input on SYNC1. In internal clock mode (also sometimes called internal oscillator mode), a resistor is connected between the RT pin and GND to configure the switching frequency, f_{SW}, of the device. The nominal switching frequency is adjustable from 100kHz to 1MHz depending on the RT resistor value, which can be calculated using Equation 6. Figure 9-4 shows the relationship curve between the RT resistor value and the configurable switching frequency range.

$$RT = 86{,}090 \times f_{SW}^{-1.104} \quad (6)$$

where

- RT in kΩ
- f_{SW} in kHz

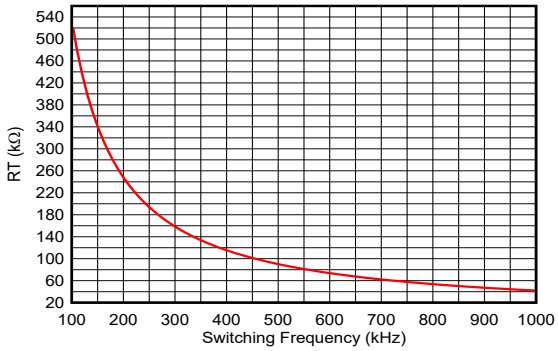

Figure 9-4. Nominal RT vs Switching Frequency

9.3.6.2 External Clock Mode

The TPS7H401x is configured for external clock mode if a clock signal is input on SYN1. In this mode, a clock is input on SYNC1 and the TPS7H401x switching will switch 180° out of phase with SYNC1.

In external clock mode, RT may be left floating as it is not required to program the switching frequency with a resistor from RT to GND. However, a resistor from RT to GND must be configured (as shown in Section 9.3.6.1) if it is desired to have a fallback default switching frequency if the input clock is not available (such as before the clock is provided to the TPS7H401x device or during a clock fault). If RT is populated in this mode and no external clock signal is detected for $t_{CLK_E_I}$ (typically 2 clock cycles), the TPS7H401x will transition to the internal clock. This is shown in Figure 9-5. If the external clock is again provided, it will switch back to the external clock in $t_{CLK_I_E}$ (typically 1 clock cycle). This is shown in Figure 9-6. When this configuration is utilized, program the internal clock frequency to the same nominal value as the external clock frequency.

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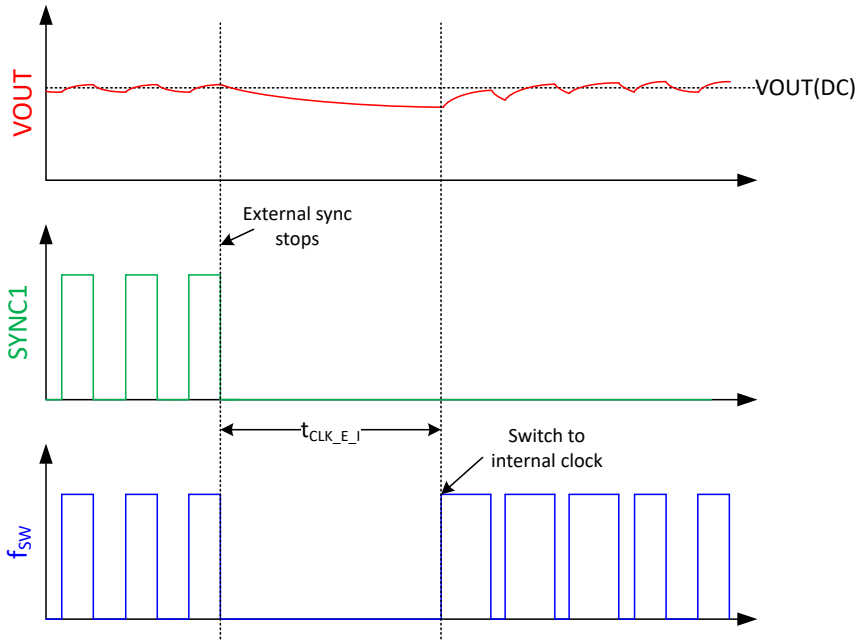

Figure 9-5. External to Internal Clock Transition

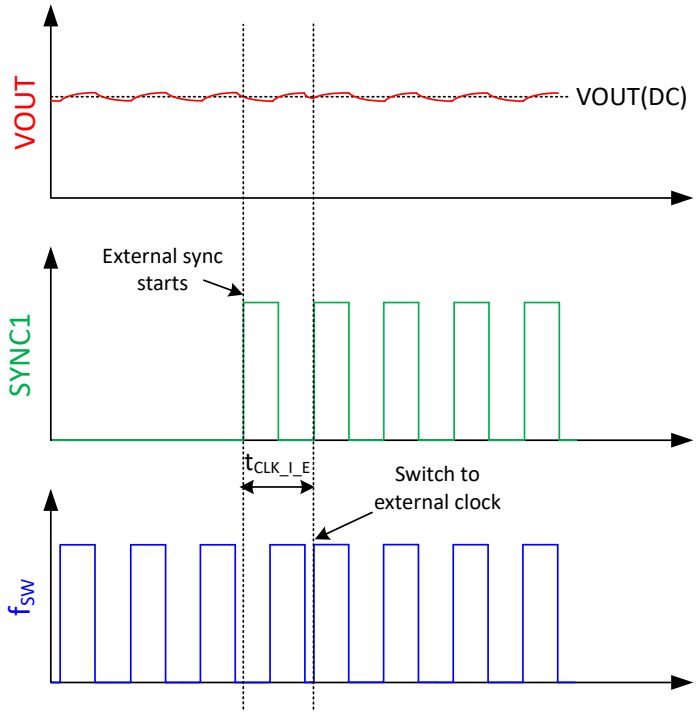

Figure 9-6. Internal to External Clock Transition

The external clock may be provided by an oscillator, FPGA, or other suitable device. Alternatively, the external clock may be provided by a TPS7H4011 device that is configured in internal oscillator mode.

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9.3.7 Turn-On Behavior

The device will enter into a pulse-skipping mode (hysteretic mode) during startup in the event that VSNS+ is greater than the voltage at the SS_TR pin. During this period, the high-side switch will remain off and the low-side switch will remain on until VSNS+ again falls below the voltage at SS_TR. This is because a lower output voltage is needed than that supported by the minimum on time.

Thus, instantaneous output pulses can be higher or lower than the desired voltage. This behavior is evident when operating at high frequency with high bandwidth or with high VIN to VOUT ratios. When the minimum on-pulse is greater than the minimum controllable on-time, the pulse-skipping behavior is generally not observed at startup.

9.3.7.1 Soft-Start (SS_TR)

A capacitor at the SS_TR pin is utilized in order to slow the rise of the internal reference voltage, $V_{REF(internal)}$. By slowing the rise of the reference voltage during startup, the output voltage slew rate will be controlled. This is useful to prevent excessive inrush current.

Measured soft start time for the SS_TR voltage to rise from 10% to 90% of its value are detailed in the Electrical Characteristics. Generally a 22nF or larger ceramic C_{SS} capacitor is recommended; however, values down to 5.6nF are shown if a faster startup is desired. Additionally, Equation 7 can be used to approximate startup equations for arbitrary capacitor values.

$$t_{SS} = 0.25 \times C_{SS} \quad (7)$$

where

- t_{SS} in ms
- C_{SS} in nF

Note that the SS_TR pin follows that of an RC charging circuit curve. Therefore, the output voltage follows a similar curve.

When any of the following scenarios occur, the SS_TR pin is discharged through the internal $R_{SS(discharge)}$ pull-down resistor (typically 442Ω):

- the input UVLO is triggered,
- the EN pin is pulled below $V_{EN(falling)}$ (0.51V typical)
- the COMP pin reaches the $COMP_{SHDN}$ threshold (1.9V typical)
- a thermal shutdown event occurs

When the SS_TR pin is discharged, the device cannot restart again until it has discharged to below $SS_{startup}$ (typically 20mV) in order to ensure proper soft-start behavior.

9.3.7.2 Safe Start-Up Into Prebiased Outputs

The device prevents the low-side MOSFET from continuously discharging a prebiased output.

9.3.7.3 Tracking and Sequencing

Many of the common power-supply sequencing methods can be implemented using the SS_TR, EN, and PWRGD pins.

The sequential method is shown in Figure 9-7 using two TPS7H401x devices. The PWRGD pin of the first device is coupled to the EN pin of the second device, which enables the second power supply after the primary supply reaches regulation. If a further delay is desired between sequencing the first and second device, an optional C_{PWRGD} capacitor may be included on PWRGD as well. This will cause an RC delay based on the value of the power good pull-up resistor and capacitor utilized.

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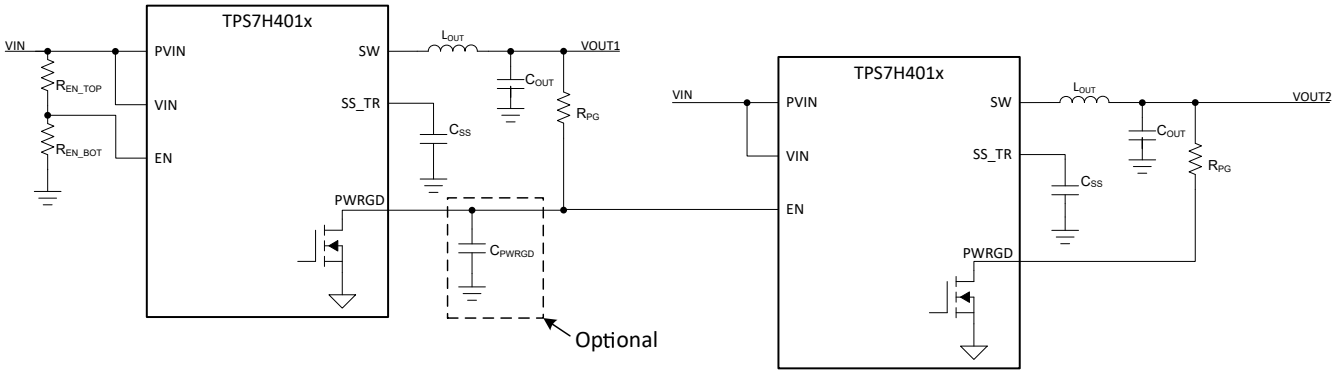

Figure 9-7. Sequential Start-Up Sequence

Figure 9-8 shows the method implementing ratiometric sequencing by connecting the SS_TR pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. Note that in this configuration, the SS_TR voltage tends towards the average of the two parts since SS_TR is the internal voltage reference of the device. This will cause some additional voltage error on the outputs of each device. This is because the precise V_{REF} utilized for the control loop takes into account the offset of each individual devices error amplifier only when operating with its own SS_TR.

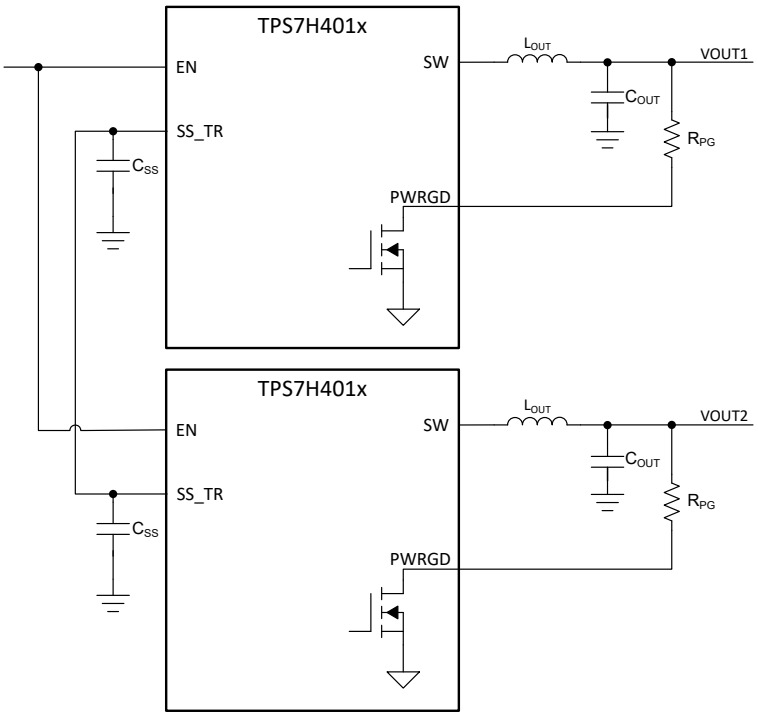

Figure 9-8. Ratiometric Start-Up Sequence

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9.3.8 Protection Modes

The following protection modes are detailed in the following sections:

- Overcurrent Protection: Section 9.3.8.1
  - High-Side 1 Overcurrent Protection (HS1): Section 9.3.8.1.1
  - High-Side 2 Overcurrent Protection (HS2): Section 9.3.8.1.2
  - COMP Shutdown: Section 9.3.8.1.3
  - Low-Side Overcurrent Sinking Protection: Section 9.3.8.1.4
- Output Overvoltage Protection (OVP): Section 9.3.8.2
- Thermal Shutdown: Section 9.3.8.3

9.3.8.1 Overcurrent Protection

The TPS7H401x device employs multiple overcurrent protection mechanisms. The device is primarily protected from overcurrent conditions with cycle-by-cycle current limiting for the high-side MOSFET. This current limit is termed high side 1 overrcurrent protection (HS1), and its value is selectable between four distinct current limits by utilizing the ILIM pin. Additional secondary protection is provided through high side 2 overcurrent protection (HS2). Finally, tertiary protection is provided through COMP shutdown. In addition to the various high-side current limit protections, a low-side sinking overcurrent protection mechanism is also provided by the TPS7H401x. These current protection mechanisms are detailed in the subsequent sections

9.3.8.1.1 High-Side 1 Overcurrent Protection (HS1)

The device implements current mode control, which uses the COMP pin voltage to control the turn-off of the high-side MOSFET and the turn-on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared. When the peak switch current intersects the programmed high side current, I_{OC_HS1}, the high-side switch is commanded off (although the high side will be on for at least the minimum on time, t_{ON}).

HS1 is implemented utilizing the COMP voltage. As the device approaches I_{OC_HS1}, COMP increases which causes the g_{mps} of the device to approach zero. Therefore, at high enough values of COMP, the output current is essentially clamped to the selected value. This functionality is shown in the simplified waveforms of Figure 9-9.

Note that the I_{OC_HS1} threshold specification is measured in an open loop configuration due to testability limitations while actual short circuit events are dynamic and in closed loop. In most cases, the resulting current limit value will be similar, but in some short circuit conditions, the values may exceed the specified thresholds. This is particularly true at low values of VIN (such as under 5V), higher switching frequencies, and colder temperatures

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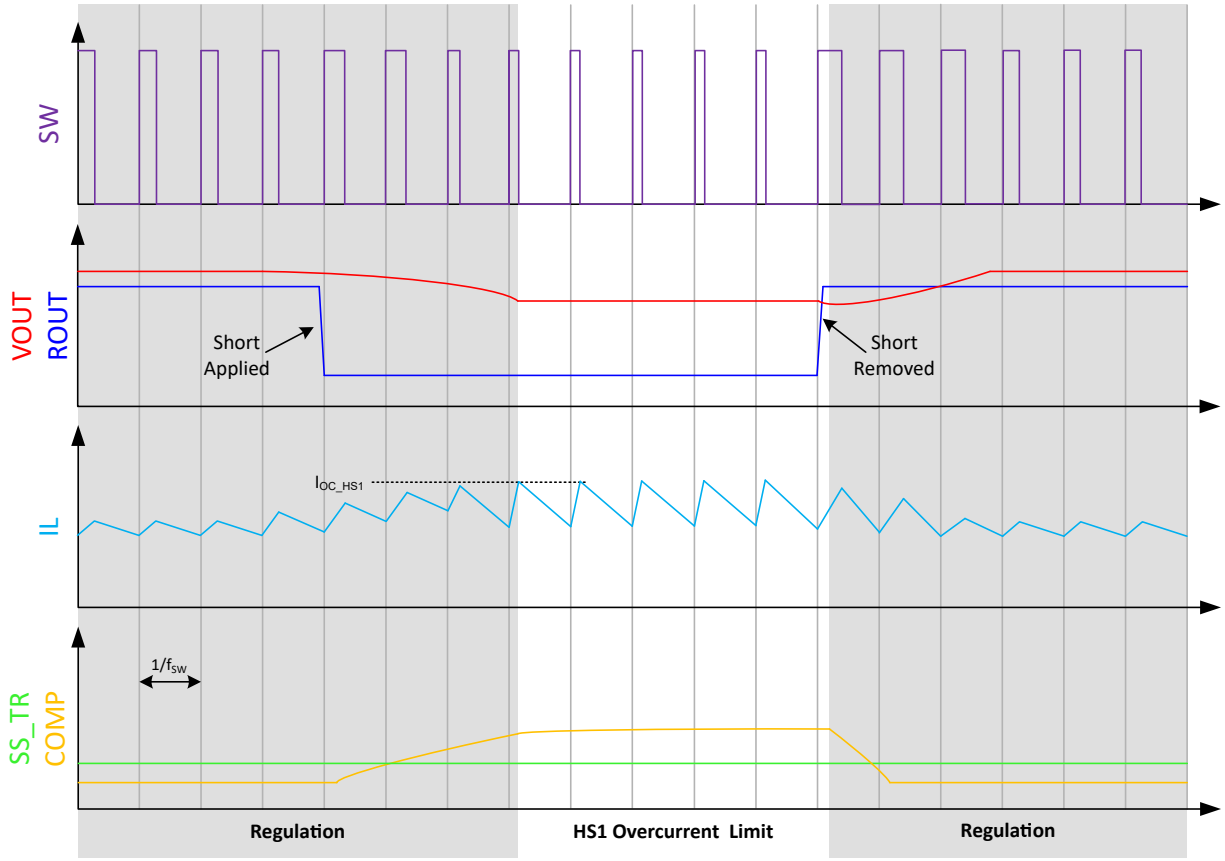

Figure 9-9. High-Side 1 Overcurrent Protection

The high side 1 overcurrent protection (HS1) threshold value is typically 9.7A for the TPS7H4012 and 5.6A for the TPS7H4013. By limiting the current to a specific value, an inductor may be appropriately sized to handle the maximum current. The recommended DC maximum output current is 6A for the TPS7H4012 and 3A for the TPS7H4013.

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9.3.8.1.2 High-Side 2 Overcurrent Protection (HS2)

Sometimes, the HS1 current limit is not sufficient to protect the device. For example, a short circuit may be so aggressive that even if the high side is only on for the minimum on time, t_{ON}, the current would continue to rise. To mitigate this risk, the TPS7H401x implements a secondary overcurrent protection in the form of high-side overcurrent protection 2 (HS2).

The HS2 current limit is reached when the current through the high side MOSFET meets or exceeds I_{OC_HS2}. To prevent sustained current increase, the next four high-side cycles are skipped while the low side MOSFET remains on in order to discharge the inductor. The simplified waveforms of this operation are shown in Figure 9-10.

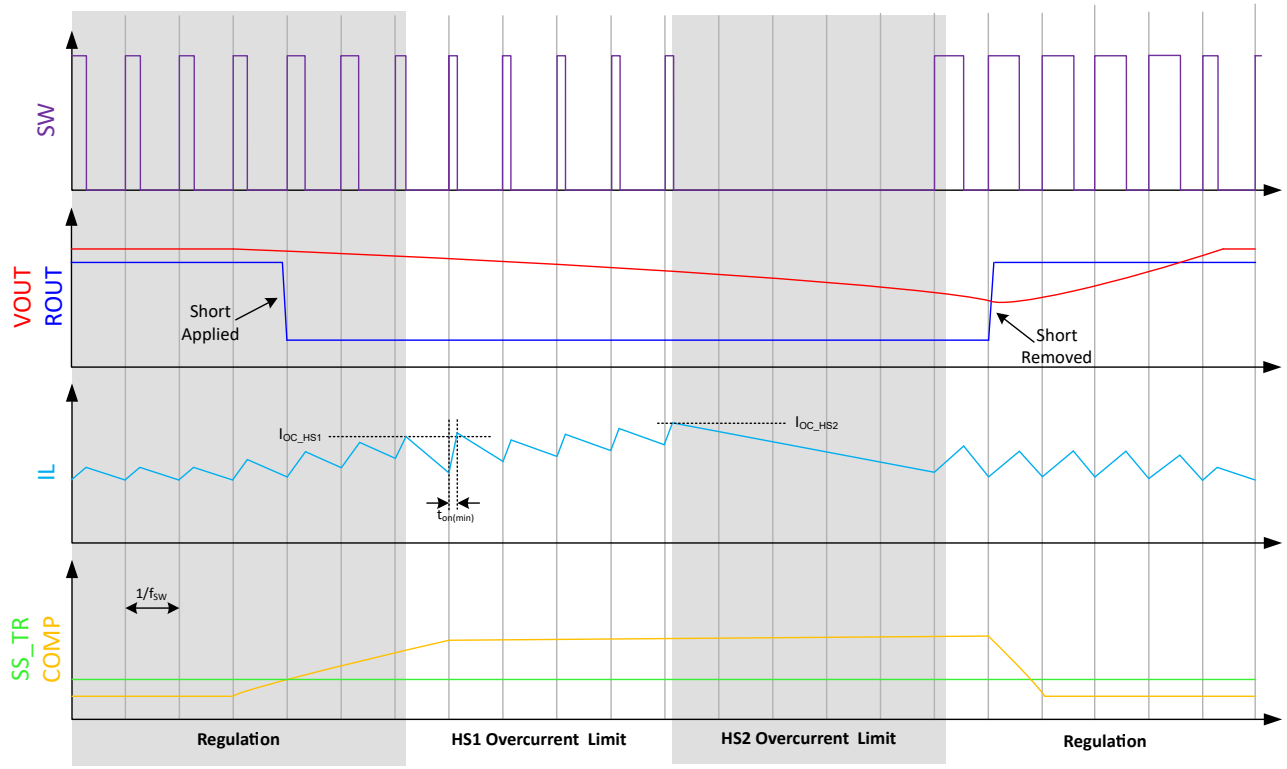

Figure 9-10. High-Side 2 Overcurrent Protection

The high side 2 overcurrent protection (HS2) threshold value is typically 11.8A for the TPS7H4012 and 6.8A for the TPS7H4013.

Similar to the I_{OC_HS1} current limit, the I_{OC_HS2} limit threshold is measured in an open loop configuration due to testability limitations while actual short circuit events are dynamic and in closed loop

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9.3.8.1.3 COMP Shutdown

Since the voltage on the COMP pin is proportional to the device output current, by clamping the COMP voltage, another method is achieved to protect the device from overcurrent events. Specifically, if COMP rises above $COMP_{SHDN}$ (typically 1.9V), the part will shutdown after a small delay time, $t_{COMP(delay)}$.

This feature is a complement to the HS1 and HS2 current limits. Since the slew rate of COMP is limited by the overall loop bandwidth and by the drive strength of the error amplifier, the time it takes COMP to reach $COMP_{SHDN}$ during a fault depends on the loop compensation and specific type of fault. During most faults, HS1 will be reached before COMP reaches $COMP_{SHDN}$. HS2 will often be reached before COMP reaches $COMP_{SHDN}$; however depending on the fault type, COMP may reach $COMP_{SHDN}$ and disable the part before HS2 is reached. Consequently, $COMP_{SHDN}$ can be thought of as a type of fail-safe.

After COMP reaches $COMP_{SHDN}$ and $t_{COMP(delay)}$ passes, the device stops switching and begins discharging the SS_TR pin through a pull-down resistance, $R_{SS(discharge)}$ (typically 442Ω). The part will not attempt a restart until SS_TR has discharged to $SS_{startup}$ (typically 20mV). This provides a cool down period for the TPS7H401x. Note that this discharge time is directly dependent upon the value of the soft start capacitor, C_{SS}. An example of the COMP shutdown functionality is shown in the simplified waveforms of Figure 9-9.

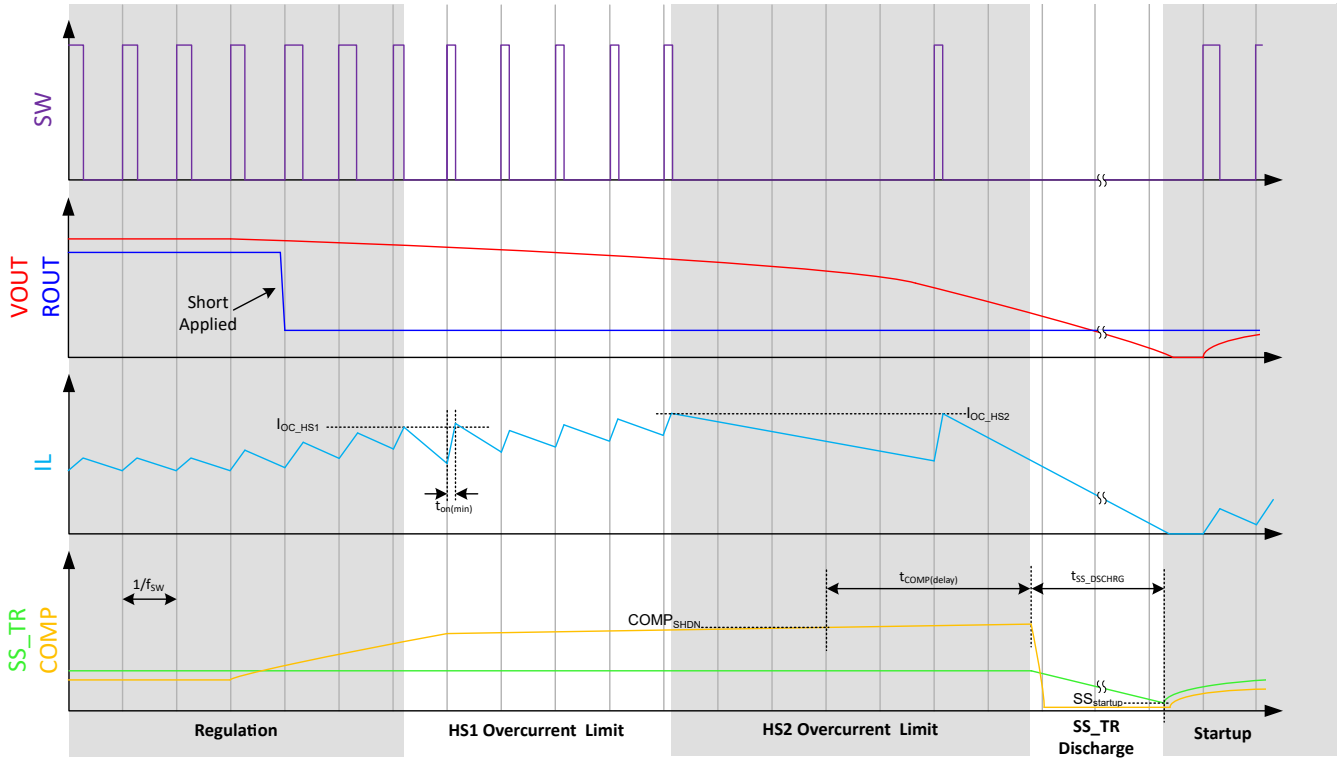

Figure 9-11. COMP Shutdown Protection

Additionally, COMP may reach $COMP_{SHDN}$ if an aggressive load step is applied to the output load and a high loop bandwidth is utilized. This is because in this situation, COMP can slew higher faster than the load can respond. This can be avoided through a compensation network that is appropriately designed for the worse case load step.

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9.3.8.1.4 Low-Side Overcurrent Sinking Protection

It is possible for the low-side MOSFET to sink current from the load (such as during light load operation). In certain situations (such as a high current load being suddenly removed or VOUT being raised above the set point), the low-side sink current can become excessive. Therefore, low-side overcurrent sinking protection is provided.

If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle. When the low-side MOSFET turns off, the switch node voltage increases and forward biases the high-side MOSFET parallel body diode (the high-side MOSFET is still off at this stage).

9.3.8.2 Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. The OVP circuit engages when VSNS+ ≥ $PWRGD_{HIGH_R\%}$ × V_{REF}. Typically, this means the OVP circuitry engages when VOUT rises above 108% of its nominal value. When OVP is active, the high-side FET stays off and the low-side FET stays on to quickly discharge VOUT.

An example that could cause an overvoltage condition is when the power supply output is overloaded for a sustained period of time. Therefore, the error amplifier compares the actual output voltage to the reference voltage. If the VSNS+ pin voltage is lower than the reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes this overshoot.

If the VSNS+ pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSNS+ voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

9.3.8.3 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 170°C (typical). The device re-initiates the power-up sequence when the junction temperature drops below 135°C (typical). The thermal shutdown protection aims to keep the device as cool as possible during over temperature conditions.

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9.3.9 Error Amplifier and Loop Response

Figure 9-12 shows a simplified model for the device control loop. It can be utilized to aid in determining the frequency response and transient response of the buck regulator system. The simplified model is composed of an operational transconductance error amplifier (OTA), the power stage, external feedback, and external compensation. The effects of slope compensation are not shown in this model. More information on the error amplifier and power stage are shown in the subsequent sections (Section 9.3.9.1 and Section 9.3.9.2 respectively).

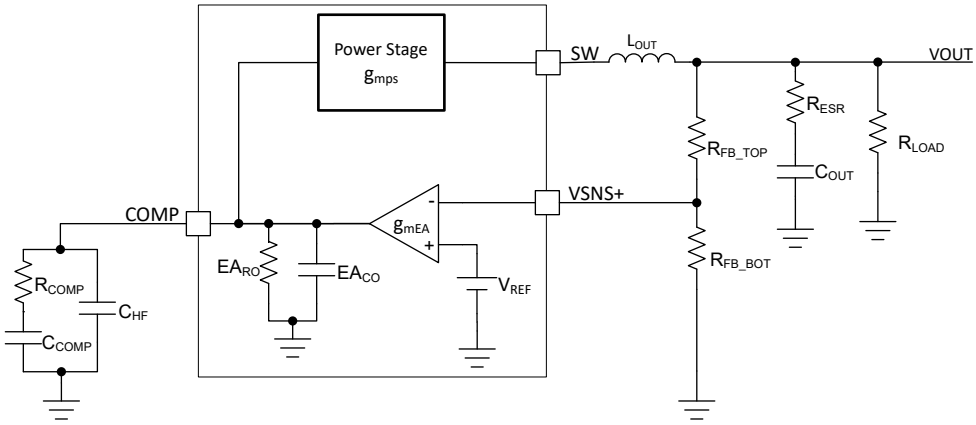

Figure 9-12. Simplified Small Signal Model For Loop Response

9.3.9.1 Error Amplifier

The TPS7H401x device utilizes a transconductance error amplifier. The error amplifier compares the VSNS+ voltage to the internal V_{REF} voltage reference.

The transconductance of the error amplifier is typically 1,650µS (µA/V). The frequency compensation network is connected between the COMP pin and GND. The error amplifier DC gain is typically 11,500V/V. The error amplifier output resistance is 7MΩ (typ).

9.3.9.2 Power Stage Transconductance

To optimize the overall device behavior at different current levels, the TPS7H4012 and TPS7H4013 have different a power stage transconductance, g_{mPS}. The TPS7H4012 has a typical g_{mPS} of 11.2S (measured at V_{COMP} = 0.7V) and the TPS7H4013 has a lower typical g_{mPS} of 6.2S (measured at V_{COMP} = 0.75V).

9.3.9.3 Slope Compensation

The desired slope compensation, SC, can be configured with a resistor from the RSC pin to GND. The TPS7H401x device adds a compensating ramp to the switch current signal for all duty cycles. Various values of RSC and the resulting slope compensation are shown in the Electrical Characteristics. Equation 8 is provided to approximate the value of RSC needed to achieve a desired slope compensation.

$$R_{SC} = 0.208 \times g_{mps} \times SC^{-1.5} \times f_{SW} \quad (8)$$

where

- R_{SC} is the suggested value of resistance in kΩ to achieve the desired slope compensation
- g_{mps} is the power stage gain in S
- SC is the positive desired value of slope compensation in A/µs (note that the Electrical Characteristics gives this value as a negative unit)
- f_{SW} is the switching frequency in kHz

For additional guidance on selecting slope compensation values, see Section 10.2.2.9 in the application section.

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9.3.9.4 Frequency Compensation

External frequency compensation is required for the TPS7H401x. There are several industry techniques used to compensate DC-DC regulators. For the TPS7H401x, type 2A compensation is most often recommended though other approaches are acceptable. See Section 10.2.2.10 in the application section for a specific example.

9.4 Device Functional Modes

The device uses fixed frequency, peak current mode control. As a synchronous buck converter, the device normally operates in continuous current mode under all load conditions. The output voltage is divided down through external resistors and VSNS+ is compared to an internal voltage reference by an error amplifier, which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference, which is compared to the high-side power switch current. When the power switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on.

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TPS7H4012 is a radiation hardened synchronous buck converter. The device is utilized to convert a higher DC input voltage to a lower DC output voltage at a maximum of 6A. It can be used over an input voltage range of 4.5V to 14V.

10.2 Typical Application

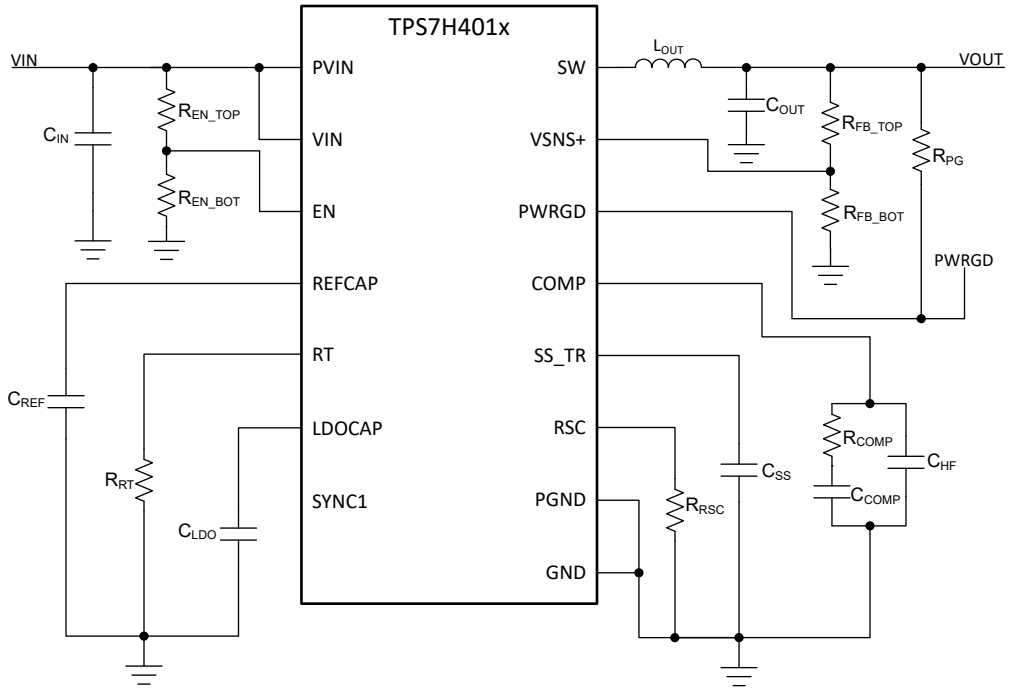

Figure 10-1. Typical Application Schematic

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10.2.1 Design Requirements

Table 10-1. Design Parameters

DESIGN PARAMETER	DESIGN VALUE
Input voltage	12V ± 5%
Output voltage	3.3V ± 1.5%
Maximum output current	6A
Transient response 5A load step	ΔVOUT = 2.5%
Output voltage ripple	20mVpp
Start input voltage (rising V_{IN})	10V
Switching frequency	500kHz

10.2.2 Detailed Design Procedure

10.2.2.1 Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade off between higher and lower switching frequencies. Higher switching frequencies may produce a smaller solution size by allowing lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which hurt the converter's efficiency and thermal performance. In this design, a switching frequency of 500kHz is selected. Using Equation 6, an RT resistor of 90.9kΩ is selected.

10.2.2.2 Output Inductor Selection

To calculate the value of the output inductor, use Equation 10. K_L is a coefficient that represents the amount of inductor ripple current relative to the maximum output current, I_{OUT}, as shown in Equation 9. Since the output capacitors must have a ripple current rating greater than or equal to the inductor ripple current, choosing a high inductor ripple current impacts output capacitors selection. In general, the inductor ripple value is at the discretion of the designer depending on specific system needs. Typical values for K_L range from 10% to 50%. For low output currents, the value of K_L could be increased to reduce the value of the output inductor.

$$K_L = \frac{I_{ripple}}{I_{OUT}} \tag{9}$$

$$L = \frac{VIN_{(max)} - VOUT}{I_{OUT} \times K_L} \times \frac{VOUT}{VIN_{(max)} \times f_{SW}} \tag{10}$$

For this design example, use K_L = 35% and $VIN_{(max)}$ = 12.6V (12V + 5%). The calculated inductor value is 2.32µH and the closest available inductor of 2.2µH is selected. The resulting ripple current can be calculated using Equation 11. It is found to be 2.2A for this design.

$$\Delta I_L = \frac{VIN_{(max)} - VOUT}{L} \times \frac{VOUT}{VIN_{(max)} \times f_{SW}} \tag{11}$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS current can be found from Equation 12 and peak inductor current can be found from Equation 13.

$$I_{L(rms)} = \sqrt{{I_{OUT}}^2 + \frac{1}{12} \times \left(\frac{VOUT \times \left(VIN_{(max)} - VOUT \right)}{VIN_{(max)} \times L \times f_{SW}} \right)^2} \tag{12}$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{L(ripple)}}{2} \tag{13}$$

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For this design, the RMS inductor current is 6A, and the peak inductor current is 7.11A. To satisfy this requirement, a Wurth 74439346022 inductor is selected. This inductor has a saturation current rating of 19.5A and an RMS current rating of 10.6A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the previously calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the maximum switch current limit, rather than the peak inductor current.

It is suggested to ensure the typical current limit value is at least 25% higher than the peak inductor current to make sure there is sufficient margin before the current limit is engaged. The typical current limit of 9.7A meets these requirements.

10.2.2.3 Output Capacitor Selection

There are several considerations in determining the value of the output capacitor. The selection of the output capacitor is driven by both the desired output voltage ripple, and the allowable voltage deviation due to a large, abrupt change in load current (load step). For space applications, the value of capacitance also has to account for the mitigation of single event effects (SEE). The output capacitance needs to be selected based on the more stringent of these three criteria. When selecting the capacitors, care should be taken to select capacitors with a sufficient voltage rating, temperature rating, and consideration of any effective capacitance changes due to DC bias effects. It is also important to note that the value of the output capacitor directly influences the modulator pole of the converter frequency response, as described in Section 10.2.2.10.

The first criteria to consider is the desired response to a load step. This generally occurs when the regulator is temporarily not able to supply sufficient output current during a large, fast increase in the current needs of the load. This may occur during a transition from no load to full load, or when powering an FPGA with large current swings. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. Equation 14 shows the minimum output capacitance, from the electrical point of view, necessary to accomplish this.

$$C_{OUT} \geq \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta VOUT} \tag{14}$$

Where ΔI_{OUT} is the change in output current, f_{SW} is the regulator switching frequency, and $\Delta VOUT$ is the allowable change in the output voltage. For this example, the transient load response is specified as a 2.5% change in VOUT for a load step of 5A. This results in a minimum capacitance of 242µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. However, for space applications and large capacitance values, tantalum capacitors are typically used, which have a certain ESR value to take into consideration.

The next criteria is to calculate the required capacitance to meet the output voltage ripple requirements using Equation 15 where $VOUT_{ripple(desired)}$ is the maximum allowable output voltage ripple, and ΔI_L is the inductor ripple current. In this case, the maximum desired output voltage ripple is 20mV, and the inductor ripple current is 2.2A. Under these conditions, a minimum capacitance value of 28µF is calculated.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \times f_{SW} \times VOUT_{ripple(desired)}} \tag{15}$$

Finally, the ESR of the capacitor must be considered when meeting the output voltage ripple requirements using Equation 16. It is determined that an ESR value of 9mΩ or less is required.

$$ESR \leq \frac{VOUT_{ripple(desired)}}{\Delta I_L} \tag{16}$$

Additional capacitance deratings for aging, temperature, and DC bias should be factored in, which increases the minimum required output capacitance value. Additionally, capacitors generally have limits to the amount of ripple

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current they can handle without failing or producing excess heat. The selected bank of output capacitors must handle the ripple current calculated in Equation 11.

For this specific design, taking into consideration all of the above requirements, 2x330µF T530 Tantalum capacitors are selected with a resulting combined ESR of 2.45mΩ at the 500kHz switching frequency. Additionally, a 22µF, 10µF, 1µF, and 100nF ceramic capacitors are added in parallel for high frequency filtering. This results in a total capacitance of 693.1µF.

Equation 17 can be used as an approximation to calculate the resulting output voltage ripple when considering both the capacitance and ESR. For this design, the resulting output ripple estimation is 6.2mV.

$$VOUT_{ripple} \approx \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} + ESR \times \Delta I_L \quad (17)$$

10.2.2.4 Input Capacitor Selection

The input supply to the TPS7H4012 must be well regulated with sufficient capacitor bypassing for proper electrical performance. While a minimum ceramic capacitor of at least 4.7µF effective capacitance near the PVIN and VIN inputs is required, additional bulk capacitance is generally required to handle the high input currents. Similar to the output capacitor selection, when selecting the input capacitors, care should be taken to select capacitors with a sufficient voltage rating, temperature rating, and consideration of any effective capacitance changes due to DC bias effects. The capacitor must also have a ripple current rating greater than the maximum input current ripple as calculated using Equation 18. For this design, I_{CINrms} is calculated to be 2.7A.

$$I_{CINrms} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times \left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} \quad (18)$$

The minimum input capacitance can then be calculated by using Equation 19 and selecting a maximum desired input ripple voltage, $\Delta VIN_{desired}$. For this design, a 20mV input voltage ripple maximum is used, resulting in a minimum input capacitance of 150µF.

$$C_{IN} \geq \frac{I_{OUT} \times 0.25}{\Delta VIN_{desired} \times f_{SW}} \quad (19)$$

Note, however, that Equation 19 does not include the effects of ESR on the input ripple voltage. Therefore, additional capacitance is utilized. Specifically, 5x100µF Tantalum capacitors are used along with 2x22µF, 2x10µF, 2x4.7µF, and 1x0.1µF ceramic capacitors are selected for a total input capacitance of 573.5µF.

10.2.2.5 Soft-Start Capacitor Selection

The soft-start capacitor C_{SS}, determines the amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is large (as is typical with space grade buck converters), which would require a large amount of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS7H401x reach the current limit, draw excessive current from the input power supply, or cause the input voltage rail to sag. Limiting the output voltage slew rate solves these problems. The soft-start capacitor value can be calculated using Equation 7.

A reasonable soft start time for many space grade buck regulators is 5.8ms, which results in a C_{SS} capacitor of 22nF.

10.2.2.6 Rising VIN Set Point (Configurable UVLO)

An external resistor divider from VIN to GND is used to enable the TPS7H4012 when a desired preset input voltage is reached. In effect, this acts as an adjustable UVLO. First, 10V is selected as the desired turn-on voltage ($VIN_{(rising)}$). Next, R_{EN_TOP} of 54.2kΩ is selected as a reasonable tradeoff between a large enough resistor to minimize power dissipation, but low enough to prevent excessive noise coupling to a high impedance node. Equation 4 is then used to calculate an R_{EN_BOT} of 3.52kΩ.

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Since the enable pin has hysteresis, the resulting turn-off voltage can be calculated using Equation 5. It is found that the $VIN_{falling}$ is 8.36V. This means that once the regulator starts switching after rising above 10V ($VIN_{(rising)}$), it will continue switching until falling below 8.36V.

10.2.2.7 Output Voltage Feedback Resistor Selection

The resistor divider network R_{FB_TOP} and R_{FB_BOT} is used to set the output voltage. For this design, 10kΩ was selected for R_{TOP}. Additionally, a 50Ω resistor was placed in series with R_{FB_TOP} to aid in measuring the control loop. Using the combined value of 10.05kΩ and Equation 1, R_{BOTTOM} is calculated as 2.233kΩ. The nearest standard 0.1% resistor of 2.23kΩ was selected.

10.2.2.8 Output Voltage Accuracy

To determine the output voltage DC accuracy, the following sources of error are considered:

- V_{REF} within the Electrical Characteristics table is the predominant source of error. This encompasses the error due to the reference voltage and error amplifier offset. The across temperature minimum of 0.594V, maximum of 0.604V, and typical of 0.6V results in an accuracy of –1.00% and +0.67%. If this error is instead centered around an average reference voltage of 0.599V, the accuracy is calculated as ±0.83%.
- The V_{REF} specification in not measured in a switching, closed-loop configuration. Figure 7-26 can be used to see the effects of output current (load regulation) and switching. However, it is seen that across the complete 6A load, there is only a small deviation that is considered small enough such that load regulation is not included in this accuracy calculation.
- The external error due to the resistor tolerance of the R_{FB_TOP} and R_{FB_BOT} resistors need to be added. Since it is assumed the error is uncorrelated, it is decided to add the errors as a sum of squares. For the selected 0.1% tolerance R_{FB_TOP} and R_{FB_BOT} resistors, the total error is R(error) = sqrt($0.1\%^2$ + $0.1\%^2$) = ±0.14%.

Equation 20 is used to calculate the system error for output voltage accuracy.

$$System_{(error)} = V_{REF(error)} + R_{FB(error)} \tag{20}$$

The negative system error calculation is $System_{(error)}$ = –1.00% – 0.14% = –1.14% and the positive system error is $System_{(error)}$ = 0.67% + 0.14% = 0.81%. Therefore, the total system error is calculated to be –1.14%./+0.81. If the total system error is centered, this comes to ±0.975%. These each meet the 1.5% target.

Lifetime drift data could similarly be added. Group C data may be used to aid in this calculation. For this example, it is assumed the lifetime drift is minimal compared to the other sources of error and it is therefore not added.

10.2.2.9 Slope Compensation Requirements

While one may chose different values of slope compensation for different applications, a commonly suggested ideal value for slope compensation is defined as the output voltage divided by the inductor size as shown in Equation 21.

$$SC_{suggested} = \frac{di}{dt} = \frac{\Delta I_L}{\Delta t_{OFF}} = \frac{VOUT}{L} \tag{21}$$

For this design, the suggested value is 1.5A/µs. Using Equation 8, the suggested value of R_{SC} is calculated to be 634kΩ. However, in this specific application example, it was decided to have more slope compensation than suggested which provided additional margin and suitability of testing different configurations. Therefore, a value of 200kΩ is used which results in 3.2A/µs.

10.2.2.10 Compensation Component Selection

The control loop of the TPS7H4012 is described in Section 9.3.9. The component selection for compensating this device is as shown below. Other industry standard approaches for compensating a peak current mode control buck regulator are also acceptable.

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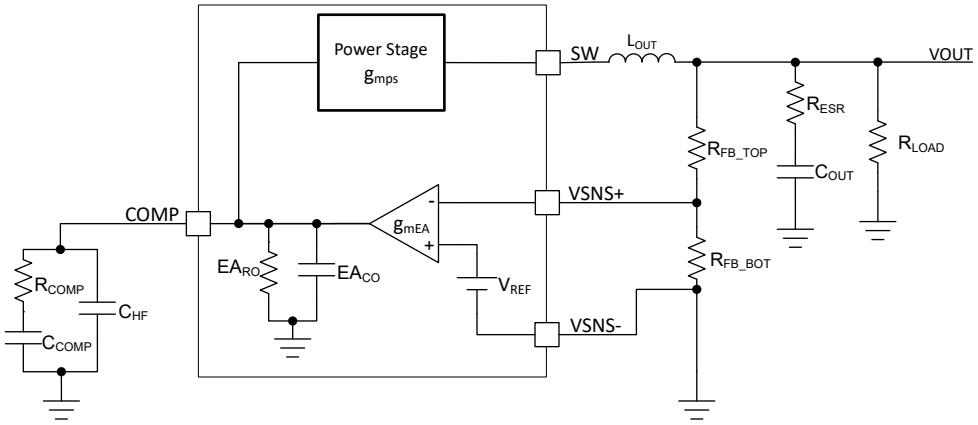

Figure 10-2. Type II Compensation With Simplified Loop

1. Determine the desired crossover frequency, $f_{CO(desired)}$. A good starting rule of thumb is to set the crossover frequency to one-tenth of the switching frequency. This will generally provide a good transient response and ensure that the modulator poles do not degrade the phase margin. For this design, a more conservative crossover frequency target of 33kHz was selected.
2. Determine the required gain from the compensated error amplifier using Equation 22:

$$A_{VM} = \frac{2\pi \times f_{CO(desired)} \times C_{OUT}}{g_{mps}} \quad (22)$$

   where g_{mps} is the power stage transconductance for the selected current limit. For this design with $f_{CO(desired)}$ = 33kHz, C_{OUT} = 693.1µF, g_{mps} = 11.2S, a value for A_{VM} of 12.8V/V is obtained.
3. R_{COMP} can be determined by Equation 23:

$$R_{COMP} = \frac{A_{VM}}{g_{mEA}} \times \frac{VOUT}{V_{REF}} \quad (23)$$

   where gm_{EA} is the transconductance of the error amplifier (1650µS typ) and V_{REF} is the reference voltage (0.6V typ). A value of 42.77kΩ is calculated and a nearby standard resistor of 42.7kΩ was selected.
4. Calculate the power stage dominate pole determined by Equation 24:

$$f_{P,PS} = \frac{I_{OUT}}{2\pi \times C_{OUT} \times VOUT} \quad (24)$$

   For this design, the dominate pole is calculated to be at 0.42kHz.
5. Place a compensation zero at the dominant pole by selecting C_{COMP} as determined by Equation 25:

$$C_{COMP} = \frac{1}{2\pi \times f_{P,PS} \times R_{COMP}} \quad (25)$$

   For this design, C_{COMP} is calculated to be 8.93nF and a nearby standard capacitor value of 8.2nF was selected.
6. Calculate the ESR zero from the output capacitor bank by Equation 24:

$$f_{1,ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (26)$$

   For this design, the ESR zero is calculated to be at 93.73kHz.
7. C_{HF} is used to cancel the zero from the equivalent series resistance (ESR) of the output capacitor C_{OUT}. It is calculated using Equation 27:

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$$C_{HF} = \frac{1}{R_{COMP} \times 2\pi \times f_{Z,ESR}} \quad (27)$$

Note that if the ESR zero is higher than half the switching frequency, use half the switching frequency instead of the ESR zero in Equation 27. For this design, C_{HF} is calculated to be 39.77pF and a nearby standard capacitor value of 22pF was selected.

Note that the components selected using these equations are often only starting values in a design. Optimizations can be made after lab testing to further improve the frequency response and ensure a closer match to the desired crossover frequency.

Note

For device models, see the TPS7H4012-SEP Design tools & simulation, TPS7H4012-SP Design tools & simulation, TPS7H4013-SEP Design tools & simulation, and TPS7H4013-SP Design tools & simulation webpages.

10.2.2.11 Schottky Diode

A Schottky diode may be connected from SW to PGND. This provides a low impedance path for the inductor current during dead time. A Schottky diode can help mitigate reference voltage drift, especially when operating at higher currents and higher switching frequencies. A Schottky diode can also help improve efficiency. Select a diode with low or no reverse recovery time for optimal efficiency and performance. True Schottky diodes have no reverse recovery time.

While a Schottky diode is good design practice, it is not required for the TPS7H4012 and TPS7H4013. However, it is recommended to ensure any resulting voltage reference variation is acceptable for a given application.

10.2.3 Application Curve

Typical plots are shown for the following conditions:

- VIN = PVIN = 12V
- VOUT = 3.3V
- IOUT = 6A
- Switching frequency = 500kHz

Graph Placeholder

Figure 10-3. Switch Node Waveform and Output Voltage Ripple

Graph Placeholder

Crossover Frequency = 22kHz, Phase Margin = 81°, Gain Margin = 23dB

Figure 10-4. Bode Plot

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10.2.4 Inverting Buck-Boost

The TPS7H401x can be configured as an inverting buck-boost in order to create a negative output voltage as shown in Figure 10-5.

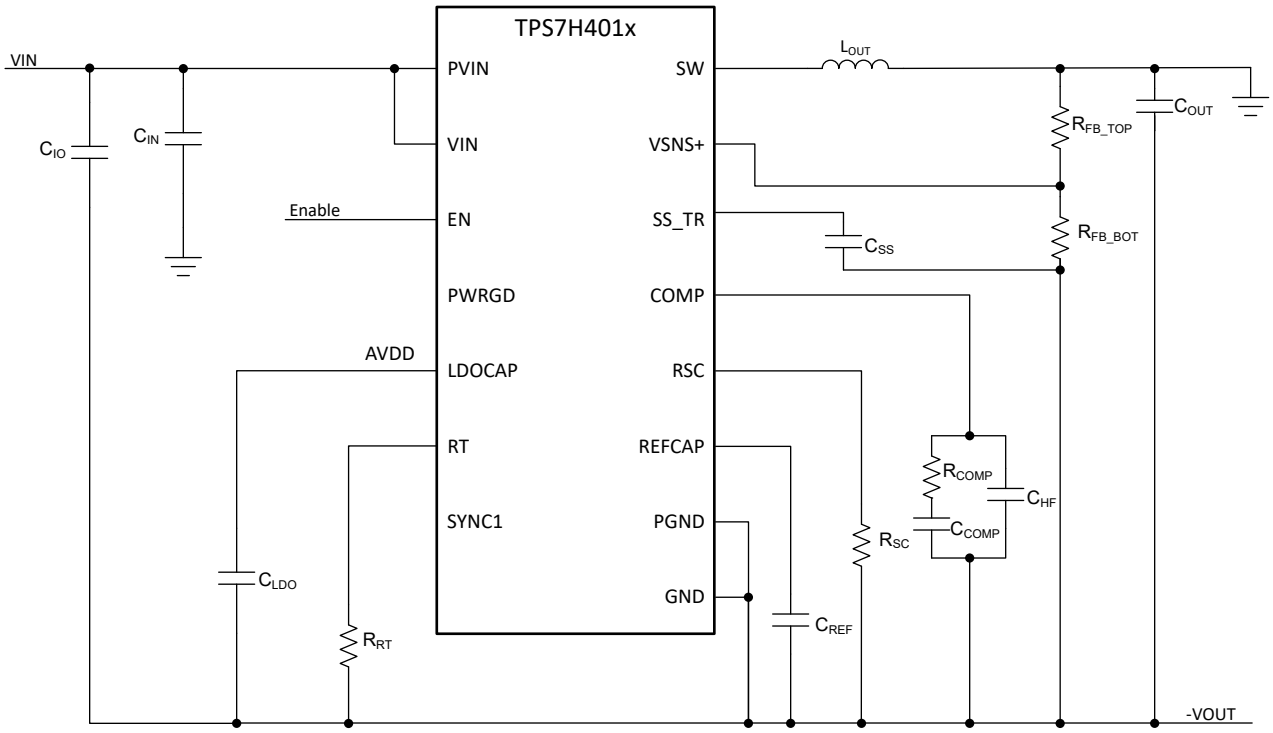

Figure 10-5. Simplified Schematic of Inverting Buck-Boost

Additional considerations for designing an inverting buck-boost are described in the application note, Working With Inverting Buck-Boost Converters. While many details and equations are provided within the application note, a few considerations for the TPS7H401x are as follows:

- Ensure the recommended maximum input voltage of 14V is followed. This means VIN + |VOUT| ≤ 14V. For example, an inverting buck-boost configured from 5V to –5V is acceptable (10V differential) but 12V to –12V would not be acceptable (24V differential).
- Be sure the current limit supports the application . The average inductor current for an inverting buck-boost is greater than the load current. This may result in higher peak currents than expected when compared to a buck converter. Additionally, this means that the average inductor current must be kept lower than the TPS7H4012 recommended maximum of 6A and TPS7H4013 maximum of 3A.
- C_{IO} in the Figure 10-5 is the standard input capacitor that would be utilized in a buck converter. C_{IN} is an input capacitor with respect to system ground which provides a low impedance path at the regulator input.
- Be sure that device logic input pins such as EN never exceed the recommended maximum rating of 7V. For example, if EN was driven to 5V from an external source and the inverting buck-boost is configured for a –5V output, this would apply 10V to EN (with respect to the device GND pin) which would exceed the rating. Take care with selecting the input voltage signals to avoid this condition. Alternatively, logic shift the signals so they are referenced with respect to -VOUT (which is the device GND pin).

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10.3 Power Supply Recommendations

The TPS7H401x is designed to operate from an input voltage supply range between 4.5V and 14V. This supply voltage must be well regulated. Power supplies must be well bypassed for proper electrical performance. This includes a minimum of one 4.7µF (after derating) ceramic capacitor, type X7R or better from PVIN to GND, and from VIN to GND. PVIN and VIN must be the same voltage, and it is recommended to externally connect PVIN and VIN. Additional local ceramic bypass capacitance may be required in systems with small input ripple specifications, as well as additional bulk capacitance if the TPS7H401x device is located more than a few inches away from its input power supply. Bypass capacitors should be placed as close as possible to the input pins, and have a low impedance path to GND.

Larger values of bypass capacitance at the output will improve the response to radiation induced transients.

10.4 Layout

10.4.1 Layout Guidelines

- Layout is a critical portion of good power supply design. See *Layout Example* for a PCB layout example.
- It is recommended to include a large topside area filled with ground. This top layer ground area should be connected to the internal ground layers using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS7H401x device in order to provide a thermal path from the exposed thermal pad to ground. The topside ground area together with the internal ground plane must provide adequate heat dissipating area.
- It is recommended that the thermal pad under the TPS7H401x is tied to GND on internal ground layers utilizing vias. The thermal pad does not need to directly connect to ground on the top layer in order to provide noise isolation between the thermal pad ground and the topside PGND, which may be noisy.
- There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supply's performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X7R dielectric.
- Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.
- The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with an X7R dielectric. Make sure to connect this capacitor to the quieter analog ground trace (if utilized) rather than the power ground trace of the PVIN bypass capacitor.
- Since the SW connection is the switching node, the output inductor should be located close to the SW pins and the PCB conductor area minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- It is critical to keep the feedback trace away from inductor EMI and other noise sources. Run the feedback trace as far from the inductor, switch (SW) node, and noisy power traces as possible. Avoid routing this trace directly under the output inductor if possible. If not possible, ensure that the trace is routed on another layer with a ground layer separating the trace and inductor.
- Keep the resistive divider used to generate the VSNS+ voltage as close to the device pin as possible in order to reduce noise pickup.
- The RT and COMP pins are sensitive to noise, so components around these pins should be located as close as possible to the IC and routed with minimal trace lengths.
- Make all of the power (high current) traces as short, direct, and thick as possible.
- It may be possible to obtain acceptable performance with alternate PCB layouts.

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10.4.2 Layout Example

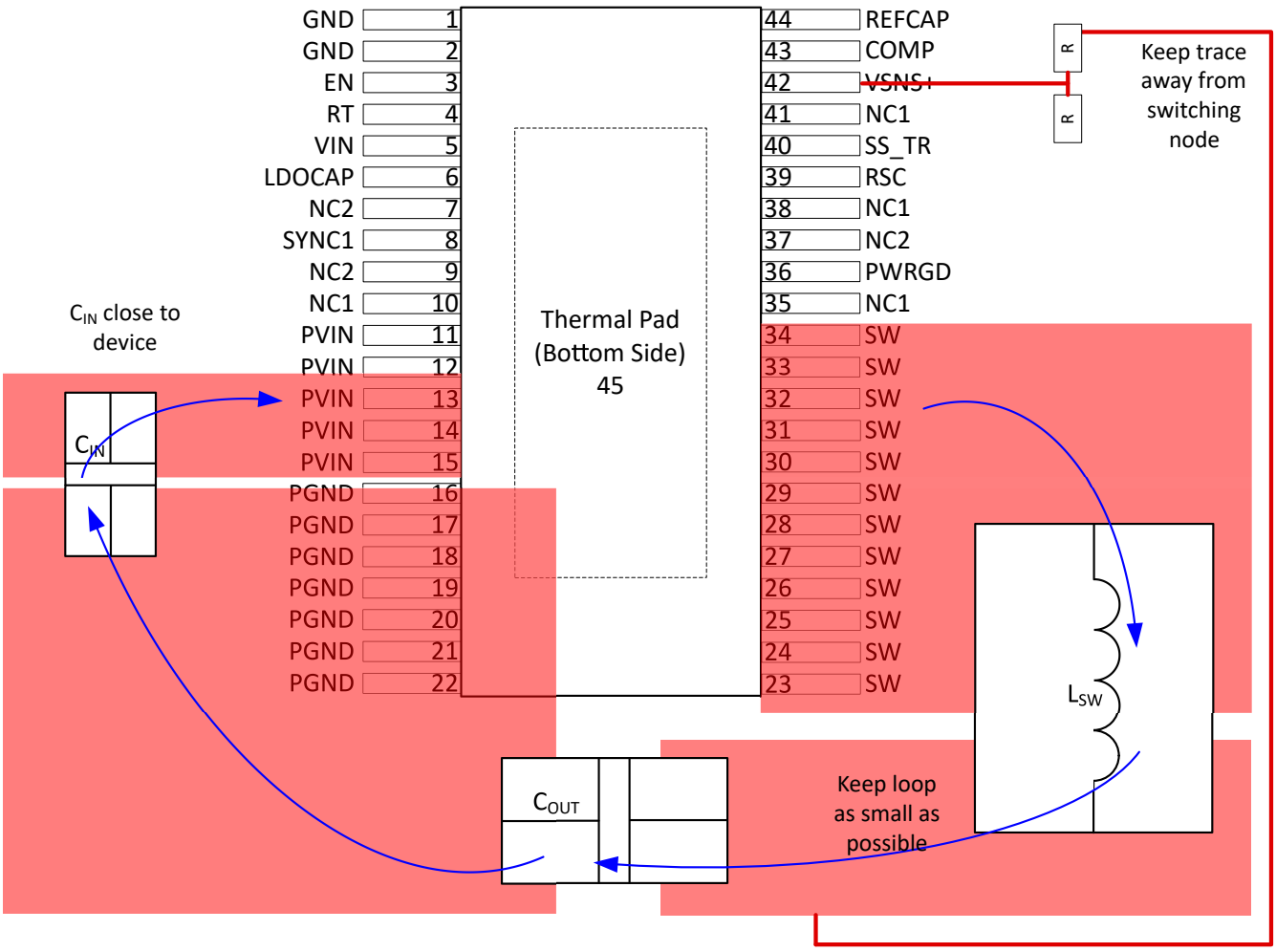

Figure 10-6. Simplified Layout Example

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11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Related Documentation

- Standard Microcircuit Drawing, 5962R21221

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

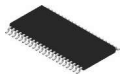
13.1 Mechanical Data

ADVANCE INFORMATION

ADVANCE INFORMATION

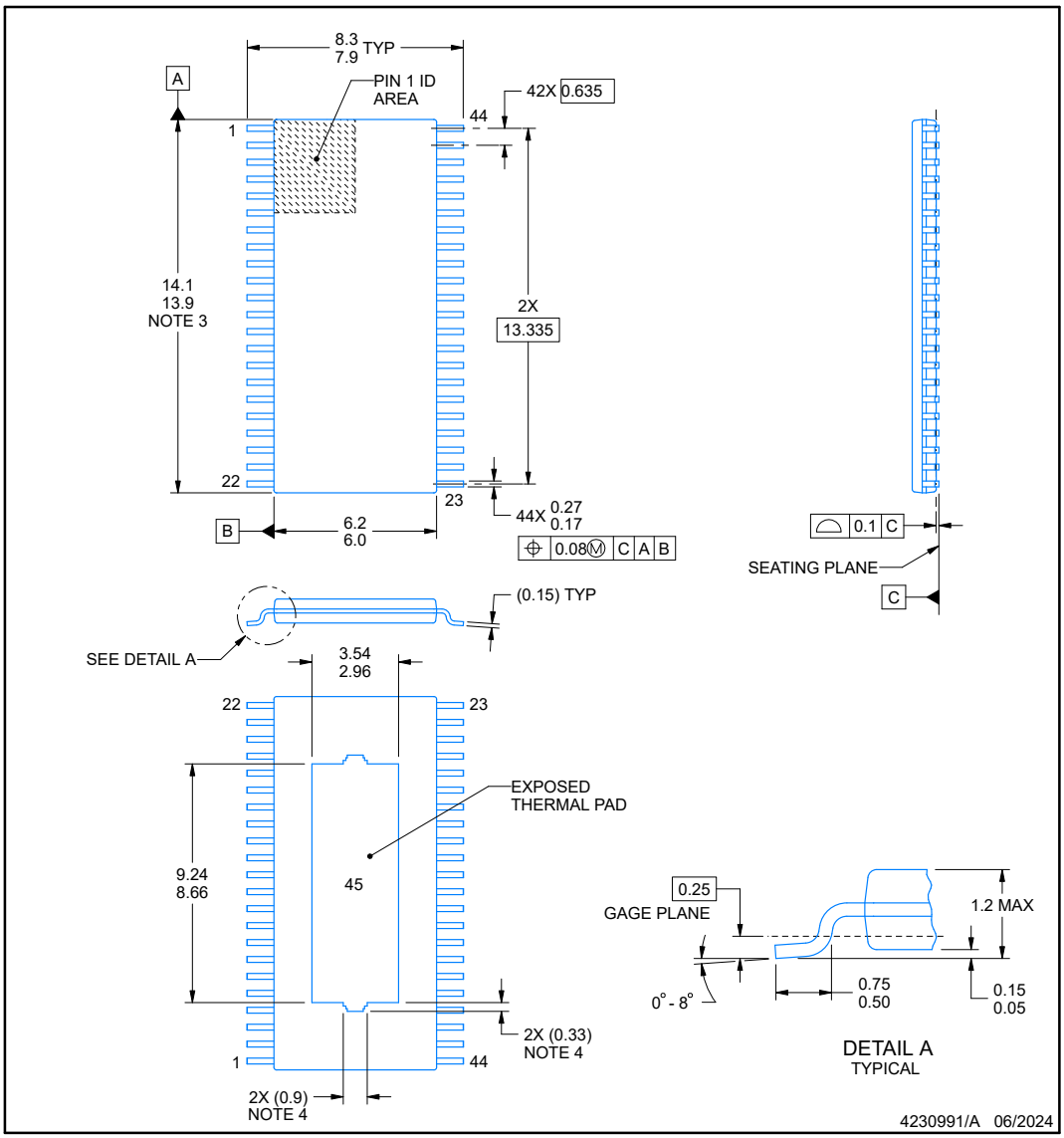
PACKAGE OUTLINE

DDW0044G



PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Features may differ or may not be present.

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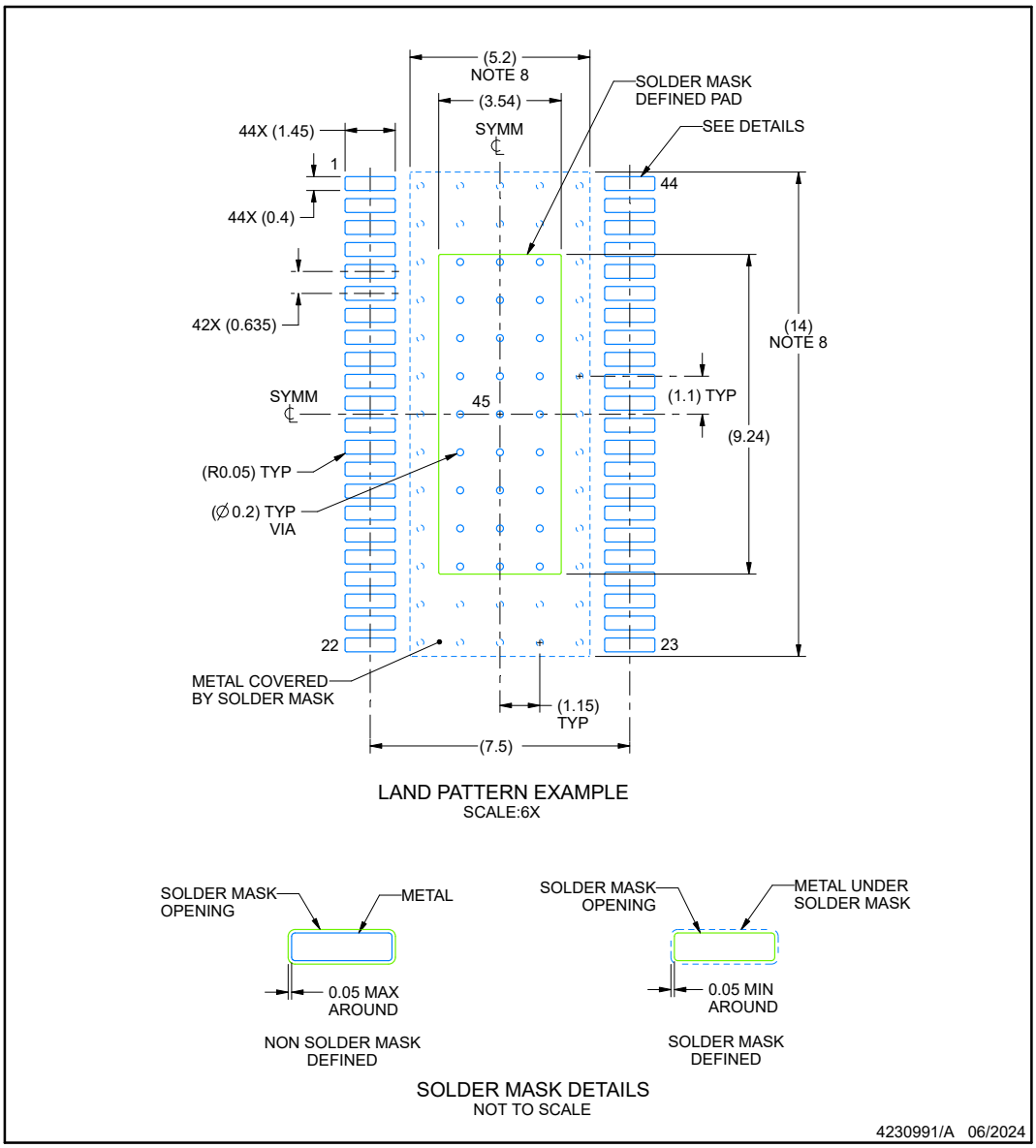
EXAMPLE BOARD LAYOUT

DDW0044G — **PowerPAD ™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.

ADVANCE INFORMATION

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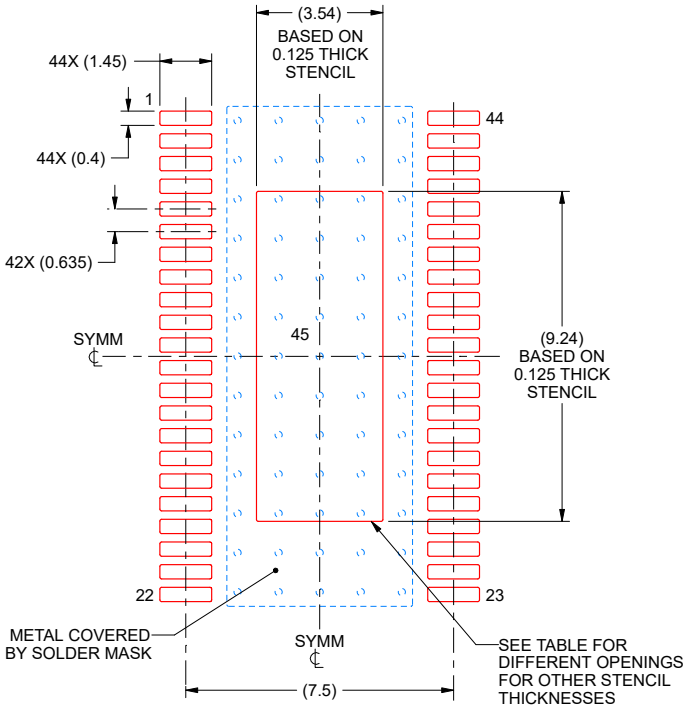
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DDW0044G — **PowerPAD ™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.96 X 10.33
0.125	3.54 X 9.24 (SHOWN)
0.15	3.23 X 8.44
0.175	2.99 X 7.81

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7H4012MDDWSEP	Active	Preproduction	HTSSOP (DDW) | 44	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	
PTPS7H4013MDDWSEP	Active	Preproduction	HTSSOP (DDW) | 44	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

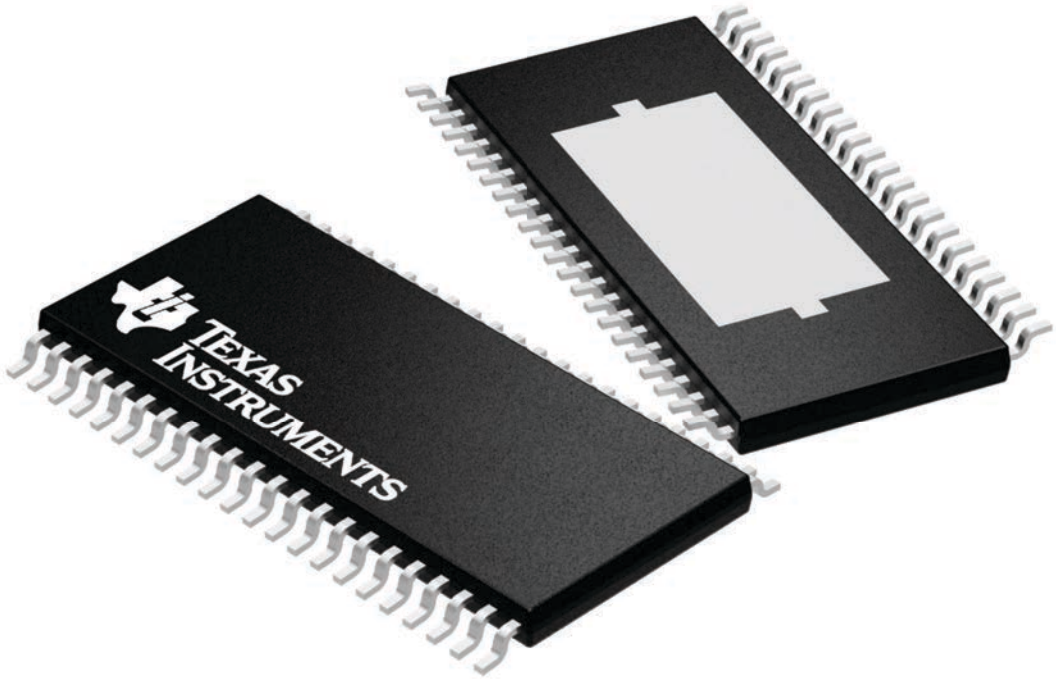
DDW 44

PowerPAD TSSOP - 1.2 mm max height

6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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