TPS7H3301-SP Sink and Source Radiation-Hardened 3-A DDR Termination Regulator With Built-In VTTREF Buffer

1 Features

- 5962R14228 (1):
  - Radiation hardness assurance (RHA) qualified to total ionizing dose (TID) 100 krad(Si)
  - Single event latch-up (SEL), single event gate rupture (SEGR), single event burnout (SEB) immune to LET = 70 MeV-cm^2/mg(2)
  - Single event transient (SET), single event functional interrupt (SEFI), and single event upset (SEU) characterized to 70 MeV-cm^2/mg(2)
- Supports DDR, DDR2, DDR3, DDR3L, and DDR4 termination applications
- Input voltage: supports a 2.5-V and 3.3-V rail(3)
- Separate low-voltage input (VLDOIN) down to 0.9 V for improved power efficiency(3)
- 3-A sink and source termination regulator includes droop compensation
- Enable input and power-good output for power supply sequencing
- VTT termination regulator
  - Output voltage range: 0.5 to 1.75 V
  - 3-A sink and source current
- Integrated precision voltage divider network with sense input
- Remote sensing (VTTSNS)
- VTTREF buffered reference
  - 49% to 51% accuracy with respect to VDDQSNS (±3 mA)
  - ±10-mA sink and source current
- Undervoltage lockout (UVLO) and overcurrent limit (OCL) functionality integrated

2 Applications

- Command and data handling (C&DH)
- Optical imaging payload
- Radar imaging payload

3 Description

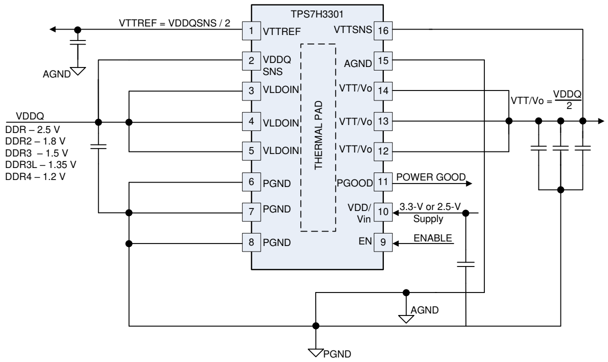
The TPS7H3301-SP is a TID and SEE radiation-hardened double data rate (DDR) 3-A termination regulator with built-in VTTREF buffer. The regulator is specifically designed to provide a complete, compact, low-noise solution for space DDR termination applications such as single board computers, solid state recorders, and payload processing.

The TPS7H3301-SP supports DDR VTT termination applications using DDR, DDR2, DDR3, DDR4. The fast transient response of the TPS7H3301-SP VTT regulator allows for a very stable supply during read/write conditions. During transients, the fast tracking feature of the VTTREF supply minimizes any voltage offset between VTT/Vo and VTTREF. To enable simple power sequencing, both an enable input and a power-good output (PGOOD) have been integrated into the TPS7H3301-SP. The PGOOD output is open-drain so it can be tied to multiple open-drain outputs to monitor when all supplies have come into regulation. The enable signal can also be used to discharge VTT/Vo during suspend to RAM (S3) power down mode.

Device Information (1)

PART NUMBER(3)	GRADE	PACKAGE
5962R1422801VXC(2)	Flight Grade RHA 100 krad(Si)	16-Pin CFP 9.60 mm × 11.00 mm Weight: 1.55 g(5)
5962-1422801VXC(2)	Flight Grade QMLV	
TPS7H3301HKR/EM	Engineering Module(4)	
TPS7H3301EVM-CVAL	Ceramic Evaluation Board	EVM

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) See *Radiation Report* for details.
(3) Applicable to DDR2, DDR3, DDR3L and DDR4. For DDR, input voltage = 3.3-V nominal. V_{IN} is 2.95 to 3.5 V for DDR1 and $V_{LDOIN} > V_{TT}/V_O$ for all DDRs.
For DDR2 3-A load condition, V_{IN} is 2.45 to 3.5 V.
V_{IN} headroom: $V_{IN\_MIN} \geq V_{TT}/V_O + 1.5$ V.
(4) These units are intended for engineering evaluation only. They are processed to a noncompliant flow (that is, no burn-in, and so forth) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.
(5) Weight is accurate to ±10%.



Standard DDR Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2020) to Revision C (September 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Electrical characteristics are tested in ambient conditions of -55ºC to 125ºC, previous reference to T_J is updated to T_A	7
• VTTSNS test condition to show -5mA test condition and updated limits; additional VTTSNS test conditions and limits at 5mA and -1A to 1A	7
• Clarified specification name VLDOIN-VTT/V_O to V_{DO}, removed Note1	7
• Production testing coverage for V_{DO} (VLDOIN-VTT/V_O) implemented across temperature, Note 2 has been removed for test conditions previously appended with Note 2	7
• Updated I_{VOSCRL} limits and test conditions for I_{VOSRCL} and I_{VOSNCL}	7
• Production testing coverage of R_{DSCHRG} implemented across temperature	7
• Clarified test condition description for $V_{TH(PG)}$	7
• Removed VDDQSNS voltage range from Electrical Characterisitics table as this is contained in the Recommended Operating Conditions table	7
• Updated V_{VTTREF} name to $V_{VTTREF(load\_reg)}$ and added new accuracy spec, $V_{VTTREFaccuracy}$	7
• Clarified test conditions for $I_{VTTREFSRCL}$ & $I_{VTTREFSNCCL}$	7
• $V_{VINUVVIN}$ tested across temperature	7
• I_{ENLEAK} tested across temperature	7
• Removed Note for T_{SON}, note is redundant for typical specifications	7
• Revised reference to 100kΩ pull-up resistor	14
• Updated power dissipation calculation for VDD/V_{IN} and VLDOIN	26

Changes from Revision A (June 2016) to Revision B (June 2020)	Page
• Changed DLA drawing number	1
• Changed radiation performance feature summary	1
• Changed feature description for supported DDR termination applications	1
• Changed VTTREF accuracy feature	1
• Changed description of supported DDR applications	1
• Added package weight to Device Information table	1

- Changed pin name references throughout document to be consistent ... 4
- Added additional thermal metrics... 6
- Added clarification of T_J temperature range in *Electrical Characteristics* table... 7
- Changed ambiguous tolerance specification for VTT/V_O to explicitly specify min/max range... 7
- Changed UVLO threshold hysteresis to own table entry ... 7
- Changed naming on VTTREF plots for consistency ... 10
- Added ceramic to capacitor description to meet stability requirements... 14
- Added correct cross reference for output current limit... 14
- Changed wording for clarity for V_{IN}/VDD ... 17
- Changed comment to reflect total ESR ... 17
- JEDEC specification references ... 19
- Changed to improved transient plot and description... 19
- Added or smaller for layout thermal via size ... 25
- Changed to improved recommended layout diagram. ... 25

5 Pin Configuration and Functions

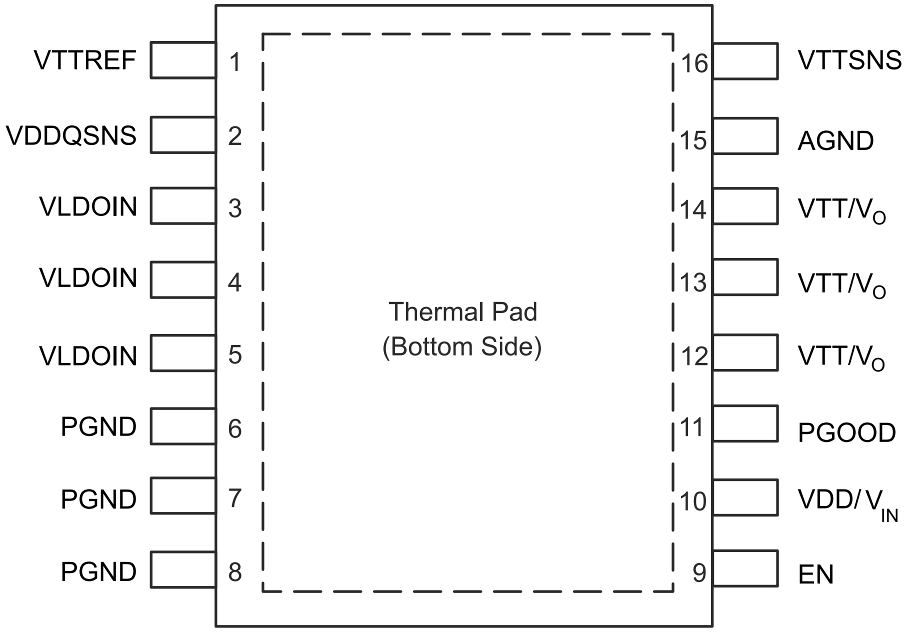


Figure 5-1. HKR Package, 16-Pin CFP (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VTTREF	1	O	Reference output. Connect to GND through 0.1-μF ceramic capacitor.
VDDQSNS	2	I	VDDQ sense input. Reference input for VTTREF.
VLDOIN	3 4 5	I	Supply voltage for the LDO. Connect to VDDQ voltage or an alternate voltage source.
PGND	6 7 8	—	Power ground. Connect output for the VTT/V_O LDO to negative pin of the output capacitor.
EN	9	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device.
VDD/V_{IN}	10	I	2.5- or 3.3-V power supply. A ceramic decoupling capacitor with a value between 1 and 10 μF is required.
PGOOD	11	O	PGOOD output pin. PGOOD pin is an open drain output to indicate the output voltage is within specification.
VTT/V_O	12 13 14	O	Power output for VTT/V_O LDO.
AGND	15	—	Signal ground. Connect to negative pin of output capacitors.(1)
VTTSNS	16	I	Voltage sense for VTT/V_O. Connect to positive pin of the output capacitor or the load.

(1) Thermal pad and package lid are internally connected to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature, unless otherwise noted[1]

			MIN	MAX	UNIT
	Input voltage[2]	VDD/V_{IN}, VLDOIN, VTTSNS, VDDQSNS	–0.36	3.6	V
		EN	–0.3	3.6	
		PGND to AGND	–0.3	0.3	
	Output voltage[2]	VTT/V_O, VTTREF	–0.3	3.6	V
		PGOOD	–0.3	3.6	
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground (AGND) pin unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

All voltage values are with respect to the network ground (AGND) pin unless otherwise noted

		MIN	NOM	MAX	UNIT
Supply voltage	VDD/V_{IN}	2.375		3.5	V
Voltage	VLDOIN	0.9		3.5	V
	EN, VTTSNS	–0.1		3.5	
	VDDQSNS	1		3.5	
	VTT/V_O, PGOOD	–0.1		3.5	
	VTTREF	–0.1		1.8	
	PGND	–0.1		0.1	
T_J	Operating junction temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(2) (1) (3)		TPS7H3301-SP HKR (CFP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.54	°C/W

(1) Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(3) Maximum power dissipation may be limited by overcurrent protection.

6.5 Electrical Characteristics

Over full temperature range, T_A = –55°C to 125°C, VDD/V_{IN} = 3.3 V and 2.375 V (for VDD/V_{IN} > VLDOIN), VLDOIN = 1.8 V, VDDQSNS = 1.8 V, VTTSNS = 0.9 V, EN = VDD/V_{IN}, *Standard DDR Application* unless otherwise noted. All voltage values are with respect to the network ground (AGND) pin unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{VDD/Vin}$	Supply current	EN = 3.3 V, no load			18	30	mA
$I_{VDD(SDN)}$	Shutdown current	EN = 0 V, VDDQSNS = 0, no load			3	5	mA
		EN = 0 V, VDDQSNS > 0.78 V, no load			6.5	8	
I_{VLDOIN}	Supply current of VLDOIN	EN = 3.3 V, no load			575	1200	µA
$I_{VLDOIN(SDN)}$	Shutdown current of VLDOIN	EN = 0 V, no load			50	100	µA
INPUT CURRENT							
$I_{VDDQSNS}$	Input current, VDDQSNS	EN = 3.3 V			4	6	µA
V_{TT}/V_O OUTPUT							
VTTSNS	Output DC voltage, V_{TT}/V_O	I_{VTT} = 5 mA	VDDQSNS = VLDOIN 2.5 V (DDR1)	1.219	1.25	1.276	V
			VDDQSNS = VLDOIN 1.8 V (DDR2)	0.889	0.9	0.921	
			VDDQSNS = VLDOIN 1.5 V (DDR3)	0.743	0.75	0.769	
			VDDQSNS = VLDOIN 1.35 V (DDR3L)	0.668	0.67	0.691	
			VDDQSNS = VLDOIN 1.2 V (DDR4)	0.593	0.6	0.617	
		I_{VTT} = -5 mA	VDDQSNS = VLDOIN 2.5 V (DDR1)	1.22	1.25	1.272	V
			VDDQSNS = VLDOIN 1.8 V (DDR2)	0.89	0.9	0.923	
			VDDQSNS = VLDOIN 1.5 V (DDR3)	0.744	0.75	0.767	
			VDDQSNS = VLDOIN 1.35 V (DDR3L)	0.669	0.675	0.691	
			VDDQSNS = VLDOIN 1.2 V (DDR4)	0.594	0.6	0.616	
		-1 A ≤ I_{VTT} ≤1 A	VDDQSNS = VLDOIN 2.5 V (DDR1)	1.219	1.26	1.301	V
			VDDQSNS = VLDOIN 1.8 V (DDR2)	0.879	0.91	0.933	
			VDDQSNS = VLDOIN 1.5 V (DDR3)	0.734	0.76	0.781	
			VDDQSNS = VLDOIN 1.35 V (DDR3L)	0.655	0.69	0.708	
			VDDQSNS = VLDOIN 1.2 V (DDR4)	0.58	0.6	0.633	
V_{DO}	Dropout voltage, V_{DO} = VLDOIN - VTTREF. V_{DO} recorded when VTTREF - VTT = 50 mV	VDDQSNS = 2.5 V (DDR1)	I_{VTT} = 0.5 A		50	230	mV
			I_{VTT} = 1 A		101	300	
			I_{VTT} = 2 A		209	400	
		VDDQSNS = 1.8 V (DDR2)	I_{VTT} = 0.5 A		54	230	
			I_{VTT} = 1 A		108	300	
			I_{VTT} = 2 A		228	400	
		VDDQSNS = 1.5 V (DDR3)	I_{VTT} = 0.5 A		52	230	
			I_{VTT} = 1 A		104	300	
			I_{VTT} = 2 A		216	400	
		VDDQSNS = 1.35 V (DDR3)	I_{VTT} = 0.5 A		50	230	
			I_{VTT} = 1 A		102	300	
			I_{VTT} = 2 A		212	400	
		VDDQSNS = 1.2 V (DDR4)	I_{VTT} = 0.5 A		50	230	
			I_{VTT} = 1 A		102	300	
			I_{VTT} = 2 A		210	400	

6.5 Electrical Characteristics (continued)

Over full temperature range, T_A = –55°C to 125°C, VDD/V_{IN} = 3.3 V and 2.375 V (for VDD/V_{IN} > VLDOIN), VLDOIN = 1.8 V, VDDQSNS = 1.8 V, VTTSNS = 0.9 V, EN = VDD/V_{IN}, *Standard DDR Application* unless otherwise noted. All voltage values are with respect to the network ground (AGND) pin unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VTT/$V_{O(TOL)}$	Output voltage tolerance to VTTREF	$I_{VTT/VO}$ = –3 A, across VDD/V_{IN} voltage range		12	25	34	mV
		$I_{VTT/VO}$ = 3 A, across VDD/V_{IN} voltage range		–34	–25	–12	
I_{VOSRCL}	VTT/V_O source current limit	Ramp output 0 A to 10 A, record current when VTT reaches lowest value		3.25		8	A
I_{VOSNCL}	VTT/V_O/VTT sink current limit	Ramp output 0 A to -10 A, record current when VTT reaches highest value		3.5		10	A
R_{DSCHRG}	Discharge impedance	VDDQSNS = 0 V, VTT/V_O = 0.3 V, EN = 0 V			18	25	Ω
POWER-GOOD COMPARATOR							
$V_{TH(PG)}$	VTT/V_O PGOOD threshold	PGOOD window lower (falling) threshold with respect to V_{VTTREF}		–23.5%	–20%	–17.5%	
		PGOOD window upper (rising) threshold with respect to V_{VTTREF}		17.5%	20%	23.5%	
		PGOOD hysteresis			5%		
$T_{PGSTUPDLY}$	PGOOD start up delay	Start up rising edge, VTTSNS within 15% of V_{VTTREF}			2		ms
$V_{PGOODLOW}$	Output low voltage	I_{SINK} = 4 mA				0.4	V
$T_{PBADDLY}$	PGOOD bad delay	VTTSNS is outside of the ±20% PGOOD window			1		µs
$I_{PGOODLK}$	Leakage current	VTTSNS = VTTREF (PGOOD high impedance), PGOOD = VDD/V_{IN} + 0.2 V				1	µA
VDDQSNS AND VTTREF OUTPUT							
$V_{VDDQSNS\_UVLO}$	VDDQSNS undervoltage lockout	V_{DDQSNS} rising			780		mV
$V_{VDDQSNSUVHYS}$	VDDQSNS undervoltage lockout hysteresis				20		mV
V_{VTTREF}	VTTREF voltage				VDDQSNS / 2		V
$VTTREF_{(load\_reg)}$	Load reg ΔVTTREF	–10 mA < I_{VTTREF} < 10 mA	VDDQSNS = 2.5 V	–15		15	mV
			VDDQSNS = 1.8 V	–15		15	
			VDDQSNS = 1.5 V	–15		15	
			VDDQSNS = 1.35 V	–15		15	
			VDDQSNS = 1.2 V	–15		15	
$VTTREF_{accuracy}$	VTTREF voltage tolerance to VDDQSNS	–10 mA < I_{VTTREF} < 10 mA	VDDQSNS = 2.5 V	49%		51%	
			VDDQSNS = 1.8 V	49%		51%	
			VDDQSNS = 1.5 V	49%		51.25%	
			VDDQSNS = 1.35 V	49%		51.5%	
			VDDQSNS = 1.2 V	49%		51.5%	
		–3 mA < I_{VTTREF} < 3 mA	VDDQSNS = 1.5 V	49%		51%	
			VDDQSNS = 1.35 V	49%		51%	
			VDDQSNS = 1.2 V	49%		51%	
$I_{VTTREFSRCL}$	V_{VTTREF} source current limit	Sourcing current ramped from 0 A to 55 mA. Find when VTTREF drops to half of its original value.		10	40		mA
$I_{VTTREFSNCCL}$	V_{VTTREF} sink current limit	Sinking current ramped from 0 A to 16.5 mA. Find when VTTREF hits peak value.		12	15		mA
$I_{VTTREFDIS}$	VTTREF discharge current	EN = 0 V, VDDQSNS = 0 V, VTTREF = 0.5 V			1.3		mA
UVLO/EN LOGIC THRESHOLD							
$V_{VINUVVIN}$	UVLO threshold	Wakeup			2.18	2.25	V
$V_{VINUVVINHYS}$	UVLO threshold hysteresis	Hysteresis			50		mV
V_{ENIH}	High-level input voltage	Enable		1.7			V
V_{ENIL}	Low-level input voltage	Enable				0.3	V
V_{ENYST}	Hysteresis voltage	Enable			0.5		V
I_{ENLEAK}	Logic input leakage current	EN		–1		1	µA
THERMAL SHUTDOWN							

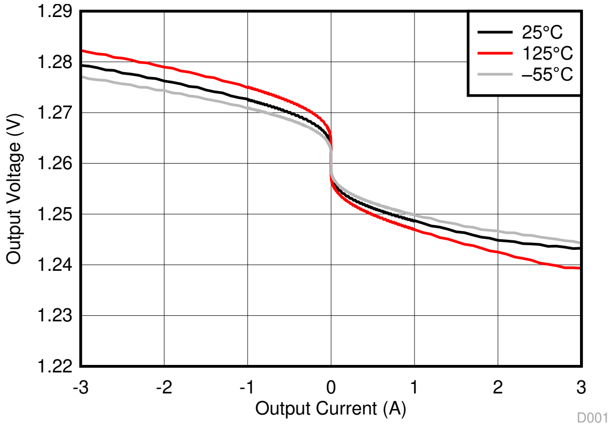
6.5 Electrical Characteristics (continued)

Over full temperature range, T_A = –55°C to 125°C, VDD/V_{IN} = 3.3 V and 2.375 V (for VDD/V_{IN} > VLDOIN), VLDOIN = 1.8 V, VDDQSNS = 1.8 V, VTTSNS = 0.9 V, EN = VDD/V_{IN}, *Standard DDR Application* unless otherwise noted. All voltage values are with respect to the network ground (AGND) pin unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SON}	Thermal shutdown threshold	Shutdown temperature		210		°C
		Hysteresis		12		

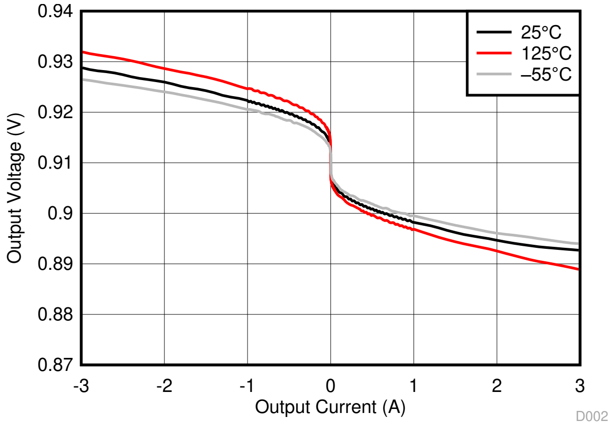
6.6 Typical Characteristics

For Figure 6-1 through Figure 6-10, (3 × 150-µF T530D157M010ATE005 tantalum + 4 × 4.7-µF MLCC) or equivalent capacitance/ESR are used on VTT output



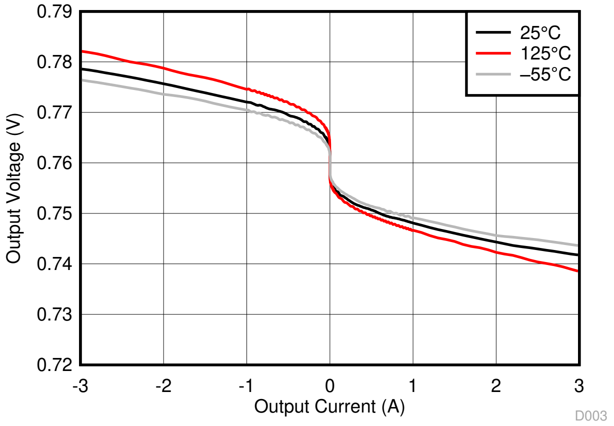
VDD/V_{IN} = 3.3 V VDDQSNS = 2.5 V

Figure 6-1. Output Voltage vs Output Current



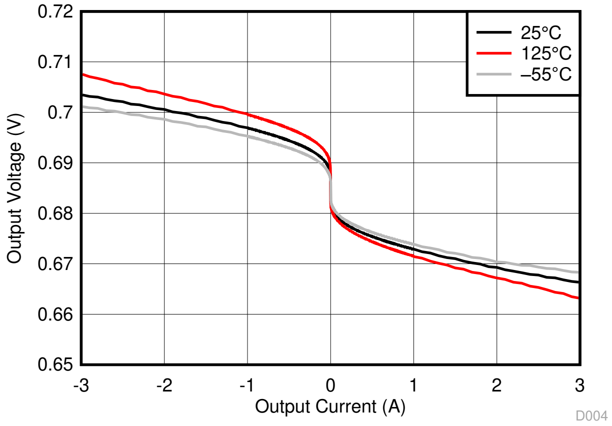
VDD/V_{IN} = 3.3 V VDDQSNS = 1.8 V

Figure 6-2. Output Voltage vs Output Current



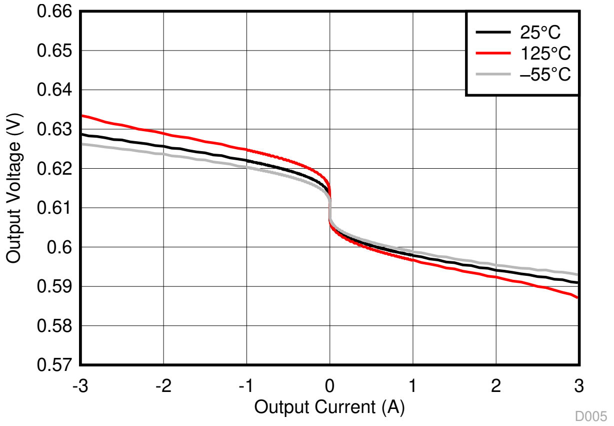
VDD/V_{IN} = 3.3 V VDDQSNS = 1.5 V

Figure 6-3. Output Voltage vs Output Current



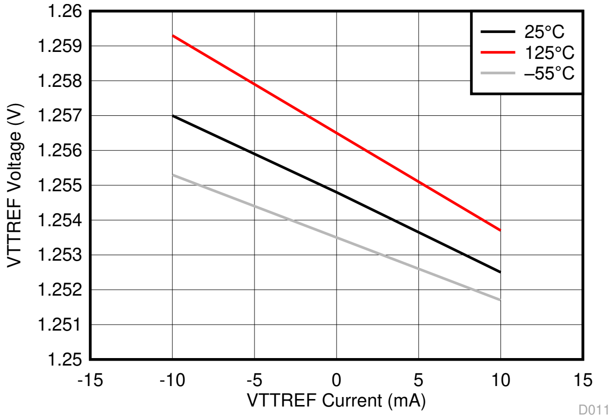
VDD/V_{IN} = 3.3 V VDDQSNS = 1.35 V

Figure 6-4. Output Voltage vs Output Current



VDD/V_{IN} = 3.3 V VDDQSNS = 1.2 V

Figure 6-5. Output Voltage vs Output Current

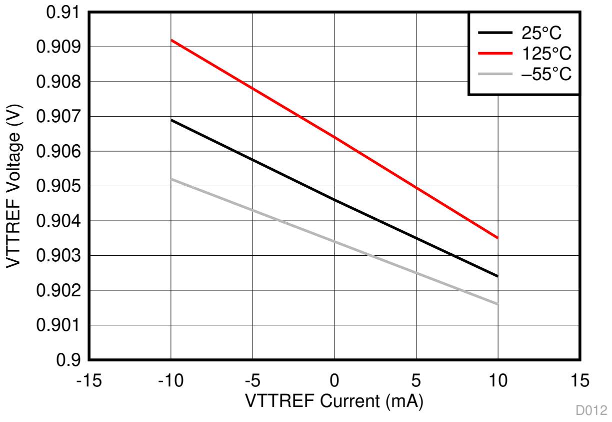


VDDQSNS = 2.5 V

Figure 6-6. VTTREF Voltage vs VTTREF Current

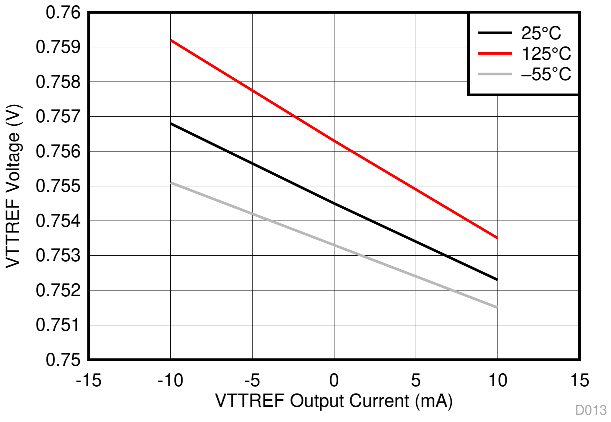
6.6 Typical Characteristics (continued)

For Figure 6-1 through Figure 6-10, (3 × 150-µF T530D157M010ATE005 tantalum + 4 × 4.7-µF MLCC) or equivalent capacitance/ESR are used on VTT output



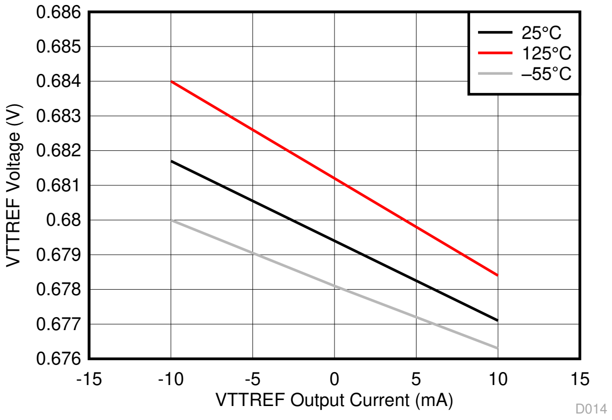
VDDQSNS = 1.8 V

Figure 6-7. VTTREF Voltage vs VTTREF Current



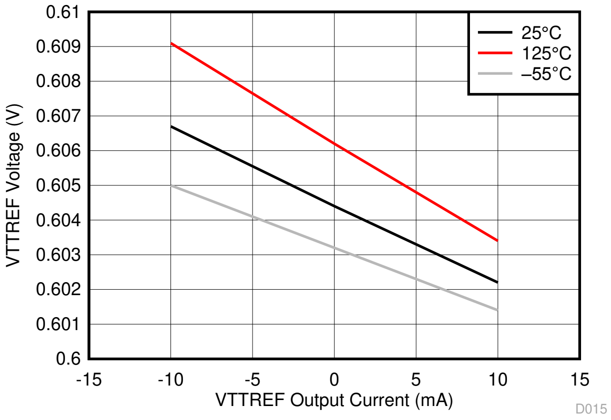
VDDQSNS = 1.5 V

Figure 6-8. VTTREF Voltage vs VTTREF Current



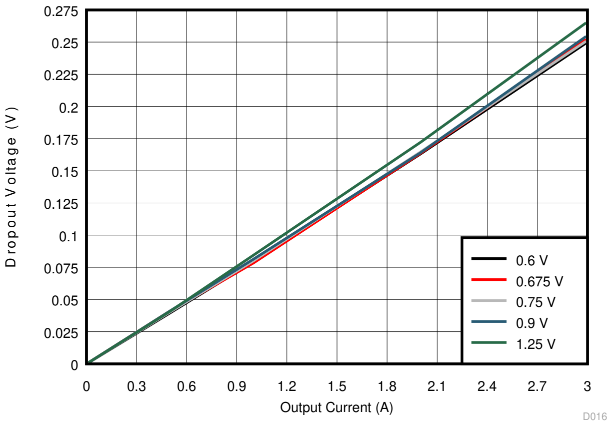
VDDQSNS = 1.35 V

Figure 6-9. VTTREF Voltage vs VTTREF Current



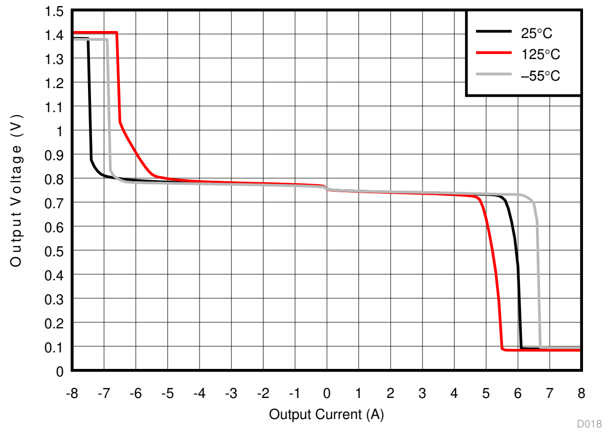
VDDQSNS = 1.2 V

Figure 6-10. VTTREF Voltage vs VTTREF Current



VDD/V_{IN} = 3.6 V

Figure 6-11. Dropout Voltage vs Output Current

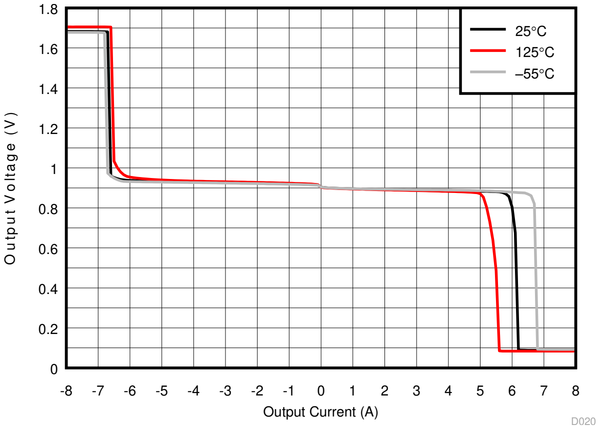


VDD/V_{IN} = 3.5 V VDDQSNS = 1.5 V

Figure 6-12. Output Voltage vs Output Current, DDR3

6.6 Typical Characteristics (continued)

For Figure 6-1 through Figure 6-10, (3 × 150-µF T530D157M010ATE005 tantalum + 4 × 4.7-µF MLCC) or equivalent capacitance/ESR are used on VTT output



VDD/V_{IN} = 3.5 V VDDQSNS = 1.8 V

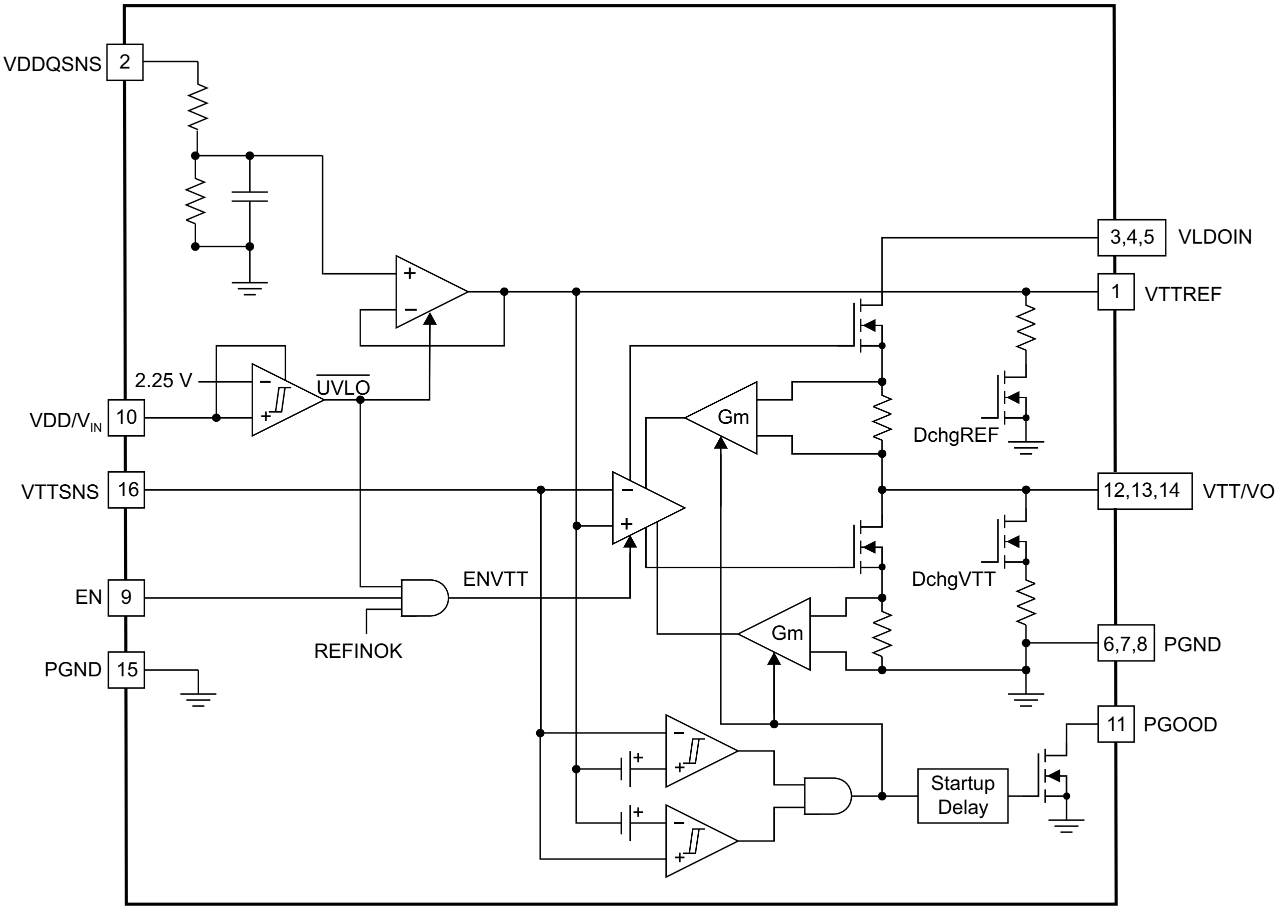
Figure 6-13. Output Voltage vs Output Current, DDR2

7 Detailed Description

7.1 Overview

The TPS7H3301-SP device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-noise systems where space and weight is a key consideration.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VTT/V_O Sink and Source Regulator

The TPS7H3301-SP is a 3-A sink and source tracking termination regulator specifically designed for low input voltage, and low external component count systems where space is a key application parameter. The TPS7H3301-SP integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sinking and sourcing current. The LDO regulator employs a fast feedback loop so that ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing pin (VTTSNS) should be connected to the positive pin of the output capacitor(s) as a separate trace from the high-current path of VTT/V_O.

The TPS7H3301-SP has a dedicated pin (VLDOIN) for VTT power supply to minimize the LDO power dissipation on user application. The minimum VLDOIN voltage is 400 mV above the 1/2 VDDQSNS voltage or as highlighted in *Section 6.5* (VLDOIN to VTT headroom) for various load conditions.

7.3.2 Reference Input (VDDQSNS)

The output voltage, VTT/V_O, is regulated to VTTREF. VDDQSNS incorporates an integrated resistor divider network. VDDQSNS should be connected to the memory supply bus (VDDQ). The TPS7H3301-SP supports

VDDQSNS voltage from 1 V to 3.5 V, making it versatile and ideal for many types of low-power LDO applications.

7.3.3 Reference Output (VTTREF)

When it is configured for DDR termination applications, VTTREF buffers the DDR VTT reference voltage for the memory application. The VTTREF block consists of an on-chip 1/2 resistor divider and a low-pass filter (LPF). VTTREF tracks 1/2 of VDDQSNS within 15 mV. It is capable of supporting both a sourcing and sinking load of 10 mA. VTTREF becomes active when VDDQSNS voltage rises to 0.78 V and VDD/V_{IN} is above the UVLO threshold. When VTTREF is less than 0.76 V, VTTREF is disabled and subsequently discharges to GND through an internal MOSFET. VTT/V_O is also discharged following the discharge of VTTREF. VTTREF is independent of the EN pin state. To meet stability criteria, a ceramic capacitor of 0.1-µF minimum must be installed close to VTTREF (pin1). Capacitor value at VTTREF (pin 1) must not exceed 2.2 µF.

7.3.4 EN Control (EN)

When EN is driven high, the TPS7H3301-SP VTT/V_O regulator begins normal operation. When EN is driven low, VTT/V_O discharges to GND through an internal 18-Ω MOSFET. VTTREF remains on when EN is driven low. EN is not tied high internally to prevent power sequencing issues with an external signal that may be controlling the enable. EN is a floating input and not internally tied, thus the user can have complete control over where and when the EN signal is generated. EN feeds directly into power-good (PGOOD). When enable is low, PGOOD is low.

7.3.5 Power-Good Function (PGOOD)

The TPS7H3301-SP provides an open-drain PGOOD output that goes high when the VTT/V_O output is within 20% of VTTREF (typ). PGOOD deasserts within 1 µs after the output exceeds the size of the power-good window. During initial VTT/V_O startup, PGOOD asserts high 2 ms (typ) after the VTT/V_O enters power-good window. Because PGOOD is an open-drain output, a 100kΩ pullup resistor between PGOOD and a stable active supply voltage rail is recommended for proper operation.

7.3.6 V_{TT} Current Protection

The LDO has a constant overcurrent limit (OCL). See Figure 6-13 for typical behavior across temperature.

7.3.7 V_{IN} UVLO Protection

For VDD/V_{IN} undervoltage lockout (UVLO) protection, the TPS7H3301-SP monitors VDD/V_{IN} voltage. When the VDD/V_{IN} voltage is lower than the UVLO threshold voltage, both the VTT and VTTREF regulators are powered off. This shutdown is a non-latch protection.

7.3.8 Thermal Shutdown

The TPS7H3301-SP monitors its junction temperature. If the device junction temperature exceeds its threshold value, (typically 210°C), the VTT/V_O and VTTREF regulators are both shutoff and discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

7.4 Device Functional Modes

The TPS7H3301-SP 3-A sink and source LDO provides low output noise to meet system needs. In order to improve efficiency in the LDO, TPS7H3301-SP LDO can operate from low VLDOIN voltage rail, thus using dual voltage source one for the VLDOIN that supports high-current and an alternate voltage source that provides voltage for VDDQSNS pin.

In some cases VLDOIN and VDDQSNS pins are tied together. In the memory system, VDDQ is a high-current supply that powers the core, the I/O, and the logic of the memory. VTTREF is a low-current, precision reference voltage that provides a threshold between a logic high (one) and a logic low (zero) that adapts to changes in the I/O supply voltage. By providing a precision threshold that adapts to the supply voltage, VTTREF realizes wider noise margins than those possible with a fixed threshold and normal variations in termination and drive impedance. Specifications vary for different DDR technologies. For example DDR3 JEDEC JESD79-3F specifies 0.49 to 0.51 times VDDQ and draws only tens to hundreds of microamps. The TPS7H3301-SP VTTREF is designed to sink and source up to 10 mA.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS7H3301-SP device is a highly-integrated sink and source LDO. The device is targeted to support VTT voltage for DDR memory applications and is capable of sourcing and sinking 3-A load current. The TPS7H3301-SP user's guide is available on www.ti.com, SLVUAK2. The guide highlights standard EVM test results, schematic, and bill of materials (BOM) for reference.

8.2 Typical Application

The design example describes a 2.5-V V_{IN}, DDR3 configuration.

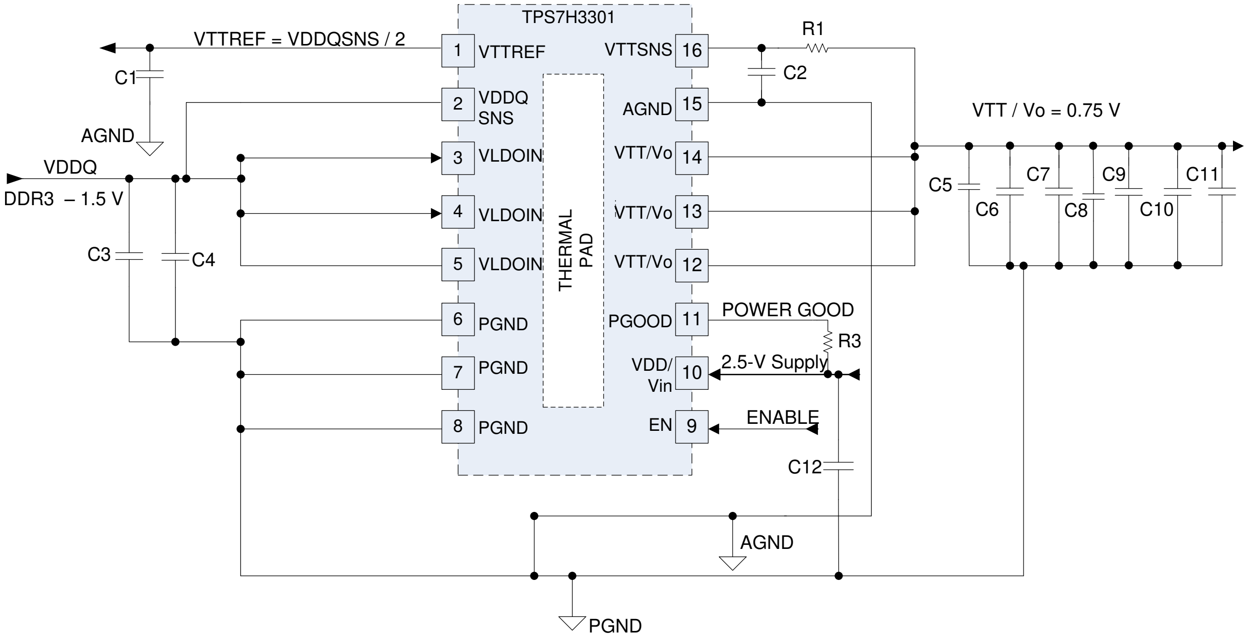


Figure 8-1. Typical Application Circuit

8.2.1 Design Requirements

See the *Section 6.3* for recommended limits.

8.2.2 Detailed Design Procedure

Table 8-1. Design Example 1 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1	Resistor	392 Ω	CRCW0603392RFKEA	
R3		100 kΩ	CRCW0603100KJNEA	
C3, C5, C6, C7	Capacitor	150 µF, 10 V	T530D157M010ATE005	Kemet
C2		1000 pF	GRM188R71H102KA01D	MuRata
C1		0.1 µF	08053C104KAT2A	AVX
C4, C8, C9, C10, C11		4.7 µF, 10 V	1210ZC475KAT2A	Murata
C12		10 µF, 10 V	GRM21BR71A106KE51L	Murata

8.2.2.1 VDD/V_{IN} Capacitor

Add a ceramic capacitor, with a value between 1- and 10-µF, placed close to the VDD/V_{IN} pin to minimize high frequency noise from the supply.

8.2.2.2 VLDO Input Capacitor

Depending on the trace impedance between the VLDOIN/VDDQ bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN/VDDQ input capacitor. Use a 150-µF (or greater) tantalum capacitor in parallel with a 4.7-µf ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VTT/V_O.

8.2.2.3 VTT Output Capacitor

For stable operation, the total capacitance of the VTT/V_O output pin must be greater than 470 µF. Attach three, 3 × 150-µF low-ESR tantalum capacitors in parallel with ceramic capacitors to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). If the total parallel ESR is greater than 2 mΩ, insert an R-C filter between the output and the VTTSNS input to achieve loop stability. The R-C filter time constant should be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

8.2.2.4 VTTSNS Connection

To achieve tight regulation with minimum effect of trace resistance, a remote sensing pin (VTTSNS) should be connected to the positive pin of the VTT pin output capacitor or capacitors as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor or capacitors is larger than 2 mΩ. The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

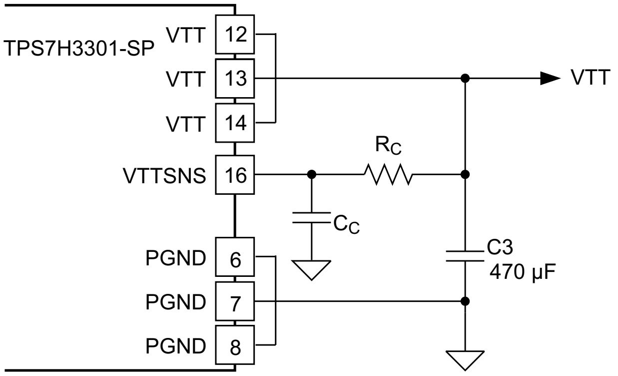


Figure 8-2. R-C Filter for VTTSNS

8.2.2.5 Low V_{IN} Applications

TPS7H3301-SP can be used in an application system where either a 2.5-V rail or a 3.3-V rail is available. The TPS7H3301-SP minimum input voltage requirement is 2.375 V. If a 2.5-V rail is used, ensure that the absolute minimum voltage (both DC and transient) at the device pin is 2.375 V or greater. The voltage tolerance for a 2.5-V rail input is between –5% and 5% accuracy, or better.

8.2.2.6 S3 and Pseudo-S5 Support

The TPS7H3301-SP provides S3 support by an EN function. The EN pin could be connected to an SLP_S3 signal in the end application. Both VTTREF and VTT/V_O are on when EN = high (S0 state). VTTREF is maintained while VTT/V_O is turned off and discharged via an internal discharge MOSFET when EN = low (S3 state). Please notice that the EN signal controls only the output buffer for VTT/V_O and therefore, while in S3 state, VDDQSNS is present in order to maintain data in volatile memory. As a result, when EN is set high to exit the S3 state, it is desired to bring V_O/VTT into regulation as fast as possible. This causes an output current controlled by the current limit of the device and the output capacitors.

When EN = low and the VDDQSNS voltage is less than 0.78 V, TPS7H3301-SP enters pseudo-S5 state. Both VTT/V_O and VTTREF outputs are turned off and discharged to GND through internal MOSFETs when pseudo-S5 support is engaged (S4/S5 state). Figure 8-3 shows a typical startup and shutdown timing diagram for an application that uses S3 and pseudo-S5 support.

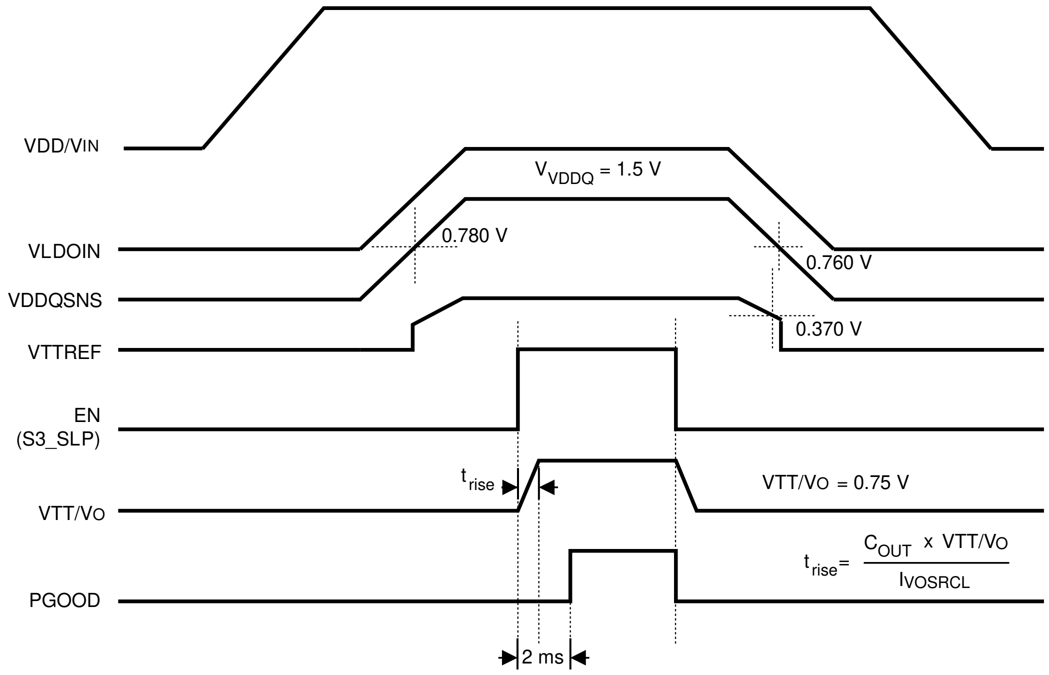


Figure 8-3. Typical Timing Diagram for S3 and Pseudo-S5 Support

8.2.2.7 Tracking Startup and Shutdown

The TPS7H3301-SP supports tracking startup of VDDQ and shutdown when EN is tied directly to the system bus and not used to turn on or turn off the device. During tracking startup, VTT/V_O follows VTTREF once VDDQSNS voltage is greater than 0.78 V. VDDQSNS incorporates a resistor divider network and a time constant of about 445 µs. The rise time of the VTT/V_O output is then a function of the rise time of VDDQSNS. If the VDDQSNS rise time is larger than 445 µs. PGOOD is asserted 2 ms after VTT/V_O is within ±20% of VTTREF. During tracking shutdown, VTT/V_O falls following VTTREF until VTTREF reaches 0.37 V. Once VTTREF falls below 0.37 V, the internal discharge MOSFETs are turned on and quickly discharge both VTTREF and VTT/V_O to GND. PGOOD is deasserted once VTT/V_O is beyond the ±20% range of VTTREF. Figure 8-4 shows the typical timing diagram for an application that uses tracking startup and shutdown.

There are no sequencing requirements between VDD/V_{IN} and VLDOIN. If VLDOIN is applied first followed by VDD/V_{IN} there is no issue. VDD/V_{IN} UVLO protection monitors VDD/V_{IN} voltage. When VDD/V_{IN} is lower than UVLO threshold both VTT and VTTREF regulators are powered off.

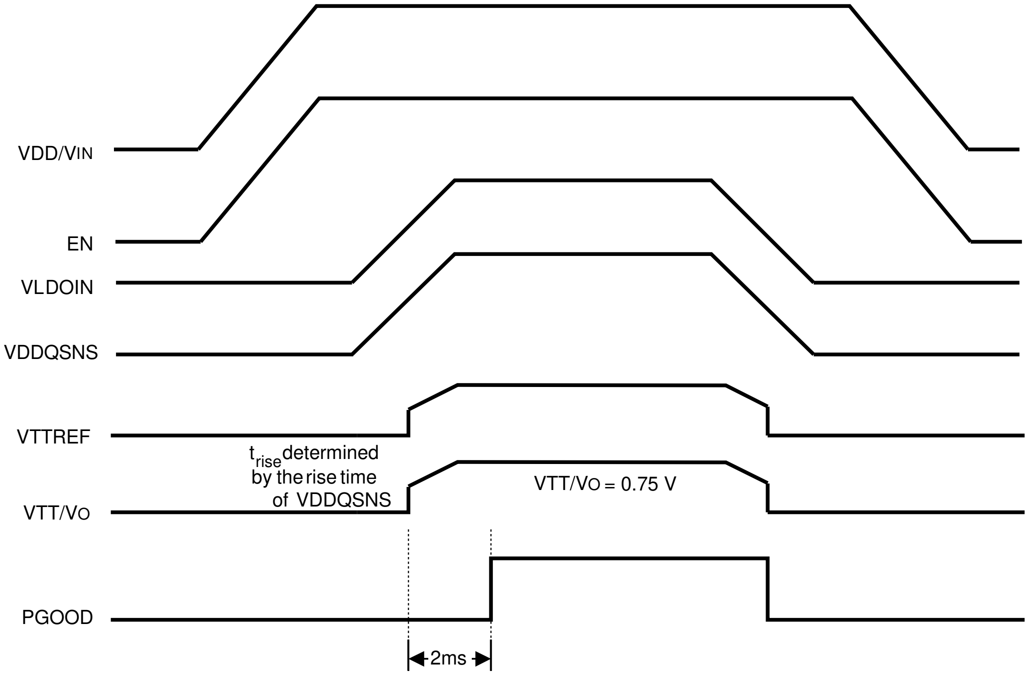


Figure 8-4. Typical Timing Diagram of Tracking Startup and Shutdown

8.2.2.8 Output Tolerance Consideration for VTT DIMM or Module Applications

The TPS7H3301-SP is specifically designed to power up the memory termination rail (as shown in Figure 8-5). The DDR memory termination structure determines the main characteristics of the VTT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. See Figure 8-6 for typical characteristics for a single memory cell.

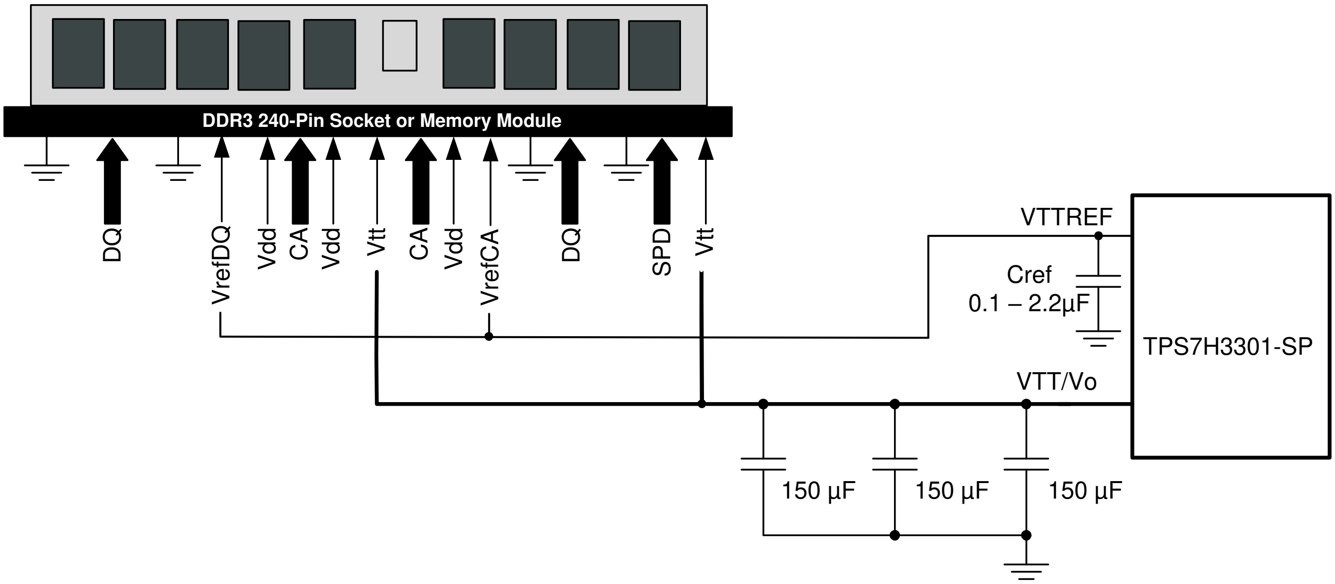


Figure 8-5. Typical Application Diagram for DDR3 VTT DIMM/Module Using TPS7H3301-SP

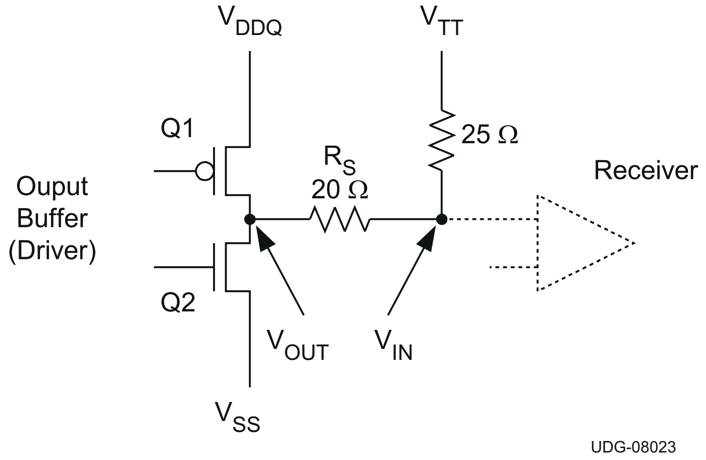


Figure 8-6. DDR Physical Signal System SSTL Signaling

In Figure 8-6, when Q1 is on and Q2 is off:

- Current flows from VDDQ via the termination resistor to VTT.
- VTT sinks current.

In Figure 8-6, when Q2 is on and Q1 is off:

- Current flows from VTT via the termination resistor to GND.
- VTT sources current.

Because VTT accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirement on VTT. Based on JEDEC VTT specifications for DDR and DDR2. See Table 8-2 for detailed information and JEDEC relevant specifications.

VTTREF – 40 mV < VTT < VTTREF + 40 mV, for both DC and AC conditions

The specification itself indicates that VTT must keep track of VTTREF for proper signal conditioning.

The TPS7H3301-SP ensures the regulator output voltage to be:

VTTREF – 34 mV < VTT < VTTREF + 34 mV, for both DC and AC conditions and –3 A < I_{VTT} < 3 A

The regulator output voltage is measured at the regulator side, not the load side. The tolerance is applicable to DDR, DDR2, DDR3 and low-power DDR3/DDR4 applications (see Table 8-2 for detailed information). To meet the stability requirement, a minimum output capacitance of 470 µF is needed, combination of both tantalum and ceramic capacitors. Considering the actual tolerance on the MLCC capacitors, four or higher 4.7-µF ceramic capacitors in parallel with 3 × 150-µF low-ESR tantalum capacitor are sufficient to meet the above requirement. Higher ESR tantalum capacitors will require multiple tantalum capacitors in parallel with ceramic capacitors to meet system needs.

Table 8-2. DDR, DDR2, DDR3, and LP DDR3 Termination Technology and Differences

	DDR	DDR2	DDR3	LOW POWER DDR3 (DDR3L)
FSB data rates	200, 266, 333 and 400 MHz	400, 533, 677 and 800 MHz	800, 1066, 1330 and 1600 MHz	Same as DDR3
Termination	Motherboard termination to VTT for all signals	On-die termination for data group. VTT/V_O used for termination of address, command and control signals.	On-die termination for data group. VTT/V_O used for termination of address, command and control signals.	Same as DDR3
Termination current demand	Max sink and source transient currents of up to 2.6 A to 2.9 A	Not as demanding • Only 34 signals (address, command, control) tied to VTT/V_O • ODT handles data signals Less than 1 A of burst current	Not as demanding • Only 34 signals (address, command, control) tied to VTT/V_O • ODT handles data signals Less than 1 A of burst current	Same as DDR3
Voltage level	2.5-V core and I/O 1.25-V VTT	1.8-V core and I/O 0.9-V VTT	1.5-V core and I/O 0.75-V VTT	1.35-V core and I/O 0.68-V VTT
Relevant JEDEC specification	JESD79F (SSTL_2 JESD8-9B)	DDR2 JESD79-2F (SSTL_18 JESD8-15)	DDR3 JESD79-3F	DDR3L JESD79-3-1A.01

The TPS7H3301-SP is designed as a Gm-driven LDO. The voltage droop between the reference input and the output regulator is determined by the transconductance and output current of the device. The typical Gm is 250 S at 3 A and changes with respect to the load in order to conserve the quiescent current (that is, the Gm is very low at no load condition). The Gm LDO regulator is a single pole system. Its unity gain bandwidth for the voltage loop is only determined by the output capacitance, as a result of the bandwidth nature of the Gm (see Equation 1).

$$F_{UGBW} = \frac{Gm}{2 \times \pi \times C_{OUT}} \tag{1}$$

where

- F_{UGBW} is the unity gain bandwidth
- Gm is transconductance
- C_{OUT} is the output capacitance

There are two limitations to this type of regulator when it comes to the output bulk capacitor requirement. To maintain stability, the zero location contributed by the ESR of the output capacitors should be greater than the –3-dB point of the current loop. This constraint means that higher ESR capacitors should not be used in the design. In addition, the impedance characteristics of the ceramic capacitor should be well understood in order to prevent the gain peaking effect around the Gm –3-dB point because of the large ESL, the output capacitor, and parasitic inductance of the VTT/V_O trace.

Figure 8-7 shows the bode plot simulation for a typical DDR3 configuration of the TPS7H3301-SP, where:

- VDD/V_{IN} = 2.4 V
- V_{VLDOIN} = 1.5 V
- VTT/V_O = 0.75 V
- I_{IO} = 2 A
- 3 × 150-μF low-ESR tantalum capacitors (T530D157M010ATE005) in parallel with 4 × 4.7-μF ceramic capacitor
- ESR = 1.66 mΩ
- ESL = 800 pH

The unity-gain bandwidth is approximately 87.3 kHz and the phase margin is 82°. The 0-dB level is crossed, the gain peaks because of the ESL effect. However, the peaking is kept well below 0 dB.

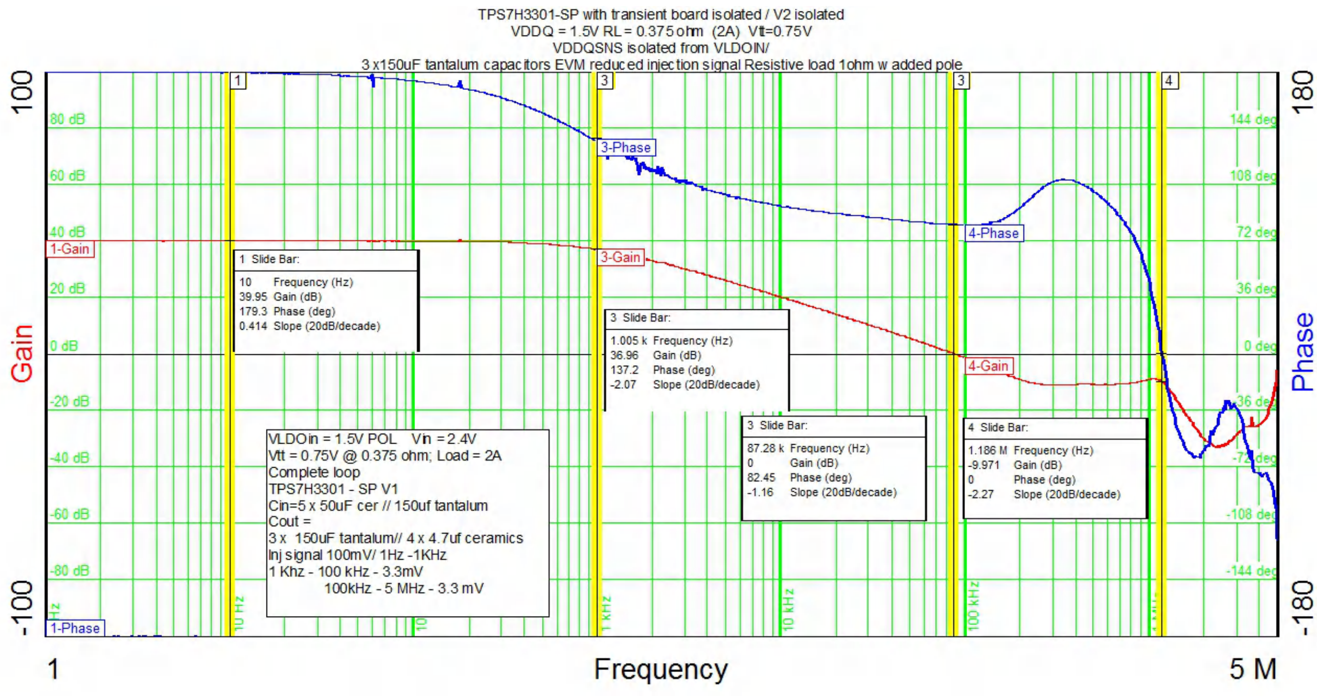


Figure 8-7. Bode Plot for a Typical DDR3 Configuration

Figure 6-3 shows the load regulation and Figure 8-8 shows the transient response for a typical DDR3 configuration. When the regulator is subjected to worst case ±3-A load step. The current shown only represents the device sourcing 3 A due to location of current probe.

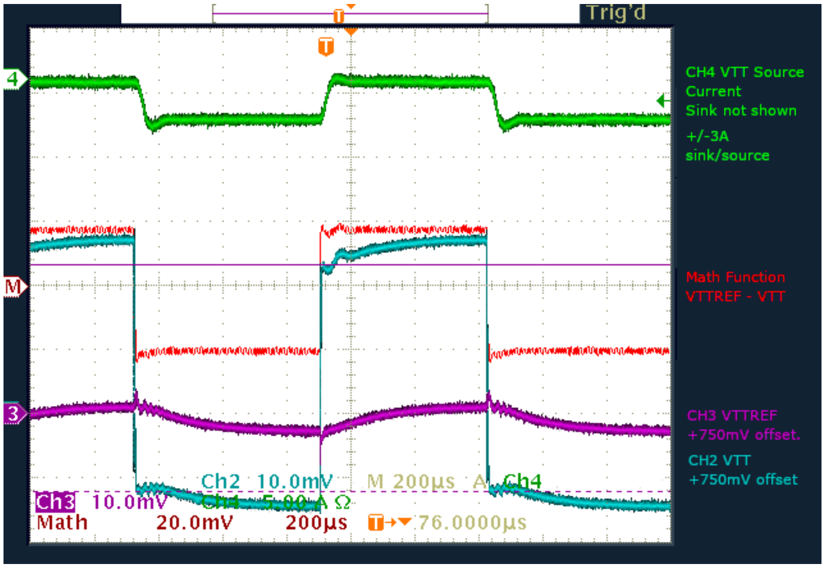


Figure 8-8. Transient Plot

8.2.2.9 LDO Design Guidelines

The minimum input (VLDOIN) to output voltage (VTT/V_O) difference (headroom) decides the lowest usable supply voltage Gm-driven to drive a certain load. For TPS7H3301-SP, a minimum of 300 mV ($VLDOIN_{MIN}$ – $VTT/V_{O\ MAX}$) is needed in order to support a Gm driven sourcing current of 3 A based on a design of VLDOIN = 3.3 V and C_{OUT} = 470 µF. Because the TPS7H3301-SP is essentially a Gm-driven LDO, its impedance characteristics are both a function of the 1/Gm and $R_{DS(on)}$ of the sourcing MOSFET (see Figure 8-9). The current inflection point of the design is between 3 A and 4 A. When I_{SRC} is less than the inflection point, the LDO is considered to be operating in the Gm region; when I_{SRC} is greater than the inflection point but less than the overcurrent limit point, the LDO is operating in the $R_{DS(on)}$ region. The typical sourcing $R_{DS(on)}$ is 154 mΩ with V_{IN} = 3 V and T_J = 125°C.

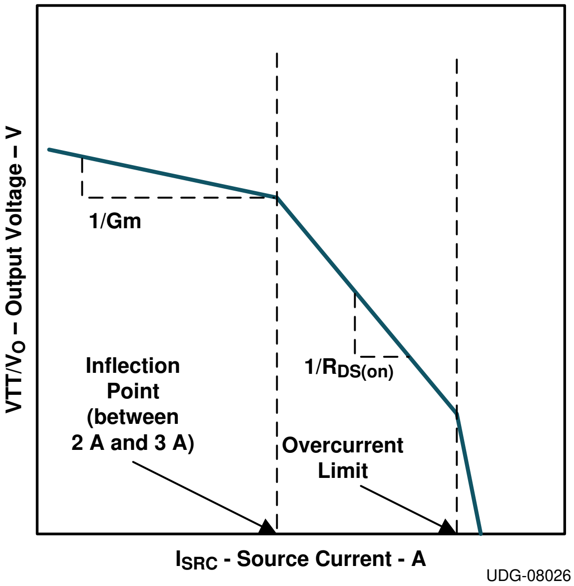


Figure 8-9. TPS7H3301-SP Impedance Characteristics

8.2.3 Application Curve

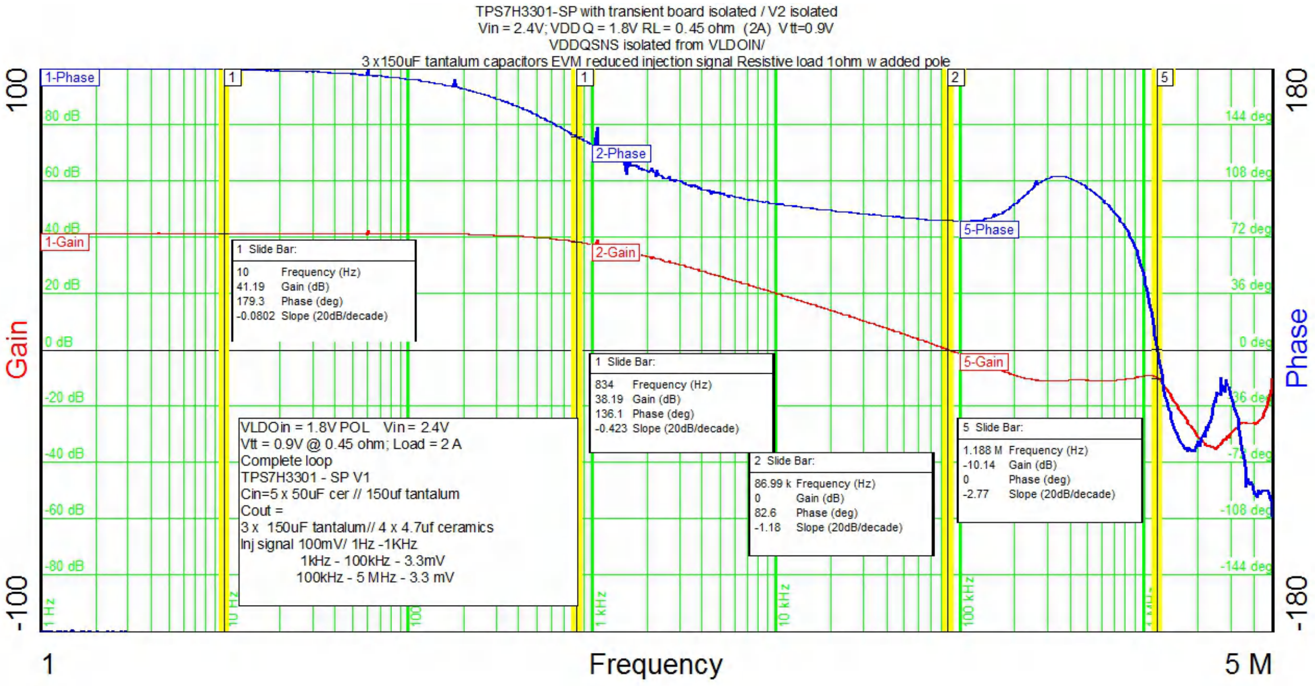


Figure 8-10. DDR2 2-A Load V_{IN} = 2.4 V, VTT/V_O = 0.9 V

Power Supply Recommendations

TPS7H3301-SP is designed to support DDR, DDR2, DDR3, DDR3L, and DDR4 VTT applications. TPS7H3301-SP VLDOIN supports voltage range from 0.9 V to 3.5 V. The supply must be well regulated. Having a separate VLDOIN supply from DDR VDDQ allows designer to optimize system efficiency. VDD/V_{IN} is used to bias the TPS7H3301-SP IC and its voltage range from 2.375 V to 3.5 V. This supply must be well regulated and bypassed with a ceramic capacitor with a value of 1 µF and 10 µF. TI recommends that VLDOIN and DDR supply VDDQ be isolated from each other. If this is not possible then an RC filter must be used to isolate VLDOIN and VDDQSNS. However, in so doing the dynamic tracking of VTT and VTTREF will be lost. See the EVM user's guide SLVUAK2 for additional details.

9 Layout

9.1 Layout Guidelines

Consider the following points before starting the TPS7H3301-SP layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the pin with short and wide connections.
- The output capacitor for VTT/V_O should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VTTSNS should be connected to the positive node of VTT/V_O output capacitors as a separate trace from the high-current power line. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor or capacitors at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the output capacitor or capacitors.
- Consider adding low-pass filter at VTTSNS if the ESR of the VTT/V_O output capacitor or capacitors is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise-generating lines.
- The negative node of the VTT/V_O output capacitor or capacitors and the VTTREF capacitor should be tied together by avoiding common impedance to the high-current path of the VTT/V_O sink and source current.
- The GND and PGND pins should be connected to the thermal land underneath the die pad with multiple vias connecting to the internal system ground planes (for better result, use at least two internal ground planes). Use as many vias as possible to reduce the impedance between PGND/GND and the system ground plane. Also, place bulk caps close to the DIMM/module or memory load point and route the VTTSNS to the DIMM/module load sense point.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package's thermal pad. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias, 0.33 mm in diameter or smaller, connected from the thermal land to the internal/solder side ground plane or planes should also be used to help dissipation.

9.2 Layout Example

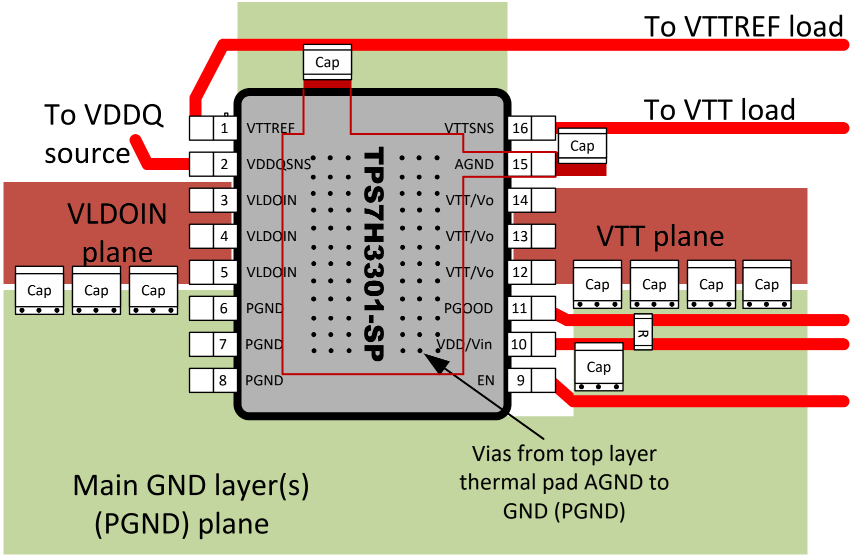


Figure 9-1. Layout Recommendation

9.3 Thermal Considerations

VTT/V_O current can flow in both source and sink directions. As the TPS7H3301-SP is a linear regulator, power is dissipated internal to the device. When the device is sourcing current, the voltage difference between VLDOIN and VTT/V_O times IO (I_{IO}) current becomes the power dissipation as shown in Equation 2.

$$P_{DISS\_SRC} = \left(V_{VLDOIN} - V_{VO}\right) x\ I_{O\_SRC} \tag{2}$$

In this case, if VLDOIN is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, V_O voltage is applied across the internal LDO regulator and the power dissipation (P_{DISS_SNK}) can be calculated by Equation 3.

$$P_{DISS\_SNK} = V_{VO} \times I_{O\_SNK} \tag{3}$$

Because the device does not sink and source current at the same time and the IO current may vary rapidly with time, the actual power dissipation should be the time average of the above dissipations over the thermal relaxation duration of the system. Another source of power consumption is the current used for the internal current control circuitry from the VDD/V_{IN} supply and the VLDOIN supply. This can be estimated as $P_{VDD/V_{IN}}$ = 105mW and P_{VLODIN} = 4.2mW or less during normal operating conditions. This power must be effectively dissipated from the package.

The thermal performance of an LDO depends on the printed circuit board (PCB) layout. Because the TPS7H3301-SP device is shipped unformed, only the recommended heat pad pattern is shown. Lead pad placement depends on final form factor.

To further improve the thermal performance of this device, using a larger than recommended thermal land as well as increasing the number of vias helps lower the thermal resistance from junction to heat slug.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H3301-SP Single-Event Effects Summary* radiation report (SLAK008)
- Texas Instruments, *TPS7H3301EVM-CVAL (HREL022)* user's guide (SLVUAK2)

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-1422801VXC	Active	Production	CFP (HKR) | 16	25 | TUBE	ROHS Exempt	Call TI	N/A for Pkg Type	-55 to 125	5962-1422801VXC TPS7H3301-SP
5962R1422801VXC	Active	Production	CFP (HKR) | 16	25 | TUBE	ROHS Exempt	Call TI	N/A for Pkg Type	-55 to 125	5962R1422801VXC TPS7H3301-RHA
TPS7H3301HKR/EM	Active	Production	CFP (HKR) | 16	25 | TUBE	ROHS Exempt	Call TI	N/A for Pkg Type	25 to 25	TPS7H3301HKREM

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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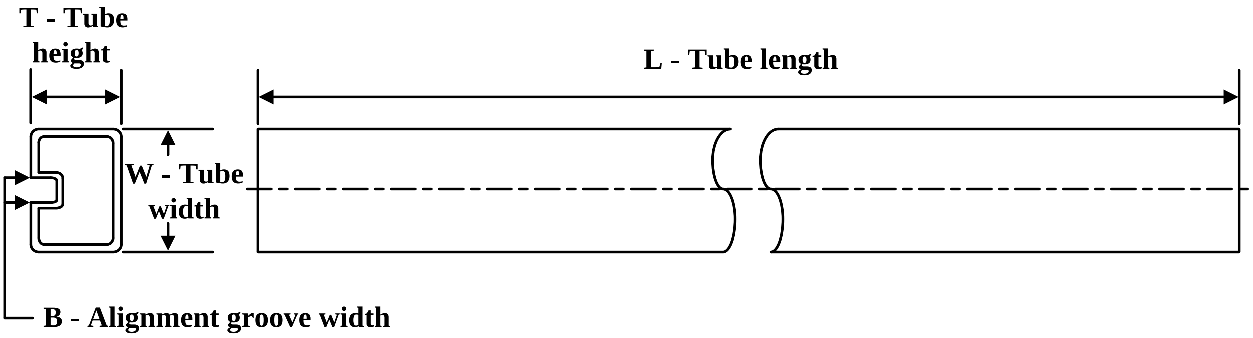
TUBE

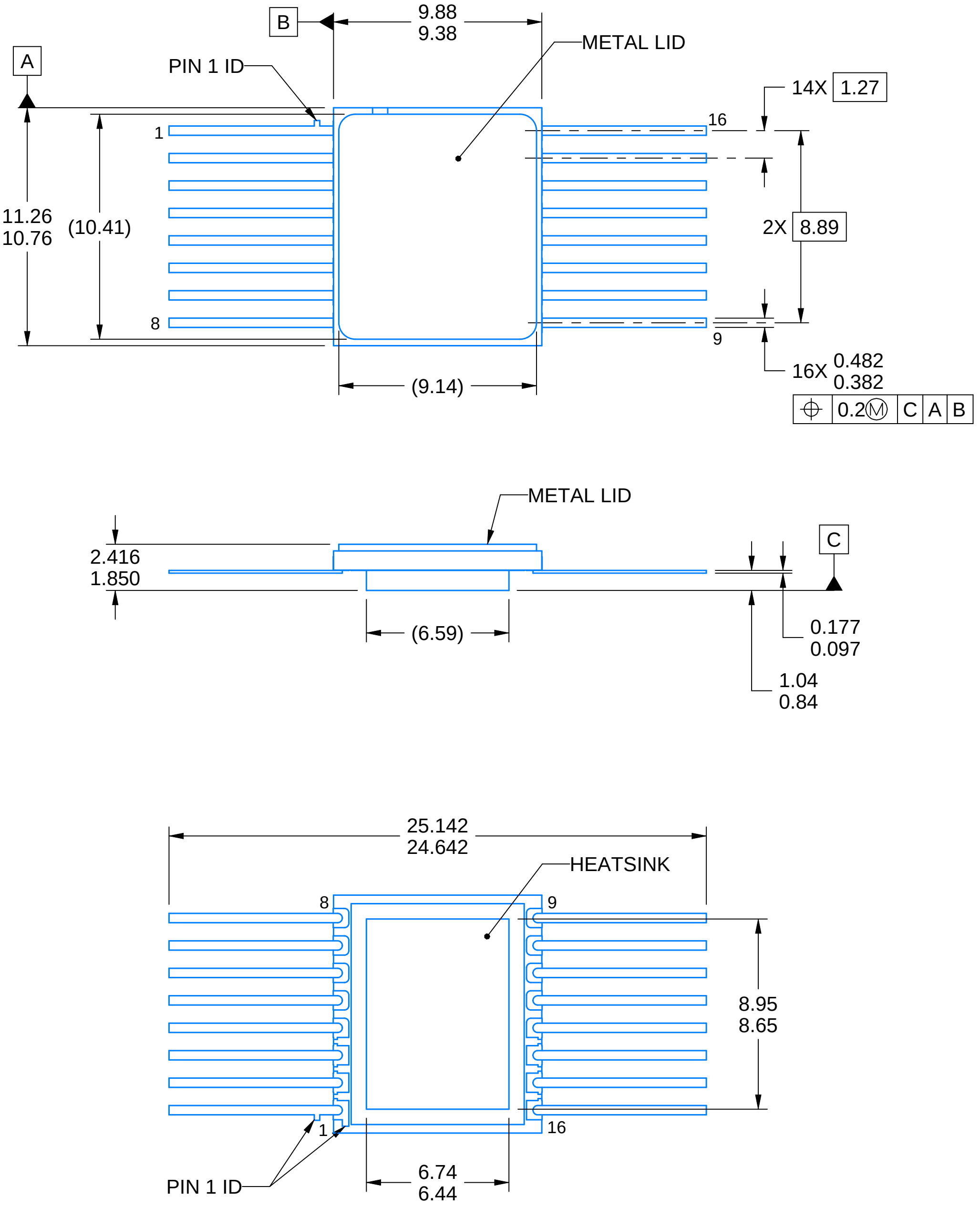


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1422801VXC	HKR	CFP	16	25	506.98	26.16	6220	NA
5962R1422801VXC	HKR	CFP	16	25	506.98	26.16	6220	NA
TPS7H3301HKR/EM	HKR	CFP	16	25	506.98	26.16	6220	NA

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



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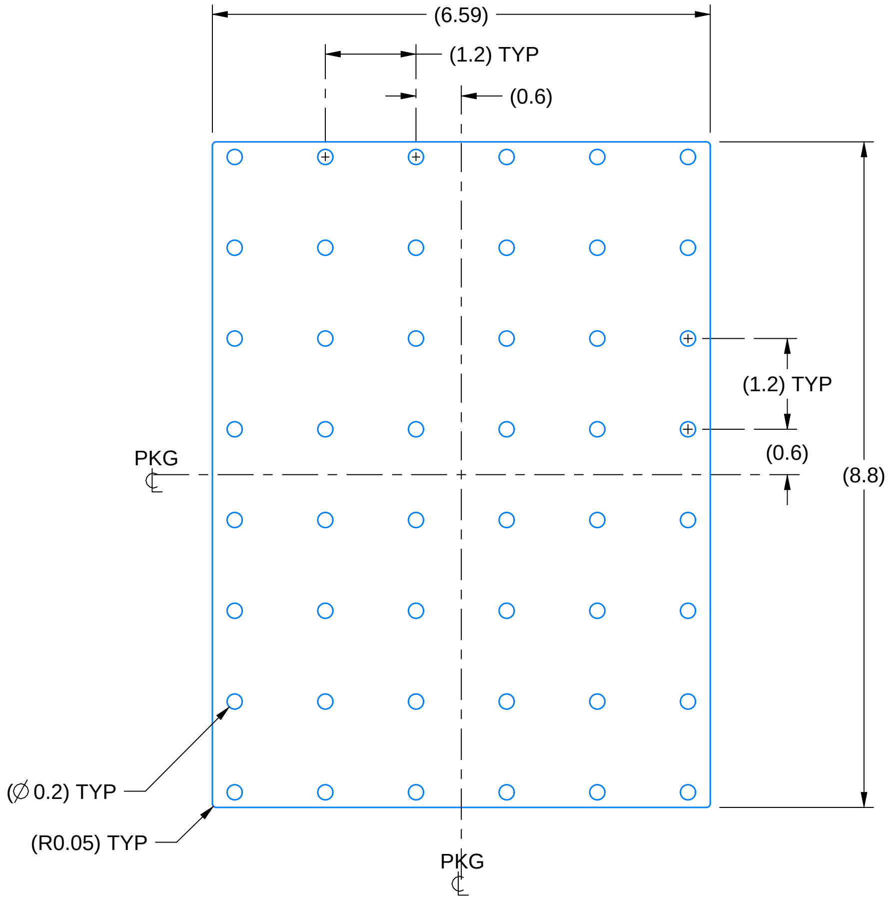
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

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