TPS7H3024-SP Radiation-Hardened, 14V, 4-Channel Supervisor With Watchdog Timer

1 Features

- Radiation performance:
  - Radiation hardness assurance (RHA) up to a total ionizing dose (TID) of 100krad(Si)
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 75MeV-cm^2/mg
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 75MeV-cm^2/mg
- Wide supply IN voltage range (V_{IN}): 3V to 14V
- Monitor up to 4 voltage rails with high accuracy:
  - TPS7H3024: 2 OV + 2 UV or 2 window with push-pull
- Monitor coherent processor execution using the watchdog timer
- Single resistor programmable global delay timer
- Programmable watchdog time-out
- Precision threshold voltage and hysteresis current:
  - V_{TH_SENSEx} of 599.7mV ± 1% across: voltage, temperature, and radiation (TID)
  - I_{HYS_SENSEx} of 24µA ± 3% across: voltage, temperature, and radiation (TID)
- Push-Pull outputs with programmable pull-up voltage between 1.6V to 7V
  - Global $\overline{\text{RESETx}}$ pull-up domain (V_{PULL_UP1})
  - Common PWRGD and $\overline{\text{WDO}}$ pull-up domain (V_{PULL_UP2})
- SR_$\overline{\text{UVLO}}$ input to reset all outputs
  - Or adjust the undervoltage lockout externally via a resistive divider
- Available in military (–55°C to 125°C) temperature range

2 Applications

- Satellite electrical power system (EPS)
- Monitoring voltage rails for complex digital processors such as: FPGAs, SoCs, AFEs, and power systems for space applications
- Monitoring of coherent processor execution

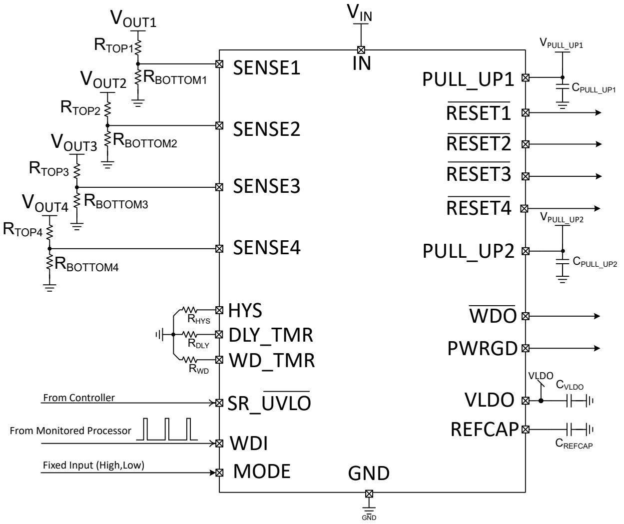
3 Description

The TPS7H3024-SP is an integrated, 3V to 14V, four-channel radiation-hardness-assured power-supply supervisor with watchdog. An accurate 599.7mV ± 1% threshold voltage and a 24µA ± 3% hysteresis current provide programmable monitoring voltages. A global programmable delay timer is programmed via a single resistor. In addition a PWRGD output is provided to monitor the global power tree status. The device also incorporates a positive edge detection watchdog timer to monitor an external processor for coherent execution. Faults can be detected and mitigated by the external controller, using the SR_$\overline{\text{UVLO}}$ input. A standard microcircuit drawing (SMD) is available for the QMLV, 5962R2420601VXC.

Device Information

PART NUMBER(1)	GRADE(2)	PACKAGE(3)
5962R2420601VXC(4)	QMLV-RHA	22-pin ceramic (CFP) 6.21mm × 7.69mm Mass = 415.6mg
TPS7H3024HFT/EM(4)	Engineering sample	

(1) Planned part numbers and device grades are shown. For additional information view the Device Options Table.
(2) For additional information about part grade, view SLYB235.
(3) Dimensions and mass are nominal values.
(4) Advance information.



Typical Application

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4 Device Options Table

GENERIC PART NUMBER	OUTPUT TYPE	FUNCTION	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H3024-SP	Push-pull	2 UV + 2 OV (or 2 window)	TID of 100 krad(Si) RLAT, DSEE free to 75 MeV-cm^2/mg	QMLV-RHA	22-pin CFP HFT	5962R2420601VXC(3)
			None	Engineering model(4)		TPS7H3024HFT/EM(3)

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view SLYB235.
(3) Advance information.
(4) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.

5 Pin Configuration and Functions

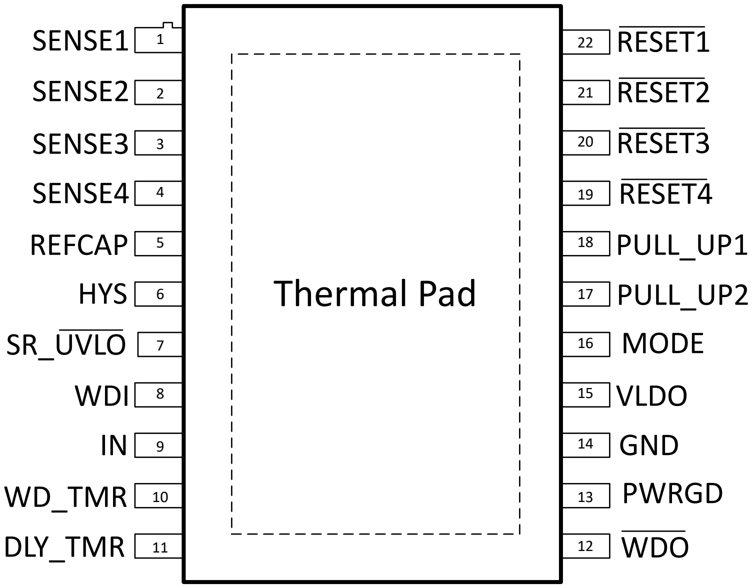


Figure 5-1. HFT Package, 22-Pin CFP (Top View)

Table 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
SENSE1	1	I	The non-inverting input of the comparator used to monitor a desired voltage rail. To set the V_{ON1} and V_{OFF1} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE1 pin. A voltage greater than V_{TH_SENSEx} (599.7mV typ.) on this pin is considered as a regulated voltage rail (V_{ON1}). The V_{OFF1} is a function of the I_{HYS} current, the resistive divider and V_{TH_SENSEx} . Refer to Top and Bottom Resistive Divider Design Equations.
SENSE2	2	I	The non-inverting input of the comparator used to monitor a desired voltage rail. To set the V_{ON2} and V_{OFF2} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE2 pin. A voltage greater than V_{TH_SENSEx} (599.7mV typ.) on this pin is considered as a regulated voltage rail (V_{ON2}). The V_{OFF2} is a function of the I_{HYS} current, the resistive divider and V_{TH_SENSEx} . Refer to Top and Bottom Resistive Divider Design Equations.
SENSE3	3	I	The non-inverting input of the comparator used to monitor a desired voltage rail. To set the V_{ON3} and V_{OFF3} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE3 pin. A voltage greater than V_{TH_SENSEx} (599.7mV typ.) on this pin is considered as a regulated voltage rail (V_{ON2}). The V_{OFF2} is a function of the I_{HYS} current, the resistive divider and V_{TH_SENSEx} .Refer to Top and Bottom Resistive Divider Design Equations.
SENSE4	4	I	The non-inverting input of the comparator used to monitor a desired voltage rail. To set the V_{ON4} and V_{OFF4} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE4 pin. A voltage greater than V_{TH_SENSEx} (599.7mV typ.) on this pin is considered as a regulated voltage rail (V_{ON4}). The V_{OFF4} is a function of the I_{HYS} current, the resistive divider and V_{TH_SENSEx} .Refer to Top and Bottom Resistive Divider Design Equations.
REFCAP	5	O	1.2V internal reference. Requires a 470nF external capacitor to GND. Do not load this pin with any additional external circuitry
HYS	6	O	Hysteresis. Connect a 49.9kΩ resistor between this pin and GND, to program the hysteresis current (typically 24µA) at SENSE1 to SENSE4. Is recommended using a resistor with a 0.1% or better tolerance.
SR_$\overline{\text{UVLO}}$	7	O	System reset / UVLO input. Force this input low to assert all outputs low. A resistor divider from V_{IN} to GND may be used to set the device turn-on level.

Table 5-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
WDI	8	I	Watchdog input. Toggle this signal from low to high to clear the watchdog timer. If this input is toggle low to high before the watchdog timer is expired the $\overline{\text{WDO}}$ will stay high, otherwise will be asserted low.
IN	9	I	Input supply to the device. Input voltage range is from 3V to 14V. Connect at least a 0.1µF ceramic capacitor as close as possible to the pin.
WD_TMR	10	I/O	Watchdog timer. Connect a resistor to GND between 56.2kΩ and 174kΩ to set the watchdog timeout. The delay can be adjusted from 0.5s to 1.5s. Leave this pin floating to deactivate the watchdog timer.
DLY_TMR	11	I/O	Delay timer. Connect a resistor to GND between 10.5kΩ and 1.18MΩ to set the out-of-fault delay. The delay can be adjusted from 0.25ms to 25ms. Leave this pin floating for no delay.
$\overline{\text{WDO}}$	12	O	Watchdog output. Push-pull output. The VOH level is set by the PULL_UP2 input supply voltage.
PWRGD	13	O	Power Good. This output indicates when all rails (SENSE1 to SENS4) are in regulation. Push-pull output. The VOH level is set by the PULL_UP2 input supply voltage.
GND	14	—	Ground.
VLDO	15	O	Output of internal regulator. Requires at least 1µF external ceramic capacitor to GND. This voltage can be used to create positive offset when monitoring negative voltages. The maximum load for this LDO is 5mA. This pin is not protected for over-current events.
MODE	16	I	Logical input to control the behavior of the output stage. For more details refer to Section 8.3.4. This input must not be dynamically changed.
PULL_UP2	17	I	Input supply voltage to program the pull-up voltage for the push-pull outputs on PWRGD and $\overline{\text{WDO}}$. Connect at least a 1µF ceramic capacitor as close as possible to the pin.
PULL_UP1	18	I	Input supply voltage to program the global pull-up voltage for the push-pull outputs on $\overline{\text{RESET1}}$ to $\overline{\text{RESET4}}$. Connect at least a 1µF ceramic capacitor as close as possible to the pin.
$\overline{\text{RESET4}}$	19	O	Reset 4. $\overline{\text{RESET4}}$ is asserted low when SENSE4 is in a fault. Push-pull output. The VOH level is set by the PULL_UP2 input supply voltage.
$\overline{\text{RESET3}}$	20	O	Reset 3. $\overline{\text{RESET3}}$ is asserted low when SENSE3 is in a fault. output. The VOH level is set by the PULL_UP2 input supply voltage.
$\overline{\text{RESET2}}$	21	O	Reset 2. $\overline{\text{RESET2}}$ is asserted low when SENSE2 is in a fault. output. The VOH level is set by the PULL_UP2 input supply voltage.
$\overline{\text{RESET1}}$	22	O	Reset 1. $\overline{\text{RESET1}}$ is asserted low when SENSE1 is in a fault. output. The VOH level is set by the PULL_UP2 input supply voltage.
Thermal pad		—	Internally grounded. It is recommended to connect this metal thermal pad to a large ground plane for effective heat dissipation (2).
Metal lid	Lid	—	The lid is internally connected to the thermal pad and GND through the seal ring. (2)

(1) I = Input, O = Output, I/O = Input or Output, — = Other
(2) Valid only for HFT package

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	16	V
	WDI, MODE	–0.3	7.5	
	SENSE1, SENSE2, SENSE3, SENSE4	–0.3	3.6	
	PULL_UP1, PULL_UP2	–0.3	7.5	
	SR_$\overline{\text{UVLO}}$	–0.3	7.5	
	DLY_TMR, WD_TMR	–0.3	3.6	
Output voltage	REFCAP	–0.3	2	V
	VLDO	–0.3	3.6	
	HYS	–0.3	3.6	
	$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$, $\overline{\text{RESET3}}$, $\overline{\text{RESET4}}$	–0.3	7.5	
	PWRGD, $\overline{\text{WDO}}$	–0.3	7.5	
Output current	$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$, $\overline{\text{RESET3}}$, $\overline{\text{RESET4}}$	–20	20	mA
	PWRGD, $\overline{\text{WDO}}$	–20	20	
Junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltages values are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range, T_A = –55°C to 125°C (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
Input voltage	IN	3		14	V
	WDI, MODE	0		7	
	SENSE1, SENSE2, SENSE3, SENSE4	0		3.5	
	PULL_UP1, PULL_UP2	1.6		7	
	SR_$\overline{\text{UVLO}}$	0		7	
Output voltage	$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$, $\overline{\text{RESET3}}$, $\overline{\text{RESET4}}$	0		7	V
	PWRGD, $\overline{\text{WDO}}$	0		7	
Output current	$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$, $\overline{\text{RESET3}}$, $\overline{\text{RESET4}}$	–10		10	mA
	PWRGD, $\overline{\text{WDO}}$	–10		10	
Junction temperature	T_J	–55		125	°C
Input voltage slew rate	SR_{IN}	0.001		10	V/µs

(1) All voltages values are with respect to GND.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H3024-SP HFT (CFP) 22 pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17	°C/W

(1) For more information about the traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).

6.5 Electrical Characteristics

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUP (3)	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS							
I_{Q_IN}	V_{IN} quiescent current	$\overline{\text{RESETx}}$ = Low and High, $V_{SR\_\overline{UVLO}}$ > $V_{TH\_SR\_\overline{UVLO}\_RISING\ (MAX)}$	1, 2, 3		1.5	2.5	mA
I_{SD_IN}	V_{IN} shutdown current	$V_{SR\_\overline{UVLO}}$ = 0V	1, 2, 3		1.5	2.1	
$UVLO_{RISE}$	V_{IN} rising undervoltage lockout		1, 2, 3	2.73	2.80	2.88	V
$UVLO_{FALL}$	V_{IN} falling udervoltage lockout		1, 2, 3	2.58	2.65	2.72	
V_{LDO}	Internal linear regulator output voltage	4V ≤ V_{IN} ≤ 14V	1, 2, 3	3.23	3.29	3.37	V
		V_{IN} = 3V	1, 2, 3	98%	99%		× V_{IN}
$VLDO_{I\_MAX}$	VLDO maximum current for out-of-regulation operation	3.65V ≤ V_{IN} ≤ 14V, VLDO= 98.5% x $VLDO_{(NOM)}$	1, 2, 3			5	mA
REFCAP	Internal bandgap voltage		1, 2, 3	1.188	1.2	1.212	V
V_{POR_IN}	IN power on reset voltage (4)	1.6V ≤ V_{PULL_UPx} ≤ 7V, V_{OL} ≤ 320mV with $I_{\overline{RESETx}}$ = –1mA	1, 2, 3		1.42	2	
$V_{POR\_PULL\_UPx}$	PULL_UPx power on reset voltage (5)	V_{IN} = 0V, V_{OL} ≤ 320mV, $I_{\overline{RESETx}}$ = –100μA	1, 2, 3		0.85	1.1	
V_{HYS}	HYS pin internal voltage	R_{HYS} = 49.9kΩ	1, 2, 3	1.164	1.2	1.236	
SENSE1 TO SENSE4, SR_UVLO, WDI AND MODE COMPARATOR INPUTS							
V_{TH_SENSEx}	Threshold voltage at SENSEx		1, 2, 3	593.1	599.7	604.9	mV
I_{HYS_SENSEx}	SENSEx hysteresis current	V_{SENSEx} = 700mV	1, 2, 3	23.28	24	24.72	μA
I_{LKG_SENSEx}	Input leakage current at SENSEx	V_{SENSEx} = 500mV	1, 2, 3		1	100	nA
$V_{TH\_SR\_\overline{UVLO}\_RISING}$	Rising threshold voltage at SR_$\overline{\text{UVLO}}$		1, 2, 3	580	602	618	mV
$V_{TH\_SR\_\overline{UVLO}\_FALLING}$	Falling threshold voltage at SR_$\overline{\text{UVLO}}$		1, 2, 3	475	499	517	
$I_{LKG\_SR\_\overline{UVLO}}$	Input leakage current at SR_$\overline{\text{UVLO}}$	$V_{SR\_\overline{UVLO}}$ = 7V	1, 2, 3		2	100	nA
$V_{TH\_WDI\_RISING}$	Rising threshold voltage at WDI		1, 2, 3	578	602	624	mV
$V_{TH\_WDI\_FALLING}$	Falling threshold voltage at WDI		1, 2, 3	473	498	521	mV
I_{LKG_WDI}	Input leakage current at WDI	V_{WDI} = 7V	1, 2, 3		1.4	100	nA
$V_{TH\_MODE\_RISING}$	Rising threshold voltage at MODE		1, 2, 3	576	600	623	mV
$V_{TH\_MODE\_FALLING}$	Falling threshold voltage at MODE		1, 2, 3	475	498	520	mV
I_{LKG_MODE}	Input leakage current at MODE	V_{MODE} = 7V	1, 2, 3		1	100	nA

6.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS		SUB-GROUP (3)	MIN	TYP	MAX	UNIT
$\overline{\text{RESET1}}$ TO $\overline{\text{RESET4}}$, PWRGD AND $\overline{\text{WDO}}$ PUSH PULL OUTPUTS								
$PULL\_UPx_{LKG}$	PULL_UPx leakage current	V_{PULL_UPx} = 7V, $\overline{\text{RESETx}}$= LOW		1, 2, 3		48	100	µA
$V_{OL\_\overline{RESETx}}$	Low-level $\overline{\text{RESETx}}$ output voltage	1.6V ≤ V_{PULL_UP1} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			5%	x V_{PULL_UP1}
			I_{LOAD} = –10mA	1, 2, 3			23%	
$V_{OH\_\overline{RESETx}}$	High-level $\overline{\text{RESETx}}$ output voltage	1.6V ≤ V_{PULL_UP1} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	95%			
			I_{LOAD} = 10mA	1, 2, 3	75%			
V_{OL_PWRGD}	Low-level PWRGD output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			5%	x V_{PULL_UP2}
			I_{LOAD} = –10mA	1, 2, 3			23%	
V_{OH_PWRGD}	High-level PWRGD output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	95%			
			I_{LOAD} = 10mA	1, 2, 3	75%			
$V_{OL\_\overline{WDO}}$	Low-level $\overline{\text{WDO}}$ output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			5%	
			I_{LOAD} = –10mA	1, 2, 3			23%	
$V_{OH\_\overline{WDO}}$	High-level $\overline{\text{WDO}}$ output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	95%			
			I_{LOAD} = 10mA	1, 2, 3	75%			
$SR_{\overline{RESETx}\_RISE}$	$\overline{\text{RESETx}}$ rising output voltage slew rate	10% to 90% of V_{PULL_UP1}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP1} ≤ 7V	9, 10, 11	17	298		V/µs
SR_{PWRGD_RISE}	PWRGD rising output voltage slew rate			9, 10, 11	17	298		
$SR_{\overline{WDO}\_RISE}$	$\overline{\text{WDO}}$ rising output voltage slew rate			9, 10, 11	17	298		
$SR_{\overline{RESETx}\_FALL}$	$\overline{\text{RESETx}}$ falling output voltage slew rate	90% to 10% of V_{PULL_UP1}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP1} ≤ 7V	9, 10, 11	44	186		
SR_{PWRGD_FALL}	PWRGD falling output voltage slew rate			9, 10, 11	44	186		
$SR_{\overline{WDO}\_FALL}$	$\overline{\text{WDO}}$ falling output voltage slew rate			9, 10, 11	44	186		
$R_{\overline{RESETx}\_PULL\_UP}$	$\overline{\text{RESET}}$ PMOS source output resistance	I_{LOAD} = 2mA	1.6V ≤ V_{PULL_UP1} < 3.3V	1, 2, 3		20	40	Ω
			3.3V ≤ V_{PULL_UP1} ≤ 7V	1, 2, 3		9	20	
$R_{PWRGD\_PULL\_UP}$	PWRGD PMOS source output resistance	I_{LOAD} = 2mA	1.6V ≤ V_{PULL_UP2} < 3.3V	1, 2, 3		20	40	
			3.3V ≤ V_{PULL_UP2} ≤ 7V	1, 2, 3		9	20	
$R_{\overline{WDO}\_PULL\_UP}$	$\overline{\text{WDO}}$ PMOS source output resistance	I_{LOAD} = 2mA	1.6V ≤ V_{PULL_UP2} < 3.3V	1, 2, 3		20	40	
			3.3V ≤ V_{PULL_UP2} ≤ 7V	1, 2, 3		9	20	
$R_{\overline{RESETx}\_PULL\_DOWN}$	$\overline{\text{RESET}}$ NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		16	36	
$R_{PWRGD\_PULL\_DOWN}$	PWRGD NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		16	36	
$R_{\overline{WDO}\_PULL\_DOWN}$	$\overline{\text{WDO}}$ NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		16	36	

6.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUP (3)	MIN	TYP	MAX	UNIT
THERMAL PROTECTION							
T_{SD_ENTER}	Thermal shutdown enter temperature				185		℃
T_{SD_EXIT}	Thermal shutdown exit temperature				171		
DELAY AND WATCHDOG TIMERS							
t_{DLY_TMR}	Delay time	R_{DLY_TMR} = 10.5kΩ	1, 2, 3	0.22	0.26	0.33	ms
		R_{DLY_TMR} = 619kΩ	1, 2, 3	11.3	12.5	13.7	
		R_{DLY_TMR} = 1.18MΩ	1, 2, 3	21.3	23.7	26.2	
t_{WD_TMR}	Watchdog time-out	R_{WD_TMR} = 56.2kΩ	1, 2, 3	0.43	0.52	0.57	s
		R_{WD_TMR} = 118kΩ	1, 2, 3	0.8	1	1.2	
		R_{WD_TMR} = 174kΩ	1, 2, 3	1.34	1.5	1.7	

(1) See the 5962R2420601VXC SMD (standard microcircuit drawing) for additional information on the RHA devices.
(2) All voltage values are with respect to GND.
(3) For subgroup definitions, see Quality Conformance Inspection table.
(4) V_{POR_IN} is the minimum V_{IN} voltage for a controlled output state, when 1.6V ≤ V_{PULL_UPx} ≤ 7V. Below V_{POR_IN}, the output state cannot be determined.
(5) $V_{POR\_PULL\_UPx}$ is the minimum V_{PULL_UPx} voltage for a controlled output state, when V_{IN} ≤ 3V. Below $V_{POR\_PULL\_UPx}$ the output state cannot be determined.

6.6 Timing Requirements

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, over temperature range (T_A = –55°C to 125°C) unless otherwise noted; includes group E radiation testing at T_A = 25°C for RHA devices (1)

PARAMETER		TEST CONDITIONS		SUB-GROUP (2)	MIN	TYP	MAX	UNIT
$t_{START\_UP\_DLY}$	Start-up delay time (3)	V_{REFCAP} ≥ 1.1V		1, 2, 3		0.3	2.8	ms
$t_{pd\_\overline{RESETx}}$	$\overline{\text{RESET}}$ propagation delay	DLY_TMR = Open, $V_{OVERDRIVE}$ = 10mV, SR_{SENSEx} = 27V/µs from 50% of SENSEx to 50% of $\overline{\text{RESETx}}$		1, 2, 3		0.62	4.3	µs
t_{pd_PWRGD}	PWRGD propagation delay	DLY_TMR = Open, $V_{OVERDRIVE}$ = 10mV, SR_{SENSEx} = 27V/µs from 50% of V_{SENSEx} to 50% of V_{PWRGD}		1, 2, 3		0.51	4.3	µs
$t_{pd\_SR\_\overline{UVLO}}$	SR_$\overline{\text{UVLO}}$ propagation delay	V_{SR_FAULT} = Falling from 1V to 0V in 10ns, V_{SENSEx} = 610mV, from 50% of $V_{SR\_\overline{UVLO}}$ to 50% of V_{PWRGD}		1, 2, 3		0.92	2	µs
t_{pd_WDI}	WDI propagation delay	V_{WDI} = Rising from 0V to 1V in 10ns, V_{SENSEx} = 610mV, from 50% of V_{WDI} to 50% of V_{WDO}	t_{WD_TMR} = 0.5s	1, 2, 3		23	40	µs
			t_{WD_TMR} = 1s			47	80	
			t_{WD_TMR} = 1.5s			68	116	
t_{PW_WDI}	WDI minimum pulse width			4, 5, 6	2			× t_{WD_OSC}
$t_{PW\_SR\_\overline{UVLO}}$	SR_UVLO minimum pulse width for valid reset			4, 5, 6		0.61	1.1	µs
$t_{h\_VENSEx\_FAULT}$	VSENSEx hold time for valid fault detection		C_{LOAD} = 100pF, $V_{OVERDRIVE}$ = |100mV|	4, 5, 6		0.56	2.2	µs
$t_{h\_VENSEx\_RISE}$	Rising threshold on VSENSEx hold time			4, 5, 6			3.7	µs

(1) See the 5962R2420601VXC SMD (standard microcircuit drawing) for additional information on the RHA device.
(2) For subgroup definitions, see Quality Conformance Inspection table.
(3) During the power-on, V_{IN} must be at or above $UVLO_{RISE(MAX)}$ for at least $t_{Start\_up\_delay}$ for all internal references to be within specification.

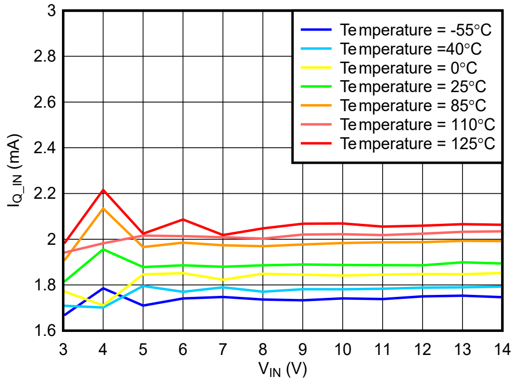
6.7 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

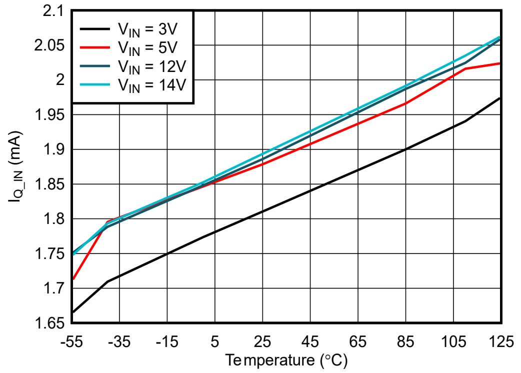
6.8 Typical Characteristics

R_{DLY_TMR} = 10.5kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, R_{HYS} = 49.9kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, MODE=Logic Low, unless otherwise noted.



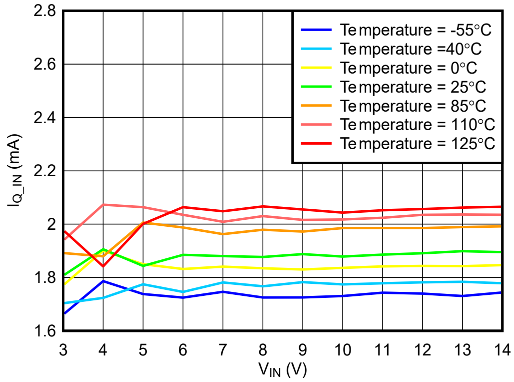
RESETx = Low V_{PULL_UPx} = 7V

Figure 6-1. I_{Q_IN} vs V_{IN} Across Temperature with RESETx = Low



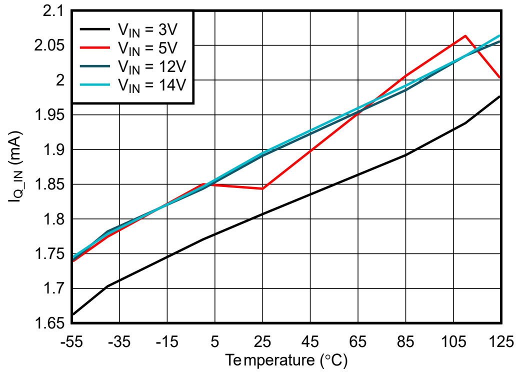
RESETx = Low V_{RESETx} = 7V

Figure 6-2. I_{Q_IN} vs Temperature Across V_{IN} with RESETx = Low



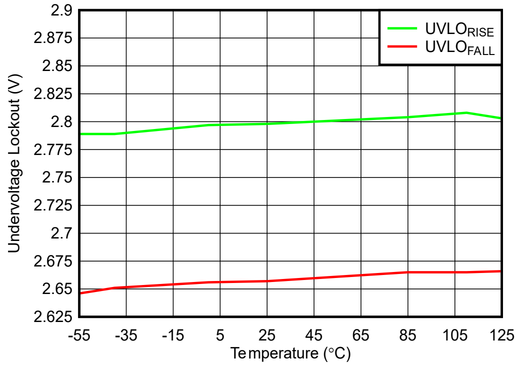
RESETx = High V_{PULL_UPx} = 7V

Figure 6-3. I_{Q_IN} vs V_{IN} Across Temperature with RESETx = High



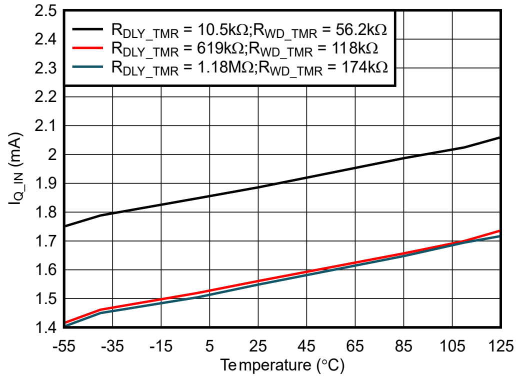
RESETx = High V_{RESETx} = 7V

Figure 6-4. I_{Q_IN} vs Temperature Across V_{IN} with RESETx = High



R_{DLY_TMR} = Floating R_{WD_TMR} = Floating

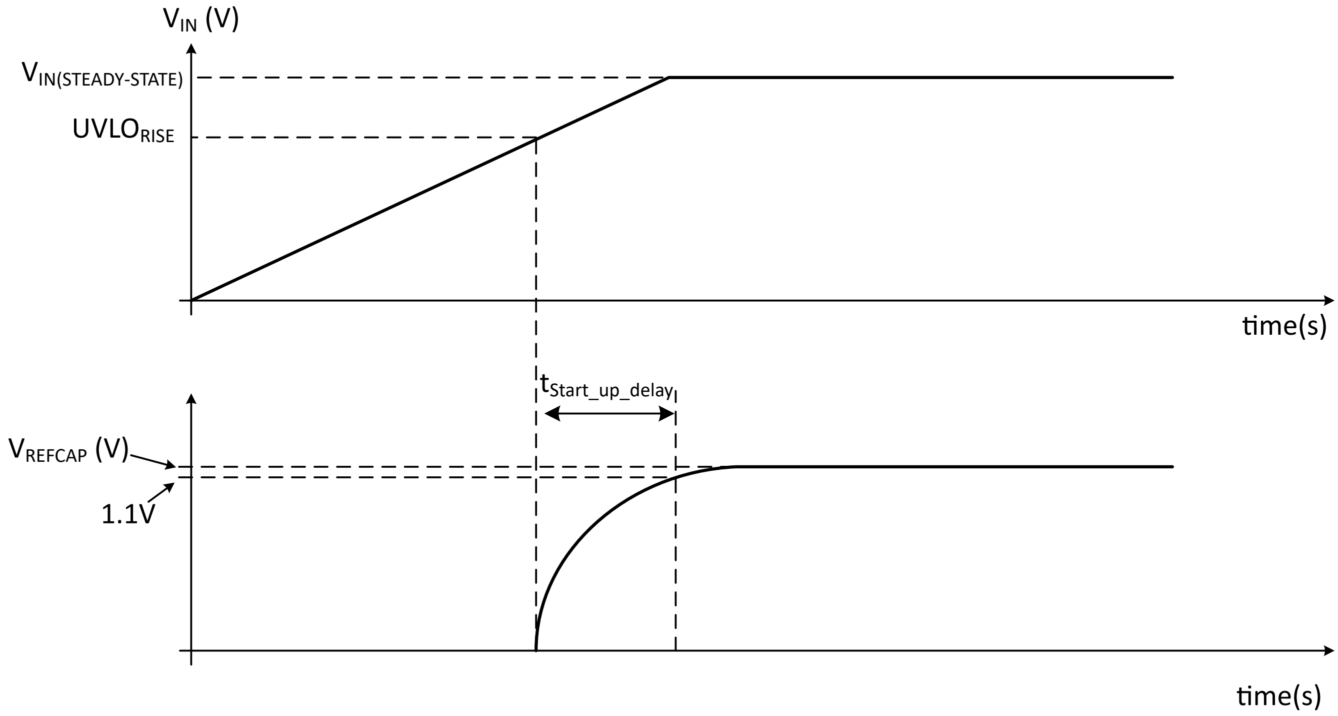
Figure 6-5. Undervoltage Lockout vs Temperature



V_{IN} = 12V RESETx = Low
V_{PULL_UPx} = 7V

Figure 6-6. IQ_IN vs Temperature Across DLY_TMR and WD_TMR Resistance

7 Parameter Measurement Information



A. $V_{IN(STEADY\text{-}STATE)}$ is a valid operating voltage between 3V and 14V

Figure 7-1. $t_{Start\_up\_delay}$ Time Measurement

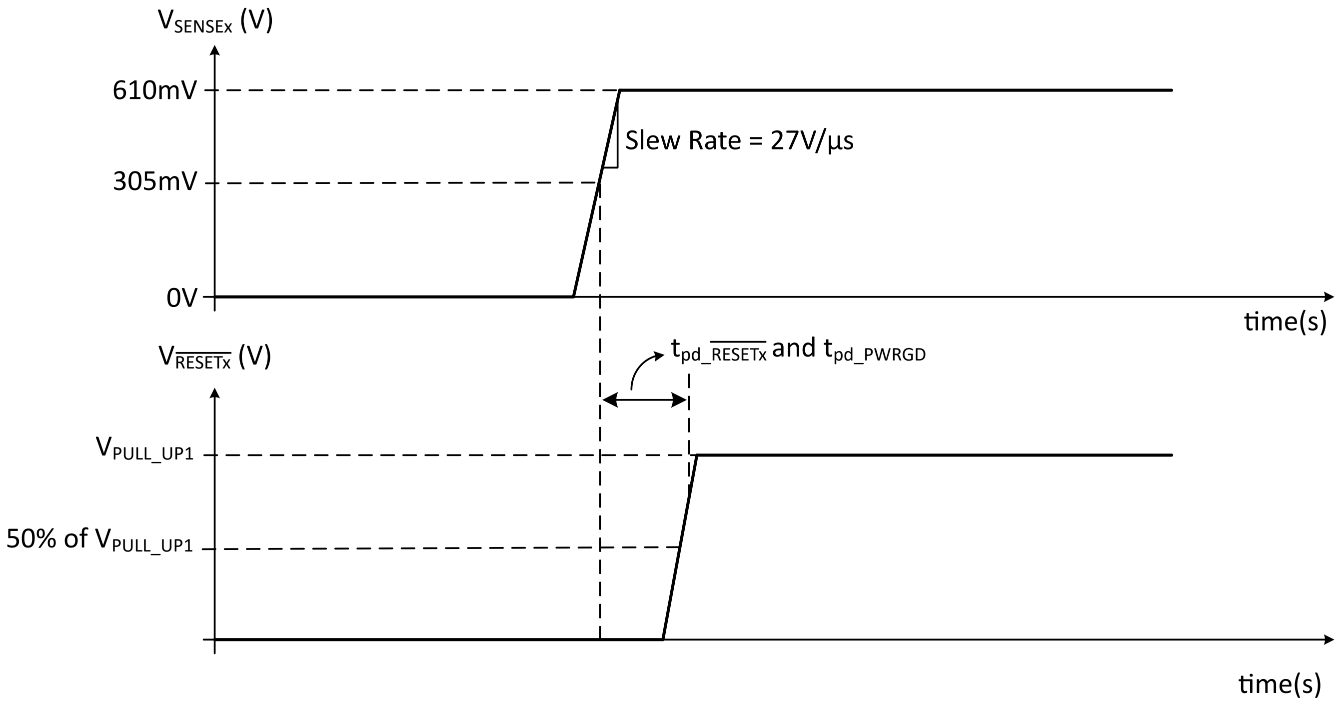


Figure 7-2. $\overline{\text{RESETx}}$ and PWRGD Propagation Delay ($t_{pd\_\overline{RESETx}}$ and t_{pd_PWRGD}) Time Measurement

A. For $t_{pd\_\overline{RESETx}}$ each SENSEx channel is measure independently while for $_{pd\_PWRGD}$ all SENSEx are ramped at same time, and the measurement is from SENSE1 to PWRGD.

8 Detailed Description

8.1 Overview

The TPS7H3024 is a four-channel, 3V to 14V, voltage supervisor with an integrated watchdog for space applications. The device is intended for devices with disable low input. The device can be configured to sense either:

1. 2 undervoltage (UV) + 2 overvoltage(OV).
2. 2 window.

This behavior is controlled by the logical value of the MODE pin. Refer to Table 8-1 for more details.

Note

The MODE logical input value, must not be dynamically changed. Once the device is power-up, the logic level most be static.

Table 8-1. TPS7H3024 Functional Modes

FUNCTION	MODE[(1)]
2 UV + 2 OV	0[(2)]
2 window	1[(3)]

(1) Mode is an static input, the user most not change the logical value dynamically. Once the device is power-up, the value most not change.
(2) 0 = $V_{MODE} < V_{TH\_MODE\_FALLING\ (MIN)}$
(3) 1 = $V_{MODE} > V_{TH\_MODE\_RISING\ (MAX)}$

The logic high for the $\overline{\text{RESET}}$x, PWRGD and $\overline{\text{WDO}}$ is externally controlled via the PULL_UPx input voltage supply. Is required to connect at least a 1µF capacitor as close to the PULL_UPx pins as possible. The logic high of all the $\overline{\text{RESET}}$x outputs is programmed via the PULL_UP1 input, while the PWRGD and $\overline{\text{WDO}}$ is programmed via PULL_UP2. The voltage range of the PULL_UPx inputs is from 1.6V to 7V.

The SENSEx inputs are connected to the non-inverting input of a comparator which is used to classify the monitored voltages as:

1. In regulation.
2. Not in regulation.

For more details on the behavior of the undervoltage and overvoltage comparators refer to Section 8.3.3.3. Each of these inputs feature a threshold level of 599.7mV (typ.) with an accuracy of ±1% across: voltage, temperature, and radiation (TID). The hysteresis voltage threshold level can be adjusted by the user and determined by the R_{TOPx} resistance and the hysteresis current (I_{HYS_SENSEx}). The I_{HYS_SENSEx} becomes active once the rising voltage at SENSEx exceeds the V_{TH_SENSEx} threshold (typically 599.7mV). I_{HYS} is 24µA with an accuracy of ±3% across: voltage, temperature, and radiation (TID). In addition the device offers an output called PWRGD to monitor the status of the power tree (complete system).

Note

In the case of the overvoltage comparators, the $\overline{\text{RESET}}$x output is logically inverted at the output of the input comparators. Refer to Figure 8-13 .

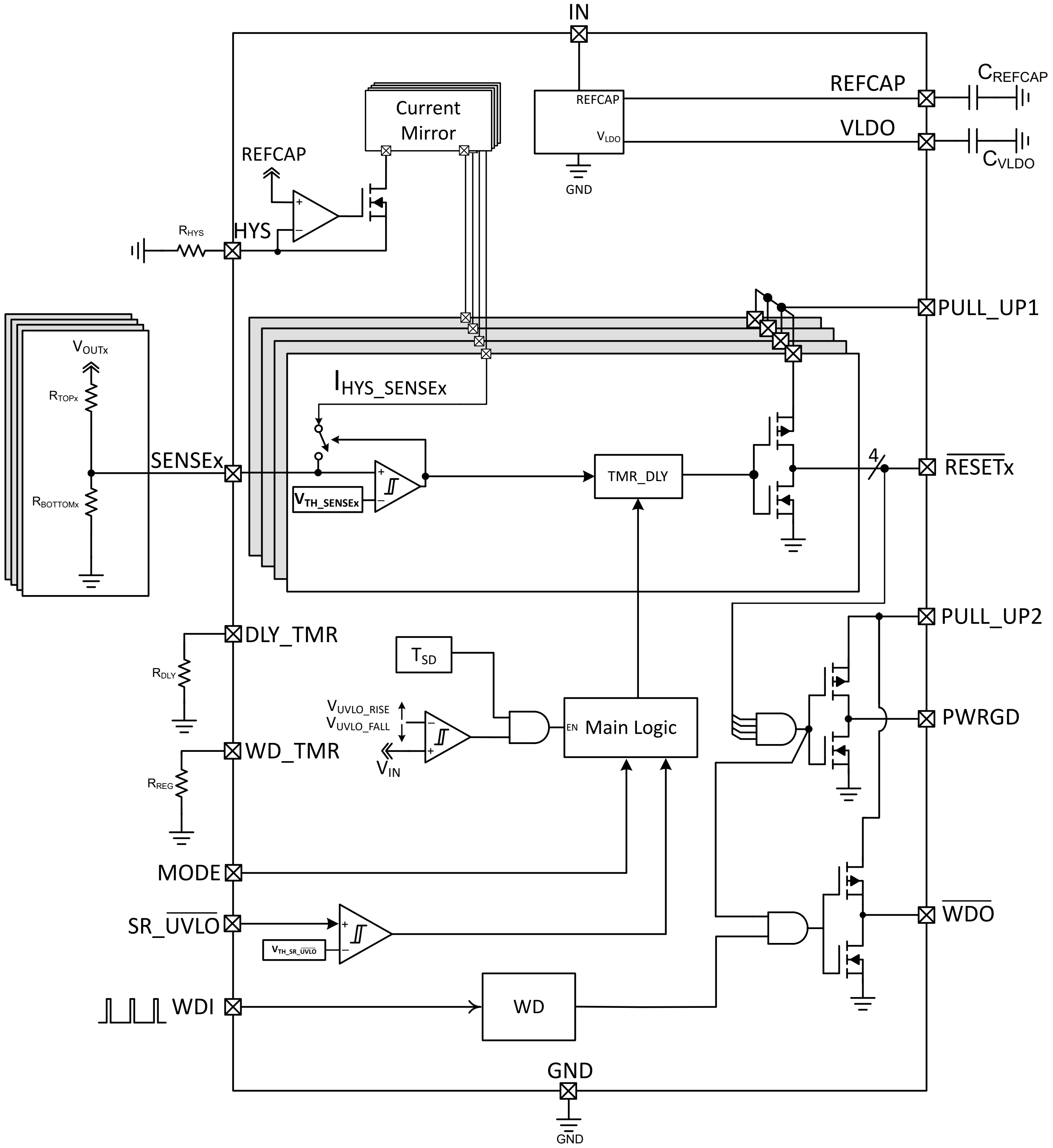
In addition to the voltage supervision, the TPS7H3024 incorporates a rising-edge watchdog timer. The WDI detects rising-edge voltage changes. When the watchdog timer logic detects a rising voltage in WDI the timer is cleared, if already active or start counting if it is the first detected pulse. With the detection of a rising pulse on WDI the system have up to the programmed time-out (0.5ms to 1.5ms nominally) to clear the timer again. If the timer is cleared before the time-out, the watchdog output ($\overline{\text{WDO}}$) remain high, otherwise will be asserted low. Usually the watchdog timer is used to monitor coherent processor execution. A processor will induce a rising-edge voltage on the WDI using an output channel and the $\overline{\text{WDO}}$ is connected to a non-maskable interrupt.

If the processor is stuck the WDI will not be toggle and by consequence the $\overline{\text{WDO}}$ will go low to reset the processor to a known state.

The device incorporates two programmable timers:

1. **DLY_TMR**: Set the out-of-fault delay. Once the monitored voltage change state, from not in regulation to in regulation, the $\overline{\text{RESETx}}$ will be asserted high once the delay programmed by user (using the DLY_TMR) is expired. This timer can be programmed from 0.25ms to 25ms, by using a 10.5kΩ to a 1.18MΩ, respectively. This delay is not valid when the input (or the monitored voltage) change state from in regulation to not in regulation, in order to propagate the fault as soon as possible.
2. **WD_TMR**: Set the time-out for the watchdog timer. When the watchdog input detects a rising voltage (WDI), the monitored process have up to the programmed time-out to provide another rising voltage in order for the output ($\overline{\text{WDO}}$) to stays high, otherwise the output will go low.

8.2 Functional Block Diagram



A. RESET2 and RESET4 output stage is driven logically inverted from the output of the input comparator, to detect overvoltage events. For more details refer to Figure 8-13.

B. When MODE=1 the RESET1 and RESET3 are of window type. For more details refer to Figure 8-9. RESET2 and RESET4 are the overvoltage comparator flag.

8.3 Feature Description

8.3.1 Input Voltage (IN), VLDO and REFCAP

During steady state operation, the input voltage of the TPS7H3024 must be between 3V and 14V. A minimum bypass capacitance of 0.1µF is required between V_{IN} and GND. The input bypass capacitors should be placed as close to the I.C. as possible. Is recommended that V_{IN} slew rate is controlled between 10V/µs to 1mV/µs for proper IC operation.

The voltage applied at V_{IN} serves as the input for the internal regulator that generates the VLDO voltage, typically 3.29V. At input voltages less the 3.29V (typ), the VLDO voltage will follow the voltage at V_{IN}. The recommended capacitance for VLDO is 1µF of ceramic type. The VLDO can be loaded up to a maximum of 5mA.

Note

The VLDO output is not protected against short circuit.

During power up, the user should wait at least 2.8ms ($t_{Start\_up\_delay}$) after V_{IN} > $UVLO_{RISE}$. This is to ensure all internal time constants are surpass, otherwise the reference may be out of the ± 1% accuracy.

Each device generates an internal 1.2V bandgap reference that is utilized throughout the various internal control logic blocks. This is the voltage present on the REFCAP pin during steady state operation. This voltage is divided down to produce the reference for the comparator inputs at:

1. SENSEx = 599.7mV typically
2. SR_UVLO = 602mV during a rising voltage and 489mV during a falling voltage, typically
3. WDI = 602mVduring a rising voltage and 498mV during a falling voltage, typically
4. MODE = 600mVduring a rising voltage and 498mV during a falling voltage, typically

The V_{TH_SENSEx} reference is measured at the RESETx outputs, to account for offsets in the error amplifier and maintains regulation within ±1% across: voltage, temperature, and radiation TID (up to 100krad in silicon). This tight reference tolerance allows the user to monitor voltage rails with high accuracy.

A 470nF capacitor to GND is required at the REFCAP pin for proper electrical operation as well as to ensure robust SET performance of the device.

8.3.1.1 Undervoltage Lockout (V_{POR_IN} < V_{IN} < UVLO)

When the voltage on V_{IN} is less than the UVLO (2.79V typ) voltage, but greater than the power-on reset voltage (V_{POR_IN}, 1.42V typ), the output pins (RESETx, PWRGD and WDO) will be in a logic low state, regardless of the voltage at the inputs of the device, named as:

- SENSEx
- SR_UVLO
- WDI
- MODE

8.3.1.2 Power-On Reset (V_{IN} < V_{POR_IN})

When the voltage on V_{IN} is lower than the power on reset voltage (V_{POR_IN}), the output signal is undefined and is not to be relied upon for proper device function.

Figure 8-1 shows the RESETx outputs relationship to a rising input voltage (V_{IN}). As can be observed, the RESETx are undefined when V_{IN} is lower than V_{POR_IN} (typically 1.42V). During this time the outputs can be any value from 0V to V_{IN}.

In this example, the input voltages to all input comparators (SENSEx) are below the V_{TH_SENSEx} (typically 599.7mV). For this reason the RESETx, PWRGD and WDO stays low after V_{IN} rises above $UVLO_{RISE}$ (typically 2.79V).

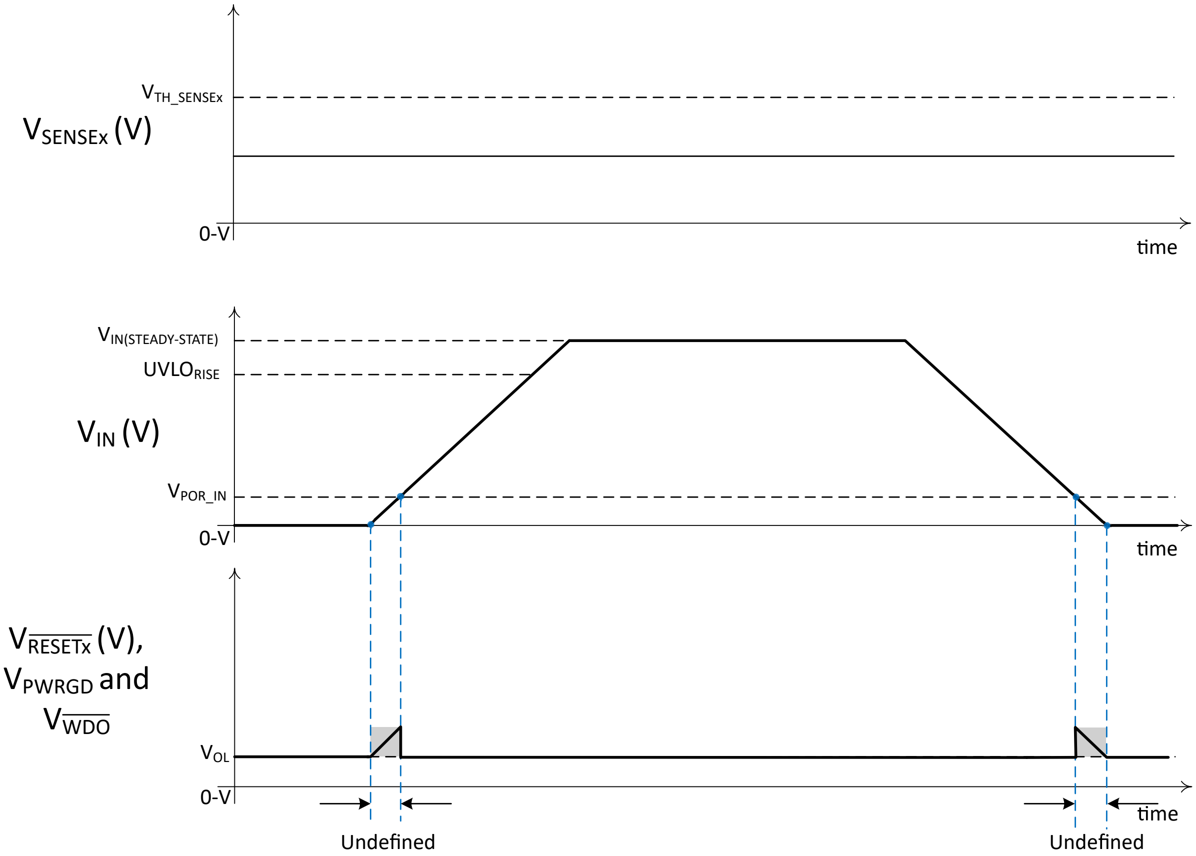


Figure 8-1. Outputs in a Valid Low State After V_{IN} > V_{POR_IN}

A. This figures assumes:

1. A valid external pull-up voltage is connected to the PULL_UPx inputs (1.6V ≤ V_{PULL_UPx} ≤ 7V).
2. $V_{IN(STEADY-SATE)}$ is a valid V_{IN} voltage between 3V to 14V.
3. All inputs are assumed to be of undervoltage (UV) type for this graph.
4. V_{OL} represents: $V_{OL\_\overline{RESETx}}$, V_{OL_PWRGD} and $V_{OL\_\overline{WDO}}$ or the low logic output voltage for all outputs.

8.3.2 SR_$\overline{\text{UVLO}}$

The SR_$\overline{\text{UVLO}}$ (system reset/undervoltage lockout) input pin allows for an external controller to propagate an external fault by asserting (or force low) all outputs at once. When SR_UVLO is low (< $V_{TH\_SR\_\overline{UVLO}\_FALLING}$) the device enters in shutdown mode and all outputs are forced logical low. As the SR_$\overline{\text{UVLO}}$ is the input to an accurate (± 3.17%) comparator with a rising threshold voltage of $V_{TH\_SR\_\overline{UVLO}\_RISING}$ = 602mVthe designer can use the pin to set a external undervoltage lock-out if desired (refer to Figure 8-2). A fixed hysteresis of 103mV is incorporated in the comparator for noise stability.

Usually the designer knows the voltage at which it's desired to enable the TPS7H3024. With that information we can calculate the resistive divider values using Equation 1. Usually the top resistor is fixed to a 10kΩ value, but any other value can be used. Using a larger value resistor will minimize power dissipation but can allow noise to couple into the outputs signal due a "weaker" pull-up.

$$R_{BOTTOM\_SR\_\overline{UVLO}} = R_{TOP\_SR\_\overline{UVLO}} \times \frac{V_{TH\_SR\_\overline{UVLO}\_RISING}}{V_{IN\_UVLO\_IDEAL} - V_{TH\_SR\_\overline{UVLO}\_RISING}} \tag{1}$$

where:

- $V_{TH\_SR\_\overline{UVLO}\_RISING}$ is the internal reference during a rising voltage in SR_$\overline{\text{UVLO}}$ (602mV typically).
  - Rather than use the typical value the designer can use the center to minimize the error across voltage, temperature and radiation as:

$$\frac{V_{TH\_SR\_\overline{UVLO}\_RISING(MIN)} + V_{TH\_SR\_\overline{UVLO}\_RISING(MAX)}}{2} = \frac{0.580\text{V} + 0.618\text{ V}}{2} = 0.599\text{V} \tag{2}$$

- $V_{IN\_UVLO\_IDEAL}$ is the desired external voltage to enable the device during a rising voltage in V_{IN}.
- $R_{TOP\_SR\_\overline{UVLO}}$ is the selected top resistor for the divider.

Once the designer knows the actual (real) resistive divider values, Equation 3 and Equation 4 can be used to calculate the nominal rising and falling external undervoltage lockout as:

$$V_{IN\_UVLO\_RISING\_NOMINAL}\left(\text{V}\right) = \left(1 + \frac{R_{TOP\_SR\_\overline{UVLO}}}{R_{BOTTOM\_SR\_\overline{UVLO}}}\right) \times V_{TH\_SR\_\overline{UVLO}\_RISING} \tag{3}$$

$$V_{IN\_UVLO\_FALLING\_NOMINAL}\left(\text{V}\right) = \left(1 + \frac{R_{TOP\_SR\_\overline{UVLO}}}{R_{BOTTOM\_SR\_\overline{UVLO}}}\right) \times V_{TH\_SR\_\overline{UVLO}\_FALLING} \tag{4}$$

In Equation 4 the designer can use the center across temperature, voltage and radiation (TID) as:

$$\frac{V_{TH\_SR\_\overline{UVLO}\_FALLING(MIN)} + V_{TH\_SR\_\overline{UVLO}\_FALLING(MAX)} +}{2} = \frac{0.475\text{V} + 0.517\text{ V}}{2} = 0.496\text{V} \tag{5}$$

During start-up the device needs to have an stable input voltage ($UVLO_{RISE}$ < V_{IN} < 14) for at least 2.8ms($t_{START\_UP\_DELAY}$). This is to ensure all internal time constants have been surpass. This will also ensure that the V_{TH_SENSEx} reference is settled and it's accuracy is within specifications (1%). When V_{IN} is a fast rising voltage an external delay capacitance can be add to the resistive divider to enable the device when the $t_{START\_UP\_DELAY}$ have been exceed. To select the capacitance (C_{DELAY}) for the SR_$\overline{\text{UVLO}}$ pin we can use Equation 6.

$$C_{DELAY}\left(\text{F}\right) > \frac{t_{DELAY}(s)}{R_{TH}\left(\Omega\right) \times \ln\left(-\frac{V_{TH}(V)}{V(t) - V_{TH}(V)}\right)} \tag{6}$$

where:

- t_{DELAY} (s) is the desired delay time in seconds (at least 2.8ms after V_{IN} > $UVLO_{RISE}$).
- R_{TH} is the Thévenin equivalent resistance. In this case the parallel between $R_{TOP\_SR\_\overline{UVLO}}$ and $R_{BOTTOM\_SR\_\overline{UVLO}}$ in ohms.

  - $$R_{TH}\left(\Omega\right) = \frac{R_{TOP\_SR\_\overline{UVLO}}\left(\Omega\right) \times R_{BOTTOM\_SR\_\overline{UVLO}}\left(\Omega\right)}{R_{TOP\_SR\_\overline{UVLO}}\left(\Omega\right) + R_{BOTTOM\_SR\_\overline{UVLO}}\left(\Omega\right)} \quad (7)$$
- V_{TH} is the Thévenin equivalent voltage. In this case the voltage at $V_{SR\_\overline{UVLO}}$ during steady state operation in volts.
  - $$V_{TH}\left(V\right) = \left(\frac{R_{BOTTOM\_SR\_\overline{UVLO}}\left(\Omega\right)}{R_{TOP\_SR\_\overline{UVLO}}\left(\Omega\right) + R_{BOTTOM\_SR\_\overline{UVLO}}\left(\Omega\right)}\right) \times V_{IN}\left(V\right) \quad (8)$$
- V(t) is the voltage at SR_$\overline{\text{UVLO}}$ ($V_{SR\_\overline{UVLO}}$) which will start the sequence up. In this case 0.602V.
  - We can use the center across temperature and voltage as specified on Equation 2.

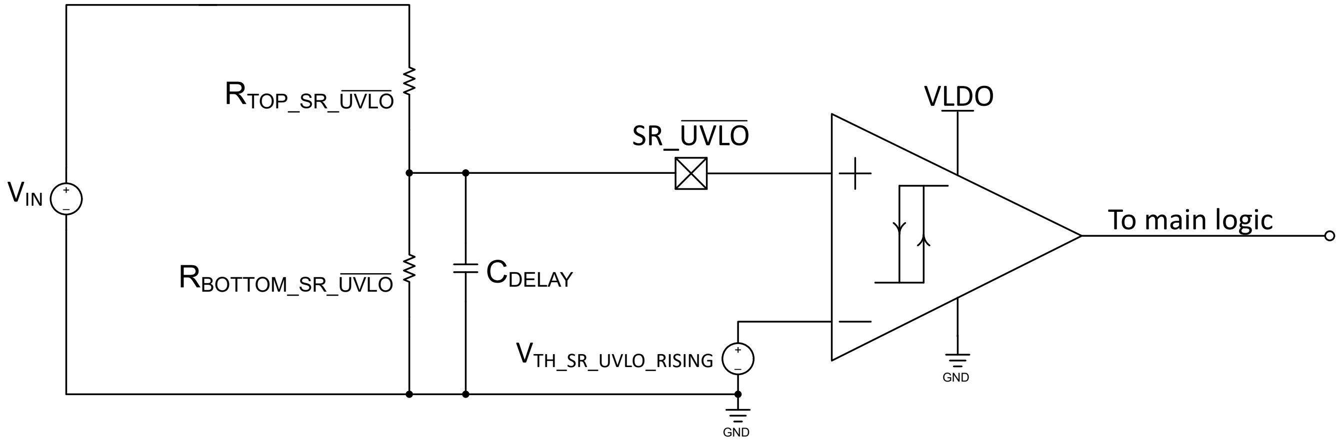
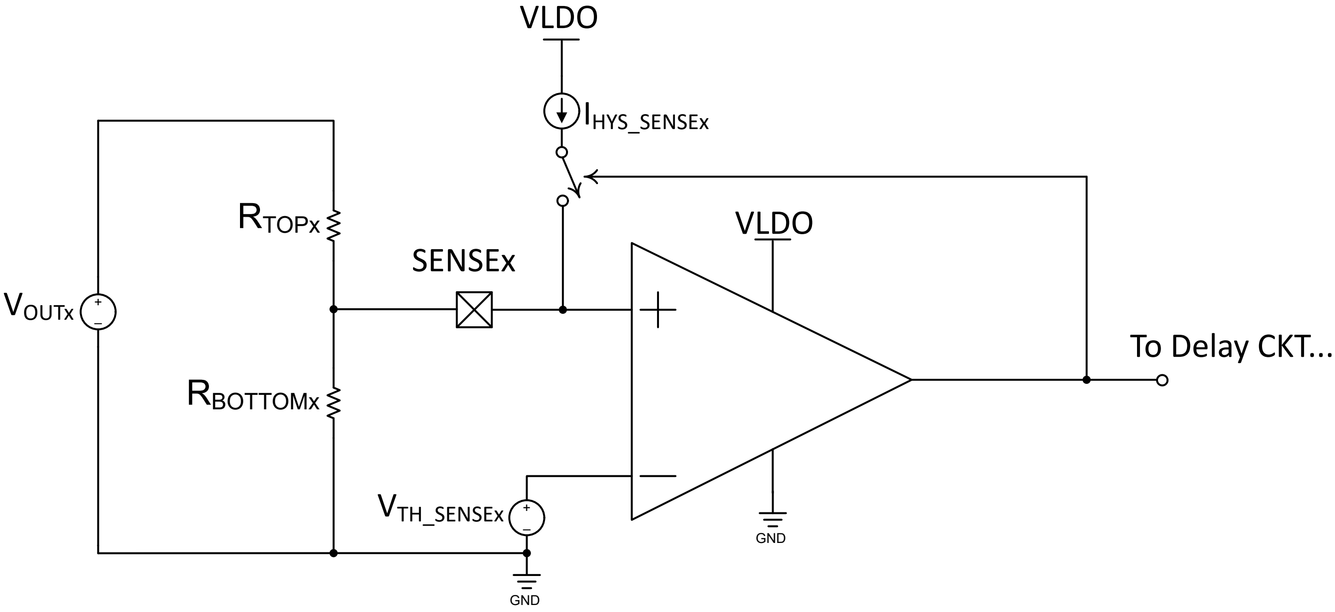


Figure 8-2. Monitor a Main Rail to Automatically Start the Sequence UP and $\overline{\text{DOWN}}$

8.3.3 SENSEx Inputs

8.3.3.1 V_{TH_SENSEX} and V_{OUTx_RISE}

The TPS7H3024 voltage supervisor integrates four input comparators, with an accurate (±1%) threshold voltage of 599.7mV (V_{TH_SENSEx}) nominal. V_{TH_SENSEx} is measured at the $\overline{\text{RESETx}}$ outputs to account for comparator offsets in the threshold. Maximum flexibility is provided as an external resistive dividers can be adjusted to sense a desired voltage rail (V_{OUTx}). Figure 8-3 shows a conceptual diagram of the comparators connected to the SENSEx inputs. As can be observed, the sensed voltage rail (V_{OUTx}) is attenuated (using an external resistive divider, R_{TOPx} and $R_{BOTTOMx}$) and compared against the V_{TH_SENSEx} voltage. Is recommended to maintain the steady-state SENSEx voltage below 1.6V, in order to maintain the threshold (V_{TH_SENSEx}) accuracy over lifetime.



Note

The comparator by itself does not have an built-in voltage hysteresis. The hysteresis is controlled externally using the hysteresis current (I_{HYS_SENSEx}) and the top resistor (R_{TOPx}). For more details refer to Section 8.3.3.4. The input comparator does not change for the undervoltage or overvoltage type. The overvoltage is implemented by inverting the signal that drives the output stage.

Figure 8-3. SENSEx Comparators Inputs

When the voltage at the monitored rail (V_{OUTx}) is rising, the hysteresis current (I_{HYS_SENSEx}) is not connected to the SENSEx input. The SENSEx (attenuated V_{OUTx}) voltage is compared to the internal reference (V_{TH_SENSEx}). When $V_{SENSEx} > V_{TH\_SENSEx}$ the voltage is considered as:

1. In regulation: for an undervoltage channel (UV).
2. Not in regulation: for an overvoltage channel (OV)

We can calculate the rising voltage threshold voltage on V_{OUTx} by doing a simple voltage divider as:

$$V_{OUTx\_RISE\_NOMINAL}\ \left(V\right) = \left(1 + \frac{R_{TOPx}}{R_{BOTTOMx}}\right) \times V_{TH\_SENSEx} \quad (9)$$

Where:

- V_{TH_SENSEx} is the nominal sense threshold voltage of 599.7mV.
  - If it is desired to minimize the error on the monitored voltage across temperature, the center can be used instead of the typical as: $V_{TH\_SENSEx} = \frac{V_{TH\_SENSEx(MIN)} + V_{TH\_SENSEx(MAX)}}{2} = 599\text{mV}$
- R_{TOPx} is the top resistor in Ω.
- $R_{BOTTOMx}$ is the bottom resistor in Ω.

As with any system, there is some variation (or errors) of the design variables, in this case the top, bottom resistors and the SENSEx threshold voltage (V_{TH_SENSEx}). Using the derivative method to calculate the total error (with the assumption that all variables are uncorrelated and both resistors have the same tolerance value), the $V_{TH\_RISEx\_NOMINAL}$ error can be calculated as:

$$V_{OUTx\_RISE\_ERROR}\ \left(V\right) = \pm\sqrt{\frac{V_{TH\_SENSEx}{}^2 \times \left[\left(2 \times R_{TOL}{}^2 \times R_{TOPx}{}^2\right) + \left(V_{TH\_SENSEx\_ACC}{}^2 \times \left(R_{TOPx} + R_{BOTTOMx}\right)^2\right)\right]}{R_{BOTTOMx}{}^2}} \quad (10)$$

Where:

- R_{TOL} is the resistors tolerance (same for top and bottom resistors) as numeric value. For example, for 0.1% tolerance resistors, we use 0.001.
- $V_{TH\_SENSEx\_ACC}$ is the SENSEx threshold accuracy as numeric value (in this case 0.01).
- R_{TOPx} and $R_{BOTTOMx}$ are in Ohms (Ω).
- V_{TH_SENSEx} is 0.599 Volts (center across temperature).

Using Equation 9 and Equation 10 we can calculate the rising voltage threshold range as:

$$V_{OUTx\_RISE} = V_{OUTx\_RISE\_NOMINAL} \pm V_{OUTx\_RISE\_ERROR} \quad (11)$$

Note

Remember V_{TH_SENSEx} is the reference voltage when accounting for the comparator offsets $V_{TH\_SENSEx} = V_{REF} + V_{IOx}$.

Although it is not required, in noisy applications it is good analog design practice to place a small bypass capacitor at the SENSEx inputs in order to reduce sensitivity to transient voltages on the monitored signal.

8.3.3.2 I_{HYS_SENSEx} and V_{OUTx_FALL}

The TPS7H3024 has a built-in hysteresis current of 24µA with an accuracy of ±3% (with R_{HYS} = 49.9kΩ). The hysteresis current is approximately equivalent to V_{HYS}/R_{HYS}. A tolerance of 0.1% for the R_{HYS} is recommended as it ultimately affects the accuracy of the hysteresis current. This current is mirrored internally across all SENSEx inputs. This hysteresis current becomes active when the SENSEx voltage is greater than the threshold voltage (599.7mV ± 1%), same as $V_{OUTx} > V_{OUTx\_RISE}$ (refer to Equation 11 and Figure 8-3). This current (I_{HYS_SENSEx}) multiplied by the R_{TOPx} resistance induces a voltage (V_{HYS_SENSEx}) that is added to the SENSEx node. This effectively boost (or increments) the node voltage (in this case V_{SENSEx}).

When V_{OUTx} voltage is falling and becomes lower than V_{OUT_FALLx} it will be considered as:

1. Not in regulation: for an undervoltage channel (UV).
2. In regulation: for an overvoltage channel (OV).

The hysteresis voltage is defined as:

$$V_{HYS\_SENSEx\_NOMINAL}\ \left(V\right) = I_{HYS\_SENSEx} \times R_{TOPx} \quad (12)$$

Where:

- $I_{HYS\_SENSEx} = 24 \times 10^{-6}$ Amps (or 24µA)
- R_{TOPx} units are in Ohms (Ω)

The falling voltage threshold can be calculated as:

$$V_{OUTx\_FALL\_NOMINAL}\ (V) = V_{OUTx\_RISE\_NOMINAL} - V_{HYS\_SENSEx\_NOMINAL} \tag{13}$$

Using Equation 9 and Equation 13

$$V_{OUTx\_FALL\_NOMINAL}\left(V\right) = \left[\left(1 + \frac{R_{TOPx}}{R_{BOTTOMx}}\right) \times V_{TH\_SENSEx}\right] - \left(I_{HYS\_SENSEx} \times R_{TOPx}\right) \tag{14}$$

Where:

- V_{TH_SENSEx} is the nominal sense threshold voltage of 0.599V
- $I_{HYS\_SENSEx} = 24 \times 10^{-6}$ Amps (or 24µA)
- R_{TOPx} and $R_{BOTTOMx}$ units are in Ohms (Ω)

The V_{OUTx_FALL} error can be calculated as:

$$V_{TH\_FALLx\_ERROR}\left(V\right) = \pm\sqrt{\frac{A + B + C + D}{R_{BOTTOMx}{}^{2}}} \tag{15}$$

Equation 15 was obtain, using the derivative method and under the assumptions that all variables are uncorrelated and both resistors have the same tolerance

Where the equation terms are:

$$A = I_{HYS\_SENSEx}{}^{2} \times I_{HYS\_SENSEx\_ACC}{}^{2} \times R_{TOPx}{}^{2} \times R_{BOTTOMx}{}^{2} \tag{16}$$

$$B = R_{TOL}{}^{2} \times R_{TOPx}{}^{2} \times V_{TH\_SENSEx}{}^{2} \tag{17}$$

$$C = R_{TOL}{}^{2} \times R_{TOPx}{}^{2} \times \left[\left(I_{HYS\_SENSEx} \times R_{BOTTOMx}\right) - V_{TH\_SENSEx}\right]^{2} \tag{18}$$

$$D = V_{TH\_SENSEx}{}^{2} \times V_{TH\_SENSEx\_ACC}{}^{2} \times \left(R_{TOPx} + R_{BOTTOMx}\right)^{2} \tag{19}$$

Where:

- R_{TOL} is the resistors tolerance (same for top and bottom resistors) as numeric value. For example, for 0.1% tolerance resistors, we use 0.001.
- $V_{TH\_SENSEx\_ACC}$ is the SENSEx threshold accuracy as numeric value (in this case 0.01).
- $I_{HYS\_SENSEx\_ACC}$ is the hysteresis current accuracy as numeric value (in this case 0.03).
- V_{TH_SENSEx} is the nominal sense threshold voltage of 0.599V.
- $I_{HYS\_SENSEx} = 24 \times 10^{-6}$ Amps (or 24µA).
- R_{TOPx} and $R_{BOTTOMx}$ units are in Ohms (Ω).

Using Equation 14 and Equation 15 we can calculate the falling voltage range as:

$$V_{OUTx\_FALL} = V_{OUTx\_FALL\_NOMINAL} \pm V_{OUTx\_FALL\_ERROR} \tag{20}$$

Figure 8-4, shows a conceptual diagram of the rising and falling voltage, it also shows the errors on this voltage due to V_{TH} accuracy, I_{HYS} accuracy, and the resistive divider tolerances. At the system level, these errors have to be taken into account for a robust design.

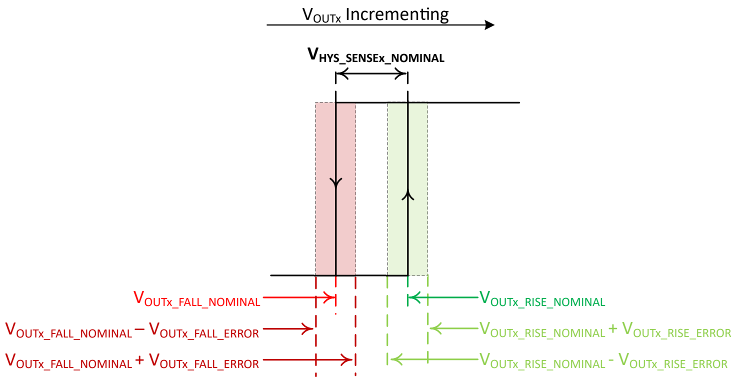
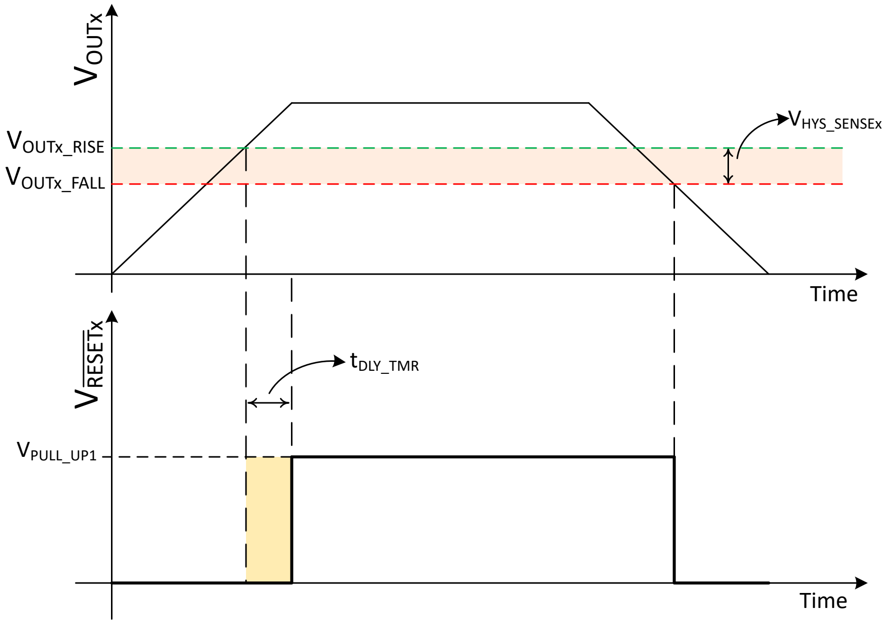


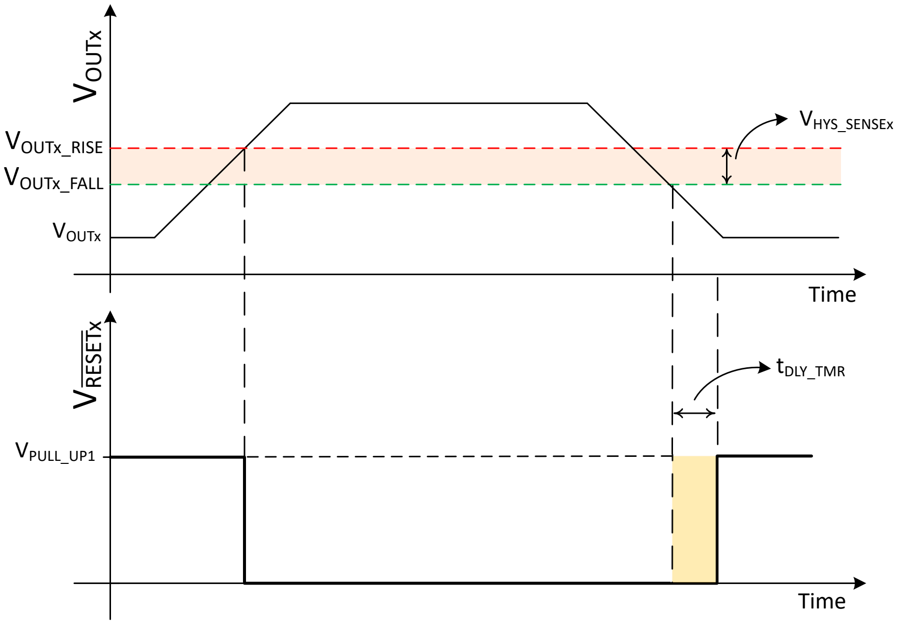
Figure 8-4. Rising and Falling Thresholds Voltages for the SENSE$_x$ Comparators

8.3.3.3 Input to Output Time Diagrams



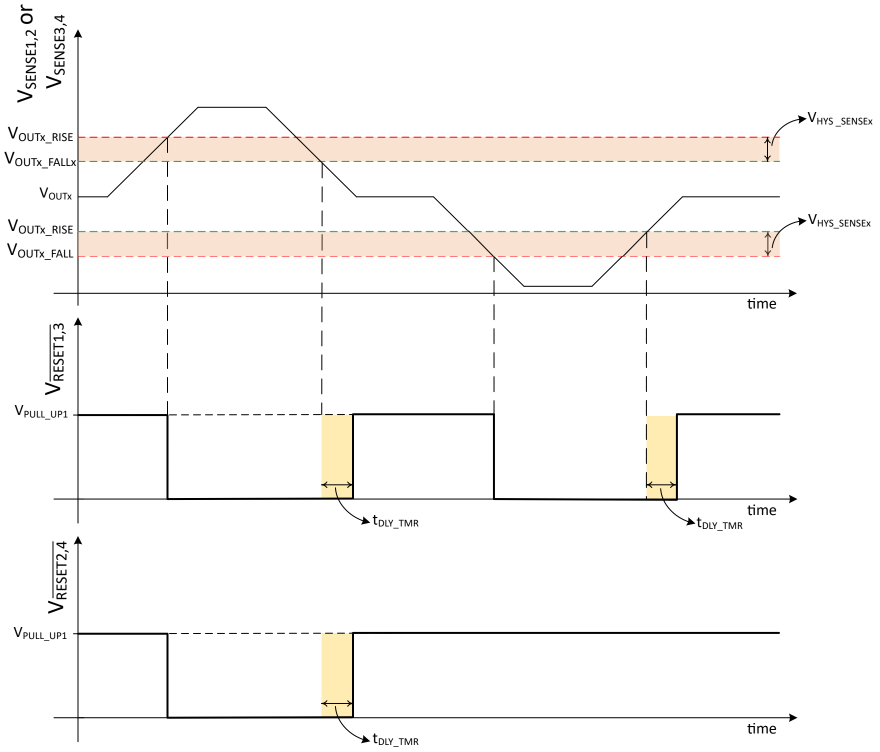
A. In TPS7H3024 the channel # 1 (pin # 1) and channel # 3 (pin # 3) are of undervoltage type, when MODE=0.

Figure 8-5. Undervoltage channel (UV) time diagram



A. In TPS7H3024 the channel # 2 (pin # 2) and channel # 4 (pin # 4) are of overvoltage type, when MODE=1.

Figure 8-6. Overvoltage channel (OV) time diagram



A. In TPS7H3024 the channel # 1 (pin # 1) and channel # 2 (pin # 2) are internally or'ed to create a window channel while the channel # 3 (pin # 3) and channel # 4 (pin # 4) are or'ed to create a second window channel, when MODE=1

B. V_{OUTx_RISE},V_{OUTx_FALL} and V_{HYS_SENSEx} for the undervoltage and overvoltage can be different values.

Figure 8-7. Window channel time diagram

8.3.3.4 Top and Bottom Resistive Divider Design Equations

At the system level the designer knows (or selects) the V_{OUTx_RISE} and V_{OUTx_FALL} levels. Usually these voltages are selected as percentages of the nominal rail voltage (V_{OUTx}) being monitored. Knowing this information, we can calculate the nominal resistive divider components values (R_{TOPx} and $R_{BOTTOMx}$) for the desired target levels. Using Equation 12 and Equation 13 we can calculate the top resistor as:

$$R_{TOPx} = \frac{V_{OUTx\_RISE} - V_{OUTx\_FALL}}{I_{HYS\_SENSEx}} \tag{21}$$

From Equation 9 we can calculate the bottom resistor as:

$$R_{BOTTOMx} = \frac{R_{TOPx} \times V_{TH\_SENSEx}}{V_{OUTx\_RISE} - V_{TH\_SENSEx}} \tag{22}$$

It's important to notice that the larger the separation between V_{OUTx_RISE} and V_{OUTx_FALL} (referred as V_{HYS_SENSEx}), the bigger the error in the falling voltage. Figure 8-8 shows a plot of the error in the V_{OUTx_FALL} for different sense hysteresis voltages ($V_{HYS\_SENSEx} = V_{OUTx\_RISE} - V_{OUTx\_FALL}$). The plot is created for three different V_{OUTx_RISE} voltages (or percentages of the nominal output voltage as 90, 95, and 97%) and two different output voltages (0.8V and 28V). As can be observed, the output voltage has very little impact on the falling voltage error (differences cannot be appreciated on the plot). The error (in percent) can go from approximately 1% (at V_{HYS_SENSEx} = 3%) to around 2.6% (at V_{HYS_SENSEx} = 80%).

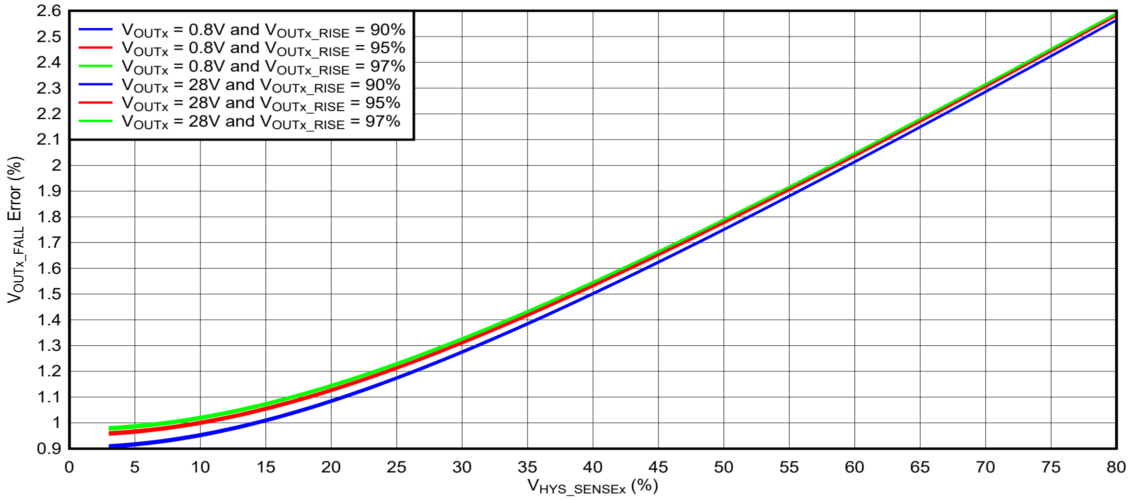


Figure 8-8. V_{OUTx_FALL} Absolute Error vs V_{HYS_SENSEx}

A. This plot does not includes the error on the V_{OUTx_FALL} due to the difference between the calculated top and bottom resistors using Equation 21 and Equation 22 and the actual resistance values that a designer can procure.
B. The resistor tolerance used for the calculation is 0.1%, V_{TH_SENSEx} accuracy is 1%, and the I_{HYS_SENSEx} accuracy is 3%.
C. In this plot the V_{HYS_SENSEx} (%) represents the separation as percentages of the nominal output voltage (V_{OUTx}).
D. In this plot, the V_{OUTx_FALL} error in % is normalized with respect to the full-scale voltage (or V_{OUTx}).

8.3.4 MODE

The mode pin is an input that change the behavior of the output stage to detect for:

1. Undervoltage (UV)
2. Overvoltage (OV)
3. Window

For more details refer to Table 8-1, Section 8.3.5.

ADVANCE INFORMATION

Note

MODE can be connected to the VLDO for a logical high. Use a series resistor for isolation and protection.

8.3.5 Output Stages ($\overline{\text{RESETx}}$, PWRGD, $\overline{\text{WDO}}$, PULL_UP1 and PULL_UP2)

The output stage's ($\overline{\text{RESET1}}$ to $\overline{\text{RESET4}}$), PWRGD and $\overline{\text{WDO}}$ are offered in push-pull type. When the output are of overvoltage type the $\overline{\text{RESETx}}$ is driven logically inverted from the output of the SENSEx comparators as shown in Figure 8-9 (also refer to Figure 8-13) .

In the case of the TPS7H3024 (push-pull outputs) with MODE=1, the SENSE1 (UV) and SENSE2 (OV) are internally or'ed and the output is used to drive the $\overline{\text{RESET1}}$ output. In this case $\overline{\text{RESET1}}$ is the output of a window comparator. $\overline{\text{RESET2}}$ is left unchanged and will be the OV flag of SENSE2. As both the window and the OV flag are available the system can interrogate the outputs to known which type of fault occur in the system (UV or OV). The same is true for SENSE3 and SENSE4, which form the second window comparator.

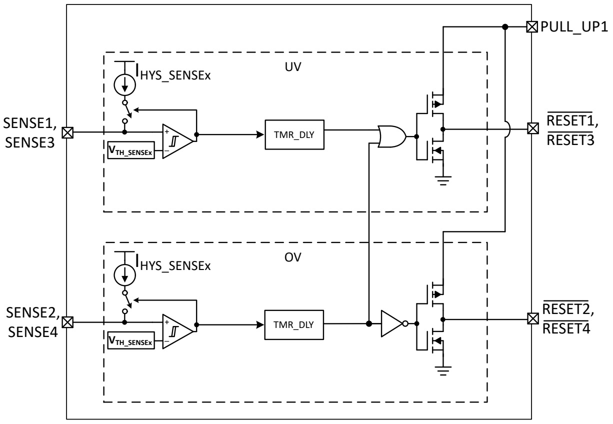


Figure 8-9. Window Comparator for TPS7H3024 when MODE=1

A. SENSE1 and SENSE2 are one window comparator channel while SENSE3 and SENSE4 create the second window comparator channel.

8.3.5.1 Push-Pull Outputs

The pull-up voltage for the push-pull outputs is externally provided by the user. PULL_UP1 (input) is the pull-up voltage domain for all $\overline{\text{RESETx}}$ outputs ($\overline{\text{RESET1}}$ to $\overline{\text{RESET4}}$), while PULL_UP2 (input) is the pull-up voltage domain for the PWRGD and $\overline{\text{WDO}}$ outputs. Refer to Figure 8-10 to Figure 8-13.

Note

There are no sequencing requirements for IN, PULL_UP1, and PULL_UP2.

Note

PULL_UPx inputs must be decouple with a 1μF ceramic capacitor as close to the pins as possible. This is to clean the voltages signals at the outputs: $\overline{\text{RESETx}}$, PWRGD and $\overline{\text{WDO}}$.

Each output stage consists of a PMOS/NMOS (CMOS) pair. The PMOS resistance is typically 9Ω (max of 20Ω) while the NMOS is 16Ω typically (max of 36Ω), when $V_{PULL\_UPx} \geq 3.3V$. PULL_UP1 and PULL_UP2, have a voltage range of 1.6V to 7V, and can be independently biased or tied to the same voltage rail, however both most be biased. The output resistance of the PMOS leg has a PULL_UPx voltage dependency. The lower the PULL_UPx voltage, the higher the PMOS resistance.

When $V_{IN} < V_{POR\_IN}$ (2V maximum) or $V_{PULL\_UPx} > V_{POR\_PULL\_UPx}$ (1.1V maximum) the output are in a known pull-down state. At this condition the outputs have reduced sinking capabilities with $V_{OL} \leq 320mV$ when the device is sinking 100µA of current into the outputs:

- $\overline{\text{RESETx}}$
- PWRGD
- $\overline{\text{WDO}}$

Once the input voltage range is withing the recommended input voltage range of 3V to 14V, the outputs have the full strength capabilities of ±10mA, per output.

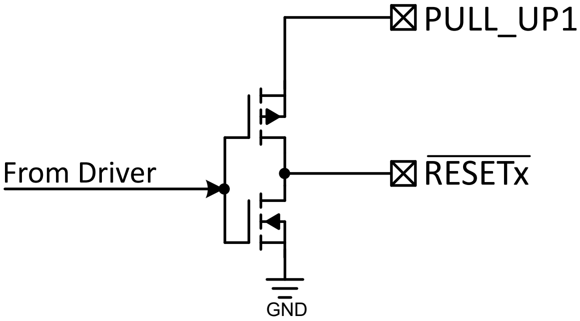


Figure 8-10. $\overline{\text{RESETx}}$ Push-Pull Output Stages for UV Channel Type

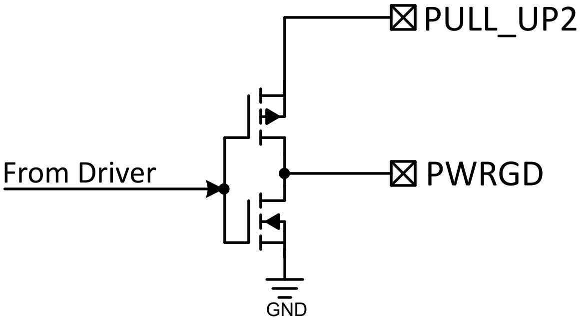


Figure 8-11. PWRGD Push-Pull Output Stage for UV Channel Type

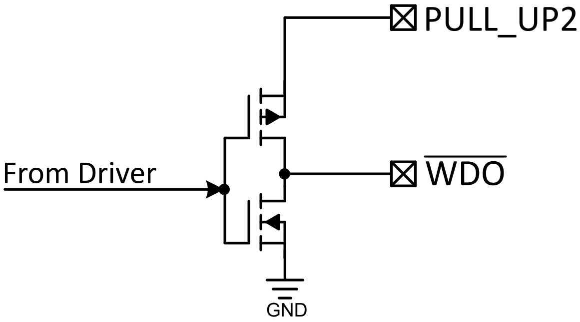
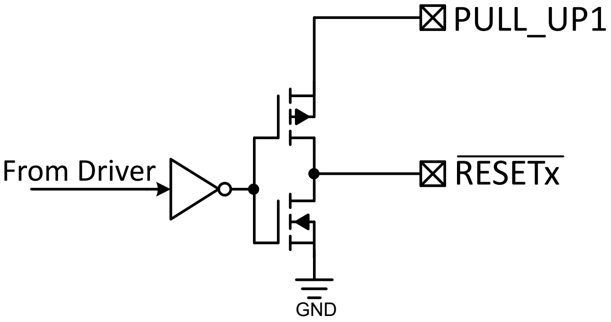


Figure 8-12. $\overline{\text{WDO}}$ Push-Pull Output Stage for UV Channel Type



A. Only the $\overline{\text{RESETx}}$ are dependent on the type of channel as: UV or OV. This is dependent in the logical value of the MODE input pin.

Figure 8-13. $\overline{\text{RESETx}}$ Push-Pull Output Stages for OV Channel Type

8.3.6 WDI

The watchdog input (WDI) pin is the input of the non-inverting input of a comparator with a stable 602mV voltage reference ($V_{TH\_WDI\_RISING}$). The comparator have a built-in 104mV (fixed) hysteresis voltage for noise stability. The watchdog state machine will clear (or reset the watchdog counter) every time a rising voltage is detected on the WDI pin. Due to inaccuracies on the watchdog timer the rising voltage edge in WDI should be sent by the processor by the $t_{WD\_TMR(MIN)}$. The WD_TMR (or timeout) an be programmed by the user using the WD_TMR input. The timer have a programmable range of 500ms to 1.5s. For more details refer to Section 8.3.7.2.

8.3.7 User-Programmable TIMERS

The TPS7H3024 has two adjustable timers:

1. DLY_TMR with a range of 260µs to 23.37ms, nominally.
2. WD_TMR with a range of 0.52s to 1.5s, nominally.

Both timers are programmed via a single resistor from the DLY_TMR and WD_TMR pins to GND. The resistors are used to program the internal oscillator frequency of the timers. Leaving the DLY_TMR or the WD_TMR pin floating will disable the timer, respectively. Disabling a timer reduces the quiescent (I_{Q_IN}) current of the device.

Note

Timers resistors conditions must be valid at power up and must not be dynamically changed.

8.3.7.1 DLY_TMR

The TPS7H3024 includes an adjustable time delay. A single resistor connected between the DLY_TMR pin and GND will program the delay. Possible resistor (R_{DLY}) values are between 10.5kΩ and 1.18MΩ for a 260µs to 23.7ms delay, respectively. This delay is valid only during the out-of-fault conditions as follow:

1. UV: in the undervoltage channel (UV) the delay is valid when V_{OUTx} voltage is rising and crosses the V_{OUTx_RISE}.
2. OV: in the overvoltage channel (OV) the delay is valid when the V_{OUTx} voltage is falling and crosses the V_{OUTx_FALL}.

For more details refer to Figure 8-5 and Figure 8-6.

If no delay is preferred for the system, the pin (DLY_TMR) can be left floating. Disabling the timer results in a reduced current consumption on the device (I_{Q_IN}). When no delay is preferred, an inherent propagation delay of 4.3µs (max) will be observed, between V_{OUTx} crossing the V_{OUTx_RISE} and V_{OUTx_FALL}.

The DLY_TMR resistor can be selected using Equation 23. Figure 8-14 shows the linear trend between the DLY_TMR resistor and the delay time.

$$R_{DLY\_TMR}(k\Omega) = \left[49.71 \times t_{DLY\_TMR}(ms)\right] - 2.5 \quad (23)$$

Table 8-2 shows nominal resistors value for different delay times.

Table 8-2. Typical DLY_TMR Resistors

Delay (ms)	R_{DLY_TMR} (kΩ)
0.260	10.5
12.5	619
23.7	1180

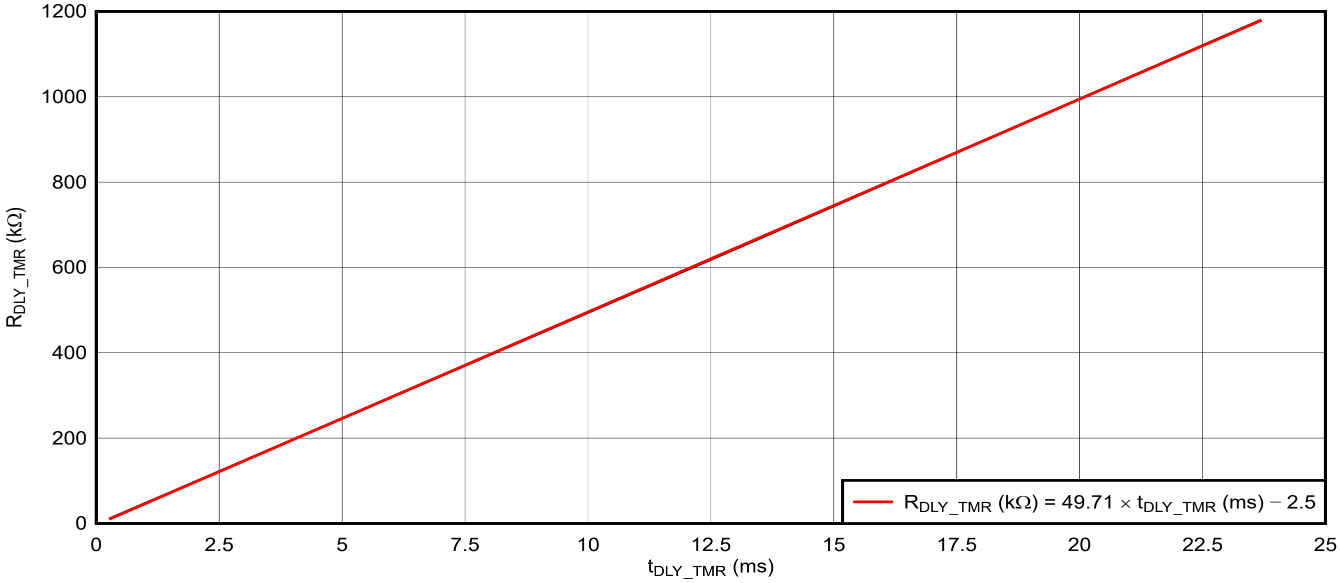


Figure 8-14. R_{DLY_TMR} vs t_{DLY_TMR} Across Full Oscillator Range

8.3.7.2 WD_TMR

The WD_TMR is an adjustable timer that programs the time-out of the internal watchdog timer. The watchdog timer is commonly used to monitor coherent processor execution. If the monitored processor is halted due to a fault, the WDI pin will not detect a rising edge resulting in asserting the $\overline{\text{WDO}}$ low, hence resetting the processor to a known state. A typical connection between the monitored processor and the TPS7H3024 is shown in Figure 8-15. Figure 8-16 shows the correct and incorrect (late pulse) handshake between the processor and the watchdog in the TPS7H3024

The user can program the WD_TMR using a single resistor between the WD_TMR pin and GND. The range of the resistor (R_{WD}) is between 56.2kΩ to 174kΩ, for a 520ms to 1.5s, respectively. If the user does not want to use the watchdog timer, the pin can be left floating. Disabling the watchdog timer reduces the quiescent (I_{Q_IN}) current of the device.

Note

When the watchdog timer is disabled (by floating the WD_TMR pin), the $\overline{\text{WDO}}$ pin is forced high.

The REG_TMR resistor can be selected using Equation 24. Figure 8-17 shows the linear trend between the WD_TMR resistor and the allowed time to clear the watchdog timer (or time-out).

$$R_{WD\_TMR}(k\Omega) = [114.5 \times t_{WD\_TMR}(ms)] - 3.5 \qquad (24)$$

Table 8-3 shows typical resistor values for different allowed regulation times.

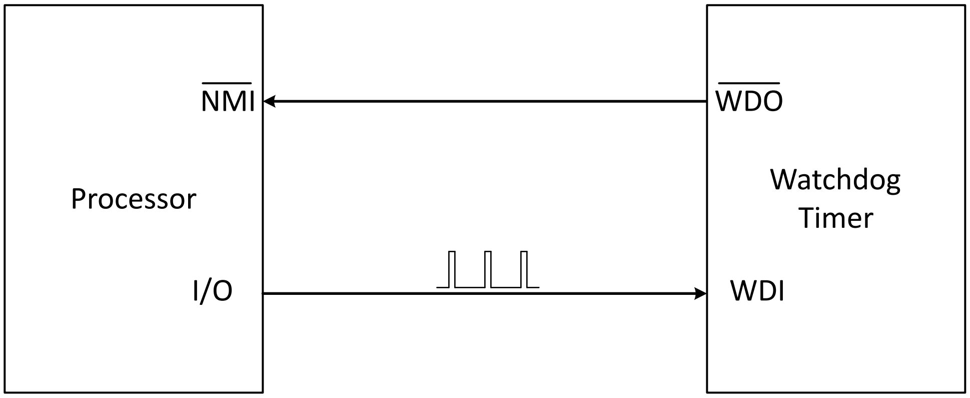


Figure 8-15. Watchdog timer typical handshake between TPS7H3024 and monitored processor

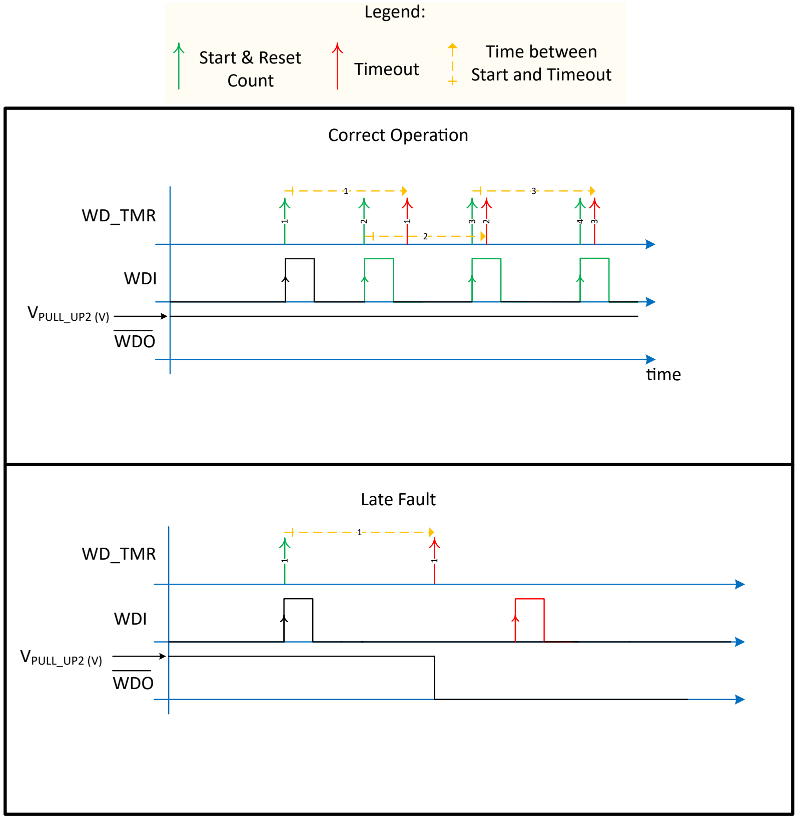


Figure 8-16. Watchdog Timing Diagram

Table 8-3. Typical REG_TMR Resistors

Allowed Regulation Time (ms)	R_{REG_TMR} (kΩ)
0.52	56.2
1	118
1.5	174

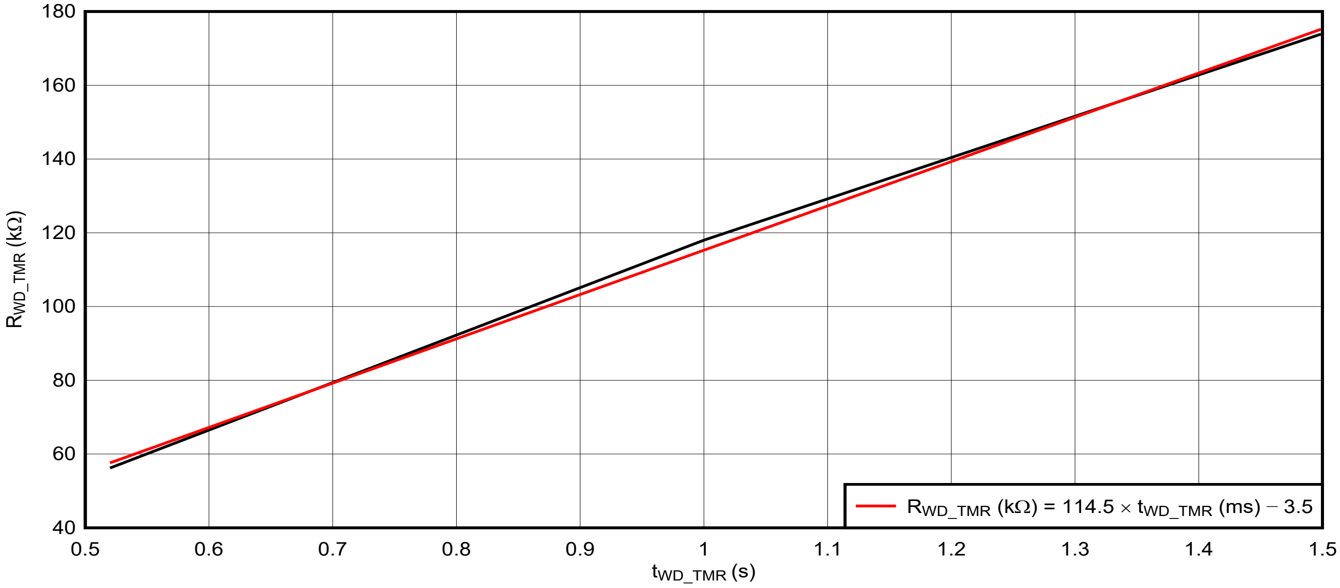


Figure 8-17. R_{WD_TMR} vs t_{WD_TMR} Across Full Oscillator Range

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H3024 is a radiation hardened 4-channel voltage supervisor with a watchdog timer. It can be used to supervise FPGAs, ASICs, AFEs, and various power systems voltage rails and processor coherent execution.

9.2 Typical Application

9.2.1 Window Voltage Monitoring

In many modern systems (or sub-systems), multiple voltage rails are often needed (we refer to this as the power tree). Often these power trees have tight voltage specification for reliable operation. If these specifications are not satisfied unreliable operation or permanent malfunction can happen. For these purposes the voltage rails are supervised on real time and corrective action (such as power-down, disabling local regulators, etc.) is propagated trough the system.

In this example 2 voltage rails are monitored using a window trigger to ensure the rails are operating within specification. Detailed design procedure and component selection is provided below. The design is summarized in Figure 9-1.

Note

All calculated numbers shown in this example are rounded to two decimal places with the exemption of the bottom resistor for the sense divider which are rounded to 3 decimal places.

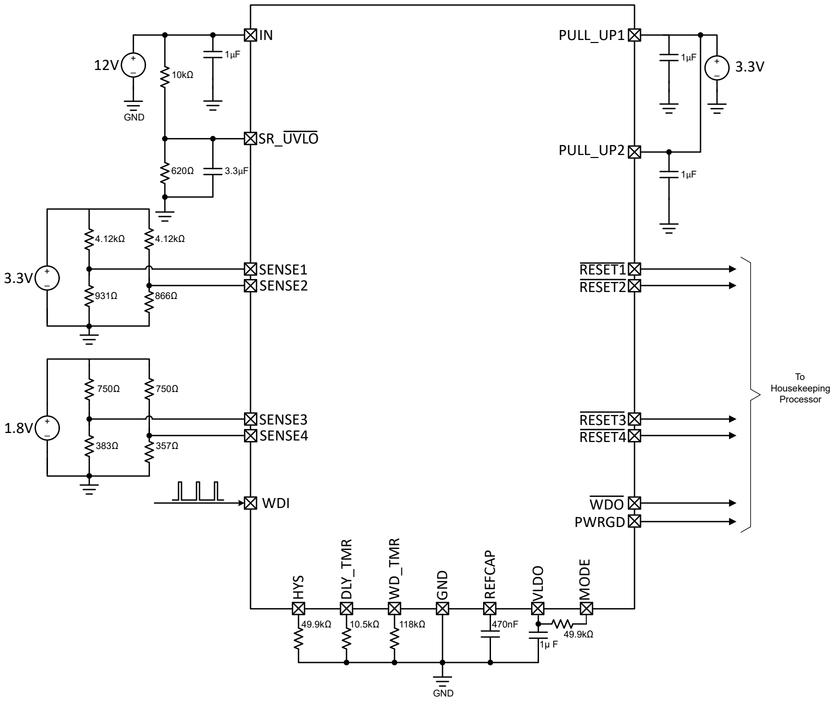


Figure 9-1. Window Voltage Monitoring with Watchdog

9.2.1.1 Design Requirements

This design requires to monitor two voltage rails using window comparators, to ensure reliable operation. As window supervision is used the upper and lower system specification bounds are monitored. In addition coherent processor execution is monitored using the watchdog. The supervisor I.C. is set to start around 86% (or 10.31V) of the nominal 12V rail, using an external resistive divider driving the SR_$\overline{\text{UVLO}}$ pin.

All flags are assumed to be monitored by a house-keeping processor, and the $\overline{\text{WDO}}$ is used to drive the non-maskable interrupt of the processor. All design conditions are defined in Table 9-1.

Table 9-1. Design Conditions

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
System nominal voltage	Monitor the 12V input voltage to the supervisor and enable the I.C. when the voltage is greater than 10.3V (86%) for at least 2.8ms. When the voltage decrements below 8.5V (or 71%) the system is disabled.	The TPS7H3024 can be accurately externally enabled by using the SR_$\overline{\text{UVLO}}$. The internal reference is accurate to 3.1% across temperature, voltage and TID. For minimal error, it is recommended to use 0.1% tolerance resistors.
V_{OUT1}= 3.3V (nominal)	Undervoltage with: $V_{OUT1\_RISE\_UV}$ = 98% and $V_{OUT1\_FALL\_UV}$ = 95%	$V_{OUT1\_RISE\_UV}$ = 3.25V $V_{OUT1\_FALL\_UV}$ = 3.15V
	Overvoltage with: $V_{OUT1\_RISE\_OV}$ = 105% and $V_{OUT1\_FALL\_OV}$ = 102%	$V_{OUT1\_RISE\_OV}$ = 3.45V $V_{OUT1\_FALL\_OV}$ = 3.35V
V_{OUT2}=1.8V (nominal)	Undervoltage with: $V_{OUT2\_RISE\_UV}$ = 98% and $V_{OUT2\_FALL\_UV}$ = 97%	$V_{OUT2\_RISE\_UV}$ = 1.77V $V_{OUT2\_FALL\_UV}$ = 1.75V
	Overvoltage with: $V_{OUT2\_RISE\_OV}$ = 103% and $V_{OUTx\_FALL\_OV}$ = 102%	$V_{OUT2\_RISE\_OV}$ = 1.86V $V_{OUT2\_FALL\_OV}$ = 1.84V
$\overline{\text{RESETx}}$ delay during the out-of-fault state	Delay of 260μs nominal	R_{DLY_TMR} = 10.5kΩ
Watchdog timeout	1 second nominal	R_{WD_TMR} = 118kΩ

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Input Power Supplies and Decoupling Capacitors

The TPS7H3024 has three input power supplies:

1. IN, the input supply to provide power to the TPS7H3024 IC. This power supply must be de-couple with at least 1μF or greater as close to the pin as possible. In this application, V_{IN} = 12V.
2. PULL_UP1, which is the input supply to program the $\overline{\text{RESETx}}$ output voltage high (V_{OH}). These outputs are connected to the house-keeping processor. This power supply must be de-couple with at least 1μF or greater as close to the pin as possible. In this application, the V_{PULL_UP1} = 3.3V.
3. PULL_UP2, which is the input supply to program the output voltage high (V_{OH}) of PWRGD and $\overline{\text{WDO}}$ outputs. These outputs are connected to the house-keeping processor, in particular $\overline{\text{WDO}}$ is usually connected to the$\overline{\text{NMO}}$ of the processor that is generating the WDI pulse. This power supply must be de-couple with at least 1μF or greater as close to the pin as possible. In this application, the V_{PULL_UP1} = 3.3V.

The TPS7H3024 also has two regulated voltage outputs that need to be decoupled for good electrical and radiation performance. These are:

1. REFCAP, the 1.2V reference, used internally in the device to generate all radiometric voltage reference such as:
    - V_{TH_SENSEx}
    - I_{HYS_SENSEx}
    - $V_{TH\_SR\_\overline{UVLO}}$

- V_{TH_WDI}
- V_{TH_MODE}

Decouple this reference with a 470nF ceramic capacitor as close to the pin as possible. Do not load this pin externally.

2. VLDO, this is the output of the internal regulator used to provide power to the internal circuits on the TPS7H3024. Decouple this regulator with at least 1µF as close to the pin as possible. This LDO can be loaded up to 5mA. Is important to understand that this LDO is not protected for short circuits.

9.2.1.2.2 SR_$\overline{\text{UVLO}}$ Threshold

In this application the SR_$\overline{\text{UVLO}}$ pin is used to monitored the input voltage supply of 12V and enable the device when the desired voltage is reach.

The I.C. is enabled when the rail voltage is greater than 10.26V (or 85.5% of the nominal voltage, typically). The falling voltage is not controlled as the hysteresis voltage on the SR_$\overline{\text{UVLO}}$ is internally controlled. However is calculated to be 8.55V (or 71.2% of the nominal voltage, typically). As the TPS7H3024 has an internal time constant ($t_{Start\_up\_delay}$) of 2.8ms (max), a delay capacitor of 3.3µF is added to SR_$\overline{\text{UVLO}}$ pin. This capacitor is added to introduce a delay in the SR_$\overline{\text{UVLO}}$ pin when V_{IN} is rising. This capacitor adds a second condition to start the sequence up, if $V_{IN} \geq 10.26V$ (typ) for at least 2.8ms then the I.C. is enabled.

Fixing the upper resistor for the resistive divider in SR_$\overline{\text{UVLO}}$, we can calculate the bottom resistor per our design requirements. The upper resistor is fixed to 10kΩ. Using the equation in Equation 1 the bottom resistor is calculated as:

$$V_{BOTTOM\_SR\_\overline{UVLO}} = 10k\Omega \times \frac{0.599V}{10.26V - 0.599V} = 620\Omega \tag{25}$$

Now that the reference resistor is calculated, we can select the actual (or real) resistor. In this case 0.1% tolerance resistor is used to select the closest value (in this specific case the reference and real resistor is the same)

- $R_{BOTTOM\_SR\_\overline{UVLO}} = 620\Omega$

With the actual resistor values, we can back-calculate the rising and falling voltages that enables and disables the supervisor (I.C.), respectively. Using Equation 3 and Equation 4 as:

$$V_{IN\_UVLO\_RISING\_NOMINAL}\left(V\right) = \left(1 + \frac{10\ k\Omega}{620\ \Omega}\right) \times 0.599\ V \cong 10.26\ V \tag{26}$$

$$V_{IN\_UVLO\_FALLING\_NOMINAL}\left(V\right) = \left(1 + \frac{10\ k\Omega}{620\ \Omega}\right) \times 0.496\ V \cong 8.50\ V \tag{27}$$

The delay capacitor is calculated using Equation 7, Equation 8 and Equation 6 as:

$$R_{TH}\left(\Omega\right) = \frac{10\ k\Omega \times 620\ \Omega}{10\ k\Omega + 620\ \Omega} = 583.80\ \Omega \tag{28}$$

$$V_{TH}\left(\Omega\right) = \left(\frac{620\ \Omega}{10\ k\Omega + 620\ \Omega}\right) \times 12\ V = 0.70\ V \tag{29}$$

$$C_{DELAY}\left(F\right) \geq \frac{0.0028\ s}{582.8\ \Omega \times \ln\left(-\frac{0.7\ V}{0.599\ V - 0.7\ V}\right)} = 2.48\ \mu F \tag{30}$$

The delay capacitor is selected as 3.3µF.

9.2.1.2.3 SENSEx Thresholds

The SENSEx inputs are used to monitor the voltage rails against system level bounds (or limits). For this design the output voltages to be monitored are:

1. V_{OUT1} = 3.3V
2. V_{OUT2} = 1.8V

The design V_{OUTx_RISE} and V_{OUTx_FALL} for each rail is specified in Table 9-2

Table 9-2. Rise and Fall Design Requirement by Channel

Channel #	Channel Type	V_{OUTx_NOM} (V)	V_{ONx_RISE} (%)	V_{ONx_RISE} (V)	V_{ONx_FALL} (%)	V_{ONx_FALL} (V)
1	UV	3.3	98	3.23	95	3.14
2	OV		105	3.47	102	3.37
3	UV	1.8	98	1.76	97	1.75
4	OV		103	1.85	102	1.84

Using Equation 21 and Equation 22 we can calculate the top and bottom reference resistors and select the closest resistor values using 0.1% resistor values. Table 9-3 shows the reference (or calculated) top and bottom resistors. Table 9-4 shows the selected resistors for the application.

Table 9-3. SENSEx Reference Nominal Resistors

Channel #	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)
1	4.13	0.94
2		0.86
3	0.75	0.39
4		0.36

An calculation example for channel 1 (or SENSE1) top and bottom resistor is shown below:

$$\frac{3.23\ \text{V} -\ 3.14\ \text{V}}{24\ \mu\text{A}} = 4.13\text{k}\Omega \tag{31}$$

$$\frac{4.13\ \text{k}\Omega \times 0.60\ \text{V}}{3.23\ \text{V}\ -\ 0.60\ \text{V}} = 0.94\text{k}\Omega \tag{32}$$

Table 9-4. SENSEx Selected Resistors Using 0.1 % Tolerance Resistors

Channel #	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)
1	4.12	0.931
2		0.866
3	0.75	0.383
4		0.357

Now that the actual resistors are known, we can calculate the actual on and off nominal voltages and the error voltages by using Equation 9, Equation 10, Equation 11, Equation 14, Equation 15, and Equation 20. Using the errors, we can calculate the upper and lower voltages and normalize the values with respect to the nominal output voltage.

Table 9-5. V_{OUTx_RISE} Nominal Values With Statistics in Volts and Percentage

Channel #	$V_{OUTx\_RISE\_NOMINAL}$ (V)	$V_{OUTx\_RISE\_NOMINAL}$(1) (%)
1	3.25	98.48
2	3.45	104.51
3	1.77	98.44
4	1.86	103.19

(1) Values are normalized to the nominal output voltage for that rail.

Table 9-6. V_{OUTx_FALL} Nominal Values with Statistics in Volts and Percentage

Channel #	$V_{OUTx\_FALL\_NOMINAL}$ (V)	$V_{OUTx\_FALL\_NOMINAL}$ (%)(1)
1	3.15	95.48
2	3.35	104.51
3	1.75	98.88
4	1.84	103.19

(1) Values are normalized to the nominal output voltage for that rail.

9.2.1.3 Application Curves

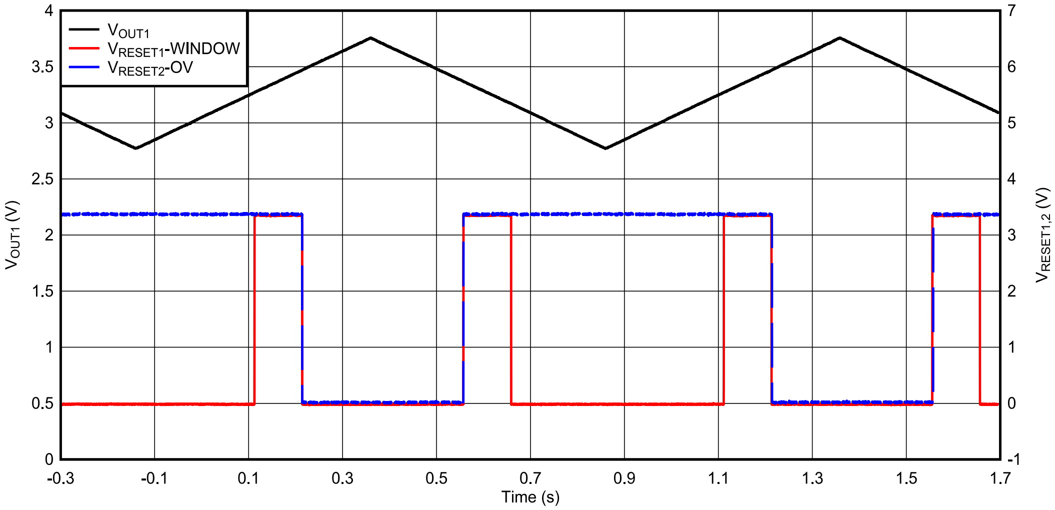


Figure 9-2. V_{OUT1}, $V_{\overline{RESET1}}$ and $V_{\overline{RESET2}}$ vs Time

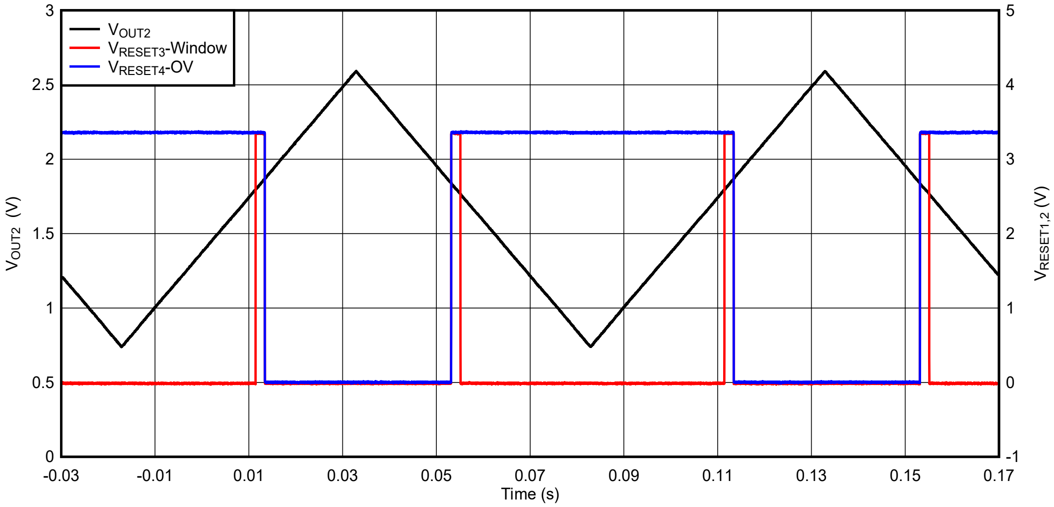


Figure 9-3. V_{OUT2}, $V_{\overline{RESET3}}$ and $V_{\overline{RESET4}}$ vs Time

9.3 Power Supply Recommendations

The TPS7H3024 is designed to operate from an input supply (V_{IN}) with a voltage range between 3V to 14V. V_{IN} needs to be de-couple with at least one 1µF ceramic capacitor from V_{IN} to GND, as close to the pin as possible

In the TPS7H3024 the PULL_UP1 and PULL_UP2 are also considered power inputs, in this case for the push-pull outputs. The voltage range on these inputs is from 1.6V to 7V. Connect at least one 1µF ceramic capacitor from PULL_UP1 to GND and from PULL_UP2 to GND. These capacitors must be placed as close to the pins as possible.

ADVANCE INFORMATION

9.4 Layout

9.4.1 Layout Guidelines

- Connect a high quality ceramic capacitor (such as X7R) as close to the pins as possible. The signals and capacitor values are:
  - V_{IN}≥ 1µF.
  - REFCAP = 470nF.
  - VLDO = 1µF.
  - PULL_UPx ≥ 1µF
- Avoid passing noisy traces near the VLDO and REFCAP pins as this are internal references to the device.
- If needed, place a small capacitor between the SENSEx pins and GND to reduce the sensitivity to transient voltages on the monitored signal.
- It is typical to use the supervisor in conjunction with switch mode power supplies, it is critical to keep the SENSEx trace away from noisy sources as much as possible. Avoid routing this trace directly under the noise-source if possible. If not possible, ensure that the trace is routed on another layer with a ground layer separating the trace and noise-source.

9.4.2 Layout Example

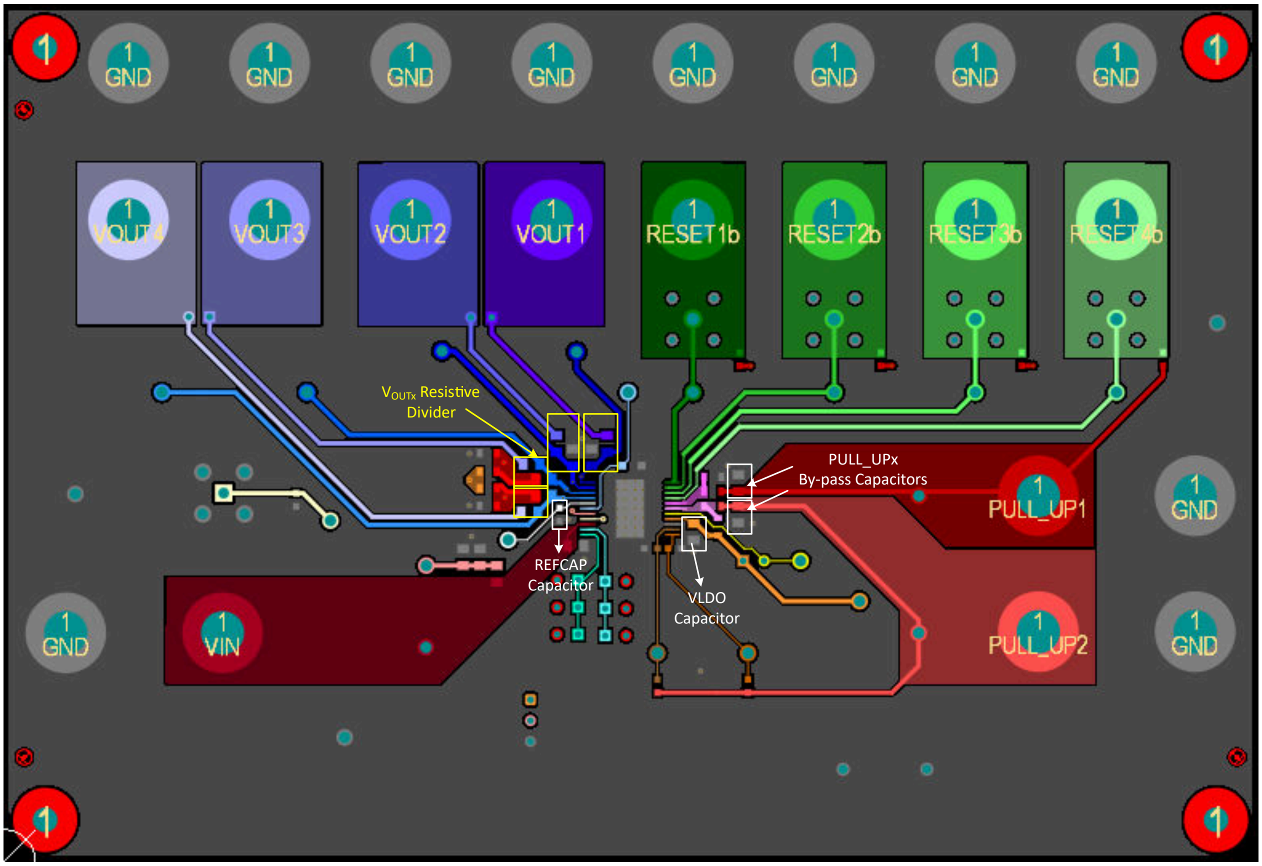


Figure 9-4. Printed Circuit Board Layout Example: Top Layer

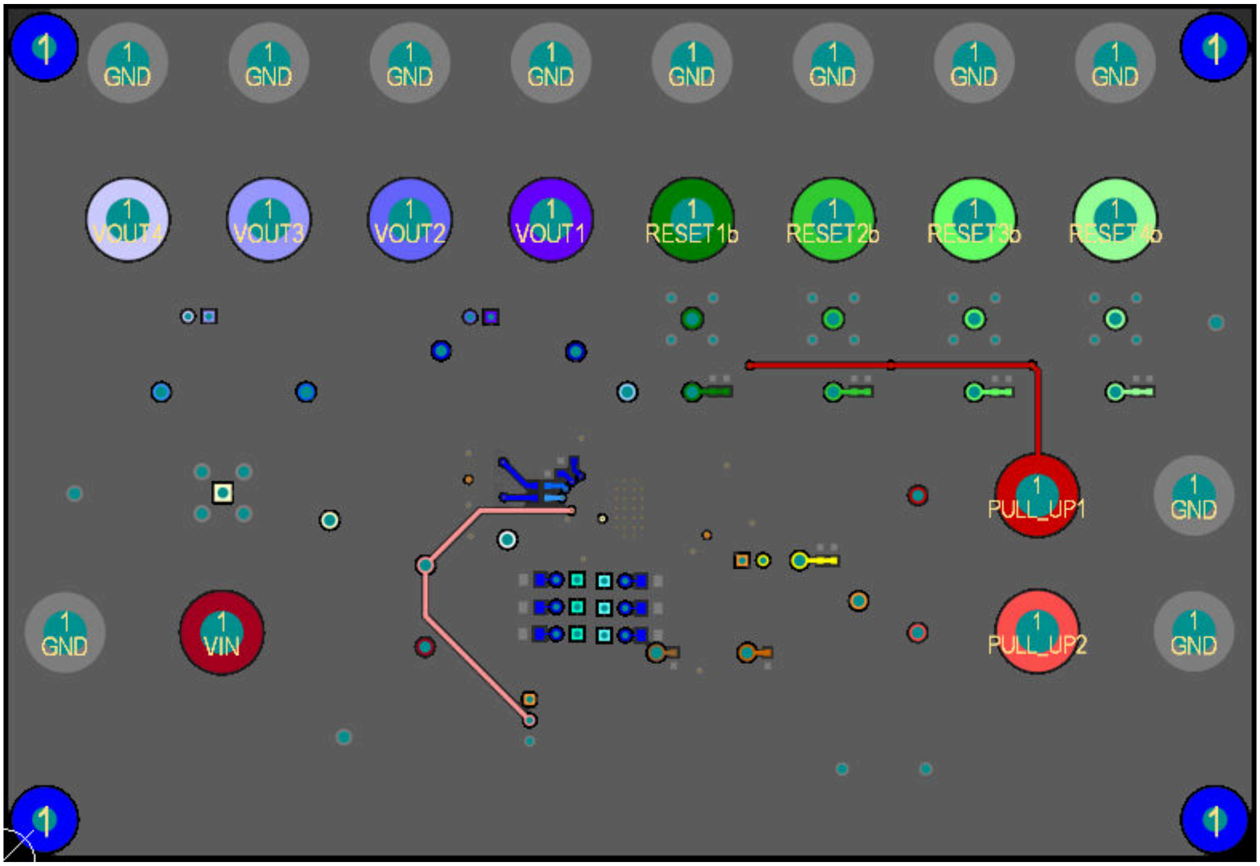


Figure 9-5. Printed Circuit Board Layout Example: Bottom Layer

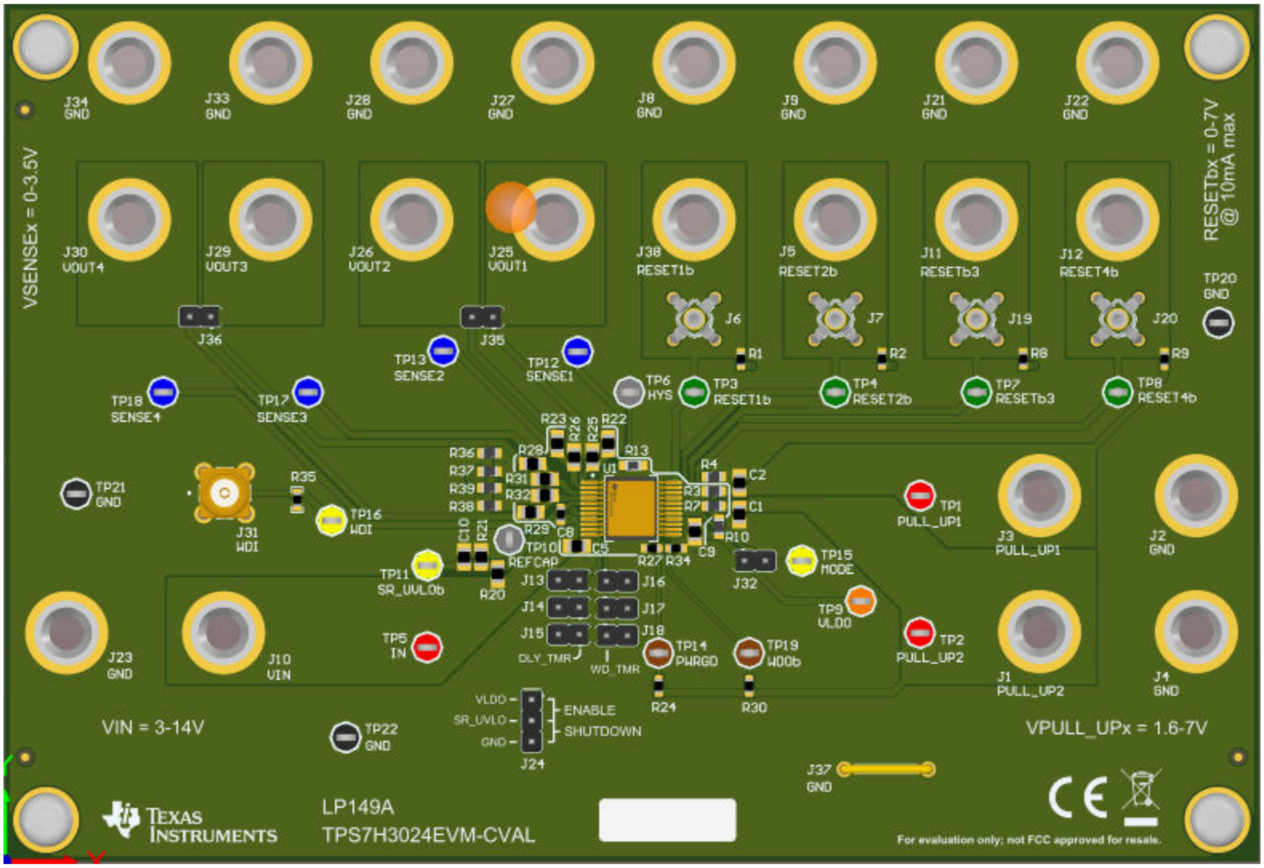


Figure 9-6. Printed Circuit Board Layout Example: Top Layer 3D View

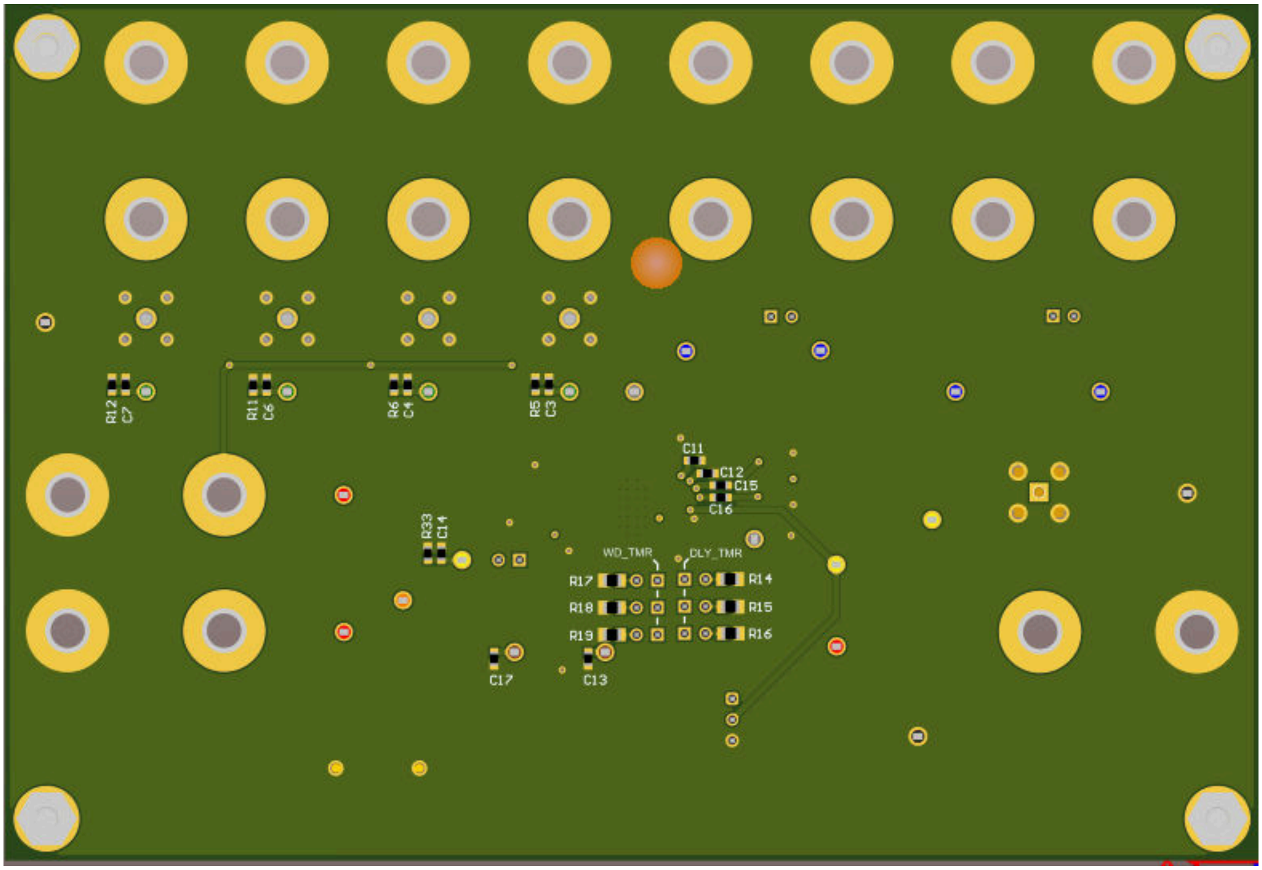


Figure 9-7. Printed Circuit Board Layout Example: Bottom Layer 3D View

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The following related documents are available for download at www.ti.com:

- *Optimizing Resistor Dividers at a Comparator Input*, SLVA450
- *TPS7H3024EVM-CVAL EVM User Guide*, SLVUD02

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

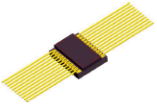
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

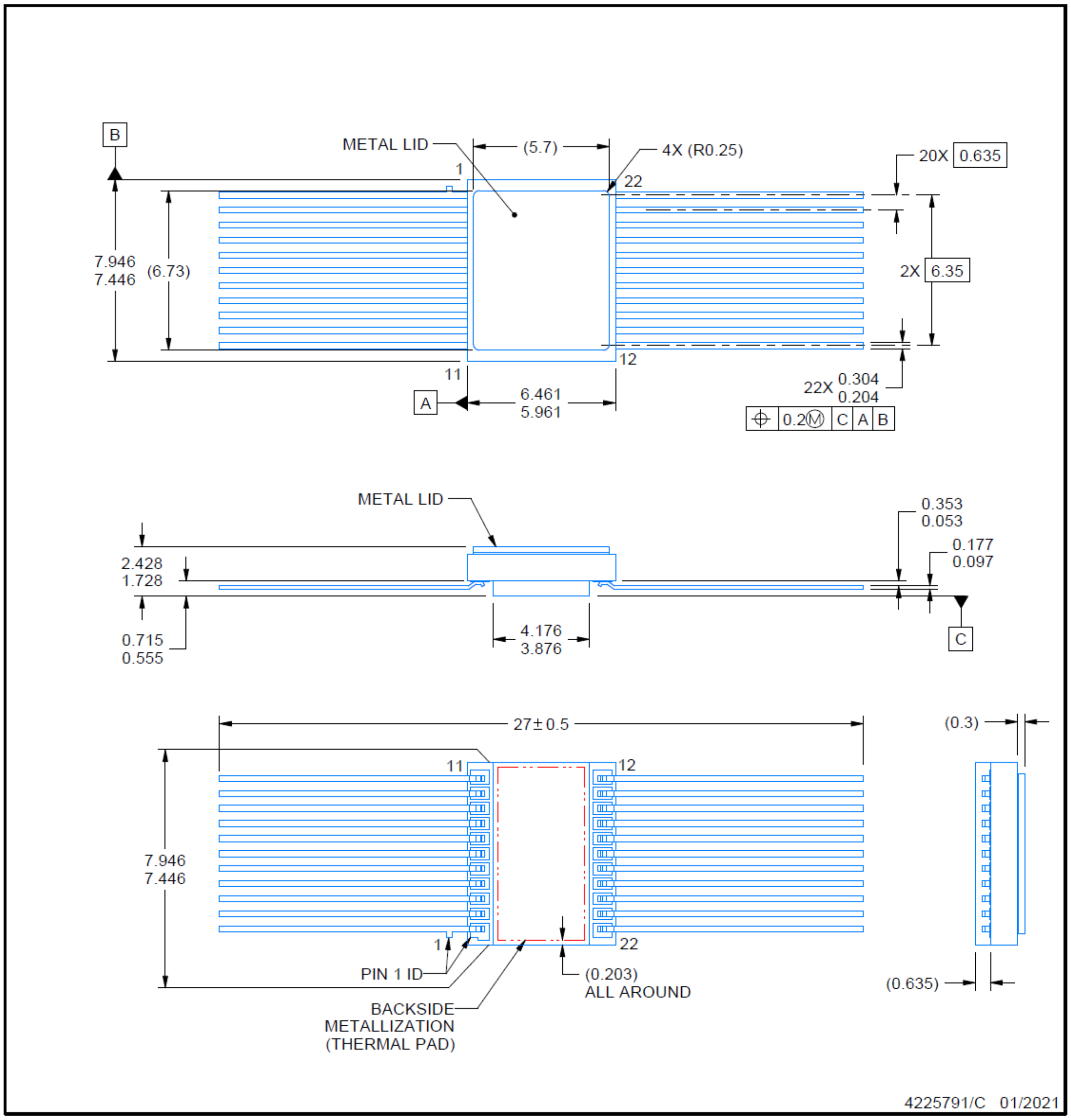
HFT0022A



PACKAGE OUTLINE

CFP - 2.428mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metalization

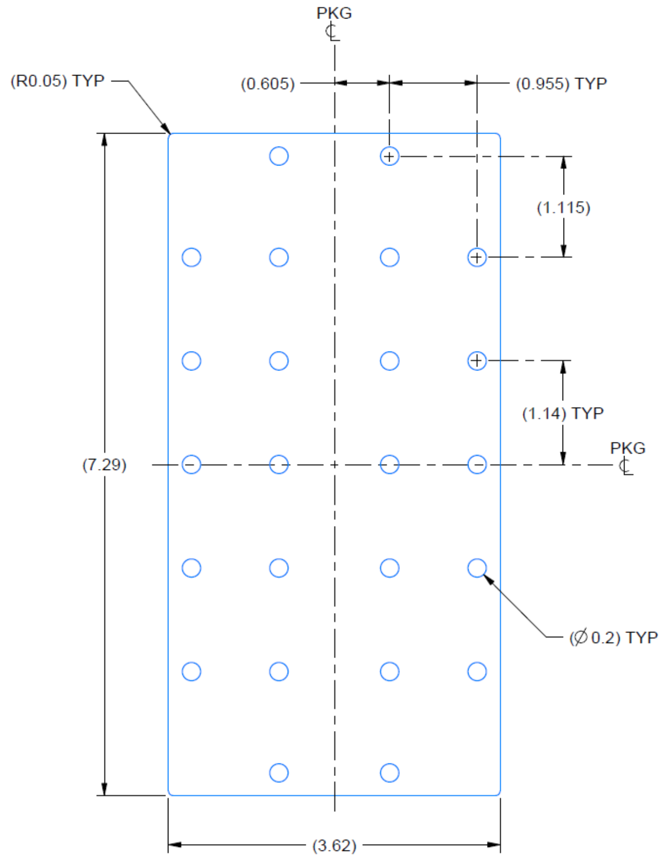
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

HFT0022A **CFP - 2.428mm max height**

CERAMIC FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7H3024HFT/EM	Active	Preproduction	CFP (HFT) | 22	15 | TUBE	-	Call TI	Call TI	25 to 25	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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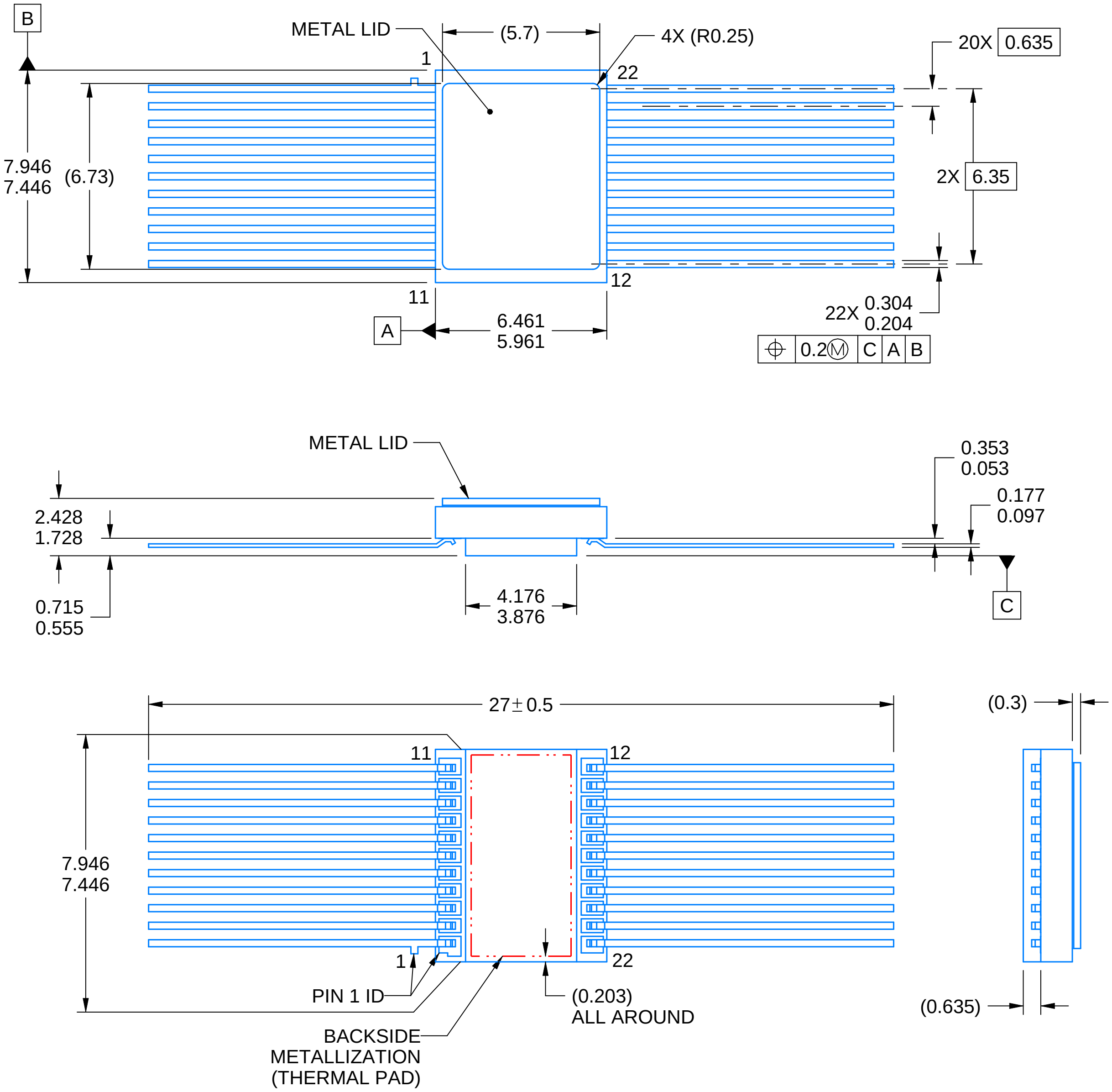
PACKAGE OUTLINE

HFT0022A

CFP - 2.428mm max height

CERAMIC FLATPACK



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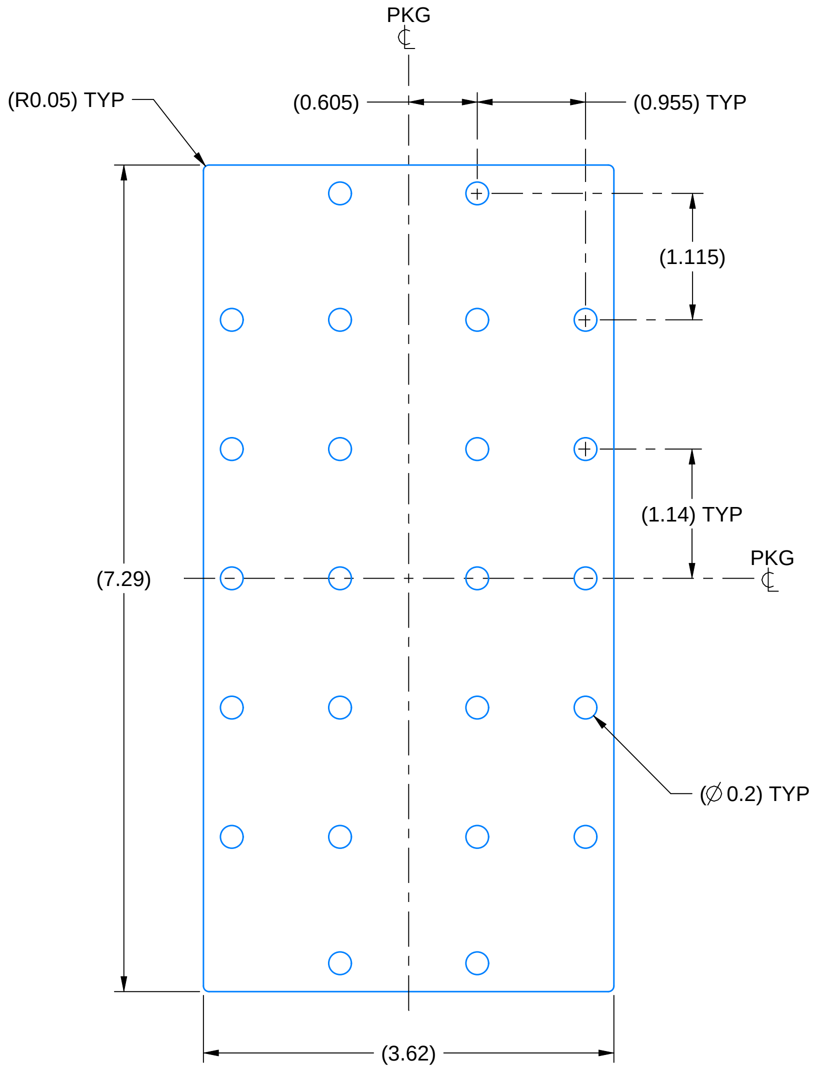

HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2186323	03/13/2020	R. RAZAK / ANIS FAUZI
B	ADD LAND PATTERN VIEW / SHEET	2190485	10/22/2020	R. RAZAK / ANIS FAUZI
C	UPDATE TOTAL LEAD LENGTH TO 27± 0.5	2192775	01/28/2021	R. RAZAK / ANIS FAUZI

SCALE	SIZE		REV	PAGE
	A	4225791	C	4 OF 4

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