TPS7B7802-Q1 Automotive, 500mA, Dual-Channel, Antenna LDO With I²C Diagnostics

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification 2
  - Device CDM ESD classification C4B
- Single and dual-channel LDO with current sense and adjustable current-limit
- 4.5V to 40V wide input voltage range, 45V load dump
- Power switch mode when tying FB to GND
- 1.5V to 20V adjustable output voltage
- Up to 300mA output current per channel
- Adjustable current-limit with external resistor
- High accuracy current-sense to detect antenna open condition at low current without further calibration
- High power-supply rejection ratio: typical 73dB at 100Hz
- Integrated reverse-polarity protection, down to –40V and no need for external diode
- 500mV maximum dropout voltage at 100mA load
- Stable with output capacitor in 2.2µF to 100µF range (ESR 1mΩ to 5Ω)
- Integrated protection and diagnostics:
  - Thermal shutdown
  - Undervoltage lockout (UVLO)
  - Short-circuit protection
  - Reverse battery polarity protection
  - Reverse-current protection
  - Output short-to-battery protection
  - Output inductive load clamp
  - Multiplexing current sense between channels and devices
  - Ability to distinguish all faults with current sense
- 16-pin HTSSOP PowerPAD™ package

2 Applications

- Infotainment active-antenna power supplies
- Surround-view camera power supplies
- High-side power switch for small-current applications

3 Description

The TPS7B770x-Q1 family of devices feature a single and dual, high-voltage low-dropout regulator (LDO) with current sensing, designed to operate with a wide input-voltage range from 4.5V to 40V (45V load dump protection). These devices provide power to the low-noise amplifiers of the active antenna through a coax cable with 300mA per channel current. Each channel also provides an adjustable output voltage from 1.5V to 20V.

These devices provide diagnostics through the current sense and error pins. To monitor the load current, a high-side current-sense circuitry provides a proportional analog output to the sensed load current. The accurate current sense allows detection of open, normal, and short-circuit conditions without the need for further calibration. Multiplex the current sense between channels and devices to save analog-to-digital converter (ADC) resources. Each channel also implements adjustable current limit with an external resistor.

An integrated reverse polarity diode eliminates the need for an external diode. These devices feature standard thermal shutdown, short-to-battery protection on the output, and reverse current protection. Each channel has internal inductive clamp protection on the output during inductive switch off.

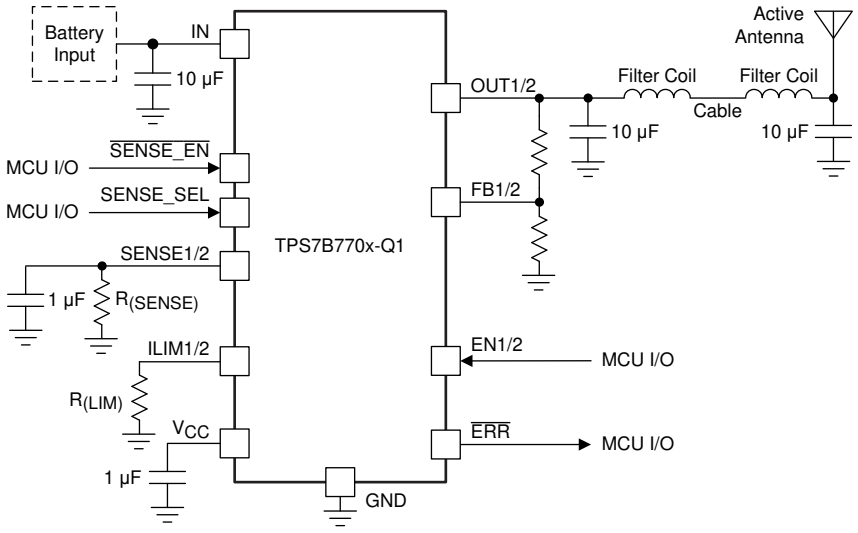
These devices operate over a –40°C to +125°C ambient temperature range.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	CHANNEL
TPS7B7701-Q1	PWP (HTSSOP, 16)	5mm × 6.4mm	Single
TPS7B7702-Q1			Dual

(1) For all available packages, see the package option addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

ADVANCE INFORMATION



Application Diagram

ADVANCE INFORMATION

Table of Contents

ADVANCE INFORMATION

ADVANCE INFORMATION

4 Pin Configuration and Functions

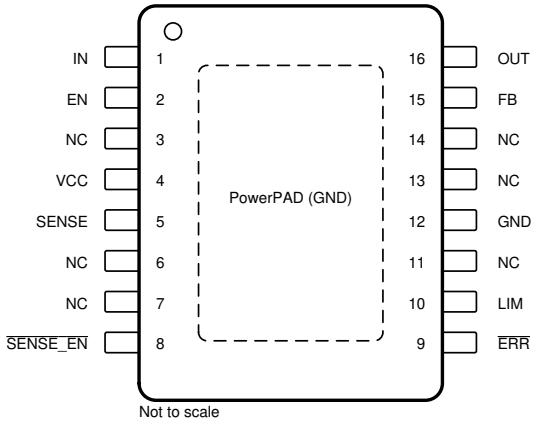


Figure 4-1. Single-Channel TPS7B7701-Q1 PWP Package, 16-Pin HTSSOP With PowerPAD (Top View)

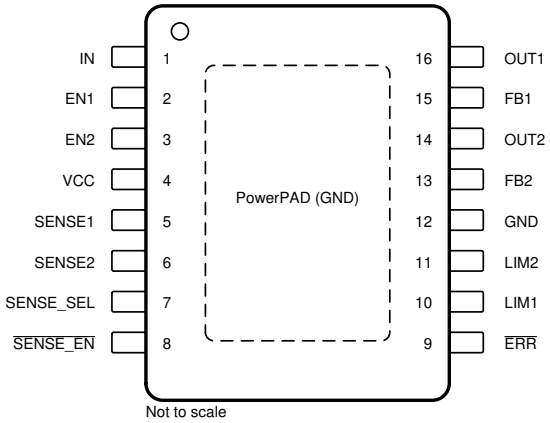


Figure 4-2. Dual-Channel TPS7B7702-Q1 PWP Package, 16-Pin HTSSOP With PowerPAD (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SINGLE-CHANNEL	DUAL-CHANNEL		
EN	2	—	Input	Active-high enable input for the OUT pin with internal pulldown.
EN1	—	2	Input	Active-high enable input for the OUT1 pin with internal pulldown.
EN2	—	3	Input	Active-high enable input for the OUT2 pin with internal pulldown.
$\overline{\text{ERR}}$	9	9	Output	This pin is an open-drain fault indicator for general faults.
FB	15	—	Input	Feedback input for setting OUT voltage. Connect FB to GND for current-limited switch operation.
FB1	—	15	Input	Feedback input for setting OUT1 voltage. Connect FB1 to GND for current-limited switch operation.
FB2	—	13	Input	Feedback input for setting OUT2 voltage. Connect FB2 to GND for current-limited switch operation.
GND	12	12	Ground	Ground reference
IN	1	1	Power	Input power-supply voltage
LIM	10	—	Output	Programmable current-limit pin. Connect a resistor to GND to set the current limitation level. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND.
LIM1	—	10	Output	Programmable current-limit pin for channel 1. Connect a resistor to GND to set the current limitation level for channel 1. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND.
LIM2	—	11	Output	Programmable current-limit pin for channel 2. Connect a resistor to GND to set the current limitation level for channel 2. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND.
NC	3, 13, 14	—	—	Not connected. Connect the NC pins to ground or leave floating.
	6, 7, 11	—	—	Internally connected. These pins must either be floated or connected to GND.
OUT	16	—	Power	Output voltage
OUT1	—	16	Power	Output voltage 1
OUT2	—	14	Power	Output voltage 2
SENSE	5	—	Output	Output of current sense for sensing. To set the SENSE output voltage level, connect a resistor between this pin and GND. In addition, connect a 1-µF capacitor from this pin to GND for frequency compensation of the current-sense loop. Short this pin to GND if not used.

Table 4-1. Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	SINGLE-CHANNEL	DUAL-CHANNEL		
SENSE1	—	5	Output	Output of current sense for sensing. SENSE1 current is proportional to the current flow through OUT1 and SENSE 2 current is proportional to OUT2 current when SENSE_SEL and $\overline{\text{SENSE\_EN}}$ are low. To set the SENSEx output voltage level, connect a resistor between this pin and GND. In addition, connect a 1-µF capacitor from the SENSEx pin to GND for frequency compensation of the current-sense loop. Short the SENSEx pin to GND if not used.
SENSE2	—	6	Output	
$\overline{\text{SENSE\_EN}}$	8	8	Input	This pin is the enable and disable of the current-sense pin for multiplexing, active-low enable.
SENSE_SEL	—	7	Input	This pin selects the current sense between channel 1 and channel 2. See Table 6-2 for details.
V_{CC}	4	4	Output	Internal 4.5V regulator. Connect 1µF ceramic capacitor between V_{CC} and GND for frequency compensation.

ADVANCE INFORMATION

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	Unregulated input, IN	–40	45	V
	EN, EN1, and EN2	–0.3	45	V
Regulated output(2)	V_{CC} (3) (4)	–0.3	6	V
	OUT1 and OUT2	–0.3	45	V
Low-voltage pins	SENSE, SENSE1, and SENSE2(3) (4)	–0.3	V_{CC} + 0.3	V
	LIM, LIM1, LIM2, $\overline{\text{SENSE\_EN}}$, SENSE_SEL, $\overline{\text{ERR}}$, FB, FB1, and FB2(3) (4)	–0.3	7	V
Operating junction temperature, T_J		–40	150	°C
Operating ambient temperature, T_A		–40	125	°C
Storage Temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) There is an internal diode connects between the OUT and GND pins with 300mA DC current capability for inductive clamp protection.
(3) All voltage values are with respect to GND.
(4) Absolute maximum voltage.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Unregulated input		4.5	40	V
	EN, EN1, and EN2		0	40	V
	Low-voltage pins	SENSE, SENSE1, SENSE2, $\overline{\text{SENSE\_EN}}$, SEN_SEL, $\overline{\text{ERR}}$, FB, FB1, FB2, LIM, LIM1, LIM2, and V_{CC}	0	5.3	V
	OUT1, OUT2, and OUT	Normal-mode operation	1.5	20	V
		Switched-mode operation	1.5	35	
C_O	Output capacitor stability range		2.2	100	µF
$C_{O(ESR)}$	Output capacitor ESR stability range		0.001	5	Ω
T_J	Junction temperature		–40	150	°C
T_A	Ambient temperature		–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS7B7701-Q1 PWP (HTSSOP) 16 PINS	TPS7B7702-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	45.9	40.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.2	27.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.7	22.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.5	22	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The thermal data is based on JEDEC standard high K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also incorporate correct attachment procedure.

5.5 Electrical Characteristics

at V_I = 14V and T_J = –40°C to +150°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
V_I	Input voltage		4.5		40	V
I_Q	Quiescent current	TPS7B7701-Q1: V_I = 4.5 to 40V, $V_{(EN)} \geq$ 2V, $I_{(OUT)}$ = 0.1mA		0.6	1	mA
		TPS7B7702-Q1: V_I = 4.5 to 40V, $V_{(EN1)}$ and $V_{(EN2)} \geq$ 2V, $I_{(OUT1)}$ and $I_{(OUT2)}$ = 0.1mA		0.6	1	
$I_{(shutdown)}$	Shutdown current	TPS7B7701-Q1: EN = GND			5	µA
		TPS7B7702-Q1: EN1 = EN2 = GND			5	
I_{nom}	Operating current	TPS7B7701-Q1: $V_{(EN)} \geq$ 2V, $I_{(OUT)} \leq$ 300mA, GND current			4.5	mA
		TPS7B7702-Q1: $V_{(EN1)}$ and $V_{(EN2)} \geq$ 2V, $I_{(OUT1)}$ and $I_{(OUT2)} \leq$ 300mA, GND current			6	
$V_{(BG)}$	Bandgap	Reference voltage for FB	–2%	1.233	2%	V
$V_{(UVLO)}$	Undervoltage lockout falling	Ramp IN down until the output turns off			4	V
V_{hys}	Hysteresis			0.4		V
INPUT CONTROL PINS (EN, EN1, EN2, $\overline{\text{SENSE\_EN}}$, AND SENSE_SEL)						
V_{IL}	Logic input low level	For EN, EN1, EN2, $\overline{\text{SENSE\_EN}}$, and SENSE_SEL	0		0.7	V
V_{IH}	Logic input high level	For EN, EN1, EN2, $\overline{\text{SENSE\_EN}}$, and SENSE_SEL	2			V
$I_{I(SENSE\_EN)}$	$\overline{\text{SENSE\_EN}}$ input current	$V_{(SENSE\_EN)}$ = 5V, $V_{(ENx)} \geq$ 2V			10	µA
$I_{I(SENSE\_SEL)}$	SENSE_SEL input current	$V_{(SENSE\_EN)}$ = 5V, $V_{(ENx)} \geq$ 2V			10	µA
$I_{I(EN)}$	Enable input current	$V_{(ENx)} \leq$ 40V			10	µA
REGULATED OUTPUT (OUT, OUT1, AND OUT2)						
V_O	Regulated output	40V ≥ $V_I \geq V_O$ + 1.5V and $V_I \geq$ 4.5V, I_O = 1 to 300mA[1]	–2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_I = V_O$ + 1.5V to 40V and $V_I \geq$ 6V, I_O = 10mA, voltage variation on FB pin			10	mV
$\Delta V_{O(\Delta IO)}$	Load regulation	I_O = 1mA to 200mA, voltage variation on FB pin			20	mV

ADVANCE INFORMATION

5.5 Electrical Characteristics (continued)

at V_I = 14V and T_J = –40°C to +150°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DROPOUT)}$	Dropout voltage	Measured between IN and OUTx, I_O = 100mA			500	mV
I_O	Output current	V_O in regulation	0		300	mA
PSRR	Power supply ripple rejection(2)	I_O = 100mA, C_O = 2.2 µF, f = 100Hz		73		dB
CURRENT SENSE AND CURRENT-LIMIT						
I_O/I_{SENSE}	OUTx to SENSEx current ratio (I_O / I_{SENSEx})	V_I = 4.5V to 40V, 5mA ≤ I_O ≤ 300mA		198		
	OUTx to SENSEx current ratio accuracy	I_O = 100 to 300mA	–3%		3%	
		I_O = 50 to 100mA	–5%		5%	
		I_O = 10 to 50mA	–10%		10%	
		I_O = 5 to 10mA	–20%		20%	
I_O/I_{LIM}	OUTx to LIMx current ratio (I_O / I_{LIM})	V_I = 4.5V to 40V, 50mA ≤ $I_{(LIMx)}$ ≤ 300mA		198		
$I_{(LIMx)}$	Programmable current-limit accuracy(3)	V_I = 4.5V to 40V, 50mA ≤ $I_{(LIMx)}$ ≤ 300mA	–8%		8%	
$I_{L(LIMx)}$	Internal current-limit	LIMx shorted to GND	340		550	mA
I_{lkg}	SENSE, SENSE1, SENSE2, LIM, LIM1, and LIM2 leakage current	ENx = GND, T_A = 25°C			2	µA
$V_{(LIMx\_th)}$	Current-limit threshold voltage	Voltage on the LIM, LIM1, and LIM2 pins when output current is limited		1.233		V
$V_{(SENSEx\_stb)}$	Current-sense short-to-battery fault voltage	When short-to-battery or reverse current conditions are detected	3.05	3.2	3.3	V
$V_{(SENSEx\_tsd)}$	Current-sense thermal shutdown fault voltage	When thermal shutdown is detected	2.7	2.85	3	V
$V_{(SENSEx\_cl)}$	Current-sense current-limit fault voltage	When current-limit conditions are detected	2.4	2.55	2.65	V
$I_{(SENSEx\_H)}$	Current-sense fault condition current	When short-to-battery, reverse current, thermal shutdown, or current-limit conditions are detected	3.3			mA
FAULT DETECTION						
$V_{(stb\_th)}$	Short-to-battery threshold	$V_{(OUTx)}$ – V_I, checked during turnon sequence	–500	–55	110	mV
$I_{(REV)}$	Reverse current detection level	Power FET on (SW or LDO mode)	–100	–40	–1	mA
T_{SD}	Thermal shutdown	Junction temperature		175		°C
$T_{SD(hys)}$	Thermal shutdown hysteresis			15		°C
INTERFACE CIRCUITRY						
V_{OL}	$\overline{ERR}$ output low	$I_{(SINK)}$ = 5mA			0.4	V
I_{lkg}	$\overline{ERR}$ open-drain leakage current	$\overline{ERR}$ high impedance, 5V external voltage is applied at $\overline{ERR}$			1	µA
$R_{(OUTx-off)}$	OUT pulldown resistor(2)	ENx = GND		50		kΩ
$I_{R(lkg)}$	Reverse leakage current	–40V < V_I < 0V, reverse current to IN		0.6		mA
V_{CC}	Internal voltage regulator	V_I = 5.5 to 40V, I_{CC} = 0mA	4.25	4.5	4.75	V
$I_{CC(lim)}$	Internal voltage-regulator current-limit		15		70	mA

(1) External feedback resistor is not considered.
(2) Design information; specified by design, not production tested.
(3) The current-limit accuracy is maintained when the current limit is set from 50mA to 300mA, and it includes the deviation of the current-limit threshold voltage $V_{(LIMx\_th)}$.

ADVANCE INFORMATION

5.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE AND CURRENT-LIMIT						
$t_{d(SENSE\_SEL\_r)}$	Current-sense delay time from the rising edge of SENSE_SEL(1)	$V_{(ENx)}$ ≥ 2V, $\overline{SENSE\_EN}$ = GND, SENSE_SEL rise from 0 to 5V		10		µs
$t_{d(SENSE\_SEL\_f)}$	Current-sense delay time from the falling edge of SENSE_SEL(1)	$V_{(ENx)}$ ≥ 2V, $\overline{SENSE\_EN}$ = GND, SENSE_SEL fall from 5 to 0V		10		µs
$t_{d(SENSE\_EN\_r)}$	Current-sense delay time from rising edge of $\overline{SENSE\_EN}$ (1)	$V_{(ENx)}$ ≥ 2V, $\overline{SENSE\_EN}$ rise from 0 to 5V		10		µs
$t_{d(SENSE\_EN\_f)}$	Current-sense delay time from falling edge of $\overline{SENSE\_EN}$ (1)	$V_{(ENx)}$ ≥ 2V, $\overline{SENSE\_EN}$ fall from 5 to 0V		10		µs
FAULT DETECTION						
$t_{(PD\_RC)}$	Reverse current (Short-to-BAT) shutdown deglitch time	Delay to shut down the switch or LDO after a drop over r_{on} becomes negative, $I_{(OUTx)}$ = –200mA (typical), T_A = 25°C		5	20	µs
$t_{(BLK\_RC)}$	Reverse current blanking time	Blanking time for reverse-current detection after power up, the rising edge of the ENx pin, or the current limiting event is over		16		ms

(1) Design information; specified by design; not production tested.

ADVANCE INFORMATION

5.7 Typical Characteristics

at V_I = 14V (unless otherwise specified)

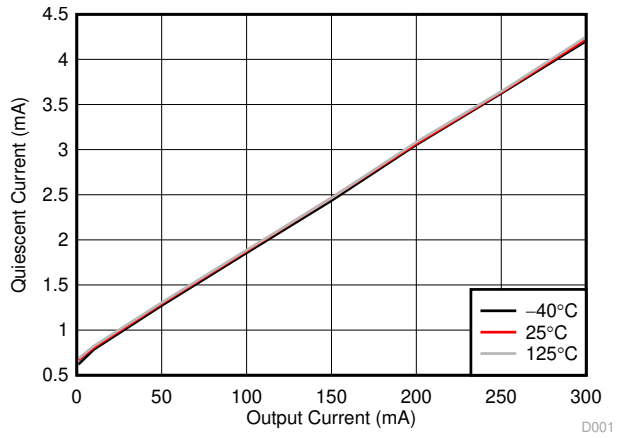


Figure 5-1. Quiescent Current vs Output Current (TPS7B7702-Q1)

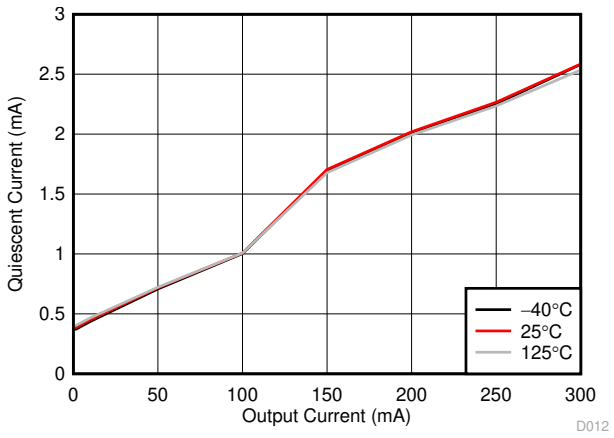


Figure 5-2. Quiescent Current vs Output Current (TPS7B7701-Q1)

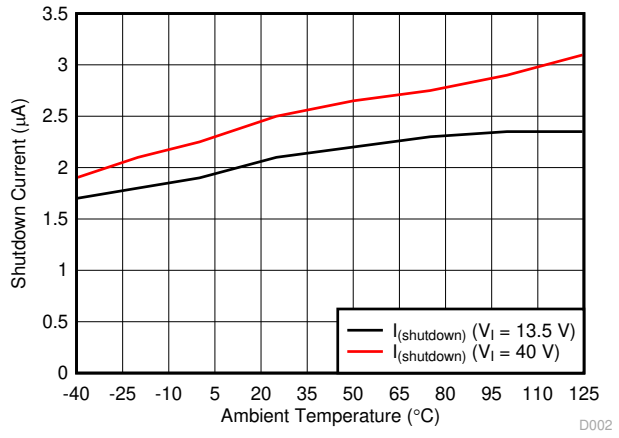
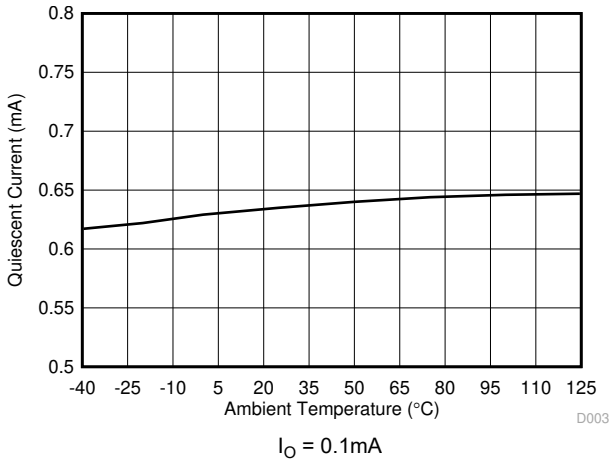


Figure 5-3. Shutdown Current vs Ambient Temperature (TPS7B7702-Q1)

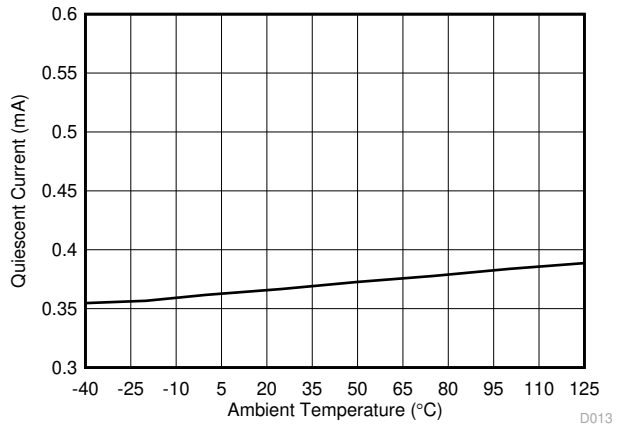


I_O = 0.1mA

Figure 5-4. Quiescent Current vs Ambient Temperature (TPS7B7702-Q1)

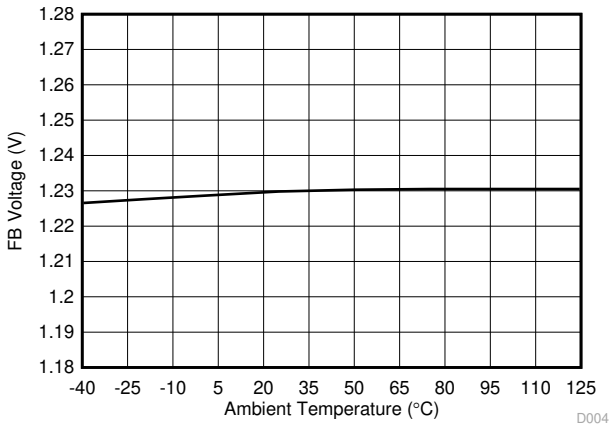
5.7 Typical Characteristics (continued)

at V_I = 14V (unless otherwise specified)



I_O = 0.1mA

Figure 5-5. Quiescent Current vs Ambient Temperature (TPS7B7701-Q1)



I_O = 10mA

Figure 5-6. FB Voltage vs Ambient Temperature

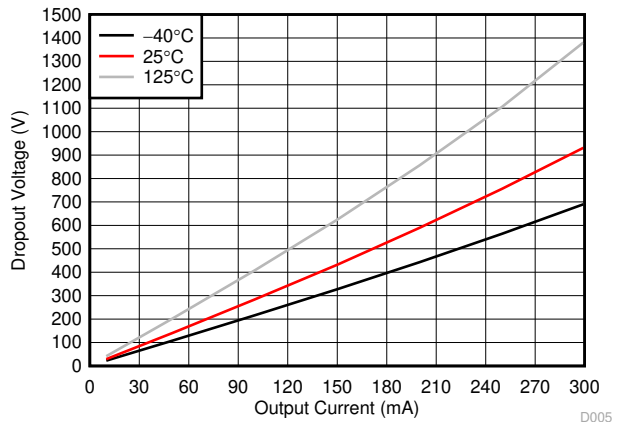
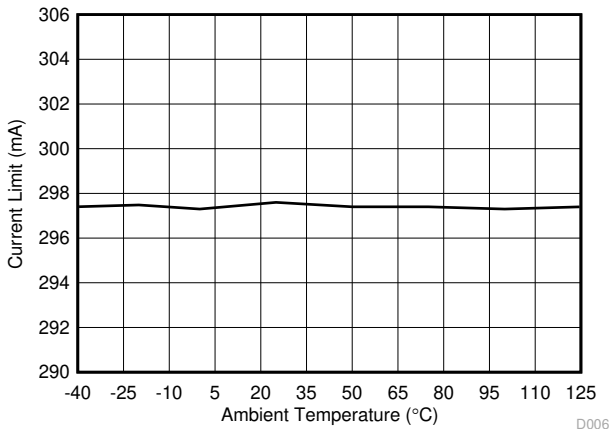
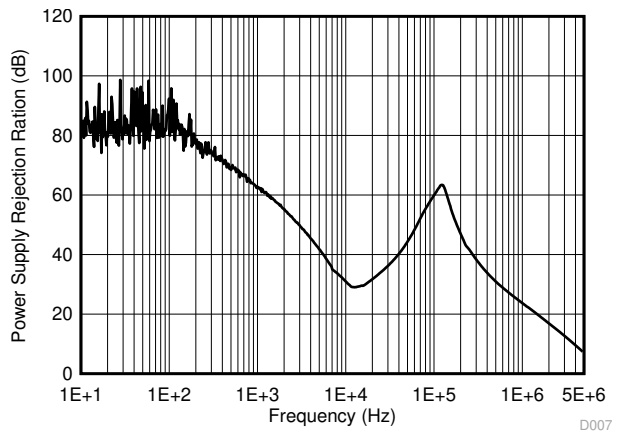


Figure 5-7. Dropout Voltage vs Output Current



I_{LIM} = 300mA

Figure 5-8. Current Limit vs Ambient Temperature



C_O = 10µF, I_O = 10mA

Figure 5-9. PSRR TPS7B770x-Q1

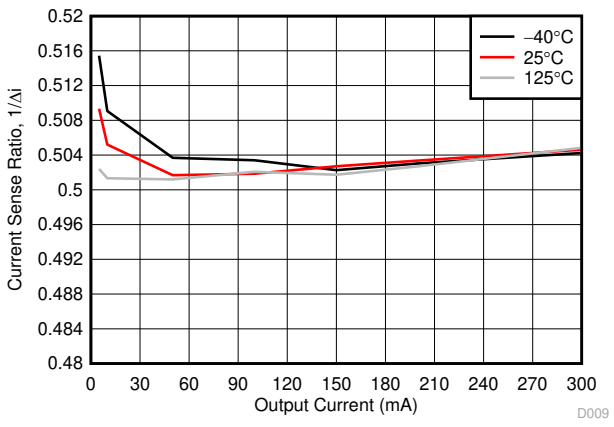


Figure 5-10. Current Sense Ratio vs Output Current, TPS7B7702-Q1 Channel 1

ADVANCE INFORMATION

ADVANCE INFORMATION

5.7 Typical Characteristics (continued)

at V_I = 14V (unless otherwise specified)

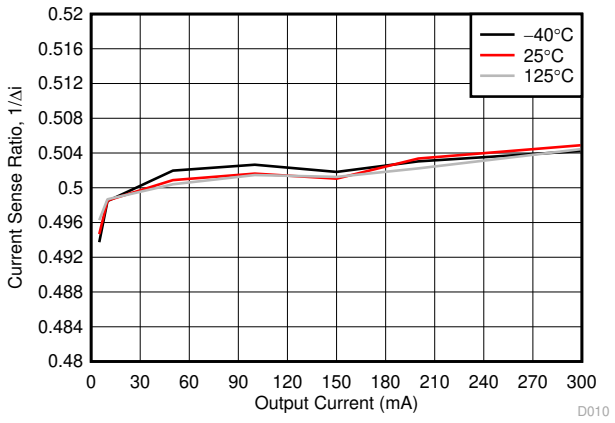
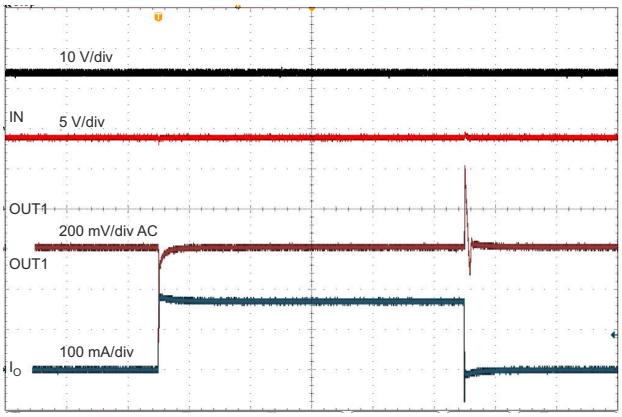
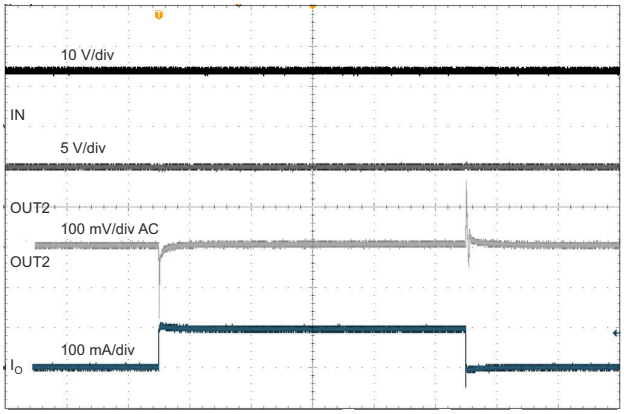


Figure 5-11. Current Sense Ratio vs Output Current, TPS7B7702-Q1 Channel 2



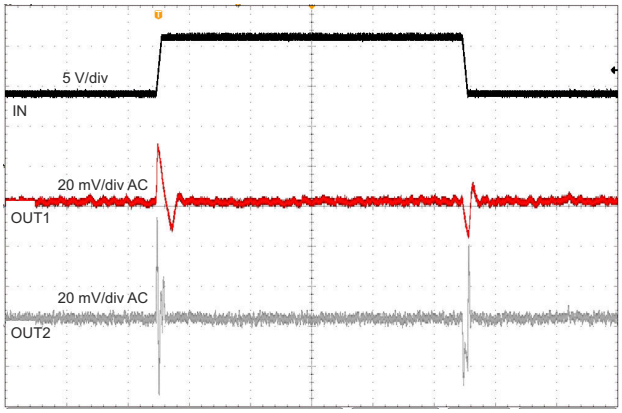
V_O = 8.5V, C_O = 10µF, I_O = 1mA to 170mA

Figure 5-12. 1mA to 170mA Load Transient



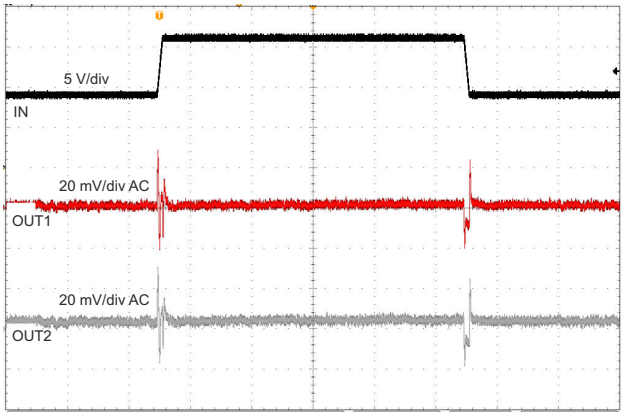
V_O = 5V, C_O = 10µF, I_O = 1mA to 100mA

Figure 5-13. 1mA to 100mA Load Transient



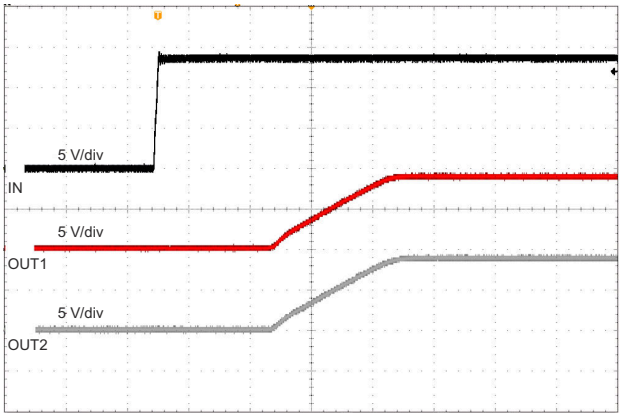
V_O = 8.5V, I_O = 50mA

Figure 5-14. 9V to 16V Line Transient (1V/µs)



V_O = 5V, I_O = 50mA

Figure 5-15. 9V to 16V Line Transient (1V/µs)

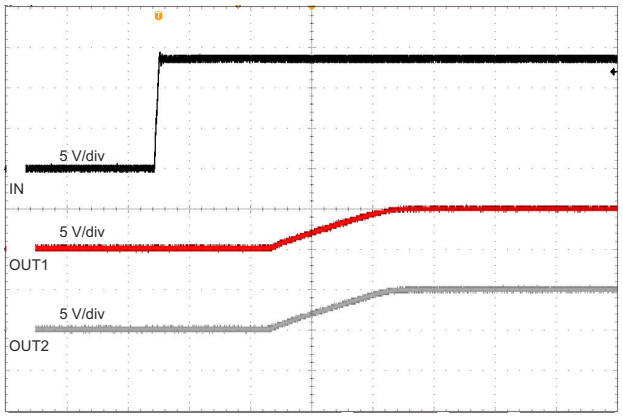


V_O = 8.5V, I_O = 100mA, V_I = 0V to 14V

Figure 5-16. Power Up (1V/µs)

5.7 Typical Characteristics (continued)

at V_I = 14V (unless otherwise specified)



V_O = 5V, I_O = 100mA, V_I = 0V to 14V

Figure 5-17. Power Up (1V/µs)

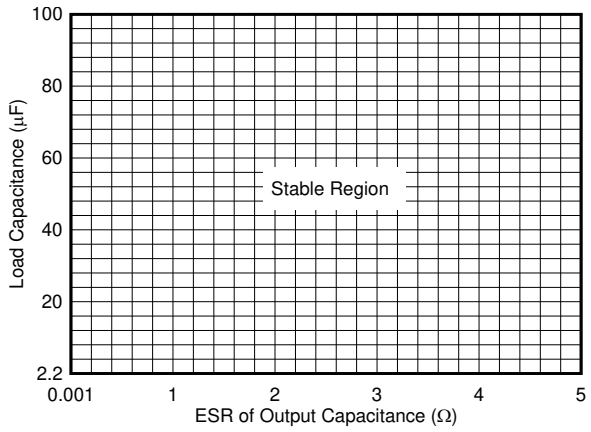


Figure 5-18. Load Capacitance vs ESR of Output Capacitance

ADVANCE INFORMATION

ADVANCE INFORMATION

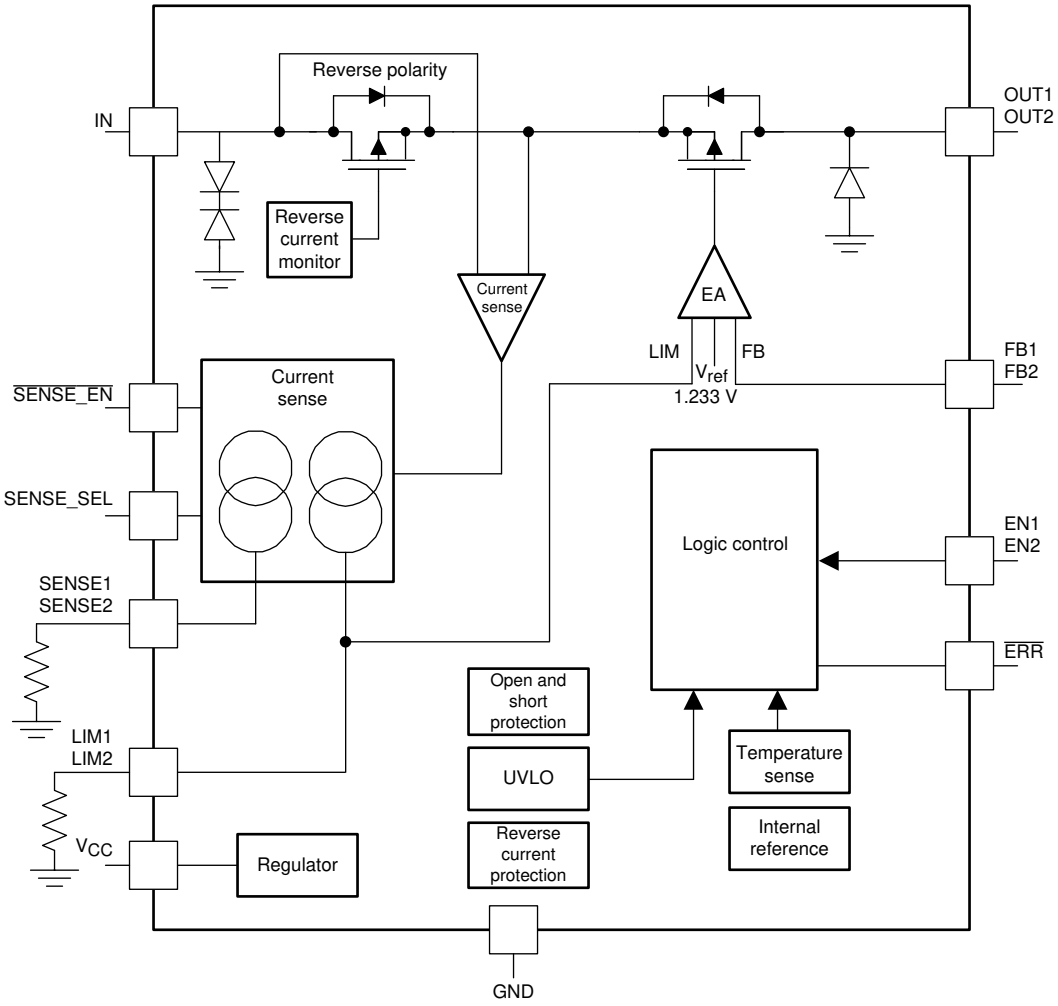
6 Detailed Description

6.1 Overview

The TPS7B770x-Q1 family of devices feature a single- or dual-channel, high voltage LDO with a current-sense function. These devices operate with a wide input-voltage range from 4.5V to 40V (45V load dump protection). These devices also offers protection of antenna lines against electrostatic discharge (ESD) and from short-to-ground, short-to-battery, and thermal overstress. Device output voltage is adjustable from 1.5V to 20V through an external resistor divider. Alternatively, each channel is configurable as a switch.

These devices monitor the load. Accurate current sense allows for detection of open, normal, and short-circuit conditions without the need of further calibration. The current sense can multiplex between channels and devices to save ADC resources. Each channel also provides an adjustable current limit with external resistor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Fault Detection and Protection

The device includes both analog current sense and digital fault pins for full diagnostics of different fault conditions.

The current-sense voltage scale is selected based on the output-current range of interest. Figure 6-1 shows a recommended setting that allows for full diagnostics of each fault. Before the device goes into current-limit mode, the output current-sense voltage is linearly proportional to the actual load current. During a thermal-shutdown (TSD) and short-to-battery (STB) condition, the current-sense voltage is set to the fault voltage level that is specified in the *Electrical Characteristics* table.

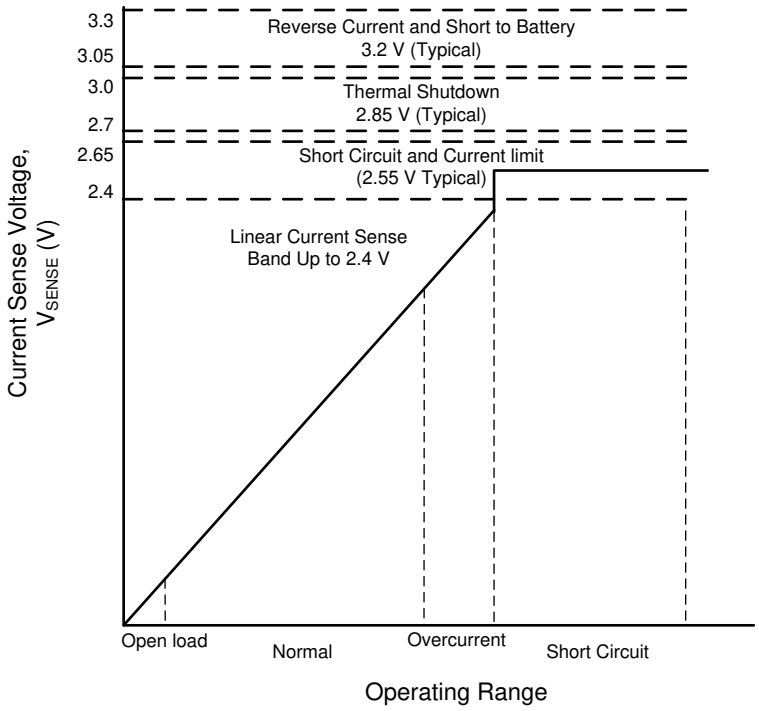


Figure 6-1. Functionality of the Current-Sense Output

6.3.2 Short-Circuit and Overcurrent Protection

The current limit on each channel is programmed by selecting the external resistor. The voltage on LIMx pin is compared with an internal voltage reference. When the threshold is exceeded, the current limit is triggered. The output of the current limited channel continues to remain on and the current is limited.

Under current-limit status, the $\overline{\text{ERR}}$ pin asserts low and the SENSE voltage of the fault channel is internally pulled up to a voltage rail from 2.4V to 2.65V as Figure 6-1 shows. At this moment, the output voltage is not disabled. The microcontroller (MCU) must monitor the voltage at the SENSEx pin or $\overline{\text{ERR}}$ pin to disable the faulted channel by pulling the $\overline{\text{ENx}}$ pin low. If a current-limit condition exists for a long period of time, thermal shutdown can trigger and shut down the output.

6.3.3 Short-to-Battery and Reverse Current Detection

Shorting the OUT pin to the battery because of a fault in the system is possible. Each channel detects this failure by comparing the voltage at the OUT and IN pins before the switch turns on. Each time the LDO switch is enabled on the rising edge of the EN pin or during the exiting of the thermal shutdown, the short-to-battery detection occurs. At this moment, if the device detects the short-to-battery fault, the LDO switch is latched off, the $\overline{\text{ERR}}$ pin is asserted low, and the fault-channel SENSE voltage is pulled up internally to a voltage rail from 3.05V to 3.3V. The device operates normally when the short-to-battery is removed and the EN pin is toggled.

ADVANCE INFORMATION

During normal operation if a short-to-battery fault results in reverse current for more than 5µs (typical), the LDO switch is latched off and the $\overline{ERR}$ pin is asserted low. To remove the latched condition after a short-to-battery (reverse current) fault, first remove the condition and then toggle the EN pin.

Series inductance and the output capacitor can produce ringing during power up or recovery from current limit, resulting in an output voltage that temporarily exceeds the input voltage. The 16ms (typical) reverse-current blanking can help filter this ringing.

For the dual-channel antenna LDO application, if both channels are enabled and one channel is shorted to ground after power up, the current drawn from the input capacitor can result in a temporary dip in the input voltage, which can trigger the reverse-current detection fault. To avoid this false trigger event, take care when selecting the input capacitor; an increase of the input capacitor value is recommended.

6.3.4 Thermal Shutdown

The device incorporates a TSD circuit as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output is turned off. When the junction temperature decreases by 15°C (typical) than the TSD trip point, the output is turned on again. The SENSE voltage is internally pulled up to a voltage rail from 2.7V to 3V during TSD status.

Note

The purpose of the design of the internal protection circuitry of the TPS7B770x-Q1 family of devices is to protect against overload conditions and is not intended as a replacement for proper heat-sinking. Continuously running the device into thermal shutdown degrades device reliability.

6.3.5 Integrated Reverse-Polarity Protection

The device integrates a reverse-connected PMOS to block the reverse current during reverse polarity at the input and output short-to-battery condition. A special ESD structure at the input is specified to withstand –40V.

6.3.6 Integrated Inductive Clamp

During output turnoff, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp to help dissipate the inductive energy stored in the cable. An internal diode is connected between OUT and GND pins with a DC-current capability of 300mA for inductive clamp protection.

6.3.7 Undervoltage Lockout

The device includes an undervoltage lockout (UVLO) threshold that is internally fixed. The undervoltage lockout activates when the input voltage on the IN pin drops below $V_{(UVLO)}$. The UVLO makes sure that the regulator is not latched into an unknown state during low input-supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required levels.

Table 6-1. Fault Table

FAILURE MODE	$V_{(SENSE)}$	$\overline{ERR}$	LDO SWITCH OUTPUT	LATCHED
Open load	$\frac{I_O \times R_{(SENSE)}}{198}$ (1)	HIGH	Enabled	No
Normal		HIGH	Enabled	No
Overcurrent		HIGH	Enabled	No
Short-circuit or current limit	2.4 to 2.65V	LOW	Enabled	No
Thermal shutdown	2.7 to 3V	LOW	Disabled	No
Output short-to-battery	3.05 to 3.3V	LOW	Disabled	Yes
Reverse current	3.05 to 3.3V	LOW	Disabled	Yes

ADVANCE INFORMATION

6.3.8 Enable (EN, EN1, and EN2)

The TPS7B7702-Q1 device features two active-high enable inputs, EN1 and EN2. The EN1 pin controls output voltage 1, OUT1, and the EN2 pin controls output voltage 2, OUT2. The devices consumes a maximum of shutdown current 5µA when the ENx pins are low. Both the EN1 and EN2 pins have a maximum internal pulldown of 10µA.

The TPS7B7701-Q1 device features one active-high enable input. The device consumes a maximum shutdown current of 5µA when the EN pin is low. The EN pin has a maximum internal pull down of 10µA.

6.3.9 Internal Voltage Regulator (V_{CC})

The device features an internal regulator that regulates the input voltage to 4.5V to power all internal circuitry. Bypass a 1µF ceramic capacitor from the V_{CC} pin to the GND pin for frequency compensation. Use the V_{CC} pin as a power supply for external circuitry with up to 15mA current capability.

6.3.10 Current Sense Multiplexing

The two, independent current sense pins (one for each channel) provide flexibility in the system design. When the ADC resource is limited, the device allows the multiplexing of the current sense pins by only using one current sense pin and one ADC to monitor all the antenna outputs.

The SENSE_SEL pin (TPS7B7702-Q1 only) selects the channels to monitor the current. The $\overline{\text{SENSE\_EN}}$ pin enables and disables the SENSE pin, allowing multiplexing between chips. Therefore, only one ADC and one resistor is needed for current-sense diagnostics of multiple outputs. When the SENSE1 pin is connected to an ADC, the current flow through both channels can be sensed by changing the electrical level at the SENSE_SEL pin.

Table 6-2 lists the selection logic for the current sense.

Table 6-2. $\overline{\text{SENSE\_EN}}$ and SEN_SEL Logic Table

$\overline{\text{SENSE\_EN}}$	SEN_SEL	SENSE1 Status	SENSE2 Status
LOW	LOW	CH1 current	CH2 current
LOW	HIGH	CH2 current	HIGH impedance
HIGH	—	HIGH impedance	HIGH impedance

Figure 6-2 shows the application of four antenna channels sharing one ADC resource.

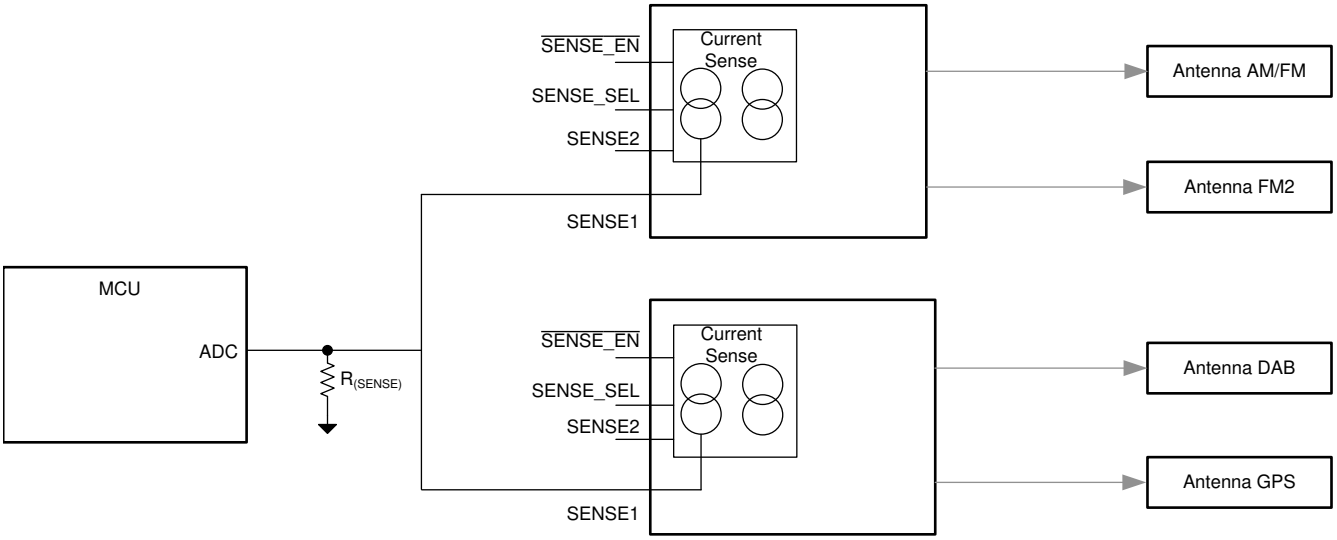


Figure 6-2. Current Multiplexing Application Block

6.3.11 Adjustable Output Voltage (FB, FB1, and FB2)

Using an external resistor divider selects an output voltage from 1.5V to 20V. Use Table 6-2 to calculate the output voltage (V_O). The recommended value for both R1 and R2 is less than 100kΩ.

$$V_O = \frac{V_{(FB)} \times (R1 + R2)}{R2} \quad (2)$$

where

- $V_{(FB)}$ = 1.233V

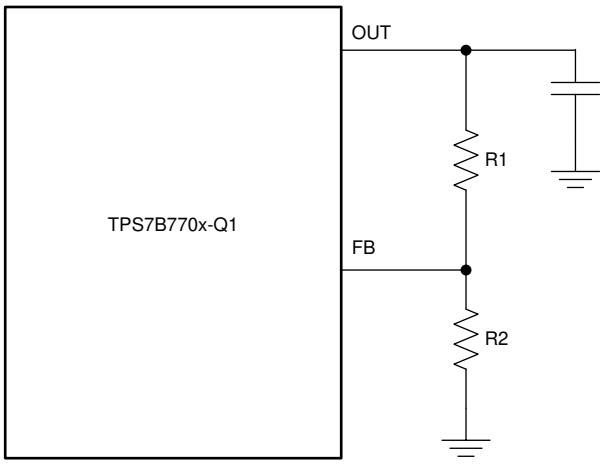


Figure 6-3. TPS7B770x-Q1 Output Voltage Setting Connection

Use the TPS7B770x-Q1 family of devices as a current-limited switch by connecting the FB pin to the GND pin.

6.4 Device Functional Modes

6.4.1 Operation With IN < 4.5V

The maximum UVLO voltage is 4V and the device operates at an input voltage above 4.5V. The device can also operate at lower input voltage. No minimum UVLO voltage is specified. At an input voltage below the actual UVLO voltage, the device does not operate.

6.4.2 Operation With EN Control

The threshold of EN rising edge is 2V (maximum). With the EN pin held above that voltage and the input voltage above 4.5V, the device becomes active. The EN falling edge is 0.7V (minimum). Holding the EN pin below that voltage disables the device which therefore reduces the quiescent current of the device.

ADVANCE INFORMATION

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS7B770x-Q1 family of devices is a single- or dual-channel 300mA LDO regulator with high, accurate current sense and a programmable current-limit function. Use the PSPICE transient model to evaluate the base function of the devices. Go to www.ti.com to download the PSPICE model and user's guide for the devices.

7.2 Typical Application

Figure 7-1 shows the typical application circuit for the TPS7B770x-Q1 family of devices. Depending on the end application, use different values of external components. An application can require a larger output capacitor during fast load steps to prevent large drops on output voltage. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

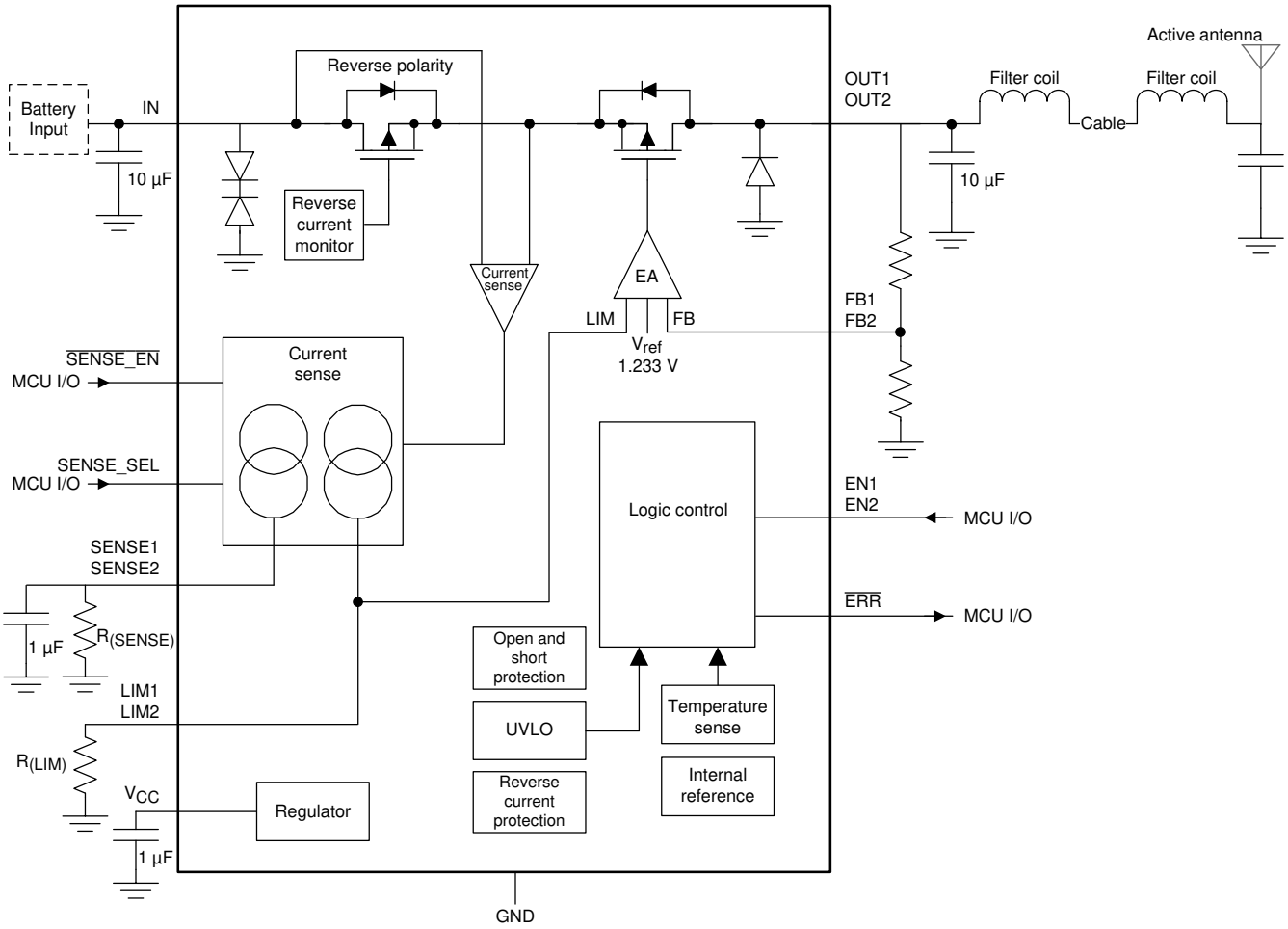


Figure 7-1. TPS7B770x-Q1 Typical Application

ADVANCE INFORMATION

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the design parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 40V
Output voltage	1.5 to 20V
Output capacitor range	2.2 to 100 µF
Output Capacitor ESR range	0.001 to 5Ω
SENSE resistor	See Current Sense Resistor Selection
Programmable current limit	50 to 300mA

7.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage
- Output voltage
- Output current
- Current limit
- ADC voltage rating

7.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10 µF. The voltage rating must be greater than the maximum input voltage.

7.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value must be from 2.2 µF to 100 µF. The ESR range must be from 1mΩ to 5Ω. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

7.2.2.3 Current Sense Resistor Selection

The current-sense outputs, SENSEx (SENSE, SENSE1, and SENSE2), are proportional to the output current at the OUT, OUT1, and OUT2 pins with a factor of 1/198. An output resistor, $R_{(SENSE)}$, must connect between the SENSEx pin and ground to generate a current sense voltage that the ADC samples. Use Equation 3 to calculate the voltage at SENSEx pin ($V_{(SENSEx)}$).

$$V_{(SENSEx)} = I_{(SENSEx)} \times R_{(SENSEx)} \quad (3)$$

where

- $$I_{(SENSEx)} = \frac{I_{(OUTx)}}{198} \quad (4)$$

For this example, select 1.5kΩ as a value for $R_{(SENSEx)}$. Do not consider the resistor and current-sense accuracy.

For a load current of 198mA, use Equation 5 to calculate the value of $V_{(SENSEx)}$.

$$I_{(SENSEx)} = \frac{I_{(OUTx)}}{198} = 1mA \rightarrow V_{(SENSEx)} = 1mA \times 1.5k\Omega = 1.5V \quad (5)$$

ADVANCE INFORMATION

To avoid any overlap between normal operation and current-limit or short-to-ground phase, using Equation 6 to select the value of the SENSE resistor is recommended.

$$R_{(SENSEx)} \leq \frac{198 \times 2.4V}{I_{Omax}} \quad (6)$$

where

- 198 is the output current to current-sense ratio
- 2.4V is the minimum possible voltage at the SENSEx pin under a short-circuit fault case
- I_{Omax} is the maximum possible output current under normal operation

To stabilize the current-sense loop, connecting a 1µF ceramic capacitor at the SENSE, SENSE1, or SENSE2 pin is required. Table 7-2 lists the current sense accuracy across temperature.

Table 7-2. Current Sense Accuracy

OUTPUT CURRENT	CURRENT SENSE ACCURACY
5mA to 10mA	20%
10mA to 50mA	10%
50mA to 100mA	5%
100mA to 300mA	3%

7.2.2.4 Current-Limit Resistor Selection

The current at the LIMx pins (LIM, LIM1, and LIM2) is proportional to the load current at the OUTx (OUT, OUT1, and OUT2) pins and is internally connected to a current-limit comparator referenced to 1.233V. The current limit is programmable through the external resistor connected at LIMx pin. Use Equation 7 to calculate the value of the external resistor, $R_{(LIMx)}$. The programmable current limit accuracy is 8% maximum across all conditions. The internal current limit of the device is set by shorting the LIM pin to ground.

$$R_{(LIMx)} = \frac{1.233V}{I_{(LIMx)}} \times 198 \quad (7)$$

where

- $$I_{(LIMx)(typical)} = \frac{1.233V}{R_{(LIMx)}} \times 198 \quad (8)$$

The current limit varies by 8%, therefore use Equation 9 to calculate the minimum current limit value and Equation 10 to calculate the maximum current limit value.

$$I_{(LIMx)(min)} = I_{(LIMx)(typical)} \times 0.92 = (0.92) \times \left(\frac{1.223V}{R_{(LIMx)}} \times 198\right) \quad (9)$$

$$I_{(LIMx)(max)} = I_{(LIMx)(typical)} \times 1.08 = (1.08) \times \left(\frac{1.223V}{R_{(LIMx)}} \times 198\right) \quad (10)$$

Select a maximum current-limit value of 200mA and use Equation 11 to calculate the value of $R_{(LIMx)}$.

$$R_{(LIMx)} = \frac{1.08 \times 198 \times 1.233V}{I_{(LIMx)(max)}} \quad (11)$$

Using Equation 11 yields a R_{LIMx} value of 1.318kΩ. The closest selectable 1% resistor is 1.33kΩ. Now using Equation 10 and plugging in 1.33kΩ for R_{LIMx} yields a maximum current of 198.2mA. Keep in mind this result does not include resistor tolerance in the calculation. To make sure that the current does not exceed the set amount, include the resistor tolerance in the equation.

ADVANCE INFORMATION

7.2.3 Application Curves

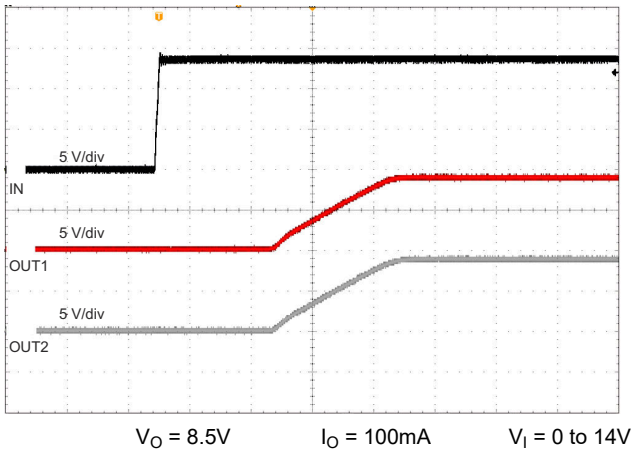


Figure 7-2. Power Up (1V/µs)

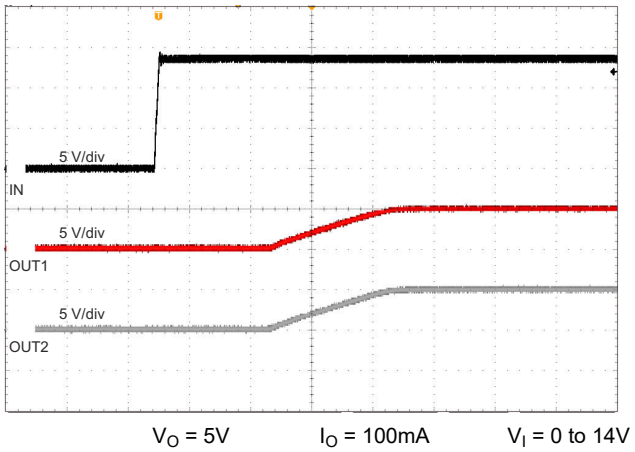


Figure 7-3. Power Up (1V/µs)

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply with a range from 4.5V to 40V. This input supply must be well-regulated. If the input supply is located more than a few inches from the TPS7B770x-Q1 device, TI recommends adding an 10µF electrolytic capacitor and a ceramic bypass capacitor at the input.

7.4 Layout

7.4.1 Layout Guidelines

For the layout of TPS7B770x-Q1 device, place the input and output capacitors close to the device as Figure 7-4 shows. To enhance the thermal performance, TI recommends surrounding the device with some vias.

Minimize equivalent-series inductance (ESL) and ESR to maximize performance and provide stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use long traces because they can negatively impact system performance and cause instability.

If possible, and to maintain the maximum performance specified in this device datasheet, use the same layout pattern used for the TPS7B770x-Q1 evaluation board, available online at www.ti.com/tool/TPS7B7702EVM.

ADVANCE INFORMATION

7.4.2 Layout Example

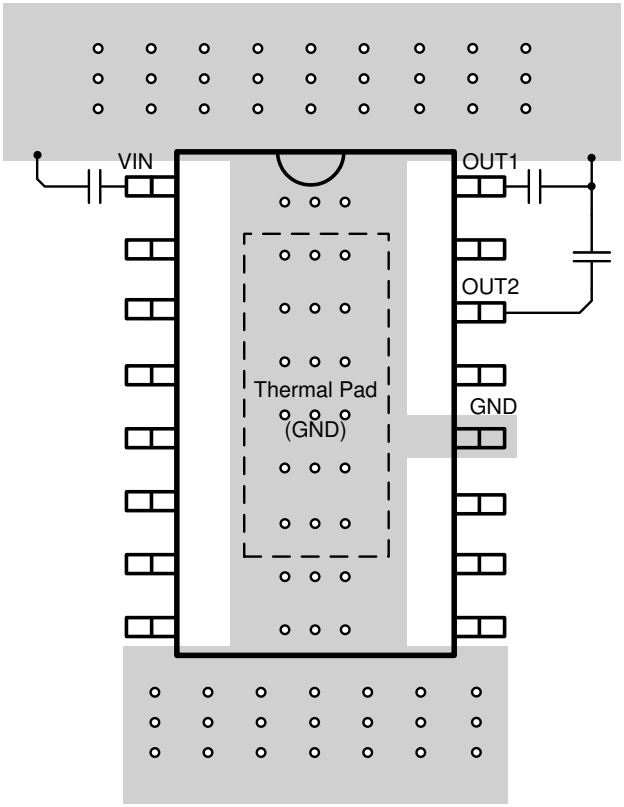


Figure 7-4. TPS7B770x-Q1 Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS7B7702-Q1 Evaluation Module* user guide

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025