TPS7B4260-Q1 Automotive, 300mA, 40V, Voltage-Tracking LDO With 6mV Tracking Tolerance

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Wide input voltage range:
  - Absolute maximum range: –40V to +45V
  - Operating range: 3.3V to 40V
- Output voltage:
  - Wide operating range: 2V to 40V
  - Output voltage flexibility: Scale V_{OUT} to values higher or lower than the reference using external resistors in a voltage divider configuration
- Maximum output current: 300mA
- Very tight output-tracking tolerance: 6mV (max)
- Low dropout voltage: 330mV at 200mA
- Combined enable and reference functionalities
- Low quiescent current at light load: 60µA
- Stable over a wide range of ceramic output capacitor values:
  - C_{OUT} range: 1µF to 100µF
  - ESR range: 1mΩ to 2Ω
- Integrated protection features:
  - Reverse current protection
  - Reverse polarity protection
  - Overtemperature protection
  - Protection against output short-circuit to ground and supply
- Available in the HSOIC (DDA) low thermal resistance ($R_{\theta JA}$ = 48°C/W) 8-pin package

2 Applications

- Powertrain pressure sensors
- Powertrain temperature sensors
- Powertrain exhaust sensors
- Powertrain fluid concentration sensors
- Body control modules (BCM)
- Zone control modules
- HVAC control modules

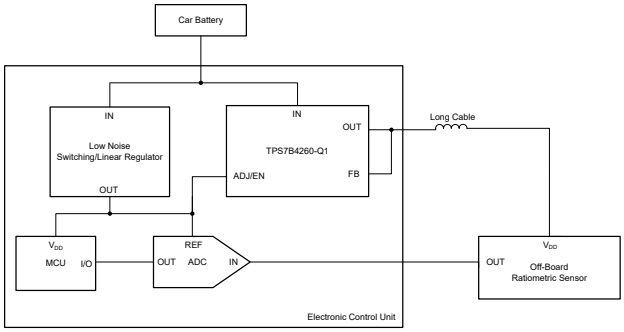
3 Description

The TPS7B4260-Q1 is a monolithic, integrated, low-dropout (LDO) voltage tracker. The device is available in an 8-pin HSOIC package. The TPS7B4260-Q1 is designed to reliably provide power to off-board sensors with a wire harness, even in harsh automotive environments. In such severe operating conditions, the cables in the harness are potentially exposed to various fault conditions, increasing risk of failure. Such conditions include short to ground, short to battery, and overtemperature. The TPS7B4260-Q1 comes with integrated protection features against each of these fault conditions, as well as protection against reverse polarity. The device incorporates a topology containing two back-to-back P-channel metal-oxide semiconductor field-effect transistors (MOSFETs). This PMOS topology eliminates the need for an external diode that is otherwise required to prevent the flow of reverse current. The high 300mA current rating of the device potentially allows a single tracker to power multiple off-board sensors simultaneously. The device is designed to handle a 45V (absolute maximum) input voltage and survive the automotive load dump transient conditions.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7B4260-Q1	DDA (HSOIC, 8)	6mm × 4.9mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

The TPS7B4260-Q1 provides a protective buffer for the ADC and MCU against fault conditions, while securely transferring power to the off-board sensors. A reference voltage applied at the adjustable input pin (ADJ/EN) is tracked with a very tight 6mV (max) tolerance at the FB pin. This tolerance holds true for all variations across the specified line, load, and temperature values. For ratiometric sensors whose output is sampled by the ADC, this tight tracking tolerance is particularly benficial. This tolerance makes sure that the error between the ADC full-scale reference and the sensor power-supply voltage is minimal. The ratiometricity of the sensor measurement is thereby maintained.

Output voltage becomes equal to the voltage at the ADJ/EN pin (± the tracking tolerance) by tying the FB pin directly to the OUT pin. If the ADC full-scale reference voltage equals the sensor supply voltage, connect the reference voltage directly to the ADJ/EN pin. If the sensor supply is lower than the reference, use a resistive divider at the ADJ/EN pin. This divider helps scale down the reference voltage to match the sensor supply voltage. If the sensor supply is higher than the reference, use a resistive divider between the FB and OUT pins. This divider helps scale up the ADC full-scale reference voltage and match the sensor supply voltage.

By setting the ADJ/EN input pin low, the TPS7B4260-Q1 switches to standby mode. In this mode, the quiescent current consumption of the LDO reduces to less than 3.8µA.

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4 Pin Configuration and Functions

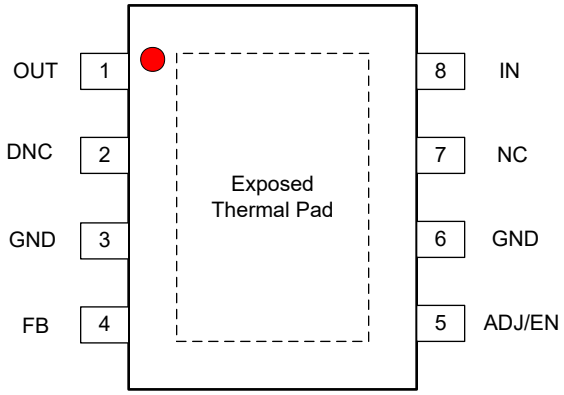


Figure 4-1. DDA Package, 8-Pin HSOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DDA		
ADJ/EN	5	I	Adjustable/enable input pin. Connect the external reference voltage to this pin. This pin connects to the inverting input of the error amplifier internally. A low signal below V_{IL} disables the device, and a high signal above V_{IH} enables the device. Connect the voltage reference directly, or with a voltage divider to attain output voltages lower than the reference. To compensate for line influences, place a 0.1µF capacitor close to this pin.
DNC	2	—	Do not connect a voltage source to this pin. Either leave the pin floating or connect to GND to improve thermal performance.
FB	4	I	Feedback pin. This pin is connected to the noninverting input of the error amplifier internally and controls the output voltage. For output voltages equal to or less than the external reference voltage, connect this pin directly to the output pin. To attain output voltage values higher than the reference, use a voltage divider with external feedback resistors.
GND	6, 3	G	GND pin. Connect this pin to a low impedance path to ground.
IN	8	I	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND. See the *Recommended Operating Conditions* table. Place the input capacitor as close to the input pin of the device as possible to compensate for line influences. See the *Input and Output Capacitor Selection* section for more details.
NC	7	—	Not internally connected. For best thermal performance, connect these pins to GND.
OUT	1	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. Select a ceramic capacitor within the range of C_{OUT} values provided in the *Recommended Operating Conditions* table. Place this capacitor as close to output of the device as possible. See the *Input and Output Capacitor Selection* section for more details.
Thermal Pad	Pad		Thermal pad. Connect the pad to GND for best possible thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input pin voltage	–40	45	V
V_{OUT}	Regulated output pin voltage	–5	45	V
V_{IN} - V_{OUT}	Input-output differential	-45	45	V
V_{FB}	Feedback pin voltage	–5	45	V
$V_{ADJ/EN}$	Adjustable reference and enable pin voltage	–40	45	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may effect the device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2500	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000	
			Corner pins		

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	3.3		40	V
V_{OUT}	Output voltage	2		40	V
$V_{ADJ/EN}$	Adjust pin voltage	2		40	V
V_{FB}	Feedback pin voltage	0		40	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor(1)		1		µF
C_{OUT}	Output capacitor(2)	1		100	µF
ESR	Output capacitor ESR requirements	0.001		2	Ω
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance recommended is 500nF.
(2) Effective output capacitance of 500nF minimum is required for stability.

5.4 Thermal Information

THERMAL METRIC[1] [2]		TPS7B4260-Q1	
		DDA (HSOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	71.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.3	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	11.5	°C/W

(1) The thermal data is based on the JEDEC standard high-K board layout, JESD 51-7. This board is a two-signal, two-plane, four-layer board with 2-oz. copper on the external layers. The copper pad is soldered to the thermal land pattern. Also, incorporate correct attachment procedure.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

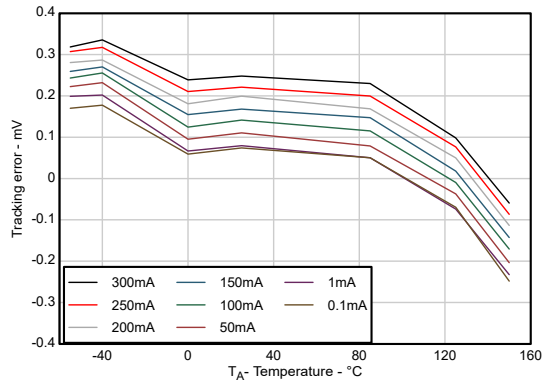
5.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, V_{OUT} = V_{FB}, I_{OUT} = 100µA, C_{OUT} = 1µF, C_{IN} = 1µF and $V_{ADJ/EN}$ = 5V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	V_{IN} = 6.2V to 40V, I_{OUT} = 100µA, T_J = 25ºC		60	72	µA
		V_{IN} = 6.2V to 40V, I_{OUT} = 100µA, –40ºC < T_J < 85ºC			77	
		V_{IN} = 6.2V to 40V, I_{OUT} = 100µA			83	
I_{GND}	Ground current	V_{IN} = 6.2V to 40V, $V_{ADJ/EN}$ = 5V, I_{OUT} = 300mA			2.45	mA
$I_{SHUTDOWN}$	Shutdown supply current	$V_{ADJ/EN}$ = 0V			3.8	µA
$I_{ADJ/EN}$	ADJ/EN pin current	I_{OUT} = 100µA			1.2	µA
$V_{UVLO\ (RISING)}$	Rising input supply UVLO	V_{IN} rising, I_{OUT} = 5mA	2.6	2.7	2.85	V
$V_{UVLO\ (FALLING)}$	Falling input supply UVLO	V_{IN} falling, I_{OUT} = 5mA	2.3	2.4	2.5	V
$V_{UVLO\ (HYST)}$	$V_{UVLO(IN)}$ hysteresis			300		mV
V_{IL}	Enable logic input low level				0.8	V
V_{IH}	Enable logic input high level		1.8			V
ΔV_{OUT}	Output voltage tracking accuracy	V_{IN} = V_{OUT} + 1.2V to 40V, I_{OUT} = 100µA to 300mA (1)	–6		6	mV
$\Delta V_{OUT\ (\Delta VIN)}$	Line regulation	V_{IN} = V_{OUT} + 1.2V to 40V, I_{OUT} = 100µA	–0.4		0.4	mV
$\Delta V_{OUT\ (\Delta IOUT)}$	Load regulation	V_{IN} = V_{OUT} + 1.2V, I_{OUT} = 100µA to 300mA (1)			0.6	mV
V_{DO}	Dropout voltage	I_{OUT} = 200mA, $V_{ADJ/EN}$ ≥ 3.3V, V_{IN} = $V_{ADJ/EN}$		330	665	mV
I_{CL}	Output current limit	V_{IN} = V_{OUT} + 1.2V, V_{OUT} short to 90% x $V_{ADJ/EN}$	320	460	530	mA
PSRR	Power-supply ripple rejection	V_{RIPPLE} = 1V_{PP}, frequency = 100Hz, I_{OUT} ≥ 5mA		80		dB
V_n	Output noise voltage	V_{OUT} = 3.3V, I_{OUT} = 1mA, BW = 10Hz to 100KHz, a 5µV_{RMS} reference is used for this measurement		150		µV_{RMS}
I_{REV}	Reverse current at V_{IN}	V_{IN} = 0V, V_{OUT} = 32V	–0.6		0.6	µA
I_{REV-N1}	Reverse current at negative V_{IN}	V_{IN} = –20V, V_{OUT} = 20V	–1.2		1.2	µA
I_{FB}	Feedback pin current			0.1	0.25	µA
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			15		°C

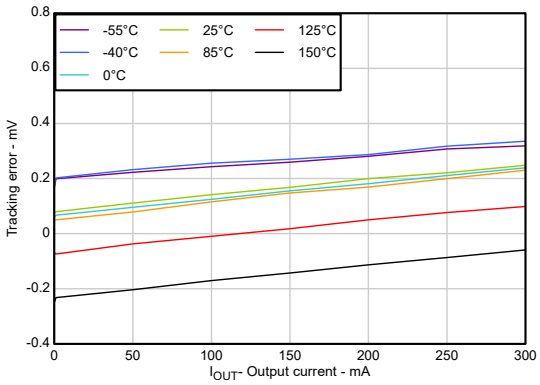
(1) Because the power dissipation is potentially large, this specification is measured using pulse testing with a low duty cycle. See the thermal information table for more information on how much power the device dissipates while maintaining a junction temperature below 150°C.

5.6 Typical Characteristics



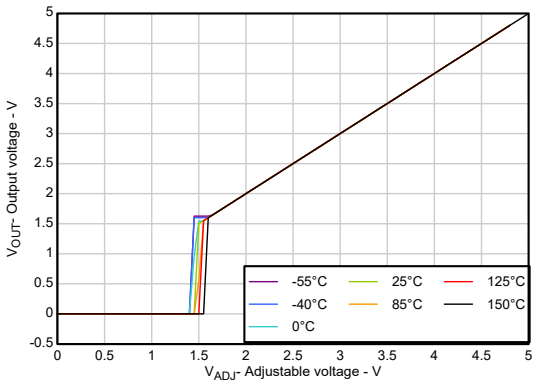
V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}

Figure 5-1. Tracking Error vs Ambient Temperature



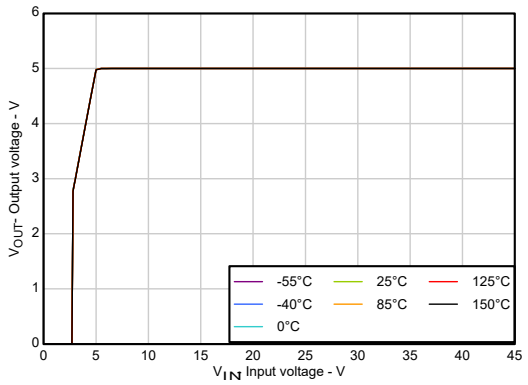
V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}

Figure 5-2. Tracking Error vs Output Current



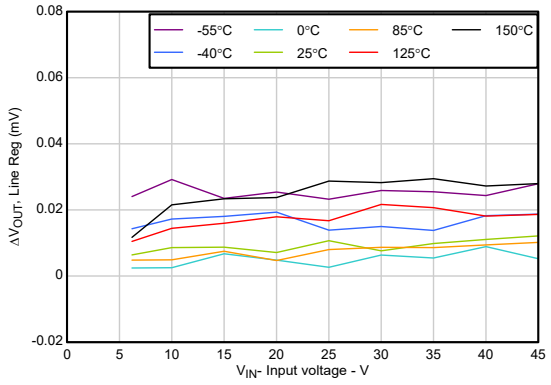
V_{IN} = 13.5V, V_{FB} = V_{OUT}, I_{OUT} = 10mA

Figure 5-3. Output Voltage vs Adjustable Reference Voltage



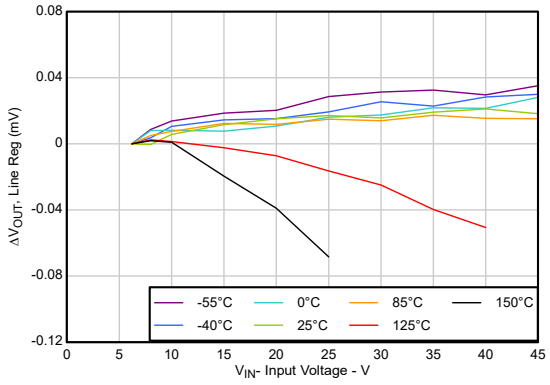
$V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, I_{OUT} = 10mA

Figure 5-4. Output Voltage vs Input Voltage



$V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, I_{OUT} = 100µA

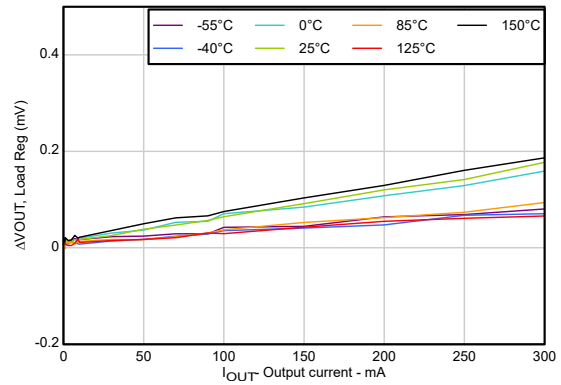
Figure 5-5. Line Regulation



$V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, I_{OUT} = 200mA

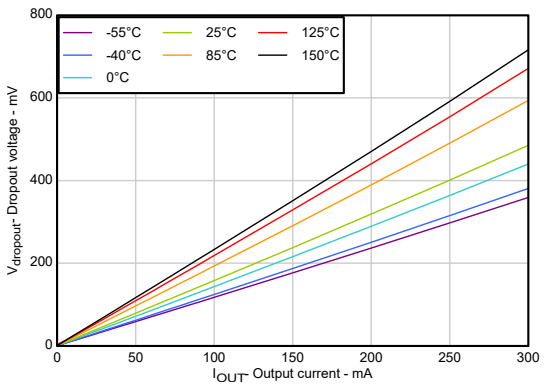
Figure 5-6. Line Regulation

5.6 Typical Characteristics (continued)



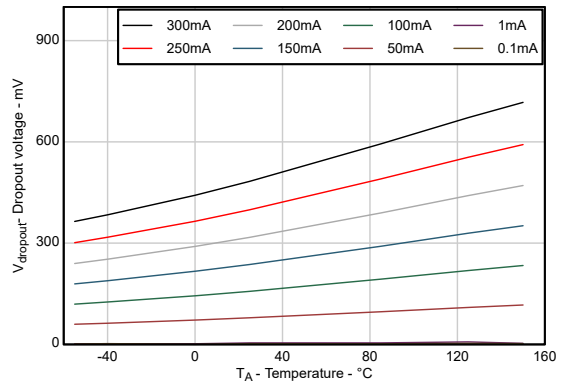
V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}

Figure 5-7. Load Regulation



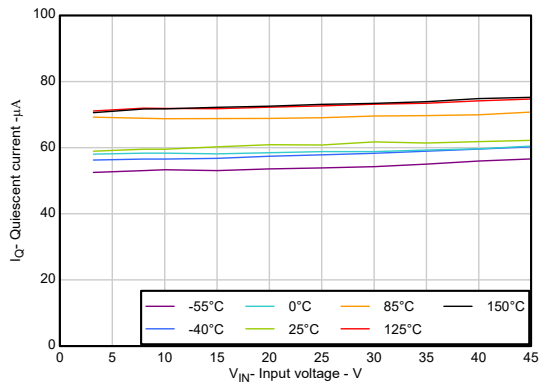
V_{IN} = 5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}

Figure 5-8. Dropout Voltage vs Load Current



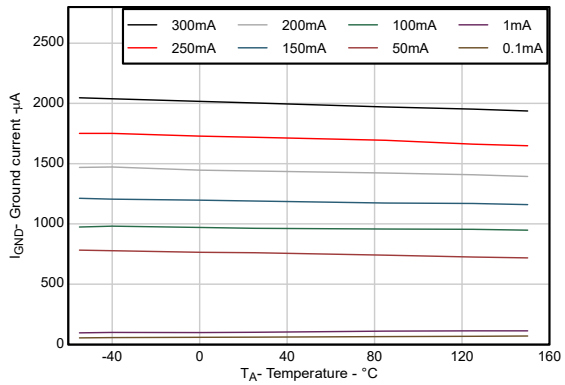
V_{IN} = 5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}

Figure 5-9. Dropout Voltage vs Ambient Temperature



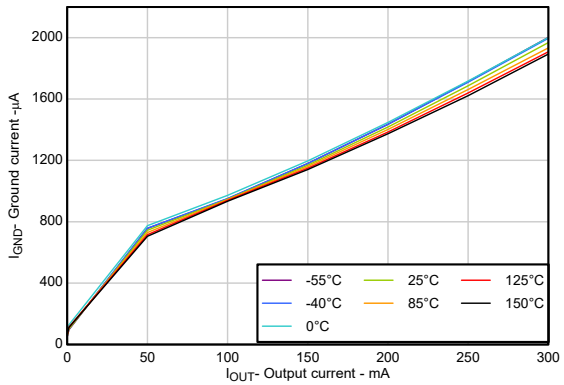
$V_{ADJ/EN}$ = 2V, V_{FB} = V_{OUT}, I_{OUT} = 100µA

Figure 5-10. Quiescent Current vs Input Voltage



V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}

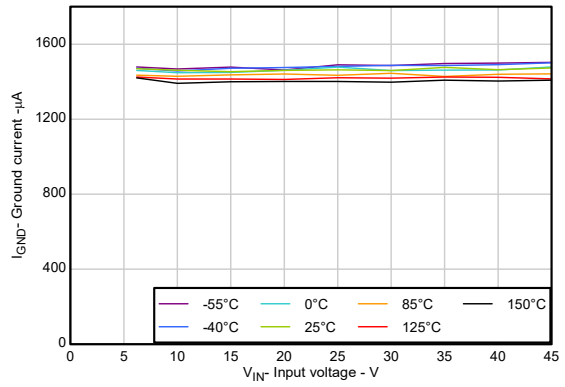
Figure 5-11. Ground Current vs Ambient Temperature



V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}

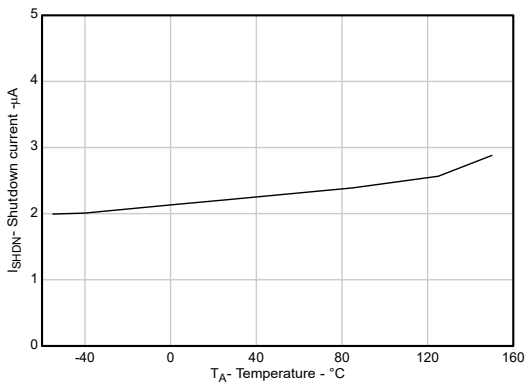
Figure 5-12. Ground Current vs Output Current

5.6 Typical Characteristics (continued)



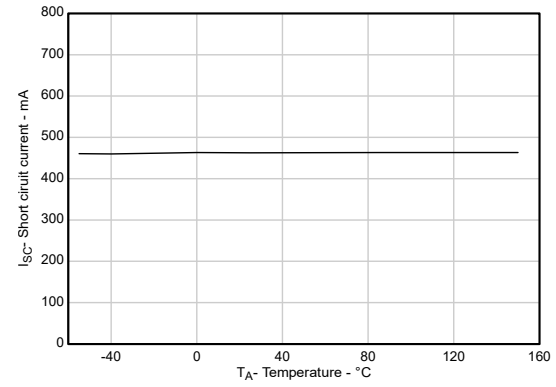
$V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, I_{OUT} = 200mA

Figure 5-13. Ground Current vs Input Voltage



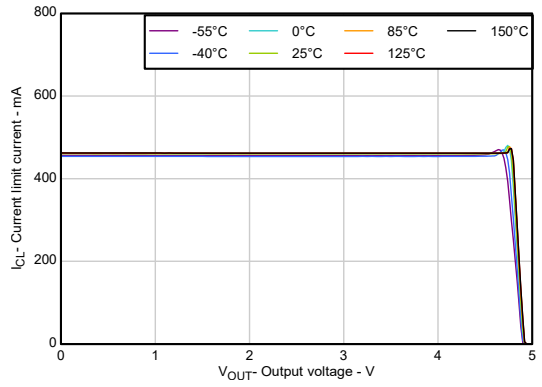
V_{IN} = 13.5V, $V_{ADJ/EN}$ = 0V, V_{FB} = V_{OUT}

Figure 5-14. Shutdown Current vs Ambient Temperature



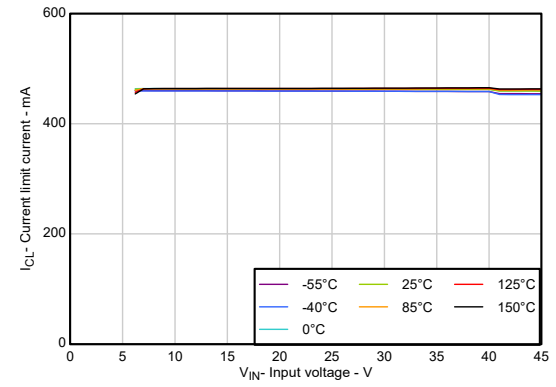
V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{OUT} = 0.9 × $V_{OUT\ NOM}$

Figure 5-15. Current Limit vs Ambient Temperature



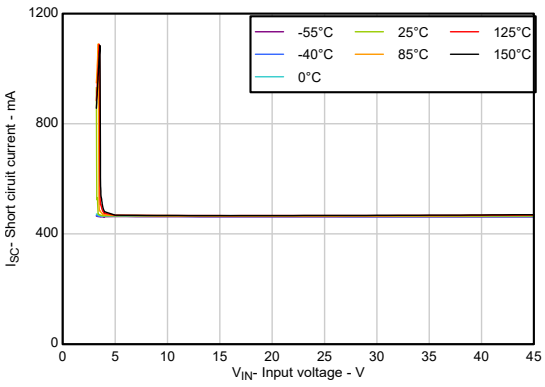
V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V

Figure 5-16. Current Limit vs Output Voltage



$V_{ADJ/EN}$ = 5V, V_{OUT} = 0.9 × $V_{OUT\ NOM}$

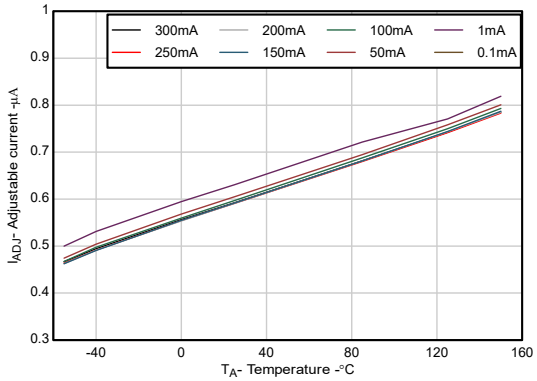
Figure 5-17. Current Limit vs Input Voltage



$V_{ADJ/EN}$ = 2V, V_{OUT} = 0V

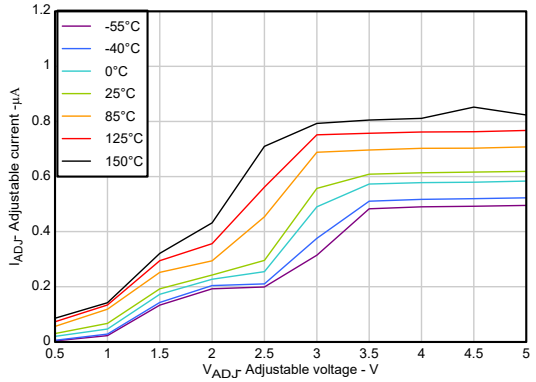
Figure 5-18. Current Limit vs Input Voltage

5.6 Typical Characteristics (continued)



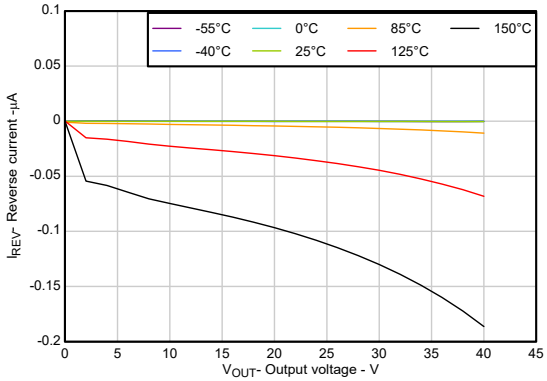
V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}

Figure 5-19. Adjustable Pin Leakage Current vs Ambient Temperature



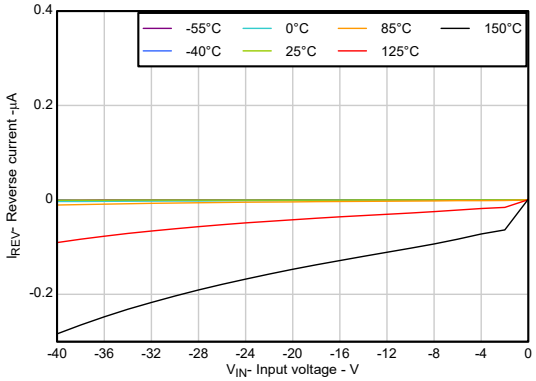
V_{IN} = 13.5V, V_{FB} = V_{OUT}, I_{OUT} = 200mA

Figure 5-20. Adjustable Pin Leakage Current vs Adjustable Pin Voltage



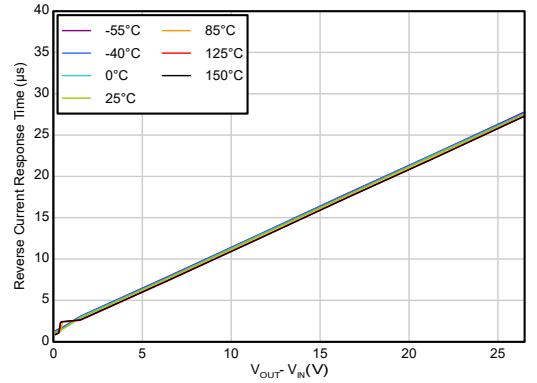
V_{IN} = 0V, V_{FB} = V_{OUT}, $V_{ADJ/EN}$ = 5V

Figure 5-21. Reverse Leakage Current vs Output Voltage



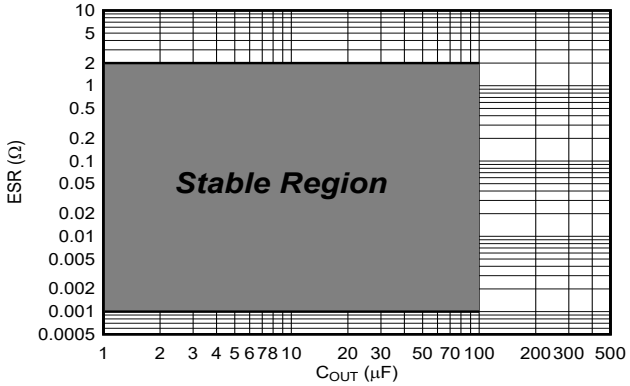
V_{OUT} = 0V, V_{FB} = V_{OUT}, $V_{ADJ/EN}$ = 5V

Figure 5-22. Reverse Leakage Current vs Input Voltage



V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, simulation results

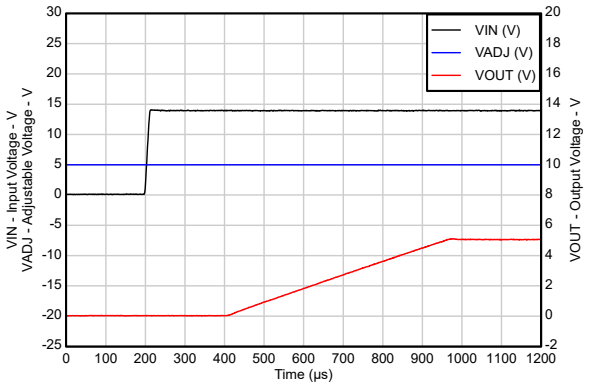
Figure 5-23. Reverse Current Protection Response Time vs Output-Input Differential Voltage



Stable region: 1mΩ ≤ ESR ≤ 2Ω, 1µF ≤ C_{OUT} ≤ 100µF

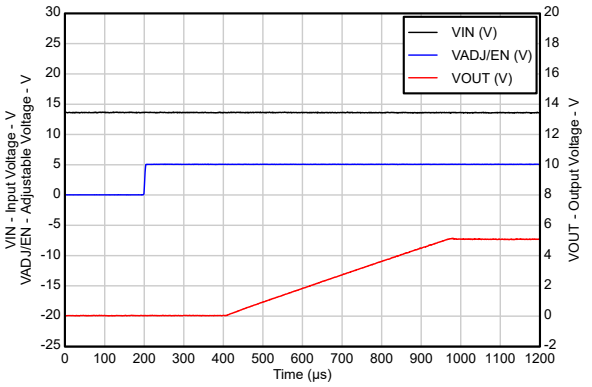
Figure 5-24. ESR vs Load Capacitance

5.6 Typical Characteristics (continued)



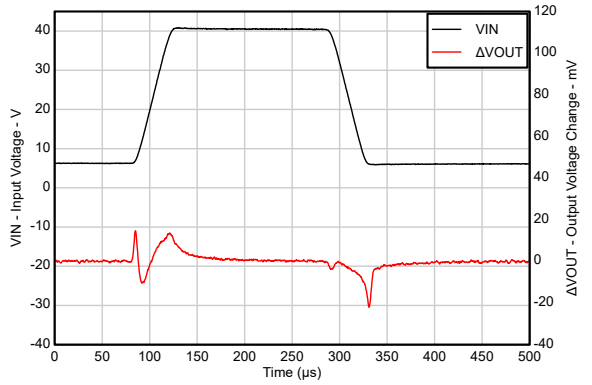
V_{IN} = 0V to 13.5V at a rate of 1V/µs, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, C_{OUT} = 1µF, I_{OUT} = 200mA

Figure 5-25. Start-Up Profile



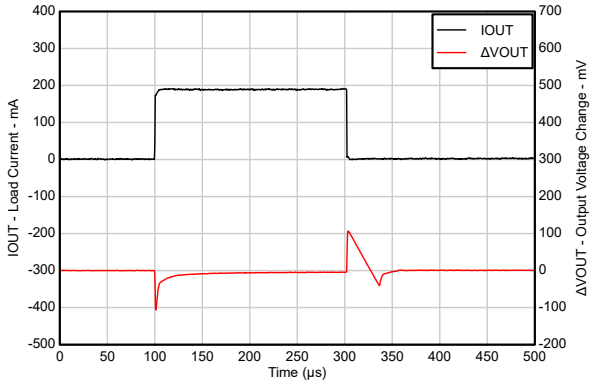
$V_{ADJ/EN}$ = 0V to 5V at a rate of 1V/µs, V_{IN} = 13.5V, V_{FB} = V_{OUT}, C_{OUT} = 1µF, I_{OUT} = 200mA

Figure 5-26. Start-Up Profile



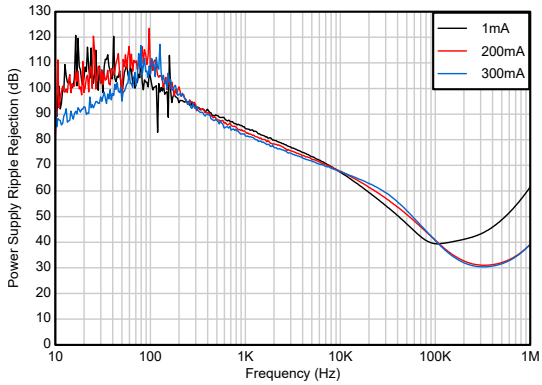
V_{IN} = 6V to 40V at a rate of 1V/µs, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, C_{OUT} = 1µF, I_{OUT} = 200mA

Figure 5-27. Line Transient



V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, C_{OUT} = 1µF, I_{OUT} = 1mA to 200mA at 1A/µs

Figure 5-28. Load Transient



V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, C_{OUT} = 1µF

Figure 5-29. PSRR vs Frequency

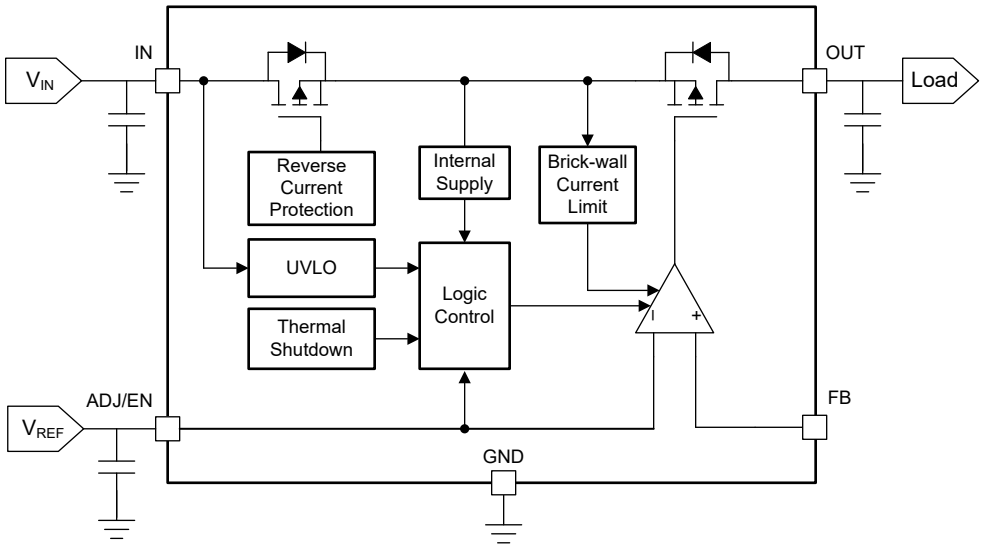
6 Detailed Description

6.1 Overview

The TPS7B4260-Q1 is an integrated, low-dropout (LDO) voltage tracker with ultra-low tracking tolerance. Because of the high risk of cable shorts when powering off-board sensors, multiple features are built into the LDO. These features protect against fault conditions resulting in short to battery, short to GND, and reverse current flow.

In addition, this device also features thermal shutdown protection, brick-wall current limiting, undervoltage lockout (UVLO), and reverse polarity protection.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Tracker Output Voltage (V_{OUT})

Because this device is a tracking LDO, the output voltage is determined by the voltage provided to the ADJ/EN pin. The LDO remains disabled as long as $V_{ADJ/EN}$ is less than V_{IL}. When $V_{ADJ/EN}$ exceeds V_{IH}, the output voltage V_{OUT} begins to rise. The device has a soft-start feature incorporated, which allows the output voltage to rise linearly and limits the in-rush current at start-up. After start-up and attaining steady state, V_{FB} remains within ±6mV from the voltage set on the ADJ/EN pin over all specified operating conditions. V_{FB} is the feedback pin voltage.

6.3.1.1 Output Voltage Equal to Reference Voltage

Figure 6-1 shows the external reference voltage applied directly to the ADJ/EN pin and the FB pin connected to the OUT pin. Under these conditions, the LDO output voltage is equal to the reference voltage, as given in Equation 1.

$$V_{OUT} = V_{REF} \quad (1)$$

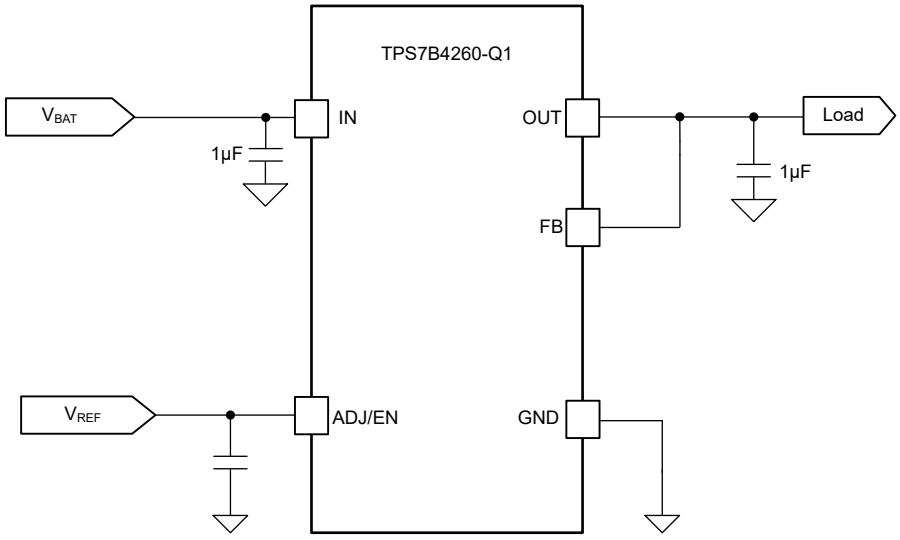


Figure 6-1. Tracker Output Voltage Equal to Reference Voltage

6.3.1.2 Output Voltage Less Than the Reference Voltage

Connecting an external resistor divider at the ADJ/EN pin, as shown in Figure 6-2, helps generate an output voltage lower than the reference voltage. Make sure both R_1 and R_2 are less than 100kΩ to minimize the error in voltage caused by the ADJ/EN pin leakage current, $I_{ADJ/EN}$. Equation 2 calculates V_{OUT}.

$$V_{OUT} = \frac{(V_{REF} \times R_2)}{R_1 + R_2} \quad (2)$$

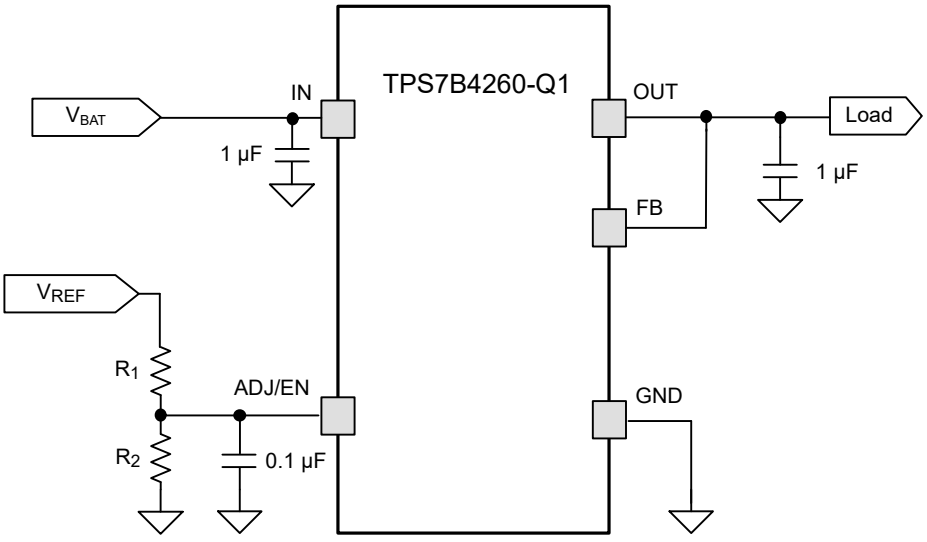


Figure 6-2. Tracker Output Voltage Less Than the Reference Voltage

6.3.1.3 Output Voltage Larger than the Reference Voltage

Connecting an external resistor divider between the OUT and FB pin, as shown in Figure 6-3, helps generate an output voltage higher than the reference voltage. Make sure R_1 and R_2 are less than 100kΩ to minimize the error in voltage caused by the FB pin leakage current, I_{FB}. Equation 3 calculates V_{OUT}.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

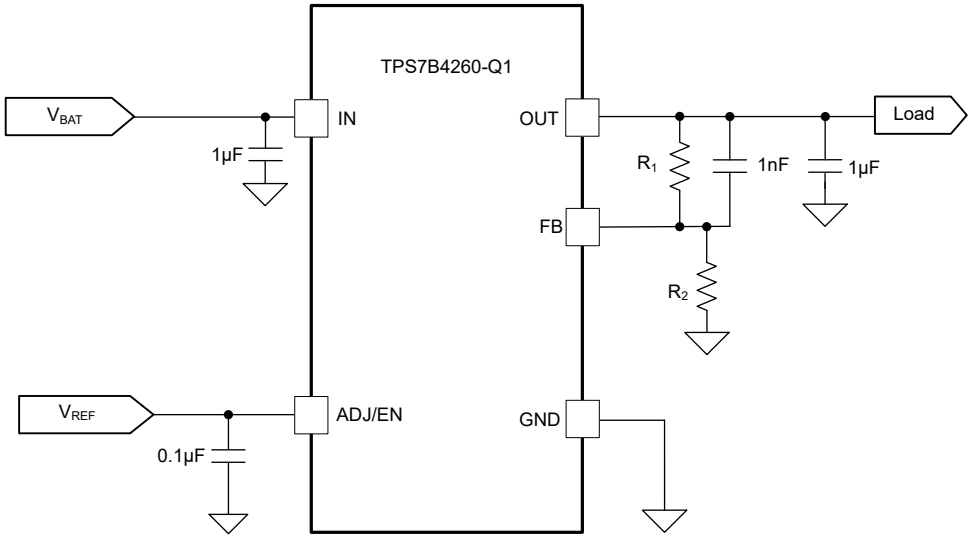


Figure 6-3. Tracker Voltage Larger Than the Reference Voltage

6.3.2 Reverse Current Protection

The TPS7B4260-Q1 incorporates a back-to-back PMOS topology. This topology protects the device against fault conditions resulting in V_{OUT} being higher than V_{IN} and blocks the flow of reverse current. No damage occurs to the device if this fault condition occurs, provided the *Absolute Maximum Ratings* are not violated. This integrated protection feature eliminates the need for an external diode. The reverse current comparator typically responds to a reverse voltage condition in 10µs. The comparator, along with the body diode of the blocking PMOS transistor, limits the reverse current to less than 1.2µA. I_{REV} is specified in the *Electrical Characteristics* table.

6.3.3 Undervoltage Lockout

The device has an internally fixed undervoltage lockout (UVLO) threshold. Undervoltage lockout activates when the input voltage V_{IN} drops below the undervoltage lockout level (see the $V_{UVLO(FALLING)}$ parameter in the *Electrical Characteristics* table). This activation makes sure the regulator is not latched into an unknown state during a low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold, the regulator shuts down. The regulator powers up in the standard power-up sequence when the input voltage recovers to the required level. See the $V_{UVLO(RISING)}$ parameter in the *Electrical Characteristics* table.

6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C, which then allows the device to cool. This feature limits the thermal dissipation within the regulator, thus protecting the regulator from damage as a result of overheating. When the junction temperature cools to approximately 160°C, the output circuitry enables. Although the device is enabled at such high temperatures, the device parameters and performance are specified up to a junction temperature of 150°C. Power dissipation, thermal resistance, and ambient temperature are the parameters that determine if the thermal protection circuit becomes enabled. When enabled, unless the power dissipation or the ambient temperature (or both) are reduced, the protection circuit continues to cycle between on and off states.

The internal protection circuitry of the TPS7B4260-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS7B4260-Q1 into thermal shutdown degrades device reliability.

6.3.5 Current Limit

The device has an internal current limit circuit that protects the device during overcurrent or shorting conditions. The current-limit circuit, as shown in Figure 6-4, is a brick-wall scheme. When the device is in current limit, the device sources I_{CL} and the output voltage is not regulated. In this scenario, the output voltage depends on the load impedance.

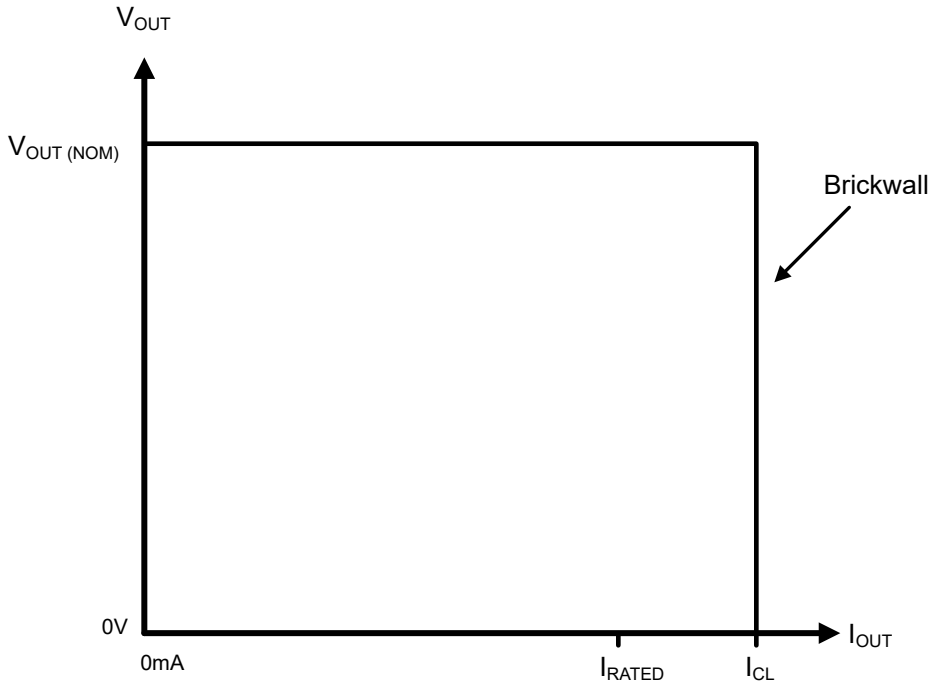


Figure 6-4. Brickwall Current Limit Scheme

During current-limit events, the potential for high power dissipation exists because of the elevated current level and the increased input-to-output differential voltage (V_{IN} – V_{OUT}). If the heat dissipation is substantial, the device enters thermal shutdown. If the current-limit condition is not removed when the device turns back on after cooling, the device enters thermal shutdown again. This cycle continues until the current-limit condition is removed. The device survives this fault, but repeatedly operating in this mode degrades long-term reliability.

The current limit (I_{CL}) for this device meets the specification provided in the *Electrical Characteristics* when the input voltage is V_{IN} ≥ 3.7V. If the device output shorts to ground when operating in the range 3.3V ≤ V_{IN} < 3.7V, current larger than I_{CL} flows through the device. This behavior is described in Figure 5-18.

6.3.6 Output Short to Battery

Figure 6-5 describes a situation where the TPS7B4260-Q1 is powered directly by the battery, and the output shorts to the battery. The TPS7B4260-Q1 survives this fault condition and no damage occurs to the device so long as the absolute maximum ratings are not voilated. Figure 6-6 describes a situation where the output shorts to the battery when the device is powered by a voltage source that is lower than V_{BAT}. In this example, the TPS7B4260-Q1 supply input voltage is set at 7V when the tracker output shorts to the battery. The tracker output typically runs at 5V and the battery typically runs at 14V. The back-to-back PMOS transistor topology helps limit the continuous reverse current flowing through V_{IN} to I_{REV}, as provided in the *Electrical Characteristics* table.

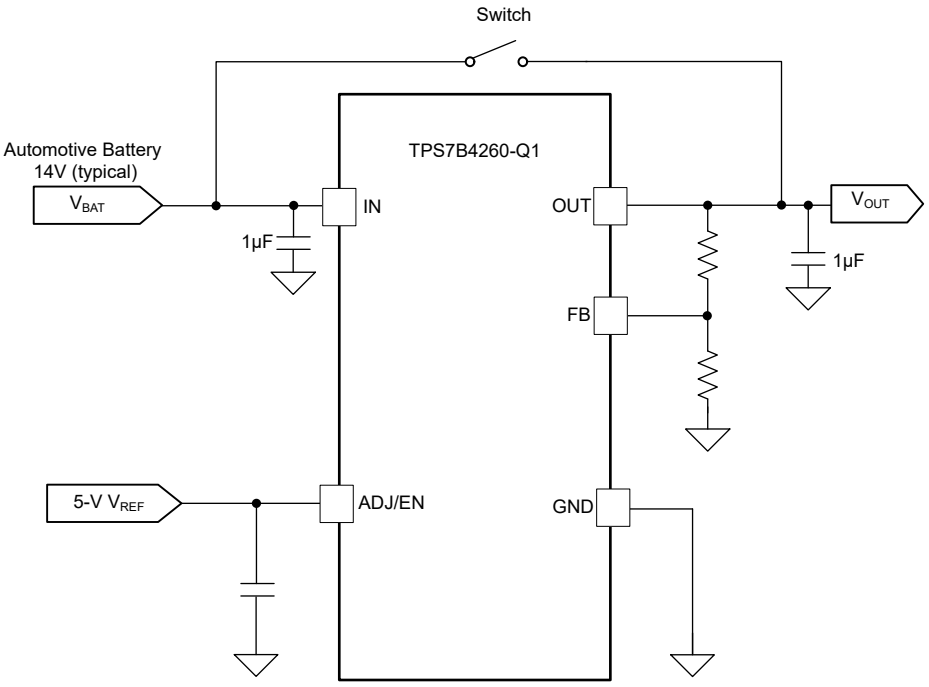


Figure 6-5. Tracker Output Short to Battery

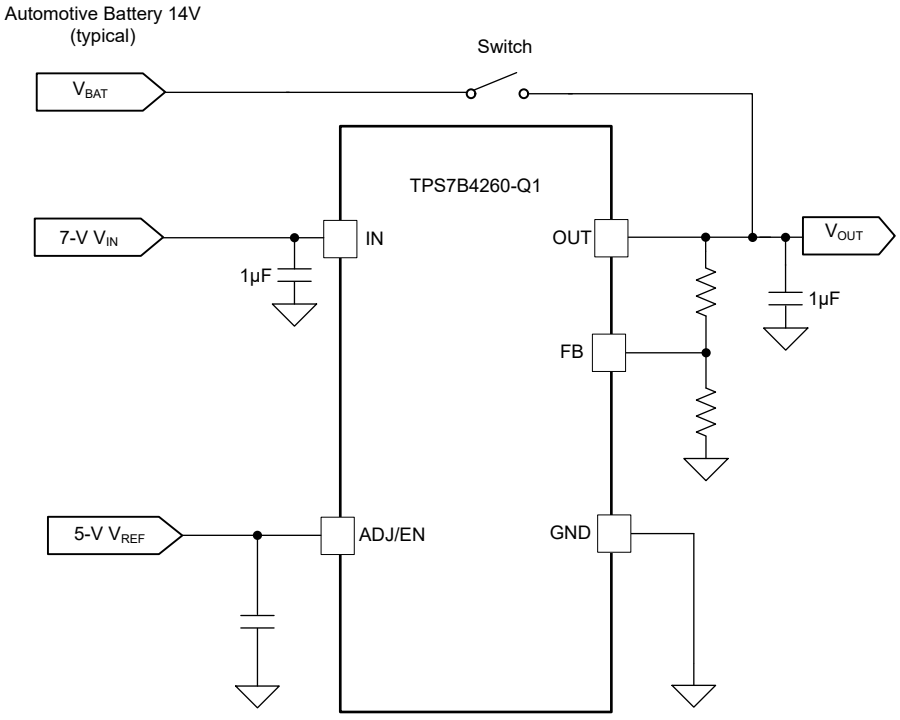


Figure 6-6. Tracker Output Voltage Higher Than the Input Voltage

6.3.7 Tracking Regulator With an Enable Circuit

By pulling the reference voltage below V_{IL}, the device disables and enters a sleep state where the device draws 3.8µA (max) from the power supply. In a typical application, the reference voltage is generally sourced from another LDO voltage rail. Disabling the device without shutting down the reference voltage is possible. Configure the device as shown in Figure 6-7 in this case. The TPS7B84-Q1 is a 150mA LDO with ultra-low quiescent current that provides the reference voltage to both the TPS7B4260-Q1 and the ADC. The operational status of the device is controlled by a microcontroller (MCU) input or output (I/O).

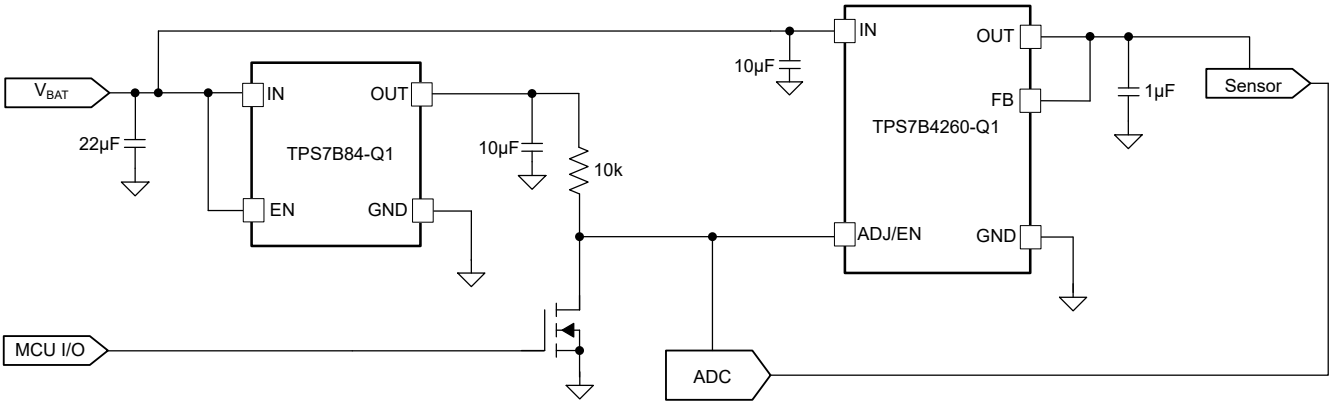


Figure 6-7. Tracking LDO With an Enable Circuit

6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER(1)			
	V_{IN}	$V_{ADJ/EN}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(Nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{ADJ/EN} > V_{IH}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J \leq 150°C$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ADJ/EN} > V_{IH}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ADJ/EN} < V_{IL}$	Not applicable	$T_J > T_{SD(shutdown)}$

(1) The device turns on when V_{IN} is greater than $V_{UVLO(RISING)}$ and $V_{ADJ/EN}$ is greater than the enable rising threshold V_{IH}.

6.4.1 Normal Operation

The device output voltage $V_{OUT(Nom)}$ tracks the reference voltage at the ADJ/EN pin when the following conditions are met:

- The input voltage is at least 3.3V ($V_{IN(min)}$) and greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The reference voltage at the ADJ/EN pin is greater than the enable rising threshold V_{IH} and stays stable at the appropriate V_{REF} value
- The output current is less than $I_{OUT(max)}$ ($I_{OUT} \leq 300mA$)
- The device junction temperature does not exceed 150°C ($T_J \leq 150°C$).

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

In the dropout state, the pass transistor of the tracker is driven into the ohmic or triode region. In this state, the input and output voltages are related as $V_{IN} < V_{OUT(NOM)} + V_{DO}$. If the tracker device enters dropout directly from normal regulation, the pass transistor transitions from saturation to the triode region. From such a scenario, if the input voltage returns to a value $V_{IN} > V_{OUT(NOM)} + V_{DO}$, the device exits dropout. The tracker takes a short period of time to pull the pass transistor back into saturation from the triode region. During this short time period when the device is exiting dropout, the output voltage potentially has a significant overshoot.

6.4.3 Operation With V_{IN} < 3.3V

For input voltages below 3.3V and above $V_{UVLO\ (FALLING)}$, the LDO continues to operate. However, certain internal circuits potentially do not have proper headroom to operate within specification. When the input voltage drops below $V_{UVLO\ (FALLING)}$, the device shuts off.

6.4.4 Disable With ADJ/EN Control

The ADJ/EN pin operates as both the reference and the enable pin to the LDO. The LDO disables if $V_{ADJ/EN}$ is taken less than V_{IL}. When disabled, the pass transistor is turned off, the internal circuits are shutdown, and the LDO is in a low-power mode.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ when the pass transistor is fully on. V_{IN} is the input voltage and V_{OUT} is the output voltage. This condition arises when the input voltage falls to a point where the error amplifier drives the gate of the pass transistor to the rail. During this condition, there is no remaining headroom for the control loop to operate. At this operating point, the pass transistor is driven fully on. Dropout voltage directly specifies the minimum $V_{IN} − V_{OUT}$ differential the device requires to maintain a regulated output voltage. If the input voltage falls to less than the nominal output regulation, then the output voltage follows, minus the dropout voltage (V_{DO}).

In dropout mode, the output voltage is no longer regulated, and transient performance is severely degraded. The device loses PSRR, and load transients potentially cause large output voltage deviation.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated output current (I_{RATED}), the dropout voltage for that current scales accordingly. I_{RATED} is specified in the *Recommended Operating Conditions* table. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{4}$$

7.1.2 Reverse Current

The TPS7B4260-Q1 incorporates reverse current protection that prevents damage from fault conditions that result in V_{OUT} being higher than V_{IN}. The reverse current comparator typically responds to a reverse voltage condition in 10µs. The comparator along with the body diode of the blocking PMOS transistor, limits the reverse current to less than 1.2µA. As long as the absolute maximum ratings are not violated, no damage occurs to the device.

7.2 Typical Application

Figure 7-1 shows a typical application circuit for the TPS7B4260-Q1.

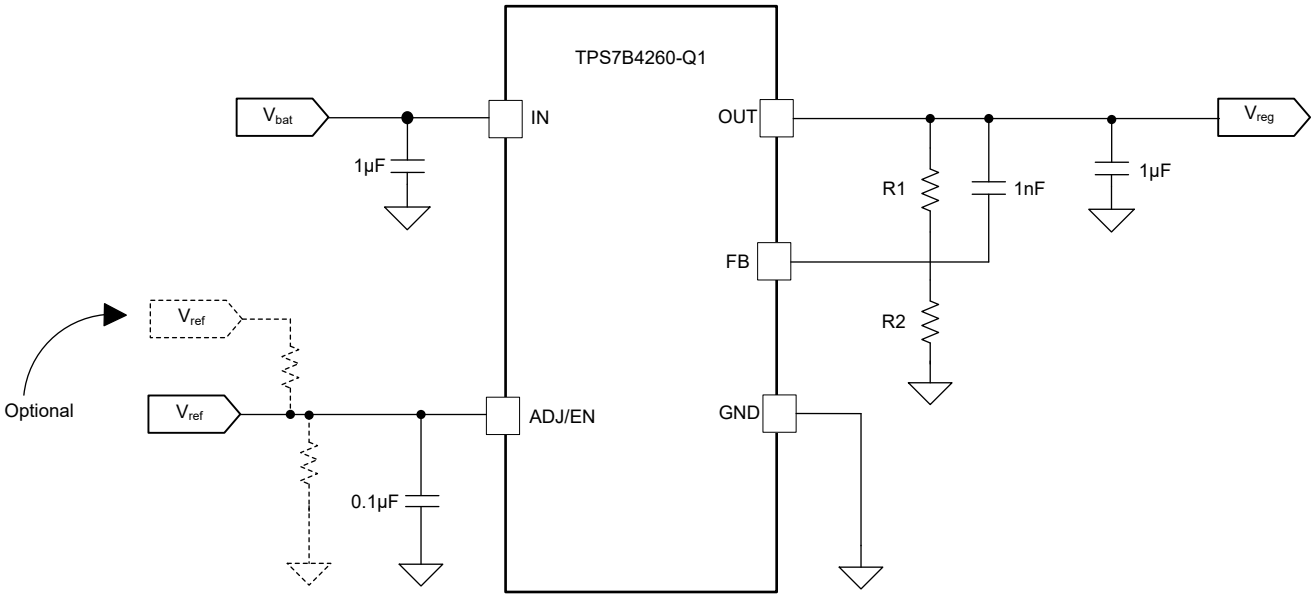


Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

Use the parameters listed in Table 7-1 for this design example.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage	3.3V to 40V
ADJ/EN reference voltage	2V to 40V
Output voltage	2V to 40V
Output current rating	300mA
Output capacitor range	1µF to 100µF
Output capacitor ESR range	1mΩ to 2Ω

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Selection

Depending on the end application, different values of external components are available. Some applications use a large output capacitor to support fast load steps. The large capacitor helps prevent a significant droop in output voltage, which otherwise results in a reset of downstream components. Use a low equivalent series resistance (ESR) ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

The TPS7B4260-Q1 requires an output capacitor of at least 1µF (500nF or larger capacitance) for stability and an ESR between 0.001Ω and 2Ω. Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For most applications, a low ESR, 10µF ceramic capacitor on the OUT pin is sufficient to provide excellent transient performance.

An input capacitor is not required for stability. However, good analog practice is to connect a capacitor (500nF or higher) between the GND and IN pin of the TPS7B4260-Q1. Some input supplies have a high impedance,

thus placing the input capacitor on the input supply helps reduce input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.2.2.2 Feedback Resistor Selection

V_{OUT} is set by the voltage at the ADJ/EN pin and the external feedback resistors R_1 and R_2, according to the following equation.

$$V_{OUT} = V_{ADJ/EN} \times \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100 times the FB pin current (I_{FB}). I_{FB} is listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation.

$$R_1 + R_2 \leq \frac{V_{OUT}}{(I_{FB} \times 100)} \quad (6)$$

7.2.2.3 Feedforward Capacitor

A feedforward capacitor (C_{FF}) is recommended to be connected between the OUT pin and the FB pin. C_{FF} improves transient, noise, and PSRR performance. However, the LDO start-up time increases with higher C_{FF} capacitance. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

As shown in Figure 7-2, poor layout practices and using long traces at the FB pin result in the formation of a parasitic capacitor (C_{FB}).

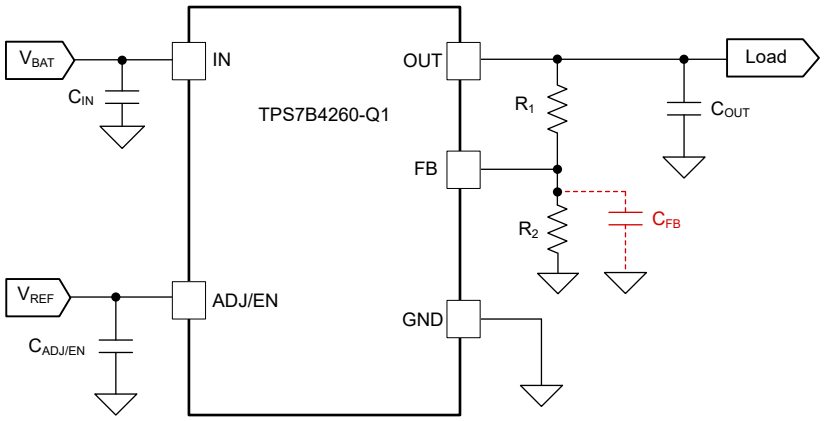


Figure 7-2. Parasitic Capacitor on the FB Pin

C_{FB} in combination with feedback resistors R_1 and R_2, potentially results in an uncompensated pole forming in the transfer function of the loop gain. A C_{FB} value as small as 20pF potentially causes the parasitic pole frequency, given by Equation 7, to fall within the bandwidth of the LDO.

$$f_P = \frac{1}{(2 \times \pi \times C_{FB} \times (R_1 \parallel R_2))} \quad (7)$$

Adding a feedforward capacitor (C_{FF}), as shown in Figure 7-3, creates a zero in the loop gain transfer function. This zero compensates for the parasitic pole created by C_{FB}. Equation 8 and Equation 9 calculate the pole and zero frequencies.

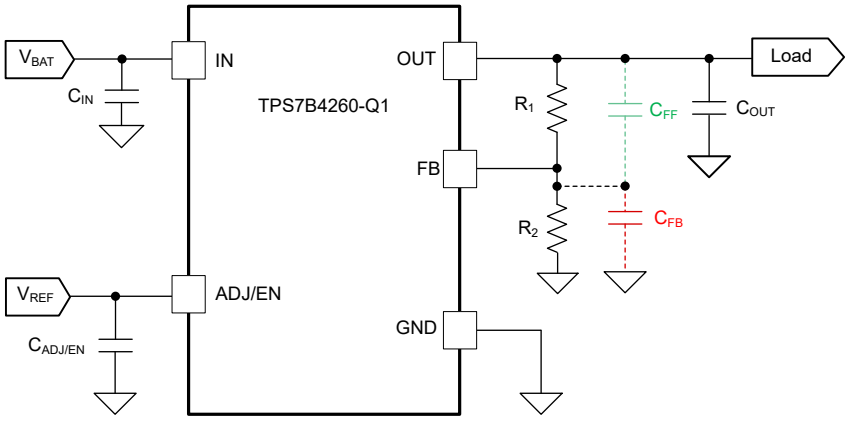


Figure 7-3. Feedforward Capacitor Helps Mitigate the Impact of the Parasitic Feedback Capacitor

$$f_P = \frac{1}{(2 \times \pi \times (R_1 \parallel R_2) \times (C_{FF} + C_{FB}))} \quad (8)$$

$$f_Z = \frac{1}{(2 \times \pi \times C_{FF} \times R_1)} \quad (9)$$

Selecting a C_{FF} value that makes f_P equal to f_Z, results in pole-zero cancellation. This C_{FF} value depends on the values of C_{FB} and the feedback resistors used in the application. Alternatively, if the feedforward capacitor is selected so that $C_{FF} \gg C_{FB}$, then the pole and zero frequencies given by Equation 8 and Equation 9 are related as:

$$\frac{f_p}{f_z} \approx \left(1 + \frac{R_1}{R_2}\right) = \frac{V_{OUT}}{V_{ADJ/EN}} \quad (10)$$

In most applications, particularly where a 3.3V or 5V V_{OUT} is generated, this ratio is not very large. Thus, implying that the frequencies are located close to each other and therefore the parasitic pole is compensated. A C_{FF} value in the range of 100pF ≤ C_{FF} ≤ 10nF typically helps prevent instability caused by C_{FB}, even for larger V_{OUT} values.

Following good layout practices helps minimize the parasitic feedback pin capacitance to values that prevent the resulting parasitic pole from causing instability. See the *Layout Guidelines* section and the *TRKRLDOEVM-119 General-Purpose Tracker LDO Evaluation Module* user guide.

7.2.3 Application Curves

The following images illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness for the HSOIC-8 (DDA) package. These plots are generated with a 101.6mm × 101.6mm × 1.6mm printed circuit board (PCB) of two and four layers. For the 2-layer board, the bottom layer is a ground plane of constant size, and the top layer copper is connected to GND and varied. For the 4-layer board, the second layer is a ground plane of constant size, the third layer is a power plane of constant size. The top and bottom layers copper fills are connected to GND and varied at the same rate. For the 4-layer board, inner planes use 1oz copper thickness. Outer layers are simulated with both 1oz and 2oz copper thickness. A 3 × 3 array of thermal vias with a 300µm drill diameter and 25µm copper plating is located underneath the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. *PowerPAD™ Thermally Enhanced Package* application note discusses the impact that thermal vias have on thermal performance.

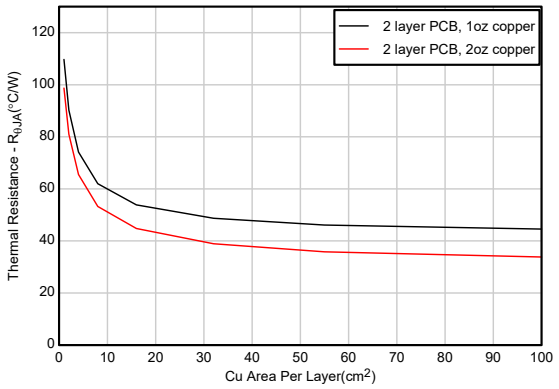


Figure 7-4. $R_{\theta JA}$ vs Copper Area (HSOIC-8 Package, 2-Layer PCB)

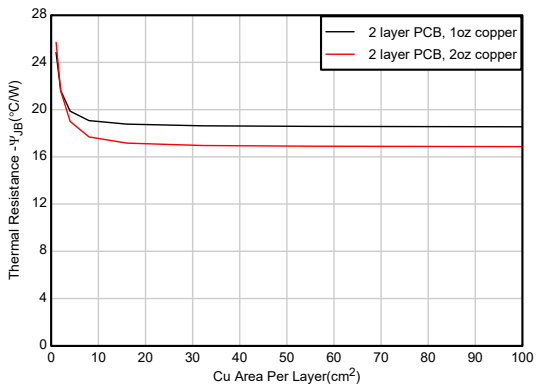


Figure 7-5. ψ_{JB} vs Copper Area (HSOIC-8 Package, 2-Layer PCB)

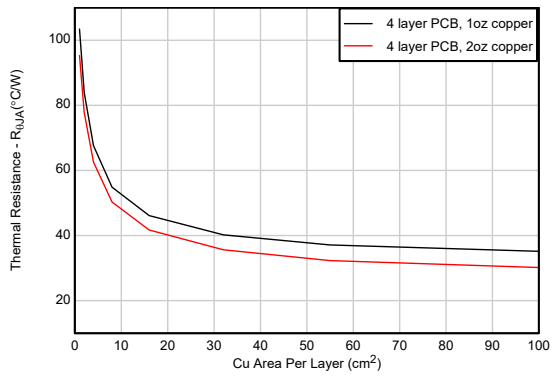


Figure 7-6. $R_{\theta JA}$ vs Copper Area (HSOIC-8 Package, 4-Layer PCB)

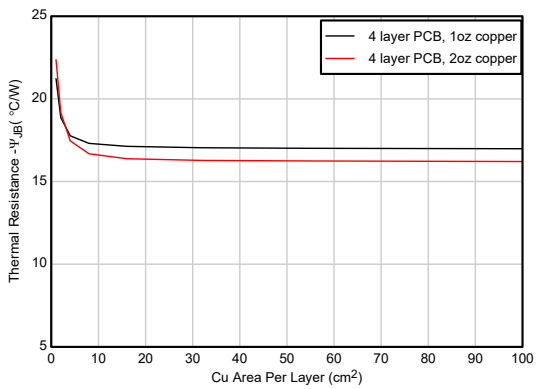


Figure 7-7. ψ_{JB} vs Copper Area (HSOIC-8 Package, 4-Layer PCB)

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3V to 40V.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board. Place these components as near as practical to the respective LDO pin connections. Place ground return connections of the input and output capacitor, as close as possible to the LDO ground pin. Use a wide, component-side, copper surface to make the connections between the two. Using vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. Use a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane helps improve accuracy of the output voltage and provide shielding from noise. This plane behaves

similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4260-Q1 are available at the end of this document and at www.ti.com.

7.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}. Connect each ground plane only at the GND pin of the device. In addition, directly connect the ground connection for the output capacitor to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR to maximize performance and provide stability. Place each capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any capacitors on the opposite side of the PCB from where the regulator is installed. Using vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces potentially also cause instability.

If possible, and to provide the maximum performance denoted in this document, use the same layout pattern used for the TPS7B4260-Q1 evaluation board. This evaluation board is available at www.ti.com.

7.4.1.3 Power Dissipation and Thermal Considerations

Equation 11 calculates the device power dissipation.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \quad (11)$$

where:

- P_D = Continuous power dissipation
- I_{OUT} = Output current
- V_{IN} = Input voltage
- V_{OUT} = Output voltage
- I_Q = Quiescent current

Because I_Q is much less than I_{OUT}, ignore the term $I_Q \times V_{IN}$ in Equation 11.

Calculate the junction temperature (T_J) with Equation 12 for a device under operation at a given ambient air temperature (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (12)$$

where:

- $R_{\theta JA}$ = Junction-to-junction-ambient air thermal impedance

Equation 13 calculates a rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (13)$$

The maximum ambient air temperature (T_{AMAX}) at which the device operates is calculated with Equation 14 for a given maximum junction temperature (T_{JMAX}).

$$T_{AMAX} = T_{JMAX} - (R_{\theta JA} \times P_D) \quad (14)$$

7.4.1.4 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design. $R_{\theta JA}$ therefore varies according to the total copper area, copper weight, and location of the planes. The *Thermal Information* table gives the $R_{\theta JA}$ value. $R_{\theta JA}$ is determined by the JEDEC

standard (Figure 7-8), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the $R_{\theta JCbot}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JCbot}$ is the package junction-to-case (bottom) thermal resistance, as given in the *Thermal Information* table.

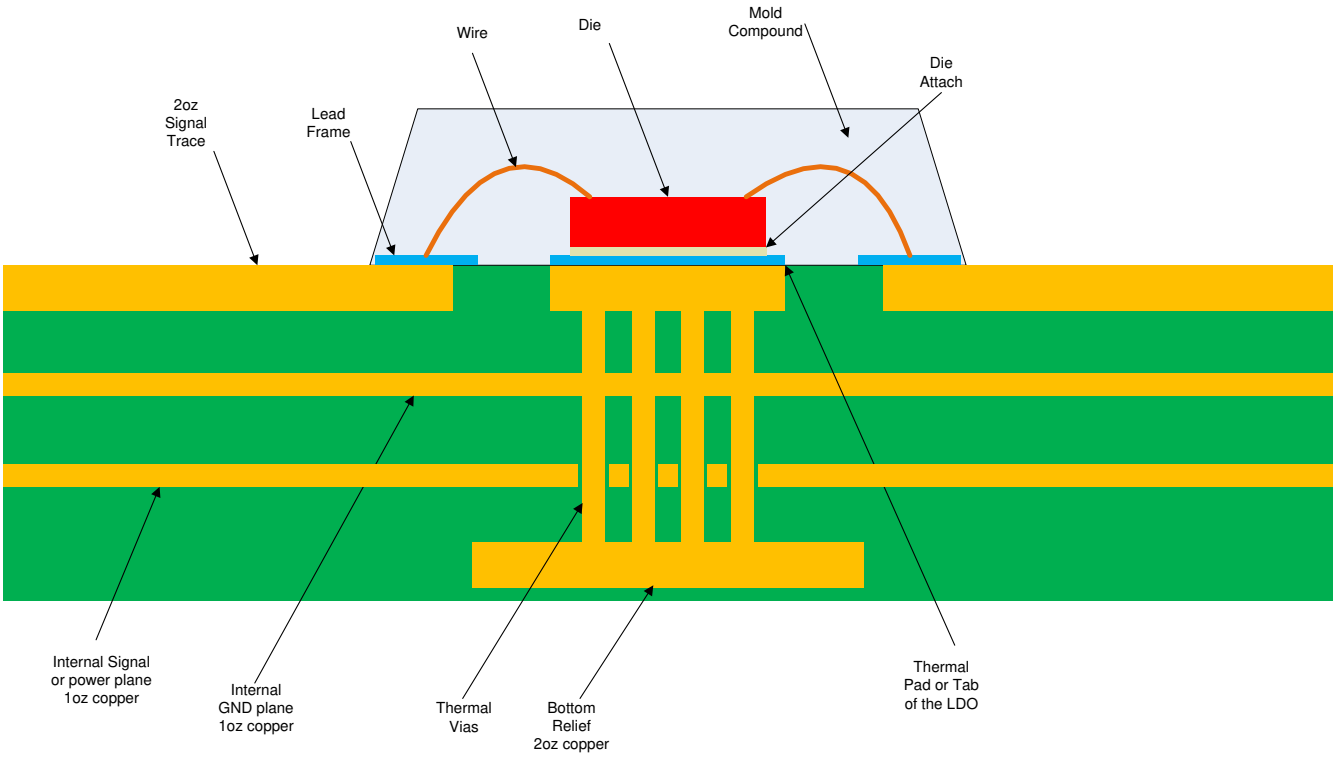


Figure 7-8. JEDEC Standard 2s2p PCB

7.4.2 Layout Example

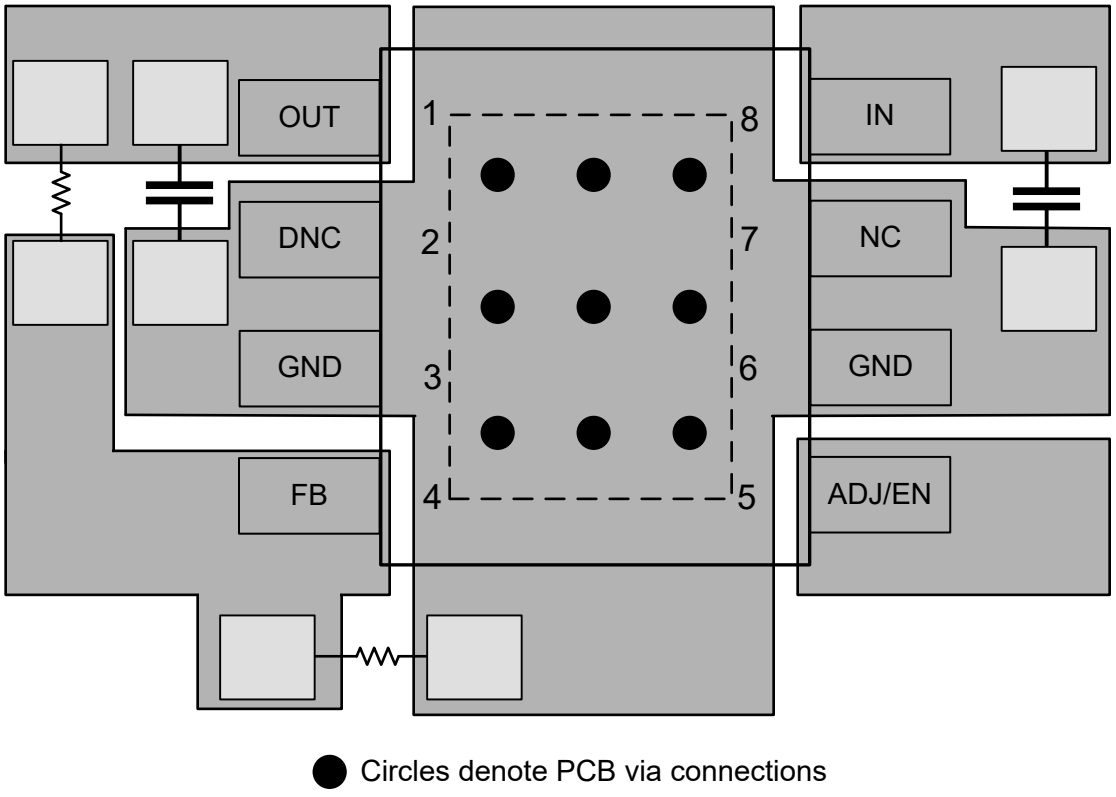


Figure 7-9. Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT(1)	V_{OUT}
TPS7B4260**QDDARQ1**	In the HSOIC (DDA) package: **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **R** is the packaging quantity. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TPS7B84-Q1 150mA, 40V, Adjustable, Low-Dropout Regulator* data sheet
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note
- Texas Instruments, *TRKRLDOEVM-119 General-Purpose Tracker LDO Evaluation Module* user guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2025) to Revision B (June 2025)	Page
• Changed figures in *Application Curves* section	24

Changes from Revision * (January 2025) to Revision A (March 2025)	Page
• Changed document status from *Advance Information* to *Production Data*	1

10 Mechanical, Packaging, and Orderable Information

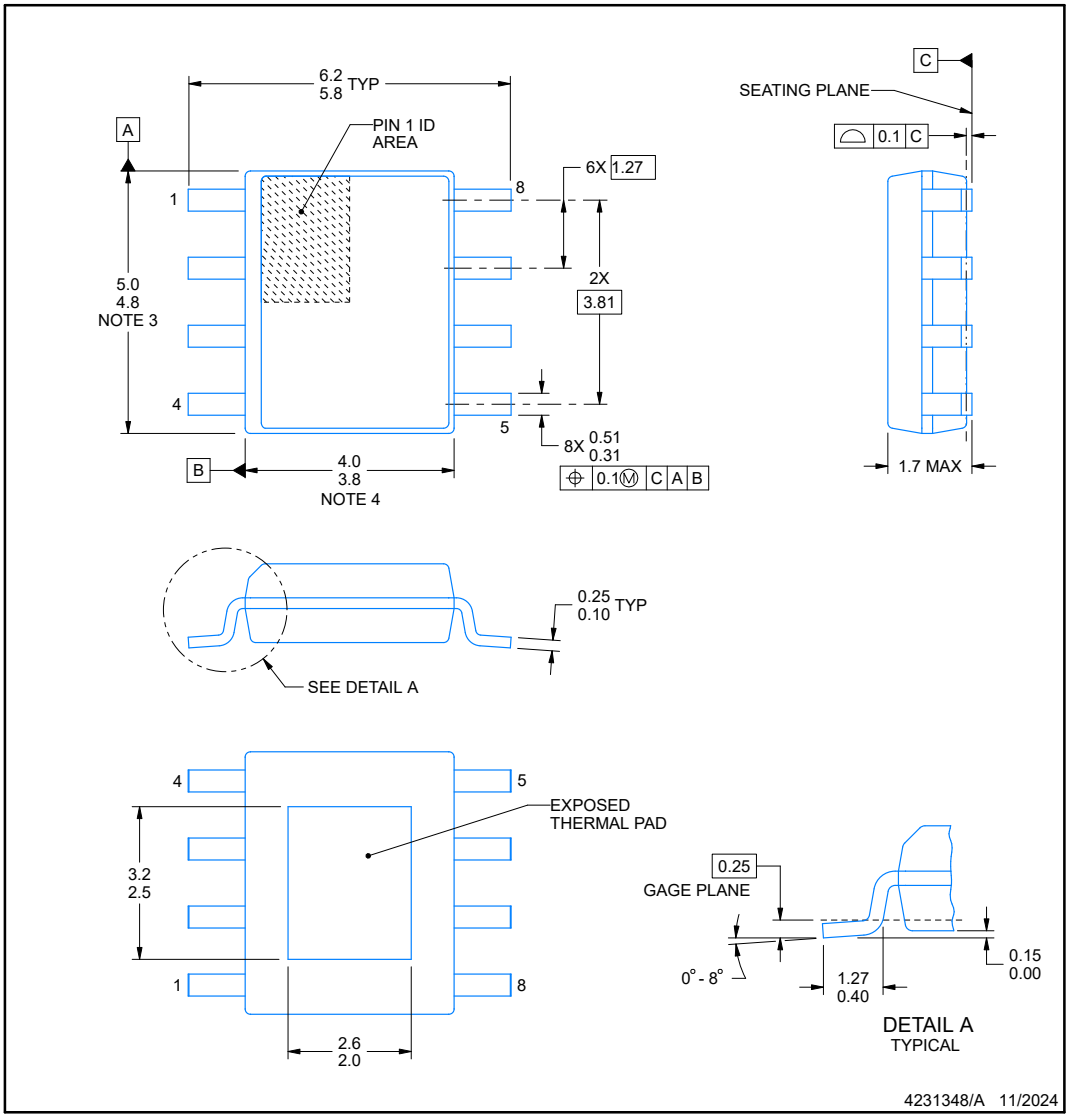
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data

PACKAGE OUTLINE

DDA0008J-C02 **PowerPAD™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

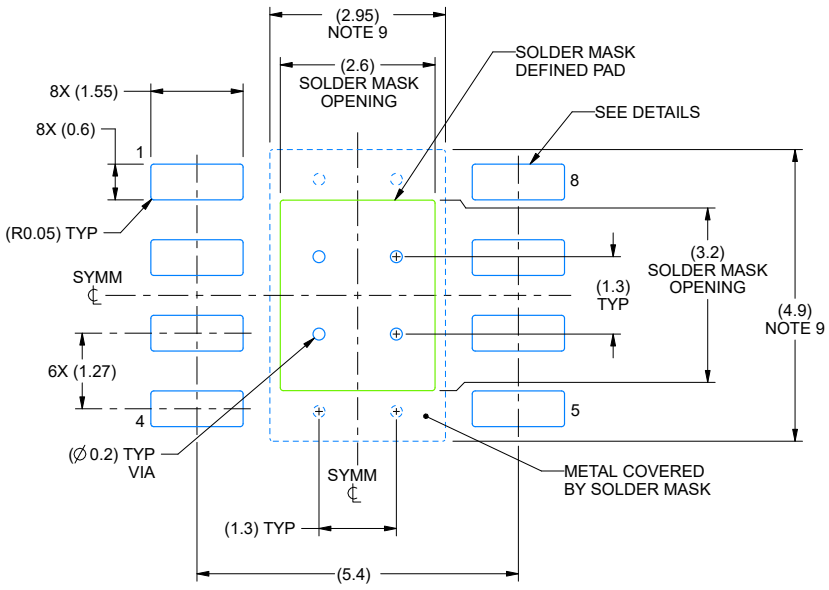
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

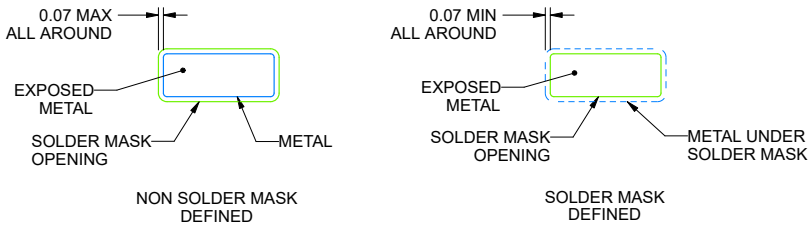
EXAMPLE BOARD LAYOUT

DDA0008J-C02 — **PowerPAD ™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS

4231348/A 11/2024

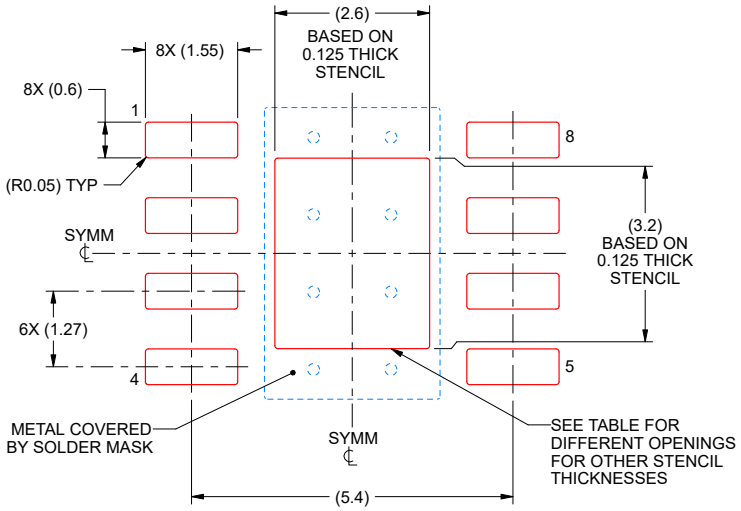
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDA0008J-C02 **PowerPAD ™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.58
0.125	2.6 X 3.2 (SHOWN)
0.150	2.37 X 2.92
0.175	2.20 X 2.70

4231348/A 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B4260QDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B4260F
TPS7B4260QDDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B4260F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

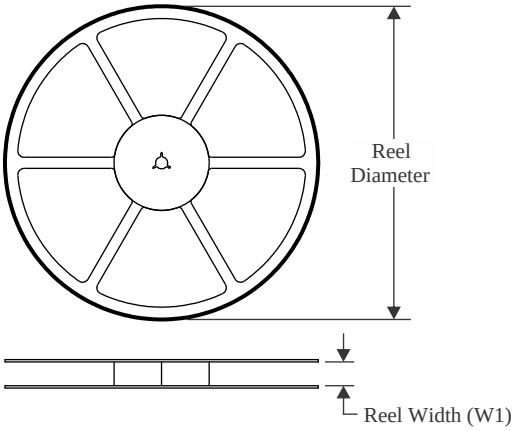
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

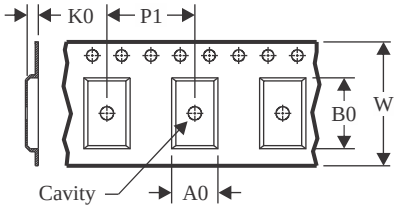
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

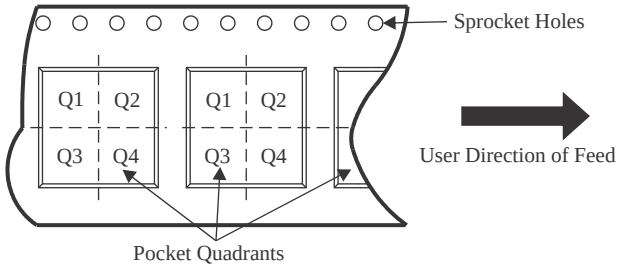


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

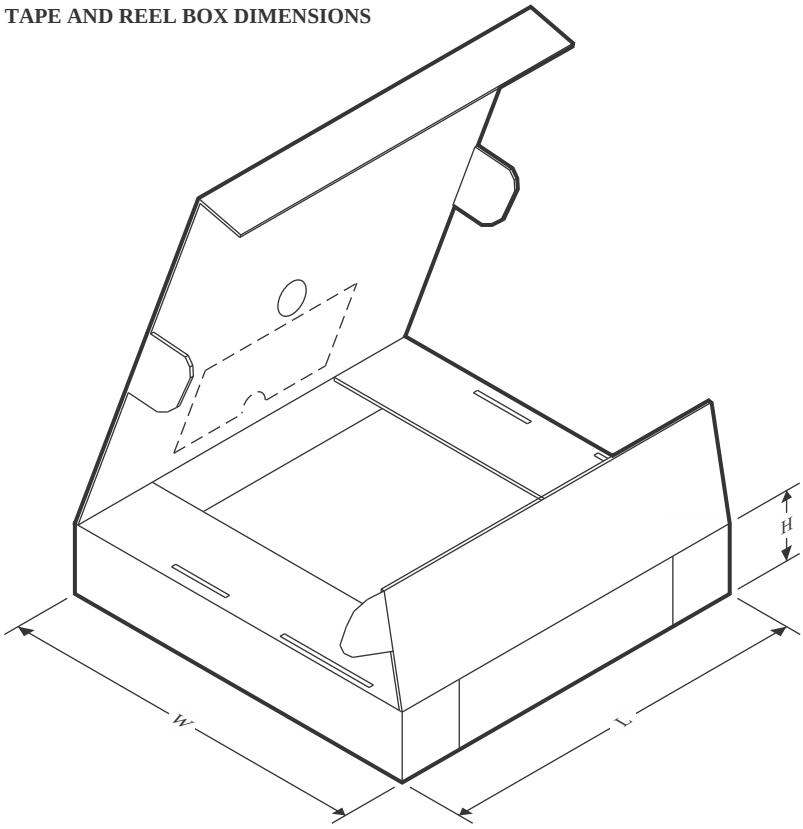
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4260QDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

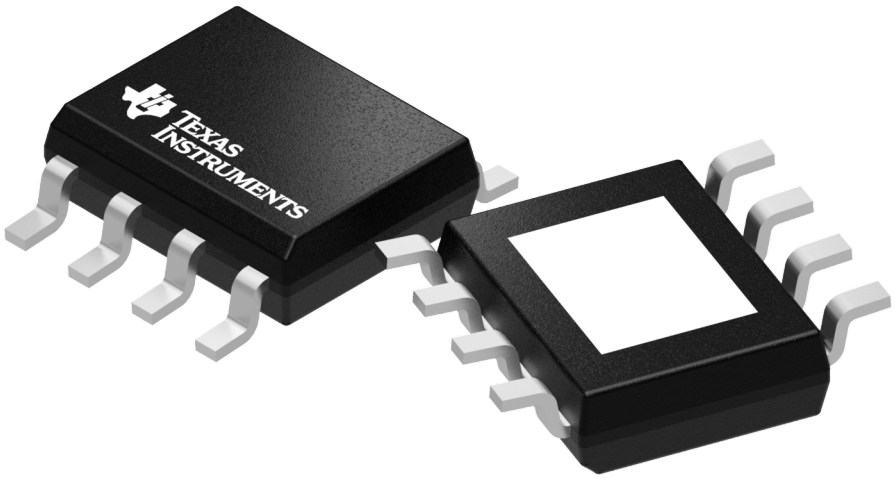


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4260QDDARQ1	SO PowerPAD	DDA	8	2500	340.5	338.1	20.6

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



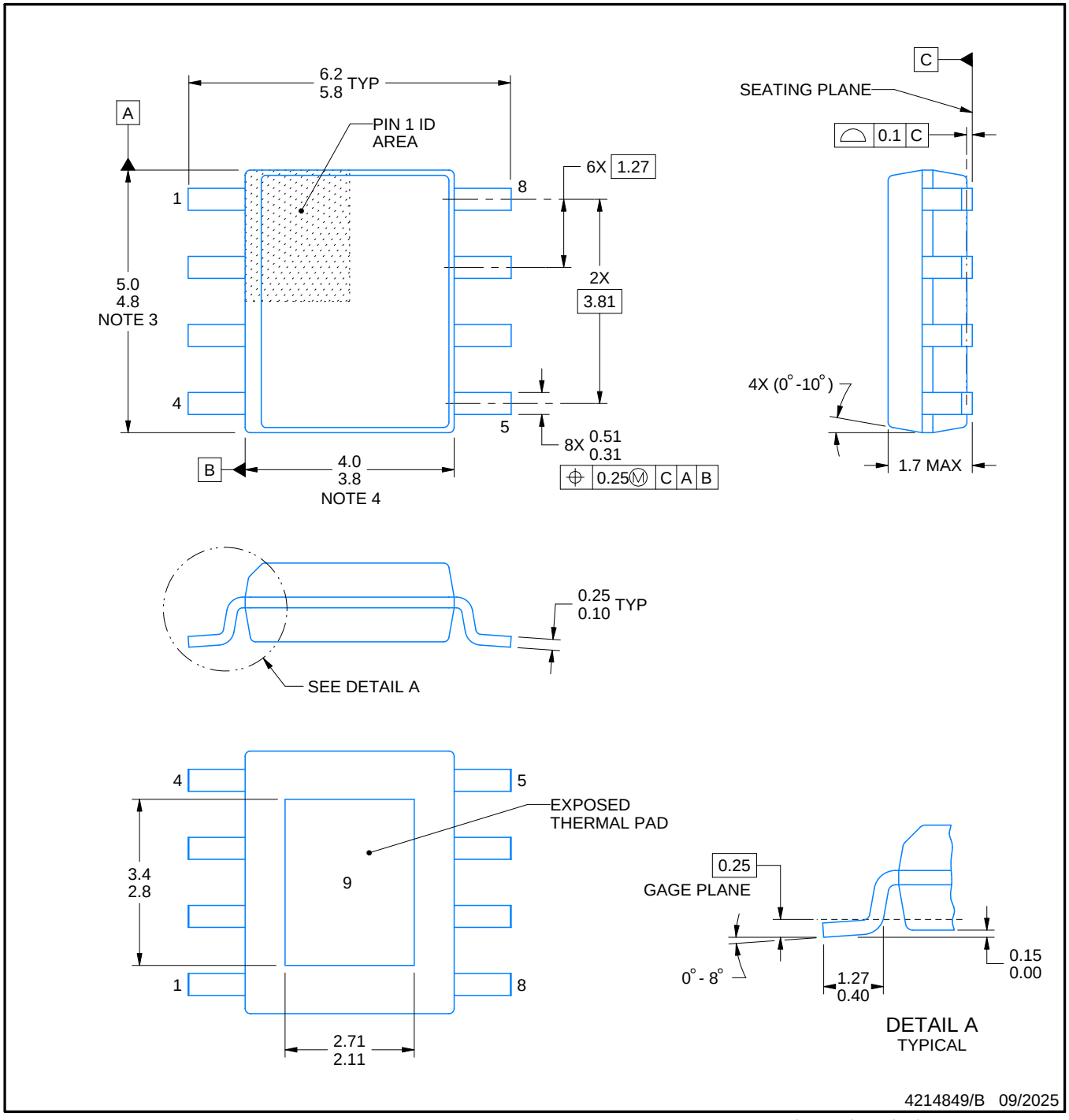
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

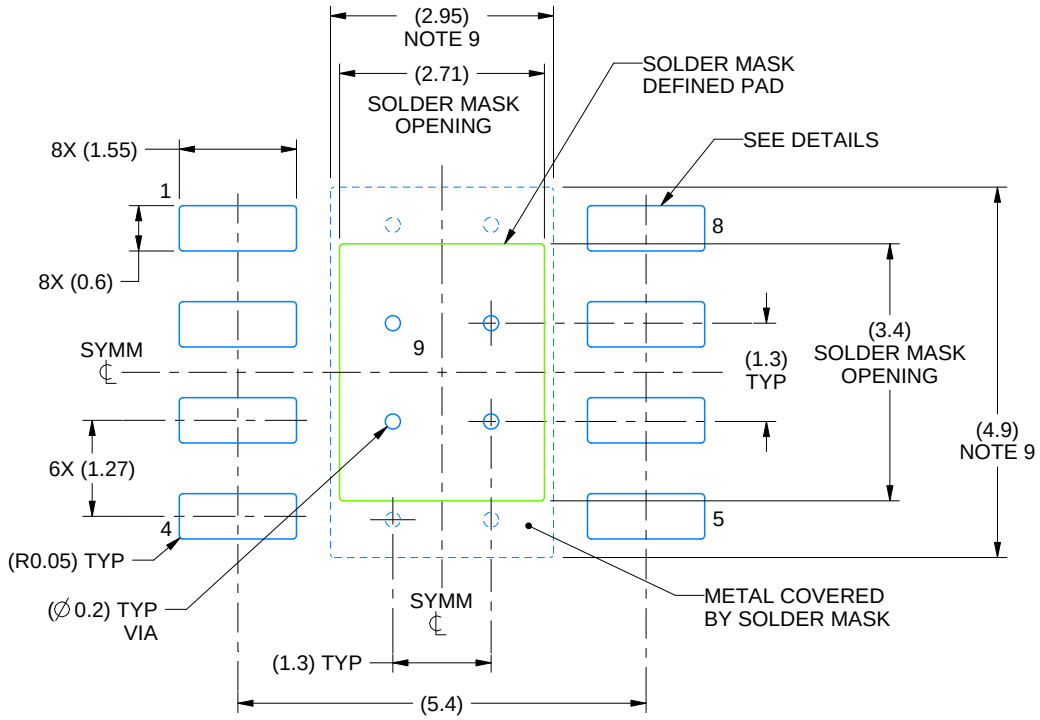
PLASTIC SMALL OUTLINE



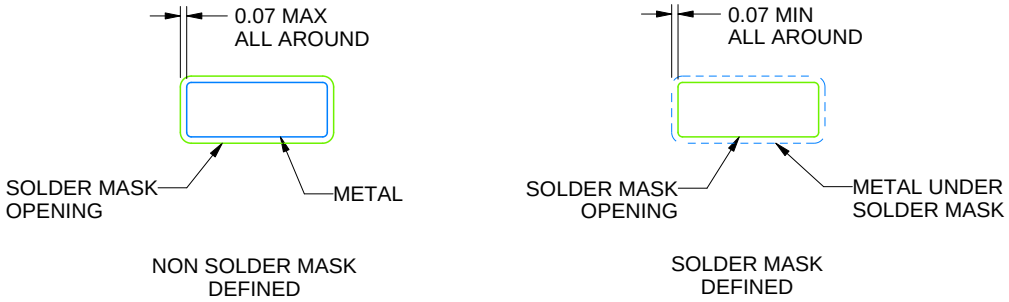
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

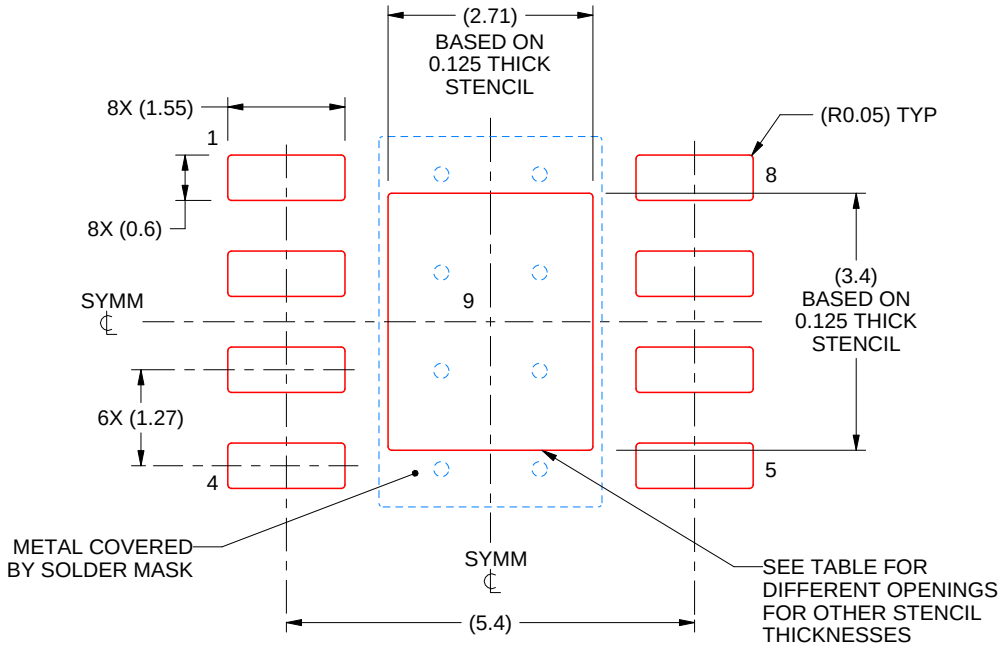
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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