



TPS7B4253-Q1 300-mA 40-V Low-Dropout Voltage-Tracking LDO With 4-mV Tracking Tolerance

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: -40°C to $+125^{\circ}\text{C}$ Ambient Operating Temperature Range
 - Device HBM ESD Classification Level 3A
 - Device CDM ESD Classification Level C6
- -40 to 45-V Wide Input-Voltage Range (Maximum)
- Output Voltage Adjusts Down to:
 - 1.5 to 40 V (HTSSOP)
 - 2 to 40 V (SO PowerPAD™)
- 300-mA Output Current Capability
- Very-Low Output Tracking Tolerance, $\pm 4\text{ mV}$
- 320-mV Low Dropout Voltage when $I_{\text{OUT}} = 200\text{ mA}$
- Separate Pins for Enable and Tracking Inputs (HTSSOP only)
- Low Quiescent Current (I_{Q}):
 - $< 4\text{ }\mu\text{A}$ when $\text{EN} = \text{LOW}$
 - $60\text{ }\mu\text{A}$ (Typical) at Light Loads
- Extremely Wide ESR Range.
 - Stable With $10\text{- to }500\text{-}\mu\text{F}$ Ceramic Output Capacitor, ESR $1\text{ m}\Omega$ to $20\text{ }\Omega$
- Reverse Polarity Protection
- Current-Limit and Thermal-Shutdown Protection
- Output Short-Circuit Proof to Ground and Supply
- Inductive Clamp at OUT Pin
- Available in the Following Packages:
 - 8-Pin SO PowerPAD Package
 - 20-Pin HTSSOP Package

2 Applications

- Off-Board Sensor Supply
- High-Precision Voltage Tracking
- Power Switch for Off-Board Load

3 Description

For automotive off-board sensors and small current off-board modules, the power supply is through a long cable from the main board. In such cases, protection is required in the power devices for the off-board loads to prevent the onboard components from damage during a short to GND or short to battery caused by a broken cable. Off-board sensors require consistent power supply as onboard components to secure high accuracy of data acquisition.

The TPS7B4253-Q1 device is designed for automotive applications with a 45-V load dump. The device can either be used as one tracking low-dropout (LDO) regulator or voltage tracker to build one closed power loop for off-board sensors with an onboard main supply. The output of the device is accurately regulated by a reference voltage at the ADJ pin.

To provide an accurate power supply to the off-board modules, the device offers a 4-mV ultralow tracking tolerance between the ADJ and FB pins across temperature. The back-to-back PMOS topology eliminates the need for an external diode under reverse polarity condition. The TPS7B4253-Q1 device also includes thermal shutdown, inductive clamp, overload, and short-to-battery protection to prevent damage to onboard components during extreme conditions.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7B4253-Q1	SO PowerPAD (8)	$4.89\text{ mm} \times 3.90\text{ mm}$
	HTSSOP (20)	$6.50\text{ mm} \times 4.40\text{ mm}$

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

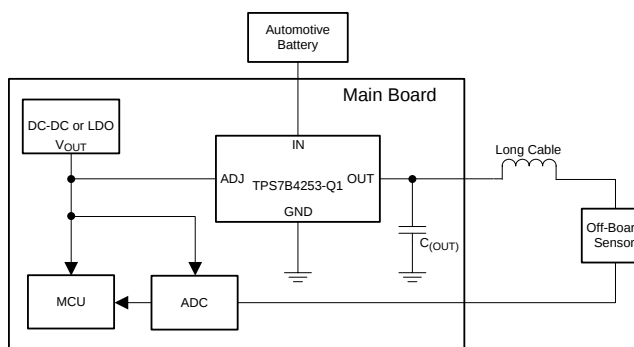


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

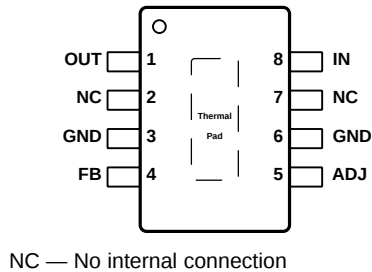
Changes from Revision B (January 2016) to Revision C	Page
• Changed the following parameters in the <i>Recommended Operating Conditions</i> table to show values for HTSSOP and SO PowerPAD packages: V_{ADJ} , V_{FB} , and V_{OUT}	4
• Corrected the <i>Functional Block Diagram</i>	10
• Added the HTSSOP package as the example for the <i>Application With Output Voltage Equal to the Reference Voltage</i> section	16
• Corrected the <i>Output Voltage Equals the Reference Voltage</i> figure	16
• Added the <i>Receiving Notification of Documentation Updates</i> section	22

Changes from Revision A (August 2015) to Revision B	Page
• Changed the note for the reference voltage minus the input voltage parameter in the <i>Absolute Maximum Ratings</i> table	4
• Added values for the SO PowerPAD package for the adjust signal valid parameters in the <i>Electrical Characteristics</i> table	5
• Changed the test condition for the adjust high signal valid parameter in the <i>Electrical Characteristics</i> table	5

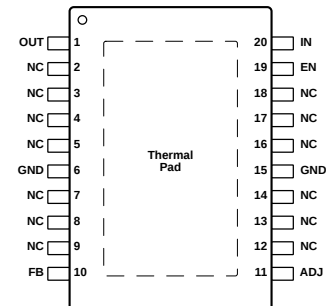
Changes from Original (January 2015) to Revision A	Page
• Changed the device status from <i>Product Preview</i> to <i>Production Data</i>	1

5 Pin Configuration and Functions

DDA PowerPAD™ Package
8-Pin SO With External Thermal Pad
Top View



PWP Package
20-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	SO PowerPAD	HTSSOP		
ADJ	5	11	I	Connect the reference to this pin. A low signal disables the device and a high signal enables the device. The reference voltage can be connected directly or by a voltage divider for lower output voltages. To compensate for line influences, connect a capacitor close to the device pins.
EN	—	19	I	This pin is the enable pin. The device goes to the STANDBY state when the enable pin goes lower than the threshold value.
FB	4	10	I	This pin is the feedback pin which can connect to the external resistor divider to select the output voltage.
GND	3	6	G	Ground reference
	6	15		
IN	8	20	I	This pin is the device supply. To compensate for line influences, connect a capacitor close to the device pins.
NC	2	2	NC	Not connected
		3		
		4		
		5		
		7		
		8		
	7	9		
		12		
		13		
		14		
	16			
	17			
	18			
OUT	1	1	O	Block to GND with a capacitor close to the device pins with respect to the capacitance and ESR requirements listed in the Output Capacitor section.
Exposed thermal pad			—	Connect the thermal pad to the GND pin or leave it floating.

(1) I = input, O = output, G = ground, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Unregulated input voltage	IN ⁽²⁾⁽³⁾	–40	45	V
Enable input voltage	Enable input voltage ⁽²⁾⁽³⁾	–40	45	V
Regulated output voltage	Regulated output voltage ⁽²⁾⁽⁴⁾	–1	45	V
Voltage difference between the input and output	IN – OUT	–40	45	V
Reference voltage	ADJ ⁽²⁾⁽³⁾	–0.3	45	V
Feedback input voltage for the tracker	FB ⁽²⁾⁽³⁾	–1	45	V
Reference voltage minus the input voltage	ADJ – IN ⁽⁵⁾		18	V
Operating junction temperature, T _J		–40	150	°C
Storage temperature, T _{stg}		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND pin.
- (3) Absolute maximum voltage.
- (4) An internal diode is connected between the OUT and GND pins with 600-mA DC current capability for inductive clamp protection.
- (5) When the (ADJ – IN) voltage is higher than 18 V, the (ADJ – OUT) voltage should maintain lower than 18 V, otherwise the device can be damaged.

6.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	NC pins	±2000	kV
			All pins except for NC pins	±4000	kV
		Charged device model (CDM), per AEC Q100-011		±1000	kV

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{IN}	Unregulated input voltage ⁽²⁾		4	40	V
V _{EN}	Enable input voltage		0	40	V
V _{ADJ}	Adjust and enable input voltage	HTSSOP package	1.5	18	V
		SO PowerPAD package	2	18	
V _{FB}	Feedback input voltage for the tracker	HTSSOP package	1.5	18	V
		SO PowerPAD package	2	18	
V _{OUT}	Output voltage	HTSSOP package	1.5	40	V
		SO PowerPAD package	2	40	
C _(OUT)	Output capacitor requirements ⁽³⁾		10	500	μF
	Output ESR requirements ⁽⁴⁾		0.001	20	Ω
T _J	Operating junction temperature range		–40	150	°C

- (1) Within the functional range the device operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related *Electrical Characteristics* table.
- (2) V_{IN} > V_{ADJ} + V_(DROPOUT)
- (3) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%, when a resistor divider is connected between the OUT and FB pins (the output voltage is higher than reference voltage), a 47-nF feedforward capacitor is required to be connected between the OUT and FB pins for loop stability, and the ESR range of the output capacitor is required to be from 0.001 to 10 Ω.
- (4) Relevant ESR value at f = 10 kHz

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7B4253-Q1		UNIT
		DDA (SO PowerPAD)	PWP (HTSSOP)	
		8 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	45.4	45.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.1	29.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	27	24.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	8.2	1.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	26.9	24.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	6.4	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

V_{IN} = 13.5 V, V_{ADJ} ≥ 1.5 V for HTSSOP, V_{ADJ} ≥ 2 V for SO PowerPAD, V_{EN} ≥ 2 V, T_J = –40°C to 150°C unless otherwise stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{I(UVLO)}	IN undervoltage detection			3.65	V
	V _{IN} falling			2.8	V
ΔVO	Output voltage tracking accuracy ⁽¹⁾ I _{OUT} = 100 μA to 300 mA, V _{IN} = 4 to 40 V V _{ADJ} < V _{IN} – 1 V 1.5 V < V _{ADJ} < 18 V for HTSSOP 2 V < V _{ADJ} < 18 V for SO PowerPAD	–4		4	mV
ΔV _{O(ΔIO)}	Load regulation steady-state I _{OUT} = 0.1 to 300 mA, V _{ADJ} = 5 V			4	mV
ΔV _{O(ΔVI)}	Line regulation steady-state I _{OUT} = 10 mA, V _{IN} = 6 to 40 V, V _{ADJ} = 5 V			4	mV
PSRR	Power supply ripple rejection f _{rip} = 100 Hz, V _{rip} = 0.5 V _{PP} , C _(OUT) = 10 μF, I _{OUT} = 100 mA		70		dB
V _(DROPOUT)	Dropout voltage (V _(DROPOUT) = V _{IN} – V _{OUT}) I _{OUT} = 200 mA, V _{IN} = V _{ADJ} ≥ 4 V ⁽²⁾		320	520	mV
I _{O(lim)}	Output current limitation V _{ADJ} = 5 V, OUT short to GND	301	450	520	mA
I _{R(IN)}	Reverse current at IN V _{IN} = 0 V, V _{OUT} = 40 V, V _{ADJ} = 5 V	–2		0	μA
I _{R(IN)}	Reverse current at negative IN V _{IN} = –40 V, V _{OUT} = 0 V, V _{ADJ} = 5 V	–10		0	μA
T _{SD}	Thermal shutdown temperature T _J increases because of power dissipation generated by the IC		175		°C
T _{SD_hys}	Thermal shutdown hysteresis		15		°C
I _Q	Current consumption 4 V ≤ V _{IN} ≤ 40 V, V _{ADJ} = 0 V, V _{EN} = 0 V 4 V ≤ V _{IN} ≤ 40 V, V _{EN} ≥ 2 V, V _{ADJ} < 0.8 V 4 V ≤ V _{IN} ≤ 40 V, I _{OUT} < 100 μA, V _{ADJ} = 5 V 4 V ≤ V _{IN} ≤ 40 V, I _{OUT} < 300 mA, V _{ADJ} = 5V		2	4	μA
			7	18	
			60	100	
			350	400	
I _{Q(DROPOUT)}	Current consumption in dropout region V _{IN} = V _{ADJ} = 5 V, I _{OUT} = 100 μA		70	140	μA
I _{I(ADJ)}	Adjust input current V _{ADJ} = V _{FB} = 5 V	HTSSOP package		0.5	μA
		SO PowerPAD package		5.5	
V _(ADJ_LOW)	Adjust low signal valid V _{OUT} = 0 V	HTSSOP package	0	0.8	V
		SO PowerPAD package	0	0.7	
V _(ADJ_HIGH)	Adjust high signal valid V _{OUT} – V _{ADJ} < 4 mV	HTSSOP package	1.5	18	V
		SO PowerPAD package	2	18	
V _(EN_LOW)	Enable low signal valid V _{OUT} = 0 V		0	0.7	V
V _(EN_HIGH)	Enable high Signal Valid OUT settled		2	40	V
I _{EN}	Enable pulldown current 2V < V _{EN} < 40 V			5	μA
I _{FB}	FB bias current V _{ADJ} = V _{FB} = 5 V			0.5	μA

(1) The tracking accuracy is specified when the FB pin is directly connected to the OUT pin which means V_{ADJ} = V_{OUT}, external resistor divider variance is not included.

(2) Measured when the output voltage, V_{OUT} has dropped 10 mV from the nominal value.

6.6 Typical Characteristics

$V_{IN} = 14\text{ V}$, $V_{ADJ} = 5\text{ V}$, $V_{FB} = V_{OUT}$, unless otherwise specified

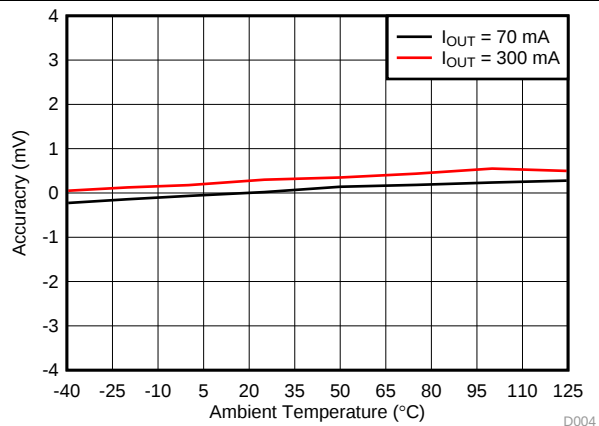


Figure 1. Tracking Accuracy vs Ambient Temperature

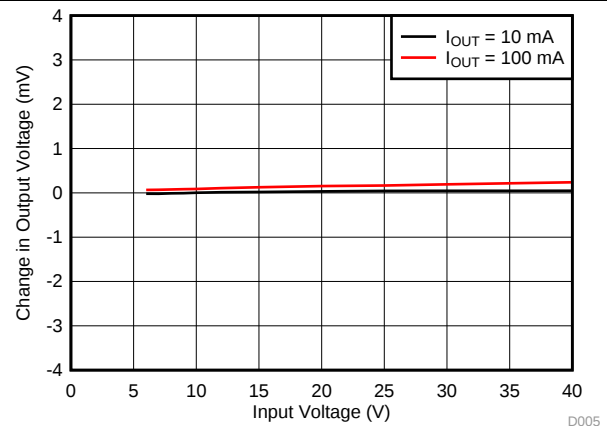


Figure 2. Line Regulation

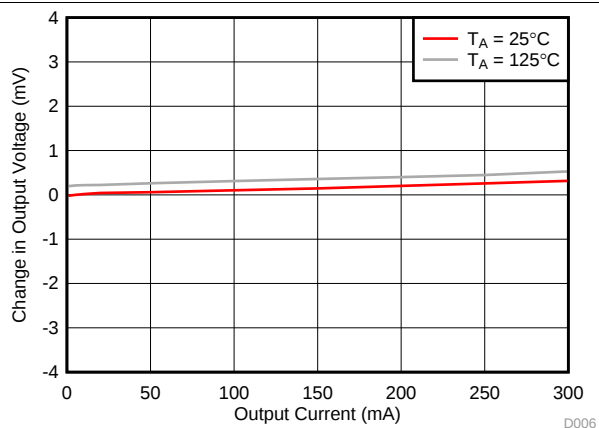


Figure 3. Load Regulation

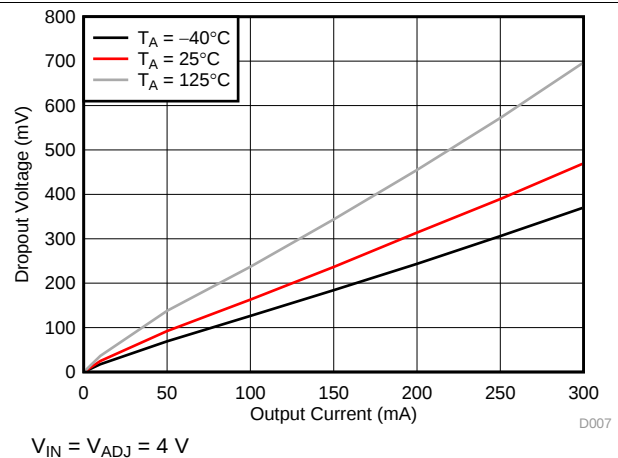


Figure 4. Dropout Voltage vs Output Current

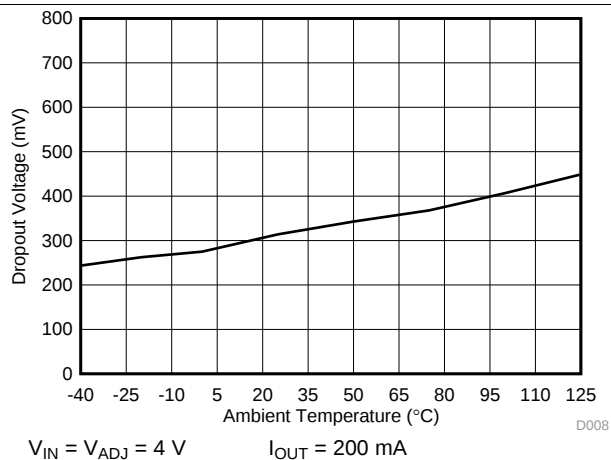


Figure 5. Dropout Voltage vs Ambient Temperature

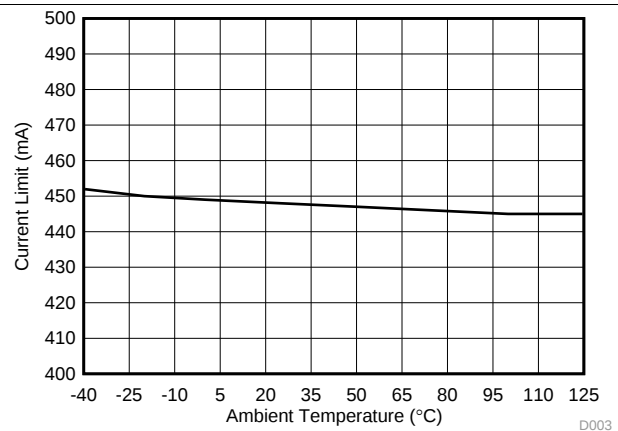


Figure 6. Current Limit ($I_{O(lim)}$) vs Ambient Temperature

Typical Characteristics (continued)

$V_{IN} = 14\text{ V}$, $V_{ADJ} = 5\text{ V}$, $V_{FB} = V_{OUT}$, unless otherwise specified

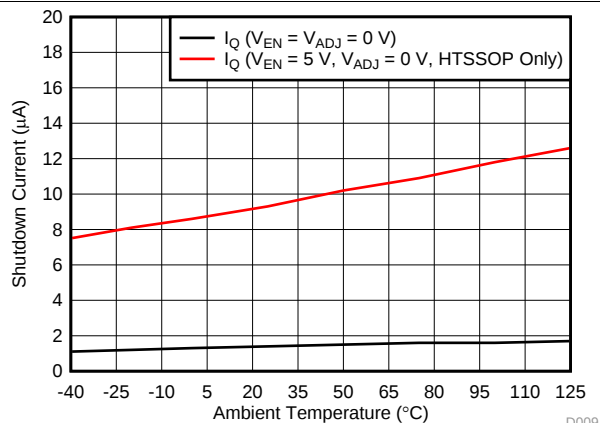


Figure 7. Shutdown Current vs Ambient Temperature

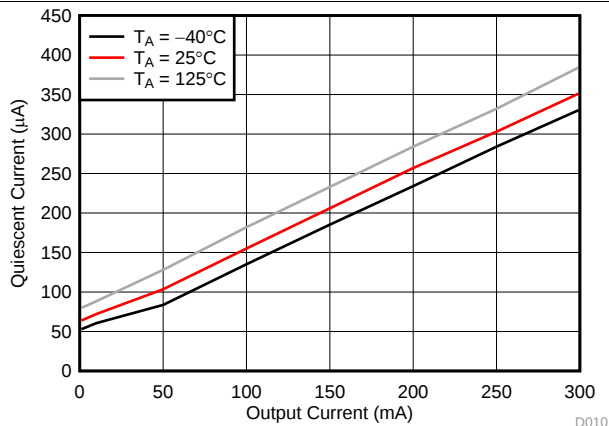


Figure 8. Quiescent Current vs Output Current

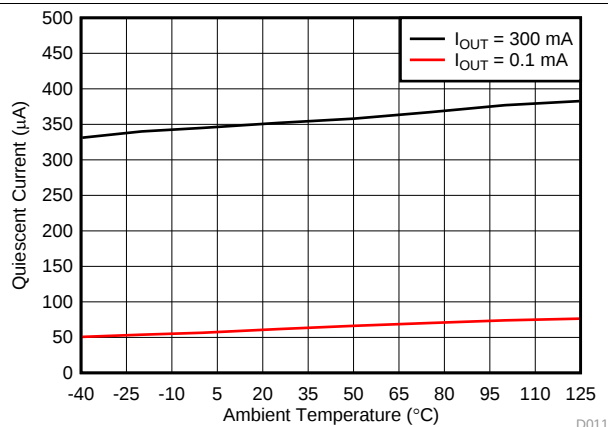
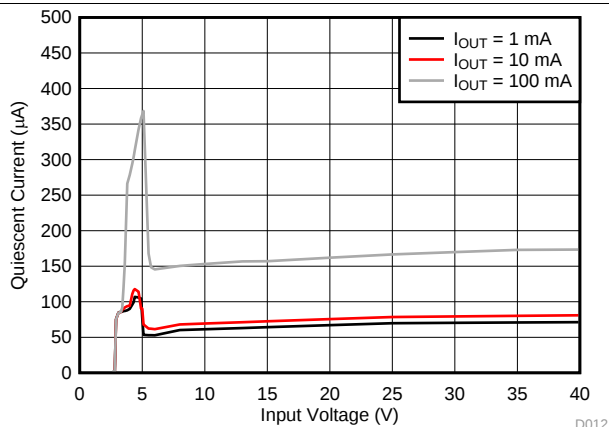


Figure 9. Quiescent Current vs Ambient Temperature



$V_{ADJ} = V_{EN} = 5\text{ V}$

Figure 10. Quiescent Current vs Input Voltage

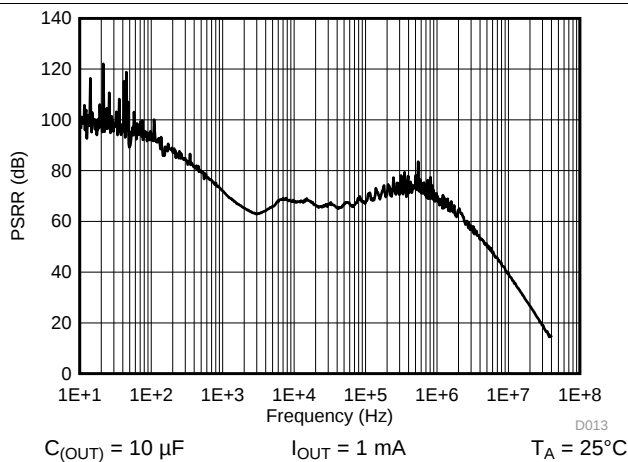


Figure 11. PSRR

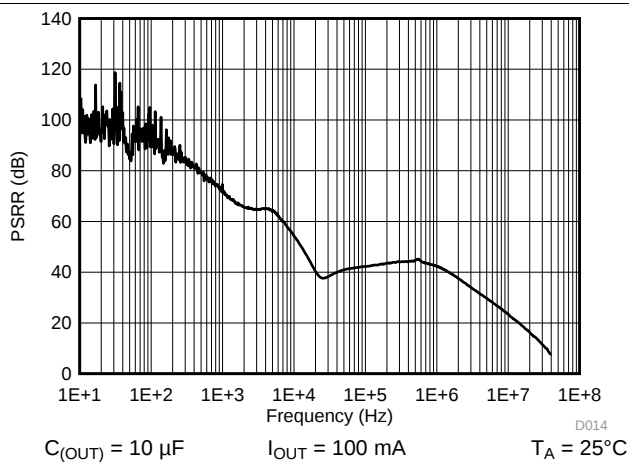


Figure 12. PSRR

Typical Characteristics (continued)

$V_{IN} = 14\text{ V}$, $V_{ADJ} = 5\text{ V}$, $V_{FB} = V_{OUT}$, unless otherwise specified

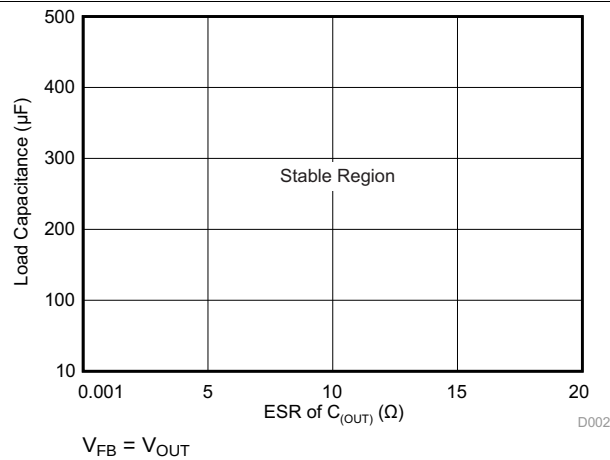


Figure 13. ESR Stability vs Load Capacitance

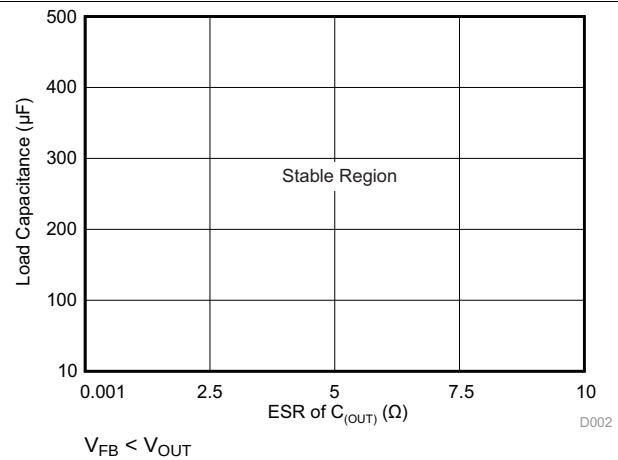


Figure 14. ESR Stability vs Load Capacitance

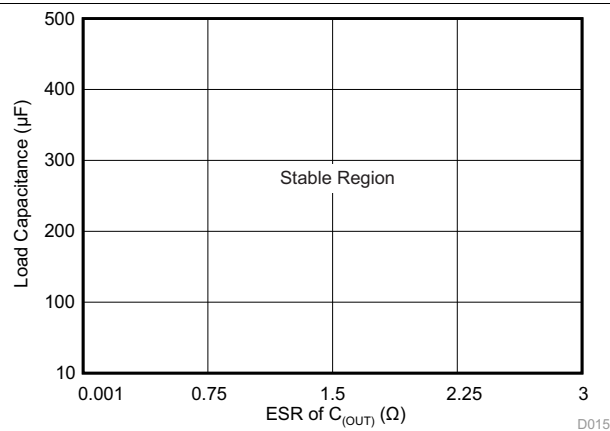


Figure 15. ESR Stability vs Load Capacitance (Multiple Output Capacitors)

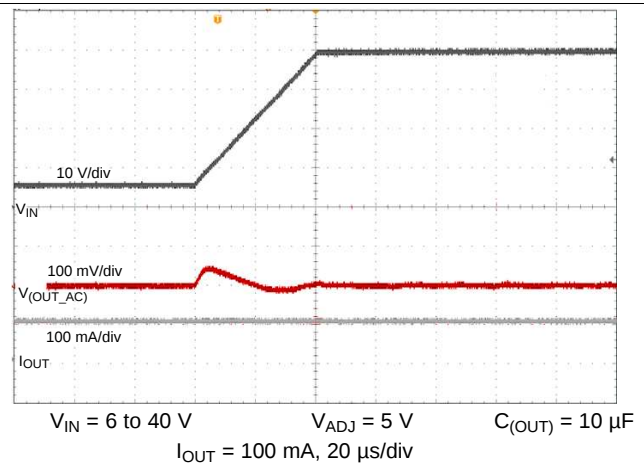


Figure 16. 6- to 40-V Line Transient

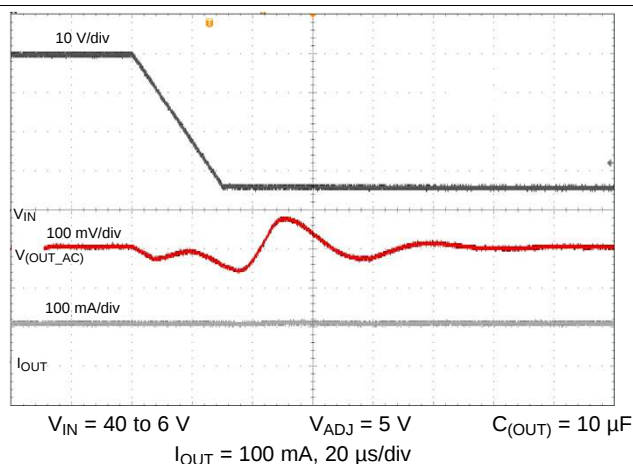


Figure 17. 40- to 6-V Line Transient

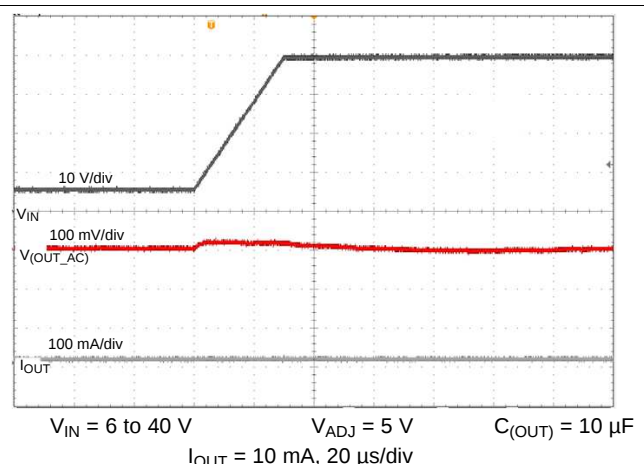
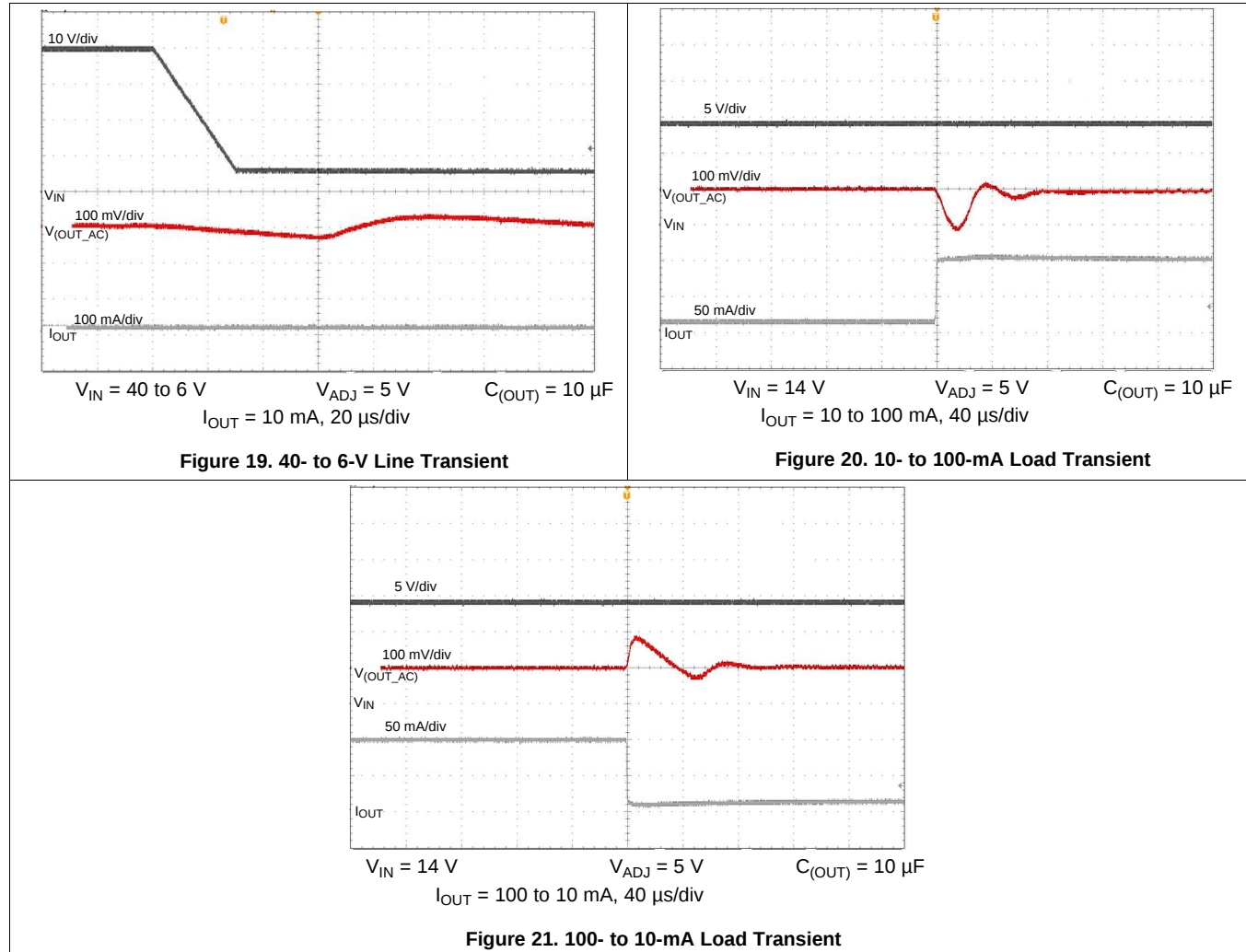


Figure 18. 6- to 40-V Line Transient

Typical Characteristics (continued)

$V_{IN} = 14\text{ V}$, $V_{ADJ} = 5\text{ V}$, $V_{FB} = V_{OUT}$, unless otherwise specified

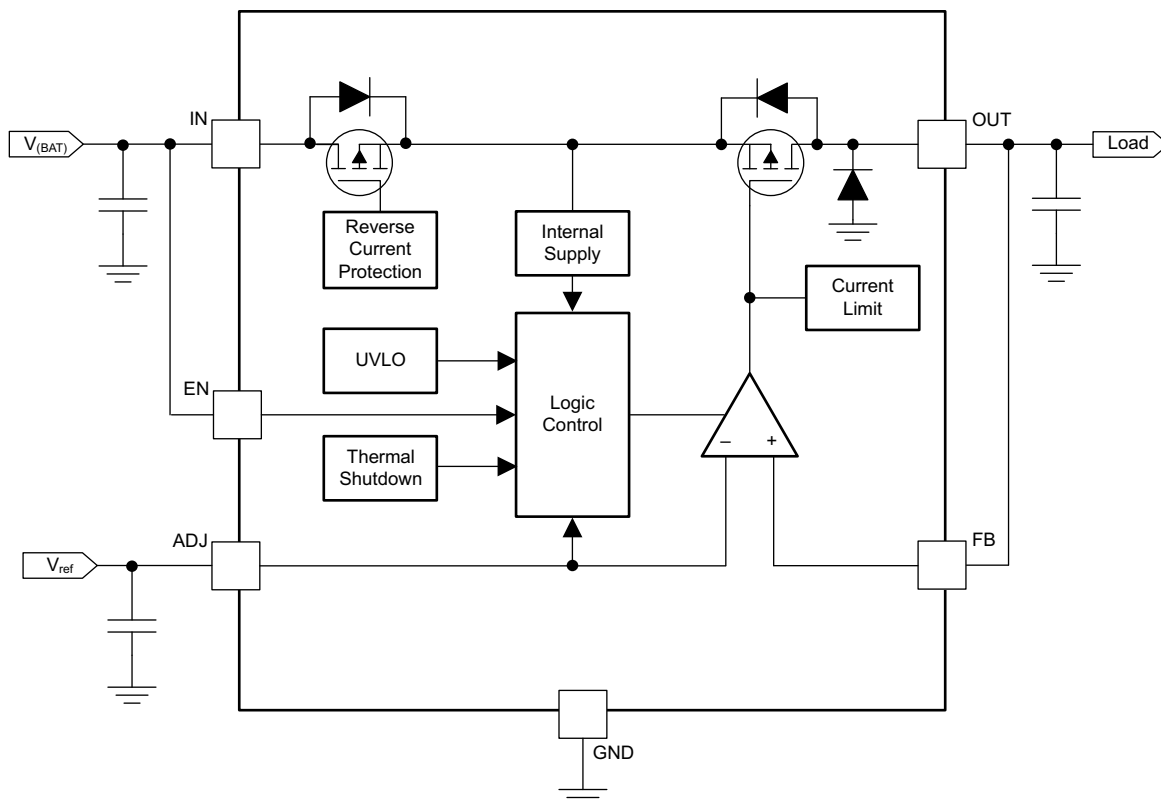


7 Detailed Description

7.1 Overview

The TPS7B4253-Q1 device is a monolithic integrated low-dropout voltage tracker with an ultralow tracking tolerance. Key protection circuits are integrated in the device, including output current limitation, reverse polarity protection, inductive load clamp, output short-to-battery protection, and thermal shutdown in case of an overtemperature event.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Short Circuit and Overcurrent Protection

The TPS7B4253-Q1 device features integrated fault protection which makes the device ideal for automotive applications. To keep the device in a safe area of operation during certain fault conditions, internal current-limit protection is used to limit the maximum output current. This protection protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, the current through the pass element is limited to $I_{O(lim)}$ to protect the device from excessive power dissipation.

7.3.2 Integrated Inductive Clamp Protection

During output turnoff, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp at the OUT pin to help to dissipate the inductive energy stored in the cable. An internal diode is connected between the OUT and GND pins with a DC-current capability of 600 mA for inductive clamp protection.

Feature Description (continued)

7.3.3 OUT Short to Battery and Reverse Polarity Protection

The TPS7B4253-Q1 device can withstand a short to battery when the output is shorted to the battery, as shown in Figure 22. Therefore, no damage to the device occurs.

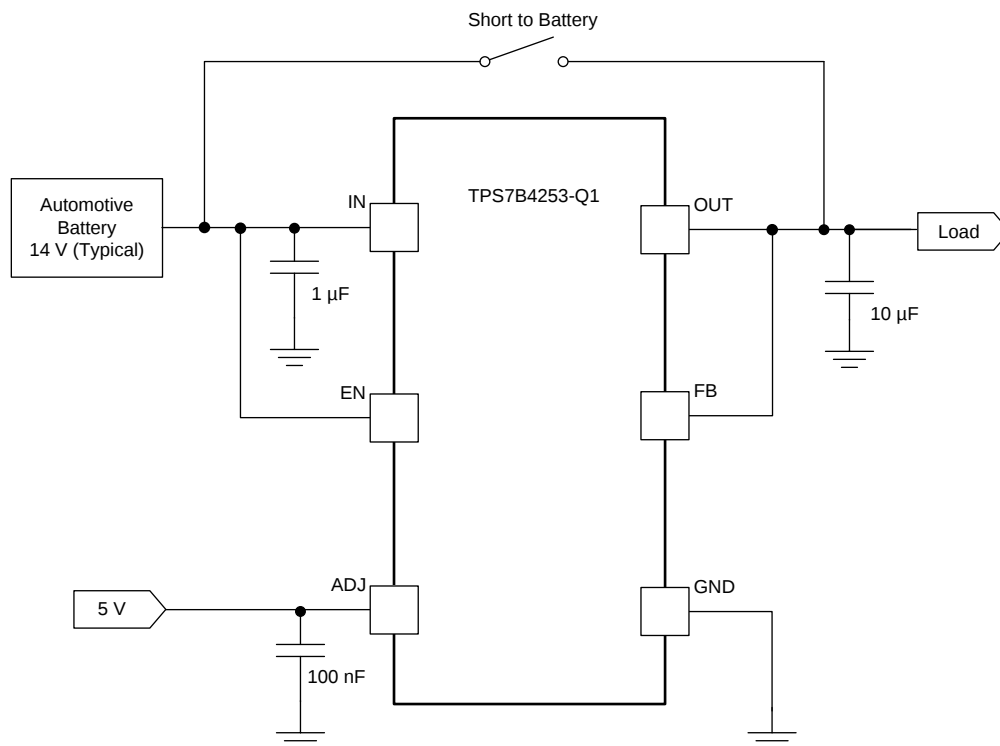


Figure 22. OUT Short to Battery, $V_{IN} = V_{(BAT)}$

A short to the battery can also occur when the device is powered by an isolated supply at lower voltage, as shown in Figure 23. In this case, the TPS7B4253-Q1 supply-input voltage is set to 7 V when a short to battery (14 V typical) occurs on the OUT pin which operates at 5 V. The internal back-to-back PMOS remains on for 1 ms during which the input voltage of the TPS7B4253-Q1 device charges up to the battery voltage. A diode connected between the output of the DC-DC converter and the input of the TPS7B4253-Q1 device is required in case the other loads connected behind the DC-DC converter cannot withstand the voltage of an automotive battery. To achieve a lower dropout voltage, TI recommends using a Schottky diode. This diode can be eliminated if the output of the DC-DC converter and the loads connect behind it withstand automotive battery voltage.

The internal back-to-back PMOS is switched to OFF when reverse polarity or short to battery occur for 1 ms. After that, the reverse current flows out through the IN pin with less than 10 μ A. In the meanwhile, a special ESD structure implemented at the input ensures the device can withstand –40 V.

Feature Description (continued)

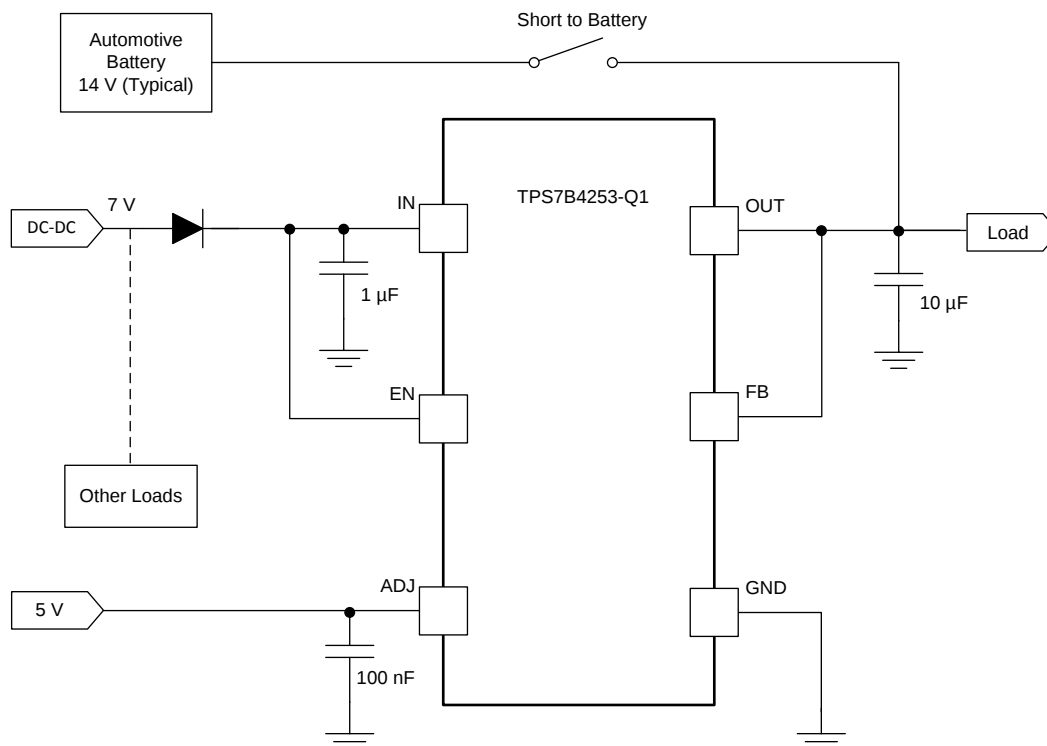


Figure 23. OUT Short to Battery, $V_{IN} < V_{BAT}$

In most cases, the output of the TPS7B4253-Q1 device is shorted to the battery through an automotive cable. The parasitic inductance on the cable results in LC oscillation at the output of the TPS7B4253-Q1 device when the short to battery occurs. Ideally, the peak voltage at the output of the TPS7B4253-Q1 device should be lower than the absolute-maximum voltage rating (45 V) during LC oscillation.

7.3.4 Undervoltage Shutdown

The device has an internally fixed undervoltage-shutdown threshold. Undervoltage shutdown activates when the input voltage on IN drops below UVLO. This activation ensures the regulator is not latched into an unknown state during a low input-supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down and then powers up with a standard power-up sequence when the input voltage is above the required levels.

7.3.5 Thermal Protection

The device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. During continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature decreases to 15°C (typical) lower than the TSD trip point, the output turns on.

NOTE

The purpose of the design of the internal protection circuitry of the TPS7B4253-Q1 device is to protect against overload conditions and is not intended as a replacement for proper heat-sinking. Continuously running the device into thermal shutdown degrades device reliability.

Feature Description (continued)

7.3.6 Regulated Output (OUT)

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has an incorporated soft-start feature to control the initial current through the pass element.

7.3.7 Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input on the EN pin activates the device and turns on the regulator. The device consumes a maximum of shutdown current 4 μ A when the EN pin is low. The EN pin has a maximum internal pulldown of 5 μ A.

7.3.8 Adjustable Output Voltage (FB and ADJ)

7.3.8.1 OUT Voltage Equal to the Reference Voltage

With the reference voltage applied directly at the ADJ pin and the FB pin connected to the OUT pin, the voltage at the OUT pin equals to the reference voltage at the ADJ pin, as shown in [Figure 24](#).

$$V_{OUT} = V_{ADJ} \quad (1)$$

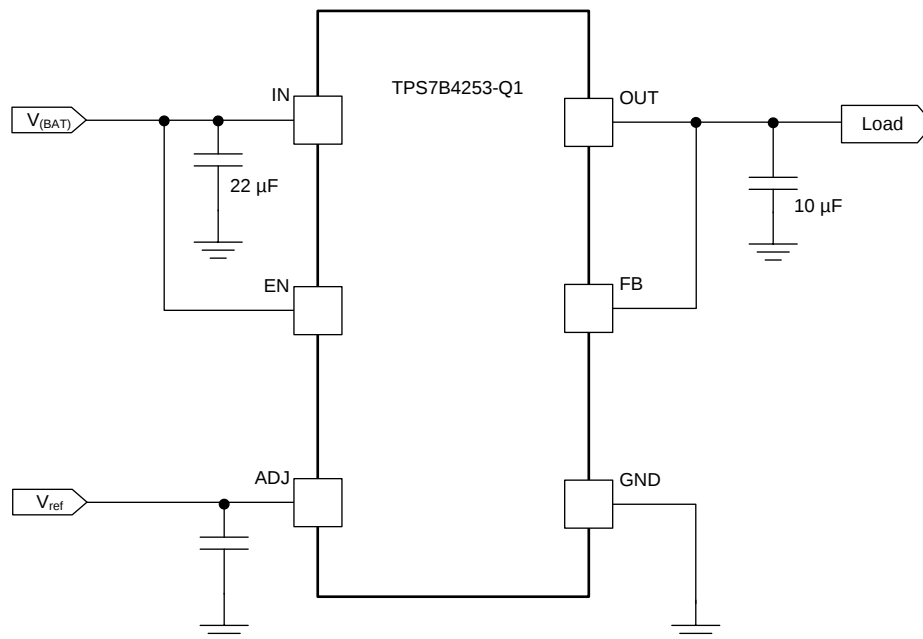


Figure 24. OUT Voltage Equal to the Reference Voltage

7.3.8.2 OUT Voltage Higher Than Reference Voltage

By using an external resistor divider connected between the OUT and FB pins, an output voltage higher than reference voltage can be generated as shown in [Figure 25](#). Use [Equation 2](#) to calculate the value of the output voltage. The recommended range for R1 and R2 is from 10 k Ω to 100 k Ω .

$$V_{OUT} = \frac{V_{ADJ} \times (R1 + R2)}{R2} \quad (2)$$

Feature Description (continued)

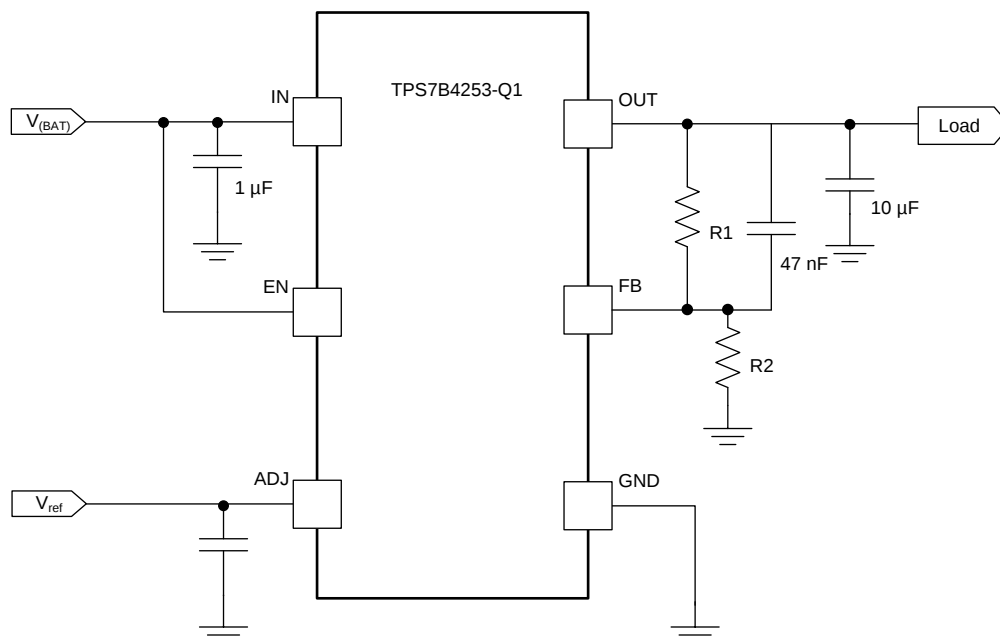


Figure 25. OUT Voltage Higher Than the Reference Voltage

7.3.8.3 Output Voltage Lower Than Reference Voltage

By using an external resistor divider connected at the ADJ pin, an output voltage lower than reference voltage can be generated as shown in Figure 26. Use Equation 3 to calculate the output voltage. The recommended value for both R1 and R2 is less than 100 kΩ.

$$V_{OUT} = \frac{V_{ref} \times R2}{R1 + R2} \quad (3)$$

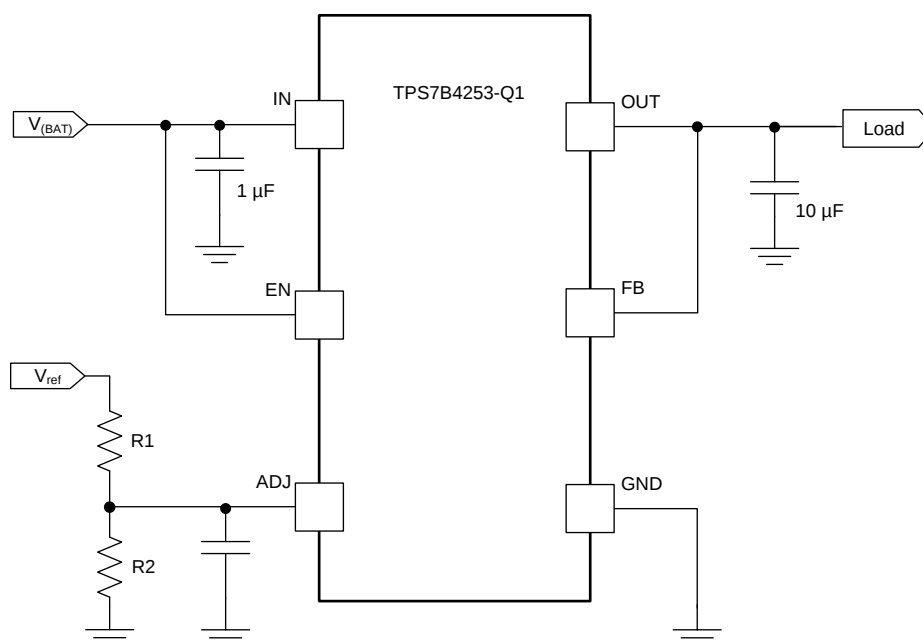


Figure 26. OUT Voltage Lower Than the Reference Voltage

7.4 Device Functional Modes

7.4.1 Operation With $V_{IN} < 4\text{ V}$

The maximum UVLO voltage is 3.65 V, and the device generally operates at an input voltage above 4 V. The device can also operate at a lower input voltage; no minimum UVLO voltage is specified. At an input voltage below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With EN Control

The enable rising edge threshold is 2 V (maximum). With the EN pin held above that voltage and the input voltage above 4 V, the device becomes active. The falling edge of the EN pin is 0.7 V (minimum). Holding the EN pin below that voltage disables the device, thus reducing the quiescent current of the device.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B4253-Q1 device is a 300-mA low-dropout tracking regulator with ultralow tracking tolerance. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

8.2.1 Application With Output Voltage Equal to the Reference Voltage

Figure 27 shows the typical application circuit for the TPS7B4253-Q1 device (using the HTSSOP package as an example). Different values of external components can be used depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

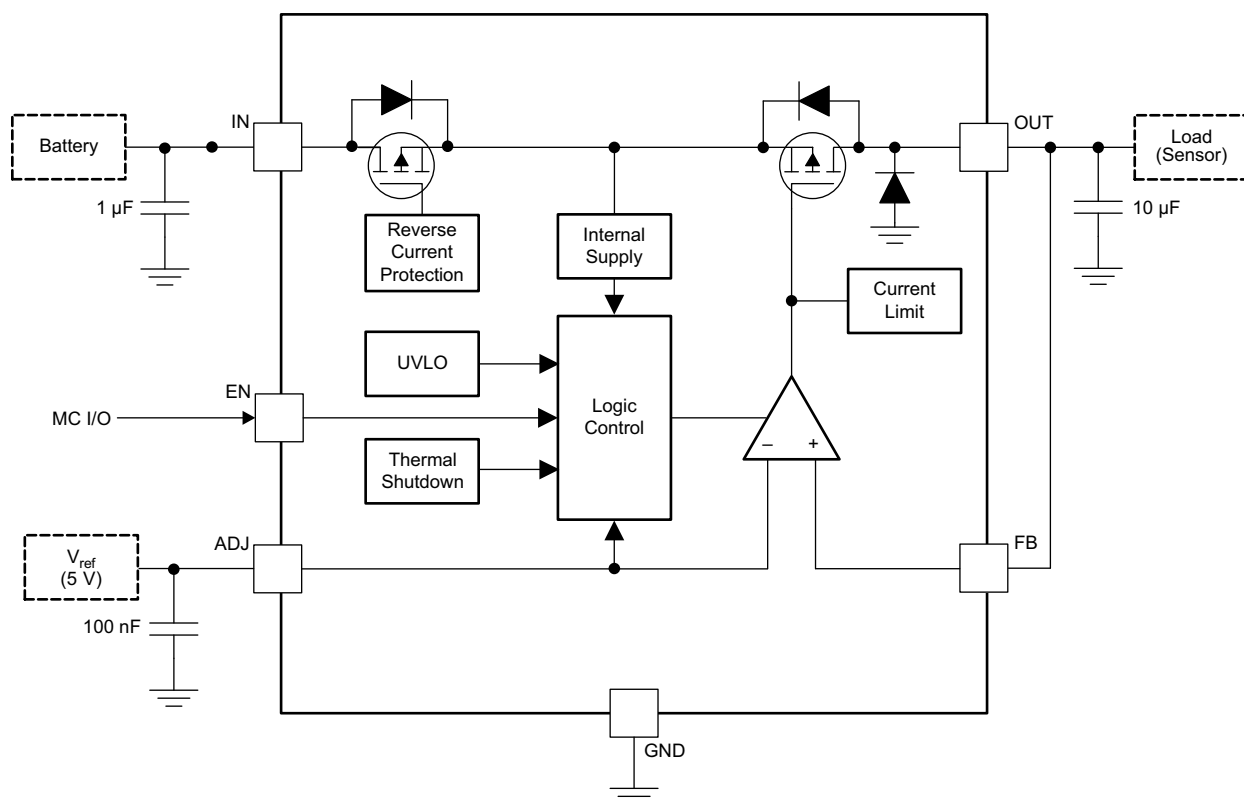


Figure 27. Output Voltage Equals the Reference Voltage

Typical Application (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	4 to 40 V
Output voltage	1.5 to 40 V
Enable voltage	2 to 40 V
ADJ voltage	1.5 to 18 V
Output capacitor	10 to 500 μ F
Output capacitor ESR range	0.001 to 20 Ω

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Reference voltage
- Output current
- Current limit

8.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 2.2 μ F. The voltage rating must be greater than the maximum input voltage.

8.2.1.2.2 Output Capacitor

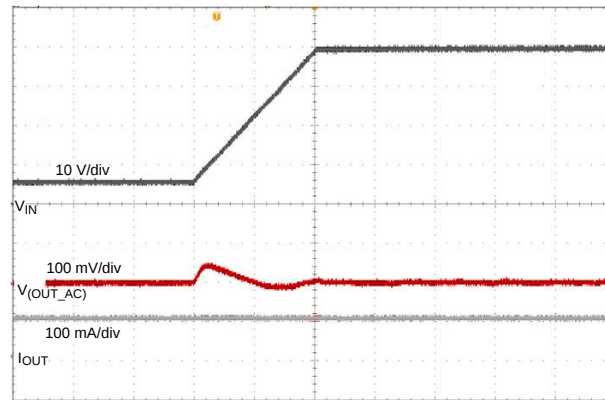
To ensure the stability of the TPS7B4253-Q1 device, the device requires an output capacitor with a value in the range from 10 μ F to 500 μ F and with an ESR range from 0.001 Ω to 20 Ω when the FB pin is directly connected to the OUT pin. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

To achieve an output voltage higher than the reference voltage, a resistor divider is connected between the OUT pin and the FB pin. In this case, a 47-nF feed forward capacitor must be connected between the OUT and FB pins for loop stability. The ESR of the output capacitor must be from 0.001 Ω to 10 Ω .

When multiple capacitors (two or more) are connected in parallel at the OUT pin, the ESR range of each output capacitor must be from 0.001 Ω to 3 Ω for loop stability.

In case the FB pin is shorted to ground, the TPS7B4253-Q1 device functions as a power switch with no need for the output capacitor.

8.2.1.3 Application Curve



$V_{IN} = 6 \text{ to } 40 \text{ V}$ $V_{ADJ} = 5 \text{ V}$ $C_{(OUT)} = 10 \mu\text{F}$
 $I_{OUT} = 100 \text{ mA}, 20 \mu\text{s/div}$

Figure 28. 6- to 40-V Line Transient

8.2.2 High-Side Switch Configuration

As shown in [Figure 29](#), by connecting the FB pin to the GND pin, the TPS7B4253-Q1 device can be used as a high-side switch with current-limit, thermal shutdown, output short-to-battery, and reverse polarity protection. The switching on and off of the device is then controlled through the EN and ADJ pins.

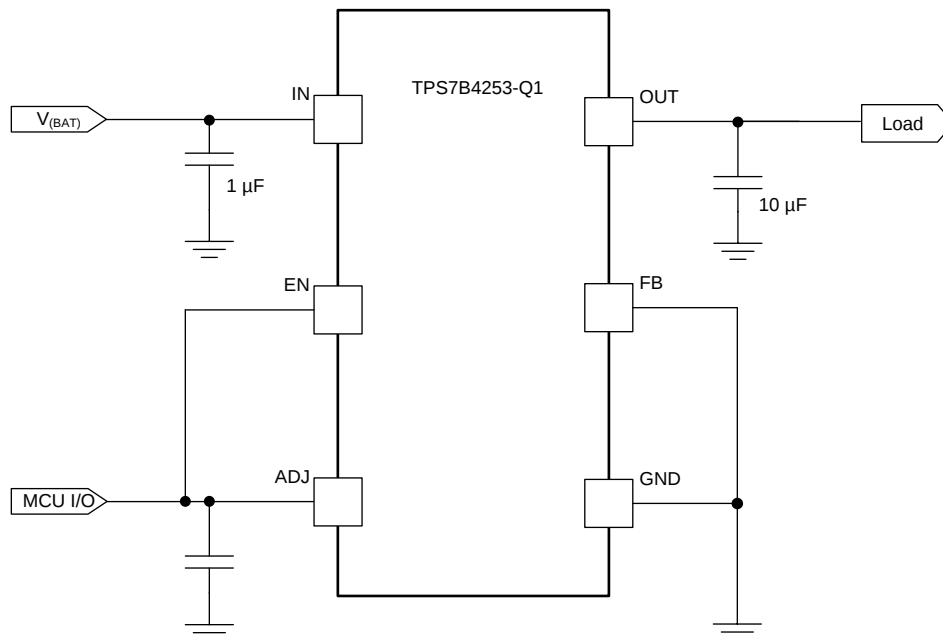


Figure 29. High-Side Switch Application

8.2.3 High Accuracy LDO

With an accurate voltage rail, the TPS7B4253-Q1 device can be used as an LDO with ultrahigh-accuracy output voltage by configuring the device as shown in [Figure 30](#).

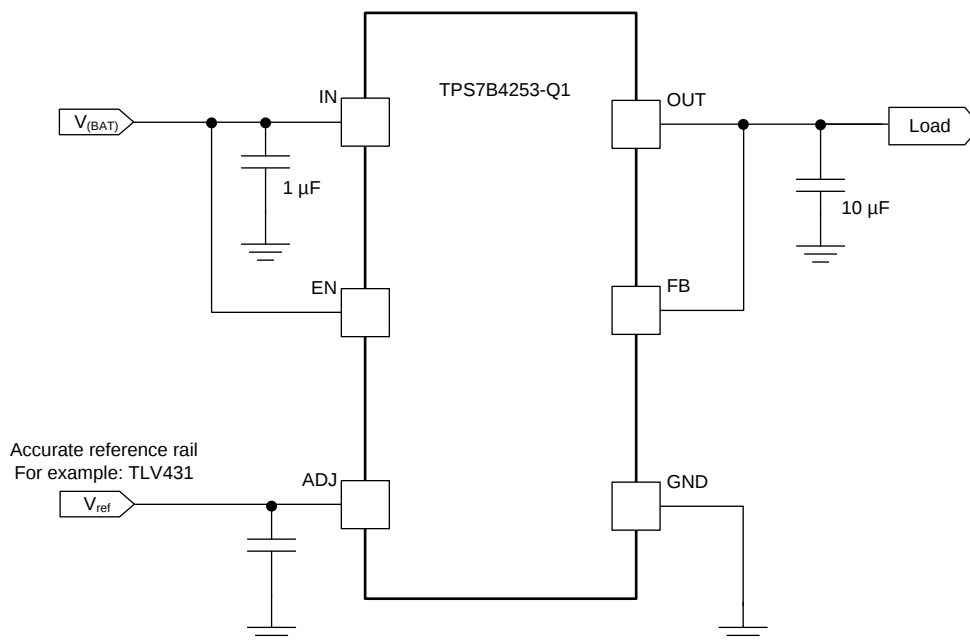


Figure 30. High-Accuracy LDO Application

For example, assume the reference voltage is a 5-V rail with 0.5% accuracy. Because the tracking accuracy between the ADJ and OUT pins is specified below 4 mV across temperature, the output accuracy of the TPS7B4253-Q1 device can be calculated with [Equation 4](#).

$$\text{Accuracy of } V_{\text{OUT}} = \frac{V_{\text{ADJ}} \times 0.5\% + 4 \text{ mV}}{V_{\text{ADJ}}} \times 100\% = \frac{5 \times 0.5\% + 0.004}{5} \times 100\% = 0.58\% \quad (4)$$

9 Power Supply Recommendations

The device is designed to operate with an input voltage supply from 4 V to 40 V. This input supply must be well regulated. If the input supply is more than a few inches away from the TPS7B4253-Q1 device, TI recommends adding an electrolytic capacitor with a value of 2.2 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For the layout of the TPS7B4253-Q1 device, place the input and output capacitors close to the devices as shown in the [Functional Block Diagram](#). To enhance the thermal performance, TI recommends surrounding the device with some vias.

Minimize equivalent series inductance (ESL) and ESR to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces for the path between the output capacitor and the OUT pins because vias can negatively impact system performance and even cause instability.

If possible, and to ensure the maximum performance specified in this data sheet, use the same layout pattern used for the TPS7B4253-Q1 evaluation board, TPS7B4253EVM, which is available at www.ti.com/tool/TPS7B4253EVM.

10.2 Layout Example

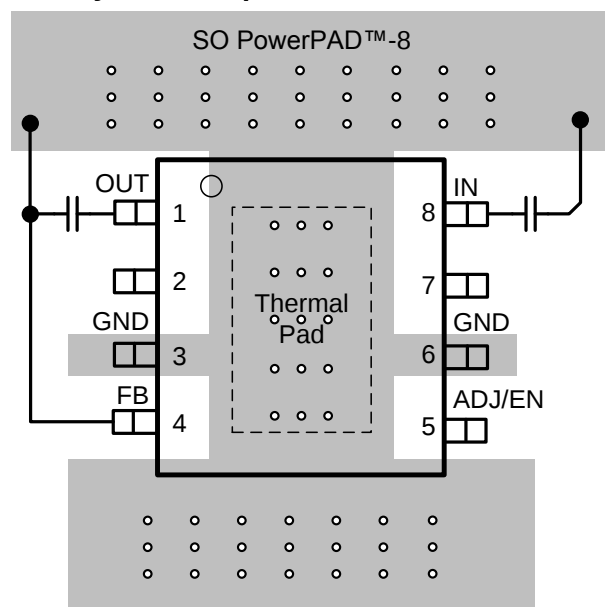


Figure 31. SO PowerPAD Package TPS7B4253-Q1 Layout Example

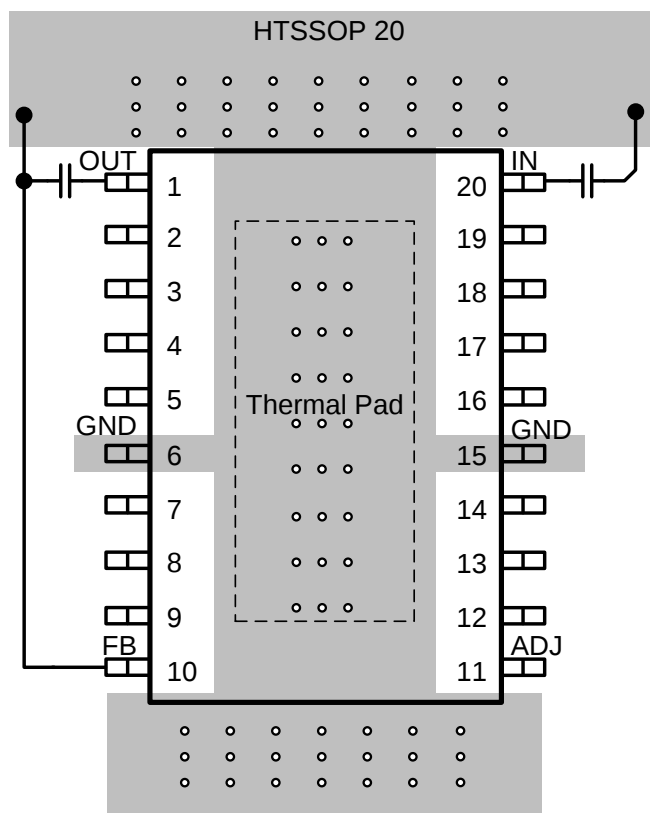


Figure 32. HTSSOP Package TPS7B4253-Q1 Layout Example

10.3 Power Dissipation and Thermal Considerations

Use [Equation 5](#) to calculate the device power dissipation.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I$$

where

- P_D = continuous power dissipation
- I_O = output current
- V_I = input voltage
- V_O = output voltage
- I_Q = quiescent current

(5)

As $I_Q \ll I_O$, the term $I_Q \times V_I$ in [Equation 5](#) can be ignored.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) with [Equation 6](#).

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where

- θ_{JA} = junction-to-junction-ambient air thermal impedance

(6)

A rise in junction temperature because of power dissipation can be calculated with [Equation 7](#).

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D)$$

(7)

For a given maximum junction temperature (T_{Jmax}), the maximum ambient air temperature (T_{Amax}) at which the device can operate can be calculated with [Equation 8](#).

$$T_{Amax} = T_{Jmax} - (\theta_{JA} \times P_D)$$

(8)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For the TPS7B4253 PSpice Transient Model, go to www.ti.com/product/TPS7B4253-Q1/toolssoftware.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- [LDO Parallel Solution Reference Design With TPS7B4253-Q1](#)
- [TPS7B4253-Q1 Evaluation Module](#)
- [TPS7B4253-Q1 Pin FMEA](#)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B4253QDDARQ1	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	4253
TPS7B4253QDDARQ1.A	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	4253
TPS7B4253QPWPRQ1	Active	Production	HTSSOP (PWP) 20	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B4253Q
TPS7B4253QPWPRQ1.A	Active	Production	HTSSOP (PWP) 20	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B4253Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

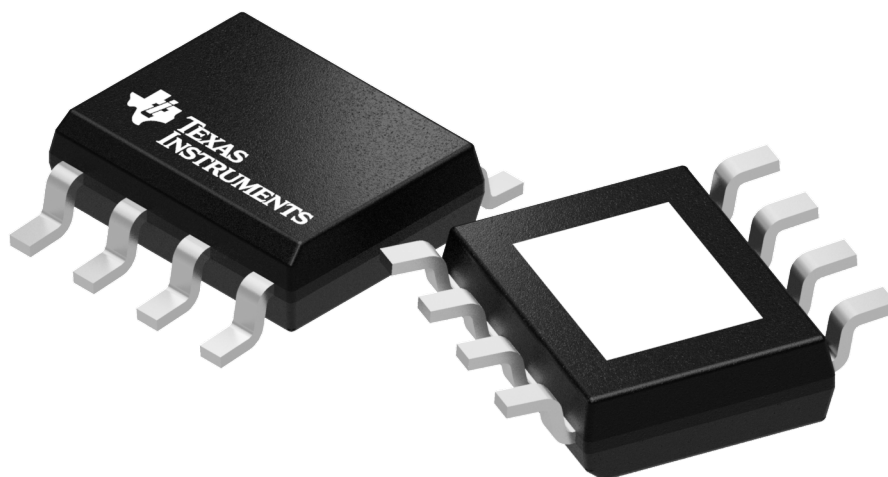
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4253QDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS7B4253QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

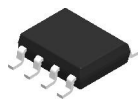


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4253QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS7B4253QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0



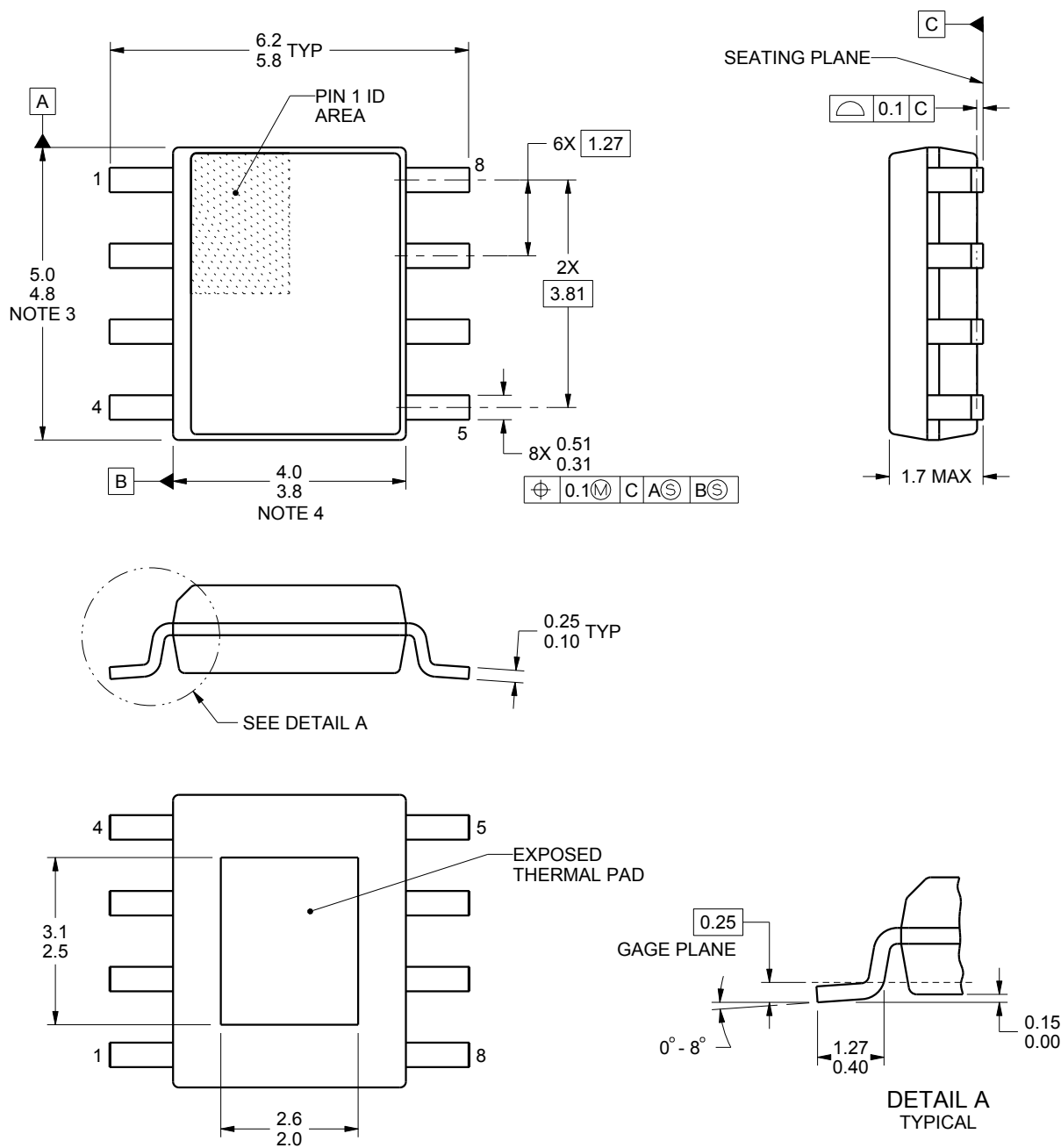
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA0008J

PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4221637/B 03/2016

PowerPAD is a trademark of Texas Instruments.

NOTES:

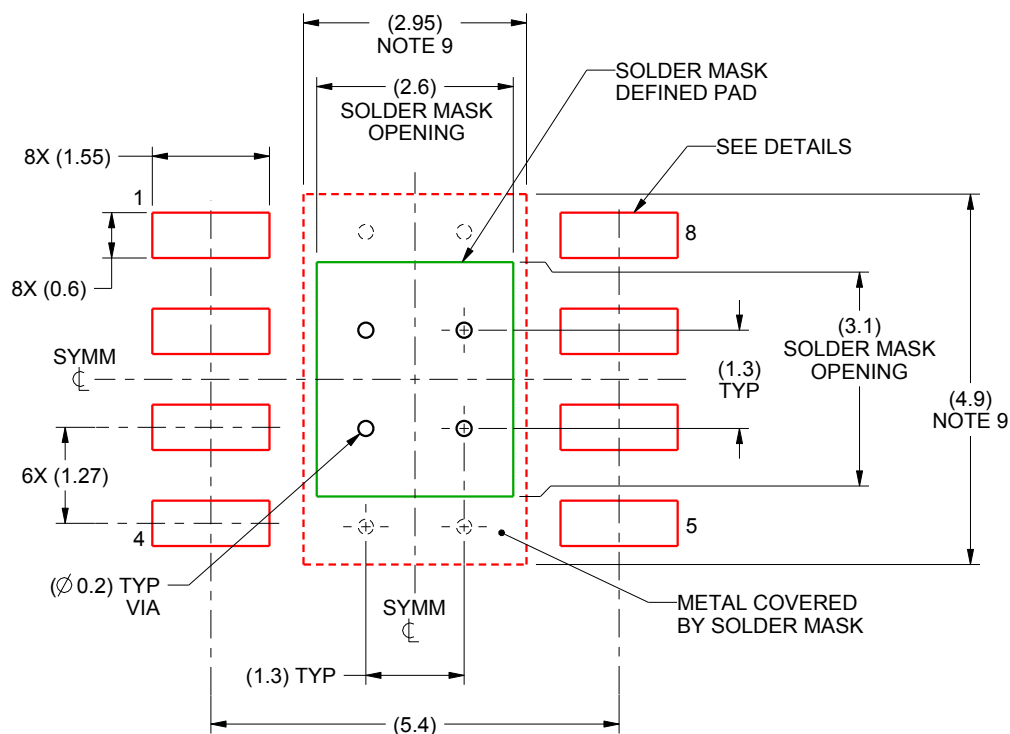
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

EXAMPLE BOARD LAYOUT

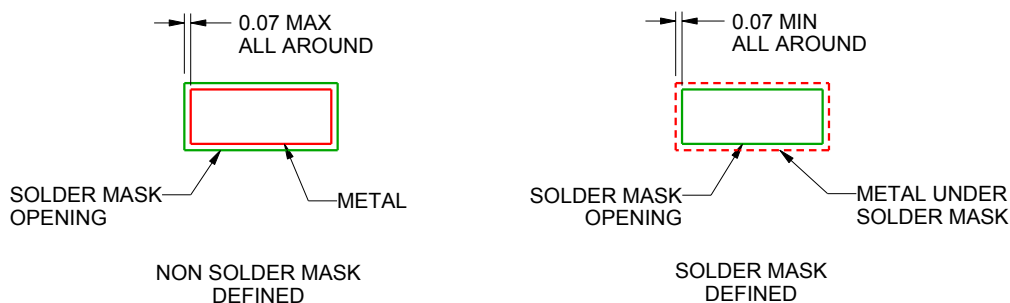
DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

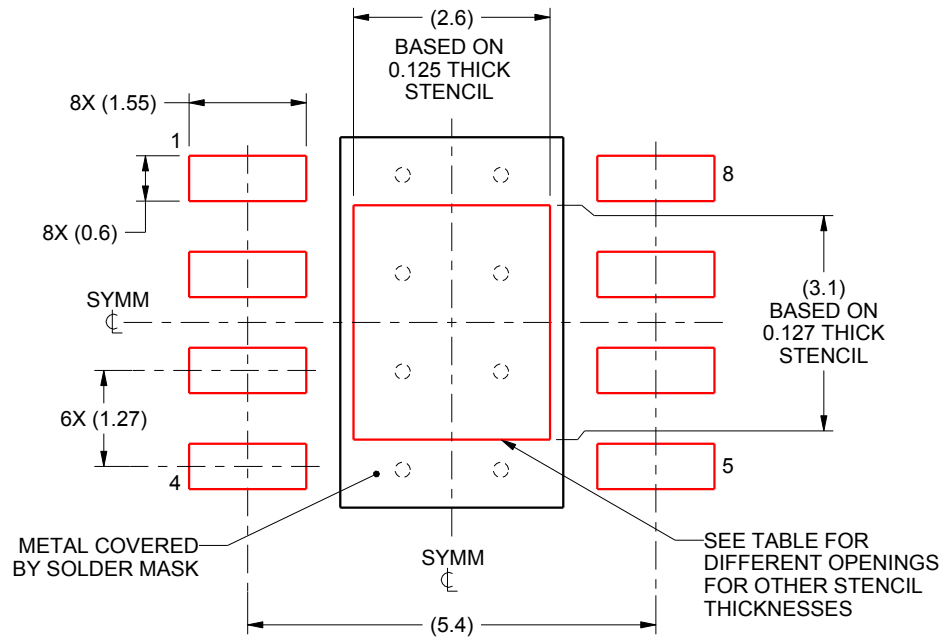
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

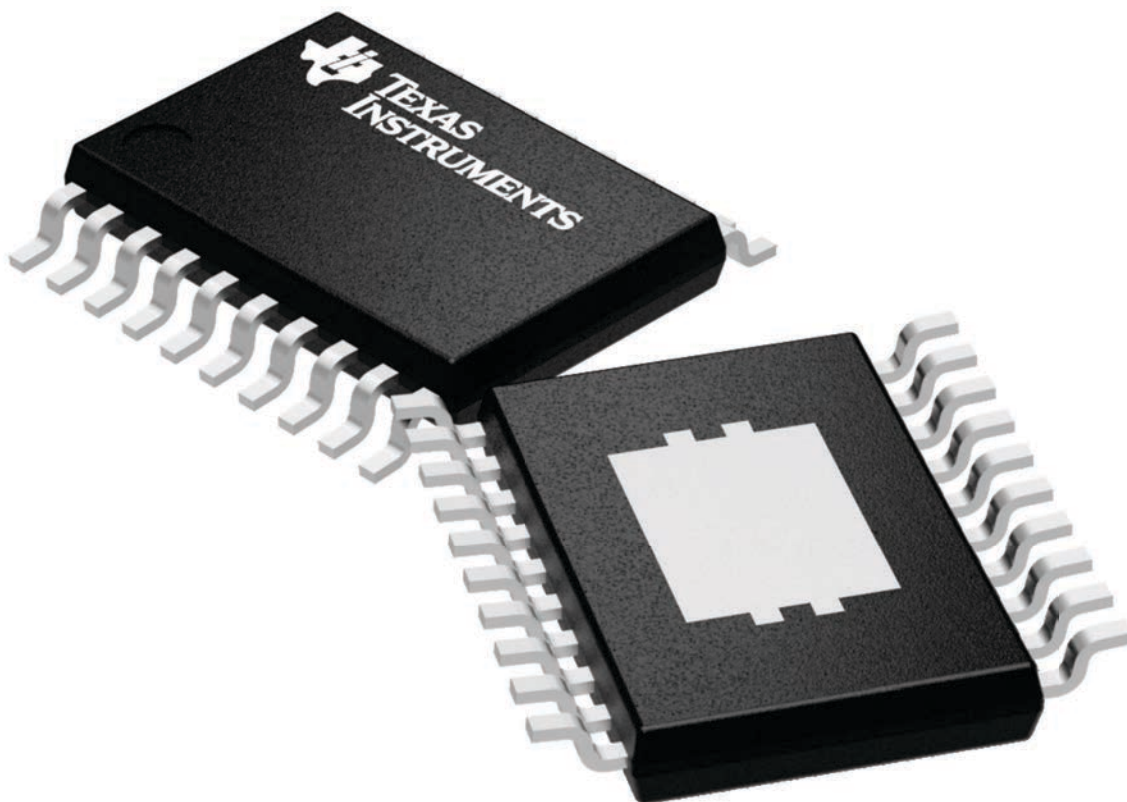
PWP 20

HTSSOP - 1.2 mm max height

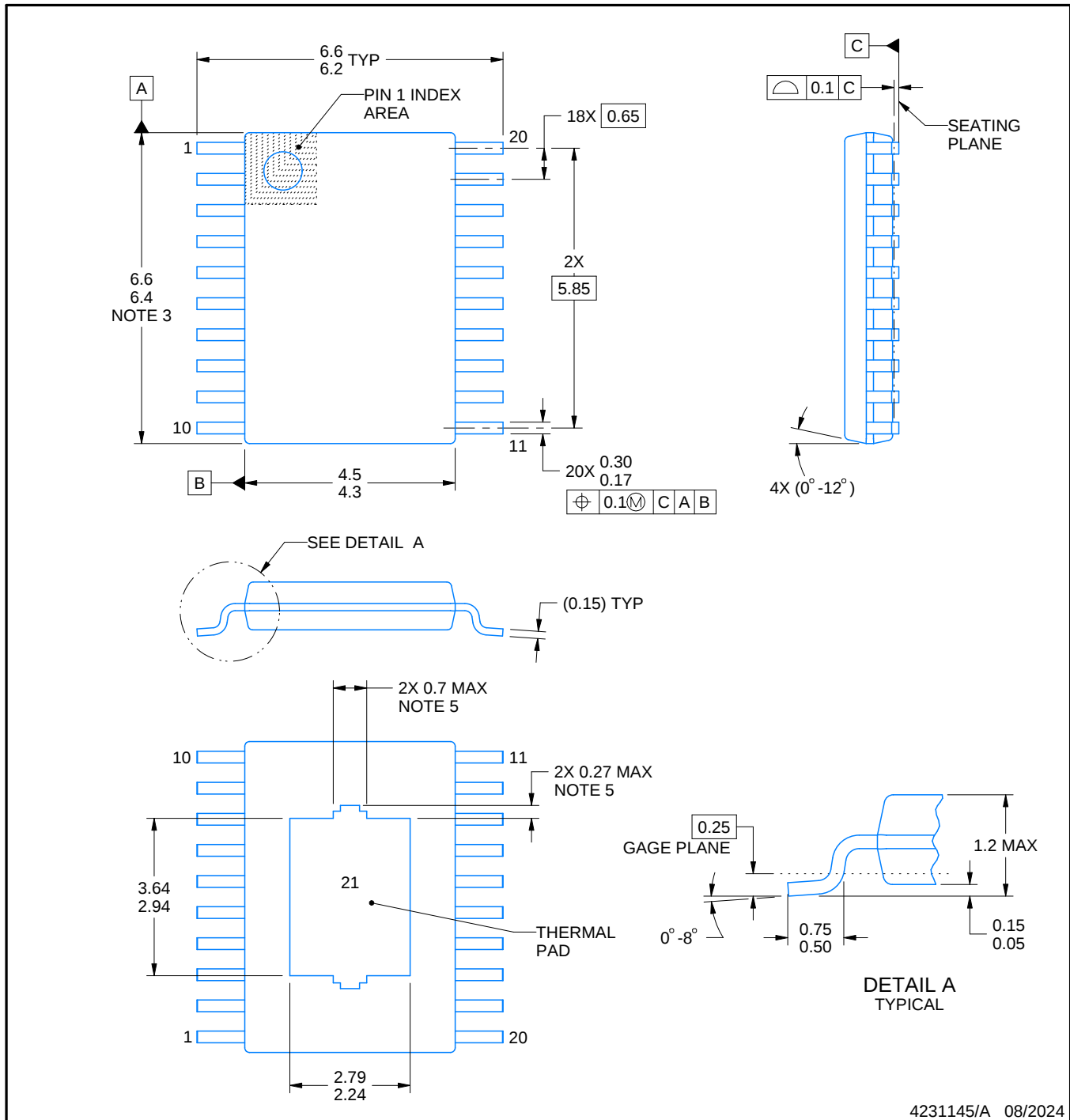
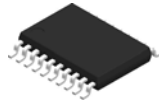
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A



4231145/A 08/2024

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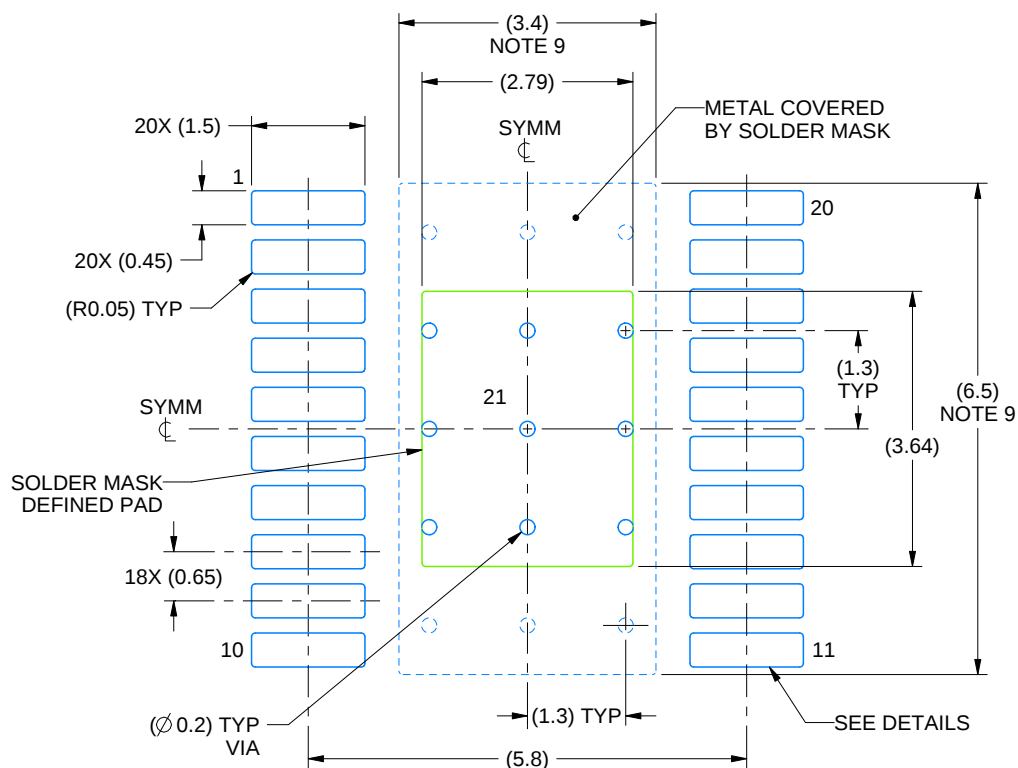
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

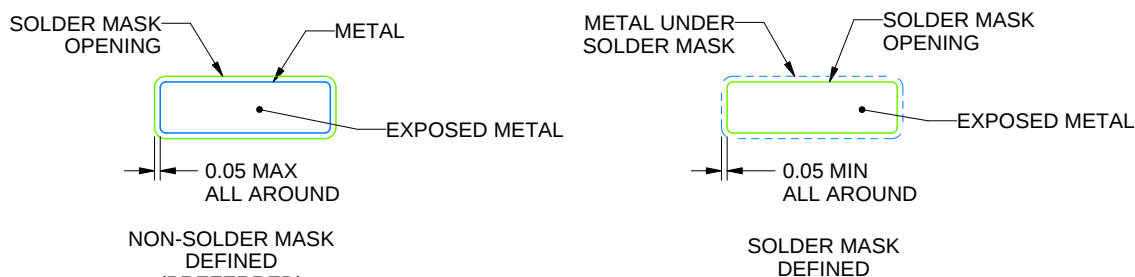
PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4231145/A 08/2024

NOTES: (continued)

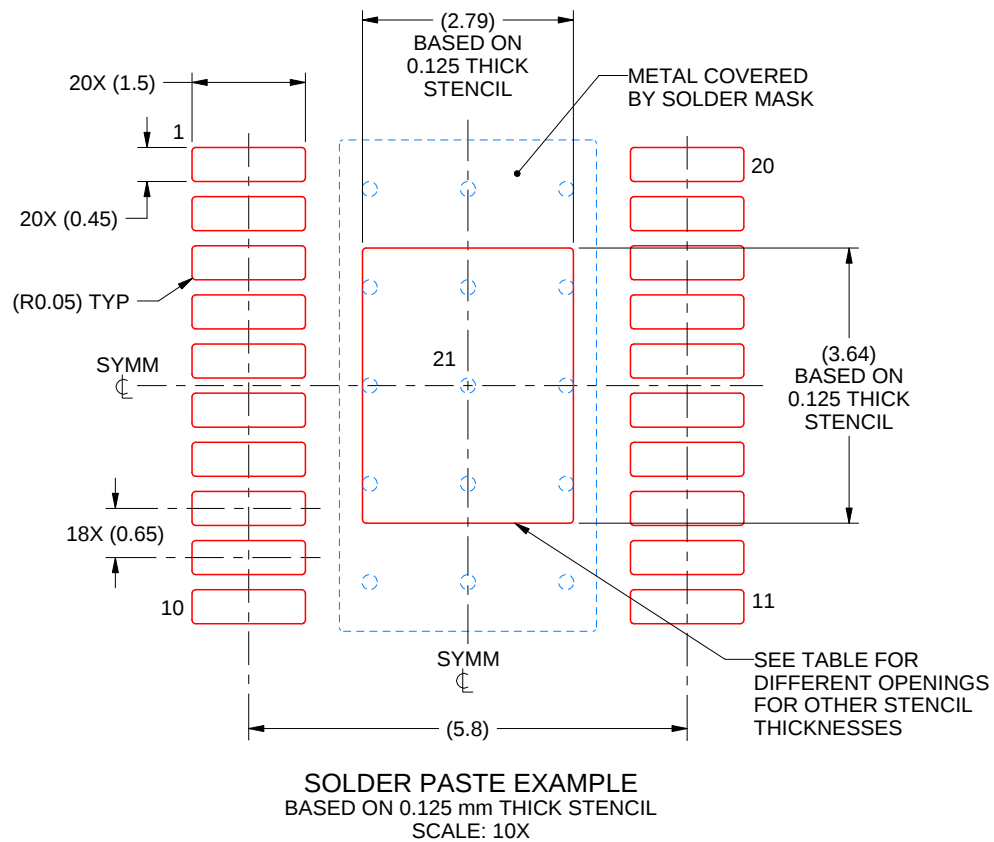
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

4231145/A 08/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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