TPS7A7002 Very Low Input, Very Low Dropout 3-A Regulator With Enable

1 Features

- Input Voltage as Low as 1.425 V
- 380-mV Maximum Dropout at 2 A
- 600-mV Maximum Dropout at 3 A
- Adjustable Output from 0.5 V
- Protections: Current Limit and Thermal Shutdown
- Enable Pin
- 1-µA Ground Current in Shutdown Mode
- Full Industrial Temperature Range
- Available in an SOIC-8, Fully RoHS-Compliant Package

2 Applications

- Telecom and Networking Cards
- Motherboards and Peripheral Cards
- Industrial
- Wireless Infrastructure
- Set-Top Boxes
- Medical Equipment
- Notebook Computers
- Battery-Powered Systems

3 Description

The TPS7A7002 is a high-performance, positive-voltage, low-dropout (LDO) regulator designed for use in applications requiring very-low input voltage and very-low dropout voltage at up to 3 A. The device operates with a single input voltage as low as 1.425 V, and with an output voltage programmable to as low as 0.5 V. The output voltage can be set using an external divider.

The TPS7A7002 features ultra-low dropout, ideal for applications where V_{OUT} is very close to V_{IN}. Additionally, the TPS7A7002 has an enable pin for further reduced power dissipation while in Shutdown mode. The TPS7A7002 provides excellent regulation over variations in line, load, and temperature.

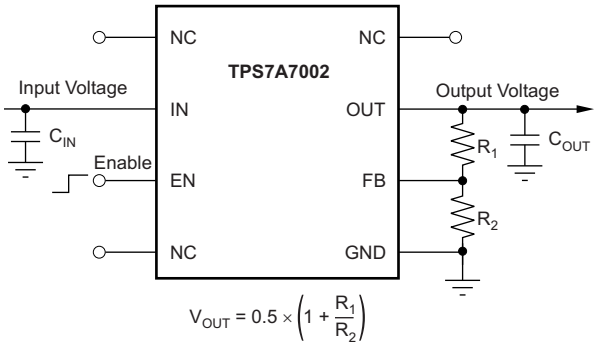
The TPS7A7002 is available in an 8-pin SO PowerPAD™ package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A7002	SO PowerPAD (8)	3.90 mm × 4.89 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application



Dropout Voltage vs Output Current (V_{OUT} = 3.3 V)

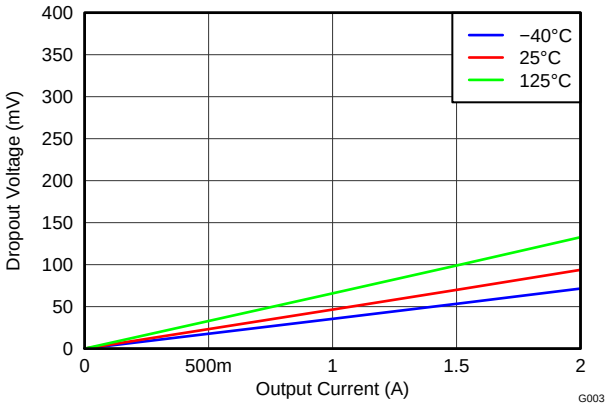


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2015) to Revision D **Page**

- Changed OUT pin description text from "TI recommends using at least a 4.7-μF ceramic capacitor, and up to 10 μF for a good transient response." to " A 4.7-μF or larger capacitor of any type is required for stability." for clarity ... 3
- Changed "operating free-air" to "junction" in *Absolute Maximum Ratings* table condition line ... 4
- Added rows for enable pin voltage, input capacitor, output capacitor, and feedforward capacitance to *Recommended Operating Conditions* table ... 4
- Added min value of 0 to output current in *Recommended Operating Conditions* table ... 4
- Changed note (1) in *Electrical Characteristics* table; deleted initial reference to R_1 and updated R_2 resistor range ... 5
- Changed *Output Capacitor (OUT)* section; reworded for clarity ... 9

Changes from Revision B (November 2013) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision A (September 2013) to Revision B **Page**

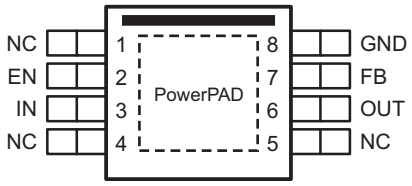
- Changed data sheet status from product preview to production data. ... 1
- Added pin 1 identifier (black bar) to pinout diagram ... 3

Changes from Original (May 2013) to Revision A **Page**

- Changed product preview data sheet ... 7

5 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	Enable input. Pulling this pin to less than 0.5 V turns the regulator off. Connect to V_{IN} if not being used.
FB	7	I	This pin is the output voltage feedback input through voltage dividers. See Table 2 for more details.
GND	8	—	Ground pin
IN	3	I	Input pin. Although it is not required for stability, TI recommends connecting a 1-μF to 10-μF capacitor with low equivalent series resistance (ESR) across this pin and GND.
NC	1, 4, 5	—	Not internally connected. The NC pins are not connected to any electrical node. TI recommends connecting the NC pins to large-area planes.
OUT	6	O	Regulated output pin. A 4.7-μF or larger capacitor of any type is required for stability.
PowerPAD	—	—	TI strongly recommends connecting the thermal pad to a large-area ground plane. If an electrically floating, dedicated thermal plane is available, the thermal pad can also be connected to it.

6 Specifications

6.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	7	V
	EN, FB, OUT	–0.3	V_{IN} + 0.3(2)	
Current	OUT	Internally limited		A
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage temperature, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 7 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.425		6.5	V
V_{EN}	Enable pin voltage	0		V_{IN}	V
C_{IN}	Input capacitor	1		10	µF
C_{OUT}	Output capacitor(1)(2)	4.7	10	200	µF
C_{FB}	Feedforward capacitance	0		100	nF
I_{OUT}	Output current	0		3	A
T_J	Junction temperature	–40		125	°C

(1) See Figure 1 and Figure 2 for additional output capacitor ESR requirements.
(2) For output capacitors larger than 47 µF, a feedforward capacitor of at least 220 pF must be used.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A7002 DDA (SO PowerPAD) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

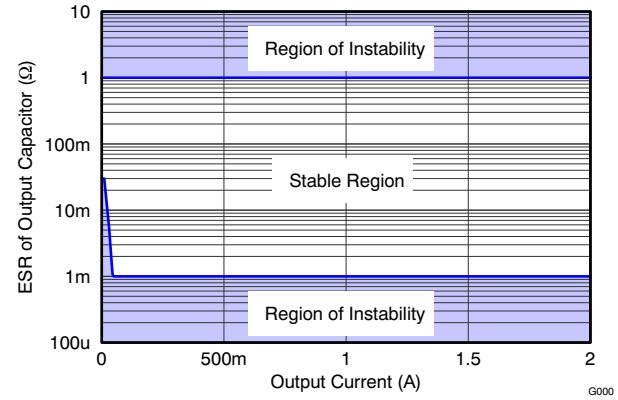
Over the full operating temperature range (see *Recommended Operating Conditions*), V_{EN} = 1.1 V, V_{FB} = V_{OUT}(1), 1.425 V ≤ V_{IN} ≤ 6.5 V, 10 µA ≤ I_{OUT} ≤ 3 A, C_{OUT} = 10 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
I_{GND}	GND pin current	V_{IN} = 3.3 V, 50-Ω load resistor between OUT and GND			3	mA
	Shutdown GND pin current	V_{IN} = 6.5 V, V_{EN} = 0 V			5	µA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage accuracy(2)(3)	V_{IN} = V_{OUT} + 0.5 V(4), I_{OUT} = 10 mA	–2%		2%	
		V_{IN} = 1.8 V, I_{OUT} = 0.8 A, 0°C ≤ T_J = T_A ≤ 85°C	–2%		2%	
		I_{OUT} = 10 mA	–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 10 mA		0.2	0.4	%/V
$\Delta V_{O(\Delta IO)}$	Load regulation(3)	10 mA ≤ I_{OUT} ≤ 3 A		0.25	0.75	%/A
V_{DO}	Dropout voltage (5)	I_{OUT} = 1 A, 0.5 V ≤ V_{OUT} ≤ 5 V			200	mV
		I_{OUT} = 2 A, 0.5 V ≤ V_{OUT} ≤ 5 V			380	
		I_{OUT} = 3 A, 0.5 V ≤ V_{OUT} ≤ 4.8 V			600	
I_{CL}	Output current limit	V_{IN} = 1.425 V, V_{OUT} = 0.9 × $V_{OUT(NOM)}$	3.36			A
FEEDBACK						
V_{REF}	Reference voltage accuracy	V_{IN} = 3.3 V, I_{OUT} = 10 mA	0.49	0.5	0.51	V
I_{FB}	FB pin current	V_{FB} = 0.5 V			1	µA
ENABLE						
I_{EN}	EN pin current	V_{EN} = 0 V, V_{IN} = 3.3 V			0.2	µA
$V_{EN(LO)}$	EN pin input low (disable)	V_{IN} = 3.3 V	0		0.5	V
$V_{EN(HI)}$	EN pin input high (enable)	V_{IN} = 3.3 V	1.1		V_{IN}	V
TEMPERATURE						
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

(1) When setting V_{OUT} to a value other than 0.5 V, connect R_2 to the FB pin using 27-kΩ ≤ R_2 ≤ 33-kΩ resistors. See Figure 7 for details of R_1 and R_2.
(2) Accuracy does not include error on feedback resistors R_1 and R_2.
(3) TPS7A7002 is not tested at V_{OUT} = 0.5 V, 2.3 V ≤ V_{IN} ≤ 6.5 V, and 500 mA ≤ I_{OUT} ≤ 3 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply to any application condition that exceeds the power dissipation limit of the package.
(4) V_{IN} = V_{OUT} + 0.5 V or 1.425 V, whichever is greater.
(5) V_{DO} = V_{IN} – V_{OUT} with V_{FB} = GND configuration.

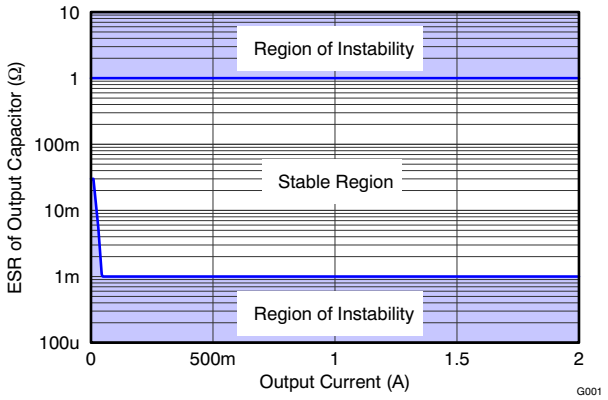
6.6 Typical Characteristics

for all fixed voltage versions and an adjustable version at T_J = 25°C, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, and using the component values in Table 2 (unless otherwise noted)



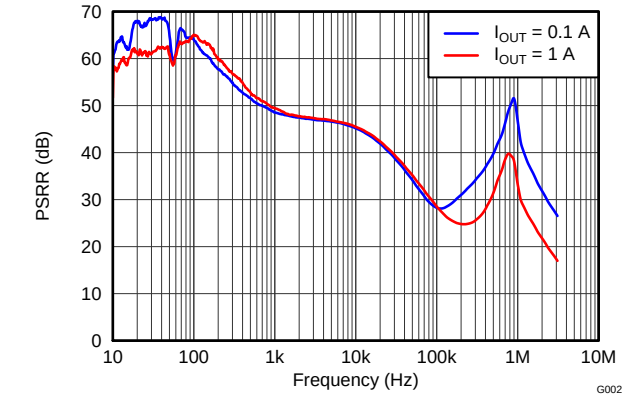
C_{OUT} = 10 µF

Figure 1. Stability Curve



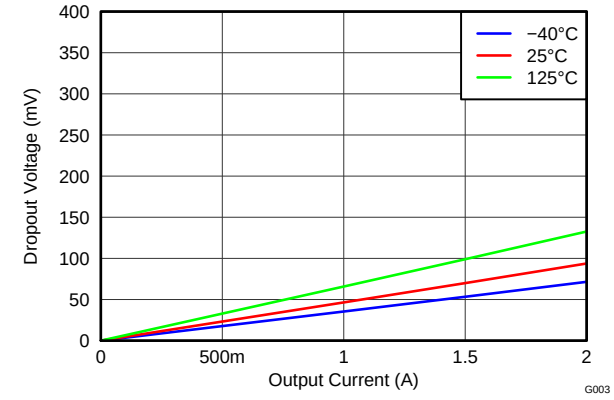
C_{OUT} = 100 µF

Figure 2. Stability Curve



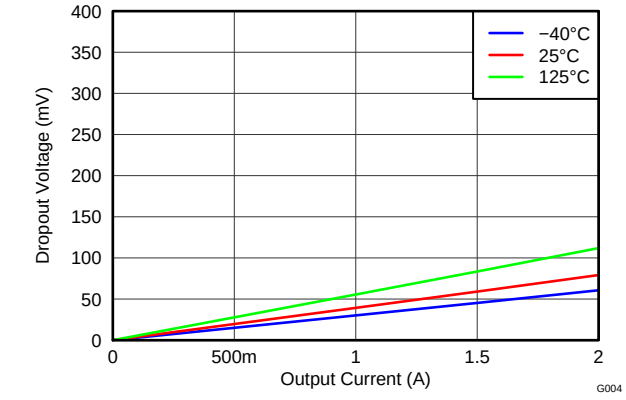
V_{IN} = 5 V, V_{OUT} = 3.3 V

Figure 3. Power-Supply Ripple Rejection vs Frequency



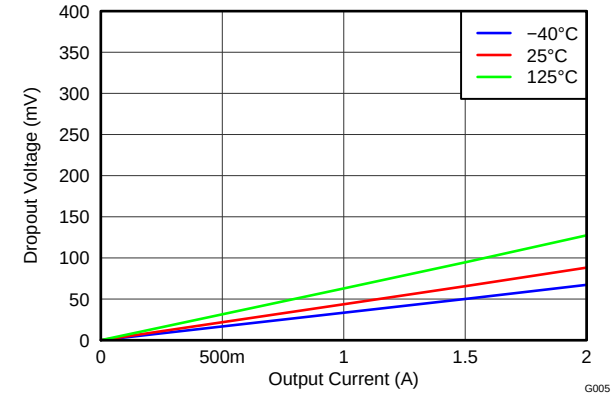
V_{OUT} = 3.3 V

Figure 4. Dropout Voltage vs Output Current



V_{OUT} = 1.6 V

Figure 5. Dropout Voltage vs Output Current



V_{OUT} = 1.4 V

Figure 6. Dropout Voltage vs Output Current

7 Detailed Description

7.1 Overview

The TPS7A7002 offers a high current supply with very-low dropout voltage. The TPS7A7002 is designed to minimize the required component count for a simple, small-size, and low-cost solution.

7.2 Functional Block Diagram

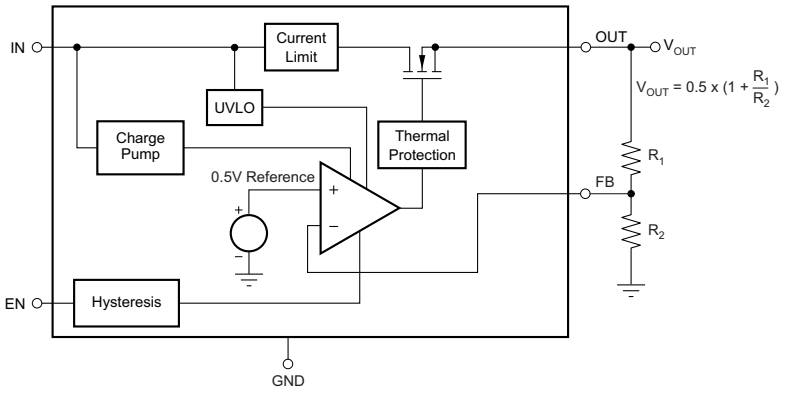


Figure 7. Adjustable Output Voltage Version

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS7A7002 internal current limit helps protect the regulator during fault conditions. During a current limit condition, the output sources a fixed amount of current largely independent of output voltage. For reliable operation, do not operate the device in a current limit state for an extended period of time.

Powering on the device with the enable pin, or increasing the input voltage above the minimum operating voltage while a low-impedance short exists on the output of the device, may result in a sequence of high-current pulses from the input to the output of the device. The energy consumed by the device is minimal during these events; therefore, there is no failure risk. Additional input capacitance helps to mitigate the load transient requirement of the upstream supply during these events.

7.3.2 Enable (EN)

The enable pin (EN) is an active-high logic input. When it is logic low, the device turns off, and the consumption current is less than 1 µA. When it is logic high, the device turns on. The EN pin must be connected to a logic high or logic low level.

When the enable function is not required, connect EN to IN.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{SD}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A7002 offers a high current supply with very-low dropout voltage, and it is designed to minimize the required component count for a simple, small-size, and low-cost solution. This section discusses the implementation of the TPS7A7002 LDO.

8.1.1 Input Capacitor (IN)

An input capacitor is not required for stability; however, TI recommends connecting a 1-µF to 10-µF low equivalent series resistance (ESR) capacitor across IN and GND as close as possible to the device.

8.1.2 Output Capacitor (OUT)

The TPS7A7002 is stable with standard ceramic capacitors with capacitance values from 4.7 µF to 47 µF without a feedforward capacitor. For output capacitors from 47 µF to 200 µF, a feedforward capacitor of at least 220 pF must be used. The TPS7A7002 is evaluated using an X5R-type, 10-µF ceramic capacitor. X5R- and X7R-type capacitors are recommended because of minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases duration of the transient response.

8.1.3 Feedback Resistors (FB)

The voltage on the FB pin sets the output voltage and is determined by the values of R1 and R2. Use Equation 1 to calculate the values of R_1 and R_2 for any voltage.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Table 2 shows the recommended resistor values for the best performance of the TPS7A7002. If the values in Table 2 are not used, keep the value of R_2 from 27 kΩ to 33 kΩ. In Table 2, E96 series resistors are used. For the actual design, pay attention to any resistor error factors.

Table 2. Sample Resistor Values for Common Output Voltages

V_{OUT}	R_1 (kΩ)	R_2 (kΩ)
1	30.1	30.1
1.2	42.2	30.1
1.5	60.4	30.1
1.8	78.7	30.1
2.5	121	30.1
3	150	30.1
3.3	169	30.1
5	274	30.1

8.2 Typical Application

This section describes the implementation of the TPS7A7002, using the feedback pin to configure the output voltage and regulate a 2-A load at 1.4 V using a 1.6-V input voltage, operating in a temperature range of 25°C to 85°C. Figure 8 shows the schematic for this typical application circuit.

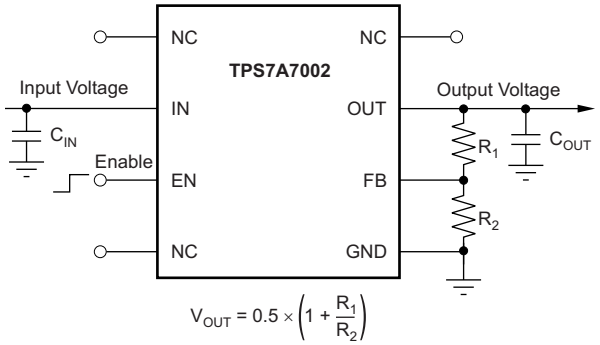


Figure 8. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.6 V ±3%
Output voltage	1.4 V ±3%
Maximum output current	2 A
Ambient temperature	25°C ≤ T_A ≤ 75°C

8.2.2 Detailed Design Procedure

At I_{OUT} = 2 A, the TPS7A7002 has a maximum dropout of less than 150 mV over temperature, as seen in Figure 9; thus, a 200-mV headroom is sufficient for operation over both input and output voltage accuracy.

To achieve 1.2 V on the output, choose the correct feedback resistors. The *Feedback Resistors (FB)* section suggests keeping the value of R_2 in the range of 27 kΩ to 33 kΩ, so select R_2 to be 30.1 kΩ, a standard resistor in the E96 series. Using Equation 1 to achieve a 1.4-V output, determine the size for R_1 using Equation 2.

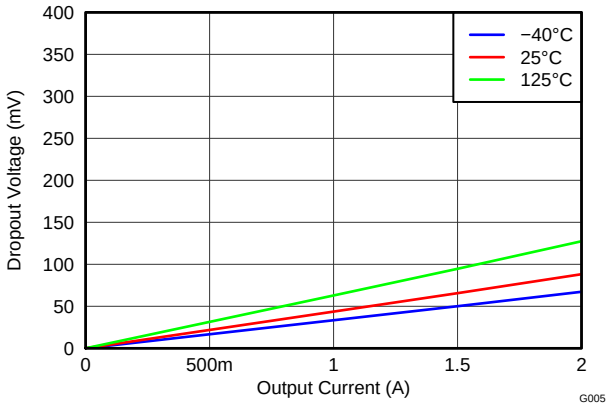
$$R_1 = ((2 \times V_{OUT}) - 1) \times R_2 \quad (2)$$

Given that R_2 = 30.1 kΩ and V_{OUT} = 1.4 V, R_1 = 54.2 kΩ. The closest resistor in the E96 series is 53.6 kΩ, giving an output voltage within the output design requirements.

With a headroom voltage of 200 mV and a 2-A maximum load, the internal power dissipation is 400 mW, and corresponds to a 18.56°C junction temperature rise for the DDA package.

With a 75°C maximum ambient temperature as per design constraints, the junction temperature is at 93.56°C, and satisfies the recommended operating junction temperature range.

8.2.3 Application Curve



V_{OUT} = 1.4 V

Figure 9. Dropout Voltage vs Output Current

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 1.425 V to 6.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best performance, place all circuit components on the same side of the circuit board, and place the external components as close to the device as practically possible. The use of vias and long traces is strongly discouraged because of parasitics that might affect performance; follow these guidelines to minimize parasitics. Also, embed a ground reference plane to maintain accuracy of the output voltage and shield noise. Make sure that this plane is connected to the PowerPAD in order to help spread (or sink) heat from the device; be aware that NC pins might be connected to this plane. The recommended layout is shown in Figure 10.

10.2 Layout Example

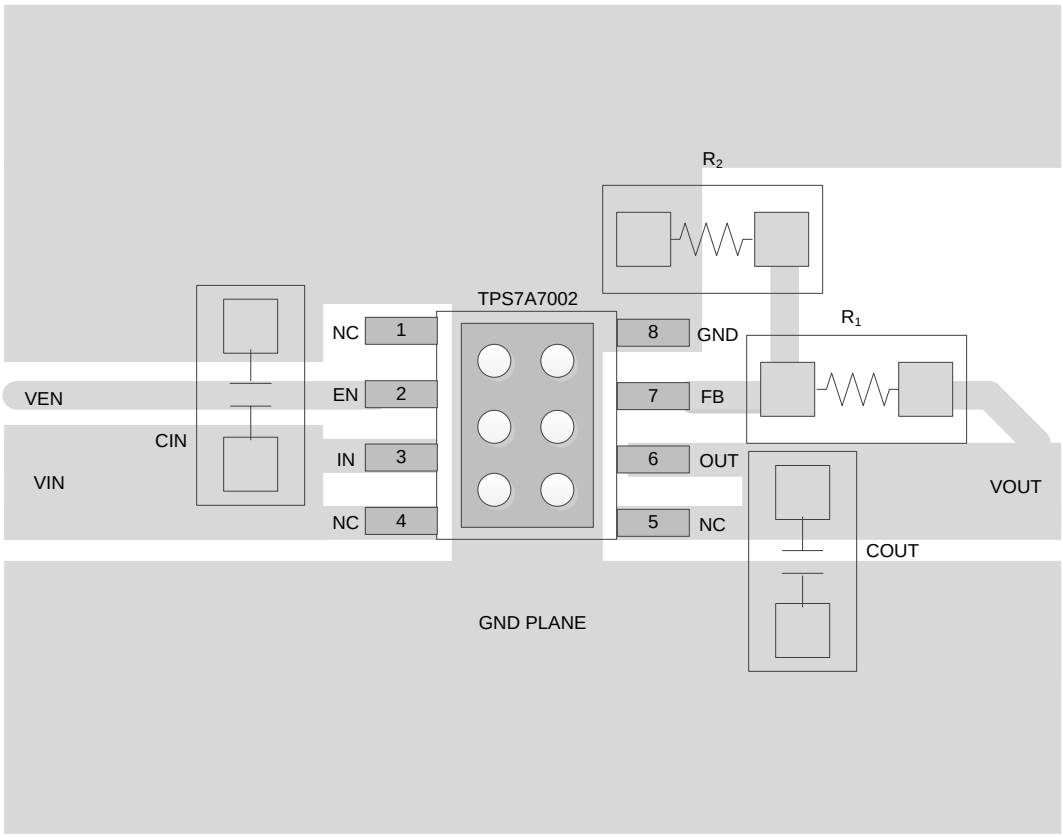


Figure 10. Layout Recommendation

10.3 Thermal Consideration

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is re-enabled.

The internal protection circuitry of the TPS7A7002 is designed to protect against overload conditions. The protection circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A7002 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

Power dissipation (P_D) of the device depends on the input voltage and load conditions, and is calculated using Equation 3.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{3}$$

In order to minimize power dissipation and achieve greater efficiency, use the lowest possible input voltage necessary to achieve the required output voltage regulation

On the SOIC (DDA) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can either be connected to ground or left floating; however, attach the pad to an appropriate amount of copper PCB area to prevent the device from overheating. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device, and is calculated using Equation 4:

$$R_{\theta JA} = \left(\frac{+125°C - T_A}{P_D} \right) \tag{4}$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

PRODUCT(1)	DESCRIPTION
TPS7A7002**yyyz**	YYY is package designator. Z is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *A Topical Index of TI LDO Application Notes*
- *Semiconductor and IC Package Thermal Metrics*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A7002DDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJA
TPS7A7002DDA.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJA
TPS7A7002DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJA
TPS7A7002DDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

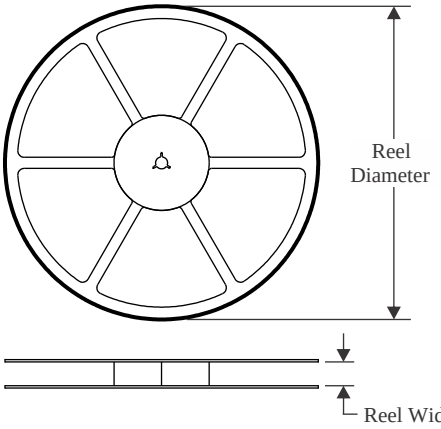
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

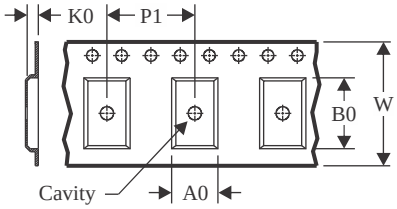
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

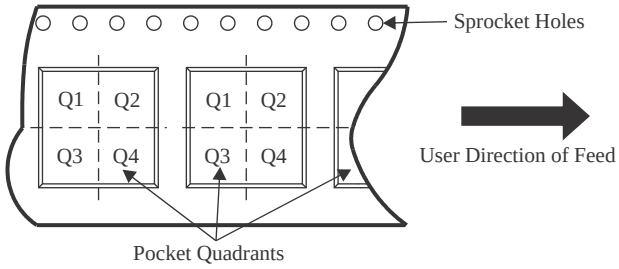


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

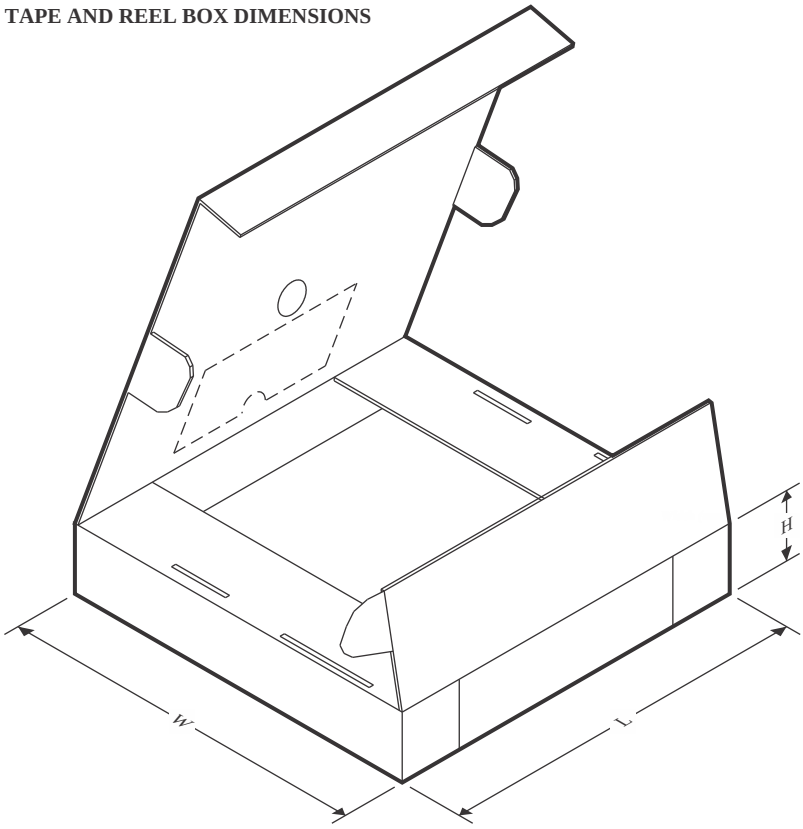
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7002DDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

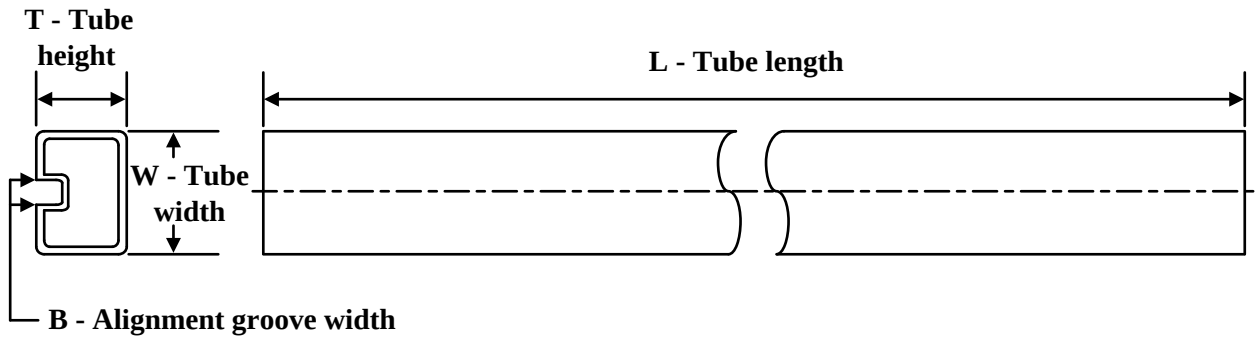
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7002DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

TUBE

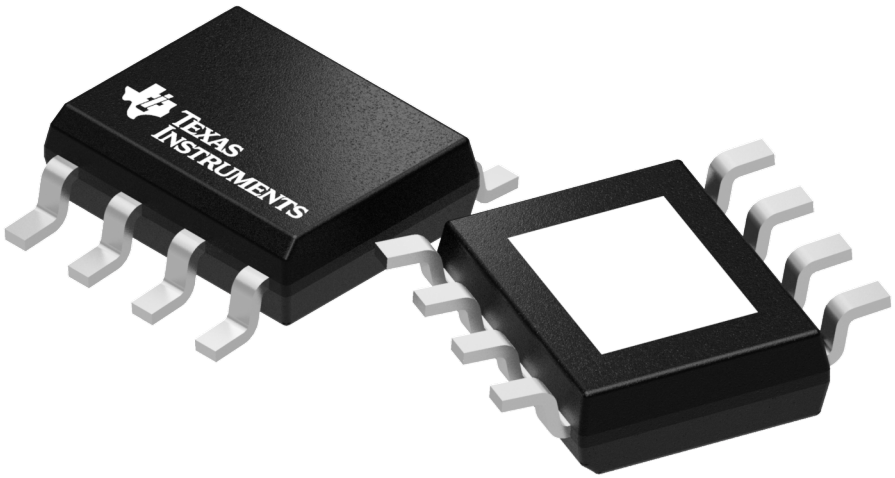


*All dimensions are nominal

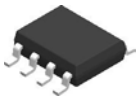
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS7A7002DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS7A7002DDA	DDA	HSOIC	8	75	507	8	3940	4.32
TPS7A7002DDA.B	DDA	HSOIC	8	75	507	8	3940	4.32
TPS7A7002DDA.B	DDA	HSOIC	8	75	517	7.87	635	4.25

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

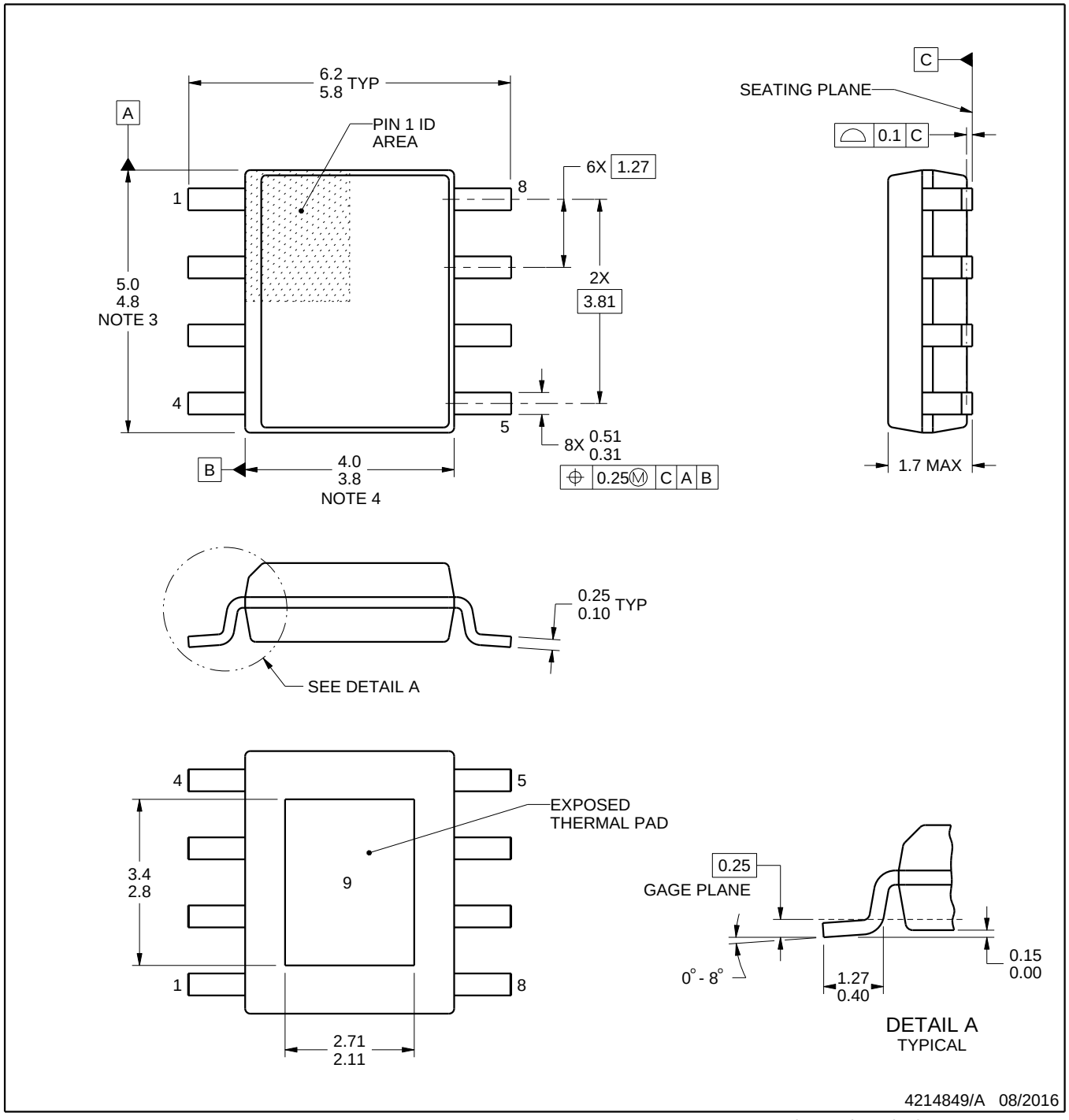


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

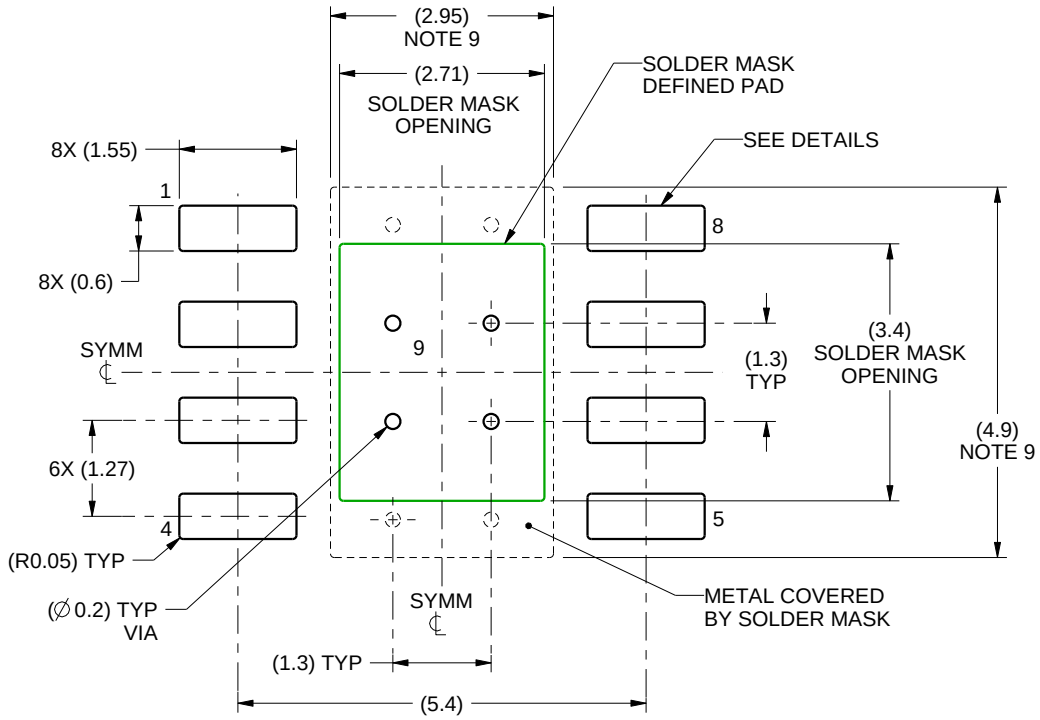
PLASTIC SMALL OUTLINE



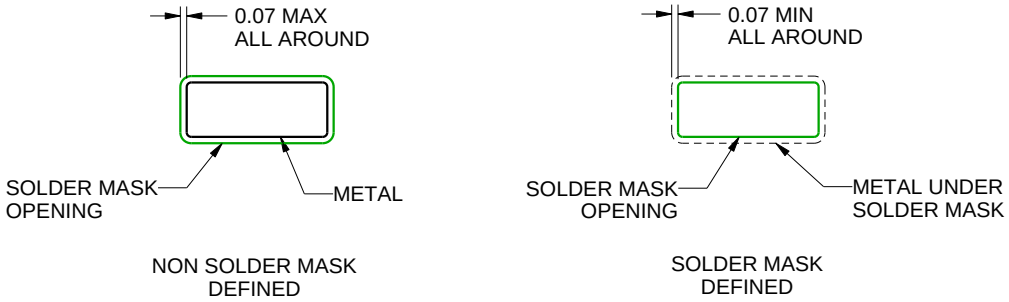
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

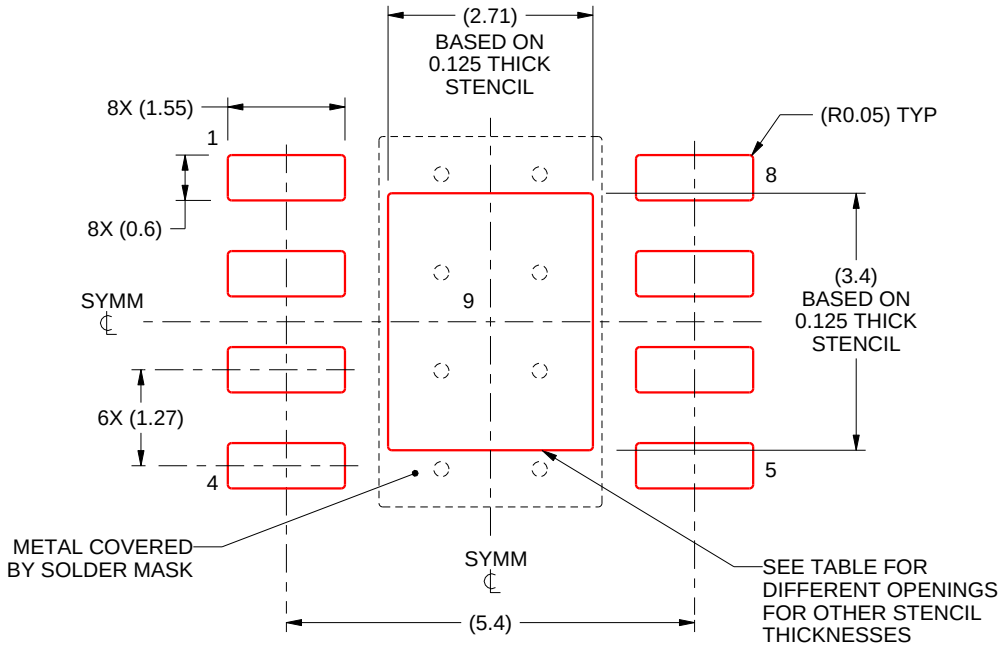
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

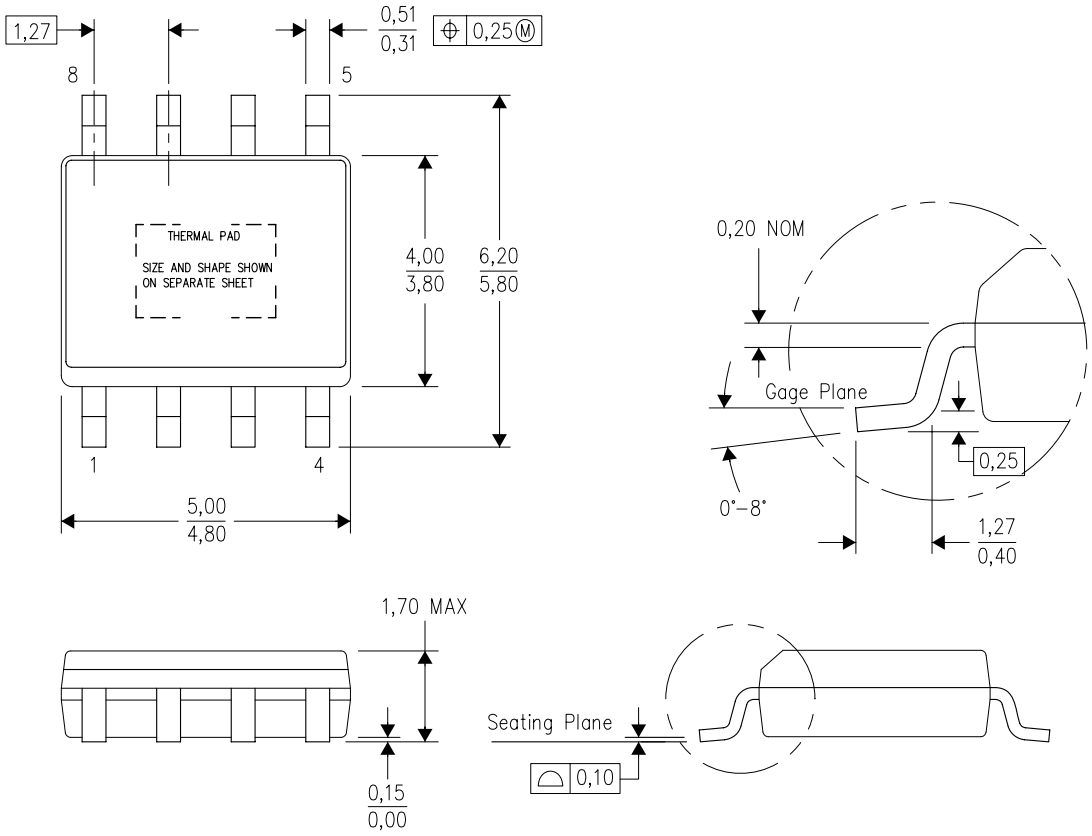
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

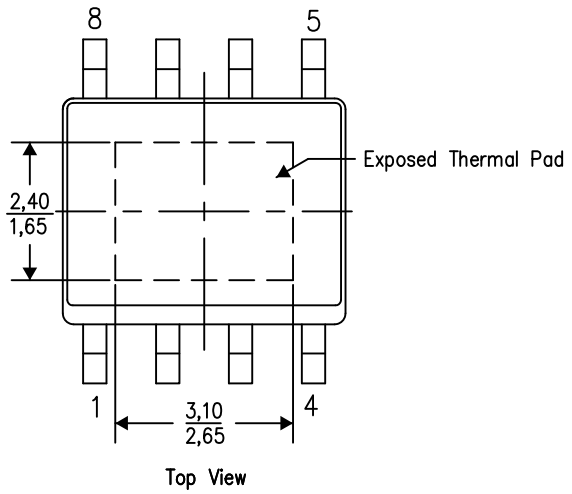
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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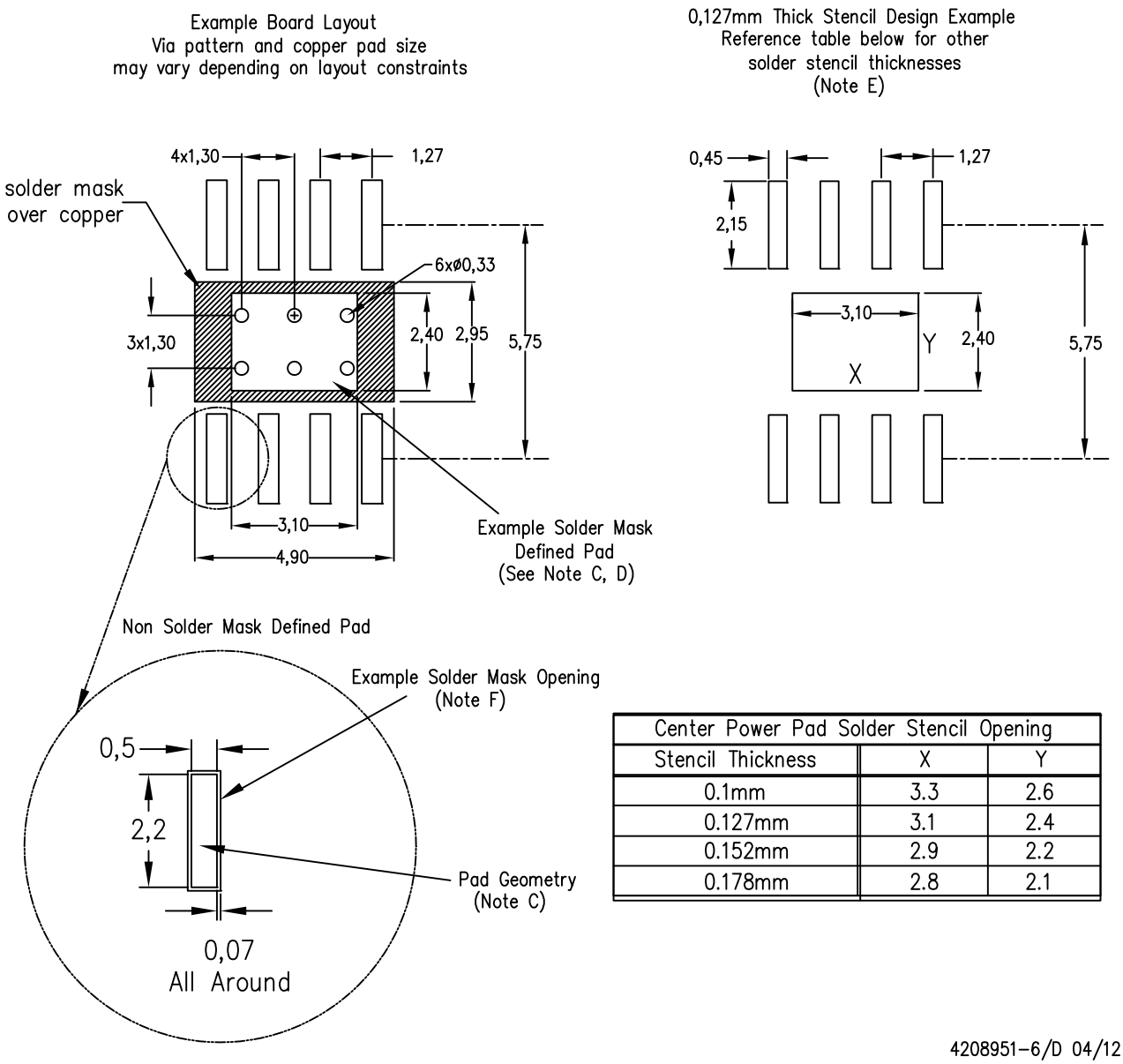
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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