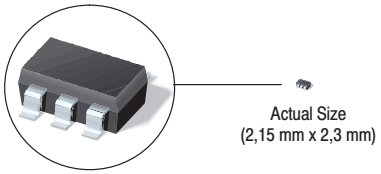


SGLS264A − SEPTEMBER 2004 − REVISED JUNE 2008

ULTRALOW-POWER SC70/SOT-323 PACKAGED 10 mA LDO LINEAR REGULATORS WITH POWER GOOD OUTPUT

FEATURES

- **Qualified for Automotive Applications**
- **10-mA Low-Dropout Regulator**
- **Ultralow 1.2-μA Quiescent Current at 10 mA**
- **5-Pin SC70/SOT-323 (DCK) Package**
- **Integrated Power Good Output**
- **Stable With Any Capacitor (>0.47 μF)**
- **Dropout Voltage Typically 105 mV at 10 mA (TPS79733)**
- **Over Current Limitation**
- **−40°C to 125°C Operating Junction Temperature Range**

APPLICATIONS

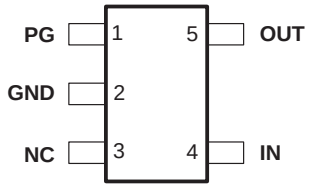
- **Battery Powered Microcontrollers and Microprocessors**

DESCRIPTION

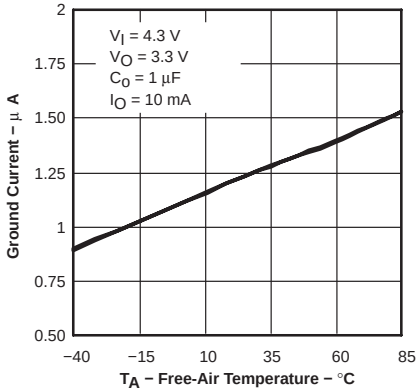
The TPS797xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage and ultralow-power operation. The device is stable with any capacitor (>0.47 μF). Therefore, implementations of this device require little board space due to the miniaturized packaging and potentially small output capacitor. In addition, the family includes an integrated open drain active-high power good (PG) output. Intended for use in microcontroller based, battery-powered applications, the TPS797xx family's low dropout and ultralow-powered operation results in a significant increase in system battery operating life. The small packaging minimizes consumption of board space.

The device is enabled when the applied voltage exceeds the minimum input voltage. The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is low, typically 105 mV at 10 mA of load current and is directly proportional to the load current. The quiescent current is ultralow (1.2 μA typically) and is stable over the entire range of output load current (0 mA to 10 mA). When properly configured with a pullup resistor, the PG output can be used to implement a power-on reset or low battery indicator. The TPS797xx is offered in 1.8-V, 3-V, and 3.3-V fixed options.

DCK PACKAGE
(TOP VIEW)



TPS79733
GROUND CURRENT
vs
FREE-AIR TEMPERATURE



AVAILABLE OPTIONS†§

T_J	VOLTAGE	PACKAGE‡	PART NUMBER	SYMBOL
−40°C to 125°C	1.8 V	SC70/SOT-323 (DCK)	TPS79718QDCKRQ1¶	QTD
	3 V		TPS79730QDCKRQ1¶	QTE
	3.3 V		TPS79733QDCKRQ1¶	QTF

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ Contact Texas Instruments for the availability of other voltage options between 1.25 V and 4.9 V.
¶ The DCKR indicates tape and reel of 3000 parts.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)¶

Input voltage range (see Note 1) . . . . . −0.3 V to 6 V
Maximum dc output voltage . . . . . 4.9 V
Peak output current . . . . . Internally limited
ESD rating, HBM . . . . . 3 kV
ESD rating, CDM . . . . . 1 kV
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating junction temperature range, T_J . . . . . −40°C to 125°C
Operating ambient temperature range, T_A . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

¶ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$ °C/W	$R_{\theta JA}$ °C/W	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25$°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K#	DCK	165.39	396.24	2.52 mW/°C	252mW	139 mW	101 mW
High K‖	DCK	165.39	314.74	3.18 mW/°C	318 mW	175 mW	127 mW

The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
‖ The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $C_o = 1$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I Input voltage (see Note 2)		I_O = 3 mA		1.8		5.5	V
		I_O = 10 mA		2		5.5	V
I_O Continuous output current (see Note 3)				0		10	mA
T_J Operating junction temperature, T_J				-40		125	°C
Output voltage (10 µA to 10 mA Load) (see Note 4)	TPS79718	T_A = 25°C,	2.8 V < V_I < 5.5 V		1.8		V
		T_J = −40°C to 125°C,	2.8 V < V_I < 5.5 V	1.71		1.89	
	TPS79730	T_A = 25°C,	4 V < V_I < 5.5 V		3		V
		T_J = −40°C to 125°C,	4 V < V_I < 5.5 V	2.880		3.12	
	TPS79733	T_A = 25°C,	4.3 V < V_I < 5.5 V		3.3		V
		T_J = −40°C to 125°C,	4.3 V < V_I < 5.5 V	3.168		3.432	
Quiescent current (GND current) (see Note 4)		T_A = 25°C,	0 µA < I_O < 10 mA		1.2		µA
		T_J = −40°C to 125°C,	I_O = 10 mA			5	
Load regulation		T_A = 25°C,	I_O = 1 µA to 10 mA		17		mV
Output voltage line regulation ($\Delta V_O/V_O$) (see Note 4)		V_O + 1 V < V_I ≤ 5.5 V,	T_A = 25°C		0.15		%/V
		V_O + 1 V < V_I ≤ 5.5 V,	T_J = −40°C to 125°C			0.8	
Output noise voltage (TPS79718)		BW = 200 Hz to 100 kHz, C_o = 10 µF, I_O = 10 mA,	T_A = 25°C		600		μV_{RMS}
Output current limit		V_O = 0 V,	See Note 4		190	300	mA
Power supply ripple rejection (TPS79718)		f = 100 Hz, I_O = 10 mA,	C_o = 10 µF, T_A = 25°C		50		dB
Dropout voltage (see Note 5)	TPS79730	I_O = 10 mA,	T_A = 25°C		110		mV
		I_O = 10 mA,	T_J = −40°C to 125°C			400	
	TPS79733	I_O = 10 mA,	T_A = 25°C		105		
		I_O = 10 mA,	T_J = −40°C to 125°C			400	
Minimum input voltage for valid PG		$I_{O(PG)}$ = 100µA,	$V_{(PG)}$ ≥ 0.8 V		1.2		V
PG trip threshold voltage		V_O decreasing		82	90	96	$\%V_O$
PG output low voltage		V_I = 1.4 V,	$I_{O(PG)}$ = 100 µA		0.14	0.4	V
PG leakage current		$V_{(PG)}$ = 5 V		0.1			nA

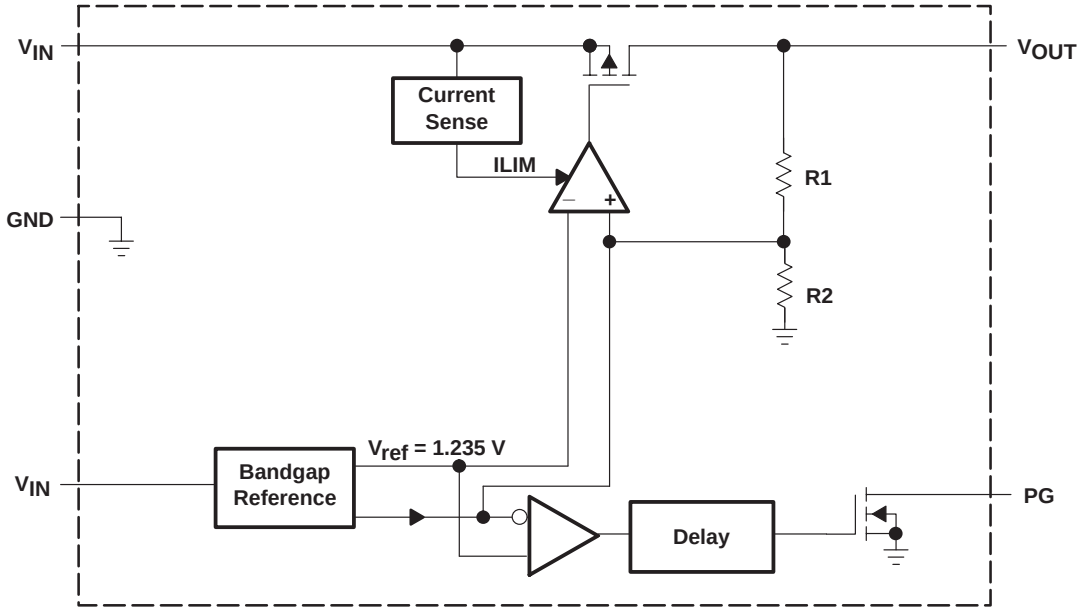
NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:
$V_I(min) = V_O(max) + V_{DO}$ (max load)

3. Continuous output current is limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

4. The minimum IN operating voltage is 1.8 V or V_O (typ) + 1 V, whichever is greater. The maximum IN voltage is 5.5 V. There is no minimum output current requirement and the maximum output current is 10 mA.

5. IN voltage equals V_O(typ) −100 mV; The TPS79730 input voltage is set to 2.9 V and the TPS79733 input voltage is set to 3.2 V. The TPS79718 dropout voltage is limited by input voltage range limitations.

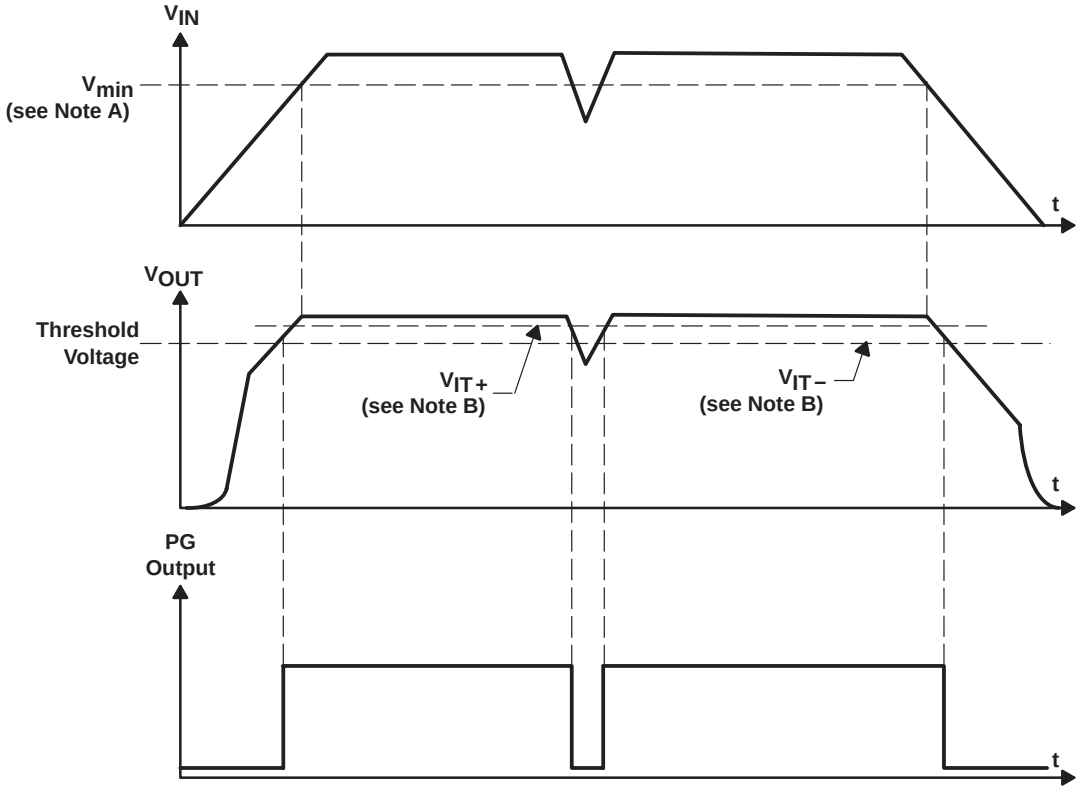
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	2		Ground
NC	3		No connection
OUT	5	O	The OUT terminal provides the regulated output voltage of the device.
PG	1	O	The PG terminal for the fixed voltage option devices is an open drain, active-high output that indicates the status of V_O (output of the LDO). When V_O exceeds approximately 90% of the regulated voltage, PG goes to a high impedance state. It goes to a low-impedance state when V_O falls below approximately 90% (i.e. overload condition) of the regulated voltage. The open drain output of the PG terminal requires a pullup resistor.
IN	4	I	The IN terminal is the power supply input to the device.

TPS797xx PG timing diagram



NOTES: A. $V_{min} = V_{OUT} + V_{DO}$
B. The PG trip voltage is typically 10% lower than the output voltage (90%V_O). V_{IT-} to V_{IT+} is the hysteresis voltage.

TYPICAL CHARACTERISTICS

TPS79733
OUTPUT VOLTAGE vs OUTPUT CURRENT

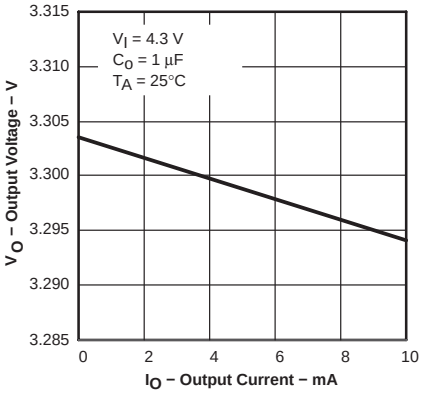


Figure 1

TPS79718
OUTPUT VOLTAGE vs OUTPUT CURRENT

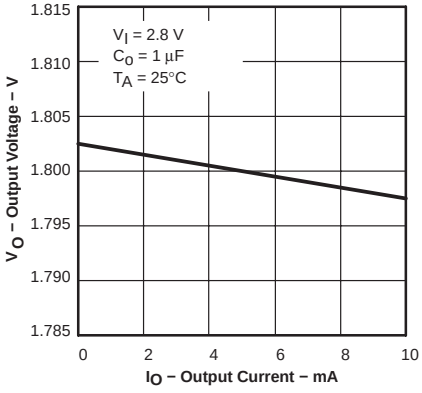


Figure 2

TPS79733
OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

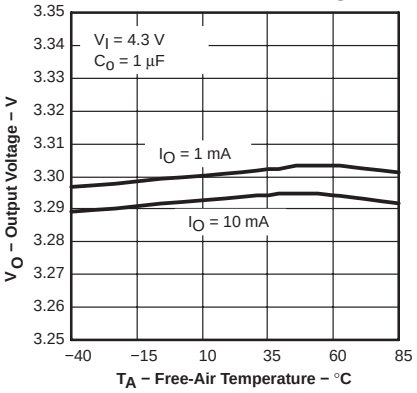


Figure 3

TPS79718
OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

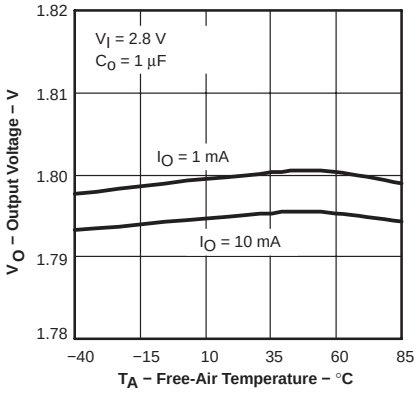


Figure 4

TPS79733
GROUND CURRENT vs FREE-AIR TEMPERATURE

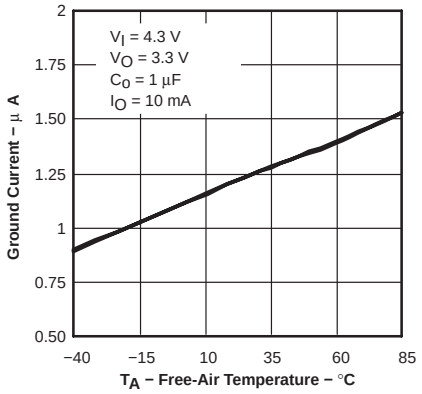


Figure 5

TPS79718
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

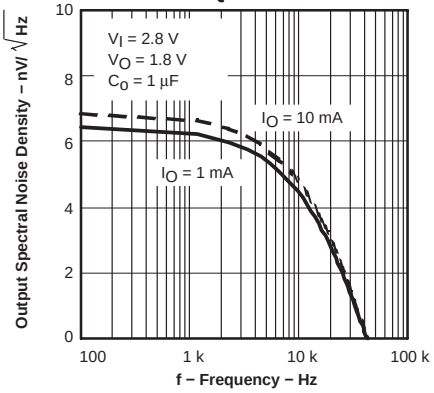


Figure 6

OUTPUT IMPEDANCE vs FREQUENCY

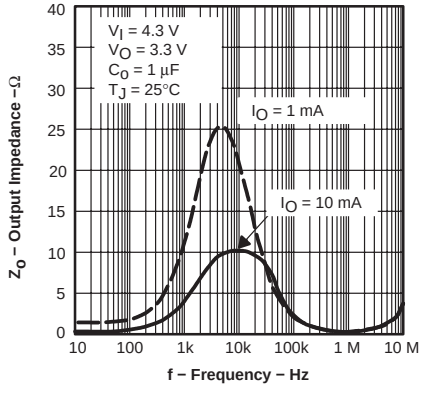


Figure 7

TPS79733
DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

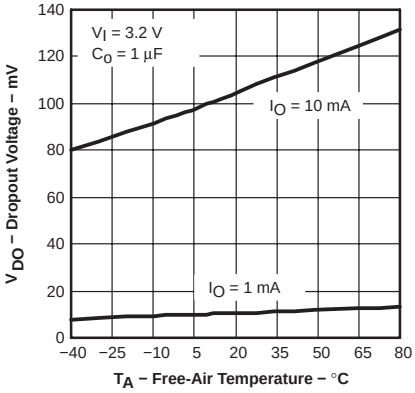


Figure 8

POWER UP / POWER DOWN

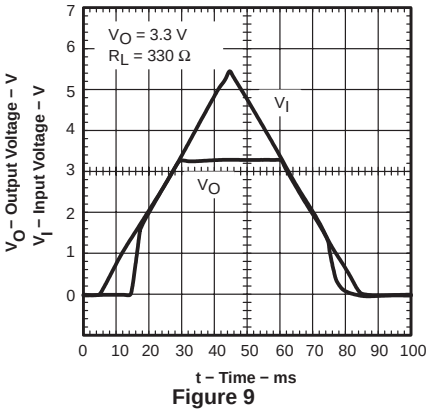


Figure 9

TYPICAL CHARACTERISTICS

TPS79718
LINE TRANSIENT RESPONSE

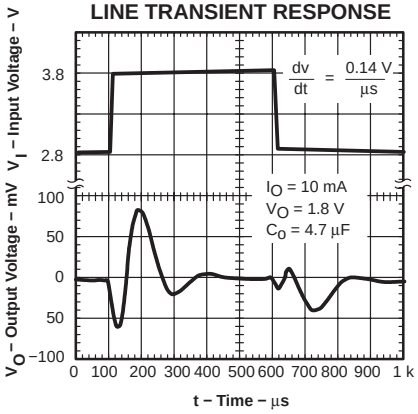


Figure 10

TPS79718
LOAD TRANSIENT RESPONSE

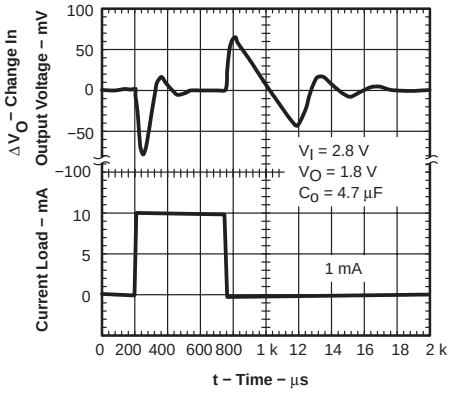


Figure 11

TPS79733
LINE TRANSIENT RESPONSE

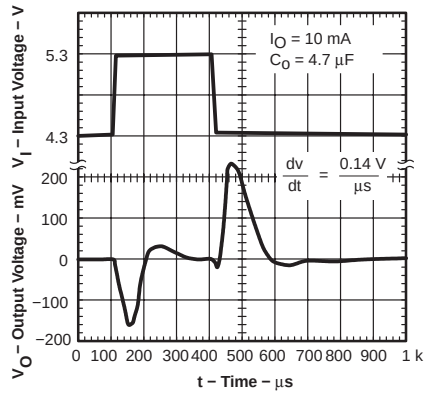


Figure 12

TPS79733
LOAD TRANSIENT RESPONSE

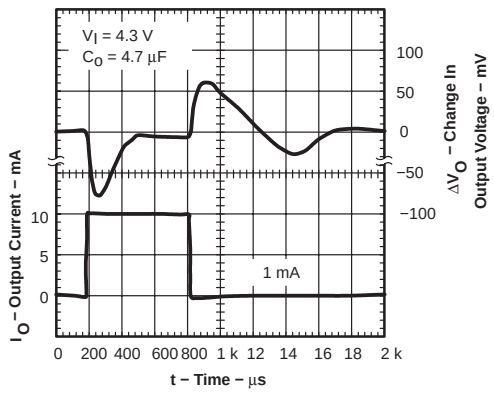


Figure 13

APPLICATION INFORMATION

The TPS797xx family of low-dropout (LDO) regulators have been optimized for use in micropower applications. They feature extremely low dropout voltages and ultralow quiescent current (1.2 μA typically).

A typical application circuit is shown in Figure 14.

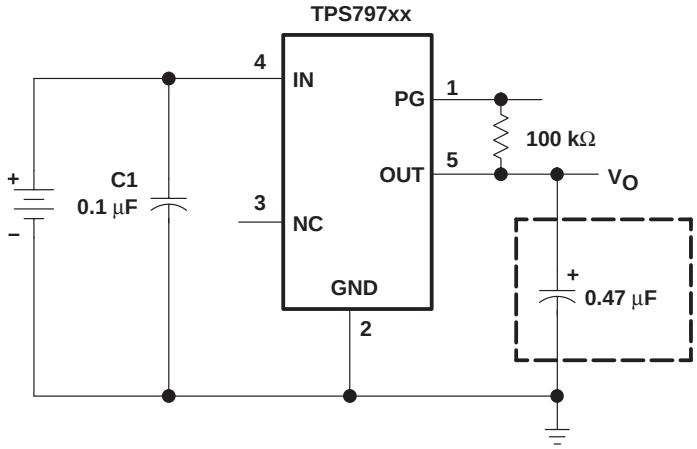


Figure 14. Typical Application Circuit

external capacitor requirements

Although not required, a 0.1-μF or larger input bypass capacitor, connected between IN and GND and located close to the TPS797xx, is recommended, especially when a highly resistive power supply is powering the LDO in addition to other devices.

Like all low-dropout regulators, the TPS797xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 0.47 μF. Any 0.47-μF capacitor is suitable. Capacitor values larger than 0.47 μF are acceptable.

APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; restrict the maximum junction temperature to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see Power Dissipation Rating Table).

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

regulator protection

The TPS797xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS797xx features internal current limiting. During normal operation, the TPS797xx limits output current to approximately 190 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

microcontroller application

One application for which this device is particularly suited is providing a regulated input voltage and power good (PG) supervisory signal to low-power devices such as mixed-signal microcontrollers. The quiescent or ground current of the TPS797xx family is typically 1.2 μA even at full load; therefore, the reduction in battery life by including the TPS797xx in the system is negligible. The primary benefits of using the TPS797xx to power low power digital devices include:

- Regulated output voltage that protects the device from battery droop and noise on the line (e.g., switch bounce)
- Smooth, monotonic power up
- PG signal for controlled device RESET
- Potential to use an existing 5-V power rail to power a 3.3-V or lower device
- Potential to provide separate digital and analog power and ground supplies for a system with only one power source

APPLICATION INFORMATION

microcontroller application (continued)

Figure 15 shows an application in which the TPS79718 is used to power Texas Instruments MSP430 mixed signal microcontroller.

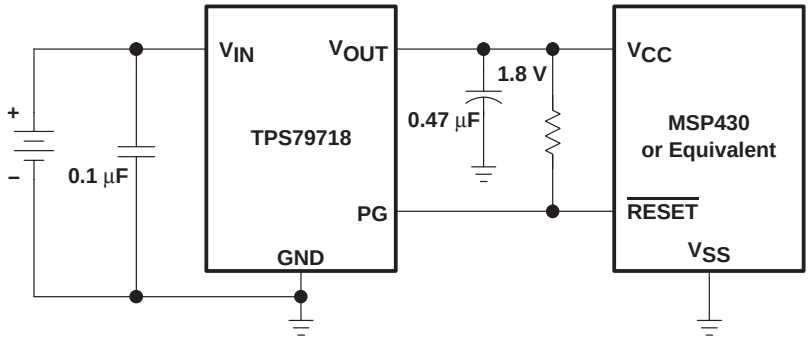


Figure 15. MSP430 Microcontroller Powered by the TPS79718 Regulator

Minimal board space is needed to accommodate the DCK (SC70/SOT-323) packaged TPS79718, the 0.1-μF output capacitor, the 0.47-μF input capacitor, and the pullup resistor on the PG pin.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79718QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QTD
TPS79718QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QTD
TPS79730QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QTE
TPS79730QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QTE
TPS79733QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QTF
TPS79733QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QTF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS797-Q1 :

- Catalog : TPS797

NOTE: Qualified Version Definitions:

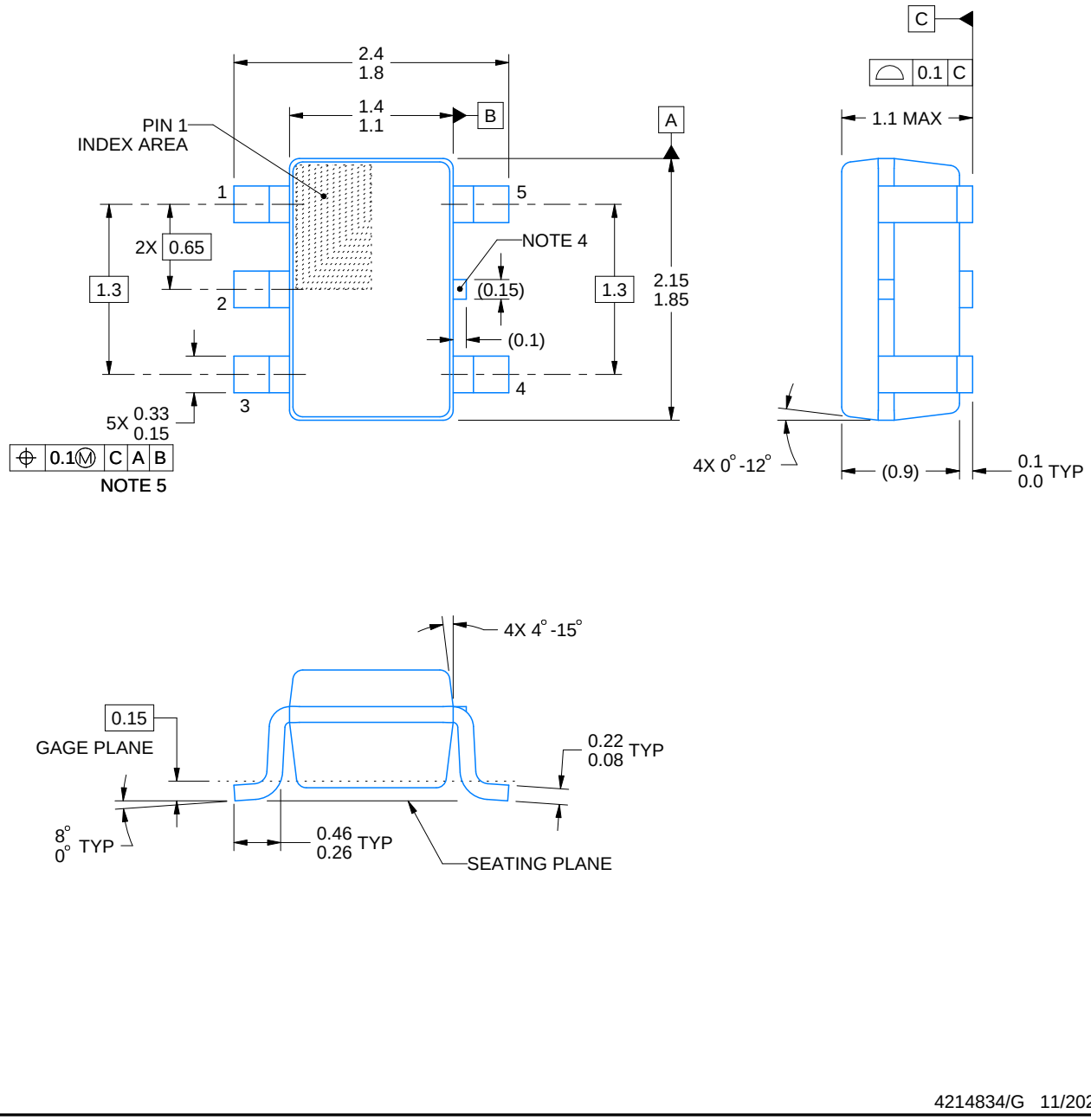
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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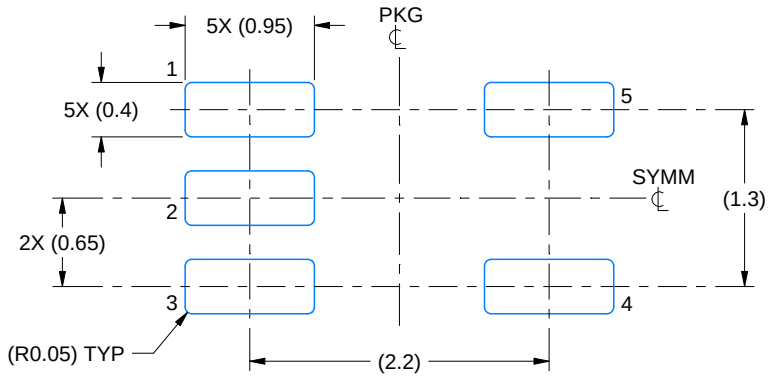
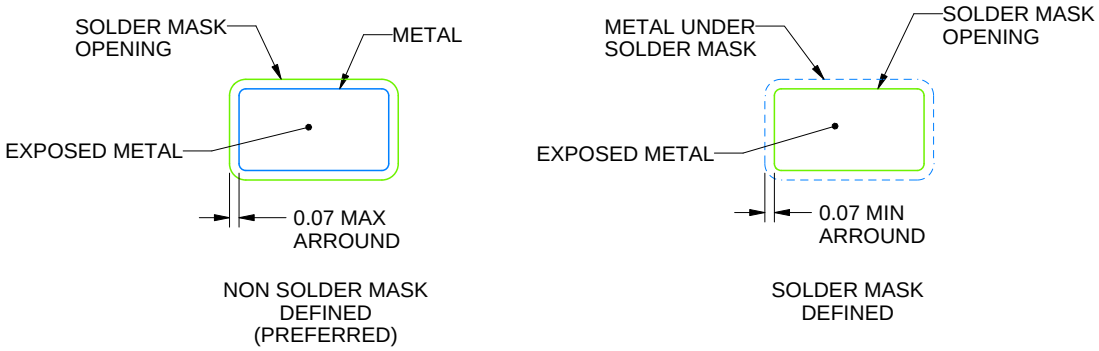
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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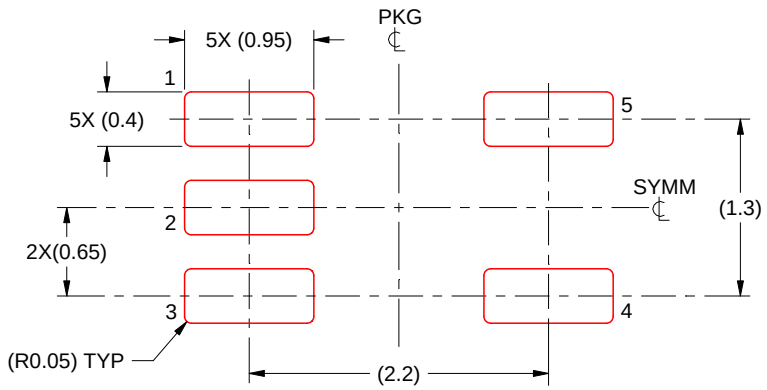
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265