TPS737-Q1 Automotive, 1A Low-Dropout Regulator With Reverse Current Protection

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4A
- Stable with 1µF or larger ceramic output capacitor
- Input voltage range: 2.2V to 5.5V
- Ultra-low dropout voltage: 130mV (typical) at 1A
- Excellent load transient response, even with only 1µF output capacitor
- NMOS topology delivers low reverse leakage current
- 1% initial accuracy
- 3% overall accuracy over line, load, and temperature
- Less than 20nA (typical) quiescent current in shutdown mode
- Thermal shutdown and current limit for fault protection
- Available in multiple output voltage versions

2 Applications

- Point of load regulation for DSPs, FPGAs, ASICs, and microprocessors
- Post-regulation for switching supplies
- Portable-, battery-powered equipment

3 Description

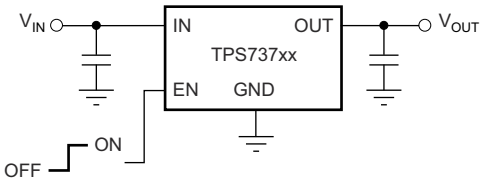
The TPS737-Q1 linear low-dropout (LDO) voltage regulator uses an n-type field effect transistor (NMOS) pass transistor in a voltage-follower configuration. This topology is relatively insensitive to output capacitor value and ESR, allowing a wide variety of load configurations. Load transient response is excellent, even with a small 1µF ceramic output capacitor. The NMOS topology also allows very low dropout.

The TPS737-Q1 uses an advanced bipolar complementary metal-oxide semiconductor (BiCMOS) process. This process yields high precision and delivers very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 20nA and is designed for portable applications. This device is protected by thermal shutdown and foldback current limit.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS737-Q1	DRB (VSON, 8)	3mm × 3mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configuration and Functions

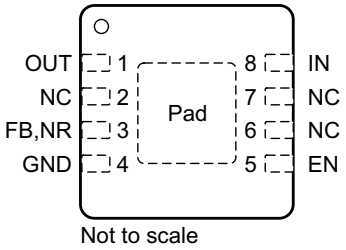


Figure 4-1. DRB Package, 8-Pin VSON (Top View)

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the *Enable Pin and Shutdown* section for more details. Do not leave EN floating. Connect EN to IN if this pin is not used.
FB	3	I	Adjustable voltage version only. This pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	4, Pad	G	Ground
IN	8	I	Unregulated input supply
NR	3	—	Fixed voltage versions only. Connecting an external capacitor to this pin bypasses noise generated by the internal band-gap, reducing output noise to very low levels.
OUT	1	O	Regulator output. A 1µF or larger capacitor of any type is required for stability.
NC	2, 6, 7	—	No internal connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	6	
	Output, V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.2		5.5	V
I_{OUT}	Output current	0		1	A
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS737-Q1 New silicon	TPS737-Q1 Legacy silicon	UNIT
		DRB (VSON)	DRB (VSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.4	52.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.6	59.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	19.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	19.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	11.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

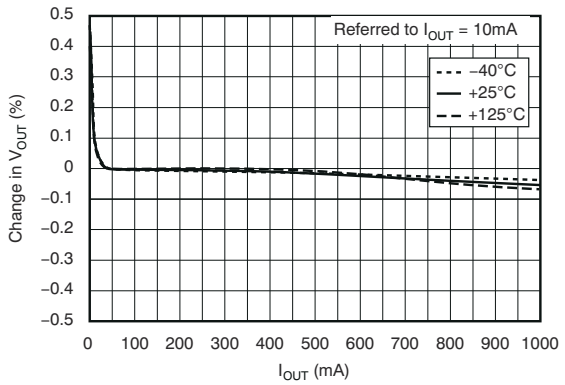
Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1V(1) , I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF (unless otherwise noted). Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1) (2)			2.2		5.5	V
V_{FB}	Internal reference	T_J = 25°C		1.192	1.204	1.216	V
V_{OUT}	Output voltage range (TPS73701)(3)			V_{FB}		5.5 - V_{DO}	V
	Accuracy(1) (4)	Nominal	T_J = 25°C	–1		1	%
			5.36V < V_{IN} < 5.5V, V_{OUT} = 5.08V, 10mA < I_{OUT} < 800mA, –40°C < T_J < 85°C, TPS73701, legacy silicon	–2		2	
		over V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 1A, legacy silicon	–3	±0.5	3	
			V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 1A, new silicon	–1.5	±0.5	1.5	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation (1)	$V_{OUT(nom)}$ + 0.5V ≤ V_{IN} ≤ 5.5V			0.01		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 1A			0.002		%/mA
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	10mA ≤ I_{OUT} ≤ 1 A			0.0005		%/mA
V_{DO}	Dropout voltage(5) (V_{IN} = $V_{OUT(nom)}$ - 0.1V)	I_{OUT} = 1A			130	500	mV
$Z_{O(DO)}$	Output impedance in dropout	2.2V ≤ V_{IN} ≤ V_{OUT} + V_{DO}			0.25		Ω
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$		1.05	1.6	2.2	A
I_{SC}	Short-circuit current	V_{OUT} = 0V			450		mA
I_{REV}	Reverse leakage current(6) (-I_{IN})	V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT}			0.1		µA
I_{GND}	Ground pin current	I_{OUT} = 10mA (I_Q)			400		µA
I_{GND}	Ground pin current	I_{OUT} = 1A, legacy silicon			1300		µA
I_{GND}	Ground pin current	I_{OUT} = 1A, new silicon			880		µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V			20		nA
I_{FB}	Feedback pin current				0.1	0.6	µA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100Hz, I_{OUT} = 1A			58		dB
		f = 10kHz, I_{OUT} = 1A			37		
V_N	Output noise voltage, BW = 10Hz to 100kHz	C_{OUT} = 10µF			27 x V_{OUT}		μV_{RMS}
t_{STR}	Startup time	V_{OUT} = 3V, R_L = 30Ω, C_{OUT} = 1µF			600		µs
$V_{EN(high)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)			0		0.5	V
I_{EN}	Enable pin current (enabled)	V_{EN} = 5.5V			20		nA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		
T_J	Operating junction temperature			–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.2V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6V, when V_{IN} ≤ 1.6V, the output locks to V_{IN} and may result in a damaging over-voltage condition on the output. To avoid this situation, disable the device before powering down V_{IN}. (Legacy silicon only)
(3) TPS73701-Q1 is tested at V_{OUT} = 1.2V.
(4) Tolerance of external resistors not included in this specification.
(5) V_{DO} is not measured for output versions with $V_{OUT(nom)}$ < 2.3V, because minimum V_{IN} = 2.2V.
(6) Fixed-voltage versions only; refer to *Application Information* section for more information.

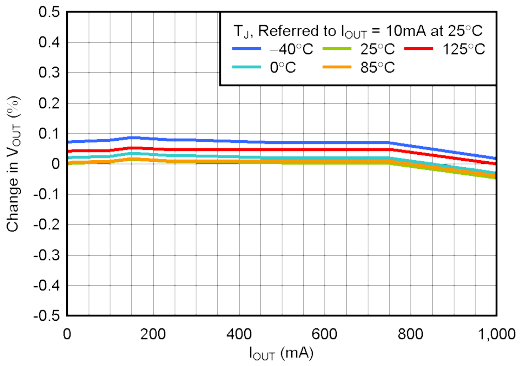
5.6 Typical Characteristics

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1V), I_{OUT} = 10mA, V_{EN} = 2.2V, C_{OUT} = 2.2µF (unless otherwise noted)



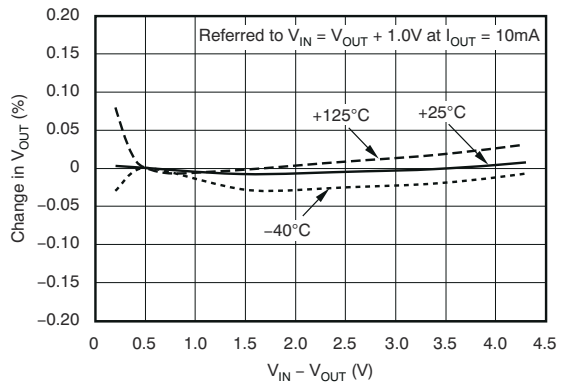
Legacy silicon

Figure 5-1. Load Regulation



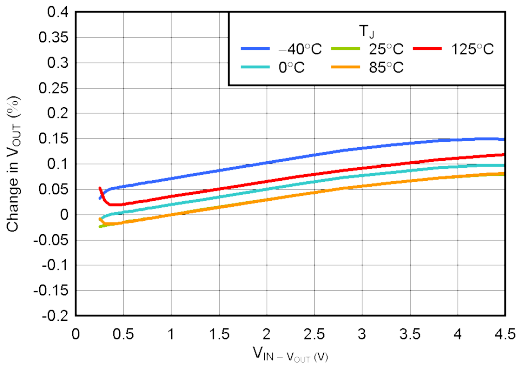
New silicon

Figure 5-2. Load Regulation



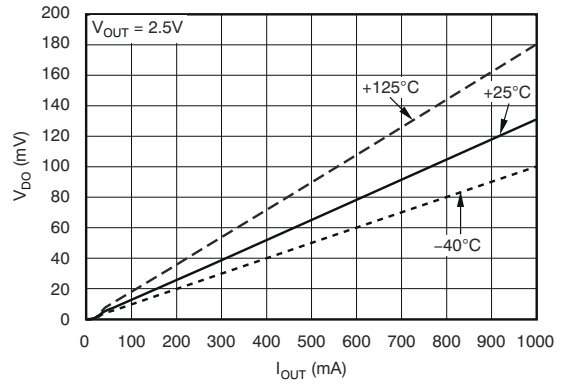
Legacy silicon

Figure 5-3. Line Regulation



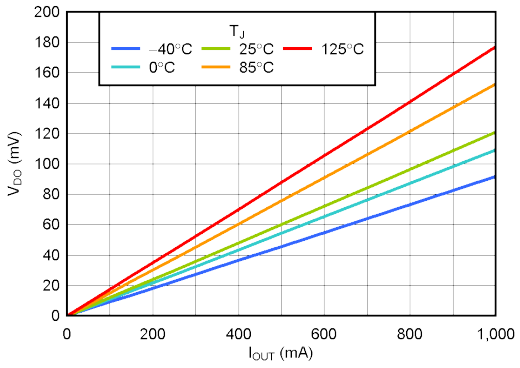
New silicon

Figure 5-4. Line Regulation



Legacy silicon

Figure 5-5. Dropout Voltage vs Output Current

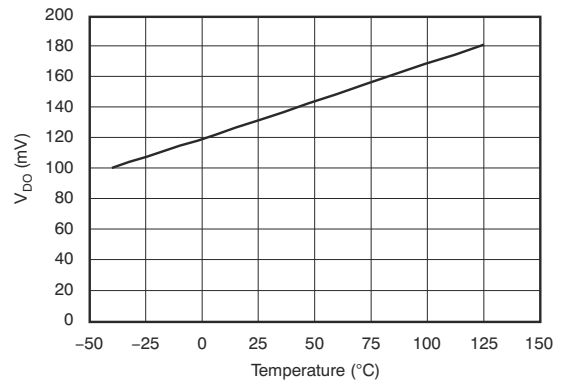


New silicon

Figure 5-6. Dropout Voltage vs Output Current

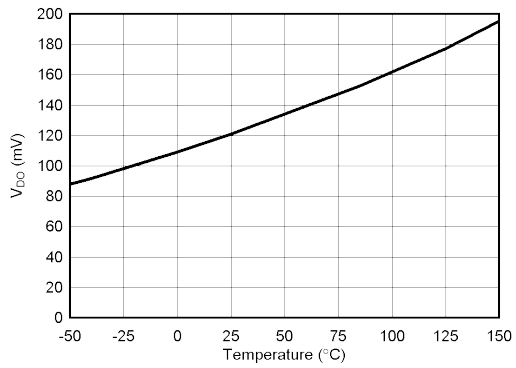
5.6 Typical Characteristics (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1V), I_{OUT} = 10mA, V_{EN} = 2.2V, C_{OUT} = 2.2µF (unless otherwise noted)



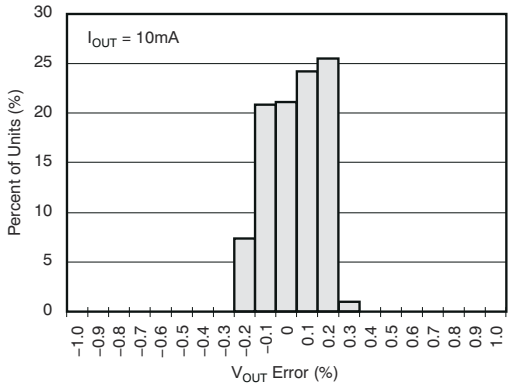
Legacy silicon

Figure 5-7. Dropout Voltage vs Temperature



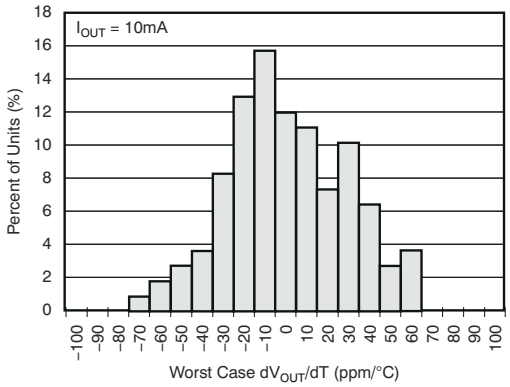
New silicon

Figure 5-8. Dropout Voltage vs Temperature



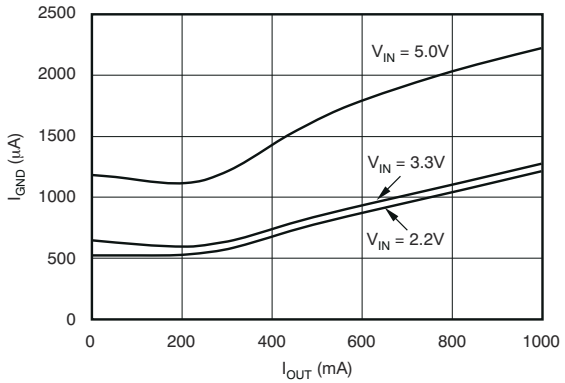
Legacy silicon

Figure 5-9. Output Voltage Histogram



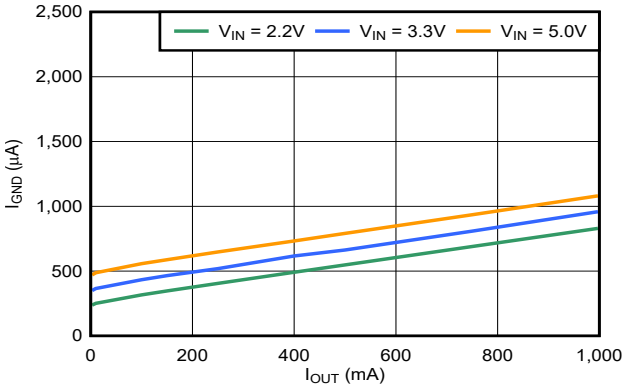
Legacy silicon

Figure 5-10. Dropout Voltage Drift Histogram



Legacy silicon

Figure 5-11. Ground Pin Current vs Output Current

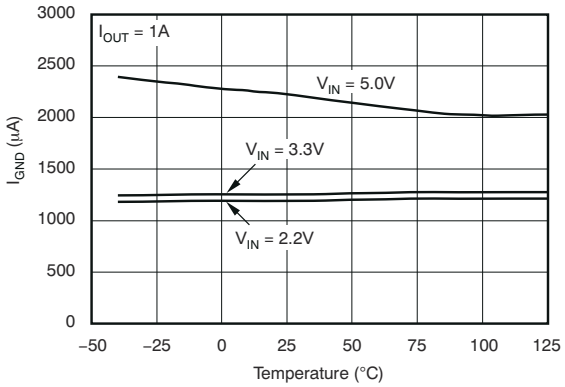


New silicon

Figure 5-12. Ground Pin Current vs Output Current

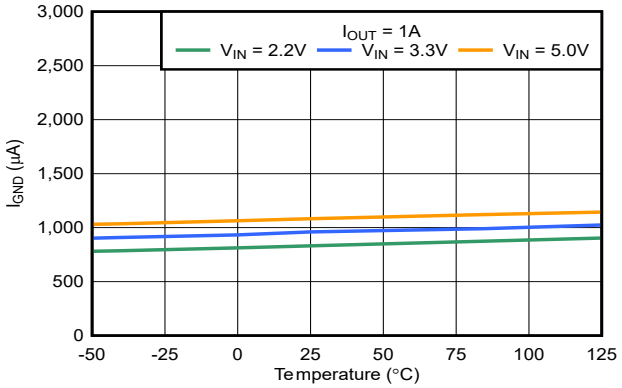
5.6 Typical Characteristics (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1V), I_{OUT} = 10mA, V_{EN} = 2.2V, C_{OUT} = 2.2µF (unless otherwise noted)



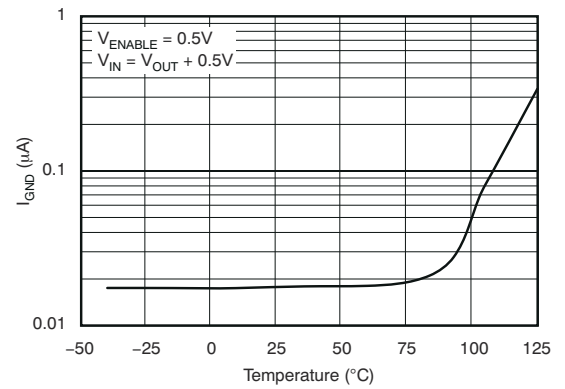
Legacy silicon

Figure 5-13. Ground Pin Current vs Temperature



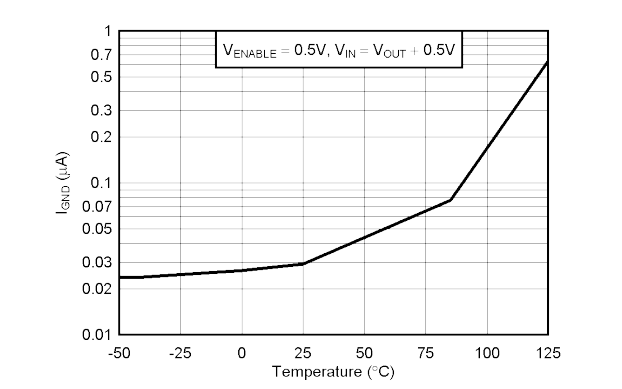
New silicon

Figure 5-14. Ground Pin Current vs Temperature



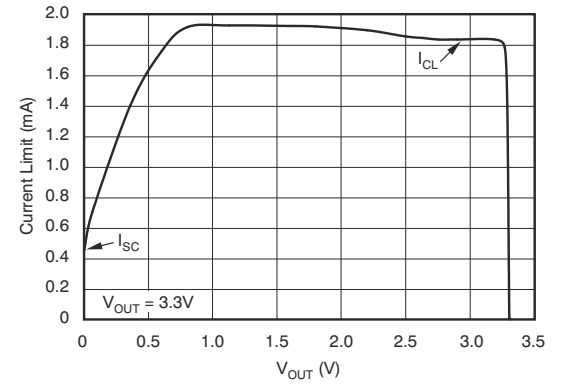
Legacy silicon

Figure 5-15. Ground Pin Current In Shutdown vs Temperature



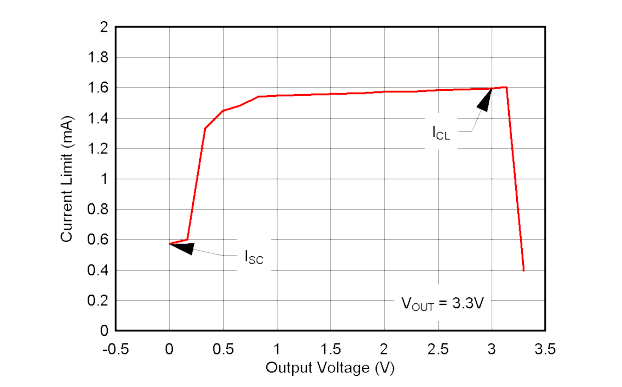
New silicon

Figure 5-16. Ground Pin Current in Shutdown vs Temperature



Legacy silicon

Figure 5-17. Current Limit vs V_{OUT} (Foldback)

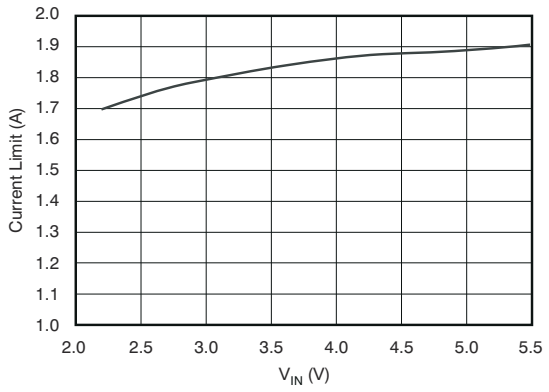


New silicon

Figure 5-18. Current Limit vs V_{OUT} (Foldback)

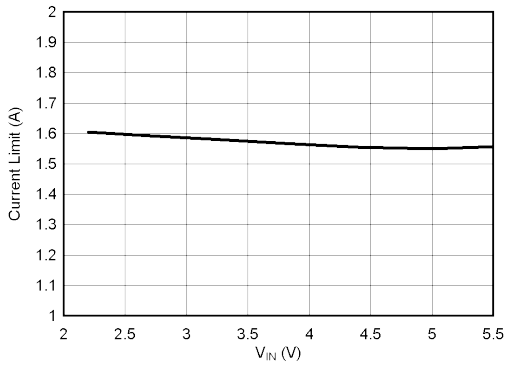
5.6 Typical Characteristics (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1V), I_{OUT} = 10mA, V_{EN} = 2.2V, C_{OUT} = 2.2µF (unless otherwise noted)



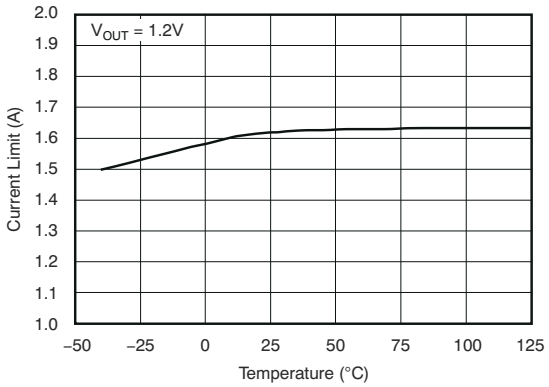
Legacy silicon

Figure 5-19. Current Limit vs V_{IN}



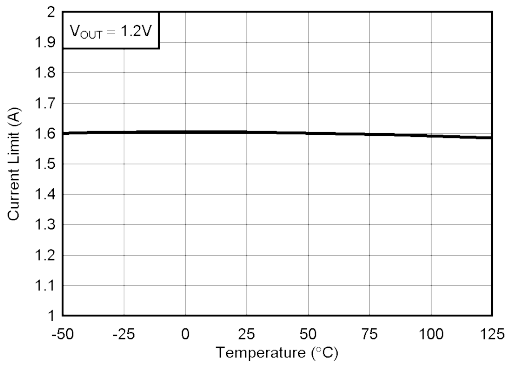
New silicon

Figure 5-20. Current Limit vs V_{IN}



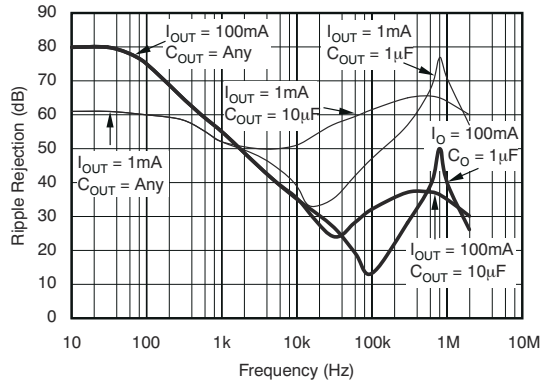
Legacy silicon

Figure 5-21. Current Limit vs Temperature



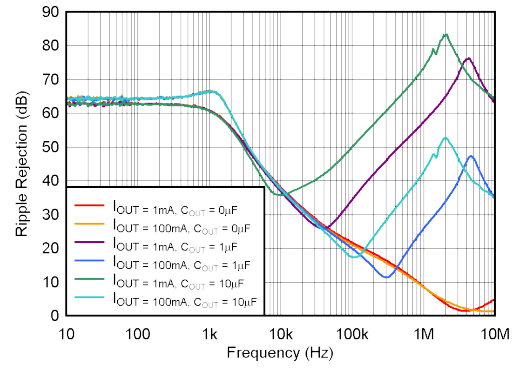
New silicon

Figure 5-22. Current Limit vs Temperature



Legacy silicon

Figure 5-23. PSRR (Ripple Rejection) vs Frequency

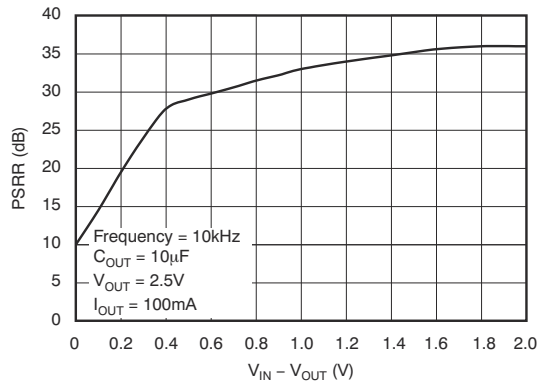


New silicon

Figure 5-24. PSRR (Ripple Rejection) vs Frequency

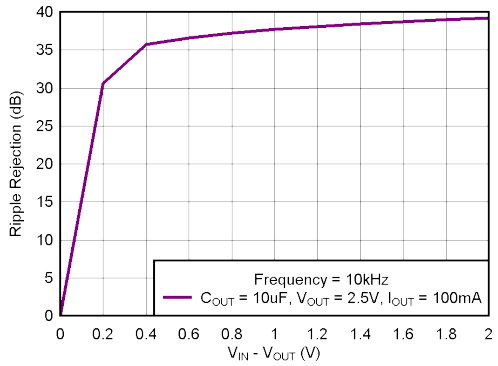
5.6 Typical Characteristics (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1V), I_{OUT} = 10mA, V_{EN} = 2.2V, C_{OUT} = 2.2µF (unless otherwise noted)



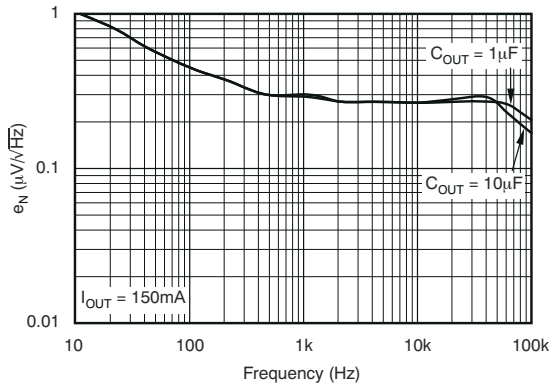
Legacy silicon

Figure 5-25. PSRR (Ripple Rejection) vs V_{IN} – V_{OUT}



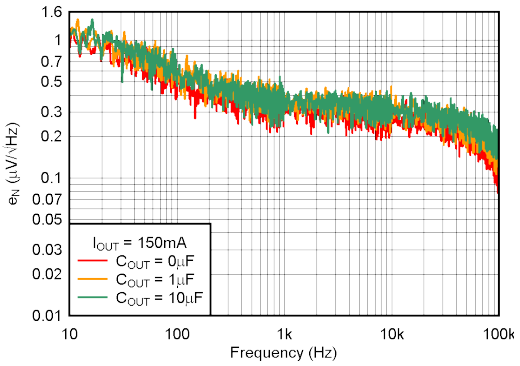
New silicon

Figure 5-26. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})



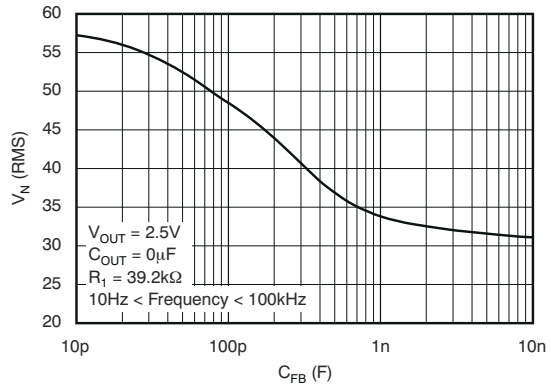
Legacy silicon

Figure 5-27. Noise Spectral Density



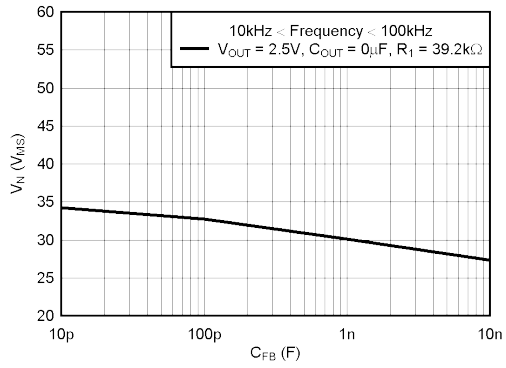
New silicon

Figure 5-28. Noise Spectral Density



Legacy silicon

Figure 5-29. TPS73701-Q1 RMS Noise Voltage vs C_{FB}

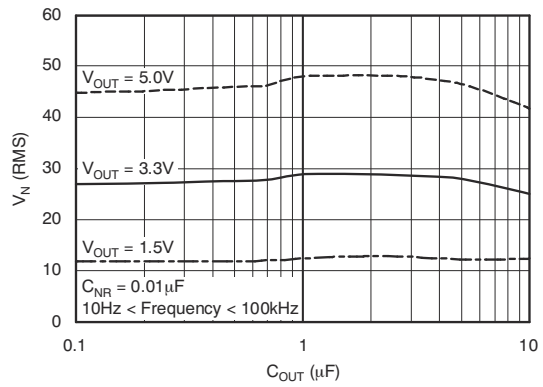


New silicon

Figure 5-30. TPS73701-Q1 RMS Noise Voltage vs C_{FB}

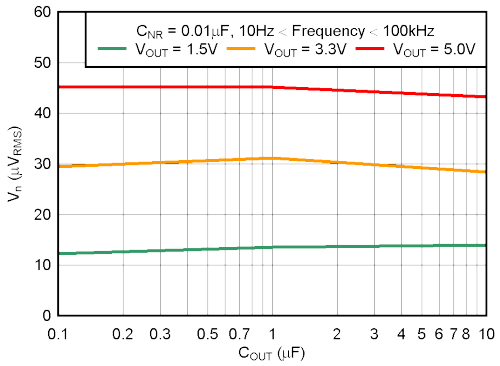
5.6 Typical Characteristics (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1V), I_{OUT} = 10mA, V_{EN} = 2.2V, C_{OUT} = 2.2µF (unless otherwise noted)



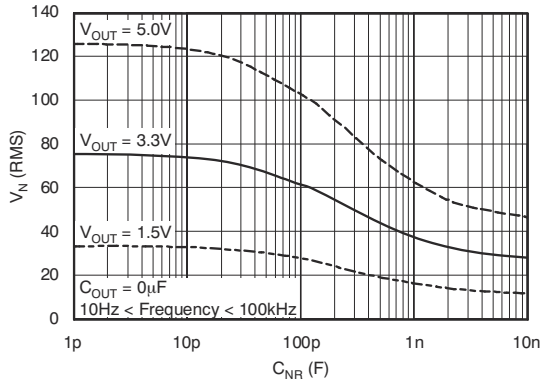
Legacy silicon

Figure 5-31. RMS Noise Voltage vs C_{OUT}



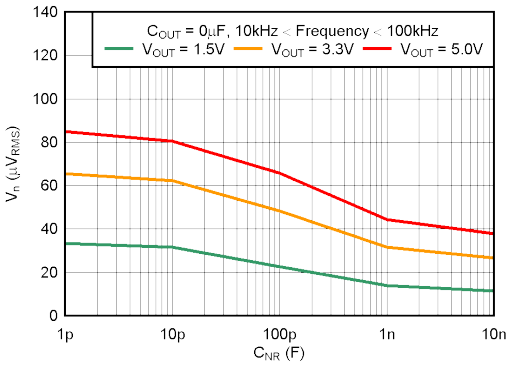
New silicon

Figure 5-32. RMS Noise Voltage vs C_{OUT}



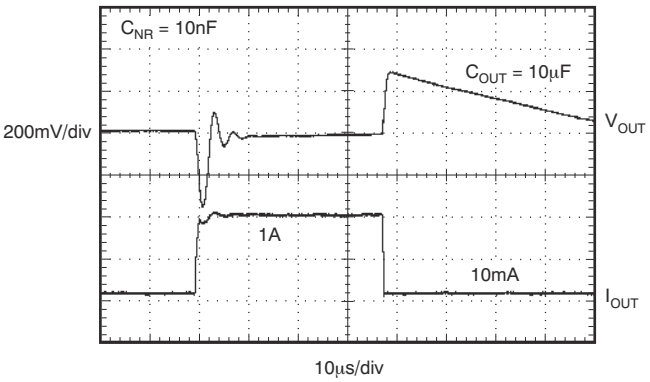
Legacy silicon

Figure 5-33. RMS Noise Voltage vs C_{NR}



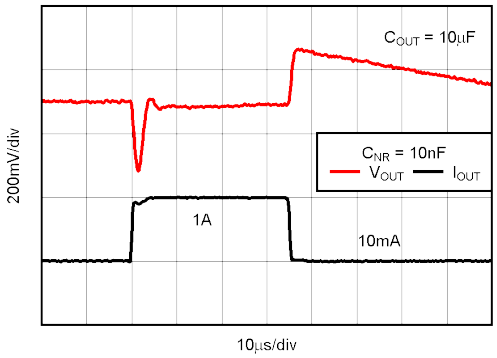
New silicon

Figure 5-34. RMS Noise Voltage vs C_{NR}



Legacy silicon

Figure 5-35. TPS73733-Q1 Load Transient Response

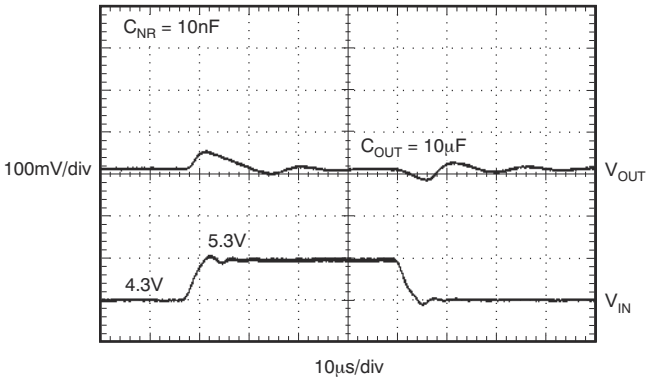


New silicon

Figure 5-36. TPS73733-Q1 Load Transient Response

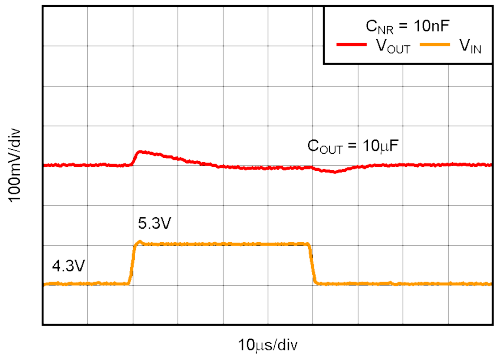
5.6 Typical Characteristics (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1V), I_{OUT} = 10mA, V_{EN} = 2.2V, C_{OUT} = 2.2µF (unless otherwise noted)



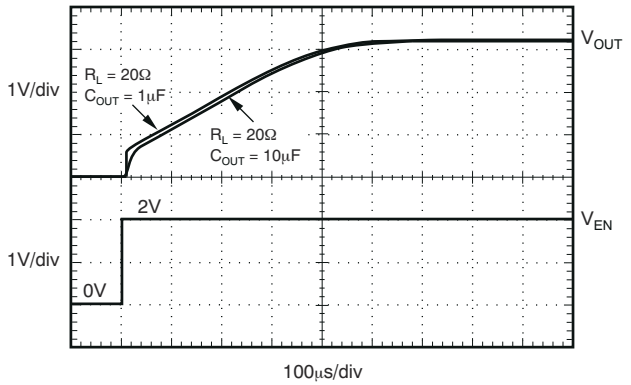
Legacy silicon

Figure 5-37. TPS73733-Q1 Line Transient Response



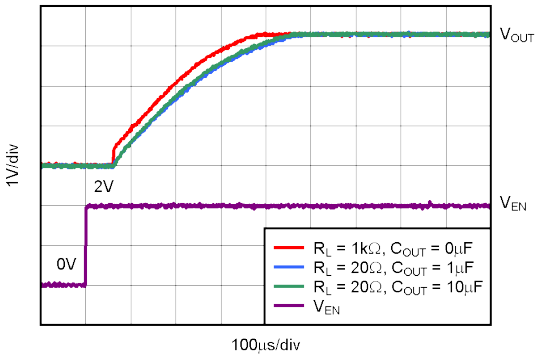
New silicon

Figure 5-38. TPS73733-Q1 Line Transient Response



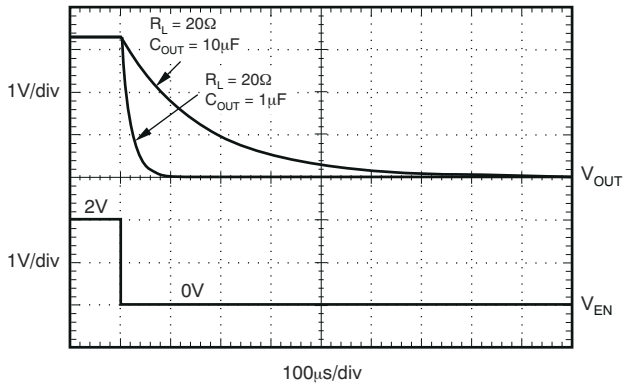
Legacy silicon

Figure 5-39. TPS73701-Q1 Turn-On Response



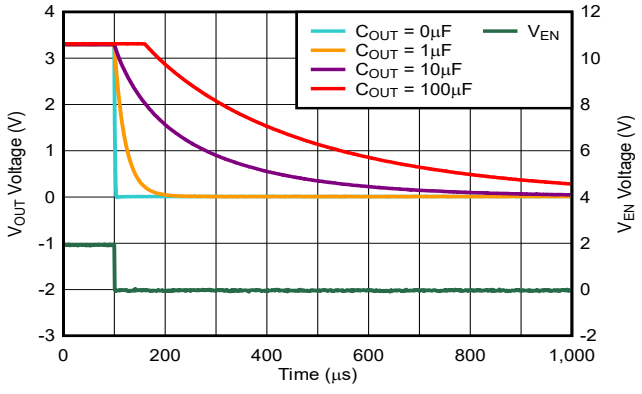
New silicon

Figure 5-40. TPS73701-Q1 Turn-On Response



Legacy silicon

Figure 5-41. TPS73701-Q1 Turn-Off Response

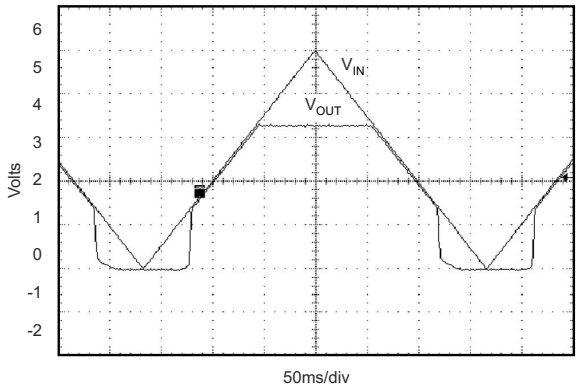


New silicon

Figure 5-42. TPS73701-Q1 Turn-Off Response

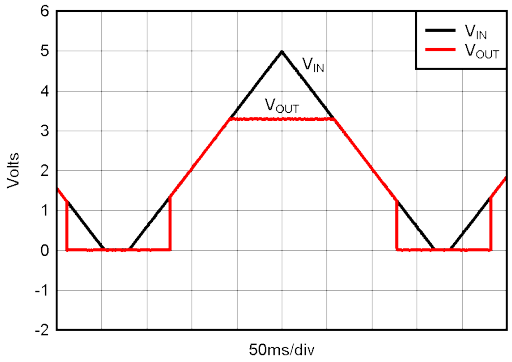
5.6 Typical Characteristics (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1V), I_{OUT} = 10mA, V_{EN} = 2.2V, C_{OUT} = 2.2µF (unless otherwise noted)



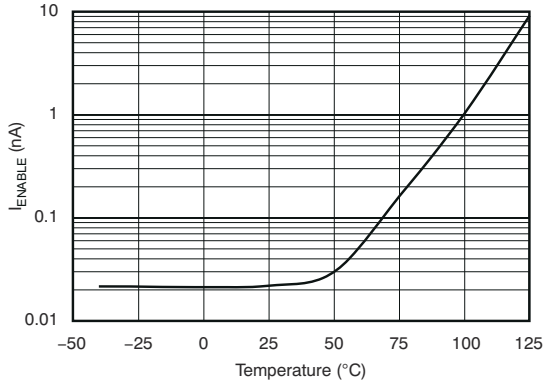
Legacy silicon

Figure 5-43. TPS73701-Q1, V_{OUT} = 3.3V Power-Up And Power-Down



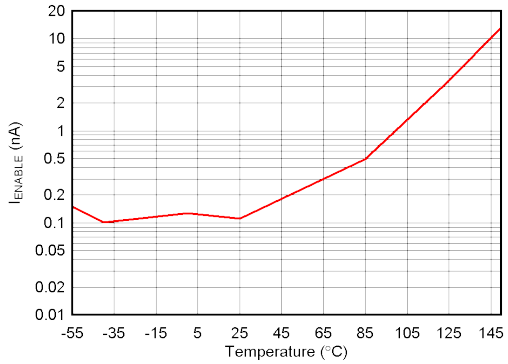
New silicon

Figure 5-44. TPS73701-Q1, V_{OUT} = 3.3V Power-Up and Power-Down



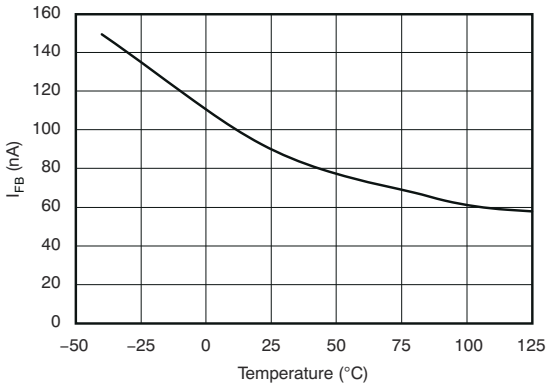
Legacy silicon

Figure 5-45. I_{ENABLE} vs Temperature



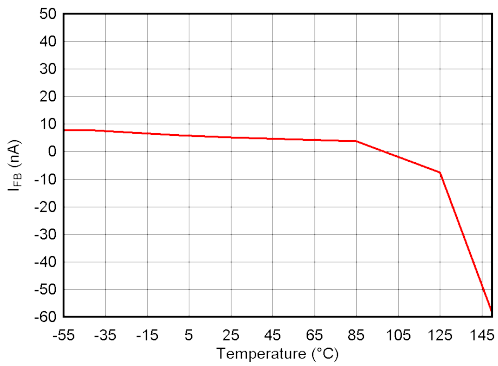
New silicon

Figure 5-46. I_{EN} vs Temperature



Legacy silicon

Figure 5-47. TPS73701-Q1 I_{FB} vs Temperature

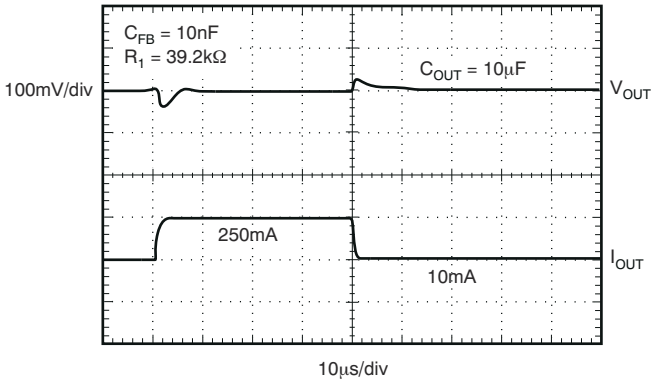


New silicon

Figure 5-48. TPS73701-Q1 I_{FB} vs Temperature

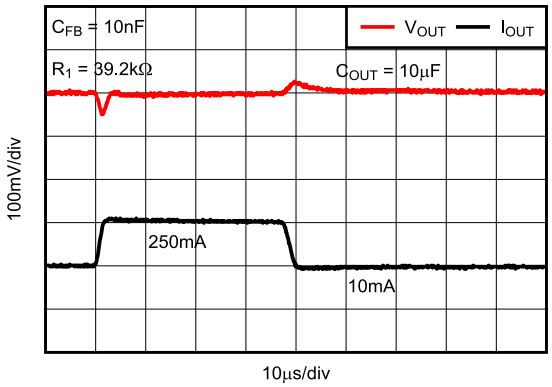
5.6 Typical Characteristics (continued)

T_J = 25°C, V_{IN} = ($V_{OUT(nom)}$ + 1V), I_{OUT} = 10mA, V_{EN} = 2.2V, C_{OUT} = 2.2µF (unless otherwise noted)



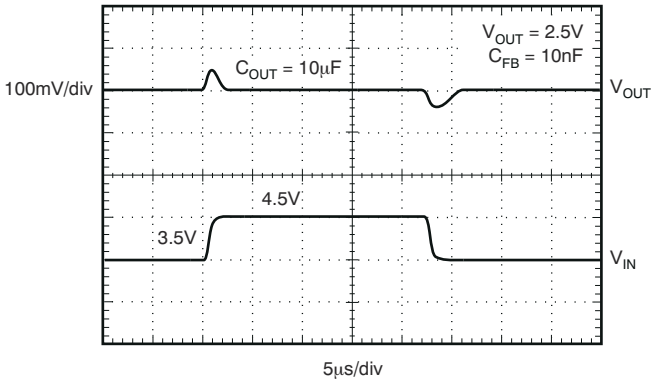
Legacy silicon

Figure 5-49. TPS73701-Q1 Load Transient, Adjustable Version



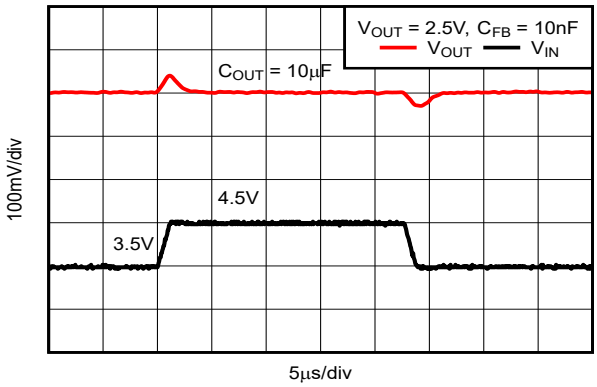
New silicon, C_{OUT} = 10µF tantalum

Figure 5-50. TPS73701-Q1 Load Transient, Adjustable Version



Legacy silicon

Figure 5-51. TPS73701-Q1 Line Transient, Adjustable Version



New silicon, C_{OUT} = 10µF tantalum

Figure 5-52. TPS73701-Q1 Line Transient, Adjustable Version

6 Detailed Description

6.1 Overview

The TPS737-Q1 is a low-dropout (LDO) regulator that uses an n-type field effect transistor (NMOS) pass transistor. This transistor achieves ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features combined with an enable input make the TPS737-Q1 designed for portable applications. This regulator offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and overcurrent protection, including foldback current limit.

Table 6-1 lists the common output voltages for standard 1% resistors.

Table 6-1. Standard 1% Resistor Values for Common Output Voltages

V_{OUT} (1)	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3V	46.4kΩ	33.2kΩ
3.3V	52.3kΩ	30.1kΩ

(1) $V_{OUT} = (R_1 + R_2) / R_2 \times 1.204$. $R_1 \parallel R_2 \cong 19k\Omega$ for best accuracy.

6.2 Functional Block Diagrams

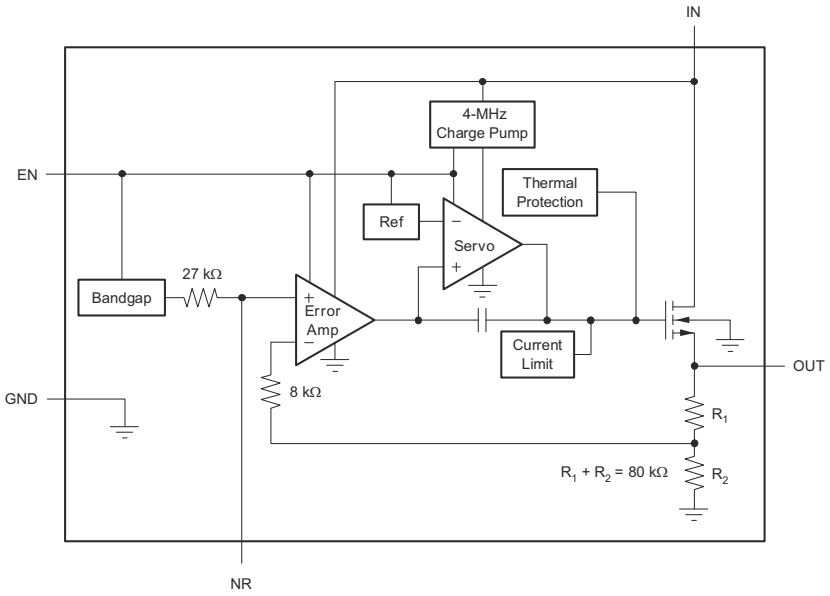
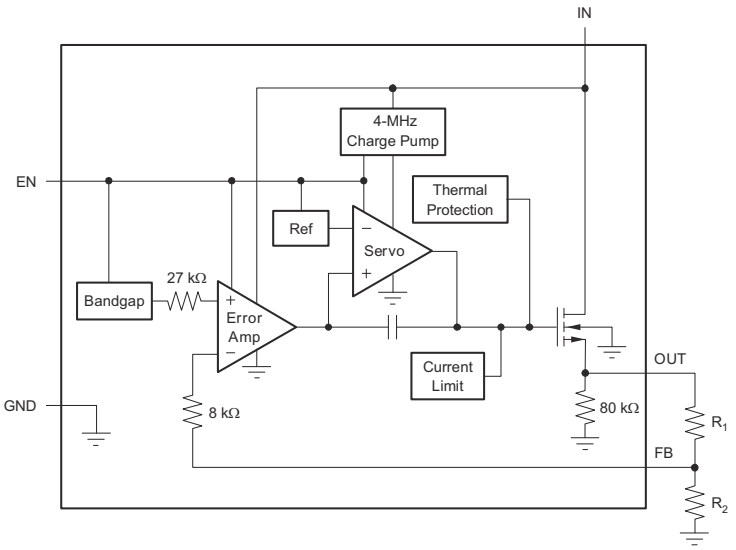


Figure 6-1. Fixed Voltage Version



See Table 6-1 for standard resistor values.

Figure 6-2. Adjustable Voltage Version

6.3 Feature Description

6.3.1 Output Noise

A precision band-gap reference is used to generate the internal reference voltage (V_{REF}). This reference is the dominant noise source within the TPS737-Q1 and generates approximately 32μV_{RMS} (10Hz to 100kHz) at the reference output (NR). The regulator control loop adds gain to the reference noise with the same gain as the reference voltage. Thus, the noise voltage of the regulator is approximately given by Equation 1.

$$V_N = 32\,\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\,\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \tag{1}$$

Because the value of V_{REF} is 1.2V, this relationship reduces to the following equation when C_{NR} is not used.

$$V_N\,(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}\,(V) \tag{2}$$

To form a low-pass filter for the voltage reference, connect an external noise-reduction capacitor (C_{NR}) from NR to ground (C_{NR}). An internal 27kΩ resistor is in series with the voltage reference and the noise-reduction pin (NR). The total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of approximately 3.2 for C_{NR} = 10nF. Thus, giving the approximate relationship for C_{NR} = 10nF in Equation 3.

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \tag{3}$$

This noise reduction effect is given in Figure 5-33.

The TPS737-Q1 uses an internal charge pump to develop an internal supply voltage. The supply voltage created is sufficient to drive the gate of the NMOS pass transistor above V_{OUT}. The charge pump generates approximately 250μV of switching noise at approximately 4MHz. However, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

6.3.2 Internal Current Limit

The TPS737-Q1 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See Figure 5-17.

6.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5V (maximum) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate. A V_{EN} above 1.7V (minimum) turns the regulator on and the output ramps back up to a regulated V_{OUT} (see Figure 5-39).

When shutdown capability is not required, connect EN to V_{IN}. However, the gate of the pass transistor potentially cannot be discharged using this configuration. Thus, the pass transistor is potentially left on (enhanced) for a significant time after removing V_{IN}. This scenario results in reverse current flow (if the IN pin is low impedance) and faster ramp times at power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output potentially overshoots at power-up.

6.3.4 Reverse Current

The NMOS pass transistor provides inherent protection against current flow from the regulator output to the input when the pass transistor gate is pulled low. To make sure all charge is removed from the gate of the pass transistor, drive the EN pin low before the input voltage is removed. If this step is not done, the pass transistor is potentially left on because of stored charge on the gate.

After the EN pin is driven low, no bias voltage is required on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin because of voltage applied on the OUT pin. There is additional current flowing into the OUT pin as a result of the 80kΩ internal resistor divider to ground (see Figure 6-1 and Figure 6-2).

For the TPS73701-Q1, reverse current potentially flows when V_{FB} is more than 1V above V_{IN}.

6.3.5 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit cycles on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage resulting from overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. Limit junction temperature to 125°C maximum for reliable operation. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. Trigger thermal protection at least 35°C above the maximum expected ambient condition of the application for good reliability. This limitation produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS737-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS737-Q1 into thermal shutdown degrades device reliability.

6.4 Device Functional Modes

Driving the EN pin over 1.7V turns on the regulator. Driving the EN below 0.5V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is reduced to 20nA (typical).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS737-Q1 LDO regulator uses an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS737-Q1 designed for portable applications.

7.2 Typical Application

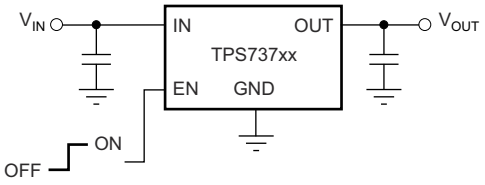


Figure 7-1. Typical Application Circuit For Fixed-Voltage Versions

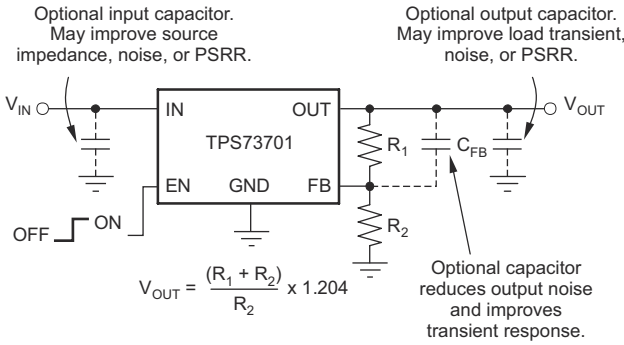


Figure 7-2. Typical Application Circuit For Adjustable-Voltage Version

7.2.1 Design Requirements

Calculate R_1 and R_2 for any output voltage using the formula in Figure 7-2. Sample resistor values for common output voltages are listed in Table 6-1.

Make the parallel combination of R_1 and R_2 approximately equal to 19kΩ for best accuracy. This 19kΩ, in addition to the internal 8kΩ resistor, presents the same impedance to the error amplifier as the 27kΩ band-gap reference output. This impedance helps compensate for leakages into the error amplifier terminals.

The TPS73701-Q1 adjustable version does not have the NR pin available. However, connecting a feedback capacitor (C_{FB}) from the output to the feedback pin (FB) reduces output noise and improves load transient performance. Limit this capacitor to 0.1µF.

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

An input capacitor is not required for stability. However, if input impedance is very low, connect a 0.1µF to 1µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A

higher-value capacitor is potentially necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source.

The TPS737-Q1 requires a 1µF output capacitor for stability. The device is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing potentially occurs when the product of C_{OUT} and total ESR drops below 50nF × Ω. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.2.2.2 Dropout Voltage

The TPS737-Q1 uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass transistor is in the linear region of operation. In this case, the input-to-output resistance is the $R_{DS(ON)}$ of the NMOS pass transistor.

The TPS737-Q1 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response for large step changes in load current. The boundary of this transient dropout region is approximately twice the DC dropout. Values of V_{IN} – V_{OUT} above this line provide normal transient response.

Operating in the transient dropout region causes an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of change in load current rate. This time is also determined by the rate of change in load current and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions, the TPS737-Q1 potentially takes a couple of hundred microseconds to return to the specified regulation accuracy. Worst-case conditions are determined by the full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to DC dropout levels.

7.2.2.3 Transient Response

The low open-loop output impedance provided by the NMOS pass transistor in a voltage follower configuration allows operation without a 1µF output capacitor. As with any regulator, the addition of additional capacitance from the OUT pin to ground reduces undershoot magnitude but increases duration. In the adjustable version, the addition of a capacitor (C_{FB}) between the OUT pin and the FB pin also improves transient response.

The TPS737-Q1 does not have an active pulldown when the output is overvoltage. This architecture allows for applications that connect higher voltage sources, such as alternate power supplies, to be connected to the output. This architecture results in an output overshoot of several percent if load current quickly drops to zero when a capacitor is connected to the output. Reduce the duration of overshoot by adding a load resistor. The overshoot decays at a rate determined by the output capacitor (C_{OUT}) and the internal and external load resistance. The rate of decay is given by Equation 4 and Equation 5.

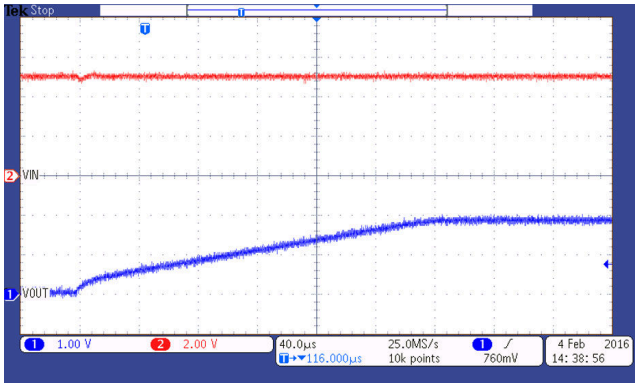
(Fixed voltage version):

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable voltage version):

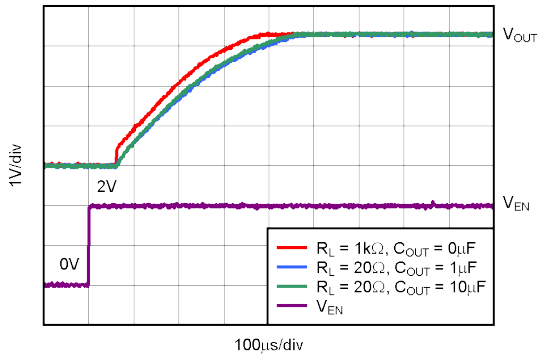
$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

7.2.3 Application Curves



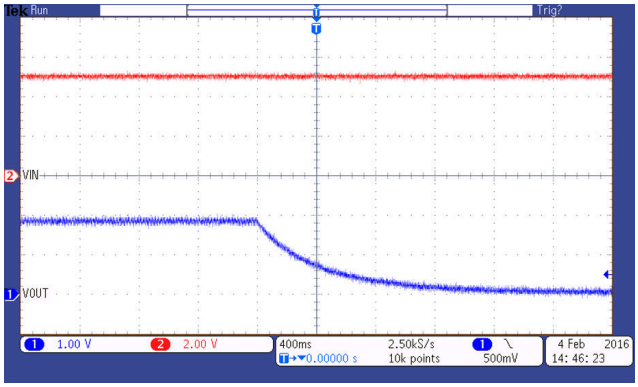
Legacy silicon

Figure 7-3. TPS737-Q1 Start-Up



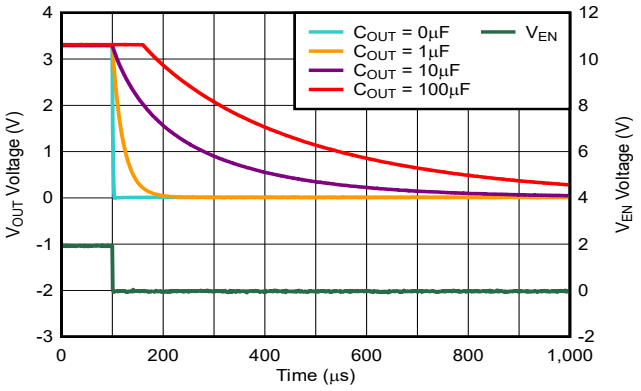
New silicon

Figure 7-4. TPS73701-Q1 Turn-On Response



Legacy silicon

Figure 7-5. TPS737-Q1 Shutdown



New silicon

Figure 7-6. TPS73701-Q1 Turn-Off Response

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.2V to 5.5V. The input voltage range provides adequate headroom for the device to have a regulated output. Make sure this input supply is well regulated. If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Improve PSRR and Noise Performance

Design the printed circuit board (PCB) with ground plane connections for V_{IN} and V_{OUT} capacitors. Make sure the ground plane is connected at the device GND pin to improve AC performance such as PSRR, output noise, and transient response. In addition, make sure the ground connection for the bypass capacitor connects directly to the GND pin of the device.

7.4.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current multiplied by the voltage drop across the output pass transistor (V_{IN} to V_{OUT}). The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Minimize power dissipation by using the lowest possible input voltage necessary to provide the required output voltage.

7.4.2 Layout Examples

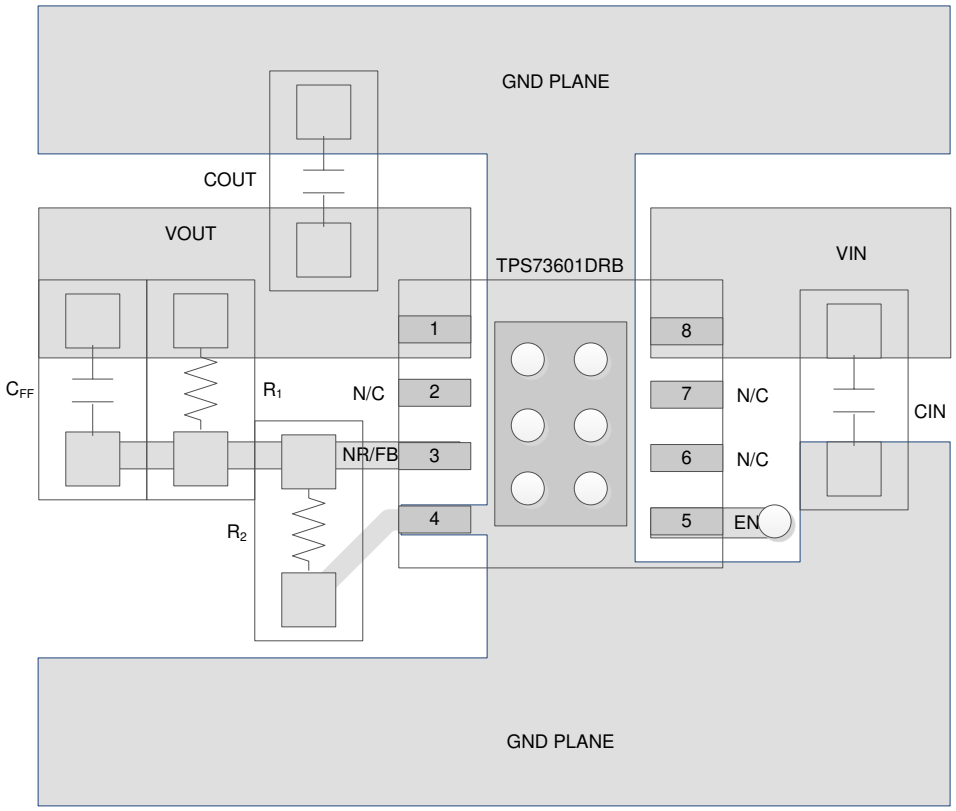


Figure 7-7. Adjustable Output Voltage Option Layout (DRB Package)

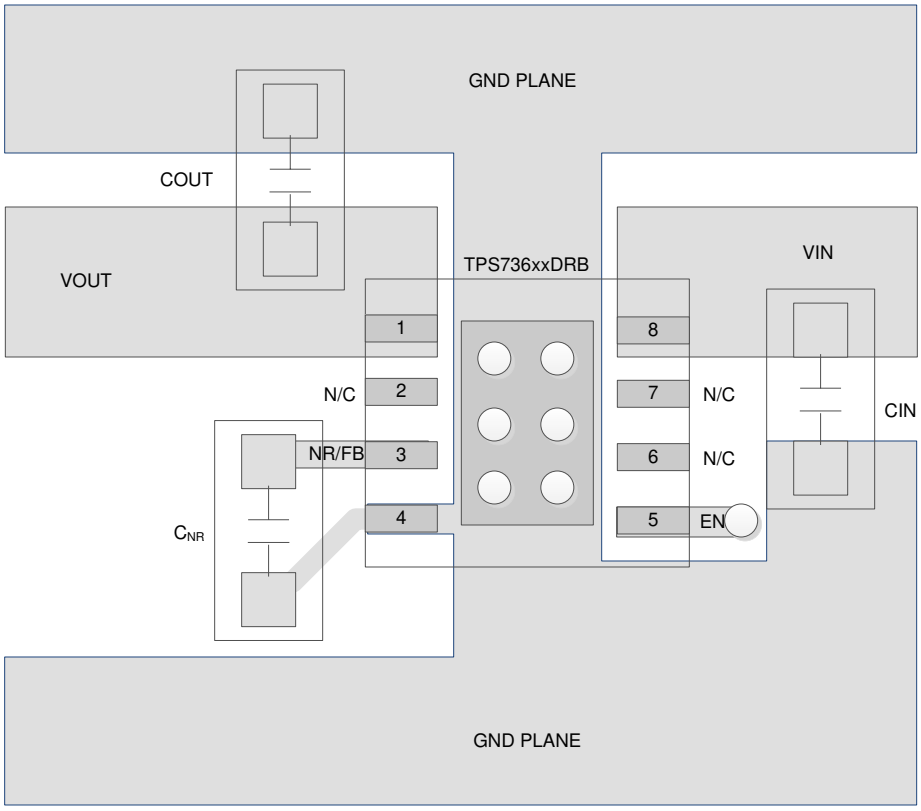


Figure 7-8. Fixed Output Voltage Option Layout (DRB Package)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Ordering Information

PRODUCT[1]	DESCRIPTION
TPS737**xxQyyyz(M3)Q1**	**xx** is the nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable[2]). **Q** indicates that the device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the *legacy silicon* (CSO: DLN) or the *new silicon* (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is used. Device performance for new and legacy silicon is denoted throughout the document. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.
(2) For fixed 1.20V operation, tie FB to OUT.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2019) to Revision C (March 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed entire document to align with current family format	1
• Added new silicon (M3) devices to document	1
• Added new silicon thermal information	4
• Updated internal reference typical value	5
• Added new silicon accuracy	5
• Added new silicon ground current	5
• Added new silicon curves to *Typical Characteristics* section	6
• Deleted *Package Mounting* section	20

Changes from Revision A (July 2016) to Revision B (September 2019)	Page
• Changed device temperature grade *AEC-Q100* Features bullet	1
• Deleted sub-bullets from Features *output voltage version* bullet	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73719QDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	719Q
TPS73719QDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	719Q
TPS73733QDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	733Q
TPS73733QDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	733Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS737-Q1 :

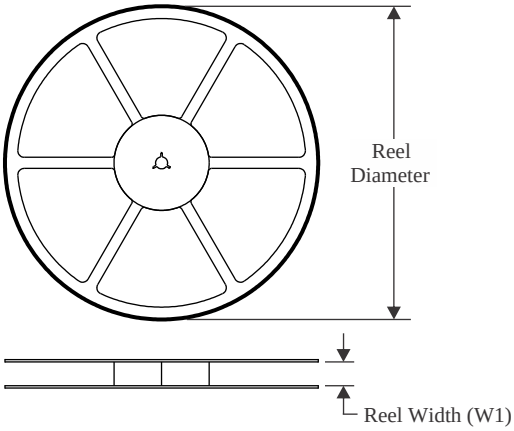
- Catalog : TPS737

NOTE: Qualified Version Definitions:

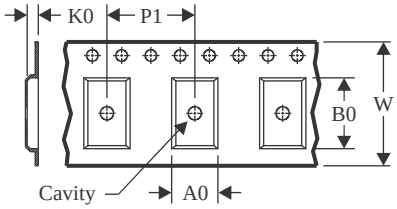
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

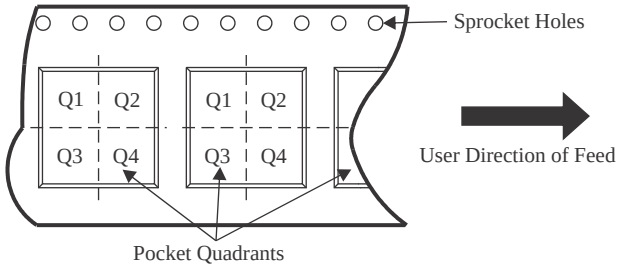


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

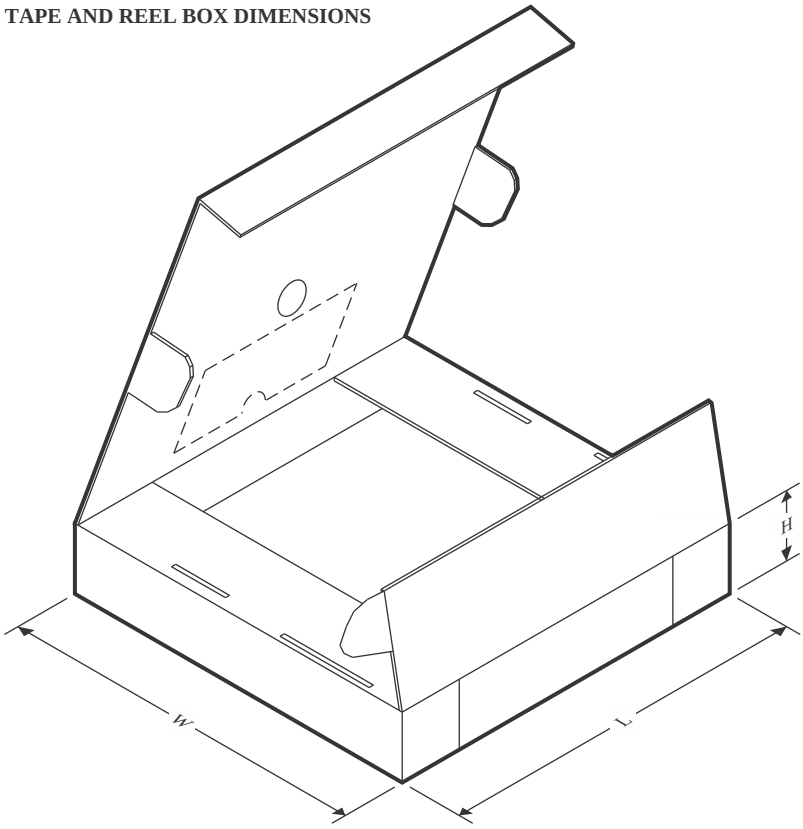
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73719QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73733QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73719QDRBRQ1	SON	DRB	8	3000	353.0	353.0	32.0
TPS73733QDRBRQ1	SON	DRB	8	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

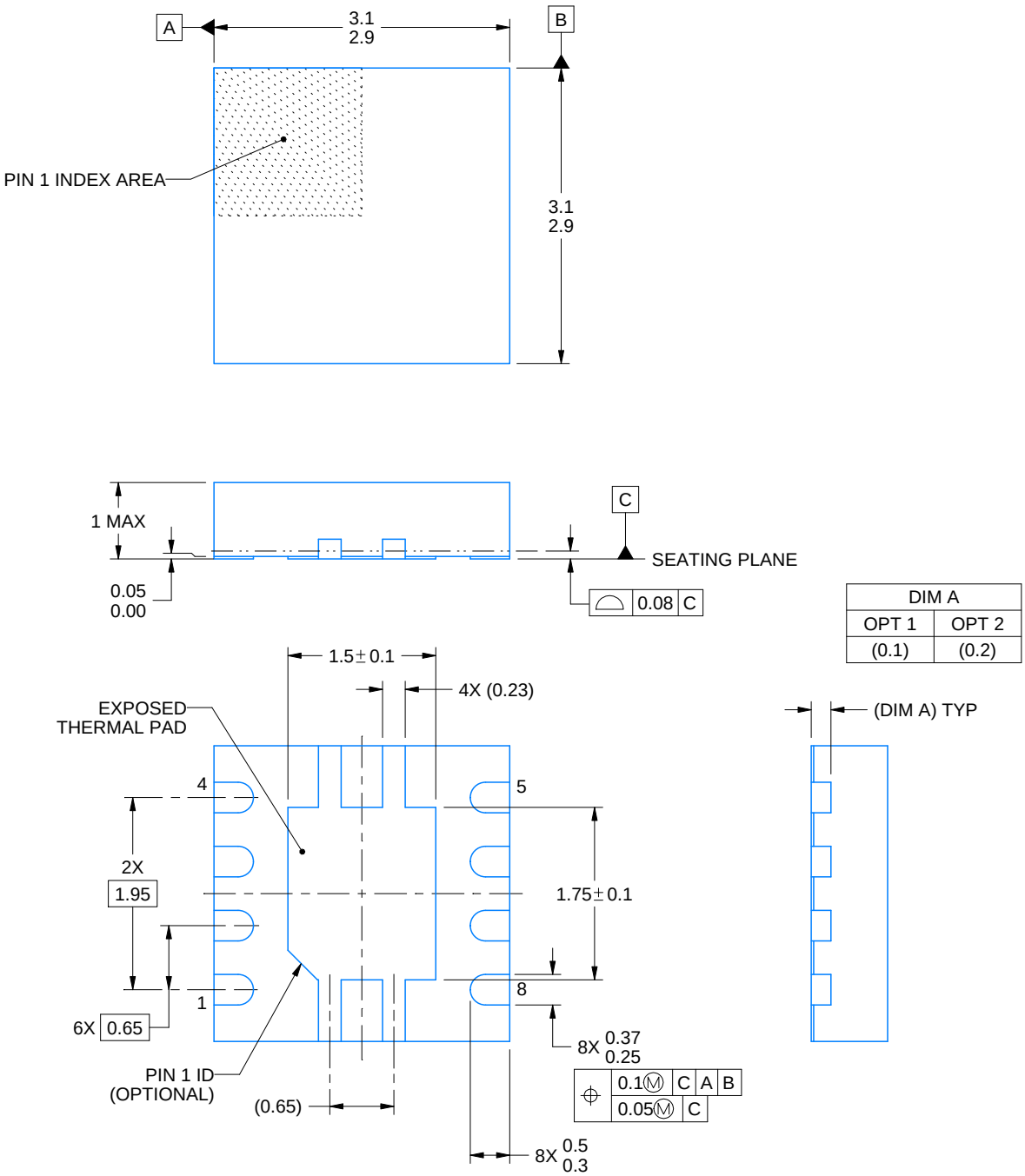
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

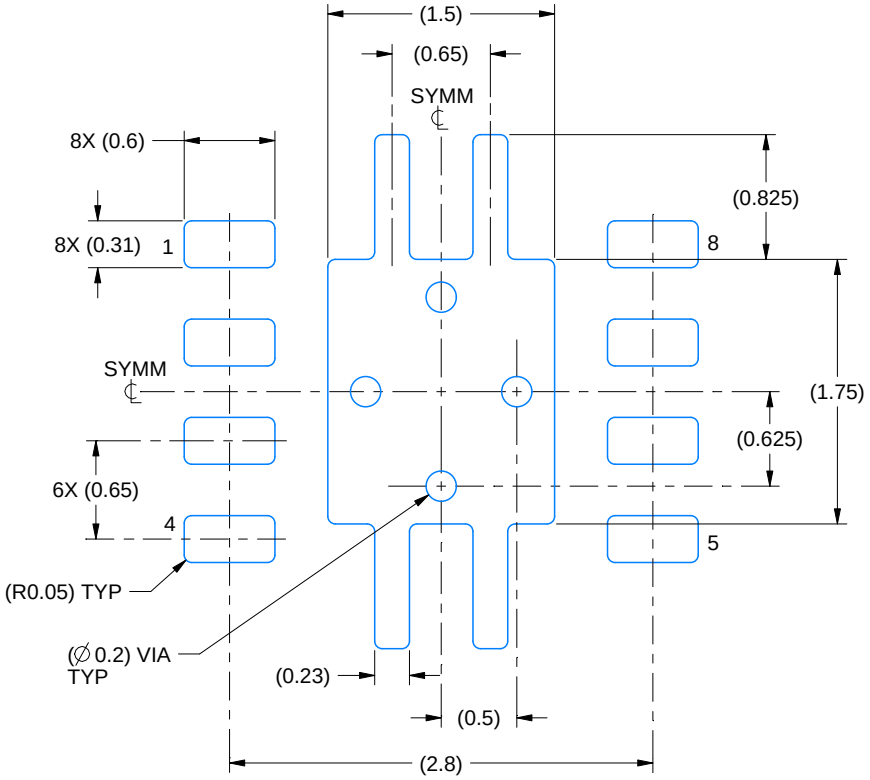
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

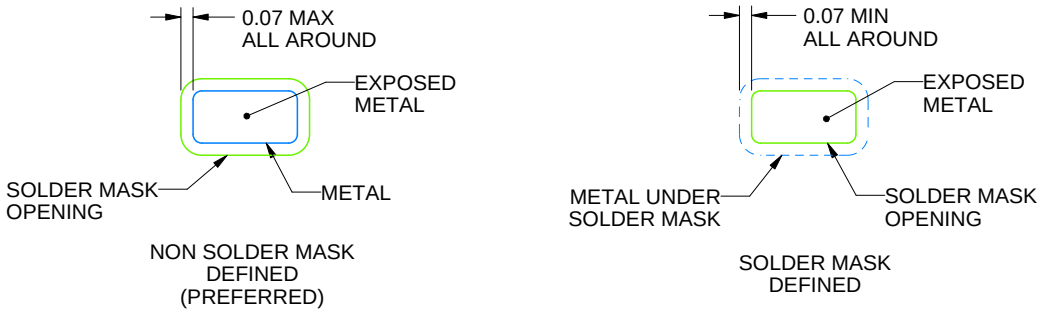
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

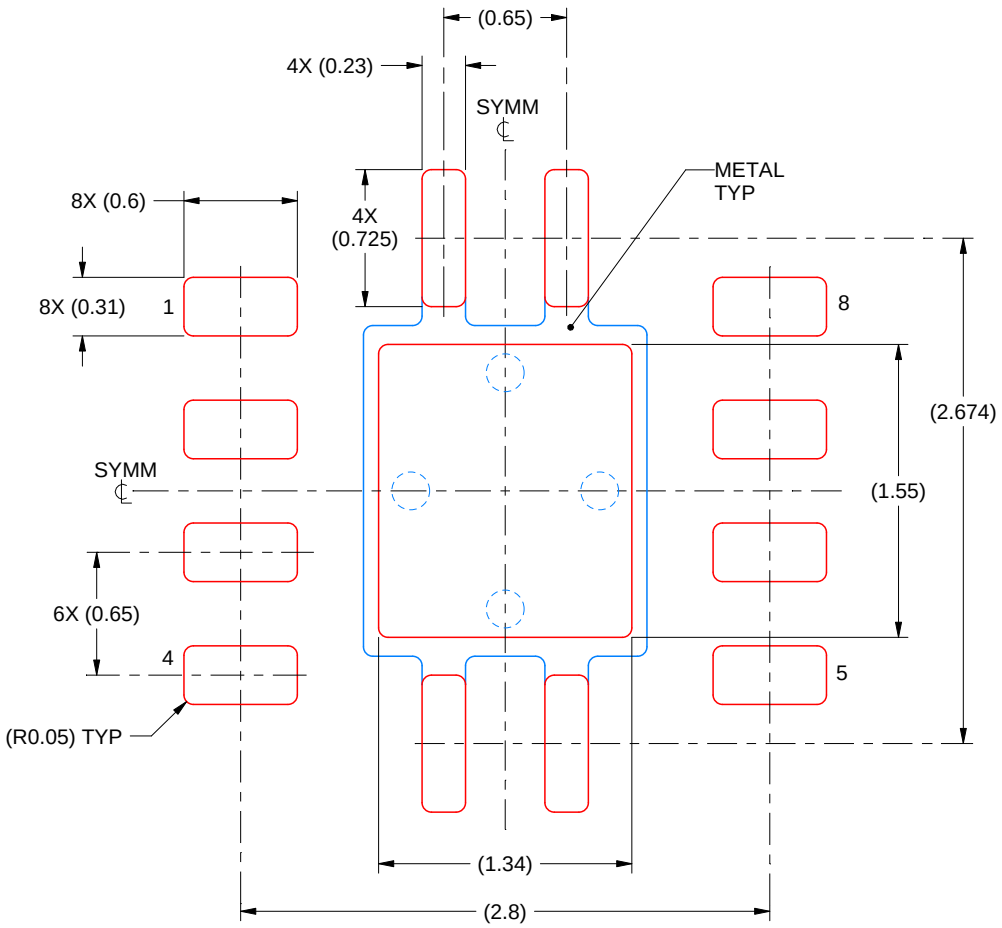


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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