TPS736-Q1 Automotive, Capacitor-Free, NMOS, 400mA, Low-Dropout Regulator With Reverse Current Protection

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Stable with no output capacitor or any value or type of capacitor
- Input voltage range: 1.7V to 5.5V
- Ultra-low dropout voltage: 75mV typical
- Excellent load transient response—with or without optional output capacitor
- New NMOS topology delivers low reverse leakage current
- Low noise: 30μV_{RMS} typical (10Hz to 100kHz)
- Initial accuracy: 0.5%
- 1% overall accuracy over line, load, and temperature
- Less than 1μA maximum I_Q in shutdown mode
- Thermal shutdown and specified minimum and maximum current limit protection
- Available in multiple output voltage versions:
  - Fixed outputs: 1.2V to 3.3V
  - Adjustable output: 1.2V to 5.5V

2 Applications

- Infotainment and clusters
- ADAS
- Body electronics and lighting

3 Description

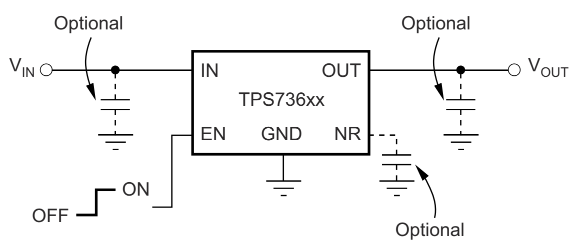
The TPS736-Q1 low-dropout (LDO) linear voltage regulator uses an NMOS topology consisting of an NMOS pass transistor in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. This topology also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS736-Q1 uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1μA and designed for portable applications. The extremely low output noise (30μV_{RMS} with 0.1μF C_{NR}) is ideal for powering VCOs. This device is protected by thermal shutdown and foldback current limit.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS736-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DCQ (SOT-223, 6)	6.5mm × 7.06mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Pin Configuration and Functions

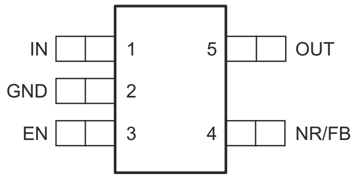


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

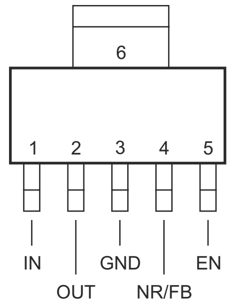


Figure 4-2. DCQ Package, 6-Pin SOT-223 (Top View)

Table 4-1. Pin Functions

PIN			Type[(1)]	DESCRIPTION
NAME	NO. SOT-23	NO. SOT-223		
EN	3	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the *Enable Pin and Shutdown* section for more information. EN can be connected to IN if not used.
FB	4	4	I	FB pin for adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	2	3, 6	—	Ground
IN	1	1	I	Input supply
NR	4	4	—	NR pin for fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal band gap, reducing output noise to very low levels.
OUT	5	2	O	Output of the regulator. There are no output capacitor requirements for stability.

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	6	
	Output, V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Operating junction, T_J	–40	150	°C
	Operating ambient, T_A	–40	125	
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.7		5.5	V
V_{OUT}	Output voltage	0		5.5	V
I_{OUT}	Output current	0		400	mA

5.4 Thermal Information

THERMAL METRIC[1]		TPS736-Q1 New silicon	TPS736-Q1 New silicon	TPS736-Q1 Legacy silicon	UNIT
		DCQ (SOT-223)	DBV (SOT-23)	DBV (SOT-23)	
		6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76	185.2	221.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.6	82.9	74.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.1	53.1	51.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.6	21.1	2.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.6	52.7	51.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

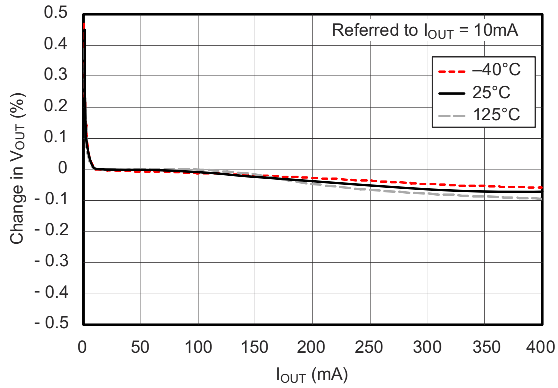
Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V[(1)] , I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted). Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range[(1)] [(2)]			1.7		5.5	V
V_{FB}	Internal reference (TPS73601)	T_J = 25°C		1.198	1.204	1.210	V
V_{OUT}	Output voltage range (TPS73601)[(3)]			V_{FB}		5.5 - V_{DO}	V
	Accuracy[(1)] [(4)]	Nominal	T_J = 25°C	–0.5		0.5	%
		over V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 400mA	–1	±0.5	1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation [(1)]	$V_{OUT(nom)}$ + 0.5V ≤ V_{IN} ≤ 5.5V			0.01		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 400mA			0.002		%/mA
		10mA ≤ I_{OUT} ≤ 400mA			0.0005		
V_{DO}	Dropout voltage[(5)] (V_{IN} = $V_{OUT(nom)}$ - 0.1V)	I_{OUT} = 400mA			75	200	mV
$Z_{O(DO)}$	Output impedance in dropout	1.7V ≤ V_{IN} ≤ V_{OUT} + V_{DO}			0.25		Ω
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	legacy silicon	400	650	800	mA
		3.6V ≤ V_{IN} ≤ 4.2V, 0℃ ≤ T_J ≤ 70℃		500		800	
		V_{OUT} = 0.9 × $V_{OUT(nom)}$	new silicon	500		800	
I_{SC}	Short-circuit current	V_{OUT} = 0V			450		mA
I_{REV}	Reverse leakage current[(6)] (-I_{IN})	V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT}			0.1	10	µA
I_{GND}	Ground pin current	I_{OUT} = 10mA (I_Q), legacy silicon			400	550	µA
		I_{OUT} = 10mA (I_Q), new silicon			400	630	
I_{GND}	Ground pin current	I_{OUT} = 400mA			800	1000	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V, –40°C ≤ T_J ≤ 100℃, legacy silicon			0.02	1.3	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V, new silicon			0.02	1	µA
I_{FB}	Feedback pin current (TPS73601)				0.1	0.45	µA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100Hz, I_{OUT} = 400mA			58		dB
		f = 10kHz, I_{OUT} = 400mA			37		
V_N	Output noise voltage, BW = 10Hz to 100kHz	C_{OUT} = 10µF, no C_{NR}			27 × V_{OUT}		μV_{RMS}
		C_{OUT} = 10µF, C_{NR} =0.01µF			8.5 × V_{OUT}		
t_{STR}	Startup time	V_{OUT} = 3V, R_L = 30Ω, C_{OUT} = 1µF			600		µs
$V_{EN(high)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(high)}$	Enable pin current (enabled)	V_{EN} = 5.5V			0.02	0.1	µA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6V, when V_{IN} ≤ 1.6V, the output locks to V_{IN} and can result in a damaging over-voltage condition on the output. To avoid this situation, disable the device before powering down V_{IN}. (Legacy silicon only)
(3) TPS73601-Q1 is tested at V_{OUT} = 2.5V.
(4) Tolerance of external resistors not included in this specification.
(5) V_{DO} is not measured for output versions with $V_{OUT(nom)}$ < 1.8V, because minimum V_{IN} = 1.7V.
(6) Fixed-voltage versions only; refer to *Application Information* section for more information.

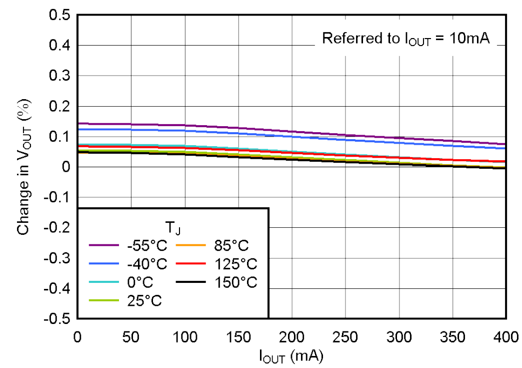
5.6 Typical Characteristics

for all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



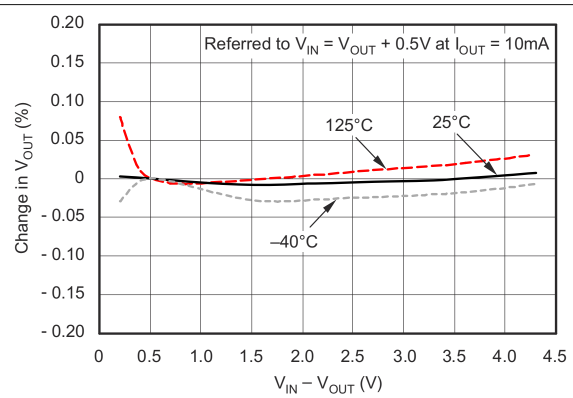
Legacy silicon

Figure 5-1. Load Regulation



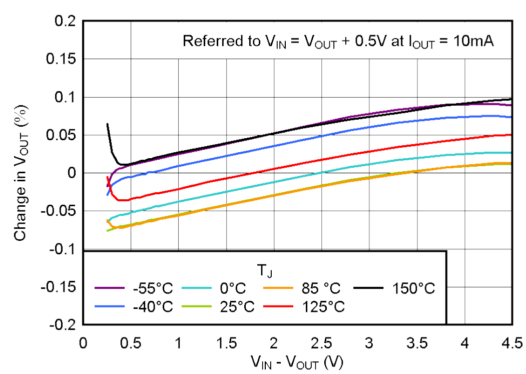
New silicon

Figure 5-2. Load Regulation



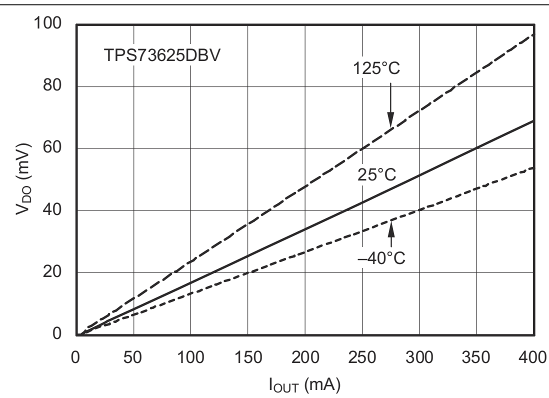
Legacy silicon

Figure 5-3. Line Regulation



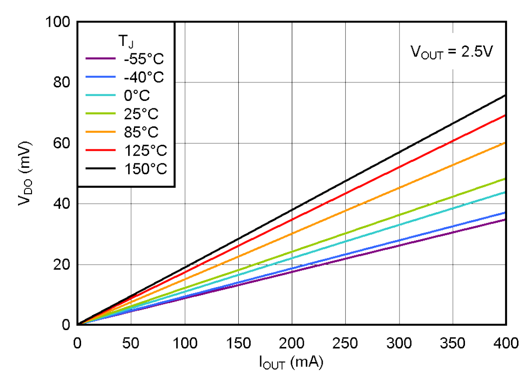
New silicon

Figure 5-4. Line Regulation



Legacy silicon

Figure 5-5. Dropout Voltage vs Output Current

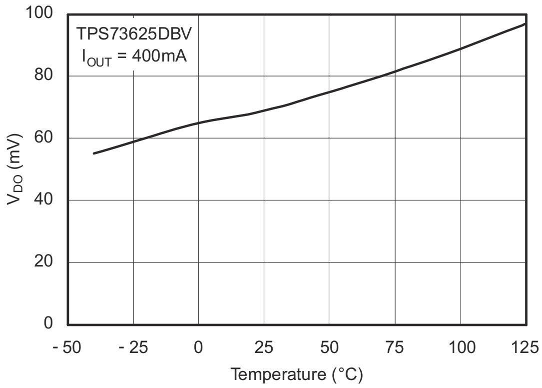


New silicon

Figure 5-6. Dropout Voltage vs Output Current

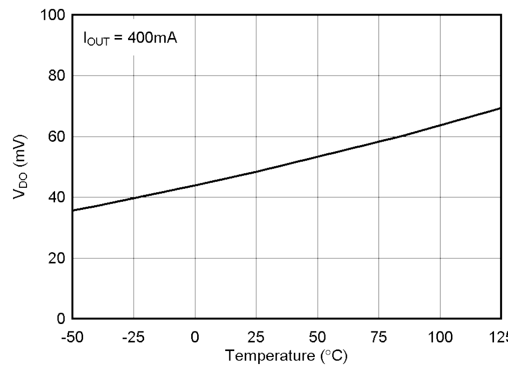
5.6 Typical Characteristics (continued)

for all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



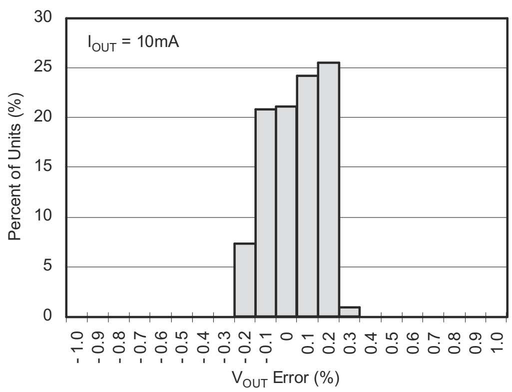
Legacy silicon

Figure 5-7. Dropout Voltage vs Temperature



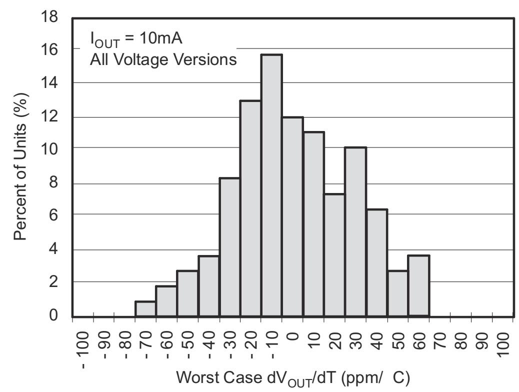
New silicon

Figure 5-8. Dropout Voltage vs Temperature



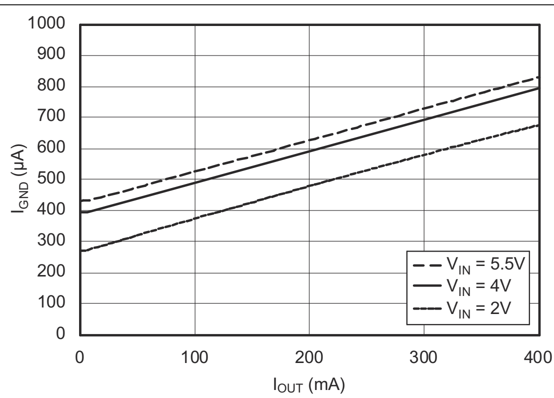
Legacy silicon

Figure 5-9. Output Voltage Accuracy Histogram



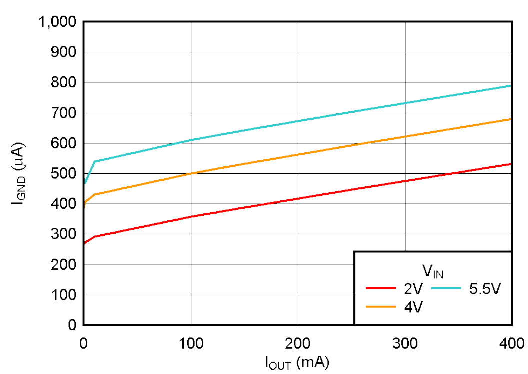
Legacy silicon

Figure 5-10. Output Voltage Drift Histogram



Legacy silicon

Figure 5-11. Ground Pin Current vs Output Current

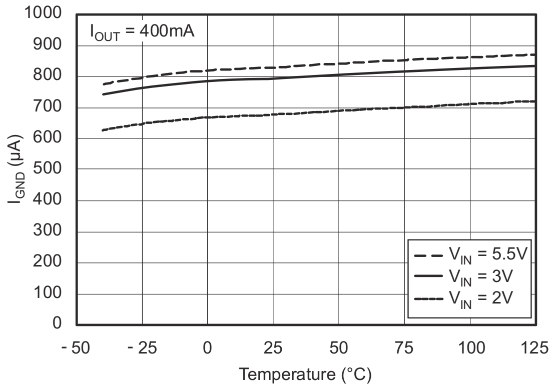


New silicon

Figure 5-12. Ground Pin Current vs Output Current

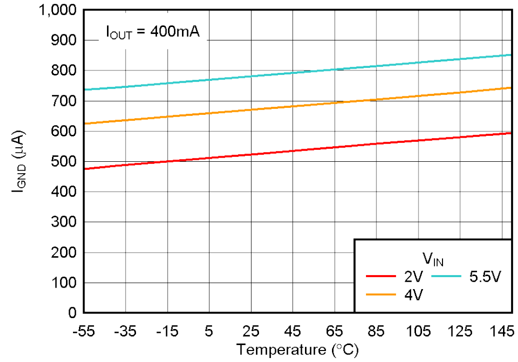
5.6 Typical Characteristics (continued)

for all voltage versions, at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



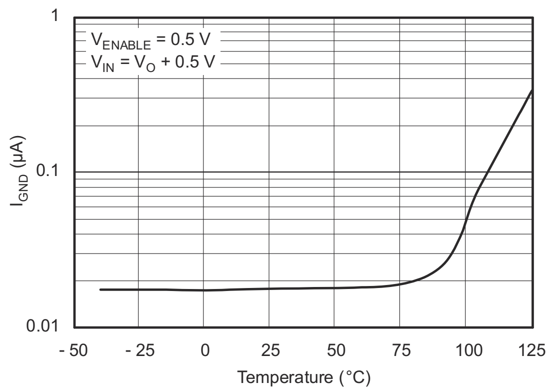
Legacy silicon

Figure 5-13. Ground Pin Current vs Temperature



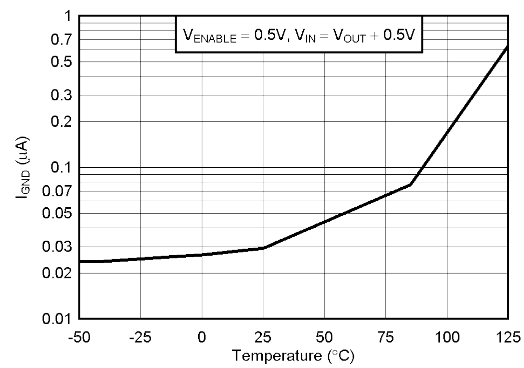
New silicon

Figure 5-14. Ground Pin Current vs Temperature



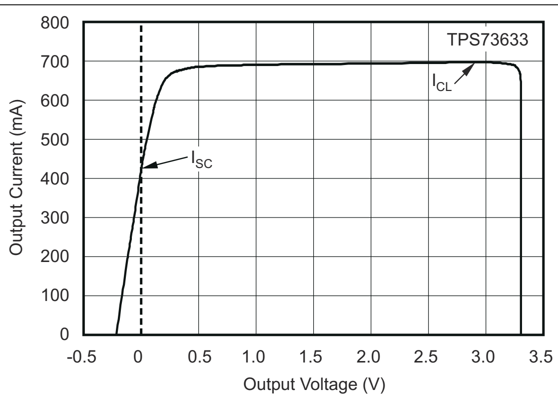
Legacy silicon

Figure 5-15. Ground Pin Current in Shutdown vs Temperature



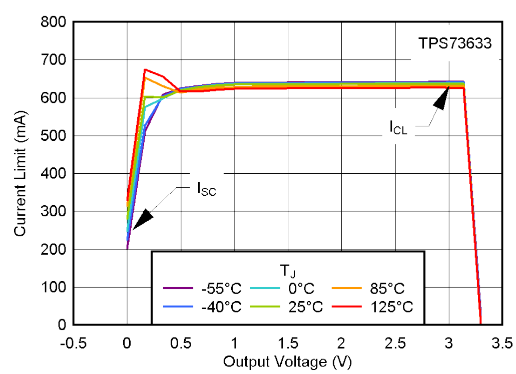
New silicon

Figure 5-16. Ground Pin Current in Shutdown vs Temperature



Legacy silicon

Figure 5-17. Current Limit vs V_{OUT} (Foldback)

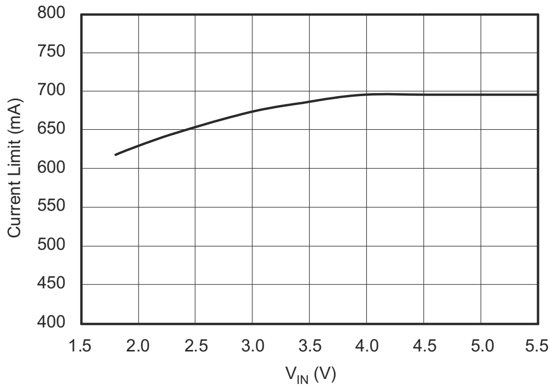


New silicon

Figure 5-18. Current Limit vs V_{OUT} (Foldback)

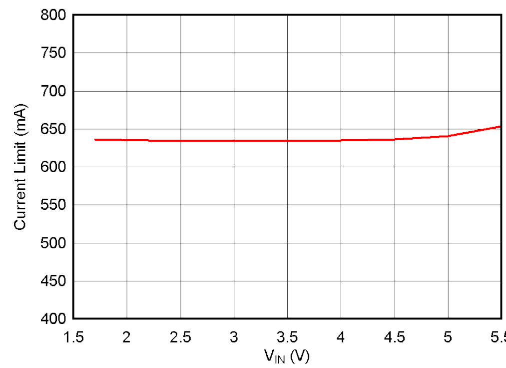
5.6 Typical Characteristics (continued)

for all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



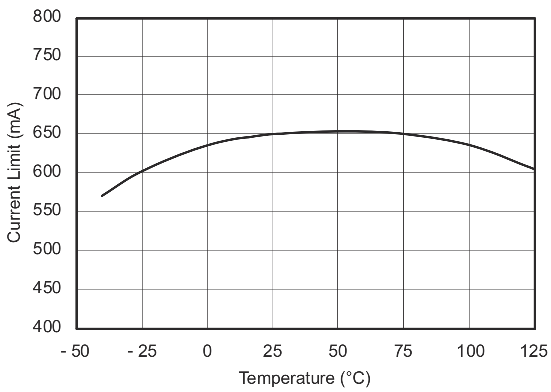
Legacy silicon

Figure 5-19. Current Limit vs V_{IN}



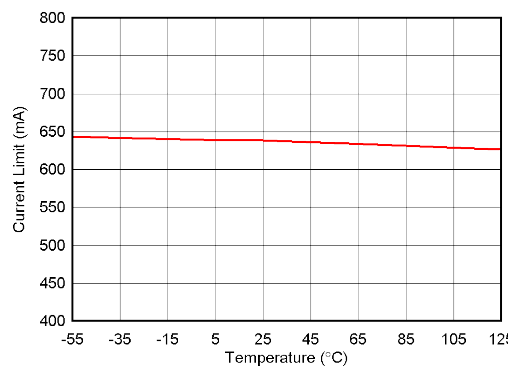
New silicon

Figure 5-20. Current Limit vs V_{IN}



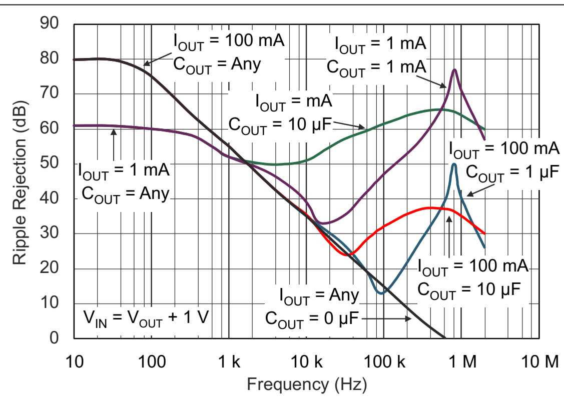
Legacy silicon

Figure 5-21. Current Limit vs Temperature



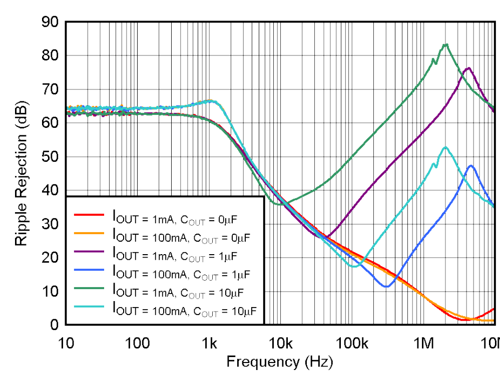
New silicon

Figure 5-22. Current Limit vs Temperature



Legacy silicon

Figure 5-23. PSRR (Ripple Rejection) vs Frequency

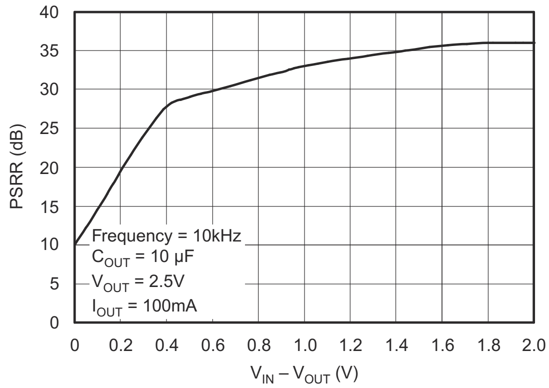


New silicon

Figure 5-24. PSRR (Ripple Rejection) vs Frequency

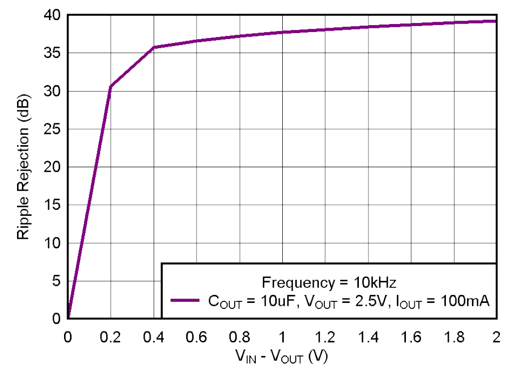
5.6 Typical Characteristics (continued)

for all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



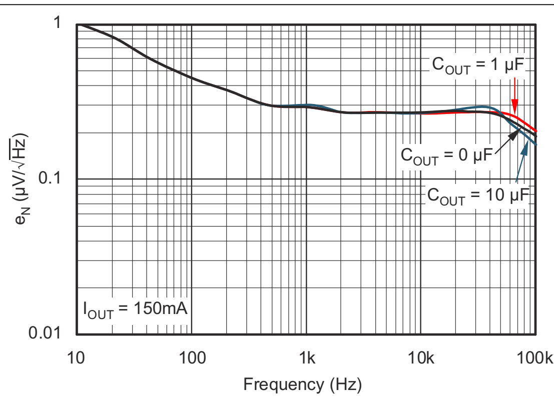
Legacy silicon

Figure 5-25. PSRR (Ripple Rejection) vs $V_{IN} – V_{OUT}$



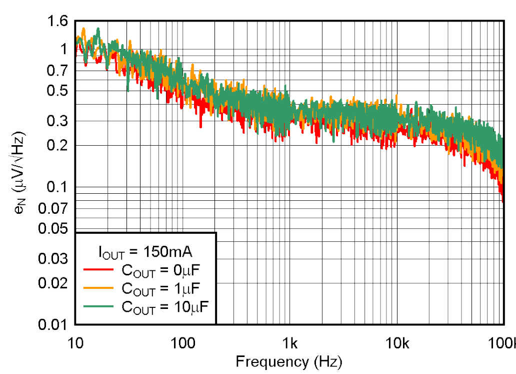
New silicon

Figure 5-26. PSRR (Ripple Rejection) vs ($V_{IN} – V_{OUT}$)



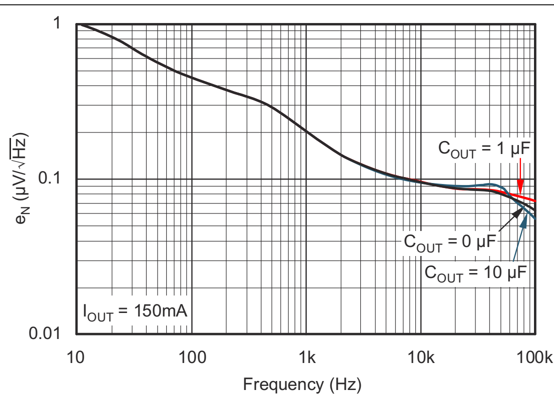
Legacy silicon

Figure 5-27. Noise Spectral Density C_{NR} = 0µF



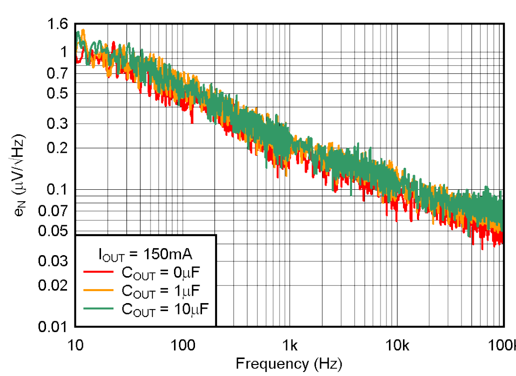
New silicon

Figure 5-28. Noise Spectral Density C_{NR} = 0µF



Legacy silicon

Figure 5-29. Noise Spectral Density C_{NR} = 0.01µF

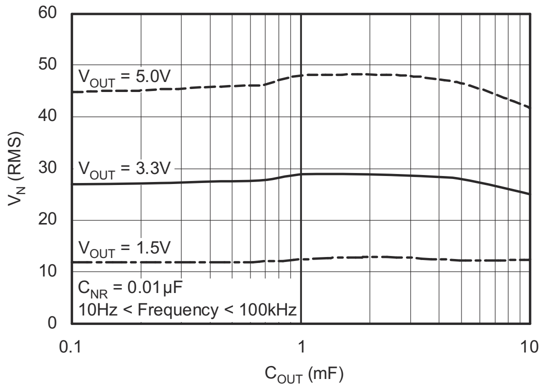


New silicon

Figure 5-30. Noise Spectral Density C_{NR} = 0.01µF

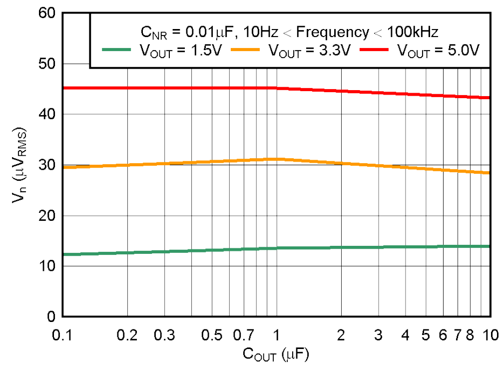
5.6 Typical Characteristics (continued)

for all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



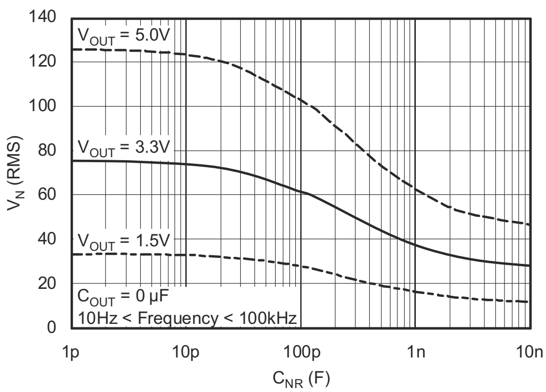
Legacy silicon

Figure 5-31. RMS Noise Voltage vs C_{OUT}



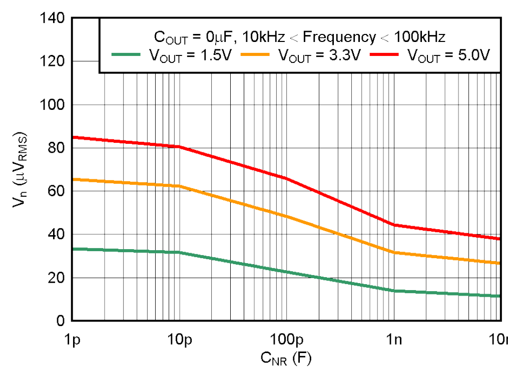
New silicon

Figure 5-32. RMS Noise Voltage vs C_{OUT}



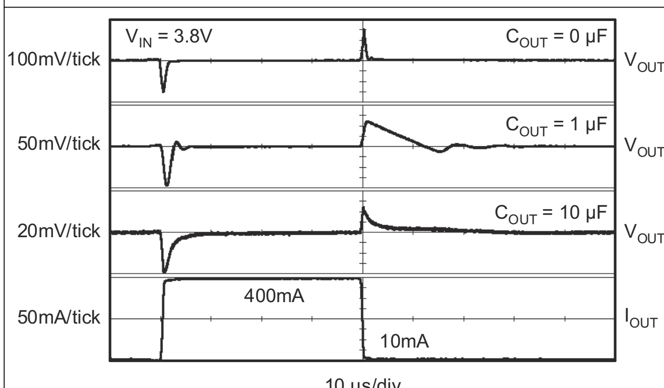
Legacy silicon

Figure 5-33. RMS Noise Voltage vs C_{NR}



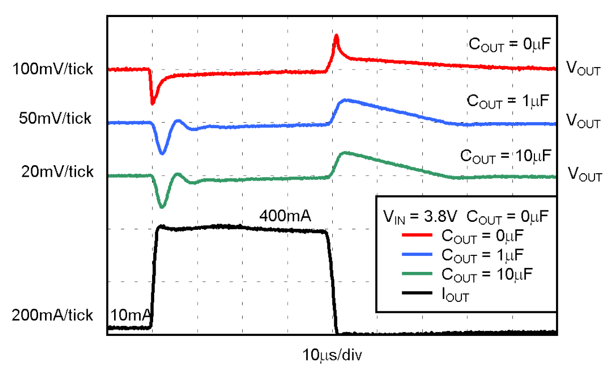
New silicon

Figure 5-34. RMS Noise Voltage vs C_{NR}



Legacy silicon

Figure 5-35. TPS73633 Load Transient Response

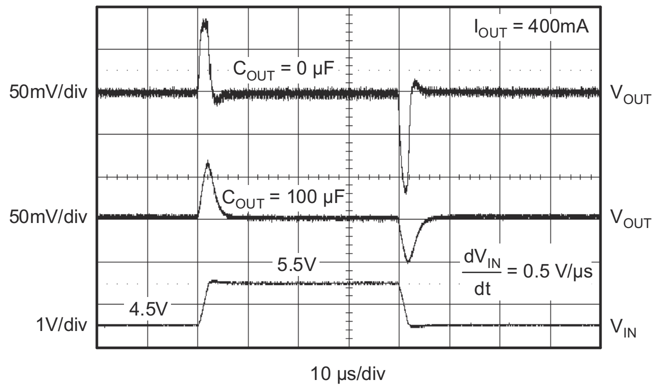


New silicon

Figure 5-36. TPS73633 Load Transient Response

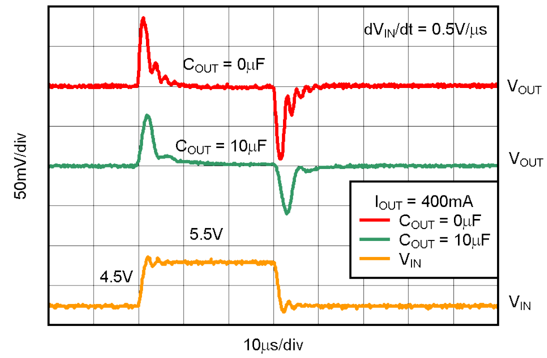
5.6 Typical Characteristics (continued)

for all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



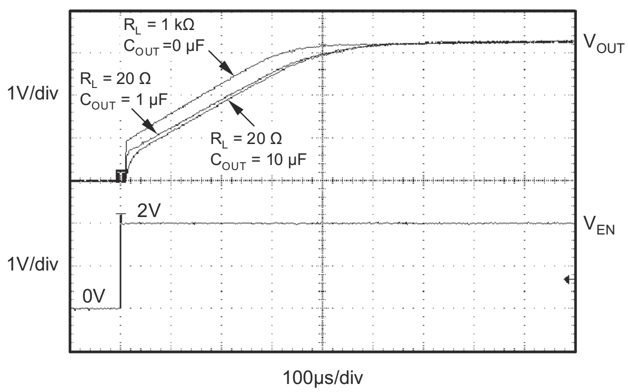
Legacy silicon

Figure 5-37. TPS73633 Line Transient Response



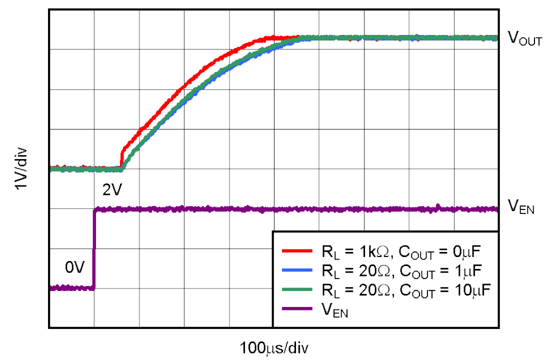
New silicon

Figure 5-38. TPS73633 Line Transient Response



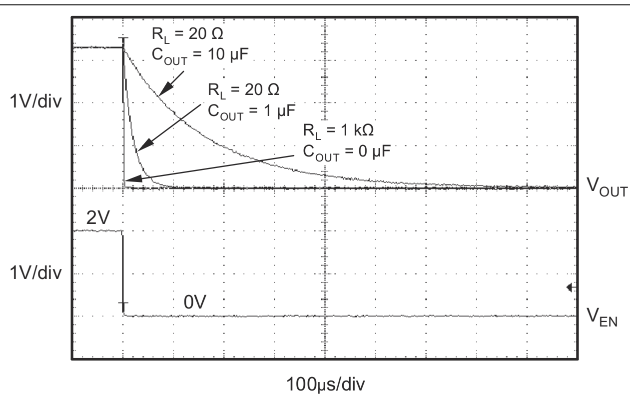
Legacy silicon

Figure 5-39. TPS73633 Turn-On Response



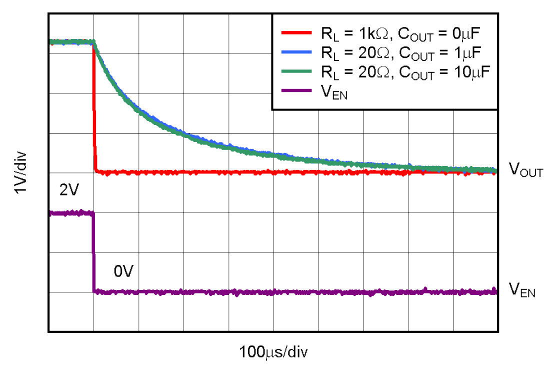
New silicon

Figure 5-40. TPS73633 Turn-On Response



Legacy silicon

Figure 5-41. TPS73633 Turn-Off Response

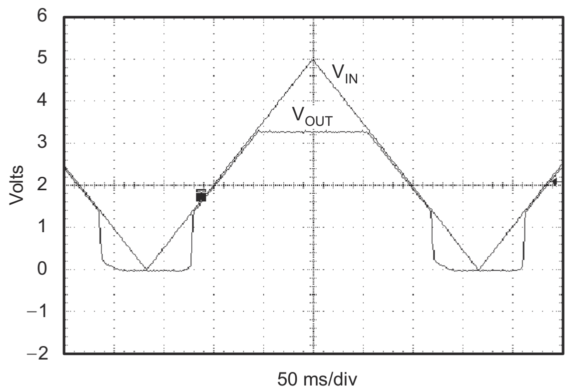


New silicon

Figure 5-42. TPS73633 Turn-Off Response

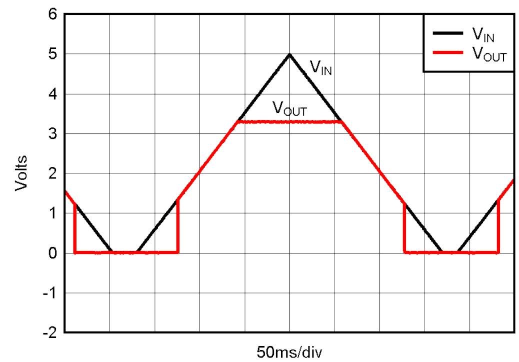
5.6 Typical Characteristics (continued)

for all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



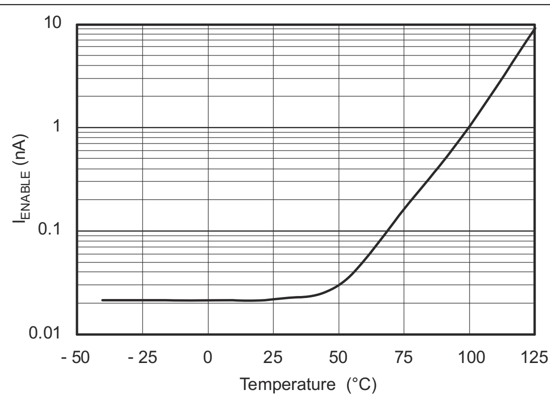
Legacy silicon

Figure 5-43. TPS73633 Power-Up, Power-Down



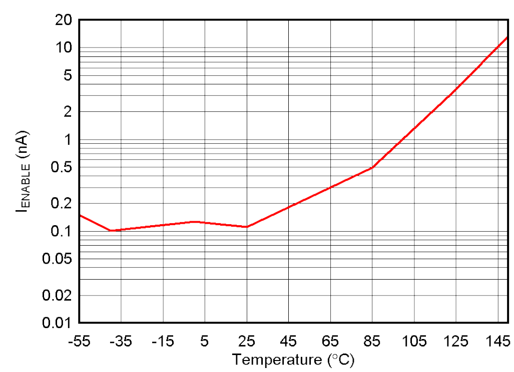
New silicon

Figure 5-44. TPS73633 Power-Up, Power-Down



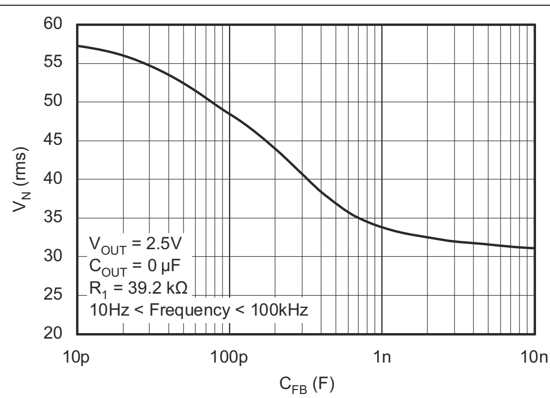
Legacy silicon

Figure 5-45. I_{ENABLE} vs Temperature



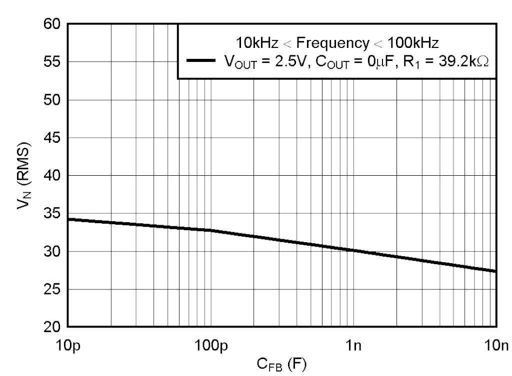
New silicon

Figure 5-46. I_{ENABLE} vs Temperature



Legacy silicon

Figure 5-47. TPS73601 RMS Noise Voltage vs C_{FB}

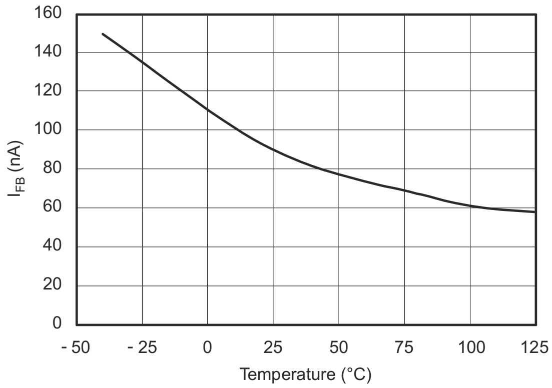


New silicon

Figure 5-48. TPS73601 RMS Noise Voltage vs C_{FB}

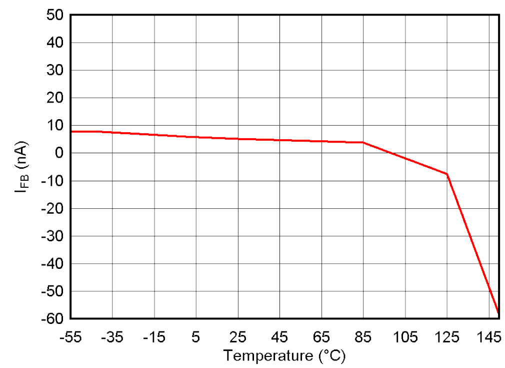
5.6 Typical Characteristics (continued)

for all voltage versions, at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



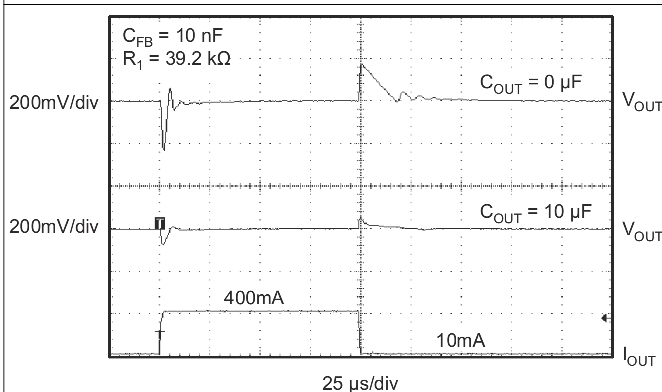
Legacy silicon

Figure 5-49. TPS73601 I_{FB} vs Temperature



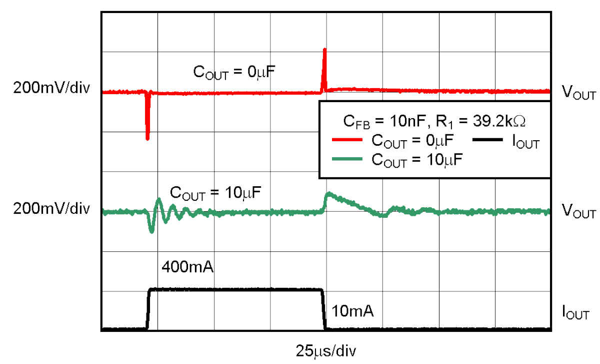
New silicon

Figure 5-50. TPS73601 I_{FB} vs Temperature



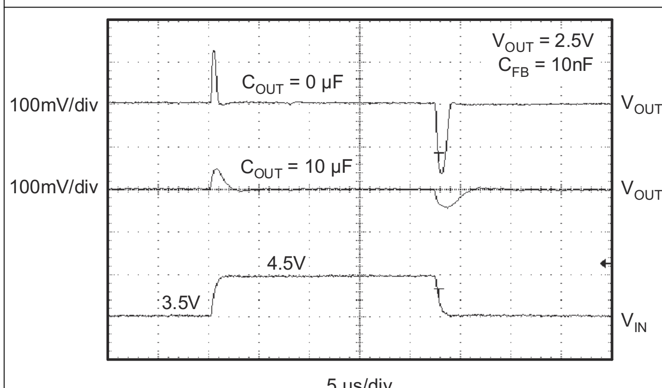
Legacy silicon

Figure 5-51. TPS73601 Load Transient, Adjustable Version



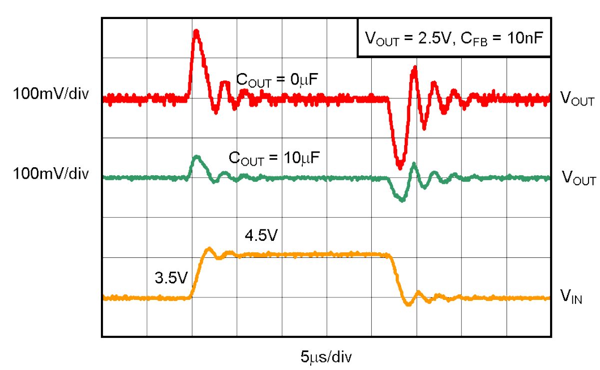
New silicon

Figure 5-52. TPS73601 Load Transient, Adjustable Version



Legacy silicon

Figure 5-53. TPS73601 Line Transient, Adjustable Version



New silicon

Figure 5-54. TPS73601 Line Transient, Adjustable Version

6 Detailed Description

6.1 Overview

The TPS736xx-Q1 belongs to a family of new-generation LDO regulators that use an NMOS pass transistor to achieve ultra-low dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS736xx-Q1 designed for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and overcurrent protection, including foldback current limit.

6.2 Functional Block Diagrams

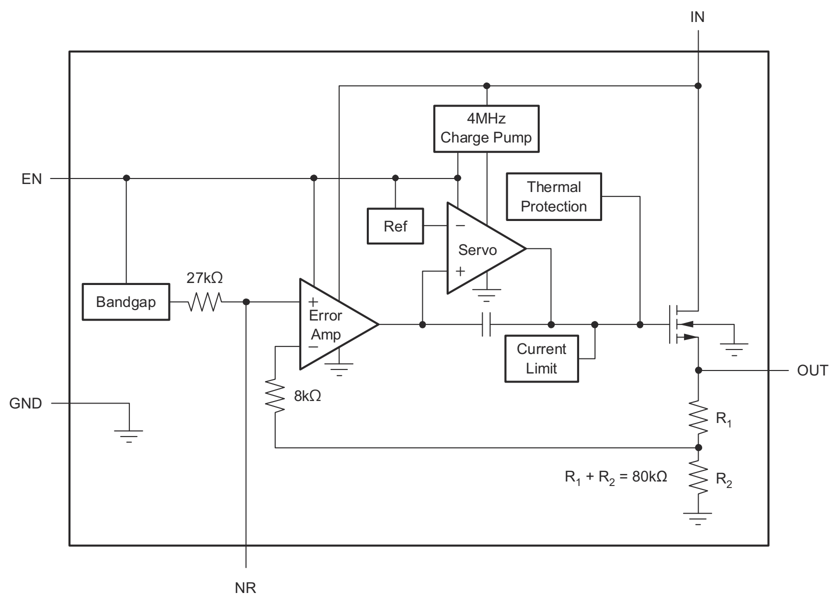
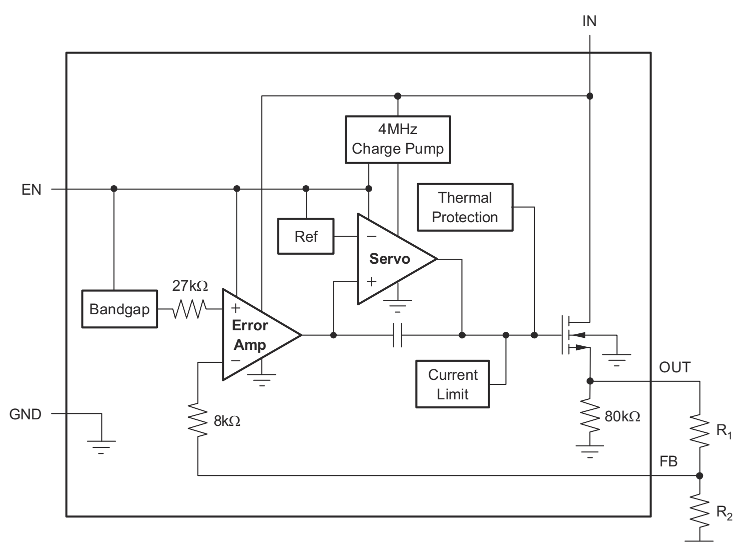


Figure 6-1. Fixed Voltage Version



See Table 6-1 for standard resistor values.

Figure 6-2. Adjustable Voltage Version

Table 6-1. Standard 1% Resistor Values for Common Output Voltages

V_{OUT} (1)	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ

(1) V_{OUT} = (R1 + R2) / R2 × 1.204; R1 || R2 ≅ 19kΩ for best accuracy.

6.3 Feature Description

6.3.1 Internal Current Limit

The TPS736xx-Q1 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V (see Figure 5-17). Approximately –0.2V of V_{OUT} results in a current limit of 0mA. Therefore, if OUT is forced below –0.2V before EN goes high, the device does not always start up. In applications that work with both a positive and negative voltage supply, the TPS736xx-Q1 must be enabled first.

6.3.2 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value of 1µF) from the OUT pin to ground reduces undershoot magnitude but increase the duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin also improves the transient response.

The TPS736xx-Q1 does not have active pulldown when the output is overvoltage. This feature allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This feature also results in an output overshoot of several percent if load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal and external load resistance. The rate of decay is given by Equation 1 or Equation 2, determined by the version.

Fixed voltage version

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \parallel R_{LOAD}} \tag{1}$$

Adjustable voltage version

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \tag{2}$$

6.3.3 Reverse Current

The NMOS pass element of the TPS736xx-Q1 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element can be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. The reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There is additional current flowing into the OUT pin due to the 80kΩ internal resistor divider to ground (see Figure 6-1 and Figure 6-2).

For the TPS73601, reverse current can flow when V_{FB} is more than 1V above V_{IN}.

6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. Thermal protection limits the dissipation of the regulator, protecting the device from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of your application. This application condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS736xx-Q1 has been designed to protect against overload conditions. Thermal protection is not intended to replace proper heat sinking. Continuously running the TPS736xx-Q1 into thermal shutdown degrades device reliability.

6.4 Device Functional Modes

6.4.1 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5V (maximum) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate. A V_{EN} above 1.7V (minimum) turns the regulator on and the output ramps back up to a regulated V_{OUT} (see Figure 5-39).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate cannot be discharged using this configuration, and the pass transistor can be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output can overshoot upon power-up.

Current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section for more information.

6.4.2 Dropout Voltage

The TPS736xx-Q1 uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the NMOS pass element.

For large step changes in load current, the TPS736xx-Q1 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of V_{IN} – V_{OUT} above this line provide normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to DC dropout levels], the TPS736xx-Q1 can take a couple of hundred microseconds to return to the specified regulation accuracy.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 7-6. Sample resistor values for common output voltages are illustrated in Figure 6-2.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19kΩ. This 19kΩ, in addition to the internal 8kΩ resistor, presents the same impedance to the error amp as the 27kΩ band-gap reference output. This impedance helps compensate for leakages into the error amp terminals.

7.2 Typical Applications

7.2.1 Typical Application Circuit for Fixed-Voltage Versions

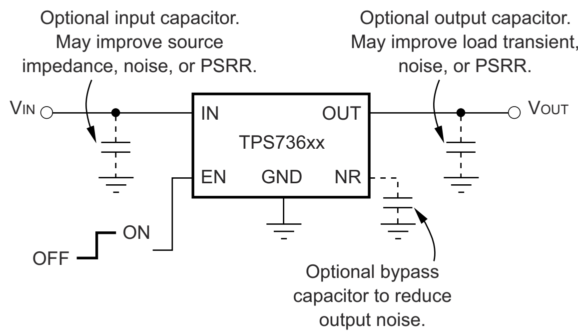


Figure 7-1. Typical Application Circuit for Fixed-Voltage Versions

7.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the input parameters.

Table 7-1. Design Parameters (Fixed-Voltage Version)

PARAMETER	EXAMPLE VALUE
Input voltage	5V, ±3%
Output voltage	3.3V, ±1%
Output current	400mA (maximum), 20mA (minimum)
RMS noise, 10Hz to 100kHz	< 30μV_{RMS}
Ambient temperature	55°C (maximum)

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Input And Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practise is to connect a 0.1μF to 1μF low ESR capacitor across the input supply near the regulator. The input capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS736xx-Q1 does not require an output capacitor for stability and has maximum phase margin with no capacitor. This regulator is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing can occur when the product of C_{OUT} and total ESR drops below 50nF × Ω. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.2.1.2.2 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS736xx-Q1. The reference generates approximately 32µV_{RMS} (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by Equation 3.

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (3)$$

Because the value of V_{REF} is 1.2V, this relationship reduces to Equation 4.

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (4)$$

for the case of no C_{NR}.

An internal 27kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship in Equation 5:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (5)$$

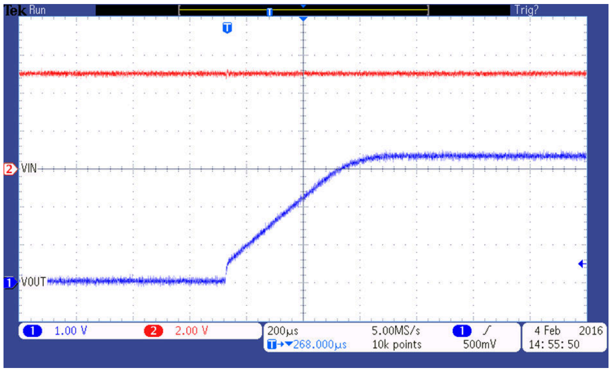
for C_{NR} = 10nF.

This noise reduction effect is shown in Figure 5-33 in the *Typical Characteristics* table.

The TPS73601 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improves load transient performance.

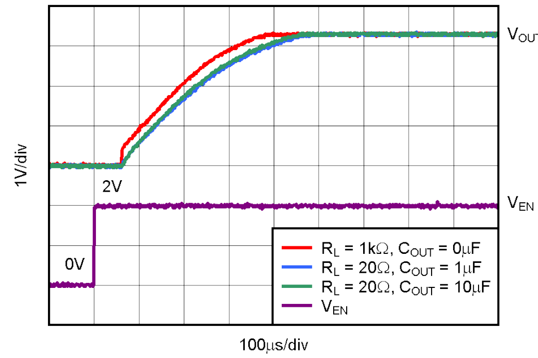
The TPS736xx-Q1 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250µV of switching noise at approximately 4MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

7.2.1.3 Application Curves



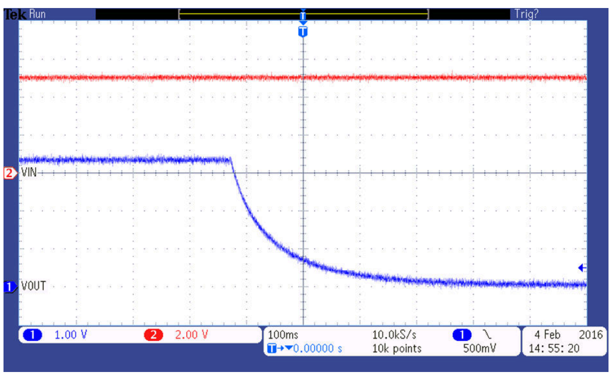
Legacy silicon

Figure 7-2. TPS73601 Start-Up



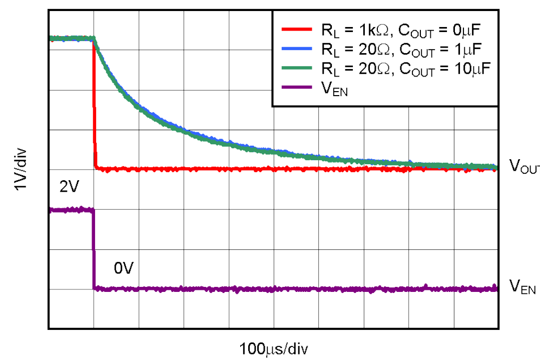
New silicon

Figure 7-3. TPS73601 Start-Up



Legacy silicon

Figure 7-4. TPS73601 Shutdown



New silicon

Figure 7-5. TPS73601 Shutdown

7.2.2 Typical Application Circuit for Adjustable-Voltage Version

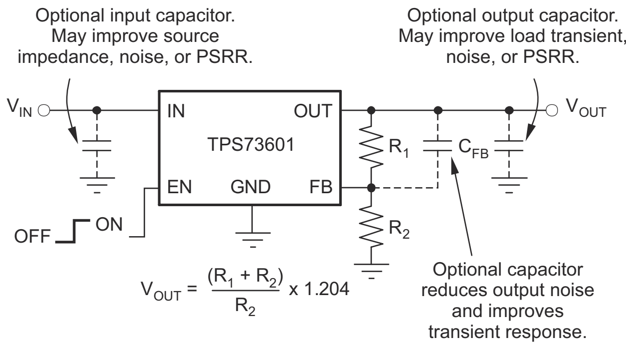


Figure 7-6. Typical Application Circuit for Adjustable-Voltage Version

7.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-2 as the input parameters.

Table 7-2. Design Parameters (Adjustable-Voltage Version)

PARAMETER	EXAMPLE VALUE
Input voltage	5V, ±3%, provided by the DC-DC converter switching at 1MHz
Output voltage	2.5V, ±1%
Output current	0.4A (maximum), 10mA (minimum)
RMS noise, 10Hz to 100kHz	< 35μV_{RMS}
Ambient temperature	55°C (maximum)

7.3 Power Supply Recommendations

This device is designed to operate with an input supply range of 1.7V to 5.5V. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, design the board with ground plane connections for V_{IN} and V_{OUT} capacitors, and the ground plane connected at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

7.4.1.1 Thermal Considerations

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Section 5.4* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improve the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), shown in Equation 6:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{6}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to provide the required output voltage.

7.4.2 Layout Examples

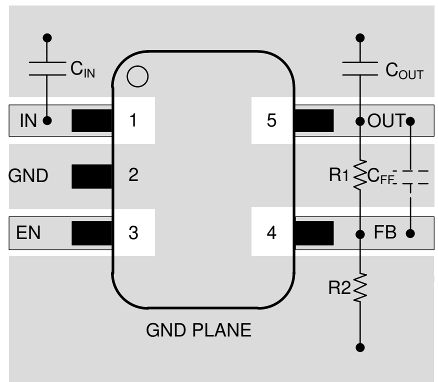


Figure 7-7. Layout Example for the DBV Package Adjustable Version

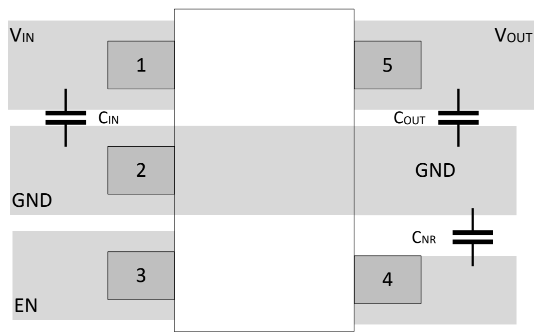


Figure 7-8. Layout Example for the DBV Package Fixed Version

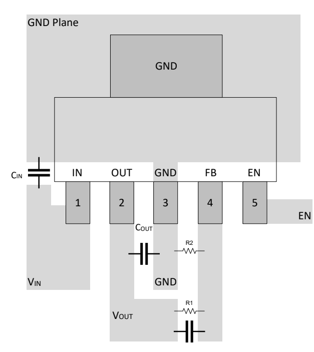


Figure 7-9. Layout Example for the DCQ Package Adjustable Version

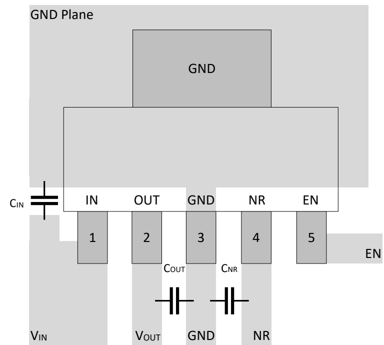


Figure 7-10. Layout Example for the DCQ Package Fixed Version

8 Device And Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Ordering Information (1)

PRODUCT	DESCRIPTION(1)
TPS736**xxQyyyz(M3)Q1**	**xx** is the nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable (2)). **Q** indicates that the device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix can ship with the *legacy silicon* (CSO: DLN) or the *new silicon* (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is being used. Device performance for new and legacy silicon is denoted throughout the document. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.
(2) For fixed 1.20V operation, tie FB to OUT.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2025) to Revision D (May 2025) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added new silicon ground pin current spec...5

10 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73601QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PTWQ
TPS73601QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PTWQ
TPS73618QDCQRM3Q1	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	73618Q
TPS73618QDCQRM3Q1.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	73618Q
TPS73618QDCQRQ1	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	73618Q
TPS73618QDCQRQ1.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	73618Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS736-Q1 :

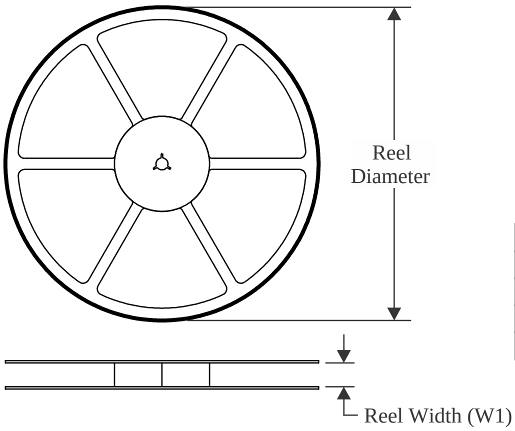
- Catalog : TPS736

NOTE: Qualified Version Definitions:

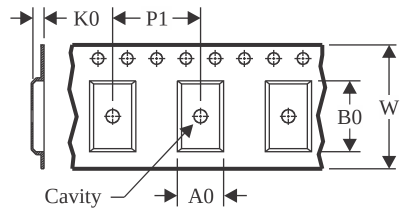
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

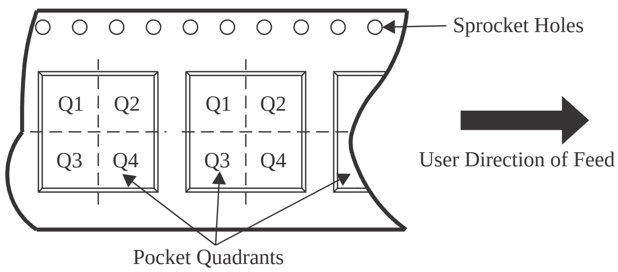


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

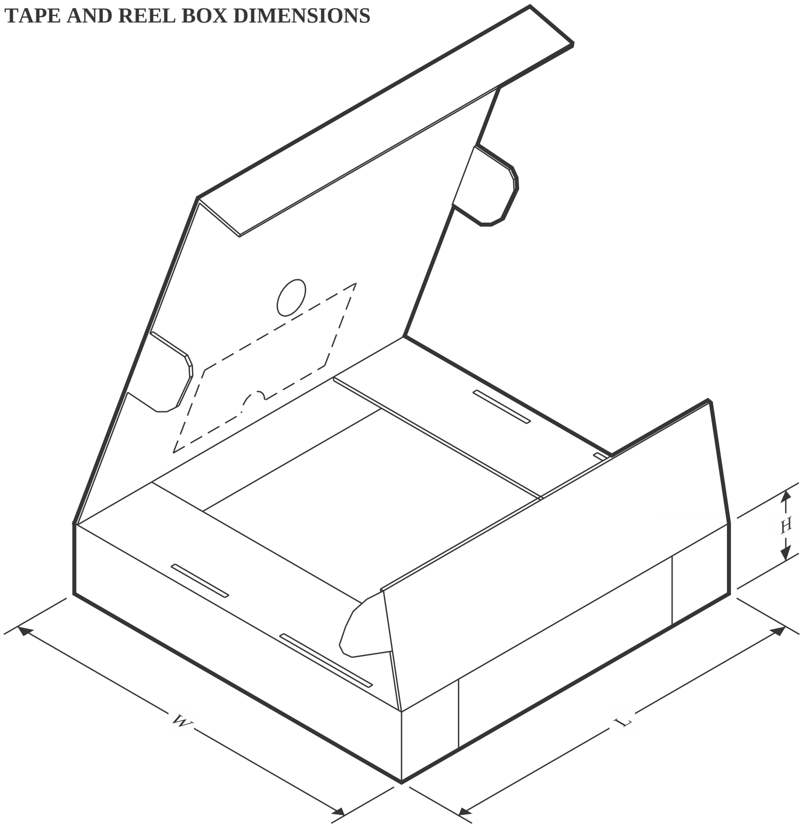
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73601QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73618QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



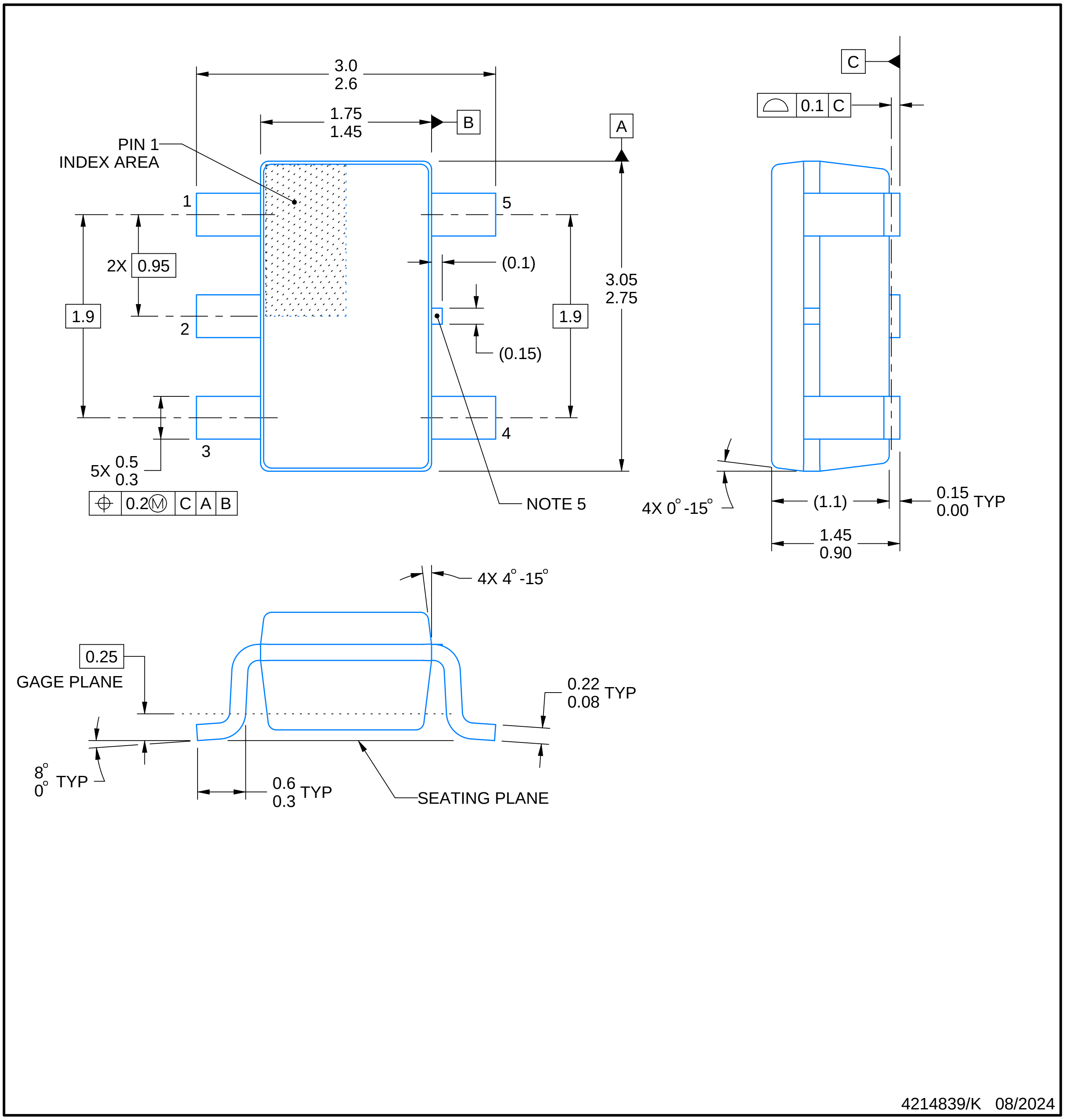
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73601QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73618QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0

PACKAGE OUTLINE

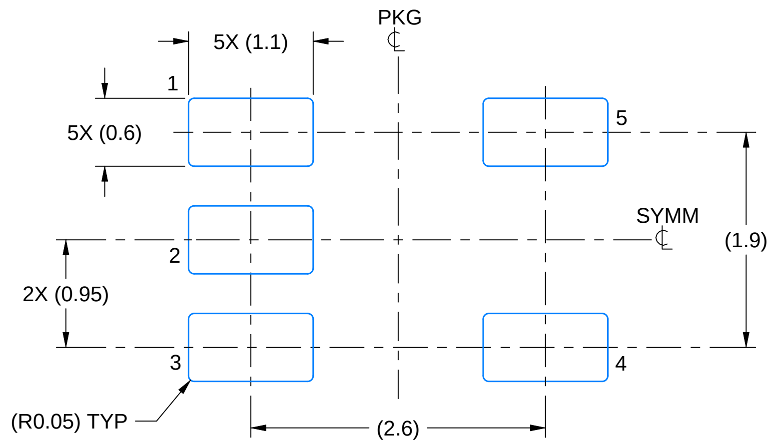
SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

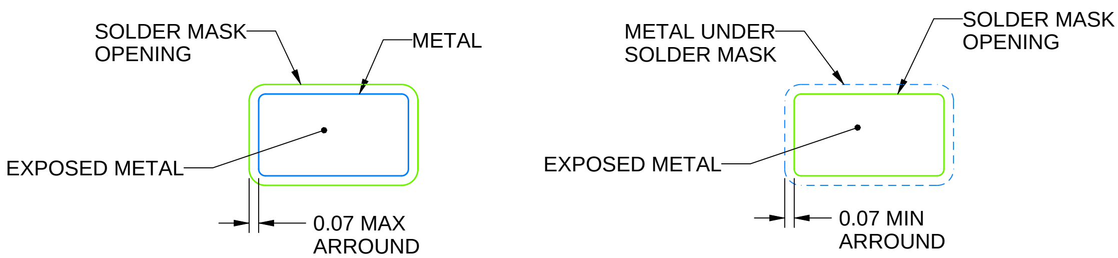


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

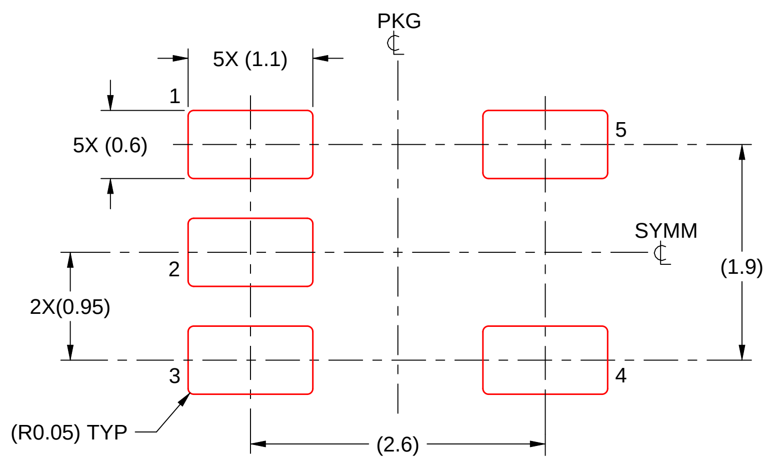


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



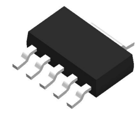
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

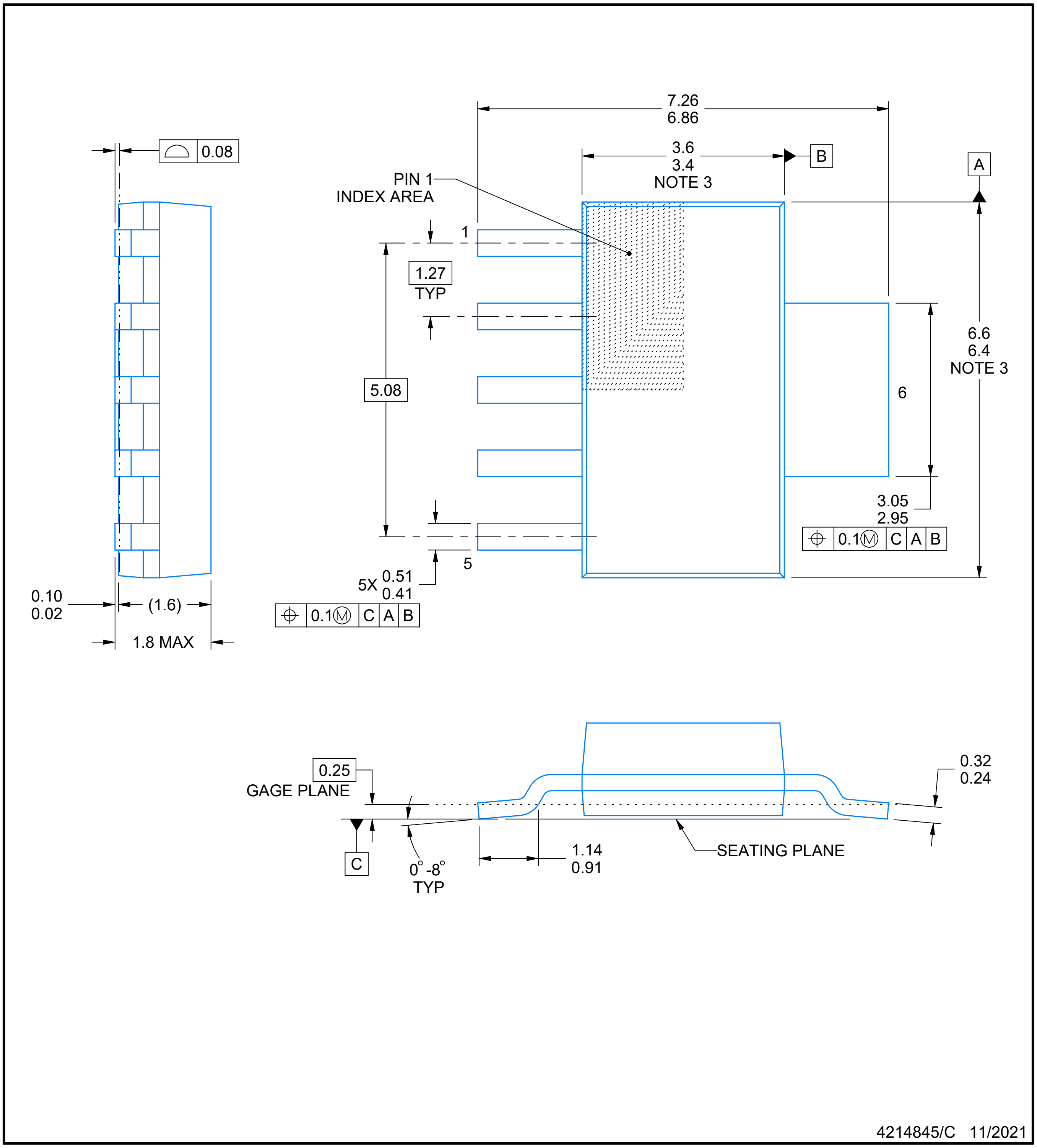
DCQ0006A



PACKAGE OUTLINE

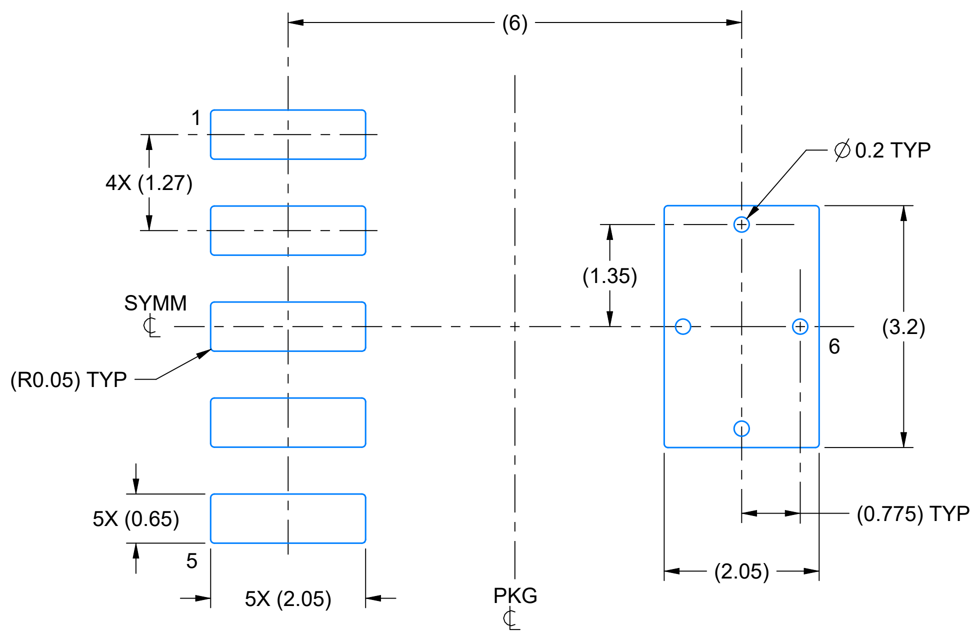
SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE

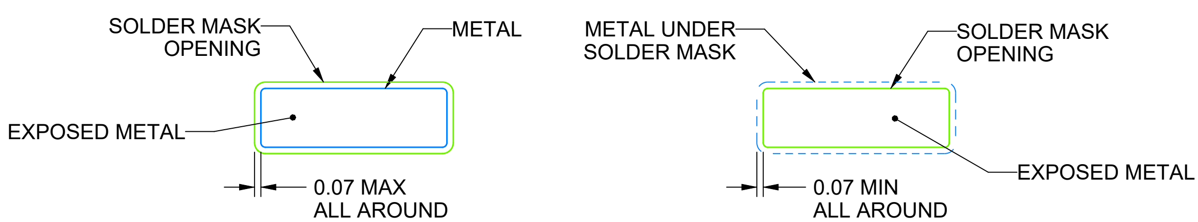


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

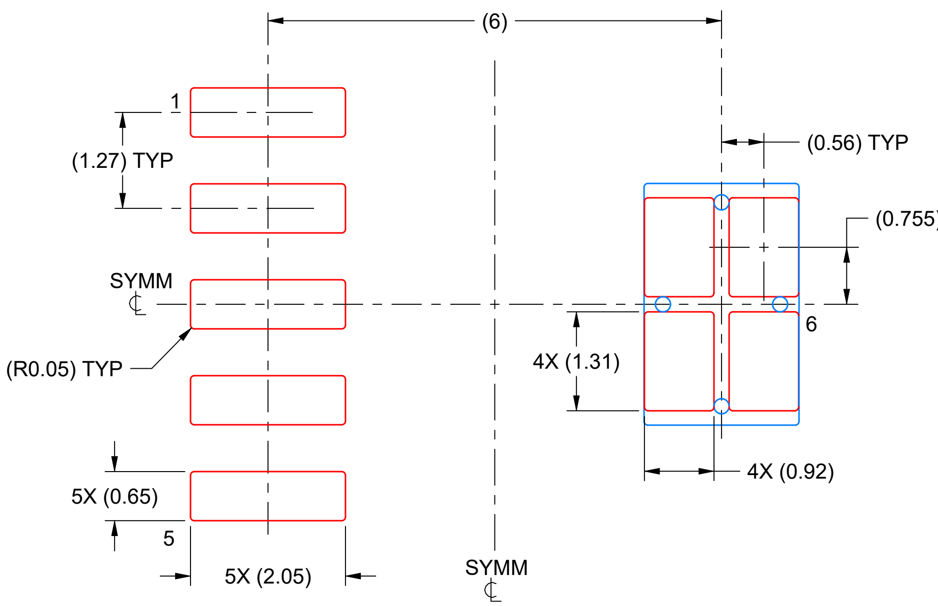


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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