# TPS735-Q1 500-mA, low quiescent current, low-noise, high PSRR, low-dropout linear regulator

## 1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Input voltage: 2.7 V to 6.5 V
- 500-mA low-dropout regulator with EN
- Low $I_Q$: 46 µA
- Multiple output voltage versions available:
  - Fixed outputs of 1 V to 4.3 V
  - Adjustable outputs from 1.25 V to 6 V
- High PSRR: 68 dB at 1 kHz
- Low noise: 13.2 $\mu V_{RMS}$
- Fast startup time: 45 µs
- Stable with a low-ESR, 2-µF output capacitor
- Excellent load and line transient response
- 2% overall accuracy (load, line, temperature, $V_{OUT}$ > 2.2 V)
- Low dropout: 280 mV at 500 mA
- 3-mm × 3-mm VSON-8 packages

## 2 Applications

- Automotive infotainment
- Navigation systems
- WiFi, WiMax modules
- Telematics systems
- Microprocessor power

## 3 Description

The TPS735-Q1 family of low-dropout (LDO), low-power linear regulators offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient responses are provided while consuming a very low 46 µA (typical) ground current.

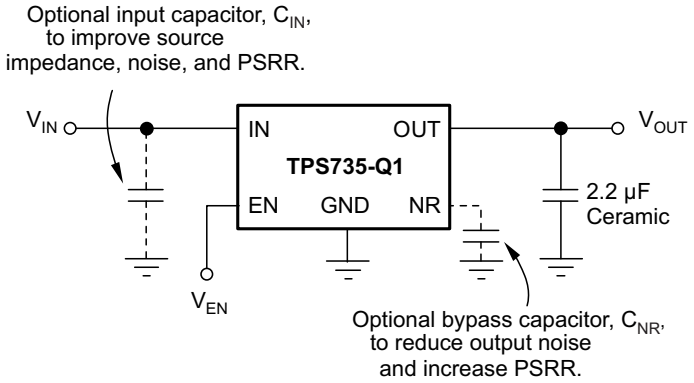
The TPS735-Q1 family of devices is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a typical dropout voltage of 280 mV at 500-mA output. The TPS735-Q1 family of devices uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% ($V_{OUT}$ > 2.2 V) over all load, line, process, and temperature variations. This family of devices is fully specified from $T_A$ = –40°C to 125°C and is offered in a low-profile, 3-mm × 3-mm VSON package.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS735-Q1 | VSON (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Typical Application**



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## 4 Revision History

**Changes from Revision A (January 2015) to Revision B** **Page**

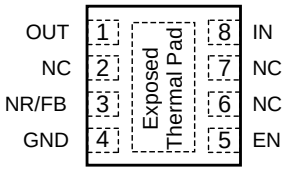
- Added title to first page figure ... 1
- Changed time scale from 10 ms to 10 µs in *TPS73525-Q1 Turn-On Response ($V_{IN}$ = $V_{EN}$)* figure ... 13
- Changed time scale from 10 ms to 10 µs in *TPS73525-Q1 Turn-On Response Using EN* figure ... 13

**Changes from Original (October 2014) to Revision A** **Page**

- Made changes to product preview document ... 1

# 5 Pin Configuration and Functions

**DRB Package**
**8-Pin VSON With Exposed Thermal Pad**
**Top View**




NC = No internal connection.

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 5 | I | Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. The EN pin can be connected to the IN pin if not used. |
| FB | 3 | I | This pin is only available for the adjustable version. The FB pin is the input to the control-loop error amplifier, and is used to set the output voltage of the device. |
| GND | 4 | — | Ground |
| IN | 8 | I | Input supply |
| NC | 2, 6, 7 | — | Not internally connected |
| NR | 3 | — | This pin is only available for the fixed voltage versions. Connecting an external capacitor to this pin bypasses noise generated by the internal band gap and allows the output noise to be reduced to very low levels. The maximum recommended capacitor is 0.01 µF. |
| OUT | 1 | O | This pin is the output of the regulator. A small 2-µF ceramic capacitor is required from this pin to ground to assure stability. |
| Exposed thermal pad | | — | The pad must be tied to the GND pin. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

At –40°C ≤ $T_J$ and $T_A$ ≤ 125°C (unless otherwise noted). All voltages are with respect to GND.(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$ | –0.3 | 7 | V |
| | $V_{EN}$ | –0.3 | $V_{IN}$ + 0.3 | V |
| | $V_{FB}$ | –0.3 | 1.6 | V |
| | $V_{OUT}$ | –0.3 | $V_{IN}$ + 0.3 | V |
| Current | $I_{OUT}$ | Internally limited | | A |
| Continuous total power dissipation | Continuous, $P_{D(tot)}$ | See the *Power Dissipation* section | | |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | °C |

(1) Stresses beyond those listed as *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | Corner pins (1, 4, 5, and 8) | ±750 | |
| | | | Other pins | ±500 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.7 | 6.5 | V |
| $V_{OUT}$ | Output voltage | $V_{FB}$ | 6 | V |
| $I_{OUT}$ | Output current(1) | 0 | 500 | mA |
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |

(1) When operating at $T_J$ near 125°C, $I_{OUT(min)}$ is 500 µA.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS735-Q1 DRB (VSON) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 54.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 71.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 28.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 28.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 9.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

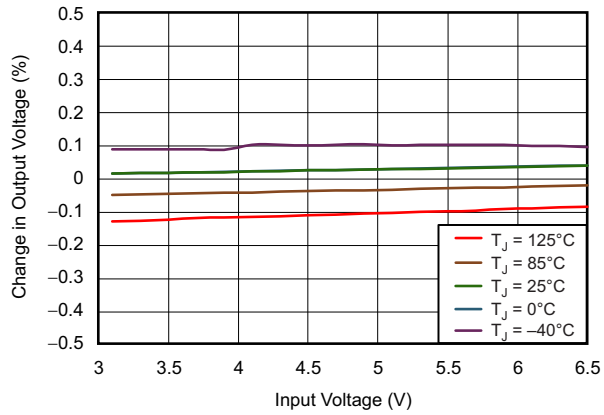
Over operating temperature range (–40°C ≤ $T_J$, $T_A$ ≤ 125°C), $V_{IN}$ = $V_{OUTnom}$ + 0.5 V or 2.7 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 2.2 µF, and $C_{NR}$ = 0.01 µF, unless otherwise noted.
For the adjustable version (TPS73501-Q1), $V_{OUT}$ = 3 V. Typical values are at $T_A$ = 25°C.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage(1) | | | 2.7 | | 6.5 | V |
| $V_{FB}$ | Internal reference (TPS73501-Q1) | $T_J$ = 25°C | | 1.196 | 1.208 | 1.220 | V |
| $V_{OUT}$ | Output voltage range (TPS73501-Q1) | | | $V_{FB}$ | | 6 | V |
| | DC output accuracy(1) | 1 mA ≤ $I_{OUT}$ ≤ 500 mA, $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ < 6.5 V | $V_{OUT}$ > 2.2 V | –2% | ±1% | 2% | |
| | | | $V_{OUT}$ ≤ 2.2 V | –3% | ±1% | 3% | |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation(1) | $V_{OUTnom}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V | | | 0.02 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation | 500 µA ≤ $I_{OUT}$ ≤ 500 mA | | | 0.005 | | %/mA |
| $V_{DO}$ | Dropout voltage(2) ($V_{IN}$ = $V_{OUTnom}$ – 0.1 V) | $I_{OUT}$ = 500 mA | | | 280 | 500 | mV |
| $I_{LIM}$ | Output current limit | $V_{OUT}$ = 0.9 × $V_{OUTnom}$, $V_{IN}$ = $V_{OUTnom}$ + 0.9 V, $V_{IN}$ ≥ 2.7 V | | 800 | 1170 | 1900 | mA |
| $I_{GND}$ | Ground pin current | 10 mA ≤ $I_{OUT}$ ≤ 500 mA | | | 45 | 65 | µA |
| $I_{SHDN}$ | Shutdown current | $V_{EN}$ ≤ 0 V | | | 0.15 | 1 | µA |
| $I_{FB}$ | Feedback pin current (TPS73501-Q1) | $V_{OUTnom}$ = 1.2 V | | –0.5 | | 0.5 | µA |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = 3.85 V, $V_{OUT}$ = 2.85 V, $C_{NR}$ = 0.01 µF, $I_{OUT}$ = 100 mA | f = 100 Hz | | 60 | | dB |
| | | | f = 1k Hz | | 68 | | dB |
| | | | f = 10 kHz | | 41 | | dB |
| | | | f = 100 kHz | | 21 | | dB |
| $V_n$ | Output noise voltage | BW = 10 Hz to 100 kHz, $V_{OUT}$ = 2.8 V | $C_{NR}$ = 0.01 µF | | 11 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| | | | $C_{NR}$ = none | | 95 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| $t_{STR}$ | Startup time | $C_{NR}$ = none | | | 45 | | µs |
| | | $C_{NR}$ = 0.001 µF | | | 45 | | µs |
| | | $C_{NR}$ = 0.01 µF | | | 50 | | µs |
| | | $C_{NR}$ = 0.047 µF | | | 50 | | µs |
| $V_{EN(HI)}$ | Enable high (enabled) | | | 1.2 | | | V |
| $V_{EN(LO)}$ | Enable low (shutdown) | | | | | 0.4 | V |
| $I_{EN(HI)}$ | Enable pin current, enabled | $V_{EN}$ = $V_{IN}$ = 6.5 V | | | 0.03 | 1 | µA |
| $T_{sd}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | | 165 | | °C |
| | | Reset, temperature decreasing | | | 145 | | °C |
| UVLO | Undervoltage lockout | $V_{IN}$ rising | | 1.9 | 2.2 | 2.65 | V |
| $V_{hys}$ | Hysteresis | $V_{IN}$ falling | | | 70 | | mV |

(1) Minimum $V_{IN}$ = $V_{OUT}$ + $V_{DO}$ or 2.7 V, whichever is greater.
(2) $V_{DO}$ is not measured for this family of devices with $V_{OUTnom}$ < 2.8 V because the minimum $V_{IN}$ = 2.7 V.

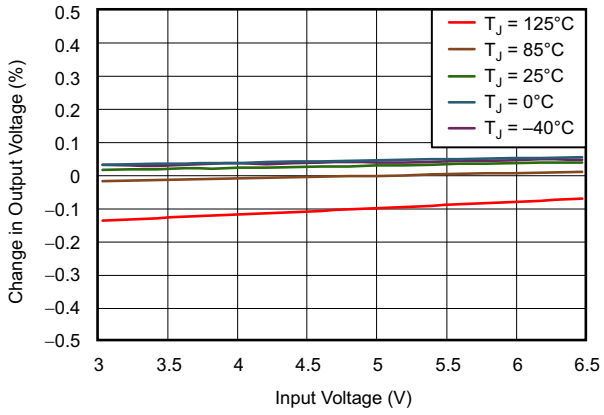
## 6.6 Typical Characteristics

Over operating temperature range (–40°C ≤ $T_J$, $T_A$ ≤ 125°C), $V_{IN}$ = $V_{OUTnom}$ + 0.5 V or 2.7 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 2.2 µF, and $C_{NR}$ = 0.01 µF, unless otherwise noted. $T_A$ = 25°C, unless otherwise noted.



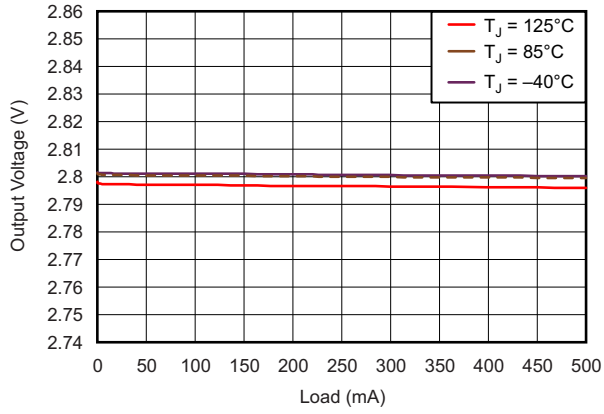

$I_{OUT}$ = 100 mA

**Figure 1. TPS73501-Q1 Line Regulation**



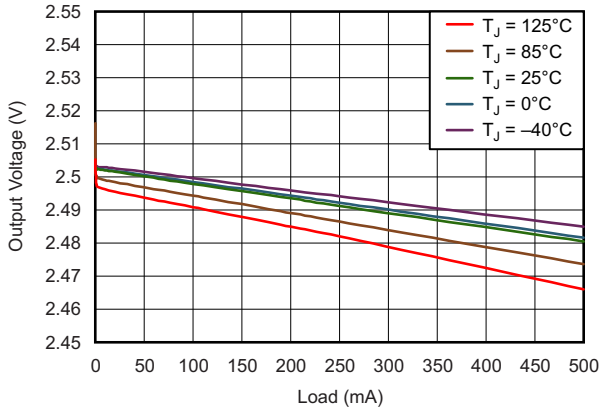

$I_{OUT}$ = 100 mA

**Figure 2. TPS73525-Q1 Line Regulation**




The y-axis range is ±2% of 2.8 V

**Figure 3. TPS73501-Q1 Load Regulation**




The y-axis range is ±2% of 2.5 V

**Figure 4. TPS73525-Q1 Load Regulation**

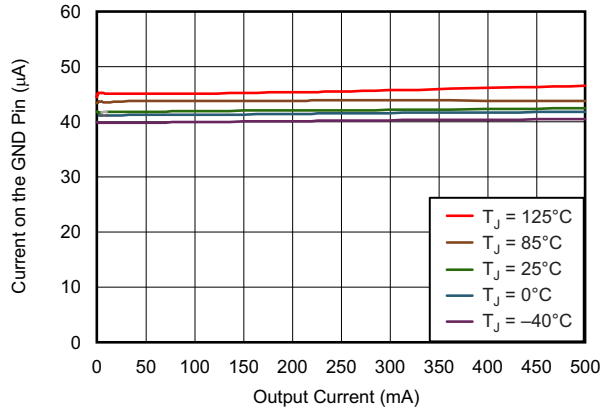
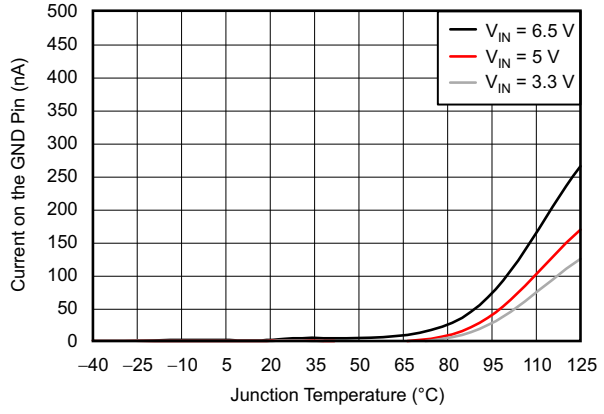



**Figure 5. TPS73525-Q1 Ground Pin Current vs Output Current**




$V_{EN}$ = 0.4 V

**Figure 6. TPS73525-Q1 Ground Pin Current (Disable) vs Temperature**

## Typical Characteristics (continued)

Over operating temperature range (–40°C ≤ $T_J$, $T_A$ ≤ 125°C), $V_{IN}$ = $V_{OUTnom}$ + 0.5 V or 2.7 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 2.2 µF, and $C_{NR}$ = 0.01 µF, unless otherwise noted. $T_A$ = 25°C, unless otherwise noted.

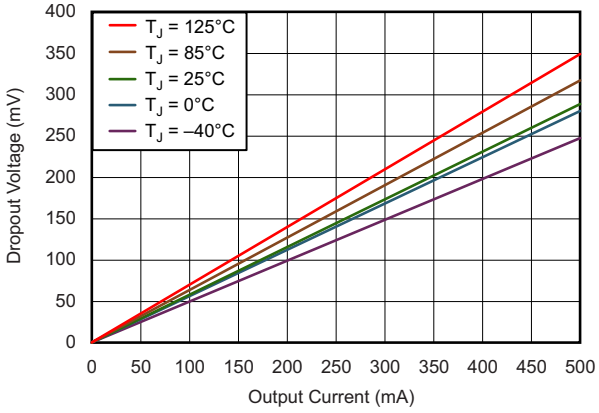



**Figure 7. TPS73501-Q1 Dropout Voltage vs Output Current**

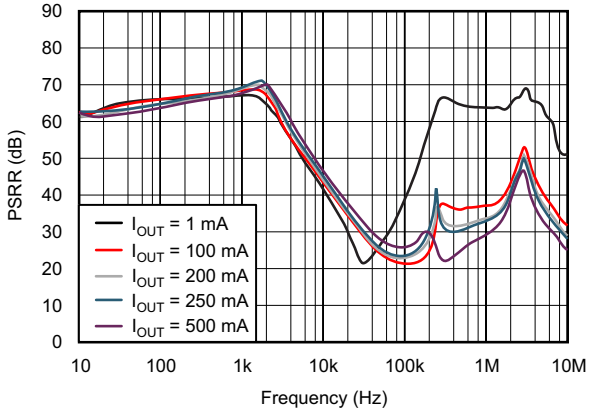



**Figure 8. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 1 V)**

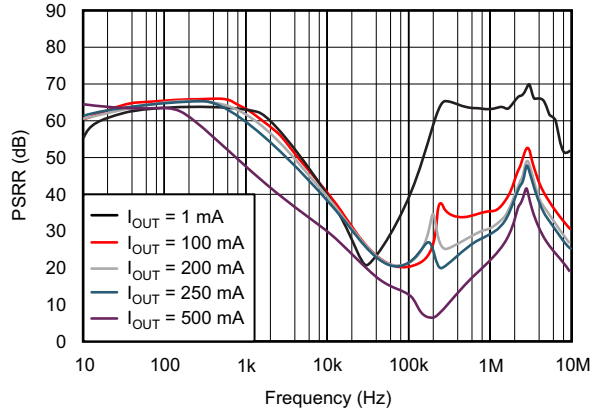



**Figure 9. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 0.5 V)**

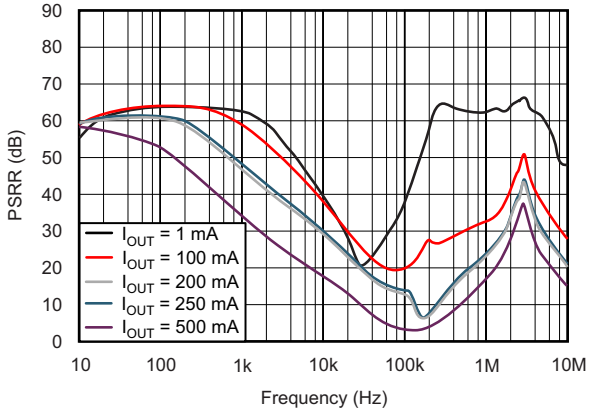



**Figure 10. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 0.3 V)**

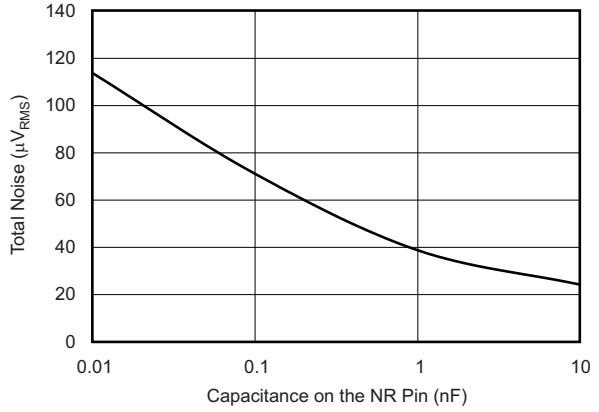
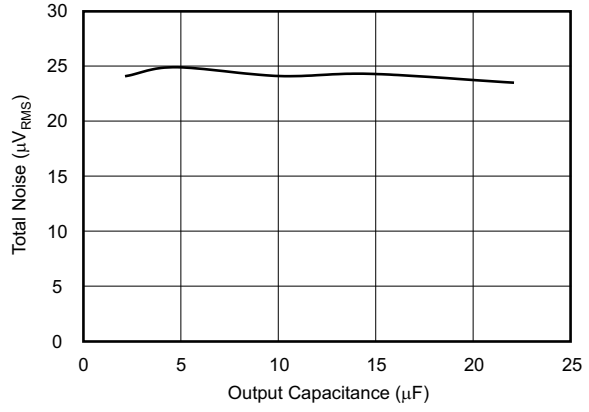



**Figure 11. TPS73525-Q1 RMS Noise vs $C_{NR}$**




$C_{NR}$ = 0.01 µF, $I_{OUT}$ = 1 mA

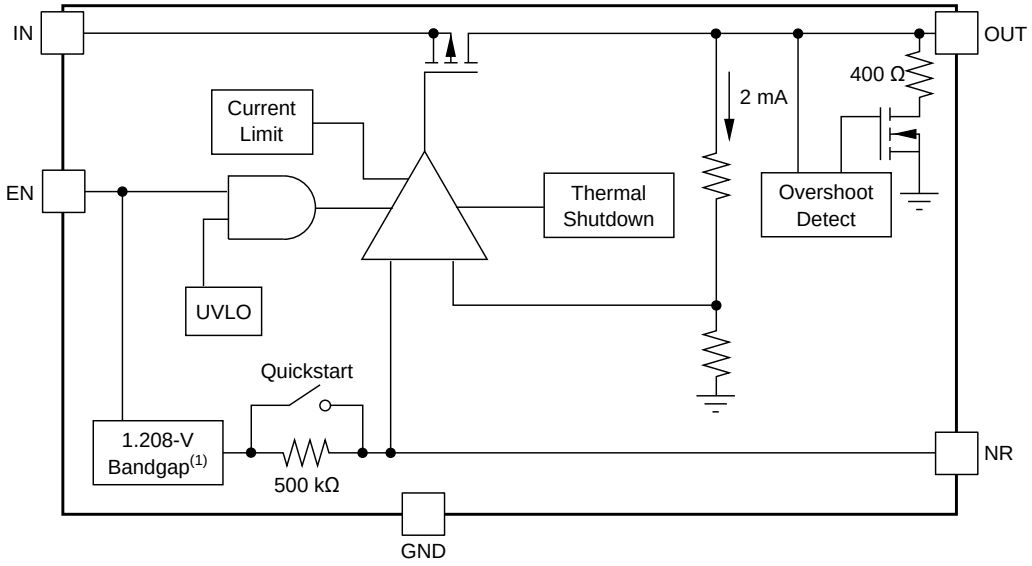
**Figure 12. TPS73525-Q1 RMS Noise vs $C_{OUT}$**

# 7 Detailed Description

## 7.1 Overview

The TPS735-Q1 family of low dropout (LDO) regulators combines the high performance required by many radio frequency (RF) and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection and very low headroom ($V_{IN}$ – $V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR. A quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS735-Q1 family of devices an excellent choice for portable applications. All versions have thermal and overcurrent protection and are fully specified from –40°C ≤ $T_J$, $T_A$ ≤ 125°C.

## 7.2 Functional Block Diagram




NOTE: Fixed voltage versions between 1 V to 1.2 V have a 1-V band-gap circuit instead of a 1.208-V band-gap circuit.

**Figure 13. Fixed Voltage Versions**

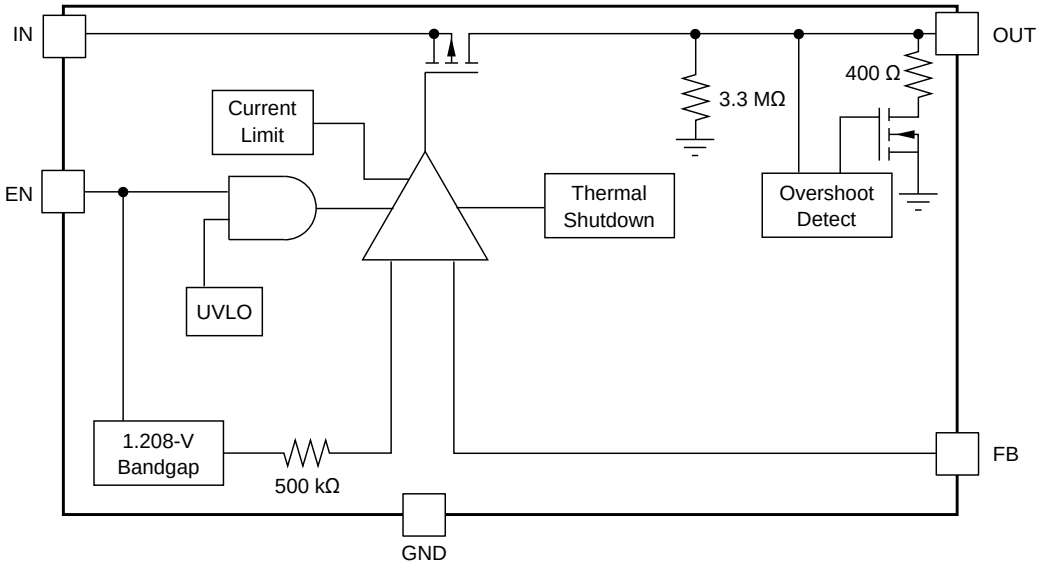



**Figure 14. Adjustable Voltage Versions**

## 7.3 Feature Description

### 7.3.1 Internal Current-Limit

The TPS735-Q1 internal current-limit helps protect the regulator during fault conditions. During current-limit, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in current-limit for extended periods of time.

The PMOS pass element in the TPS735-Q1 family of devices has a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting can be appropriate.

### 7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can be connected to the IN pin.

### 7.3.3 Dropout Voltage

The TPS735-Q1 family of devices uses a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in the linear region of operation and the input-to-output resistance ($R_{(IN/OUT)}$) of the PMOS pass element. $V_{DO}$ scales with the output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when ($V_{IN}$ – $V_{OUT}$) approaches dropout. This effect is shown in the *Typical Characteristics* section (see Figure 8 through Figure 10).

### 7.3.4 Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS735-Q1 family of devices use a quick-start circuit to fast-charge the noise reduction capacitor, $C_{NR}$, if present (see the *Functional Block Diagram* section). This architecture allows the combination of very-low output noise and fast startup times. The NR pin is high impedance so a low-leakage $C_{NR}$ capacitor must be used. Most ceramic capacitors are appropriate in this configuration. A high-quality, COG-type (NPO) dielectric ceramic capacitor is recommended for $C_{NR}$ when used in environments where abrupt changes in temperature can occur.

Note that for fastest start-up, apply $V_{IN}$ first, then drive the enable pin (EN) high. If the EN pin is tied to the IN pin, start-up is somewhat slower. Refer to the *Typical Application* section (see Figure 17 and Figure 18). The quick-start switch is closed for approximately 135 μs. To ensure that $C_{NR}$ is charged during the quick-start time, use a capacitor with a value of no more than 0.01 μF.

### 7.3.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the transient response duration. In the adjustable version, adding $C_{FB}$ between the OUT and FB pins improves stability and transient response performance. The transient response of the TPS735-Q1 family of devices is enhanced by an active pulldown that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 400-Ω resistor to ground.

### 7.3.6 Undervoltage Lockout (UVLO)

The TPS735-Q1 family of devices uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that the UVLO typically ignores undershoot transients on the input if the transients are less than 50 μs in duration.

### 7.3.7 Minimum Load

The TPS735-Q1 family of devices is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. Below 500 μA and at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown to turn on. The output pulldown limits voltage drift to 5% (typically) but ground current can increase by approximately 50 μA. In most applications, the junction does not reach high temperatures at light loads because very little power is dissipated. Therefore, the specified ground current is valid at no load in most applications.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO voltage and has not decreased below the UVLO threshold minus $V_{hys}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the thermal shutdown temperature.

### 7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is equal to the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and the LDO behaves like a resistor. Line or load transients in dropout can result in large output voltage deviations.

### 7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus $V_{hys}$, or has not yet exceeded the UVLO threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal mode | $V_{IN} > V_{OUTnom} + V_{DO}$ and $V_{IN} >$ UVLO | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{LIM}$ | $T_J < 165°C$ |
| Dropout mode | UVLO $< V_{IN} < V_{OUTnom} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | — | $T_J < 165°C$ |
| Disabled mode (any true condition disables the device) | $V_{IN} <$ UVLO $– V_{hys}$ | $V_{EN} < V_{EN(LO)}$ | — | $T_J > 165°C$ |

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS735-Q1 family of automotive-qualified LDO regulators provides a design with an ultra-low noise, high PSRR, low-dropout linear regulation with a very small ground current (46 µA, typical).

The devices are stable with ceramic capacitors, and have a dropout voltage of 280 mV at the full output rating of 500 mA. The features of the TPS735-Q1 family of devices enables the LDO regulators to be suitable for a wide variety of applications, with minimal design complexity.

## 8.2 Typical Application

Figure 15 shows the basic circuit connections for fixed-voltage models. Figure 16 gives the connections for the adjustable output version (TPS73501-Q1). Use the equation in Figure 16 to calculate the value of R1 and R2 for any output voltage.

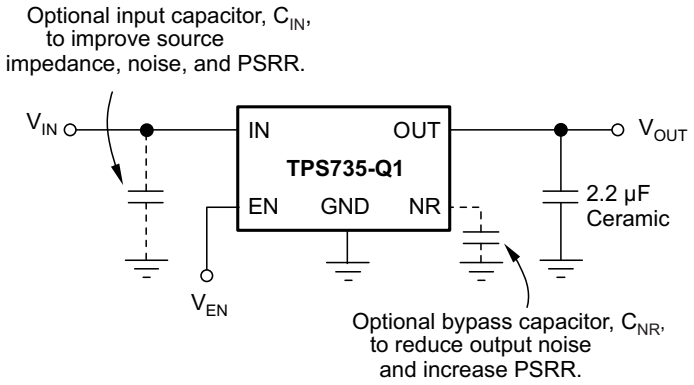



**Figure 15. Typical Application Circuit for Fixed Voltage Versions**

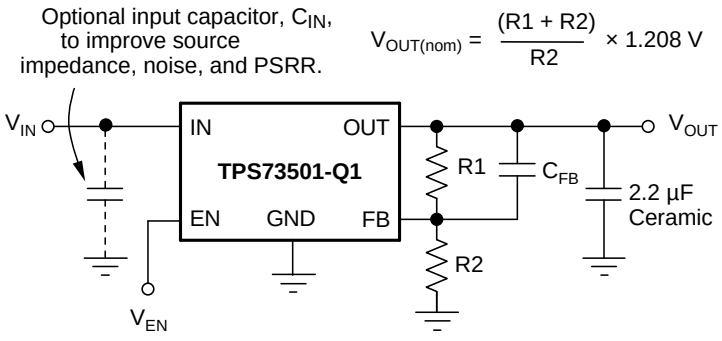



**Figure 16. Typical Application Circuit for Adjustable Voltage Versions**

## Typical Application (continued)

### 8.2.1 Design Requirements

#### *8.2.1.1 Input and Output Capacitor Requirements*

Although an input capacitor is not required for stability, connecting a 0.1-μF to 1-μF low-equivalent series-resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher-value capacitor can be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor can be necessary to ensure stability.

The TPS735-Q1 family of devices is designed to be stable with standard ceramic output capacitors of values 2 μF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor is < 1 Ω and, therefore, the output capacitor type must either be ceramic or conductive polymer electrolytic.

#### *8.2.1.2 Feedback Capacitor Requirements (TPS73501-Q1 only)*

The feedback capacitor ($C_{FB}$), shown in Figure 16, is required for stability. For a parallel combination of R1 and R2 equal to 250 kΩ, any value between 3 pF to 1 nF can be used. Fixed voltage versions have an internal 30-pF feedback capacitor that is quick-charged at start-up. Larger value capacitors also improve noise slightly. The TPS73501-Q1 device is stable in unity-gain configurations (the OUT pin is tied to the FB pin) without $C_{FB}$.

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Output Noise*

In most LDO regulators, the band gap is the dominant noise source. If a noise-reduction capacitor ($C_{NR}$) is used with the TPS735-Q1 family of devices, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output-resistor divider and the error-amplifier input. To minimize noise in a given application, use a 0.01-μF noise reduction capacitor. For the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2 μA of divider current has the same noise performance as a fixed voltage version with a $C_{NR}$. To further optimize noise, ESR of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing the total output noise up to 10%. The maximum recommended capacitor is 0.01 μF.

Equation 1 calculates the approximate integrated output noise from 10 Hz to 100 kHz with a $C_{NR}$ value of 0.01 μF.

$$V_n\ (\mu V_{RMS}) = 11\ (\mu V_{RMS} / V) \times V_{OUT}\ (V) \quad (1)$$

The TPS73501-Q1 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the previously listed recommendations.

## Typical Application (continued)

### 8.2.3 Application Curves

At $V_{IN}$ = $V_{OUTnom}$ + 0.5 V or 2.7 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 2.2 µF, $C_{NR}$ = 0.01 µF, and $T_A$ = 25°C, unless otherwise noted.

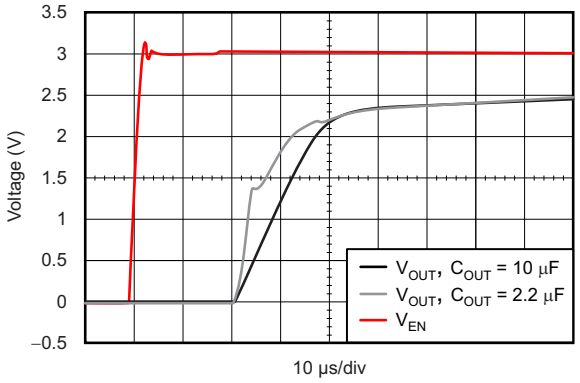



**Figure 17. TPS73525-Q1 Turn-On Response ($V_{IN}$ = $V_{EN}$)**

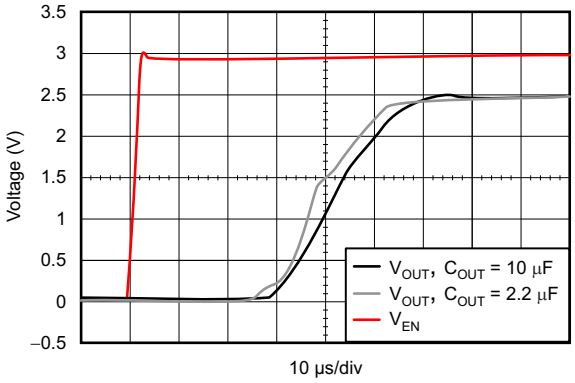



**Figure 18. TPS73525-Q1 Turn-On Response Using EN**

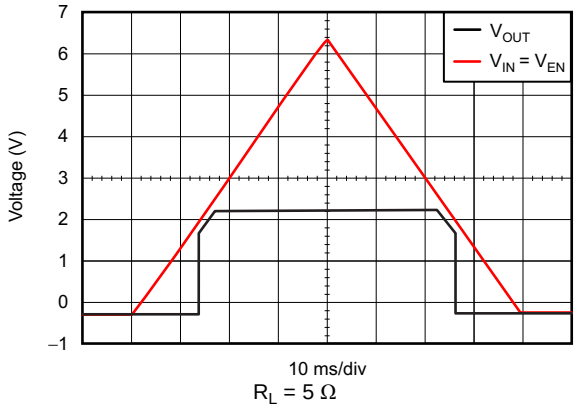



**Figure 19. TPS73525-Q1 Power-Up and Power-Down ($V_{IN}$ = $V_{EN}$)**

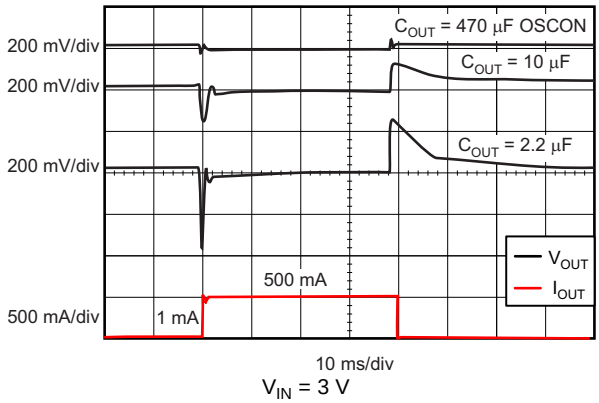



**Figure 20. TPS73525-Q1 Load Transient Response**

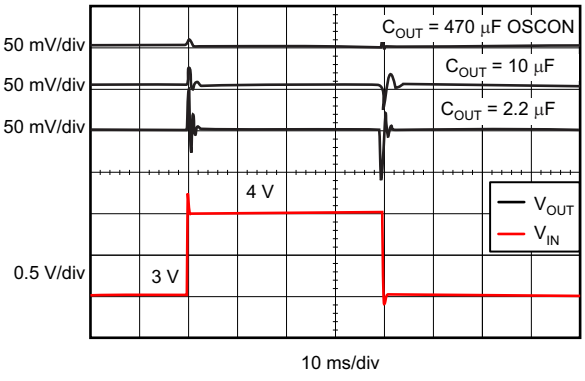



**Figure 21. TPS73525-Q1 Line Transient Response**

# 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

# 10 Layout

## 10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the PowerPAD™. In most applications, this ground plane is necessary to meet thermal requirements.

### 10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), designing the board with separate ground planes for $V_{IN}$ and $V_{OUT}$ is recommended, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

### 10.1.2 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the thermal margin in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 40°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS735-Q1 family of devices is designed to protect against overload conditions. This protection circuitry is not intended to replace proper heatsinking. Continuously running the TPS735-Q1 family of devices into thermal shutdown degrades device reliability.

### 10.1.3 Package Mounting

Solder pad footprint recommendations for the TPS735-Q1 family of devices are available from the Texas Instruments web site at www.ti.com.

### 10.1.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

## Layout Guidelines (continued)

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

**NOTE**

When the device is used in a condition of high input and low output voltages, $P_D$ can exceed the junction temperature rating even when the ambient temperature is at room temperature.

Equation 3 is an example calculation for the power dissipation ($P_D$) of the DRB package.

$$P_D = (6.5\ V – 1.2\ V) \times 500\ mA = 2.65\ W \quad (3)$$

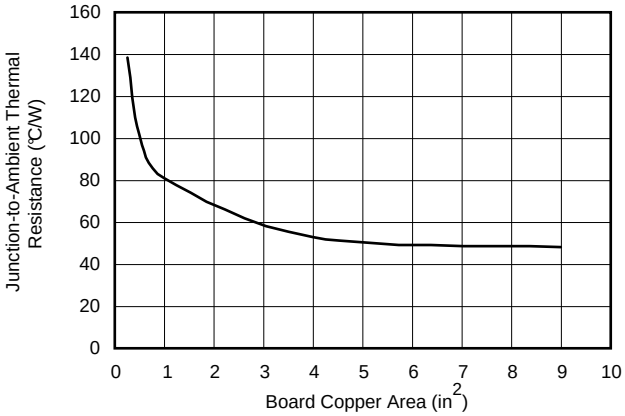
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output performance.

On the DRB package, the primary conduction path for heat is through the exposed thermal pad to the PCB. The pad can be connected to ground or left floating; however, the pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum allowable junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device. Use Equation 4 to calculate the maximum junction-to-ambient thermal resistance.

$$R_{\theta JA} = \frac{(125°C – T_A)}{P_D} \quad (4)$$

## Layout Guidelines (continued)

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 22.




NOTE: The $R_{\theta JA}$ value at a board size of 9 $in^2$ (that is, 3 in × 3 in) is a JEDEC standard.

**Figure 22. $R_{\theta JA}$ vs Board Size**

Figure 22 shows the variation of $R_{\theta JA}$ as a function of copper area in the board that is connected to the thermal pad. Figure 22 is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not to be used to calculate actual thermal performance.

**NOTE**

When the device is mounted on an application PCB, TI strongly recommends using $\Psi_{JT}$ and $\Psi_{JB}$, as explained in the *Estimating Junction Temperature* section.

### 10.1.5 Estimating Junction Temperature

Using the thermal metrics $\Psi_{JT}$ and $\Psi_{JB}$, as shown in the *Thermal Information* table, the junction temperature can be estimated with the corresponding formulas (given in Equation 5).

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D$$

where:

- $P_D$ is the power dissipation calculated with Equation 2,
- $T_T$ is the temperature at the center-top of the device package, and
- $T_B$ is the PCB temperature measured 1 mm away from the device package on the PCB surface (as shown in Figure 23). (5)

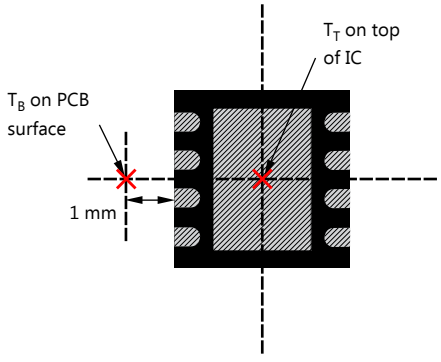



**Figure 23. Measuring Points for $T_T$ and $T_B$**

## Layout Guidelines (continued)

**NOTE**

Both $T_T$ and $T_B$ can be measured on actual application boards using an infrared thermometer.

For more information about measuring $T_T$ and $T_B$, see the application note, *Using New Thermal Metrics*, SBVA025.

According to Figure 24, the thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) have very little dependency on copper area. Using $\Psi_{JT}$ or $\Psi_{JB}$ with Equation 5 is a good way to estimate $T_J$ by simply measuring $T_T$ or $T_B$ on an application board.

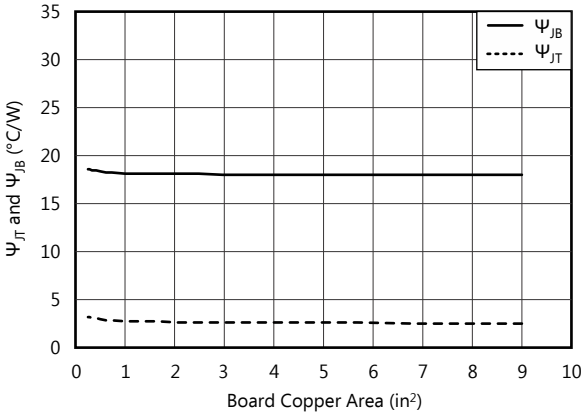
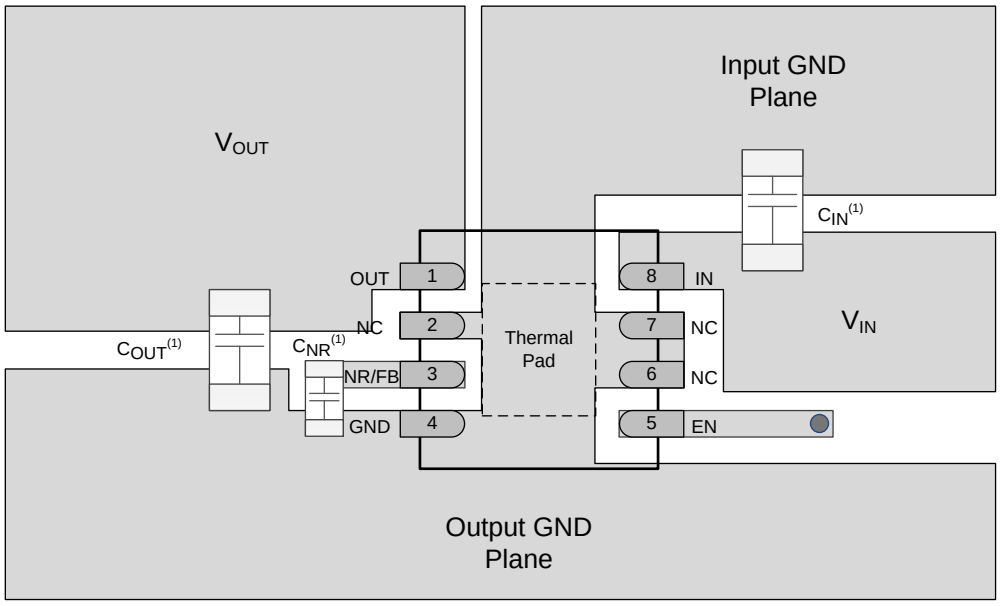



**Figure 24. $\Psi_{JT}$ and $\Psi_{JB}$ vs Board Size**

## 10.2 Layout Example




(1) $C_{IN}$ and $C_{OUT}$ are 0603 capacitors and $C_{NR}$ is a 0402 capacitor. The footprint is shown to scale with package size.

**Figure 25. TPS735-Q1 Fixed Version Layout Reference Diagram**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Device Nomenclature

**Table 2. Device Nomenclature(1)**

| PRODUCT | $V_{OUT}$ |
|---|---|
| TPS735**xx(x)***yyyz* | **XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 33 = 3.3 V; 125 = 1.25 V).<br>**YYY** is the package designator.<br>**Z** is the tape and reel quantity (R = 3000, T = 250).<br>**01** is the adjustable version. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Semiconductor and IC package thermal metrics* application report
- Texas Instruments, *TPS735xxEVM-276* user's guide
- Texas Instruments, *Using new thermal metrics* application report

## 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 Trademarks

E2E is a trademark of Texas Instruments.
PowerPAD is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

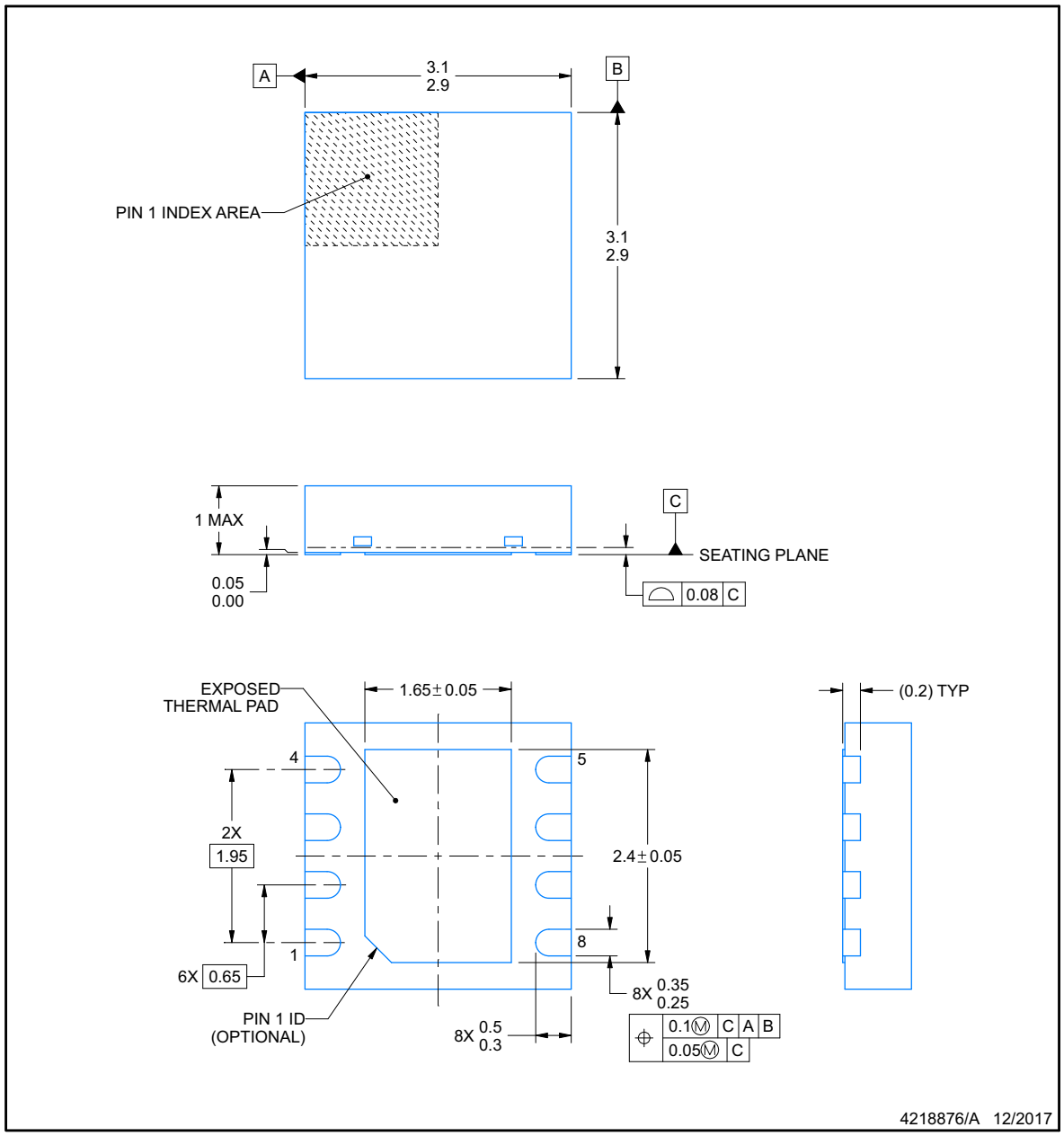
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated family of devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OUTLINE

## DRB0008B

## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

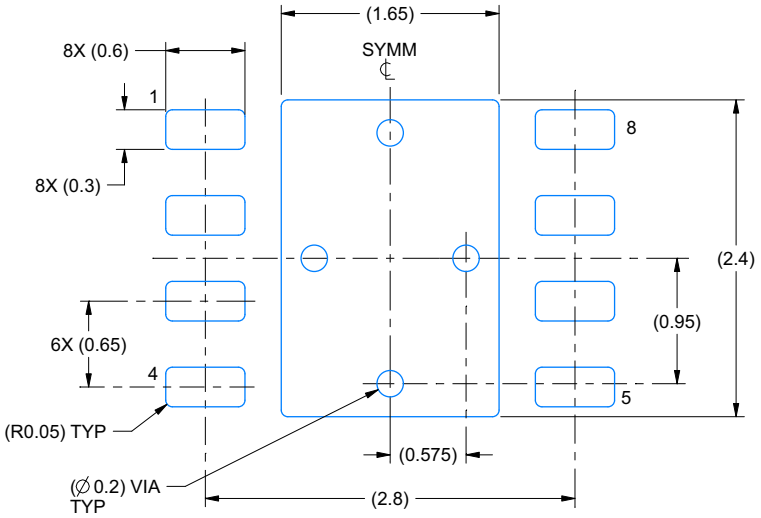
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

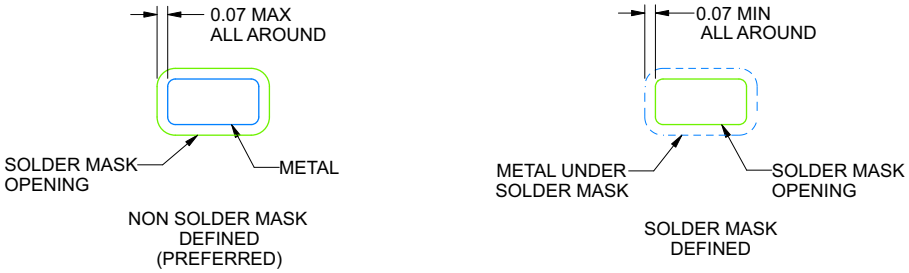
## DRB0008B

### VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
SCALE:20X




SOLDER MASK DETAILS

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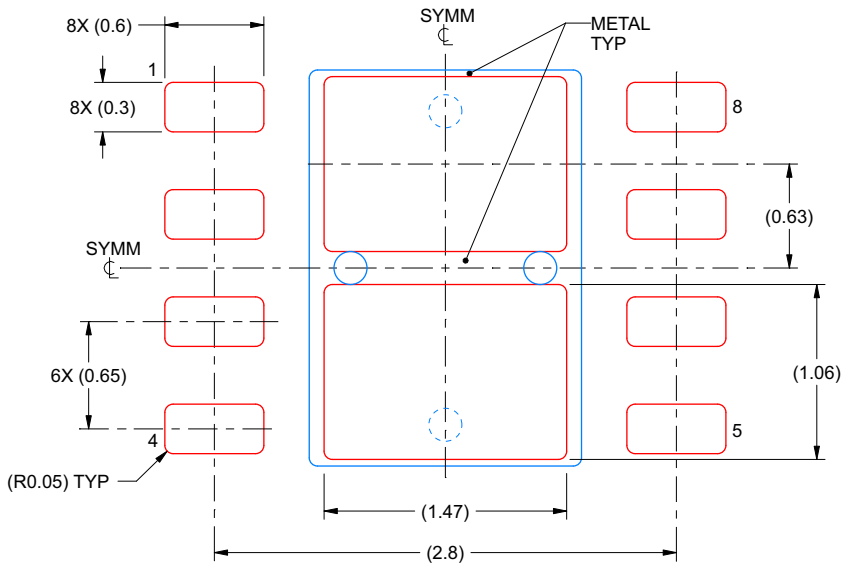
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**DRB0008B** — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS73501QDRBRQ1 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 501DRB |
| TPS73501QDRBRQ1.B | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 501DRB |
| TPS73512QDRBRQ1 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 512DRB |
| TPS73512QDRBRQ1.B | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 512DRB |
| TPS73515QDRBRQ1 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 515DRB |
| TPS73515QDRBRQ1.B | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 515DRB |
| TPS73518QDRBRQ1 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 518DRB |
| TPS73518QDRBRQ1.B | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 518DRB |
| TPS73525QDRBRQ1 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 525DRB |
| TPS73525QDRBRQ1.B | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 525DRB |
| TPS73527QDRBRQ1 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 527DRB |
| TPS73527QDRBRQ1.B | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 527DRB |
| TPS73530QDRBRQ1 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 530DRB |
| TPS73530QDRBRQ1.B | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 530DRB |
| TPS73533QDRBRQ1 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 533DRB |
| TPS73533QDRBRQ1.B | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 533DRB |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF TPS735-Q1 :**

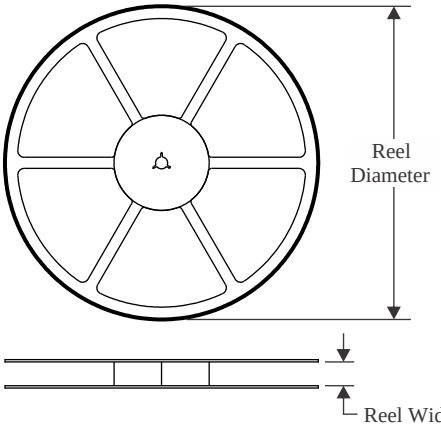
- Catalog : TPS735

NOTE: Qualified Version Definitions:

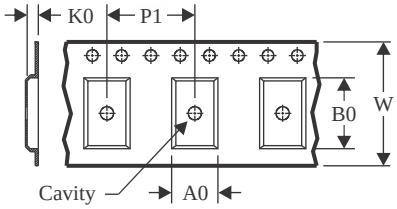
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

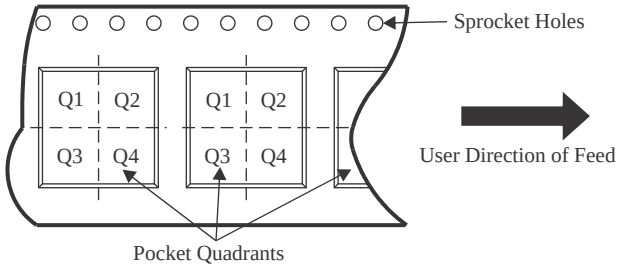



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

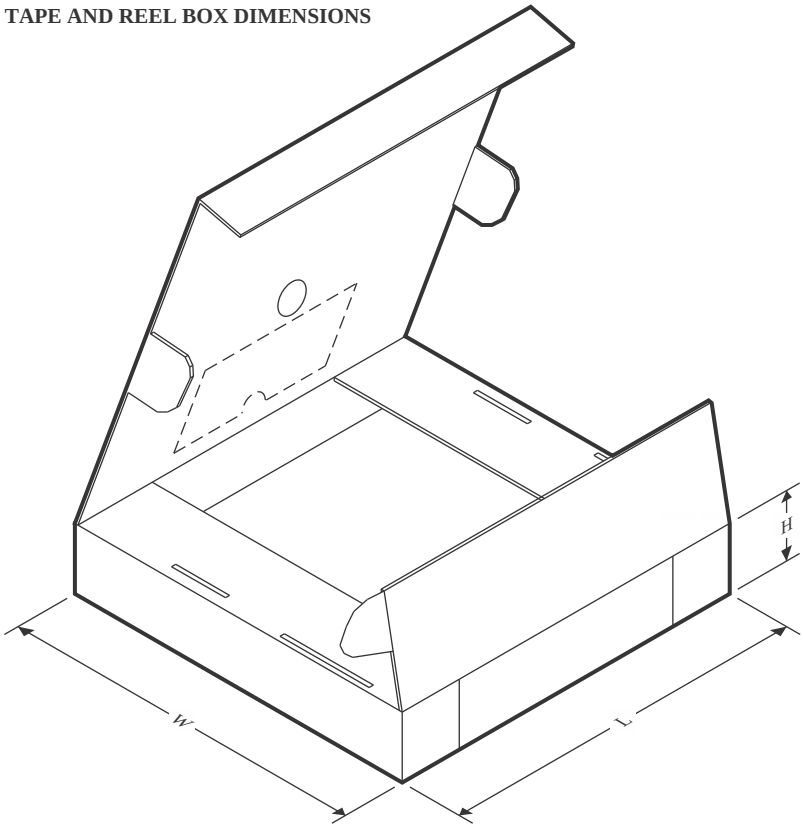
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS73501QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73512QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73515QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73518QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73525QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73527QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73530QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73533QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS73501QDRBRQ1 | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| TPS73512QDRBRQ1 | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| TPS73515QDRBRQ1 | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| TPS73518QDRBRQ1 | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| TPS73525QDRBRQ1 | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| TPS73527QDRBRQ1 | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| TPS73530QDRBRQ1 | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| TPS73533QDRBRQ1 | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |

## GENERIC PACKAGE VIEW

# DRB 8

# VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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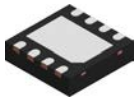
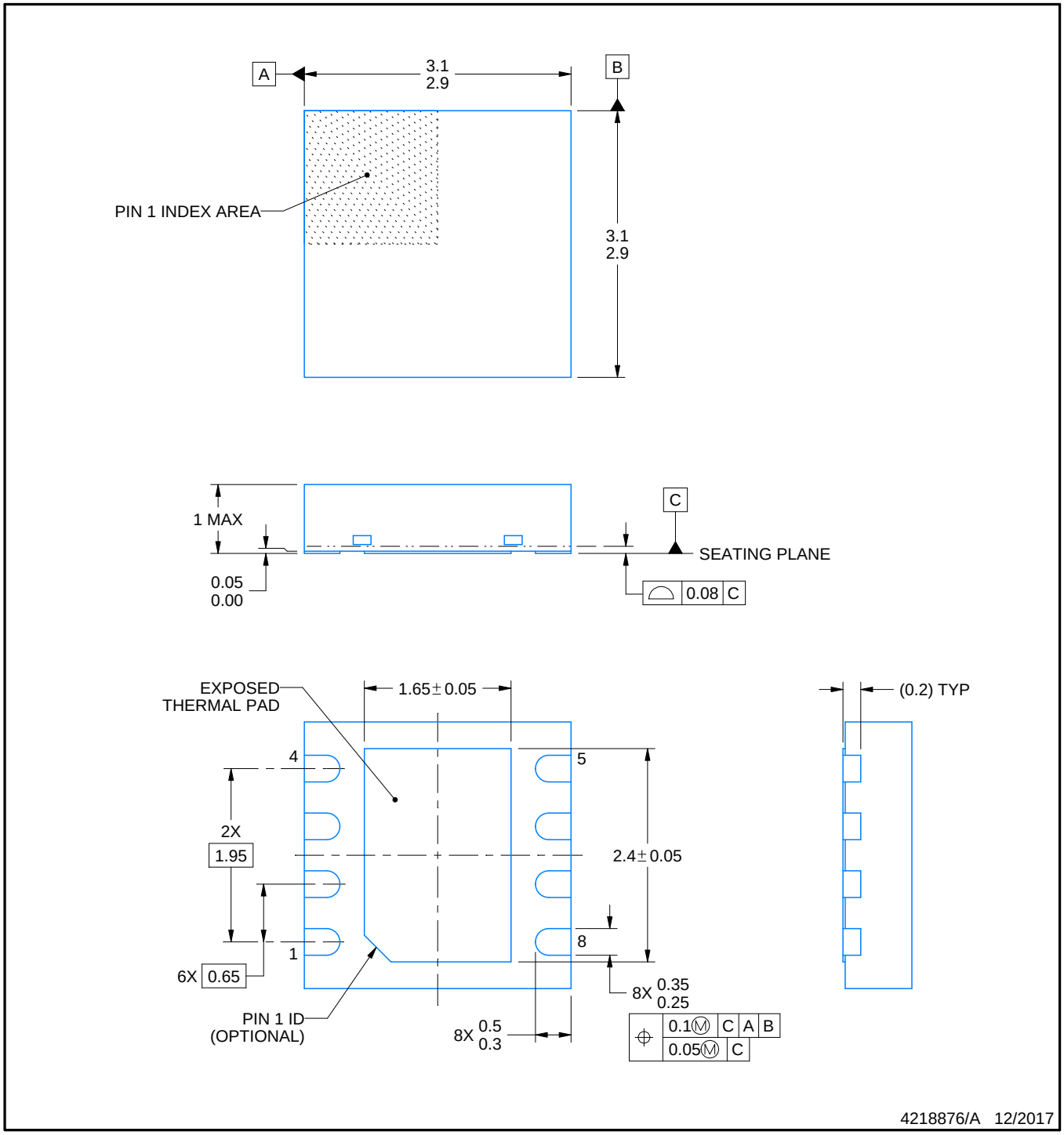
# DRB0008B



# PACKAGE OUTLINE

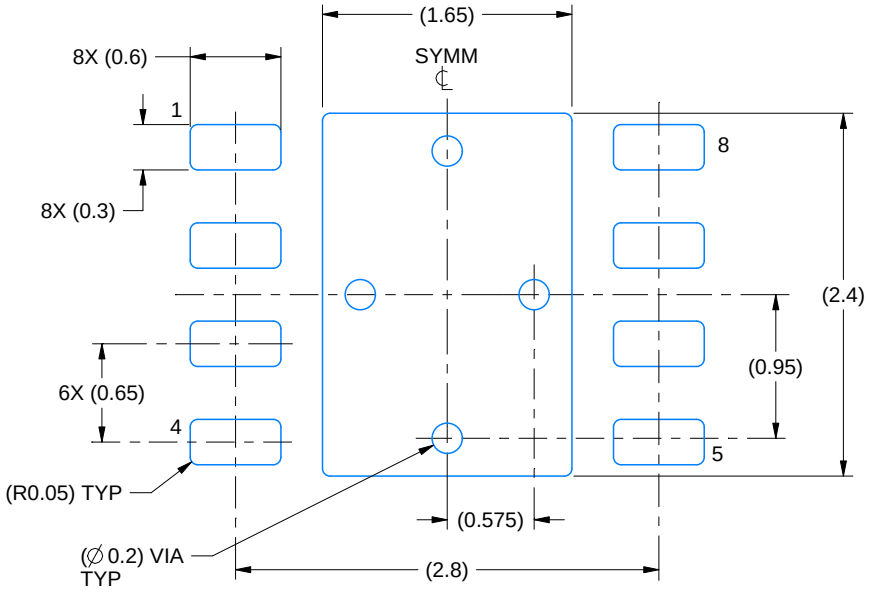
## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

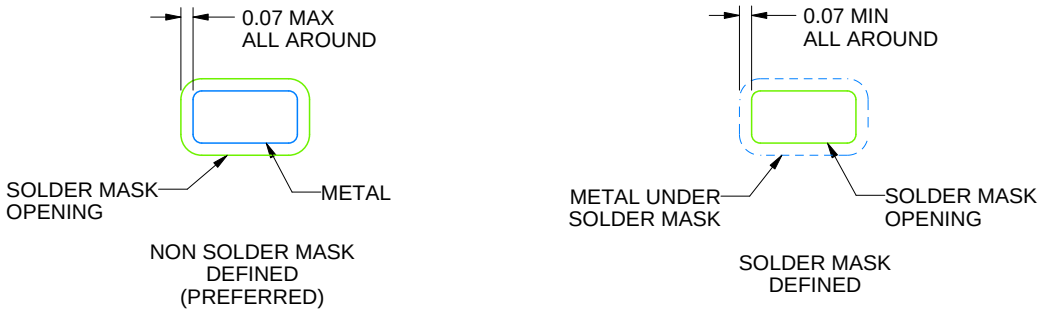



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X




SOLDER MASK DETAILS

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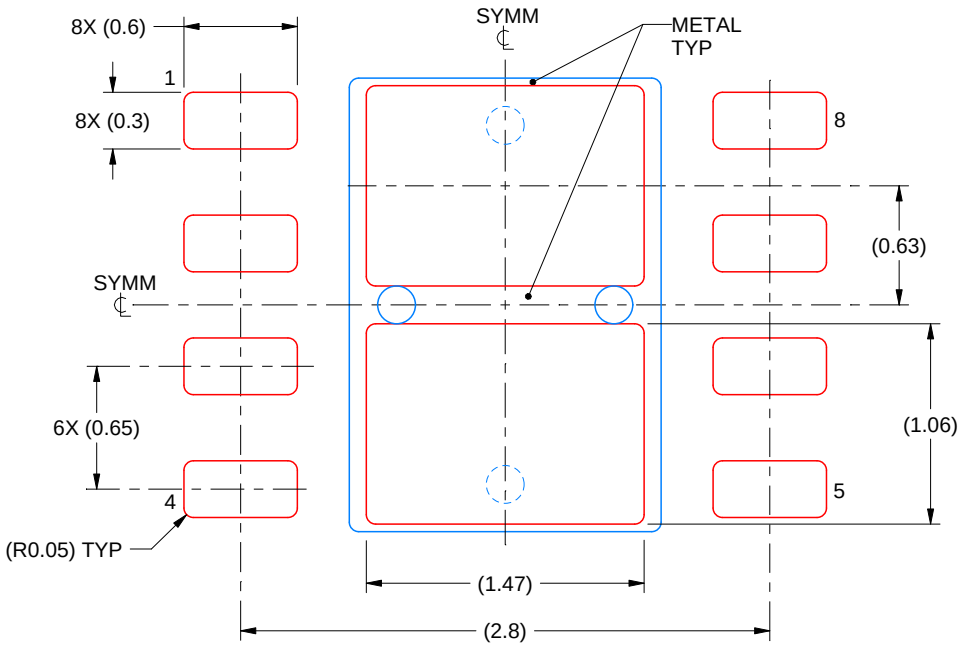
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025