TPS731 Capacitor-Free, NMOS, 150mA, Low-Dropout Regulator With Reverse Current Protection

1 Features

- Stable with or without capacitors of all types
- Input voltage range of 1.7V to 5.5V
- Ultra-low dropout voltage: 30mV typical (150mA load)
- Excellent load transient response—with or without optional output capacitor
- New NMOS topology provides low reverse leakage current
- Low noise: 30μV_{RMS} typical (10kHz to 100kHz)
- 0.5% initial accuracy
- 1% overall accuracy over line, load, and temperature
- Less than 1μA maximum I_Q in shutdown mode
- Thermal shutdown and specified minimum and maximum current-limit protection
- Available in multiple output voltage versions:
  - Fixed outputs: 1.20V to 5V
  - Adjustable outputs: 1.2V to 5.5V
  - Custom outputs available

2 Applications

- Smart grid and energy
- Building automation
- Set-top boxes
- Medical equipment
- Test and measurement
- Point-of-sale terminals
- Wireless infrastructure

3 Description

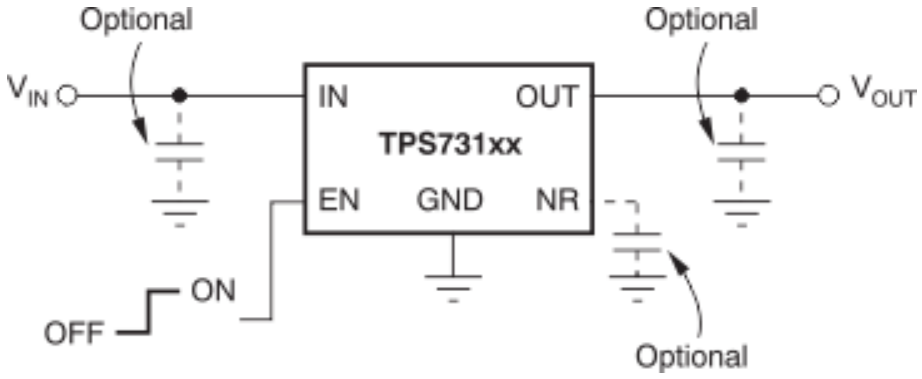
The TPS731 low-dropout (LDO) linear voltage regulator uses an NMOS pass transient in a voltage-follower configuration. This topology is stable using output capacitors with low equivalent series resistance (ESR), and even allows operation without a capacitor. The device also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS731 uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is less than 1μA and is designed for portable applications. The extremely low output noise (30μV_{RMS} with 0.1μF C_{NR}) is designed for powering VCOs. This device is protected by thermal shutdown and foldback current limit.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS731	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit for Fixed-Voltage Versions

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4 Pin Configuration and Functions

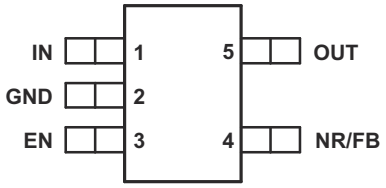


Figure 4-1. DBV Package, 5-Pin SOT-23, Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN	3	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the *Enable Pin and Shutdown* section for more details. EN can be connected to IN if not used.
FB	4	I	Adjustable-voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	2	—	Ground.
IN	1	I	Input supply.
NR	4	—	Fixed-voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
OUT	5	O	Output of the regulator. There are no output capacitor requirements for stability.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	6	
	Output, V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.7		5.5	V
I_{OUT}	Output current	0		150	mA
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS731 New silicon	TPS731 Legacy silicon	UNIT
		DBV (SOT-23)	DBV (SOT-23)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.2	207.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.9	124.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.1	35	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.1	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.7	34.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

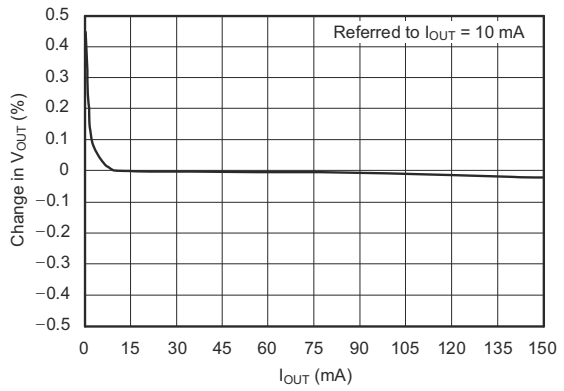
Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V[1] , I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted). Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range[1]			1.7		5.5	V
V_{FB}	Internal reference (TPS73101)	T_J = 25°C		1.198	1.204	1.210	V
V_{OUT}	Output voltage range (TPS73101)[2]			V_{FB}		5.5 - V_{DO}	V
	Accuracy[1] [3]	Nominal	T_J = 25°C	–0.5		0.5	%
		V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 150mA	–1	±0.5	1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation [1]	$V_{OUT(nom)}$ + 0.5V ≤ V_{IN} ≤ 5.5V			0.01		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 150mA			0.002		%/mA
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	10mA ≤ I_{OUT} ≤ 150mA			0.0005		%/mA
V_{DO}	Dropout voltage[4] (V_{IN} = $V_{OUT(NOM)}$ - 0.1V)	I_{OUT} = 150mA			30	100	mV
$Z_{O(DO)}$	Output impedance in dropout	1.7V ≤ V_{IN} ≤ V_{OUT} + V_{DO}			0.25		Ω
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$		150	360	500	mA
I_{SC}	Short-circuit current	V_{OUT} = 0V			200		mA
I_{REV}	Reverse leakage current[5] (-I_{IN})	V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT}			0.1	10	µA
I_{GND}	Ground pin current	I_{OUT} = 10mA (I_Q), legacy silicon			400	550	µA
		I_{OUT} = 10mA (I_Q), new silicon			400	630	
I_{GND}	Ground pin current	I_{OUT} = 10mA (I_Q), V_{OUT} = 5V only, new silicon			580	700	µA
I_{GND}	Ground pin current	I_{OUT} = 150mA			550	750	µA
I_{GND}	Ground pin current	I_{OUT} = 150mA, V_{OUT} = 5V only, new silicon			700	850	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V, –40°C ≤ T_J ≤ 100°C, legacy silicon			0.02	1	µA
		V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V, new silicon			0.02	1	
I_{FB}	Feedback pin current (TPS73101)				0.1	0.3	µA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100Hz, I_{OUT} = 150mA			58		dB
		f = 10kHz, I_{OUT} = 150mA			37		
V_N	Output noise voltage, BW = 10Hz to 100kHz	C_{OUT} = 10µF, no C_{NR}			27 × V_{OUT}		μV_{RMS}
		C_{OUT} = 10µF, C_{NR} =0.01µF			8.5 × V_{OUT}		
t_{STR}	Startup time	V_{OUT} = 3V, R_L = 30Ω, C_{OUT} = 1µF, C_{NR} = 0.01µF			600		µs
$V_{EN(high)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(high)}$	Enable pin current (enabled)	V_{EN} = 5.5V			0.02	0.1	µA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		
T_J	Operating junction temperature			–40		125	℃

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7V, whichever is greater.
(2) TPS73101 is tested at V_{OUT} = 2.5V.
(3) Tolerance of external resistors not included in this specification.
(4) V_{DO} is not measured for output versions with $V_{OUT(nom)}$ < 1.8V, because minimum V_{IN} = 1.7V.
(5) Fixed-voltage versions only; refer to *Application Information* section for more information.

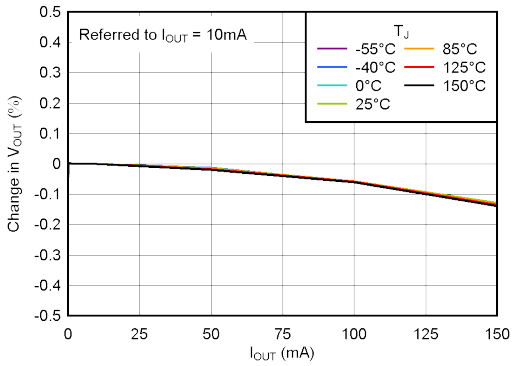
5.6 Typical Characteristics

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



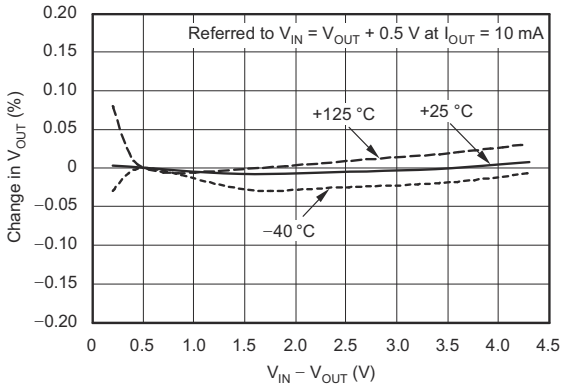
Legacy silicon

Figure 5-1. Load Regulation



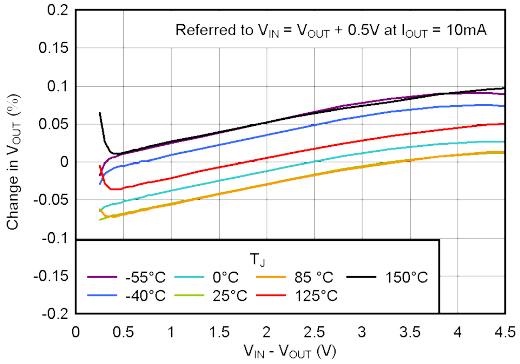
New silicon

Figure 5-2. Load Regulation



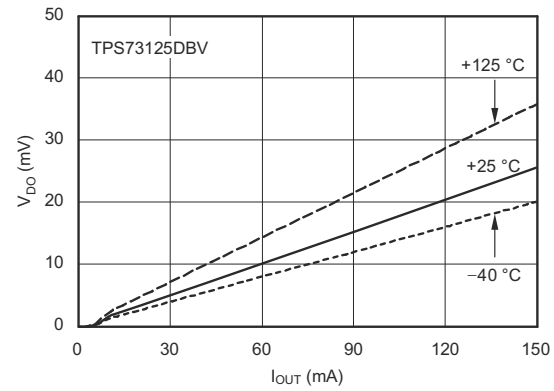
Legacy silicon

Figure 5-3. Line Regulation



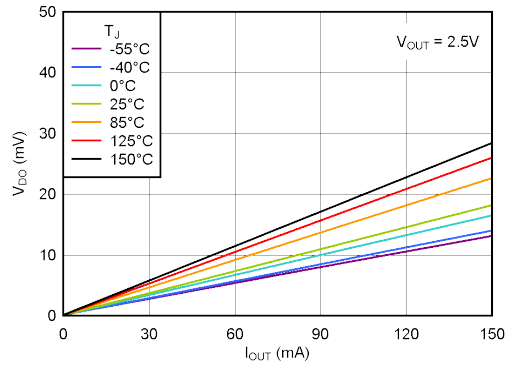
New silicon

Figure 5-4. Line Regulation



Legacy silicon

Figure 5-5. Dropout Voltage vs Output Current

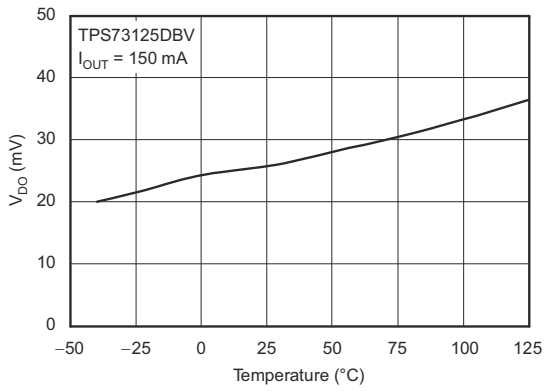


New silicon

Figure 5-6. Dropout Voltage vs Output Current

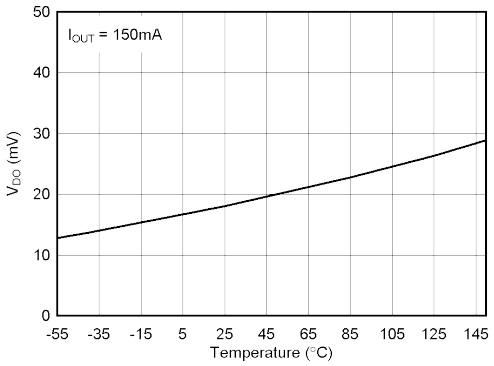
5.6 Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



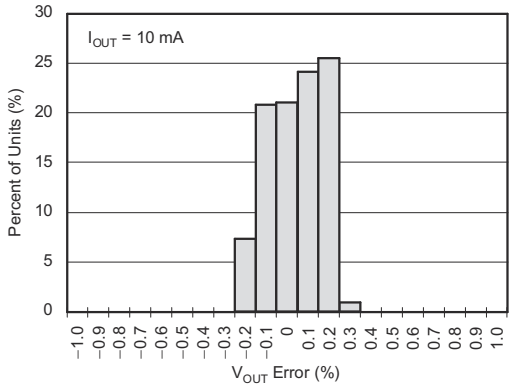
Legacy silicon

Figure 5-7. Dropout Voltage vs Temperature



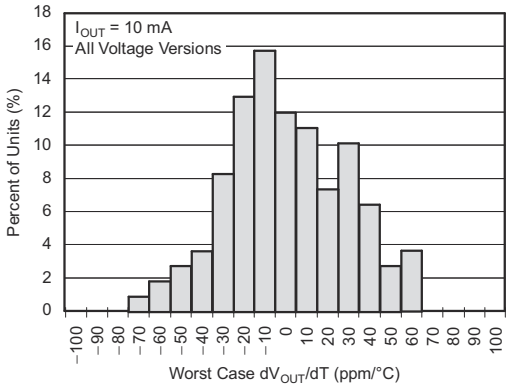
New silicon

Figure 5-8. Dropout Voltage vs Temperature



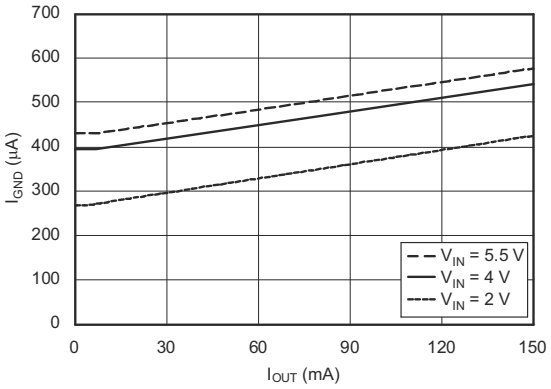
Legacy silicon

Figure 5-9. Output Voltage Accuracy Histogram



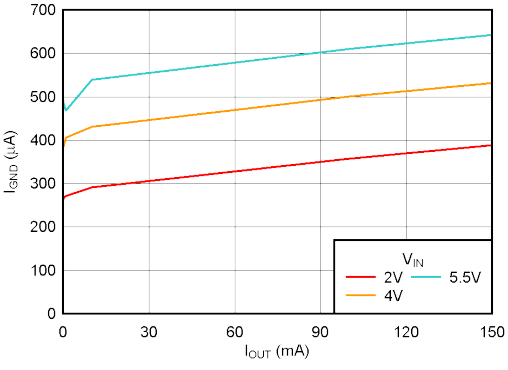
Legacy silicon

Figure 5-10. Output Voltage Drift Histogram



Legacy silicon

Figure 5-11. Ground Pin Current vs Output Current

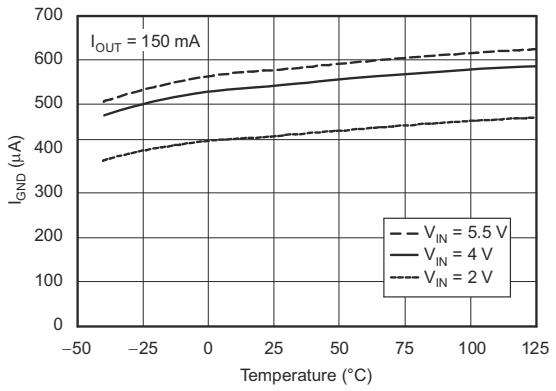


New silicon

Figure 5-12. Ground Pin Current vs Output Current

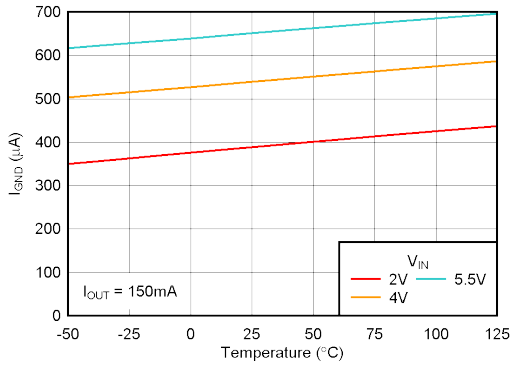
5.6 Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



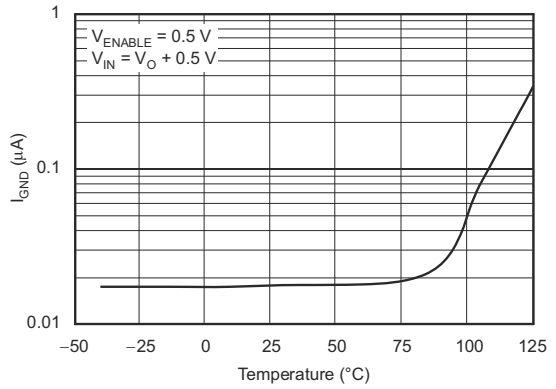
Legacy silicon

Figure 5-13. Ground Pin Current vs Temperature



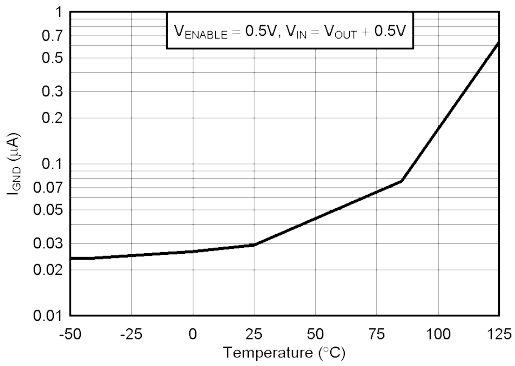
New silicon

Figure 5-14. Ground Pin Current vs Temperature



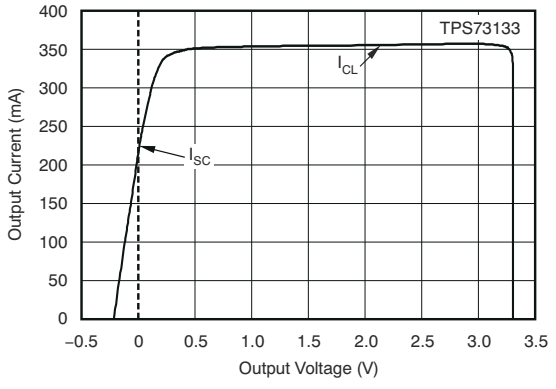
Legacy silicon

Figure 5-15. Ground Pin Current in Shutdown vs Temperature



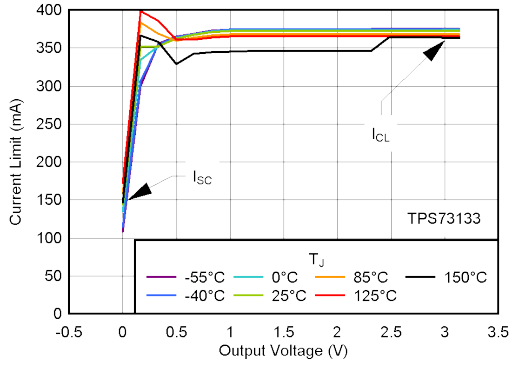
New silicon

Figure 5-16. Ground Pin Current in Shutdown vs Temperature



Legacy silicon

Figure 5-17. Current Limit vs V_{OUT} (Foldback)

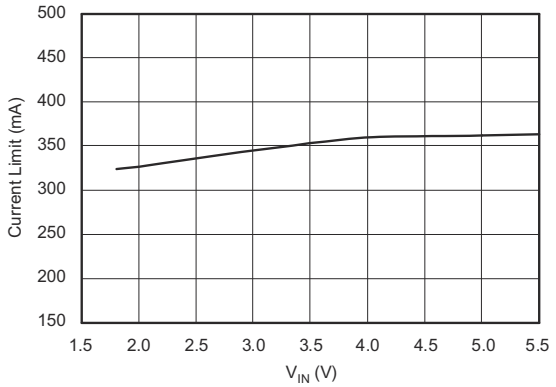


New silicon

Figure 5-18. Current Limit vs V_{OUT} (Foldback)

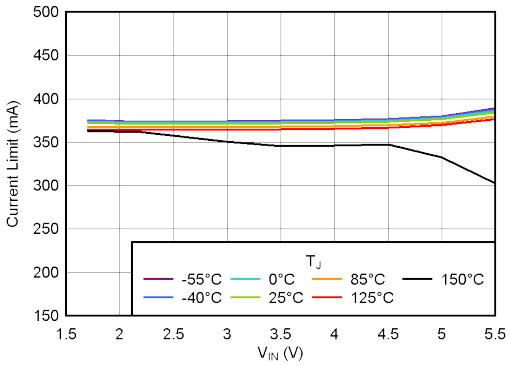
5.6 Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



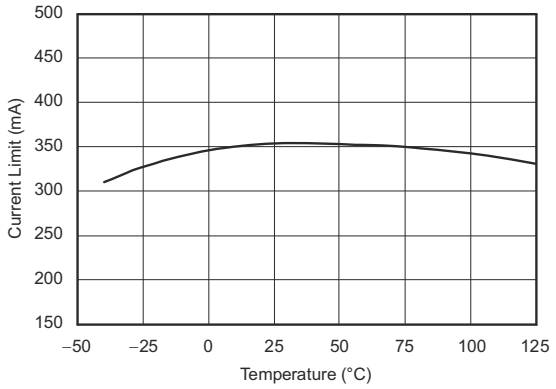
Legacy silicon

Figure 5-19. Current Limit vs V_{IN}



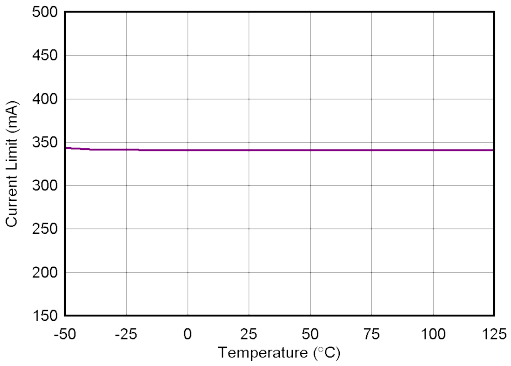
New silicon

Figure 5-20. Current Limit vs V_{IN}



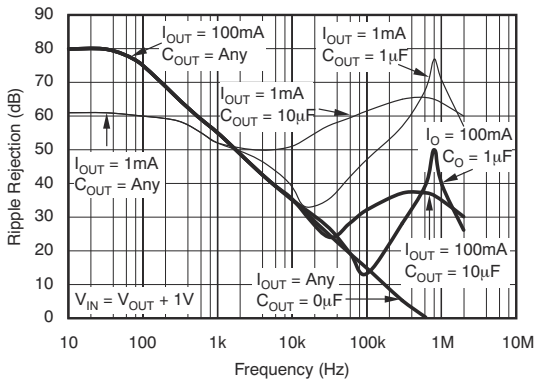
Legacy silicon

Figure 5-21. Current Limit vs Temperature



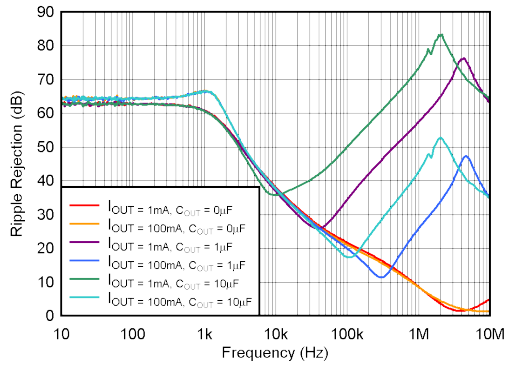
New silicon

Figure 5-22. Current Limit vs Temperature



Legacy silicon

Figure 5-23. PSRR (Ripple Rejection) vs Frequency

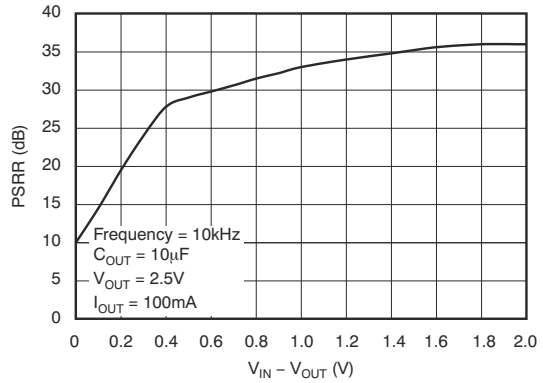


New silicon

Figure 5-24. PSRR (Ripple Rejection) vs Frequency

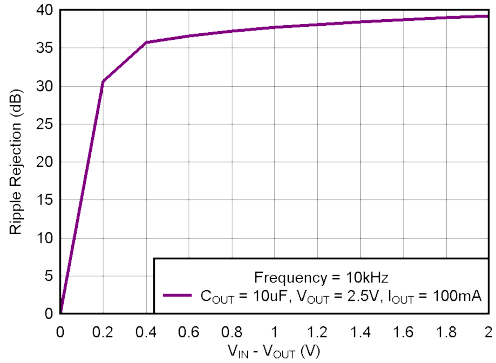
5.6 Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



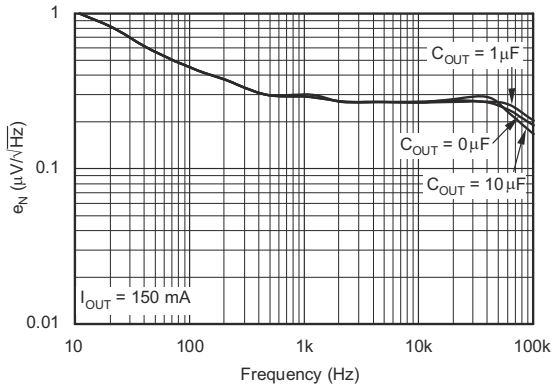
Legacy silicon

Figure 5-25. PSRR (Ripple Rejection) vs V_{IN} – V_{OUT}



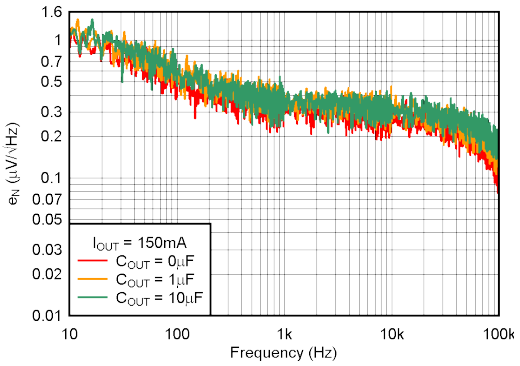
New silicon

Figure 5-26. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})



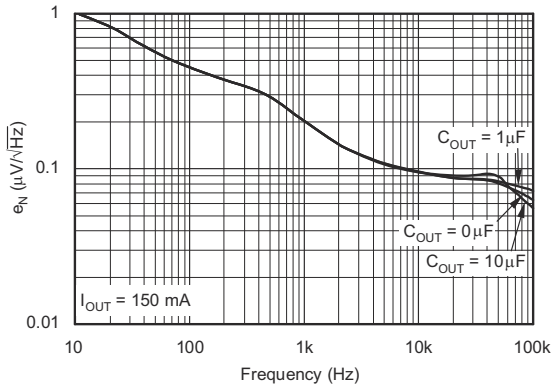
Legacy silicon

Figure 5-27. Noise Spectral Density C_{NR} = 0µF



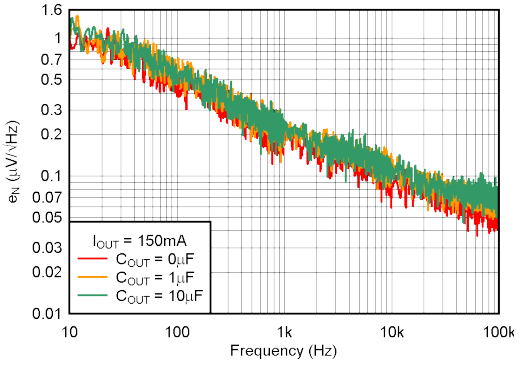
New silicon

Figure 5-28. Noise Spectral Density C_{NR} = 0µF



Legacy silicon

Figure 5-29. Noise Spectral Density C_{NR} = 0.01µF

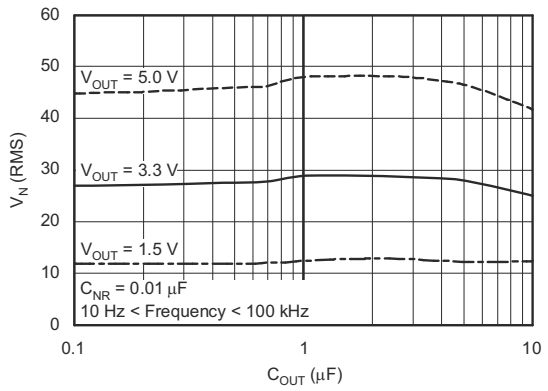


New silicon

Figure 5-30. Noise Spectral Density C_{NR} = 0.01µF

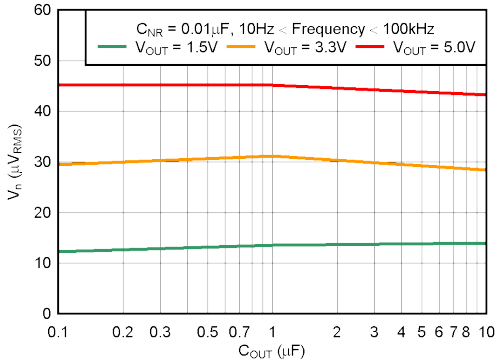
5.6 Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



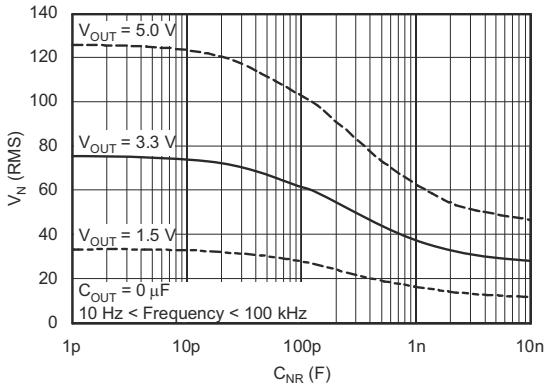
Legacy silicon

Figure 5-31. RMS Noise Voltage vs C_{OUT}



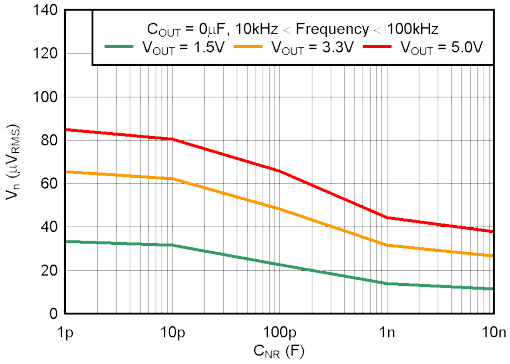
New silicon

Figure 5-32. RMS Noise Voltage vs C_{OUT}



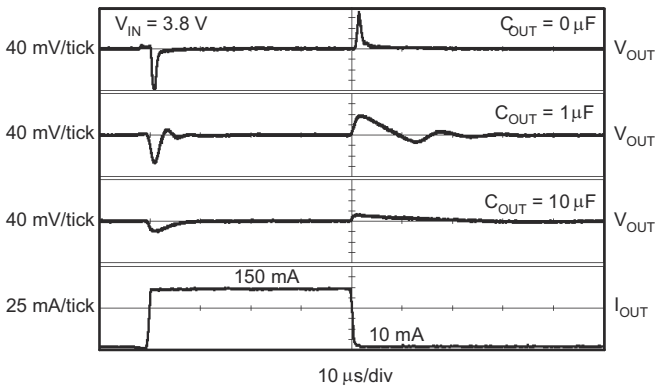
Legacy silicon

Figure 5-33. RMS Noise Voltage vs C_{NR}



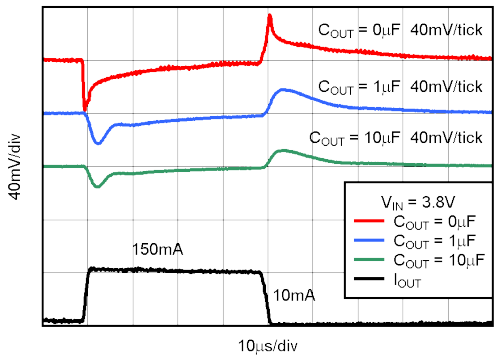
New silicon

Figure 5-34. RMS Noise Voltage vs C_{NR}



Legacy silicon

Figure 5-35. TPS73133 Load Transient Response

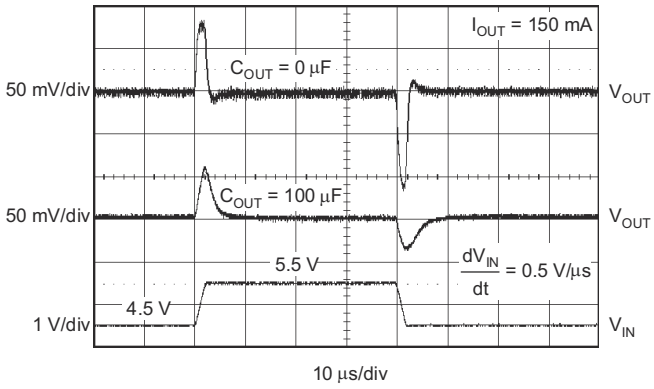


New silicon

Figure 5-36. TPS73133 Load Transient Response

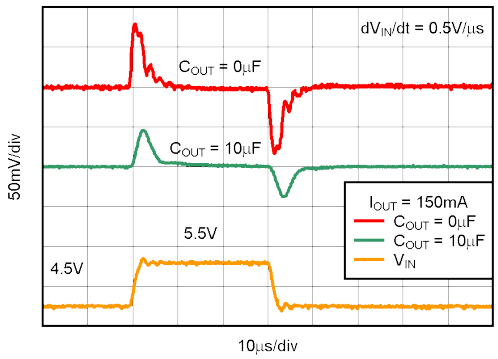
5.6 Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



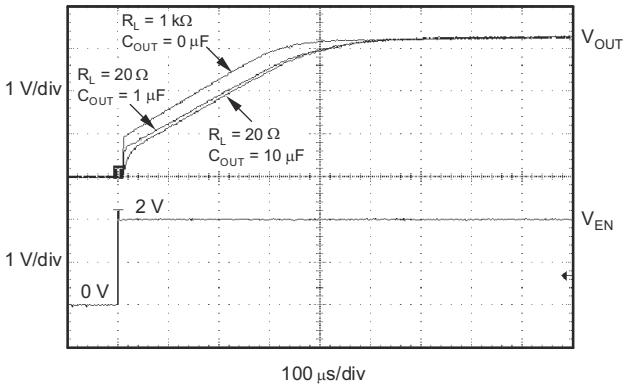
Legacy silicon

Figure 5-37. TPS73133 Line Transient Response



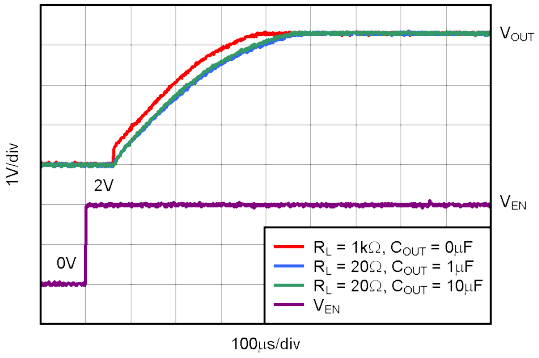
New silicon

Figure 5-38. TPS73133 Line Transient Response



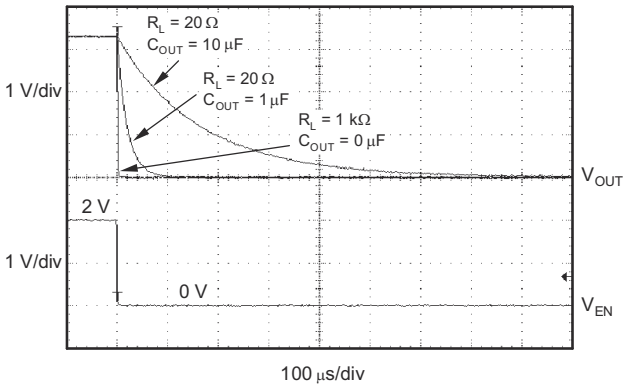
Legacy silicon

Figure 5-39. TPS73133 Turn-On Response



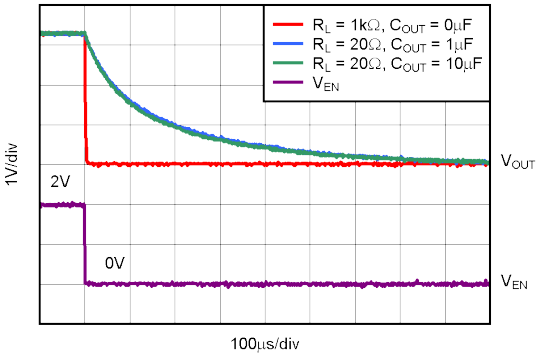
New silicon

Figure 5-40. TPS73133 Turn-On Response



Legacy silicon

Figure 5-41. TPS73133 Turn-Off Response

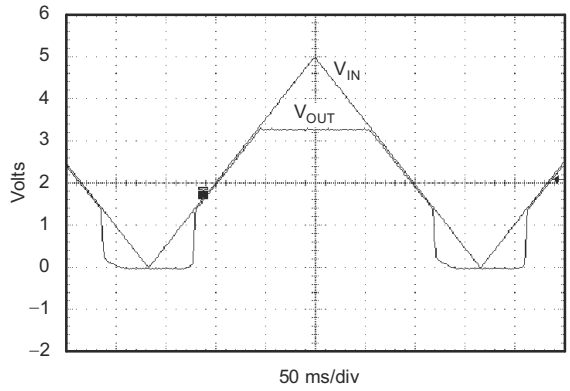


New silicon

Figure 5-42. TPS73133 Turn-Off Response

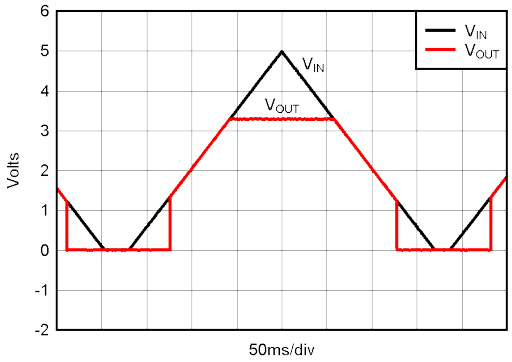
5.6 Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



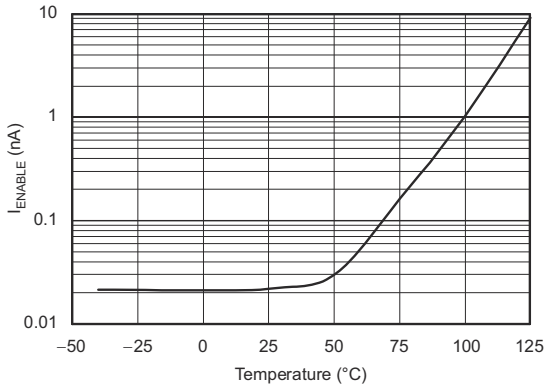
Legacy silicon

Figure 5-43. TPS73133 Power-Up and Power-Down



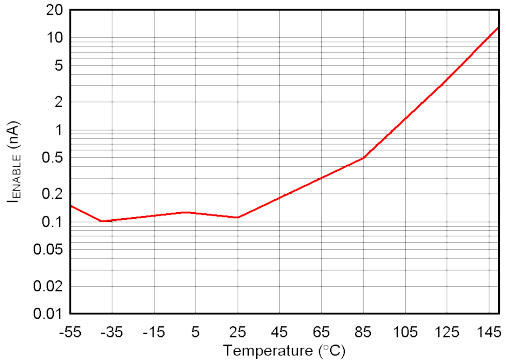
New silicon

Figure 5-44. TPS73133 Power-Up and Power-Down



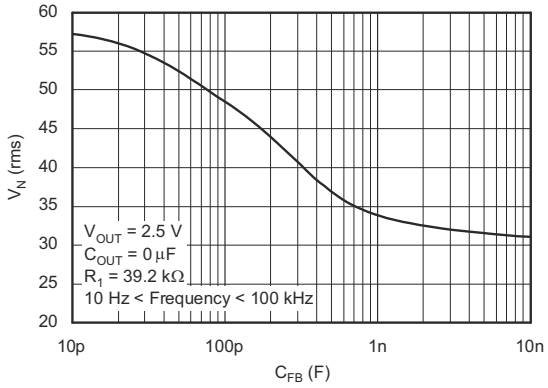
Legacy silicon

Figure 5-45. I_{ENABLE} vs Temperature



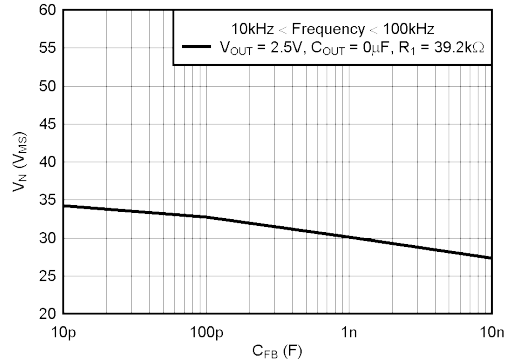
New silicon

Figure 5-46. I_{ENABLE} vs Temperature



Legacy silicon

Figure 5-47. TPS73101 RMS Noise Voltage vs C_{FB}

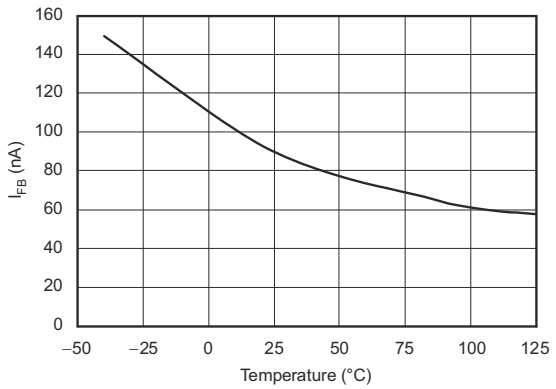


New silicon

Figure 5-48. TPS73101 RMS Noise Voltage vs C_{FB}

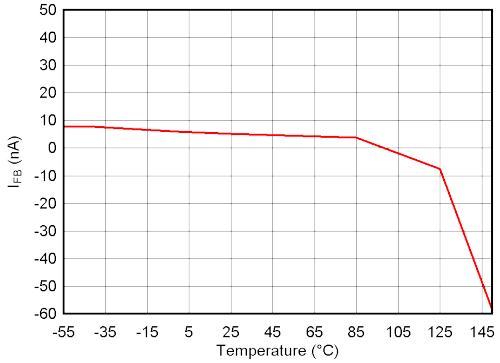
5.6 Typical Characteristics (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



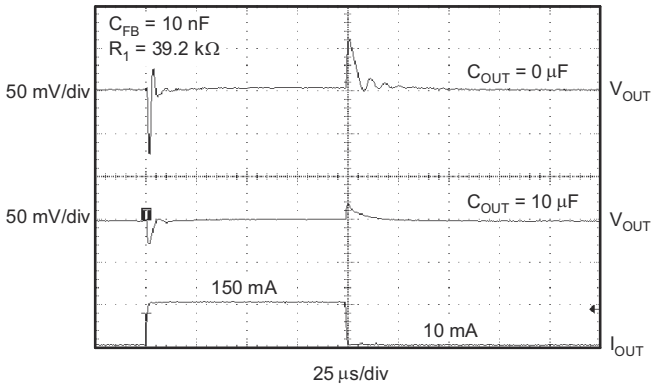
Legacy silicon

Figure 5-49. TPS73101I_{FB} vs Temperature



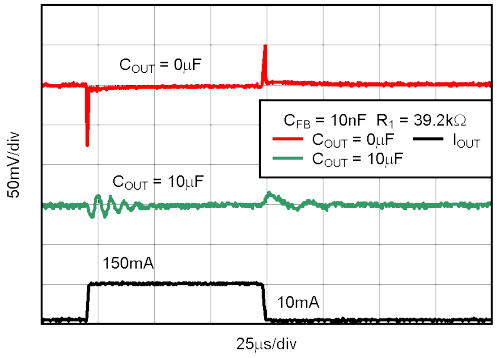
New silicon

Figure 5-50. TPS73101I_{FB} vs Temperature



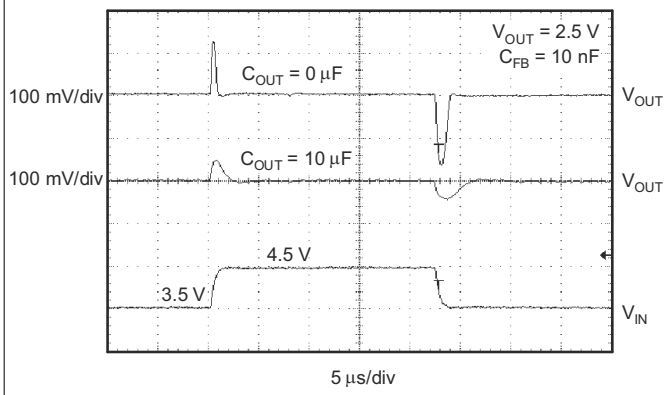
Legacy silicon

Figure 5-51. TPS73101 Load Transient, Adjustable Version



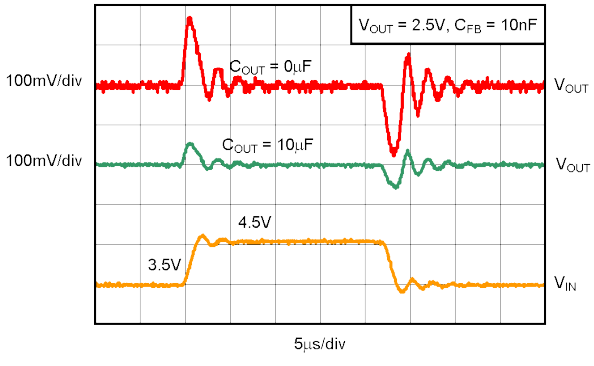
New silicon

Figure 5-52. TPS73101 Load Transient, Adjustable Version



Legacy silicon

Figure 5-53. TPS73101 Line Transient, Adjustable Version



New silicon

Figure 5-54. TPS73101 Line Transient, Adjustable Version

6 Detailed Description

6.1 Overview

The TPS731 low-dropout linear regulator operates down to an input voltage of 1.7V and supports output voltages down to 1.2V while sourcing up to 150mA of load current. This linear regulator uses an NMOS pass transistor with an integrated 4MHz charge pump to provide a dropout voltage of less than 100mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. In fact, the TPS731 does not require an output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this linear regulator an excellent choice when powering a load where the effective capacitance is unknown.

The TPS731 also features a noise-reduction (NR) pin that allows for additional reduction of the output noise. With a noise-reduction capacitor of 0.01µF connected from the NR pin to GND, the TPS73115 output noise ranges as low as 12.75μV_{RMS}. The low noise output featured by the TPS731 makes the device designed for powering VCOs or any other noise-sensitive load.

6.2 Functional Block Diagrams

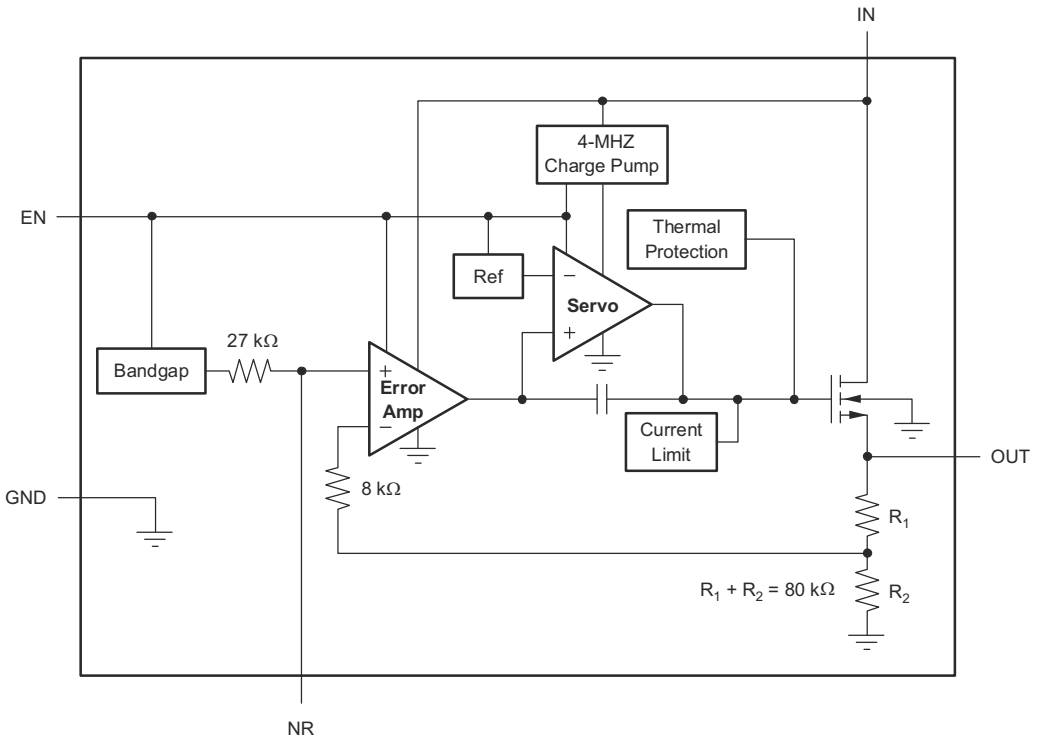
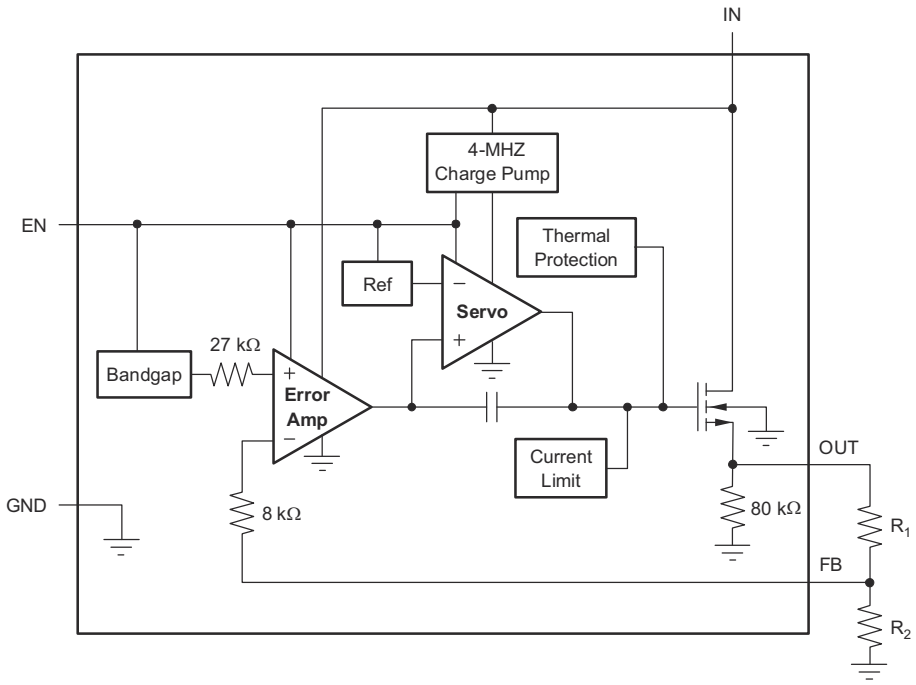


Figure 6-1. Fixed-Voltage Version



Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2 V	Short	Open
1.5 V	23.2 kΩ	95.3kΩ
1.8 V	28.0 kΩ	56.2 kΩ
2.5 V	39.2kΩ	36.5 kΩ
2.8 V	44.2 kΩ	33.2 kΩ
3.0 V	46.4 kΩ	30.9 kΩ
3.3 V	52.3 kΩ	30.1 kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \cdot 1.204$; $R_1 \| R_2 \cong 19\ k\Omega$ for best accuracy.

Figure 6-2. Adjustable-Voltage Version

6.3 Feature Description

6.3.1 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS731xx and it generates approximately $32\mu V_{RMS}$ (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by Equation 1:

$$V_{IN} = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Because the value of V_{REF} is 1.2V, this relationship reduces to Equation 2 for the case of no C_{NR}.

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

An internal 27kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship shown in Equation 3 for C_{NR} = 10nF.

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in the Typical Characteristics section.

The TPS73101 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improves load transient performance.

The TPS731xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250μV of switching noise

at approximately 4MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

6.3.2 Internal Current Limit

The TPS731xx internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See Figure 5-17.

Note from Figure 5-17 that approximately –0.2V of V_{OUT} results in a current limit of 0mA. Therefore, if OUT is forced below –0.2V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS731xx should be enabled first.

6.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5V (maximum) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate. A V_{EN} above 1.7V (minimum) turns the regulator on and the output ramps back up to a regulated V_{OUT} (see Figure 5-39).

When shutdown capability is not required, connect EN to V_{IN}. However, the pass transistor potentially does not discharge using this configuration, thus leaving the pass transistor left on (enhanced) for a significant time after removing V_{IN}. This scenario results in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output potentially overshoots upon power up.

The current limit foldback prevents device start-up under some conditions. See the *Internal Current Limit* section.

6.3.4 Reverse Current

The NMOS pass element of the TPS731xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. The reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There will be additional current flowing into the OUT pin due to the 80kΩ internal resistor divider to ground (see Figure 6-1 and Figure 6-2).

For the TPS73101, reverse current may flow when V_{FB} is more than 1.0V above V_{IN}.

6.4 Device Functional Modes

6.4.1 Normal Operation With $1.7V \le V_{IN} \le 5.5V$ and $V_{EN} \ge 1.7V$

The TPS731xx family requires an input voltage of at least 1.7V to function properly and attempt to maintain regulation.

When operating the device near 5.5V, take care to suppress any transient spikes that may exceed the 6.0V absolute maximum voltage rating. The device should never operate at a DC voltage greater than 5.5V.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The TPS731xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS731xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

7.2 Typical Application

Figure 7-1 shows the basic circuit connections for the fixed-voltage models. Figure 7-2 gives the connections for the adjustable output version (TPS73101).

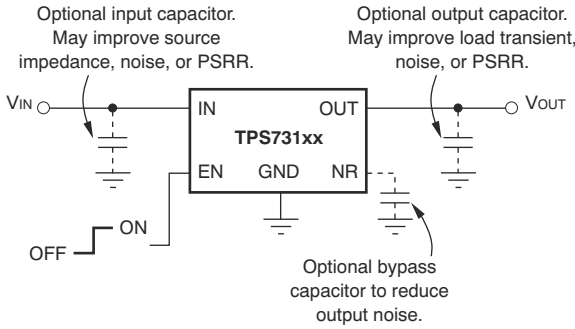


Figure 7-1. Typical Application Circuit for Fixed-Voltage Versions

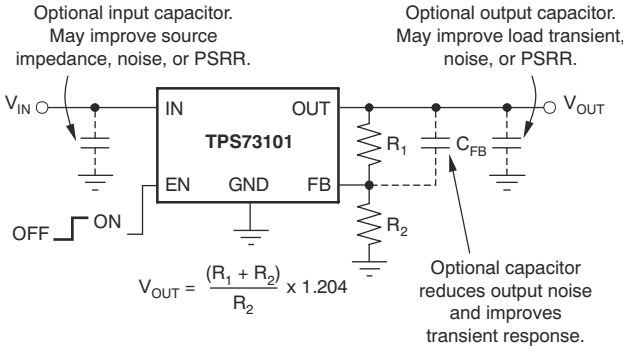


Figure 7-2. Typical Application Circuit for Adjustable-Voltage Version

7.2.1 Design Requirements

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 7-2. Sample resistor values for common output voltages are shown in Figure 6-2.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19kΩ. This 19kΩ, in addition to the internal 8kΩ resistor, presents the same impedance to the error amp as the 27kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1µF, low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

7.2.2.2 Dropout Voltage

The TPS731xx uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the NMOS pass element.

For large step changes in load current, the TPS731xx requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of V_{IN} – V_{OUT} above this line insure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to DC dropout levels], the TPS731xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

7.2.2.3 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1µF) from the output pin (OUT) to ground will reduce undershoot magnitude but increase its duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin will also improve the transient response.

The TPS731xx does not have active pulldown when the output is overvoltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal and external load resistance. The rate of decay is given by Equation 4 and Equation 5:

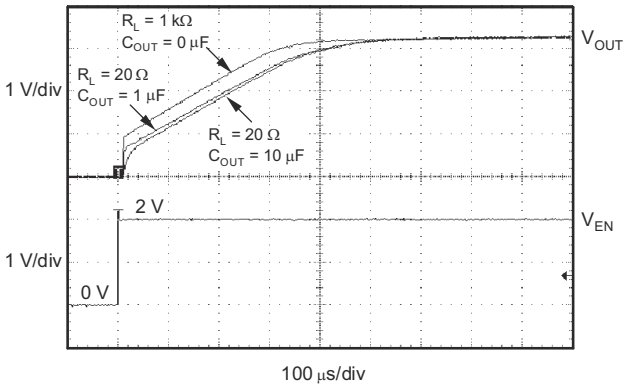
(Fixed-voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable-voltage version)

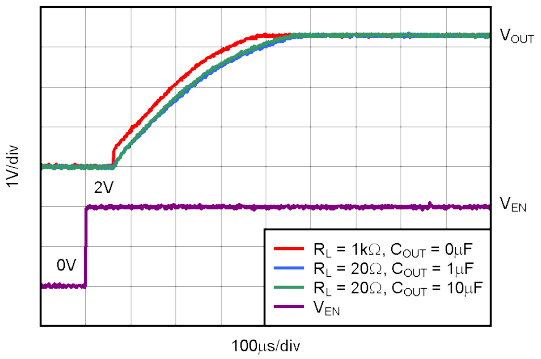
$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

7.2.3 Application Curves



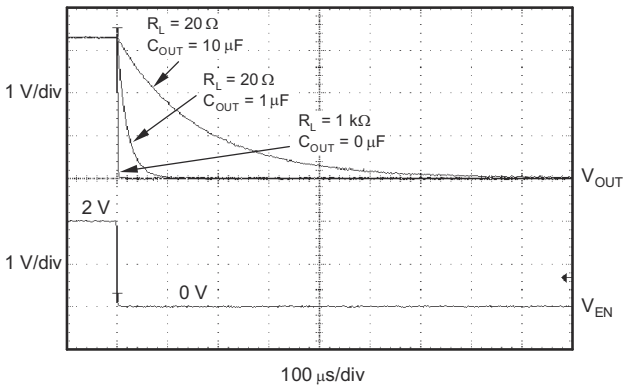
Legacy silicon

Figure 7-3. TPS73133 Turn-On Response



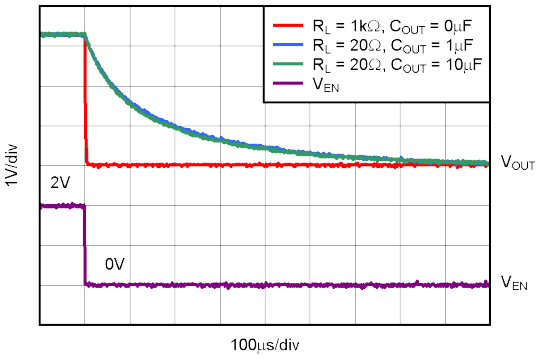
New silicon

Figure 7-4. TPS73133 Turn-On Response



Legacy silicon

Figure 7-5. TPS73133 Turnoff Response



New silicon

Figure 7-6. TPS73133 Turn-Off Response

7.3 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 1.7V and 5.5V. The input voltage range provides adequate headroom for the device to have a regulated output. Verify this input supply must is regulated. If the input supply is noisy, additional input capacitors with low ESR help improve output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

To improve AC performance (such as PSRR, output noise, and transient response), design the PCB with ground plane connections for V_{IN} and V_{OUT} capacitors. Connect the ground plane at the ground pin (GND) of the device. In addition, verify the ground connection for the bypass capacitor connects directly to the GND pin of the device.

7.4.1.1 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS731xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS731xx into thermal shutdown degrades device reliability.

7.4.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC boards are shown in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass transistor (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation is minimized by using the lowest possible input voltage necessary to provide the required output voltage.

7.4.2 Layout Examples

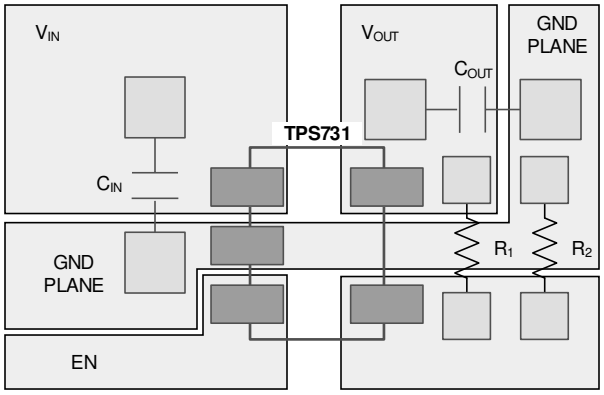


Figure 7-7. Example Layout for the Adjustable-Output Version (DBV Package)

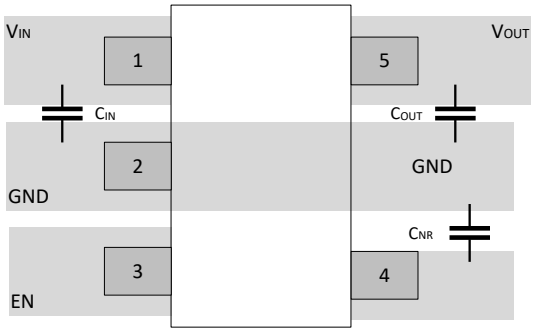


Figure 7-8. Layout Example for the Fixed-Output Version (DBV Package)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS731 is available through the product folders under *Tools & Software*.

8.1.2 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
TPS731**xx yyy z (M3)**	**xx** is the nominal output voltage (for example, 25 = 2.5V; 01 = Adjustable). **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the *legacy silicon* (CSO: DLN) or the *new silicon* (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is used. Device performance for new and legacy silicon is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Solder Pad Recommendations for Surface-Mount Devices* application note.

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (August 2025) to Revision P (April 2026)	Page
• Added silicon 5V output ground current specification	5
• Added silicon 5V output ground pin current at maximum load specification	5

Changes from Revision N (December 2015) to Revision O (August 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed entire document to align with current family format	1
• Added new silicon (M3) devices to document	1
• Added nomenclature distinguishing between new silicon and legacy silicon information throughout document	1
• Changed *Applications*	1
• Added new silicon DBV thermals	4
• Changed VFB typical value	5
• Added new silicon ground pin current spec	5
• Added new silicon shutdown current spec	5
• Added new silicon curves to *Typical Characteristics* section	6
• Added V_{EN} above 1.7V discussion to *Enable Pin and Shutdown* section	17
• Added new silicon curves to *Application Curves* section	20
• Changed *Layout Guidelines* section	20
• Changed *JEDEC low- and high-K boards* to *JEDEC boards* in *Power Dissipation* section	21
• Added *Layout Example for the Fixed-Output Version (DBV Package)* figure to *Layout Examples*	21
• Changed *Device Nomenclature*	22

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73101DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PWYQ
TPS73101DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PWYQ
TPS73101DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PWYQ
TPS73101DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PWYQ
TPS73101DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PWYQ
TPS73101DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PWYQ
TPS73101DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PWYQ
TPS73101DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PWYQ
TPS73101DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PWYQ
TPS731125DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BYX
TPS731125DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BYX
TPS731125DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	BYX
TPS73115DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T31
TPS73115DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T31
TPS73115DBVRG4	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T31
TPS73115DBVRG4.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T31
TPS73115DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T31
TPS73118DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32
TPS73118DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32
TPS73118DBVR1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32
TPS73118DBVR1G4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32
TPS73118DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T32
TPS73118DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32
TPS73118DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32
TPS73118DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32
TPS73118DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T32
TPS73125DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI
TPS73125DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI
TPS73125DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PHWI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73125DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI
TPS73125DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI
TPS73125DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI
TPS73125DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHWI
TPS73130DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T33
TPS73130DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T33
TPS73130DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T33
TPS73130DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T33
TPS73130DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T33
TPS73131DBVR	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BYS
TPS73131DBVR.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BYS
TPS73131DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	BYS
TPS73132DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T52
TPS73132DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T52
TPS73132DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	T52
TPS73133DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34
TPS73133DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34
TPS73133DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34
TPS73133DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34
TPS73133DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T34
TPS73133DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34
TPS73133DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34
TPS73133DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34
TPS73133DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T34
TPS73150DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T35
TPS73150DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T35
TPS73150DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T35
TPS73150DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T35
TPS73150DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T35
TPS73150DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T35
TPS73150DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T35

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

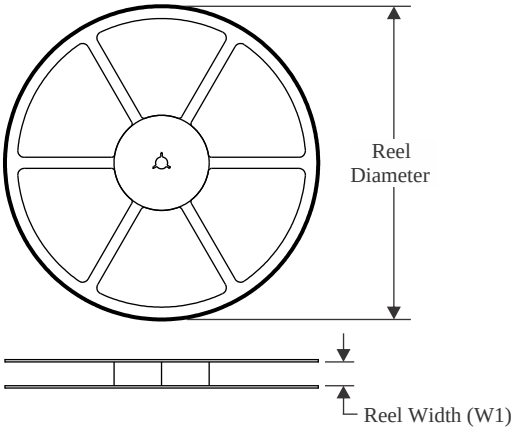
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

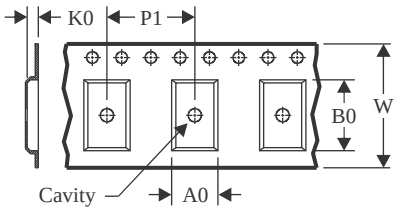
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

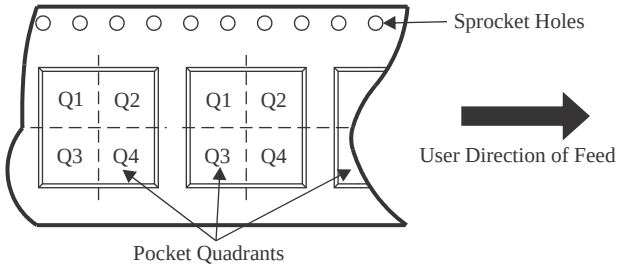


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

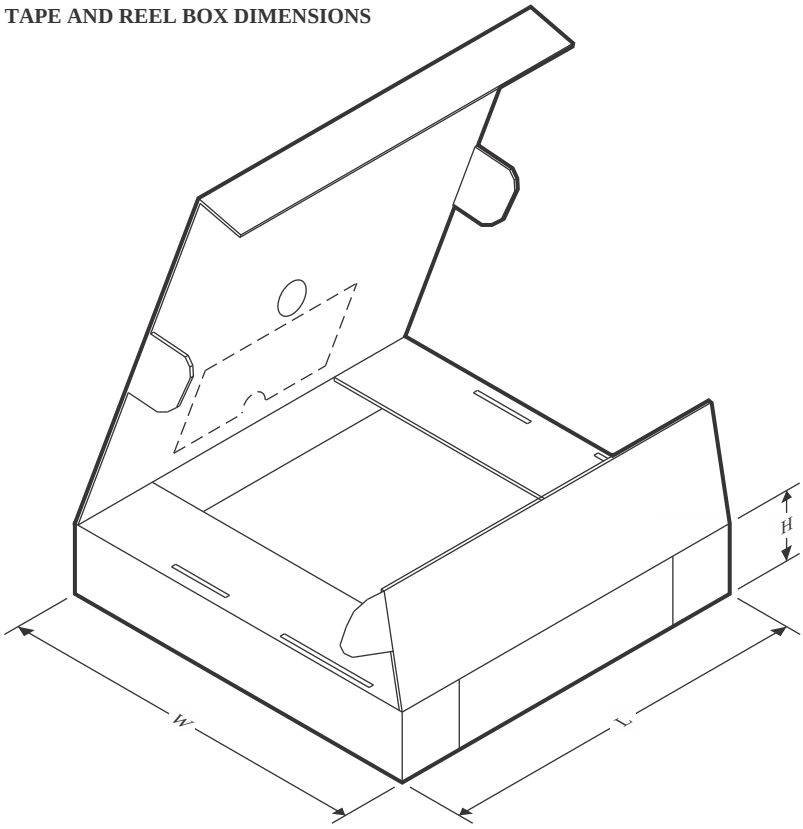


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73101DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73101DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73101DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73101DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73101DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS731125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73115DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73115DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73115DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73118DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73118DBVR1G4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73118DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73118DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73118DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73125DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73125DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73125DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73130DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73130DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73130DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73131DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73132DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73133DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73133DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73133DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73133DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73133DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73150DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73150DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73150DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73150DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73101DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73101DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73101DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73101DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS73101DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS731125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73115DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73115DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73115DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73118DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73118DBVR1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73118DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73118DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73118DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73125DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73125DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0

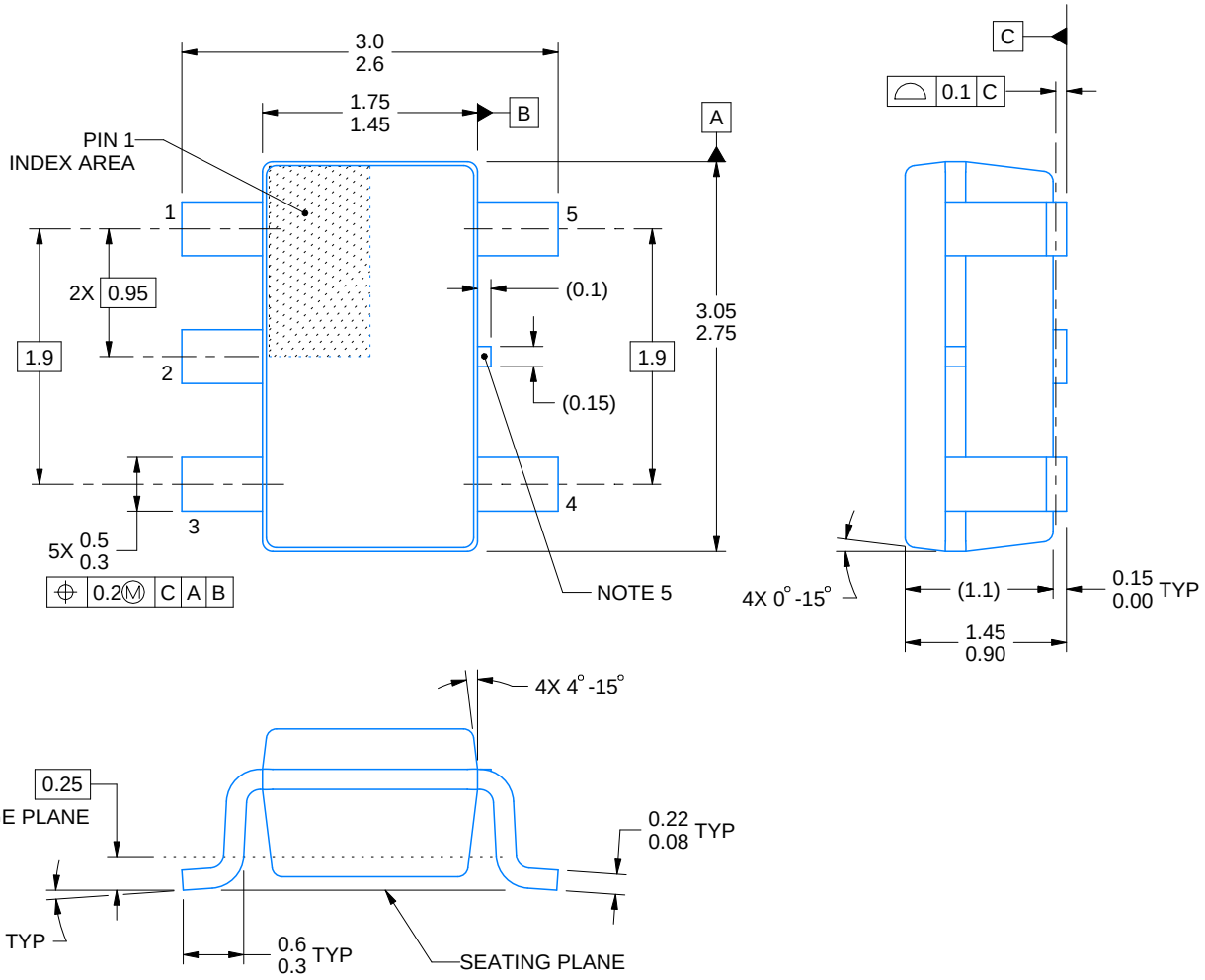
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73130DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73130DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73130DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73131DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73132DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73133DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73133DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73133DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73133DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73133DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73150DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73150DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73150DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73150DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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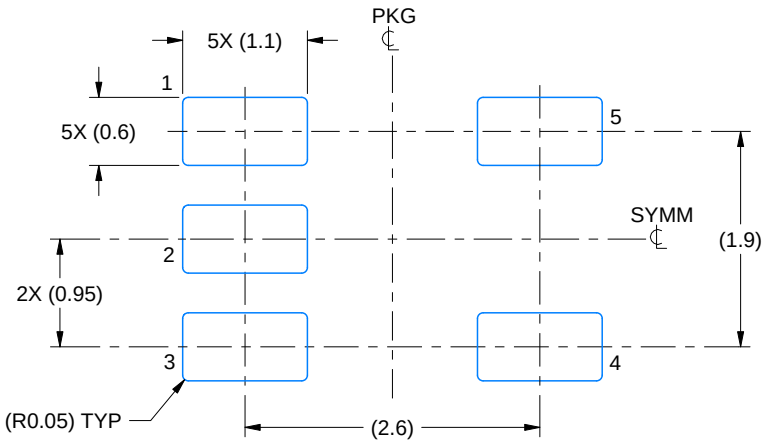
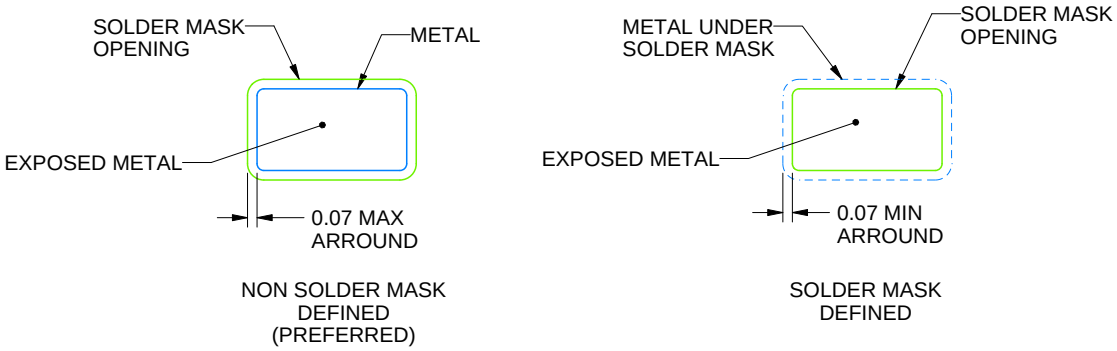
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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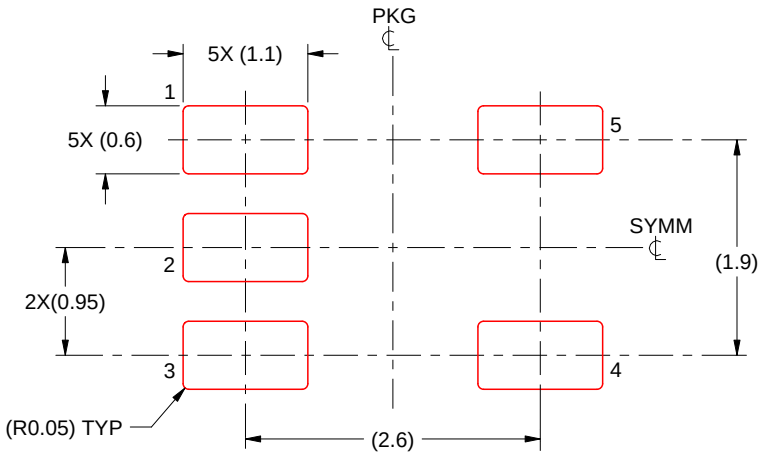
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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