TPS65251-x 4.5-V to 18-V Input, High Current, Synchronous Step Down Three Buck Switchers With Integrated FET

1 Features

- Wide input supply voltage range (4.5 to 18 V)
- Output range: 0.8 V to V_{IN} – 1 V
- Continuous loading: 3 A (buck 1), 2 A (buck 2 and 3)
- Maximum current: 3.5 A (buck 1), 2.5 A (buck 2 and 3)
- Adjustable switching frequency 300 kHz to 2.2 MHz set by external resistor
- Dedicated enable for each buck
- External synchronization pin for oscillator
- Adjustable current limit set by external resistor
- Soft-start pins
- Current-mode control with simple compensation circuit
- Power good
- Automatic PFM/PWM operation
- VQFN package, 40-pin 6-mm × 6-mm RHA

2 Applications

- Set top boxes
- Blu-ray™ DVD
- DVR
- DTV
- Car audio/video
- Security camera

3 Description

The TPS65251-x features three synchronous wide-input range, high-efficiency buck converters. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5-, 9-, 12- or 15-V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8 V and close to the input supply. Each converter features an enable pin that allows a delayed start-up for sequencing purposes, soft-start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIMx) pin that enables the designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. The current mode control allows a simple RC compensation.

The switching frequency of the converters can either be set with an external resistor connected to ROSC pin or can be synchronized to an external clock connected to the SYNC pin if needed. The switching regulators are designed to operate from 300 kHz to 2.2 MHz. 180° out-of-phase operation between Buck 1 and Buck 2, 3 (Buck 2 and 3 run in phase) minimizes the input filter requirements.

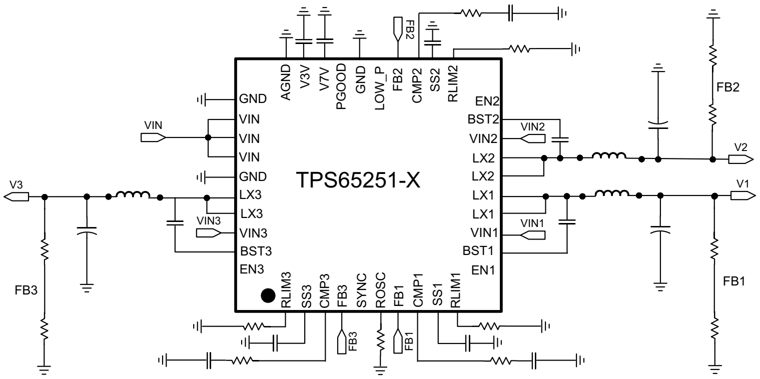
TPS65251-x features a supervisor circuit that monitors each converter output. The PGOOD pin is asserted when sequencing is done, all PG signals are reported and a selectable end of reset time lapses. The polarity of the PGOOD signal is active high.

All converters feature an automatic low-power pulse PFM skipping mode, which improves efficiency during light loads and standby operation, while ensuring a very-low output ripple, allowing for a value of less than 2% at low output voltages.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
TPS65251-1	VQFN (40)	6.00 mm × 6.00 mm
TPS65251-2		
TPS65251-3		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

Changes from Revision A (January 2015) to Revision B (January 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	1
• Change VIN1, VIN2, VIN3, LX1, LX2, and LX3 maximum rating voltage from 18 V to 20 V	5
• Change LX1, LX2, and LX3 minimum rating voltage from –1 V to –3 V	5

Changes from Revision * (January 2015) to Revision A (January 2015)	Page
• Updated device status to production data	1

5 Pin Configuration and Functions

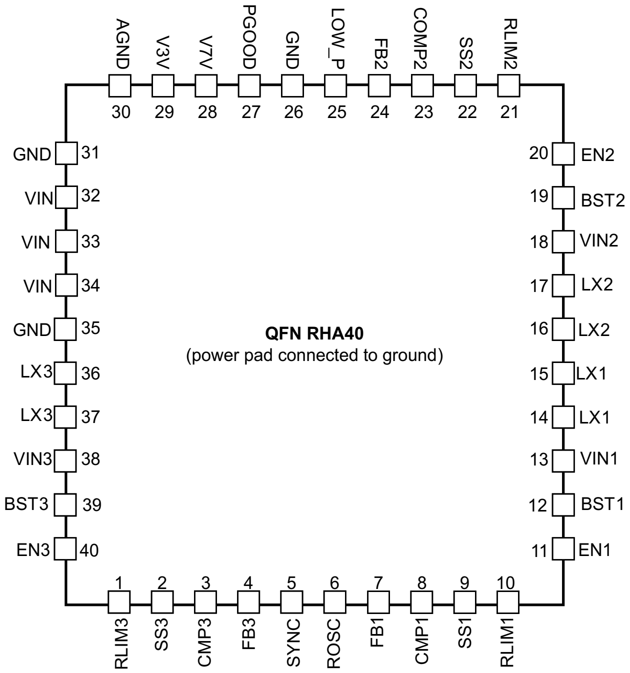


Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
RLIM3	1	I	Current limit setting for Buck 3. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS3	2	I	Soft-start pin for Buck 3. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
COMP3	3	O	Compensation for Buck 3. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB3	4	I	Feedback input for Buck 3. Connect a divider set to 0.8 V from the output of the converter to ground.
SYNC	5	I	Synchronous clock input. If there is a sync clock in the system, connect to the pin. When not used, connect to GND.
ROSC	6	I	Oscillator set. This resistor sets the frequency of the internal autonomous clock. If external synchronization is used, the resistor should be fitted and set to about 70% of external clock frequency.
FB1	7	I	Feedback pin for Buck 1. Connect a divider set to 0.8 V from the output of the converter to ground.
COMP1	8	O	Compensation pin for Buck 1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	9	I	Soft-start pin for Buck 1. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
RLIM1	10	I	Current limit setting pin for Buck 1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	11	I	Enable pin for Buck 1. A low-level signal on this pin disables it. If pin is left open, a weak internal pull-up to V3V allows for automatic enable. For a delayed start-up, add a small ceramic capacitor from this pin to ground.
BST1	12	I	Bootstrap capacitor for Buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	13	I	Input supply for Buck 1. Fit a 10-µF ceramic capacitor close to this pin.
LX1	14	O	Switching node for Buck 1
	15		
LX2	16	O	Switching node for Buck 2
	17		
VIN2	18	I	Input supply for Buck 2. Fit a 10-µF ceramic capacitor close to this pin.
BST2	19	I	Bootstrap capacitor for Buck 2. Fit a 47-nF ceramic capacitor from this pin to the switching node.

Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
EN2	20	I	Enable pin for Buck 2. A low-level signal on this pin disables it. If pin is left open, a weak internal pull-up to V3V allows for automatic enable. For a delayed start-up, add a small ceramic capacitor from this pin to ground.
RLIM2	21	I	Current limit setting for Buck 2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	22	I	Soft-start pin for Buck 2. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
COMP2	23	O	Compensation pin for Buck 2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter
FB2	24	I	Feedback input for Buck 2. Connect a divider set to 0.8 V from the output of the converter to ground.
LOW_P	25	I	Low-power operation mode (active-high) input for TPS65251
GND	26		Ground pin
PGOOD	27	O	Power good. Open-drain output asserted after all converters are sequenced and within regulation. Polarity is factory selectable (active-high default).
V7V	28	O	Internal supply. Connect a 10-µF ceramic capacitor from this pin to ground.
V3V	29	O	Internal supply. Connect a 3.3- to 10-µF ceramic capacitor from this pin to ground.
AGND	30		Analog ground. Connect all GND pins and the power pad together.
GND	31		Ground pin
VIN	32	I	Input supply
	33		
	34		
GND	35		Ground pin
LX3	36	O	Switching node for Buck 3
	37		
VIN3	38		Input supply for Buck 3. Fit a 10-µF ceramic capacitor close to this pin.
BST3	39	I	Bootstrap capacitor for Buck 3. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN3	40	I	Enable pin for Buck 3. A low-level signal on this pin disables it. If pin is left open, a weak internal pull-up to V3V allows for automatic enable. For a delayed start-up, add a small ceramic capacitor from this pin to ground.
PAD	—	—	Power pad. Connect to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VIN1,VIN2, VIN3, LX1, LX2, LX3	–0.3	20	V
	LX1, LX2, LX3 (maximum withstand voltage transient <10 ns)	–3	23	V
	BST1, BST2, BST3, referenced to Lx pin	–0.3	7	V
	V7V	–0.3	7	V
	V3V, RLIM1, RLIM2, RLIM3, EN1, EN2, EN3, SS1, SS2,SS3, FB1, FB2, FB3, PGOOD, SYNC, ROSC, RST_IN, LOW_P, COMP1, COMP2, COMP3	–0.3	3.6	V
	AGND, GND	–0.3	0.3	V
T_J	Operating virtual junction temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input operating voltage	4.5		18	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS65251-x	UNIT
		RHA	
		40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.3	
Ψ_{JT}	Junction-to-top characterization parameter	0.2	
Ψ_{JB}	Junction-to-board characterization parameter	N/A	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 Hz (unless otherwise noted)

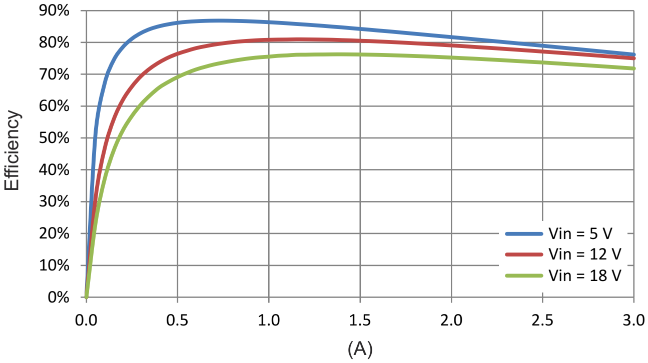
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4.5		18	V
IDD_{SDN}	Shutdown	EN pin = Low for all converters		175		µA
IDD_{Q}	Quiescent, low power disabled (Lo)	Converters enabled, no load Buck 1 = 3.3 V, Buck 2 = 2.5 V, Buck 3 = 7.5 V, L = 4.7 µH , f_{SW} = 800 kHz		20		mA
$IDD_{Q\_LOW\_P}$	Quiescent, low power enabled (Hi)	Converters enabled, no load Buck 1 = 3.3 V, Buck 2 = 2.5 V, Buck 3 = 7.5 V, L = 4.7 µH , f_{SW} = 800 kHz		1		mA
$UVLO_{VIN}$	V_{IN} undervoltage lockout	Rising V_{IN}		4.22		V
		Falling V_{IN}		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		µs
V_{3p3}	Internal biasing supply			3.3		V
V_{7V}	Internal biasing supply			6.25		V
$V7V_{UVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V7V_{UVLO\_DEGLITCH}$		Falling edge		110		µs
BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT START, SWITCHING FREQUENCY AND SYNC CIRCUIT, LOW POWER MODE)						
V_{IH}	Enable threshold high	External GPIO mode, V3p3 = 3.2 to 3.4 V	0.66 x V_{3p3}			V
	Enable high level	V3p3 = 3.2 to 3.4 V, V_{ENX} rising	1.55	1.67	1.82	
V_{IL}	Enable threshold low	External GPIO mode, V3p3 = 3.2 to 3.4 V			0.33 x V_{3p3}	V
	Enable low level	V3p3 = 3.2 to 3.4 V, V_{ENX} falling	0.98	1.10	1.24	
R_{EN_DIS}	Enable discharge resistor		–25%	2.1	25%	kΩ
ICH_{EN}	Pullup current enable pin			1.1		µA
t_{D}	Discharge time enable pins	Power-up		10		ms
I_{SS}	Soft-start pin current source			5		µA
F_{SW_BK}	Converter switching frequency range	Set externally with resistor	0.3		2.2	MHz
R_{FSW}	Frequency setting resistor	Depending on set frequency	50		600	kΩ
f_{SW_TOL}	Internal oscillator accuracy	f_{SW} = 800 kHz	–10%		10%	
V_{SYNCH}	External clock threshold high	V3p3 = 3.3 V			1.24	V
V_{SYNCL}	External clock threshold low	V3p3 = 3.3 V	1.55			V
$SYNC_{RANGE}$	Synchronization range		0.2		2.2	MHz
$SYNC_{CLK\_MIN}$	Sync signal minimum duty cycle		40%			
$SYNC_{CLK\_MAX}$	Sync signal maximum duty cycle				60%	
VIH_{LOW_P}	Low power mode threshold high	V3p3 = 3.3 V, V_{ENX} rising	1.55			V
VIL_{LOW_P}	Low power mode threshold Low	V3p3 = 3.3 V, V_{ENX} falling			1.24	V

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 Hz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FEEDBACK, REGULATION, OUTPUT STAGE						
V_{FB}	Feedback voltage	V_{IN} = 12 V, T_J = 25°C	–1%	0.8	1%	V
		V_{IN} = 4.5 to 18 V	–2%	0.8	2%	
I_{FB}	Feedback leakage current				50	nA
t_{ON_MIN}	Minimum on-time (current sense blanking) to specify output regulation			70	100	ns
$RLIM_1$	Limit resistance range	V_{IN} = 12 V, f_{SW} = 500 kHz	75		300	kΩ
$RLIM_{2,3}$	Limit resistance range	V_{IN} = 12 V, f_{SW} = 500 kHz	1.1		5.1	A
$ILIM_1$	Buck1 current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz	100		300	kΩ
$ILIM_2$	Buck2 current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz	1.2		4.1	A
$ILIM_3$	Buck3 current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz	1.2		4.1	A
MOSFET (BUCK 1)						
H.S. Switch	Turn-on resistance high-side FET on CH1	BOOT = 6.5 V, T_J = 25°C		95		mΩ
L.S. Switch	Turn-on resistance low-side FET on CH1	V_{IN} = 12 V, T_J = 25°C		50		mΩ
MOSFET (BUCK 2)						
H.S. Switch	Turn-on resistance high-side FET on CH2	BOOT = 6.5 V, T_J = 25°C		120		mΩ
L.S. Switch	Turn-on resistance low-side FET on CH2	V_{IN} = 12 V, T_J = 25°C		80		mΩ
MOSFET (BUCK 3)						
H.S. Switch	Turn-on resistance high-side FET on CH3	BOOT = 6.5 V, T_J = 25°C		120		mΩ
L.S. Switch	Turn-on resistance low-side FET on CH3	V_{IN} = 12 V, T_J = 25°C		80		mΩ
ERROR AMPLIFIER						
g_M	Error amplifier transconductance	–2 μA < I_{COMP} < 2 μA		130		μmhos
gm_{PS}	COMP to ILX g_M	ILX = 0.5 A		10		A/V
POWER GOOD RESET GENERATOR						
VUV_{BUCKX}	Threshold voltage for buck under voltage	Output falling		85%		
		Output rising (PG is asserted)		90%		
$t_{UV\_deglitch}$	Deglitch time (both edges)	Each buck		11		ms
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		13		ms
t_{OFF_HICCUP}	Hiccup mode OFF time	All converters disabled. After t_{OFF_HICCUP} elapses, all converters go through sequencing again.		11		ms
VOV_{BUCKX}	Threshold voltage for buck over voltage	Output rising (high-side FET is forced off)		106%		
		Output falling (high-side FET is allowed to switch)		104%		
t_{RP}	Minimum reset period	TPS65251-1		1000		ms
		TPS65251-2		32		
		TPS65251-3		256		
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shutdown trip point	Rising temperature		160		°C
T_{HYST}	Thermal shutdown hysteresis	Device restarts		20		°C
$t_{TRIP\_DEGLITCH}$	Thermal shutdown deglitch		100		120	μs

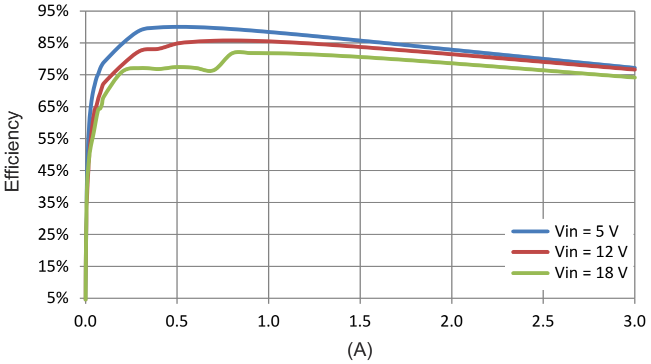
6.6 Typical Characteristics for Buck 1

T_A = 25°C, V_{IN} = 12 V, V_O = 1.2 V, L = 4.7 µH, C_O = 68 µF, f_{SW} = 500 Hz (unless otherwise noted)



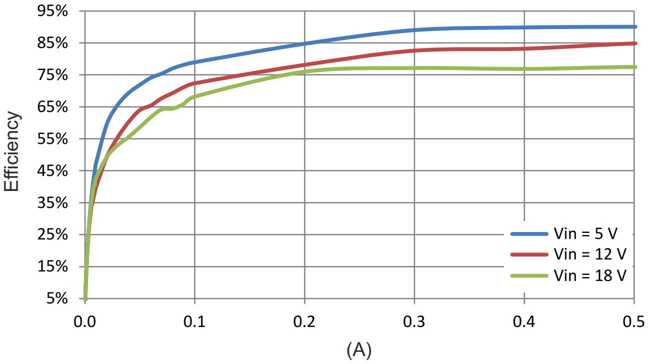
L = 4.7 µH, 20 mΩ

Figure 6-1. Efficiency, Forced PWM



L = 4.7 µH, 20 mΩ

Figure 6-2. Efficiency, LOW_P Mode



L = 4.7 µH, 20 mΩ

Figure 6-3. Efficiency, LOW_P Mode, 0 to 500 mA

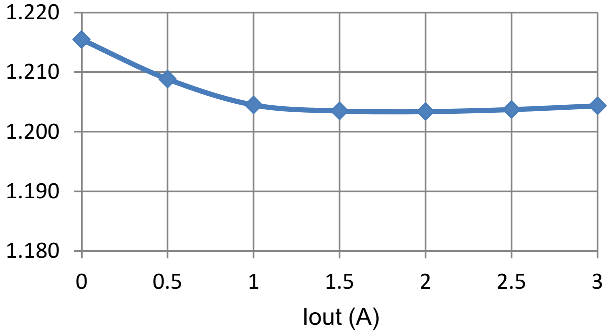


Figure 6-4. Load Regulation, 25°C, 1% 100-PPM Resistor

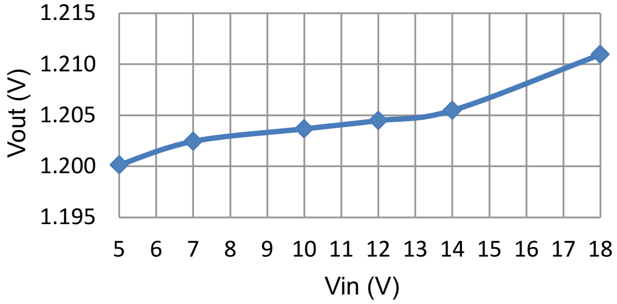


Figure 6-5. Line Regulation, Load = 1 A

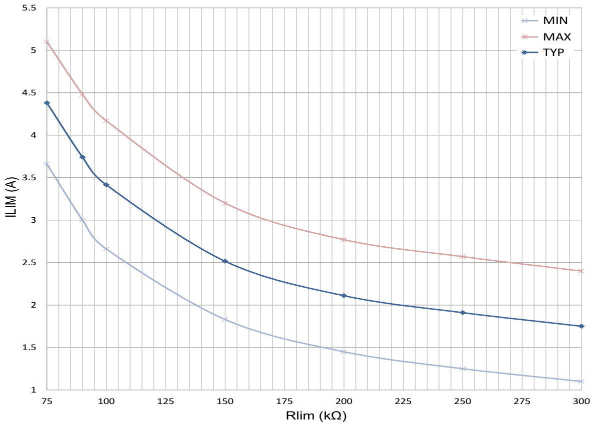
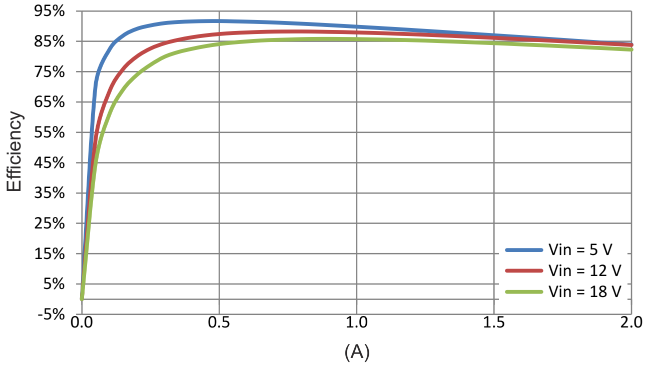


Figure 6-6. Current Limit V_{IN} = 12 V, f_{SW} = 500 KHz

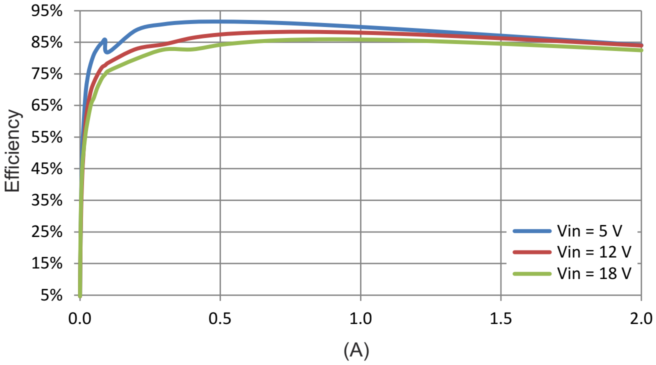
6.7 Typical Characteristics for Buck 2

T_A = 25°C, V_{IN} = 12 V, V_O = 1.8 V, L = 4.7 µH, C_O = 68 µF, f_{SW} = 500 Hz (unless otherwise noted)



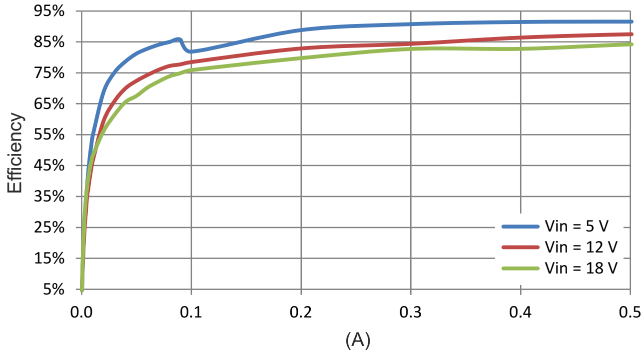
L = 4.7 µH, 27 mΩ

Figure 6-7. Efficiency, Forced PWM



L = 4.7 µH, 27 mΩ

Figure 6-8. Efficiency, LOW_P Mode



L = 4.7 µH, 27 mΩ

Figure 6-9. Efficiency, LOW_P Mode, 0 to 500 mA

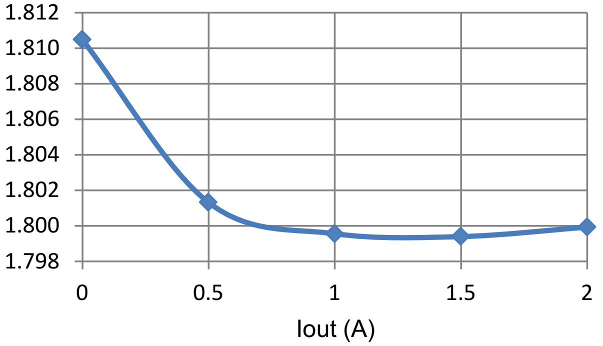


Figure 6-10. Load Regulation, 25°C, 1% 100-PPM Resistor

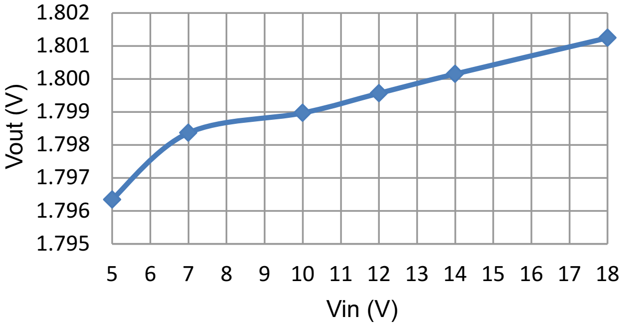


Figure 6-11. Line Regulation, Load = 1 A

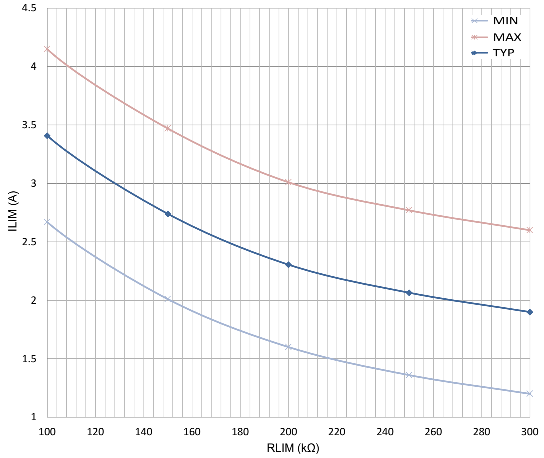
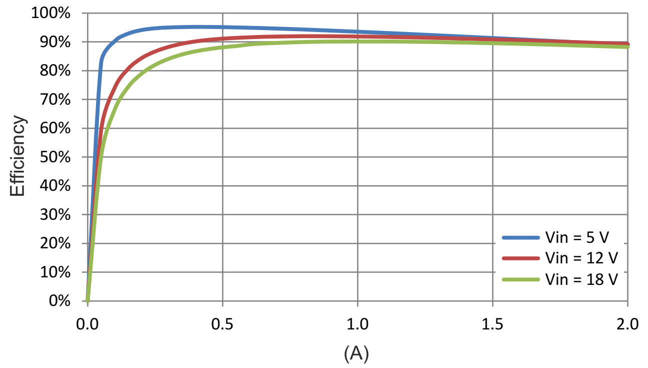


Figure 6-12. Current Limit V_{IN} = 12 V, f_{SW} = 500 kHz

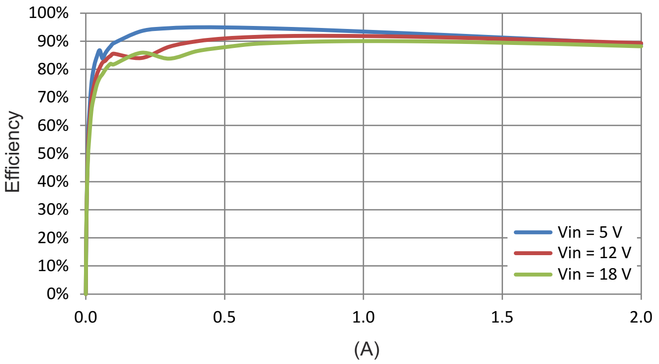
6.8 Typical Characteristics for Buck 3

T_A = 25°C, V_{IN} = 12 V, V_O = 3.3 V, L = 4.7 µH, C_O = 68 µF, f_{SW} = 500 Hz (unless otherwise noted)



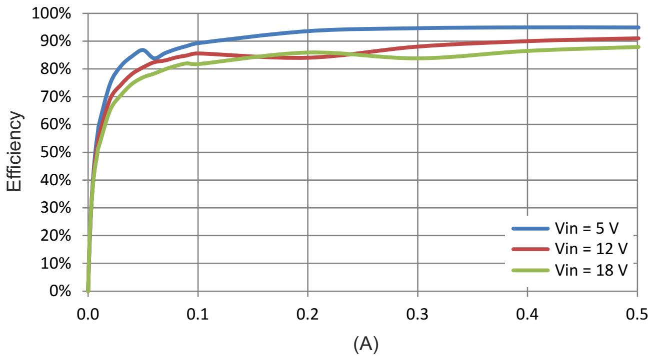
L = 4.7 µH, 27 mΩ

Figure 6-13. Efficiency, Forced PWM



L = 4.7 µH, 27 mΩ

Figure 6-14. Efficiency, LOW_P Mode



L = 4.7 µH, 27 mΩ

Figure 6-15. Efficiency, LOW_P Mode, 0 to 500 mA

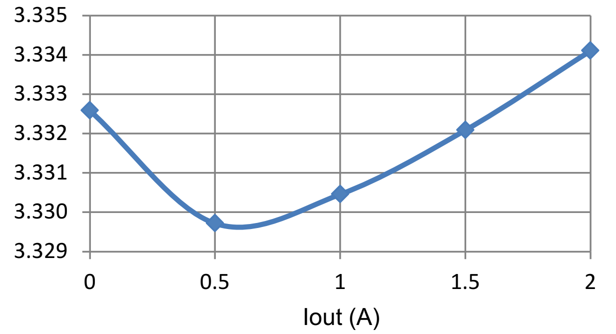


Figure 6-16. Load Regulation, 25°C, 1% 100-PPM Resistor

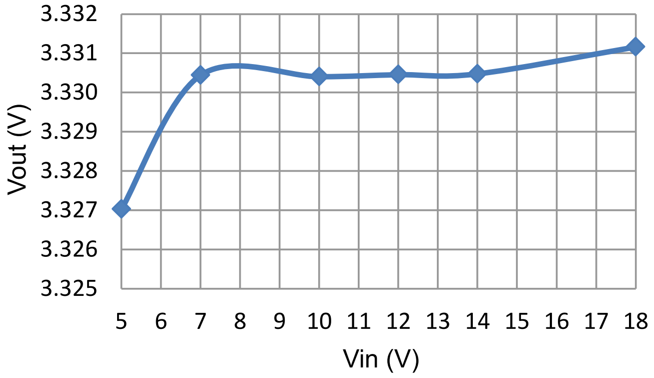


Figure 6-17. Line Regulation, Load = 1 A

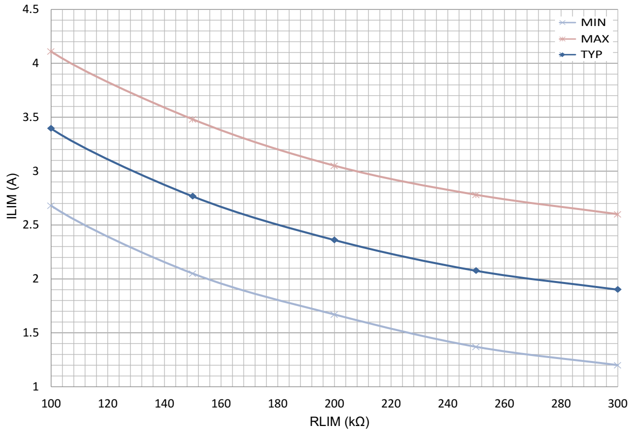


Figure 6-18. Current Limit V_{IN} = 12 V, f_{SW} = 500 KHz

7 Detailed Description

7.1 Overview

TPS65251-x is a power management IC with three step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. TPS65251-x can support 4.5- to 18-V input supply, high load current, 300-kHz to 2.2-MHz clocking. The buck converters have an optional PSM mode, which can improve power dissipation during light loads. Alternatively, the device implements a constant frequency mode by connecting the LOW_P pin to ground. The wide switching frequency of 300 kHz to 2.2 MHz allows for efficiency and size optimization. The switching frequency is adjustable by selecting a resistor to ground on the ROSC pin. The SYNC pin also provides a means to synchronize the power converter to an external signal. Input ripple is reduced by 180° out-of-phase operation between Buck 1 and Buck 2. Buck 3 operates in phase with Buck 2.

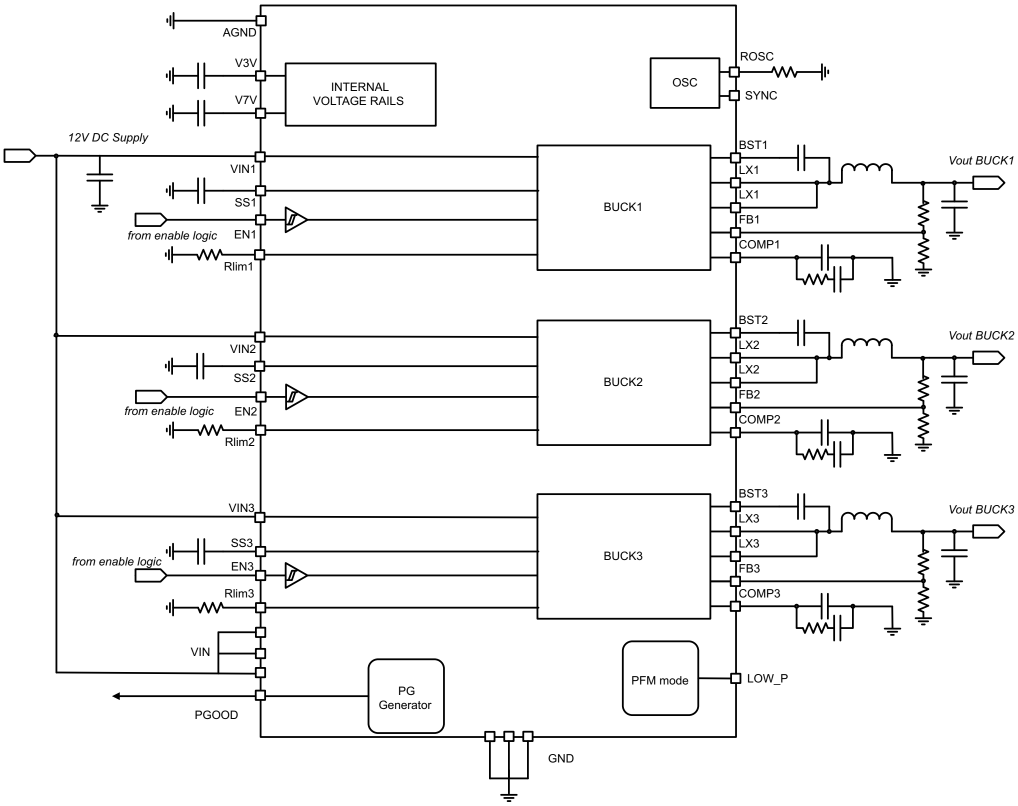
All three buck converters have peak current mode control which simplifies external frequency compensation. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz.

Each buck converter has an individual current limit, which can be set up by a resistor to ground from the RLIM pin. The adjustable current limiting enables high-efficiency design with smaller and less expensive inductors.

The device has two built-in LDO regulators. During a standby mode, the 3.3-V LDO and the 6.5-V LDO can be used to drive MCU and other active loads. By this, the system is able to turn off the three buck converters and improve the standby efficiency.

The device has a power-good comparator monitoring the output voltage. Each converter has its own soft-start and enable pins, which provide independent control and programmable soft-start.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjustable Switching Frequency

To select the internal switching frequency, connect a resistor from ROSC to ground. Figure 7-1 shows the required resistance for a given switching frequency.

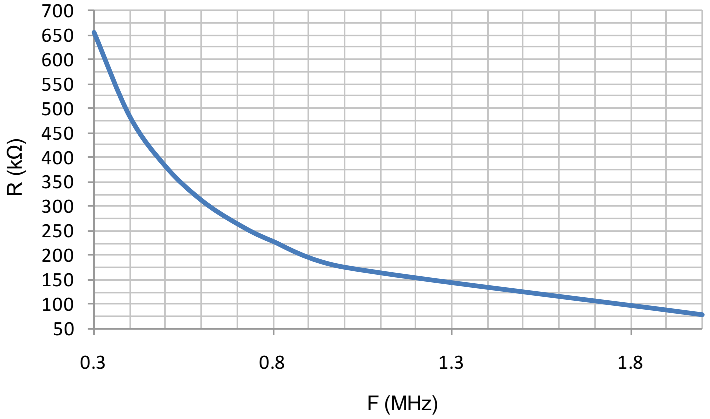


Figure 7-1. ROSC vs Switching Frequency

$$R_{OSC}\,(k\Omega) = 174 \times f\,(\text{MHz})^{-1.122} \quad (1)$$

For operation at 800 kHz, a 230-kΩ resistor is required.

7.3.2 Synchronization

The status of the SYNC pin is ignored during start-up and the TPS65251’s control only synchronizes to an external signal after the PGOOD signal is asserted. The status of the SYNC pin is ignored during start-up and the TPS65251 only synchronizes to an external clock if the PGOOD signal is asserted. When synchronization is applied, the PWM oscillator frequency must be lower than the sync pulse frequency to allow the external signal trumping the oscillator pulse reliably. When synchronization is not applied, the SYNC pin should be connected to ground.

7.3.3 Out-of-Phase Operation

Buck 1 has a low conduction resistance compared to Buck 2 and 3. Normally Buck 1 is used to drive higher system loads. Buck 2 and 3 are used to drive some peripheral loads like I/O and line drivers. The combination of Buck 2's and Buck 3’s loads may be on par with Buck 1’s load. To reduce input ripple current, Buck 2 operates in phase with Buck 3; Buck 1 and Buck 2 operate 180° out-of-phase. This enables the system, having less input ripple, to lower component cost, save board space, and reduce EMI.

7.3.4 Delayed Start-Up

If a delayed start-up is required on any of the buck converters, fit a ceramic capacitor to the ENx pins. The delay added is approximately 1.67 ms per nF connected to the pin. Note that the EN pins have a weak 1-µA pull-up to the 3V3 rail.

7.3.5 Soft-Start Time

The device has an internal pullup current source of 5 µA that charges an external slow-start capacitor to implement a slow-start time. Equation 2 shows how to select a slow-start capacitor based on an expected slow-start time. The voltage reference (V_{REF}) is 0.8 V and the slow-start charge current (I_{ss}) is 5 µA. The soft-start circuit requires 1 nF per 200 µs to be connected at the SS pin. A 1-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant pins.

$$t_{SS}\ (ms) = V_{REF}\ (V) \times \left(\frac{C_{SS}\ (nF)}{I_{SS}\ (\mu A)}\right) \tag{2}$$

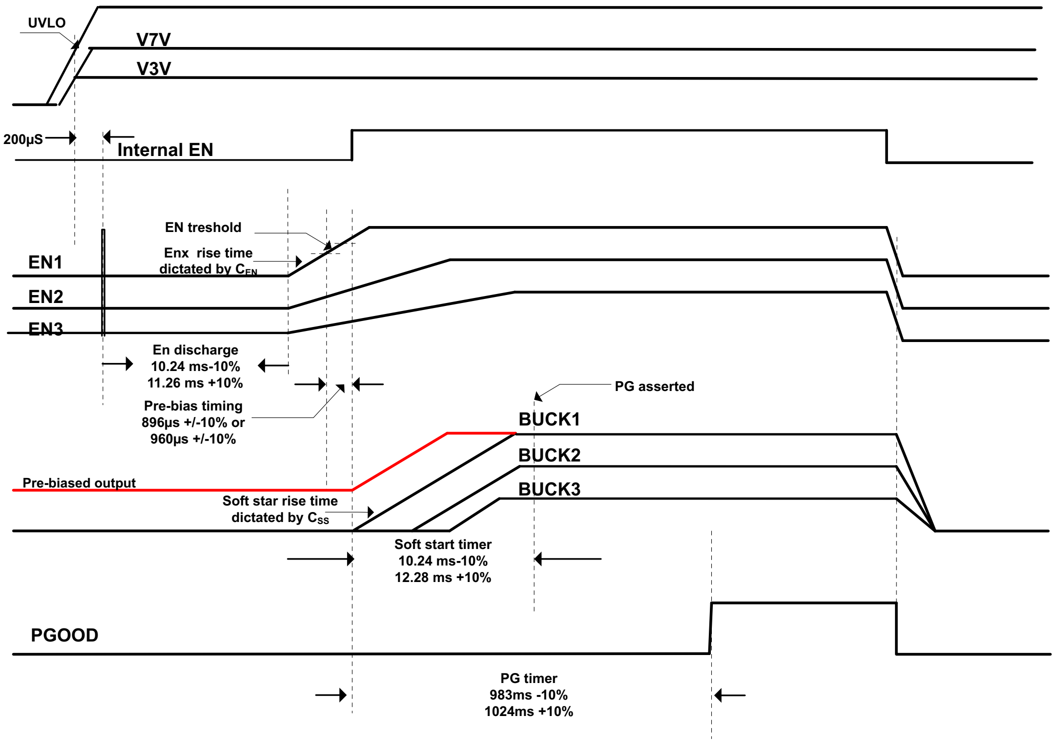


Figure 7-2. TPS65251-x Timing Diagram

7.3.6 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends to use 1% tolerance or better divider resistors. To improve efficiency at light load, start with 40.2 kΩ for the R1 resistor and use Equation 3 to calculate R2.

$$R2 = R1 \times \left(\frac{0.8\ V}{V_O - 0.8\ V}\right) \tag{3}$$

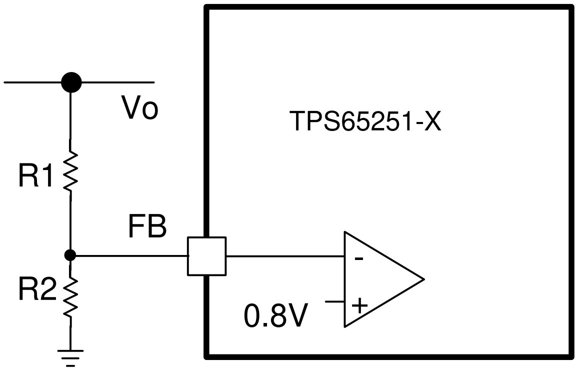


Figure 7-3. Voltage Divider Circuit

7.3.7 Input Capacitor

Use 10-µF X7R/X5R ceramic capacitors at the input of the converter inputs. Connect these capacitors as close as physically possible to the input pins of the converters.

7.3.8 Bootstrap Capacitor

The device has three integrated boot regulators and requires a small ceramic capacitor between the BST and LX pin to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.047 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric because of the stable characteristics over temperature and voltage.

7.3.9 Error Amplifier

The device has a transconductance error amplifier. The frequency compensation network is connected between the COMP pin and ground.

7.3.10 Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent subharmonic oscillations in peak current mode control.

7.3.11 Power Good

The PGOOD pin is an open-drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. TI recommends to use a pullup resistor from the PGOOD to the output of Buck 1. The PGOOD is pulled up when all three buck converters' outputs are more than 90% of its nominal output voltage.

The reset time of the PGOOD pin varies according to the part:

- TPS65251-1 is 1 s.
- TPS65251-2 is 32 ms.
- TPS65251-3 is 256 ms.

The polarity of the PGOOD pin is active high.

7.3.12 3.3-V and 6.5-V LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 10 µF for V7V pin 28
- 3.3 µF for V3V pin 29

7.3.13 Current Limit Protection

All converters operate in hiccup mode: After an overcurrent event lasting more than 10 ms is sensed in any of the converters, all the converters shut down for 10 ms, then the start-up sequencing is retried. If the overload has been removed, the converter ramps up and operates normally. If this is not the case, the converter senses another overcurrent event and shuts down again, repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for <10 ms, only the relevant affected converter goes into and out of under voltage and no global hiccup mode occurs. The converter is protected by the cycle-by-cycle current limit during that time.

7.3.14 Overvoltage Transient Protection (OVP)

The device incorporates an OVP circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVP threshold, which is typical 106% of the internal voltage reference. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops below the lower OVP threshold, which is typical 104%, the high-side MOSFET is allowed to turn on the next clock cycle.

7.3.15 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. After the die temperature decreases below 140°C, the device reinitiates the power-up sequence. The thermal shutdown hysteresis is 20°C.

7.4 Device Functional Modes

7.4.1 Low-Power/Pulse Skipping Operation

When a synchronous buck converter operates at light load or standby conditions, the switching losses are the dominant source of power losses. Under these load conditions, TPS65251-x uses a pulse skipping modulation technique to reduce the switching losses by keeping the power transistors in the off-state for several switching cycles, while maintaining a regulated output voltage. Figure 7-4 shows the output voltage and load plus the inductor current.

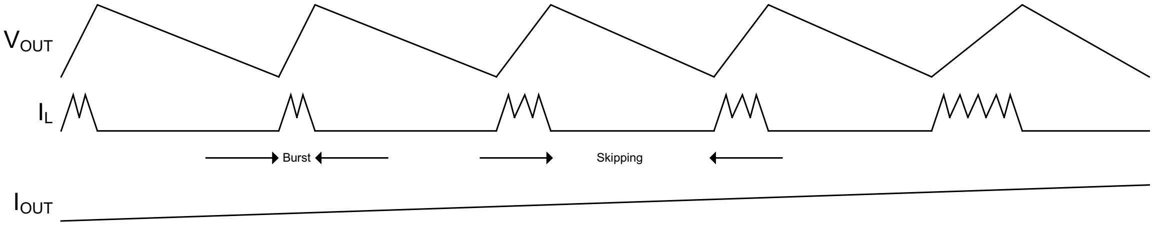


Figure 7-4. Low Power/Pulse Skipping

During the burst mode, the converter continuously charges up the output capacitor until the output voltage reaches a certain limit threshold. The operation of the converter in this interval is equivalent to the peak inductor current mode control. In each switch period, the main switch is turned on until the inductor current reaches the peak current limit threshold. As the load increases, the number of pulses increases to make sure that the output voltage stays within regulation limits. When the load is very light, the low-power controller has a zero crossing detector to allow the low-side MOSFET to operate even in light load conditions. The transistor is not disabled at light loads. A zero crossing detection circuit disables it when inductor current reverses. During the whole process, the body diode does not conduct, but is used as blocking diode only.

During the skipping interval, the upper and lower transistors are turned off and the converter stays in idle mode. The output capacitors are discharged by the load current until the moment when the output voltage drops to a low threshold.

The choice of output filter influences the performance of the low-power circuit. The maximum ripple during low-power mode can be calculated as:

$$V_{OUT\_RIPPLE} = \frac{K_{RIP} T_S}{C_{OUT}} \tag{4}$$

where

- K_{RIP} is 1.4 for Buck 1.
- K_{RIP} is 0.7 for Buck 2 and Buck 3.

T_S can be calculated as:

$$T_S = \frac{0.35}{\left[\left(\frac{V_{IN} - V_{OUT}}{L}\right)\frac{V_{OUT}}{V_{IN}}\right]} \tag{5}$$

8 Application and Implementation

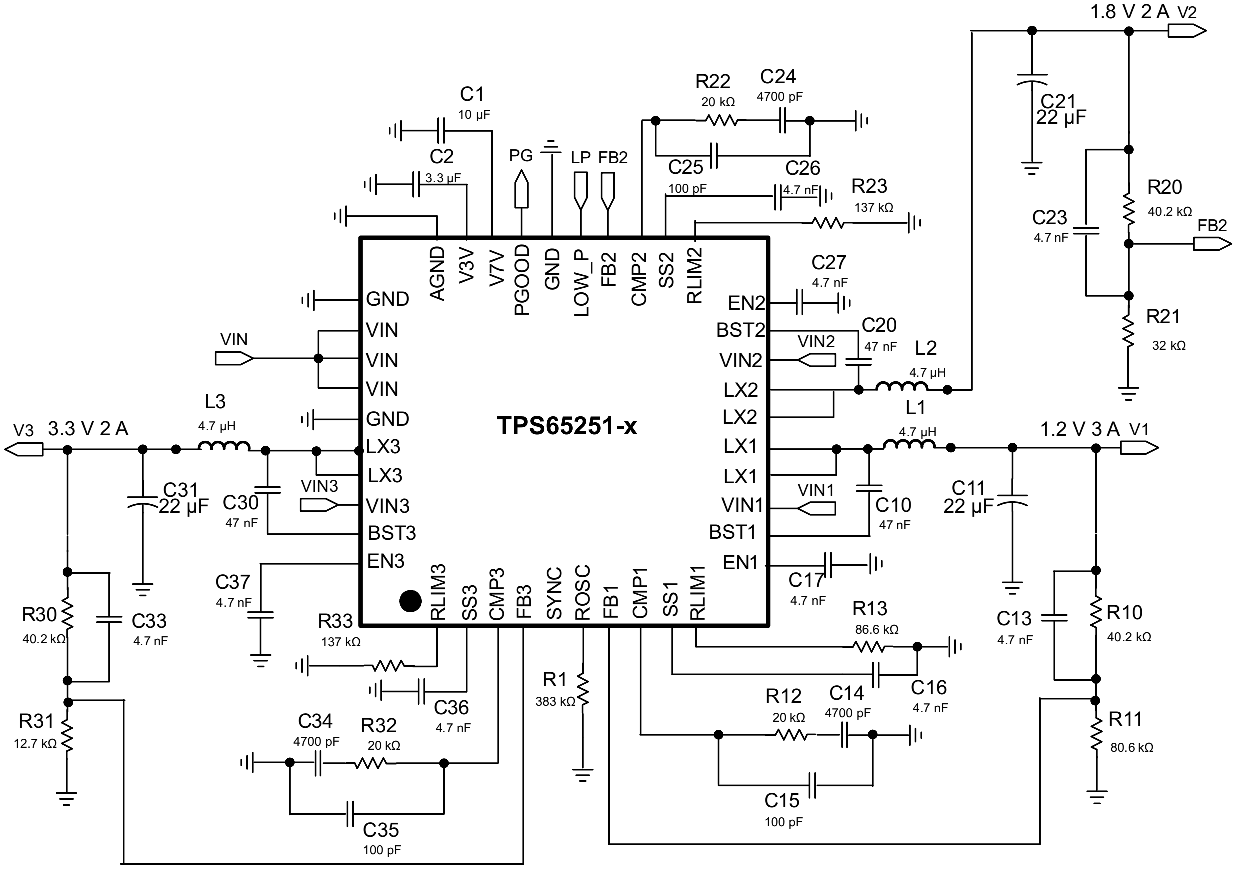
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is triple synchronous step down dc/dc converter. It is typically used to convert a higher dc voltage to lower dc voltages with continuous available output current of 3 A/2 A/2 A. The following design procedure can be used to select component values for the TPS65251-x.

8.2 Typical Application



A. VIN pins require local decoupling capacitors.

Figure 8-1. Typical Application Circuit

8.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Output voltage	1.2 V
Transient response 0.5-A to 2-A load step	120 mV
Maximum output current	3 A
Input voltage	12 V nom, 9.6 to 14.4 V
Output voltage ripple	<30 mV p-p

DESIGN PARAMETERS	VALUE
Switching frequency	500 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Loop Compensation Circuit

A typical compensation circuit could be type II (R_c and C_c) to have a phase margin between 60° and 90°, or type III (R_c, C_c and C_{ff}) to improve the converter transient response. C_{Roll} adds a high frequency pole to attenuate high-frequency noise when needed. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

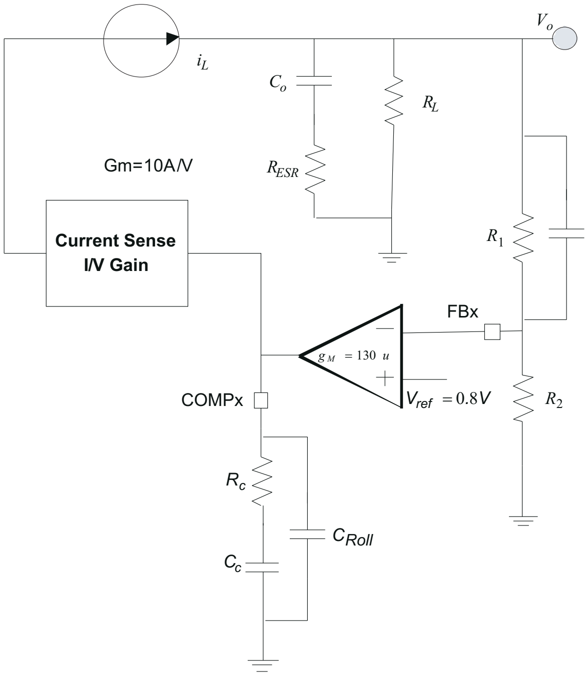


Figure 8-2. Loop Compensation

To calculate the external compensation components use Table 8-1:

Table 8-1. Design Guideline for the Loop Compensation

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies between 500 kHz and 1 MHz give best trade off between performance and cost. When using smaller L and Cs, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Type III circuit recommended for switching frequencies higher than 500 kHz.
Select cross over frequency (fc) to be less than 1/5 to 1/10 of switching frequency.	Suggested fc = fs/10	Suggested fc = fs/10
Set and calculate R_c.	$R_C = \frac{2\pi \times f_c \times V_O \times C_O}{g_M \times Vref \times gm_{ps}}$ (6)	$R_C = \frac{2\pi \times f_c \times C_O}{g_M \times gm_{ps}}$ (7)
Calculate C_c by placing a compensation zero at or before the converter dominant pole $f p = \frac{1}{C_O \times R_L \times 2\pi}$ (8)	$C_c = \frac{R_L \times Co}{R_c}$ (9)	$C_c = \frac{R_L \times Co}{R_c}$ (10)

Table 8-1. Design Guideline for the Loop Compensation (continued)

	TYPE II CIRCUIT	TYPE III CIRCUIT
Add C_{Roll} if needed to remove large signal coupling to high impedance COMP node. Make sure that $fp_{Roll} = \frac{1}{2 \times \pi \times R_C \times C_{Roll}}$ (11) is at least twice the cross over frequency.	$C_{Roll} = \frac{Re_{sr} \times C_O}{R_C}$ (12)	$C_{Roll} = \frac{Re_{sr} \times C_O}{R_C}$ (13)
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff} is smaller than soft-start equivalent frequency ($1/T_{ss}$).	NA	$C_{ff} = \frac{1}{2 \times \pi \times fz_{ff} \times R_1}$ (14)

8.2.2.2 Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, you will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the converter's performance. The converter is capable of running from 300 kHz to 2.2 MHz. Unless a small solution size is an ultimate goal, a moderate switching frequency of 500 kHz is selected to achieve both a small solution size and a high efficiency operation. Using Figure 7-1, R1 is determined to be 383 kΩ

8.2.2.3 Output Inductor Selection

To calculate the value of the output inductor, use Equation 15. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, KIND is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use KIND = 0.2 and the inductor value is calculated to be 3.6 µH. For this design, a nearest standard value was chosen: 4.7 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 16 and Equation 17.

$$Lo = \frac{Vin - Vout}{Io \times K_{ind}} \times \frac{Vout}{Vin \times fsw} \tag{15}$$

$$Iripple = \frac{Vin - Vout}{Lo} \times \frac{Vout}{Vin \times fsw} \tag{16}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times Lo \times fsw} \right)^2} \tag{17}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{18}$$

8.2.2.4 Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements.

Equation 19 gives the minimum output capacitance to meet the transient specification. For this example, L_O = 4.7 µH, ΔI_{OUT} = 1.5 A – 0.75 A = 0.75 A and ΔV_{OUT} = 120 mV. Using these numbers gives a minimum capacitance of 18 µF. A standard 22-µF ceramic capacitor is chose in the design.

$$Co > \frac{\Delta {I_{OUT}}^2 \times L_o}{V_{out} \times \Delta Vout} \tag{19}$$

Equation 20 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. From Equation 16, the output current ripple is 0.46 A. From Equation 20, the minimum output capacitance meeting the output voltage ripple requirement is 1.74 µF.

$$\mathrm{Co} > \frac{1}{8 \times f\mathrm{sw}} \times \frac{1}{\frac{\mathrm{Vripple}}{\mathrm{Iripple}}} \tag{20}$$

Additional capacitance de-rating for aging, temperature and DC bias should influence this minimum value. For this example, one 22-µF, 6.3-V X7R ceramic capacitor with 3 mΩ of ESR will be used.

8.2.2.5 Input Capacitor

A minimum 10-µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND. These capacitors should be connected as close as physically possible to the input pins of the converters as they handle the RMS ripple current shown in Equation 21. For this example, I_{OUT} = 3 A, V_{OUT} = 1.2 V, V_{INmin} = 9.6 V, from Equation 21, the input capacitors must support a ripple current of 0.99 A RMS.

$$\mathrm{Icirms} = \mathrm{Iout} \times \sqrt{\frac{\mathrm{Vout}}{\mathrm{Vinmin}} \times \frac{(\mathrm{Vinmin} - \mathrm{Vout})}{\mathrm{Vinmin}}} \tag{21}$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 22. Using the design example values, I_{OUTmax} = 3 A, C_{IN} = 10 µF, f_{SW} = 500 kHz, yields an input voltage ripple of 150 mV.

$$\Delta\mathrm{Vin} = \frac{\mathrm{Ioutmax} \times 0.25}{\mathrm{Cin} \times f\mathrm{sw}} \tag{22}$$

8.2.2.6 Soft-Start Capacitor

The soft-start capacitor determines the minimum amount of time it will take for the output voltage to reach its nominal programmed value during power-up. This is useful if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level.

The soft-start capacitor value can be calculated using Equation 23. In this example, the converter's soft-start time is 0.8 ms. In TPS65251-x, Iss is 5 µA and Vref is 0.8 V. From Equation 23, the soft-start capacitance is 5 nF. A standard 4.7-nF ceramic capacitor is chosen in this design. In this example, C16 is 4.7 nF

$$\mathrm{Css(nF)} = \frac{\mathrm{Tss(ms)} \times \mathrm{Iss(\mu A)}}{\mathrm{Vref(V)}} \tag{23}$$

8.2.2.7 Bootstrap Capacitor Selection

A 0.047-µF ceramic capacitor must be connected between the BST to LX pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10-V or higher voltage rating.

8.2.2.8 Adjustable Current Limiting Resistor Selection

The converter uses the voltage drop on the high-side MOSFET to measure the inductor current. The overcurrent protection threshold can be optimized by changing the trip resistor. Figure 6-6 governs the threshold of overcurrent protection for Buck 1. When selecting a resistor, do not exceed the graph limits. In this example, the over current threshold is 3.2 A. In order to prevent a premature limit trip, the minimum line is used and the resistor is 86.6 kΩ.

When setting high-side current limit to large current values, ensure that the additional load immediately prior to an overcurrent condition will not cause the switching node voltage to exceed 20 V. Additionally, ensure during worst case operation, with all bucks loaded immediately prior to current limit, the maximum virtual junction temperature of the device does not exceed 125°C.

8.2.2.9 Output Voltage and Feedback Resistors Selection

For the example design, 40.2 kΩ was selected for R10. Vout is 1.2 V, Vref = 0.8 V. Using Equation 24, R11 is calculated as 80.4 kΩ. A standard 80.6-kΩ resistor is chose in this design.

$$R11 = \frac{Vout - Vref}{Vref} \times R10 \tag{24}$$

8.2.2.10 Compensation

A type-II compensation circuit is adequate for the converter to have a phase margin between 60 and 90 degrees. The following equations show the procedure of designing a peak current mode control dc/dc converter.

The compensation design takes the following steps:

1. Set up the anticipated cross-over frequency. In this example, the anticipated cross-over frequency (fc) is 65 kHz. The power stage gain (gm_{PS}) is 10 A/V and the GM amplifier gain (g_M) is 130 μA/V.

$$R12 = \frac{2\pi \times fc \times Vo \times Co}{g_M \times Vref \times gm_{ps}} \tag{25}$$

2. Place compensation zero at low frequency to boost the phase margin at the crossover frequency. From the procedures above, the compensation network includes a 20-kΩ resistor (R12) and a 4700-pF capacitor (C1).
3. An additional pole can be added to attenuate high frequency noise.

From the procedures above, the compensation network includes a 20-kΩ resistor (R12) and a 4700-pF capacitor (C14).

8.2.2.11 3.3-V and 6.5-V LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 10 μF for V7V pin 28
- 3.3 μF to 10 μF for V3V pin 29

8.2.3 Application Curves

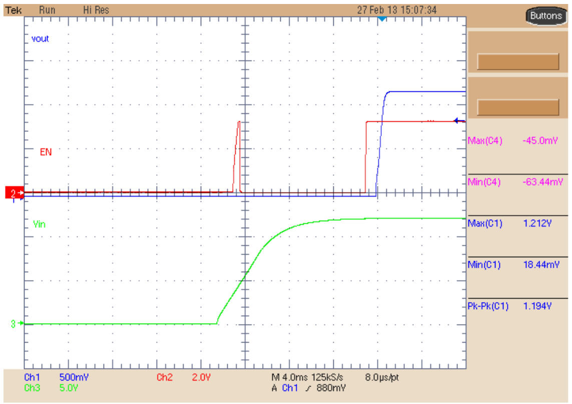


Figure 8-3. Buck 1 Start-Up (Ch3 = V_{IN})

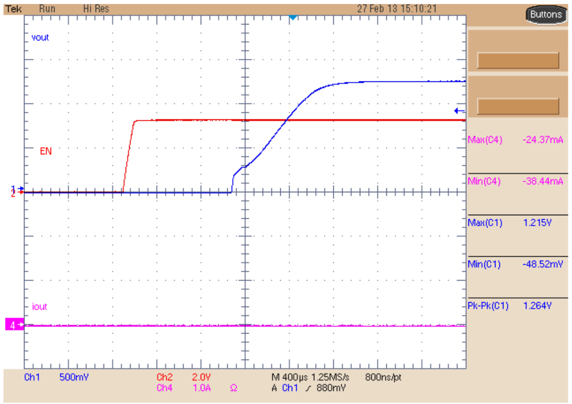


Figure 8-4. Buck 1 Soft-Start

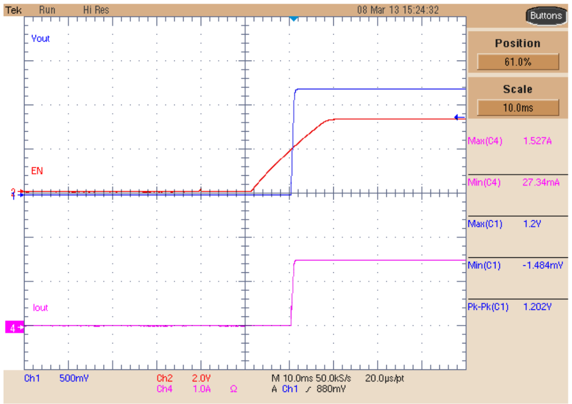


Figure 8-5. Buck 1 Start-Up 1.5-A Resistive

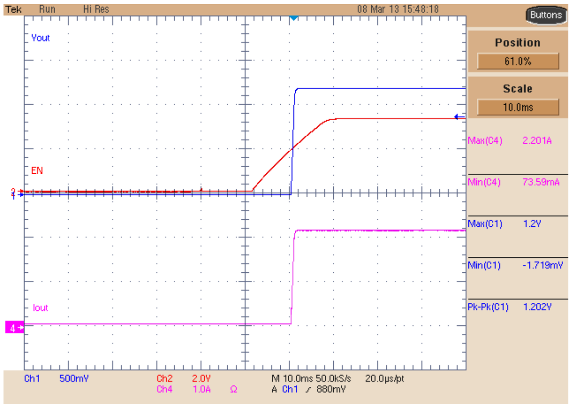


Figure 8-6. Buck 1 Soft-Start 2-A Load

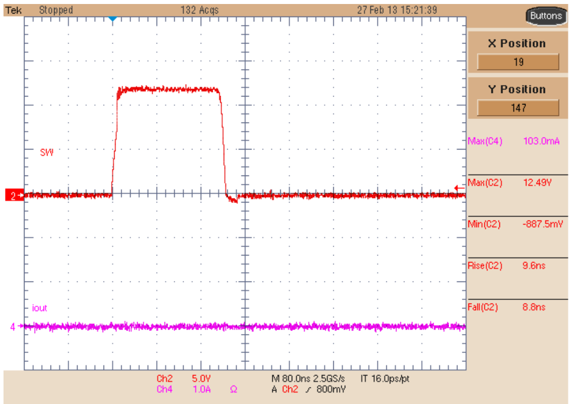


Figure 8-7. Buck 1 Switching Node, No Load

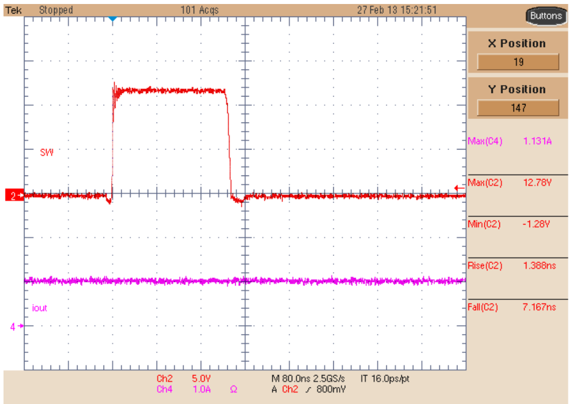


Figure 8-8. Buck 1 Switching Node, 1-A Load

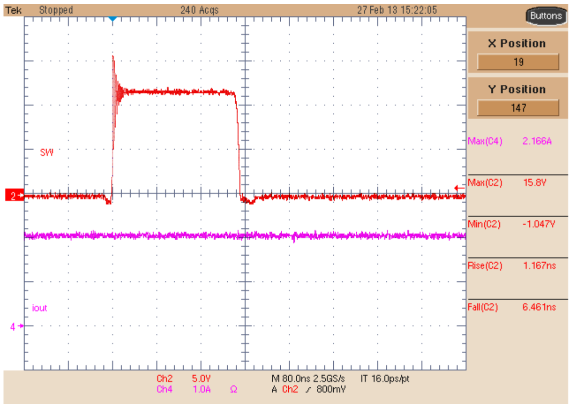


Figure 8-9. Buck 1 Switching Node, 2-A Load

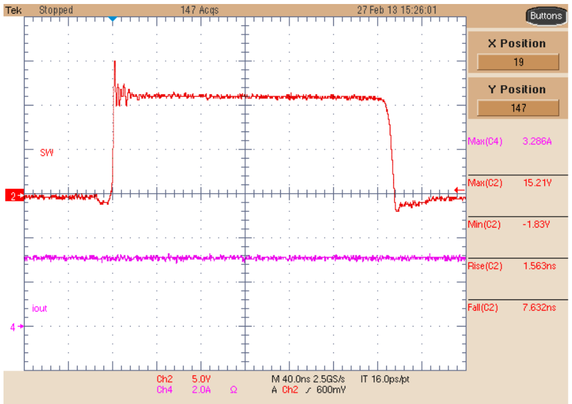


Figure 8-10. Buck 1 Switching Node, 3-A Load

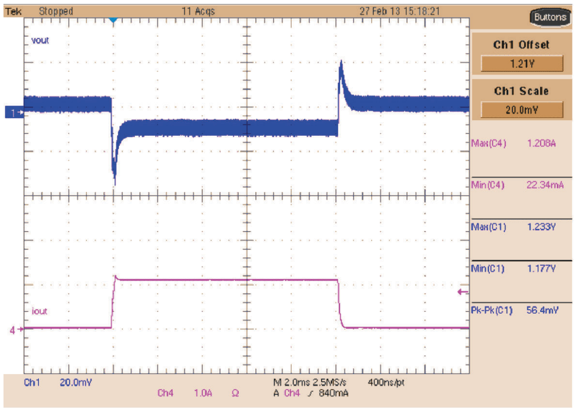


Figure 8-11. Buck 1 Dynamic Response, 0- to 1-A Step

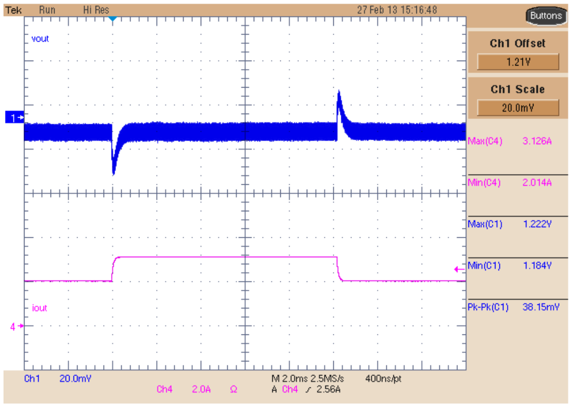


Figure 8-12. Buck 1 Dynamic Response, 2-A to 3-A Step

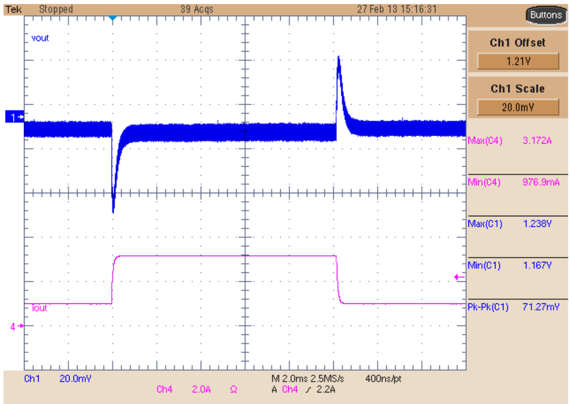


Figure 8-13. Buck 1 Dynamic Response, 1-A to 3-A Step

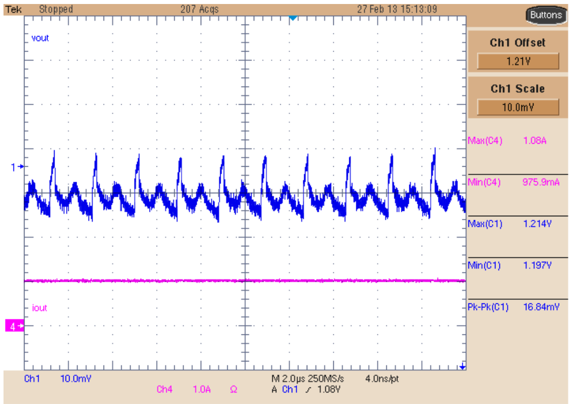


Figure 8-14. Buck 1 Ripple, 1-A Load

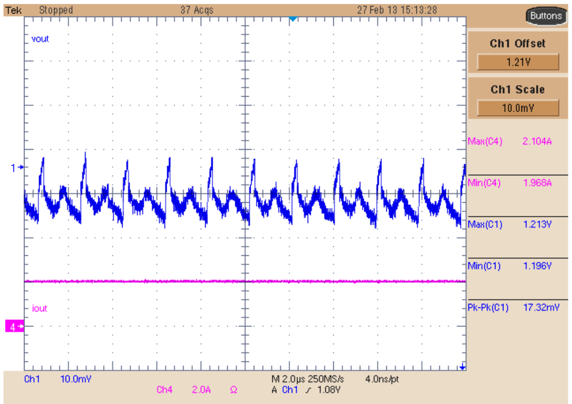


Figure 8-15. Buck 1 Ripple, 2-A Load

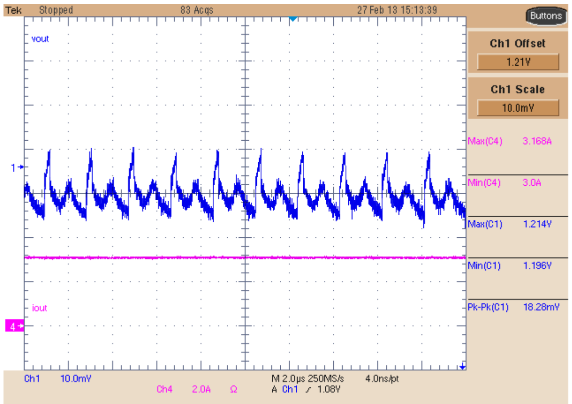
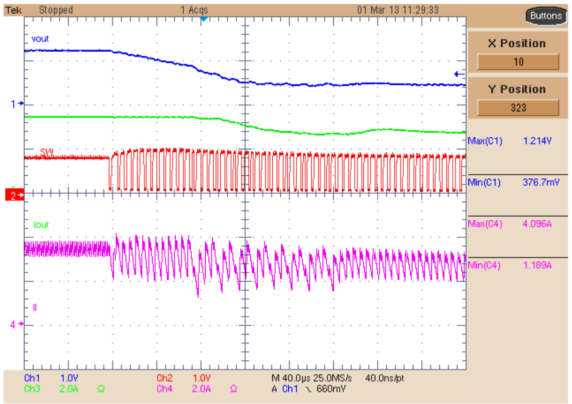
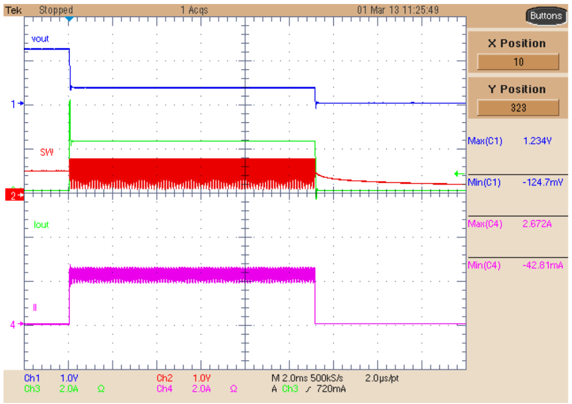


Figure 8-16. Buck 1 Ripple, 3-A Load



Ch1 = V_{OUT} Ch2 = COMP1 Ch3 = I_{OUT}
Ch4 = Inductor

Figure 8-17. Buck 1 Current Limit Operation With Slow Rising Output Current, Trip at 4 A



Ch1 = V_{OUT} Ch2 = COMP1 Ch3 = I_{OUT}
Ch4 = Inductor

Figure 8-18. Buck 1 Current Limit Operation, Hiccup

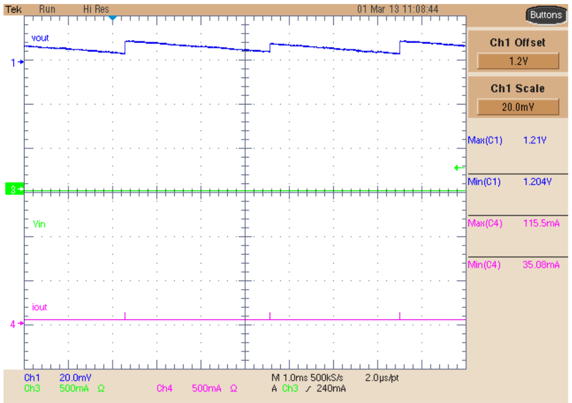


Figure 8-19. Buck 1 Low-Power Output, No Load

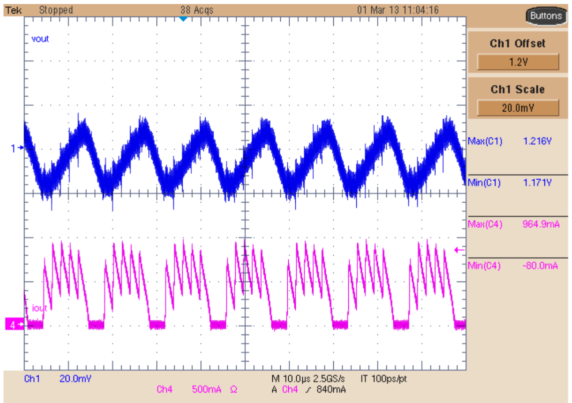
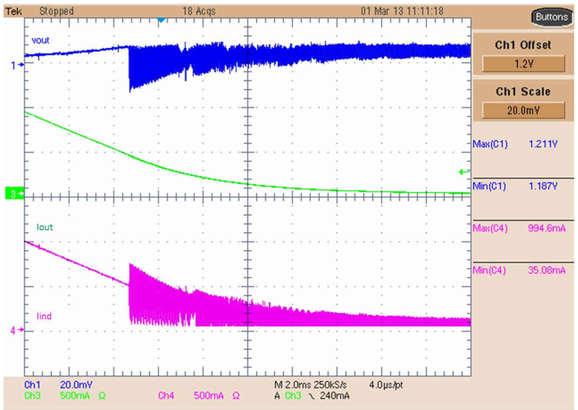
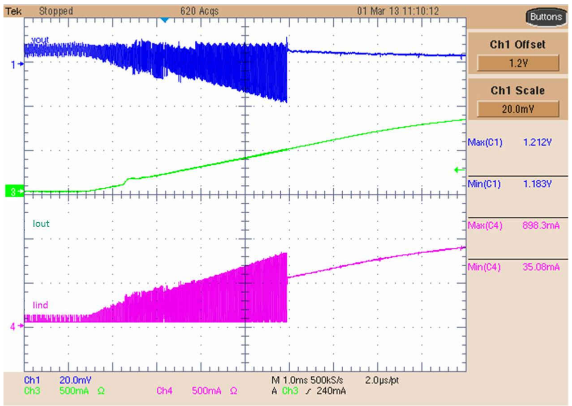


Figure 8-20. Buck 1 Low-Power Operation



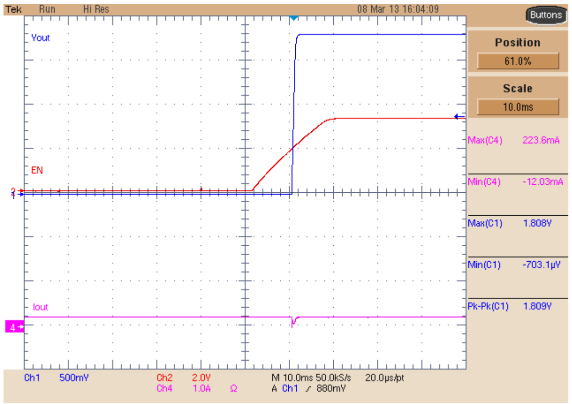
Ch1 = V_{OUT} Ch3 = I_{OUT} Ch4 = Inductor

Figure 8-21. Buck 1 PFM to PWM Transition



Ch1 = V_{OUT} Ch3 = I_{OUT} Ch4 = Inductor

Figure 8-22. Buck 1 PWM to PFM Transition



Ch3 = V_{IN}

Figure 8-23. Buck 2 Start-Up, No Load

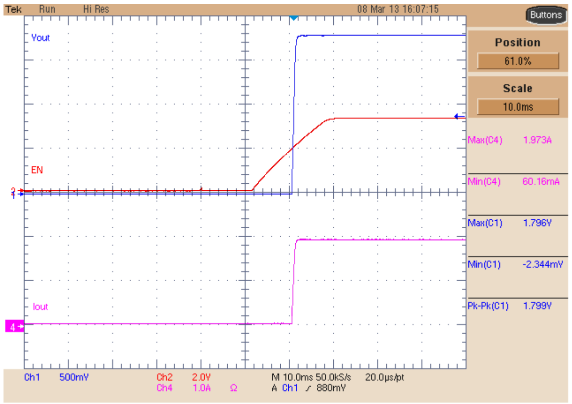


Figure 8-24. Buck 2 Start-Up, 2-A Load

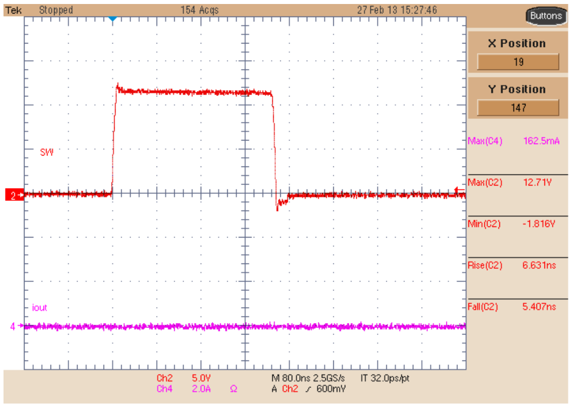


Figure 8-25. Buck 2 Switching Node, No Load

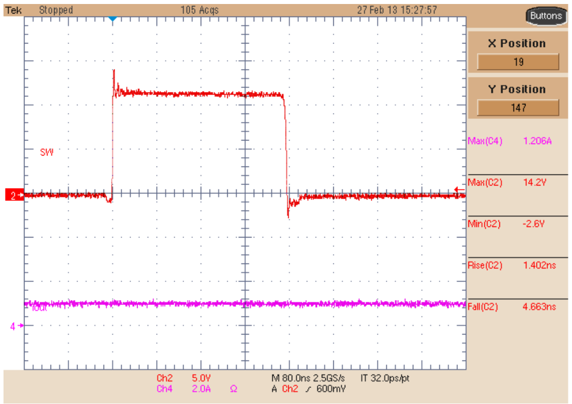


Figure 8-26. Buck 2 Switching Node, 1-A Load

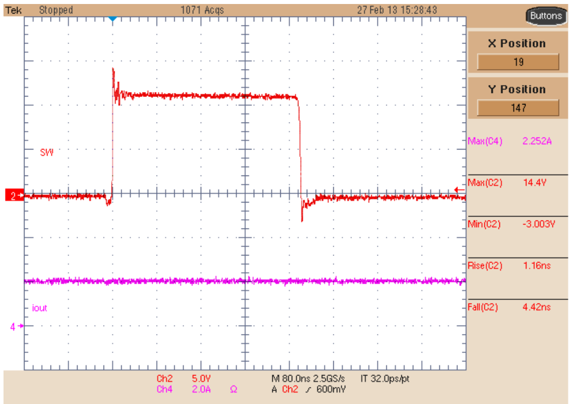


Figure 8-27. Buck 2 Switching Node, 2-A Load

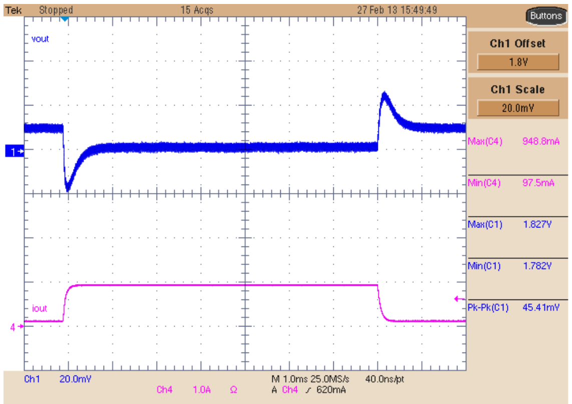


Figure 8-28. Buck 2 Dynamic Response, 0-A to 1-A Step

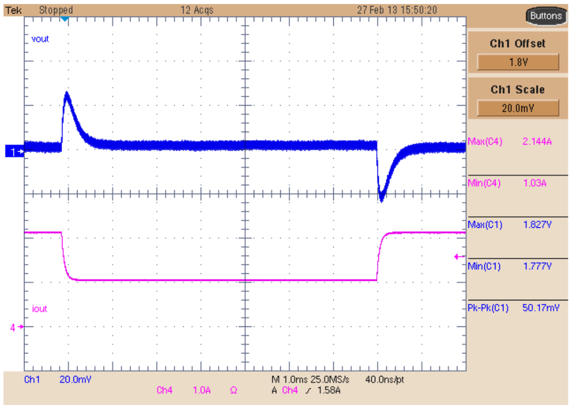


Figure 8-29. Buck 2 Dynamic Response, 1-A to 2-A Step

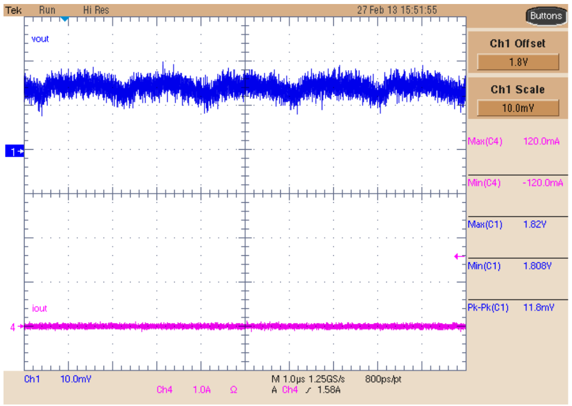


Figure 8-30. Buck 2 Ripple, No Load

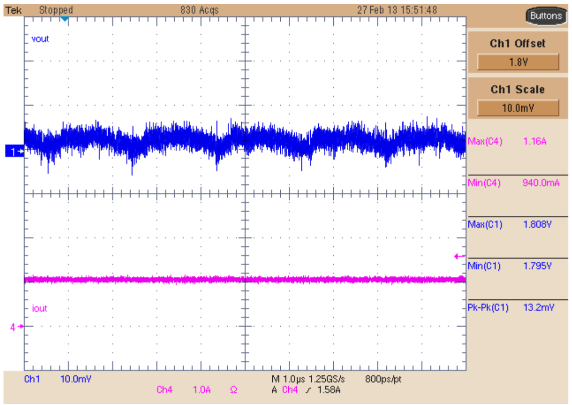


Figure 8-31. Buck 2 Ripple, 1-A Load

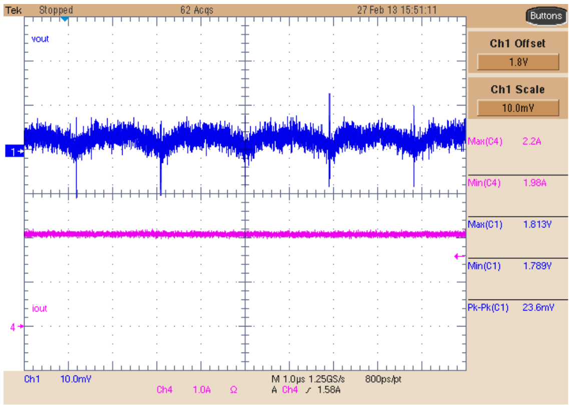


Figure 8-32. Buck 2 Ripple, 3-A Load

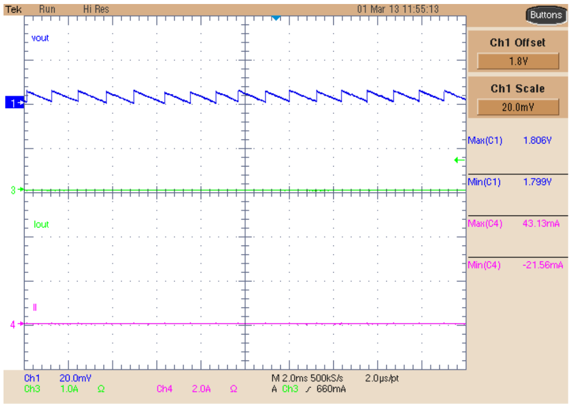
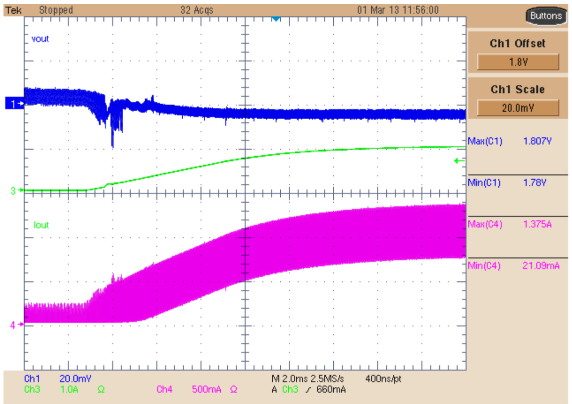
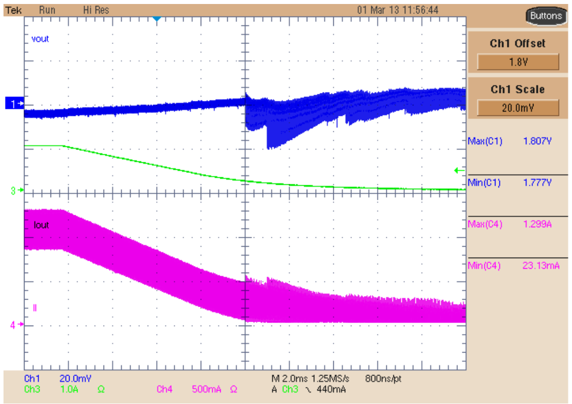


Figure 8-33. Buck 2 Low-Power Output, No Load



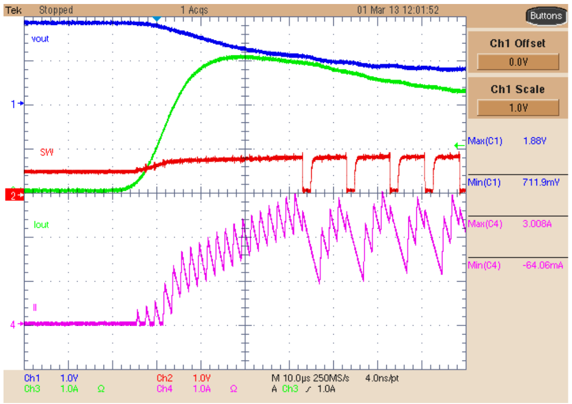
Ch1 = V_{OUT} Ch3 = I_{OUT} Ch4 = Inductor

Figure 8-34. Buck 2 PFM to PWM Transition



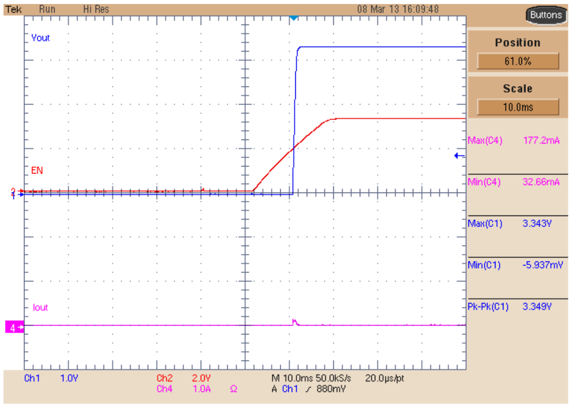
Ch1 = V_{OUT} Ch3 = I_{OUT} Ch4 = Inductor

Figure 8-35. Buck 2 PWM to PFM Transition



Ch1 = V_{OUT} Ch2 = COMP1 Ch3 = I_{OUT}
Ch4 = Inductor

Figure 8-36. Buck 2 Current Limit Operation



Ch3 = V_{IN}

Figure 8-37. Buck 3 Start-Up

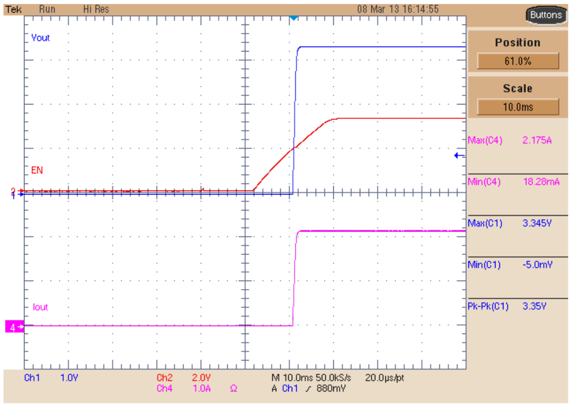


Figure 8-38. Buck 3 Soft-Start

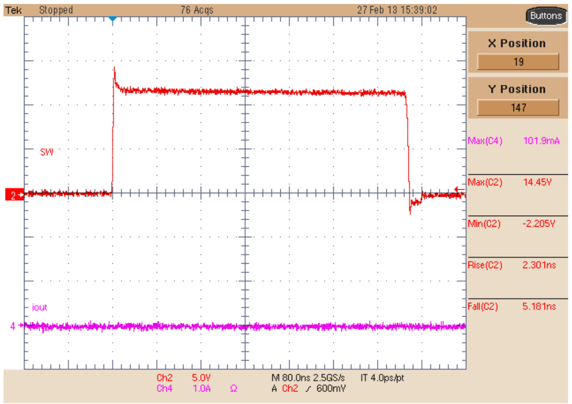


Figure 8-39. Buck 3 Switching Node, No Load

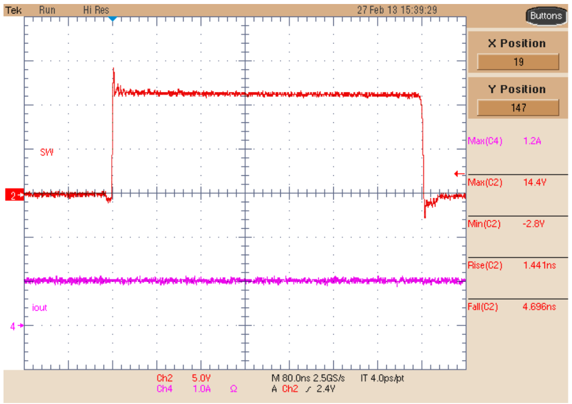


Figure 8-40. Buck 3 Switching Node, 1-A Load

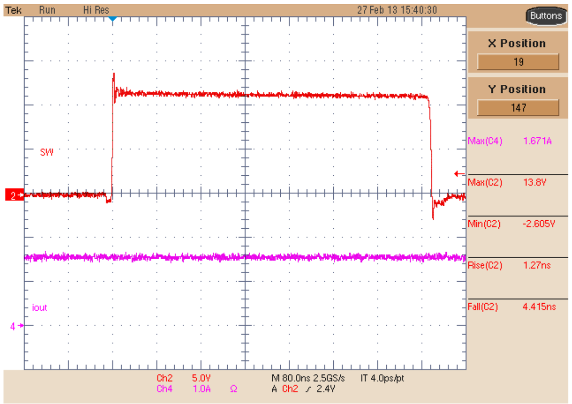


Figure 8-41. Buck 3 Switching Node, 1.5-A Load

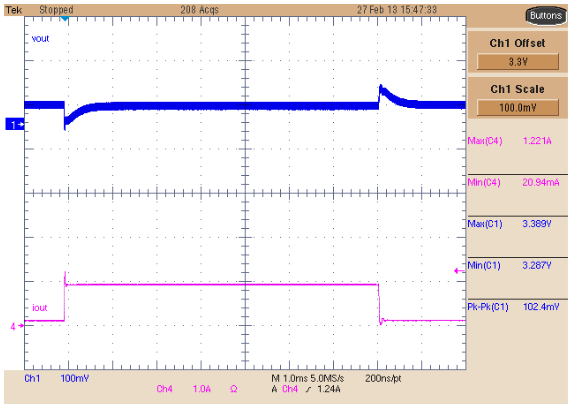


Figure 8-42. Buck 3 Dynamic Response, 0-A to 1-A Step

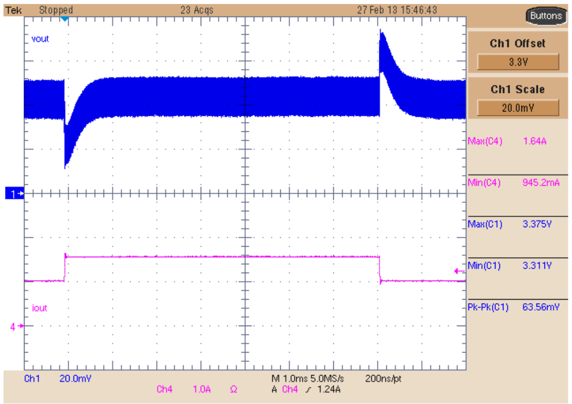


Figure 8-43. Buck 3 Dynamic Response, 1-A to 1.5-A Step

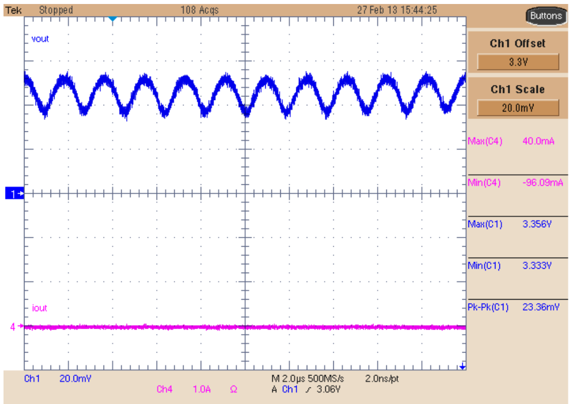


Figure 8-44. Buck 3 Ripple, No Load

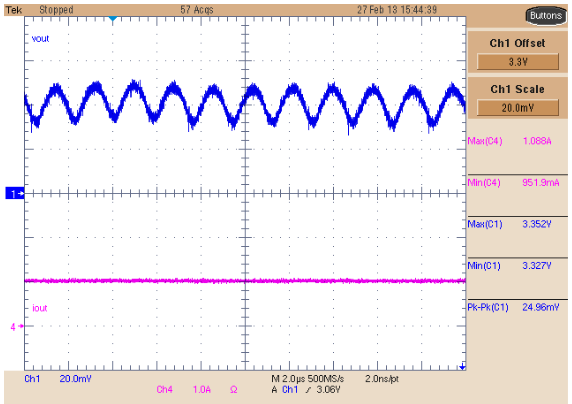


Figure 8-45. Buck 3 Ripple, 1-A Load

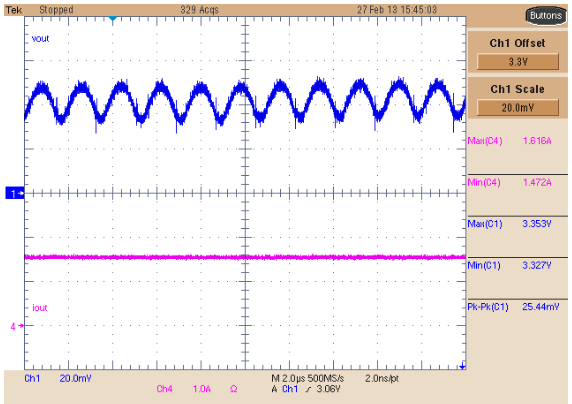


Figure 8-46. Buck 3 Ripple, 3-A Load

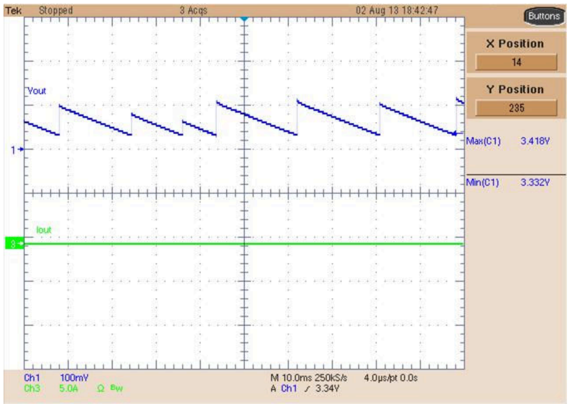
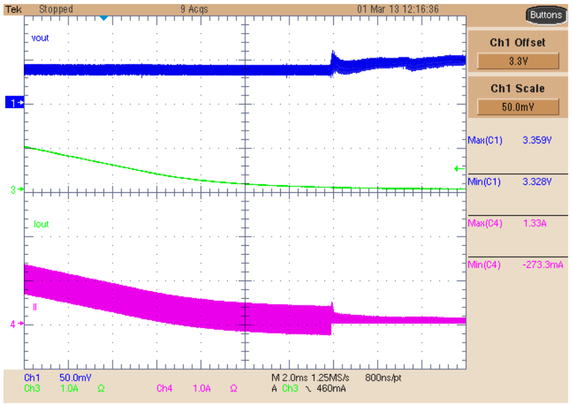
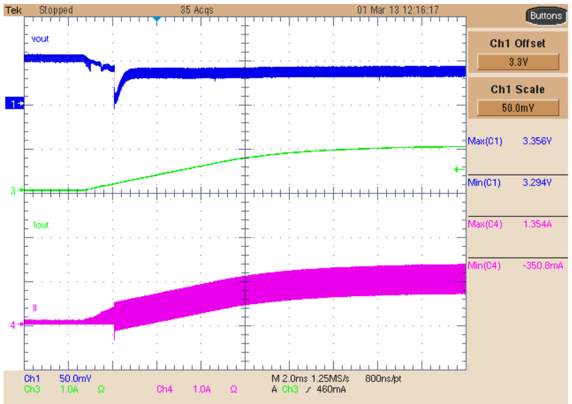


Figure 8-47. Buck 3 Low-Power Output, No Load



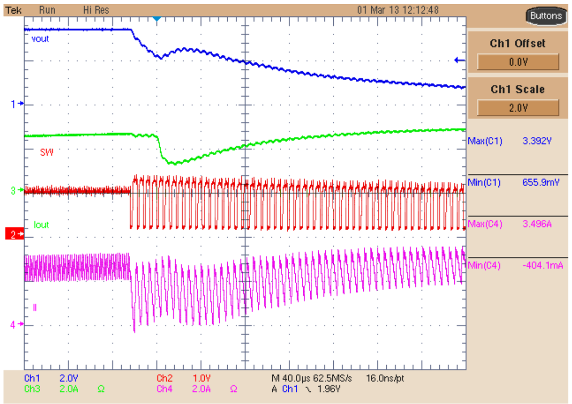
Ch1 = V_{OUT} Ch3 = I_{OUT} Ch4 = Inductor

Figure 8-48. Buck 3 PFM to PWM Transition



Ch1 = V_{OUT} Ch3 = I_{OUT} Ch4 = Inductor

Figure 8-49. Buck 3 PWM to PFM Transition



Ch1 = V_{OUT} Ch2 = COMP1 Ch3 = I_{OUT}
Ch4 = Inductor

Figure 8-50. Buck 3 Current Limit Operation

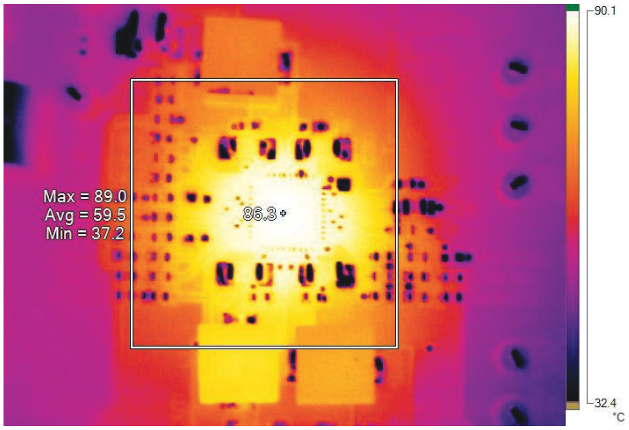


Figure 8-51. Temperature Profile, V_O = 1.2 V, I_O = 3 A, V_O = 1.8 V, I_O = 2 A, V_O = 3.3 V, I_O = 2 A, T_A = 28°C

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4.5 V and 18 V. This input power supply should be well regulated. If the input supply is located more than a few inches from the TPS65251-x converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of PMIC designs.

- Place VOUT, and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area sould be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter cpacitor and directly under the TPS65251-x device to provide a thermal path from the Powerpad land to ground.
- The AGND pin should be tied directly to the power pad under the IC and the power pad.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the COMP pins. The COMP and OSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

10.2 Layout Example

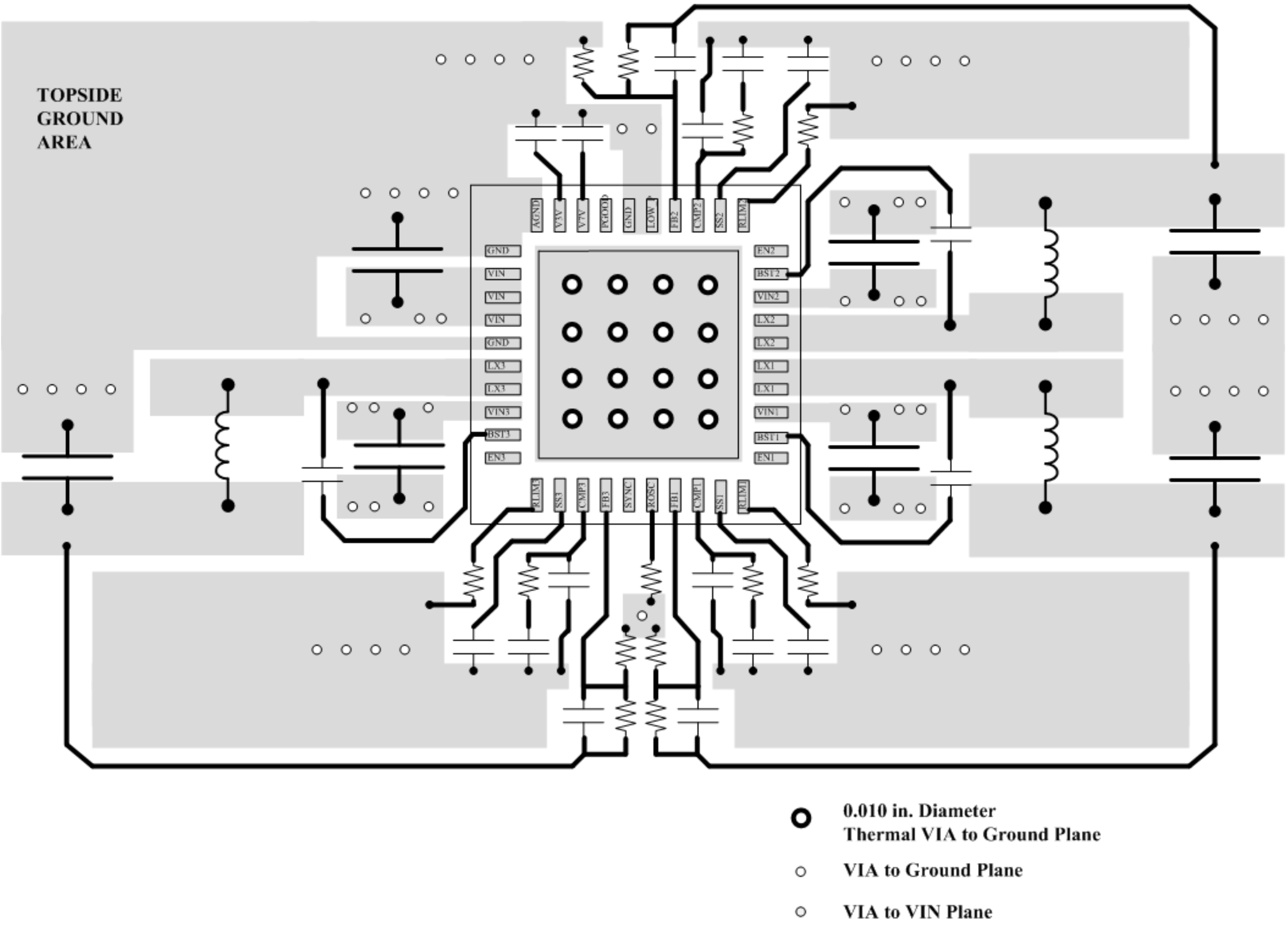


Figure 10-1. Layout Schematic

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

Blu-ray™ is a trademark of Blu-ray Disc Association.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65251-1RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-1
TPS65251-1RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-1
TPS65251-1RHARG4	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-1
TPS65251-1RHARG4.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-1
TPS65251-1RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-1
TPS65251-1RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-1
TPS65251-2RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-2
TPS65251-2RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-2
TPS65251-2RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-2
TPS65251-2RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-2
TPS65251-3RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-3
TPS65251-3RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-3
TPS65251-3RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-3
TPS65251-3RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65251-3

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

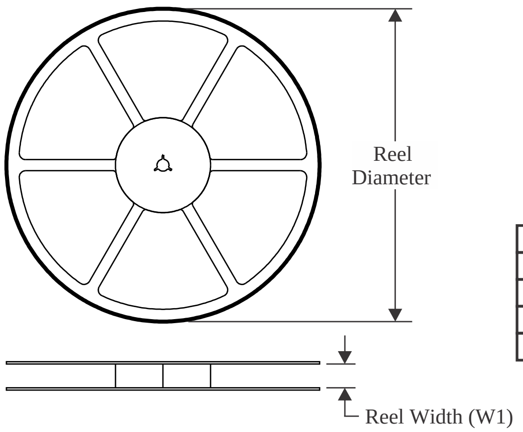
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

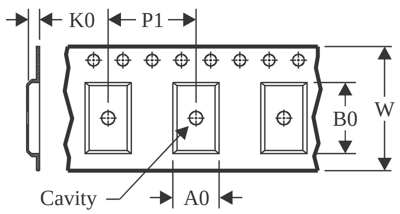
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

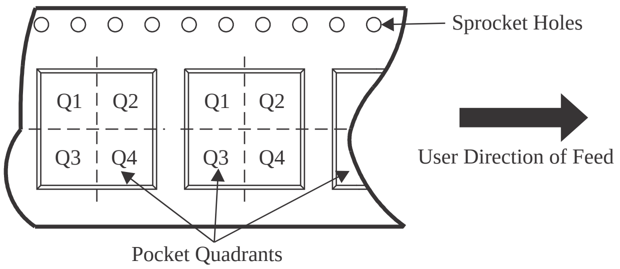


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

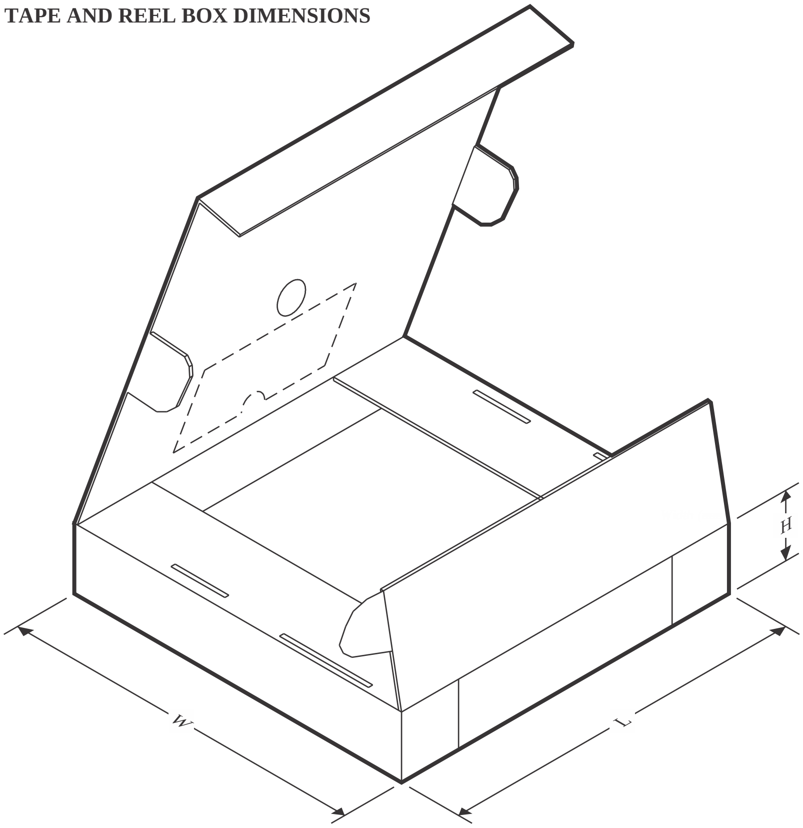
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65251-1RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65251-1RHARG4	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65251-1RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65251-2RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65251-2RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65251-3RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65251-3RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65251-1RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65251-1RHARG4	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65251-1RHAT	VQFN	RHA	40	250	210.0	185.0	35.0
TPS65251-2RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65251-2RHAT	VQFN	RHA	40	250	210.0	185.0	35.0
TPS65251-3RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65251-3RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

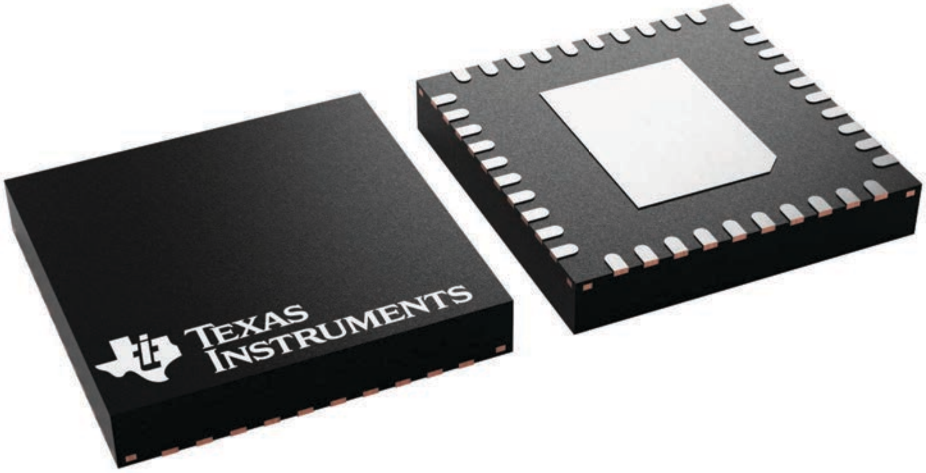
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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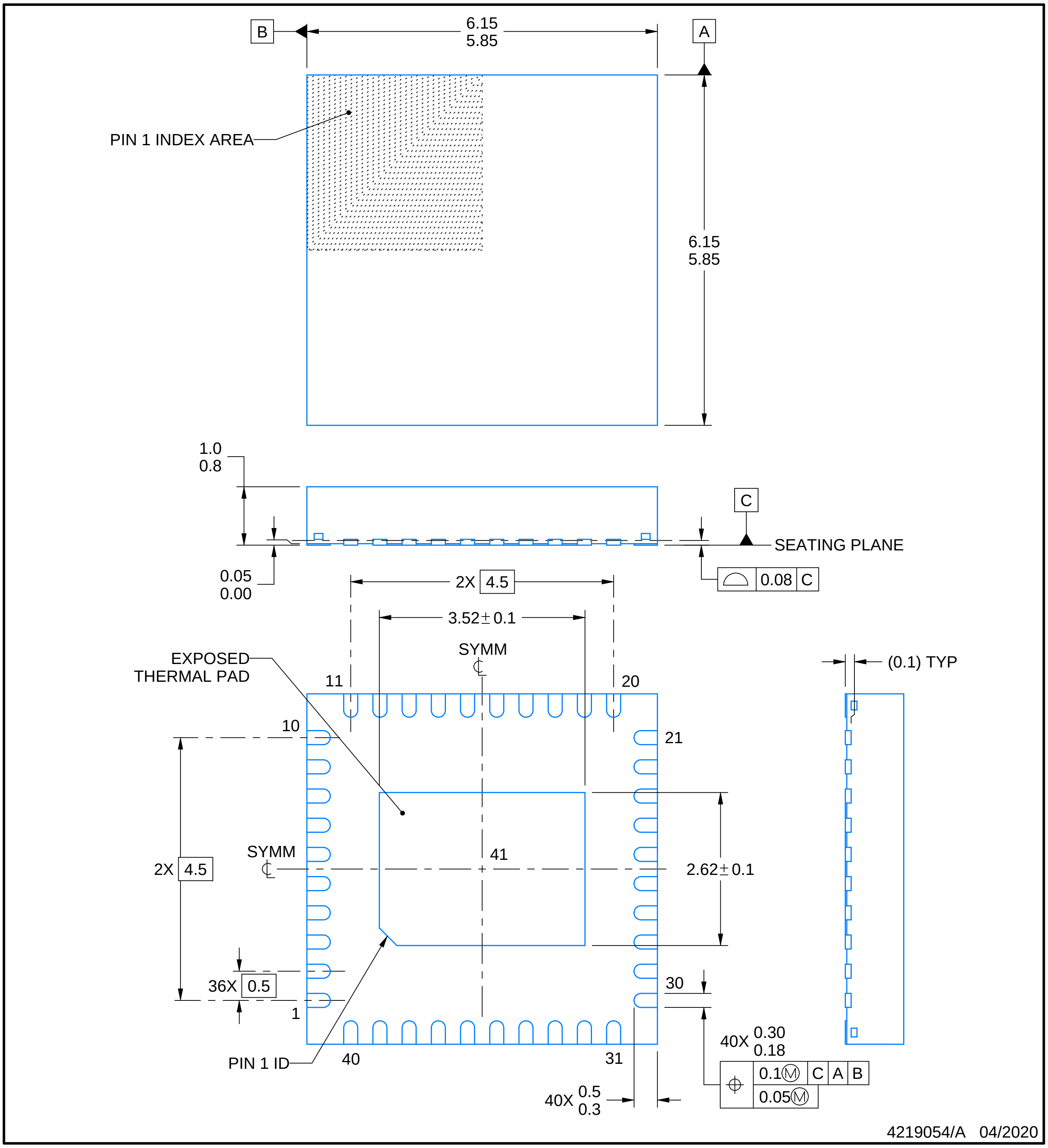
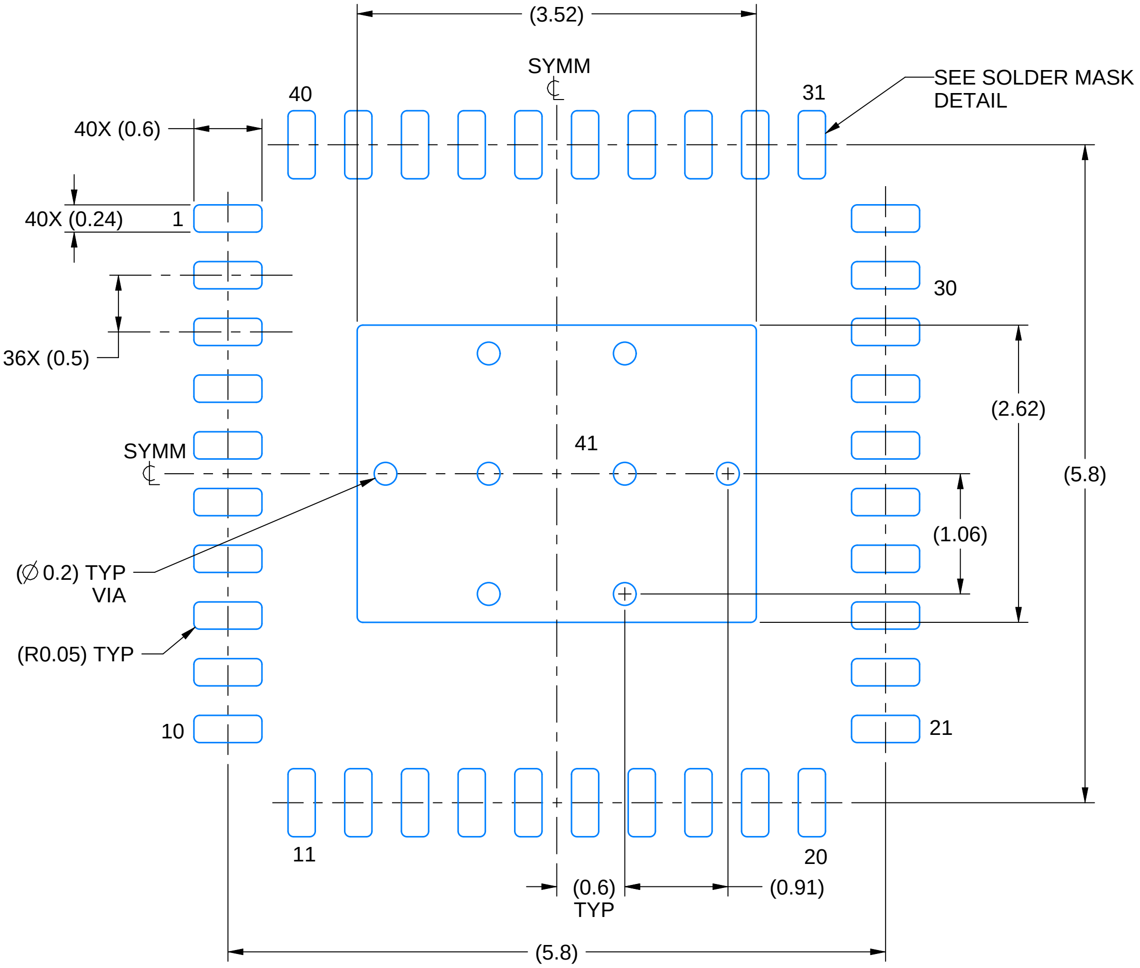
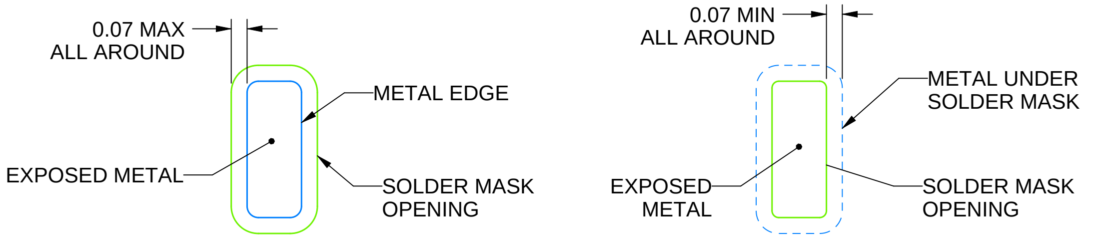


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



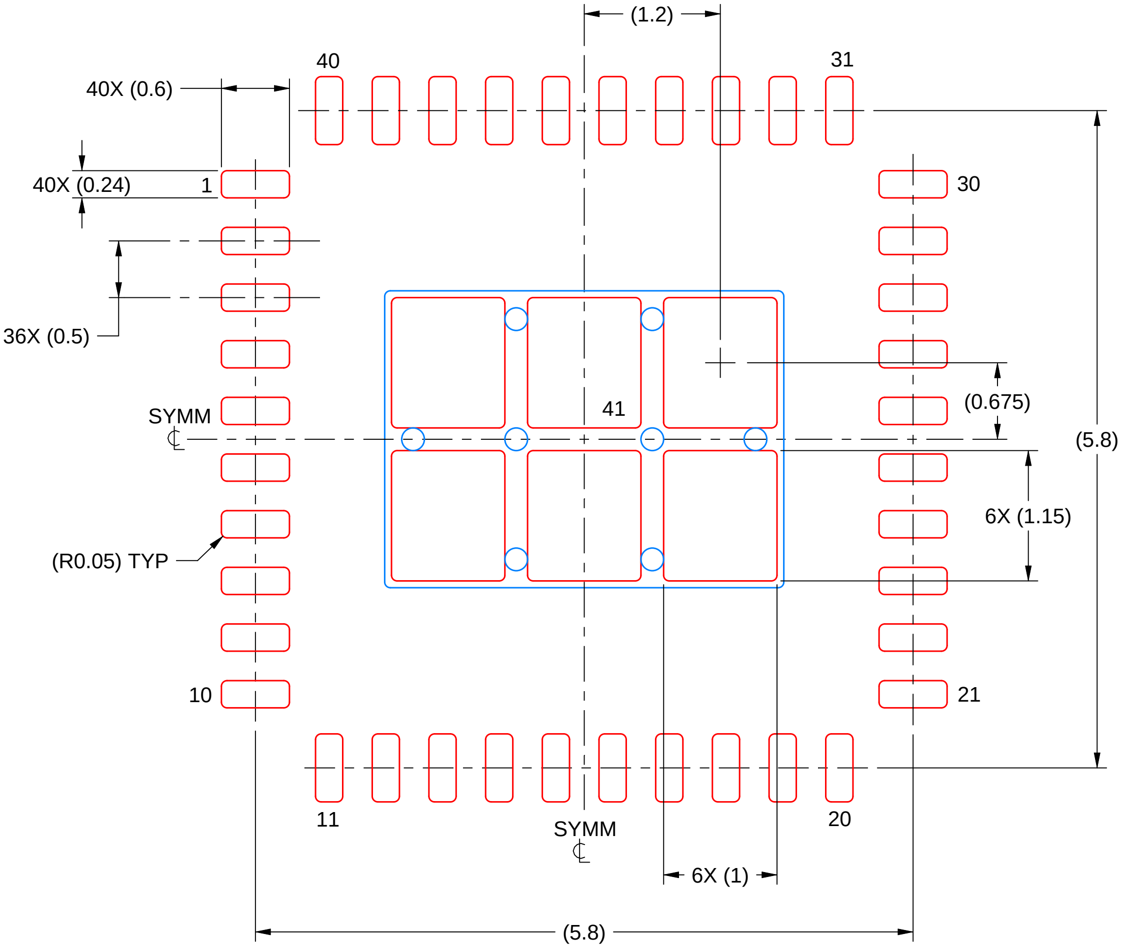
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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