

# TPS65215-Q1 Power Management IC (PMIC) with 3 BUCKs and 2 LDOs for Automotive **Applications**

#### 1 Features

- 3 buck converters at up to 2.3MHz switching frequency.
  - 1× VIN: 2.5V 5.5V; I<sub>OUT</sub>: 3.5A; V<sub>OUT</sub> 0.6V –
  - 2× VIN: 2.5V 5.5V; I<sub>OUT</sub>: 1.5A; V<sub>OUT</sub> 0.6V 3.4V
- 2 linear regulators:
  - 1x VIN: 1.5V 5.5V; I<sub>OUT</sub>: 400mA; V<sub>OUT</sub>: 0.6V 3.4V (configurable as load switch and bypassmode, supporting SD-card)
  - 1x VIN: 2.2V 5.5V; I<sub>OUT</sub>: 300mA; V<sub>OUT</sub>: 1.2V 3.3V (configurable as load switch)
- Dynamic voltage scaling on all three buck
- Low IQ/PFM, PWM-mode (quasi-fixed frequency) or fixed frequency mode
- Programmable power sequencing and default voltages
- I<sup>2</sup>C interface, supporting standard, fast-mode and fast-mode+
- 2 GPOs, 1 GPIO, and 3 multi-function-pins
- **EEPROM** programmability
- Functional safety capable

# 2 Applications

- Low power automotive MPUs such as AM62x-Q1 and AM64x-Q1
- Head units, Digital Cluster, Telematic Control Units, Lidar Proc.
- DMS/OMS, eMirror and CMS
- Automotive Lighting
- **Automotive Audio Amplifiers**
- Powertrain
- ISP and deep learning

## 3 Description

The TPS65215-Q1 is a Power Management IC (PMIC) designed to supply a wide range of SoCs in automotive applications. The device is characterized across an ambient temperature range of -40°C to +125°C, making the PMIC an excellent choice for automotive applications. The device includes three synchronous stepdown DC-DC converters and two linear regulators.

The DC-DC converters are capable of 1x 3.5A and 2x 1.5A. The converters require a small 470nH inductor, 4.7µF input capacitance, and a minimum 10µF output capacitance per rail depending on the switching mode configuration.

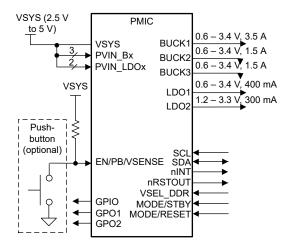
One of the LDOs supports an output current of 400mA at an output voltage range of 0.6V to 3.4V. The LDO supports bypass mode, acting as a load-switch, and allow voltage-changes during operation. The other LDO supports an output current of 300mA at an output voltage range of 1.2V to 3.3V. The LDO also supports load-switch mode.

The I2C-interface, IOs, GPIOs and multi-function-pins (MFP) allow a seamless interface to a wide range of SoCs.

## **Package Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE (NOM)
TPS65215-Q1	32-pin QFN - Wettable Flank	5.00mm × 5.00mm

For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application



# **Table of Contents**

1 Features1	6.1 Overview28
2 Applications1	6.2 Functional Block Diagram29
3 Description1	6.3 Feature Description30
4 Pin Configuration and Functions3	6.4 Device Functional Modes53
5 Specifications7	6.5 Multi-PMIC Operation59
5.1 Absolute Maximum Ratings7	6.6 User Registers63
5.2 ESD Ratings	6.7 Device Registers64
5.3 Recommended Operating Conditions7	7 Application and Implementation130
5.4 Thermal Information9	7.1 Application Information
5.5 System Control Thresholds9	7.2 Typical Application130
5.6 BUCK1 Converter	7.3 Power Supply Recommendations137
5.7 BUCK2, BUCK3 Converter14	7.4 Layout138
5.8 General Purpose LDOs (LDO1)17	8 Device and Documentation Support140
5.9 General Purpose LDOs (LDO2)19	8.1 Receiving Notification of Documentation Updates 140
5.10 GPIOs and multi-function pins (EN/PB/	8.2 Support Resources140
VSENSE, nRSTOUT, nINT, GPO1, GPO2, GPIO,	8.3 Trademarks140
MODE/RESET, MODE/STBY, VSEL_SD/	8.4 Electrostatic Discharge Caution140
VSEL_DDR)21	8.5 Glossary140
5.11 Voltage and Temperature Monitors23	9 Revision History140
5.12 I <sup>2</sup> C Interface24	10 Mechanical, Packaging, and Orderable
5.13 Typical Characteristics26	Information141
6 Detailed Description28	



# **4 Pin Configuration and Functions**

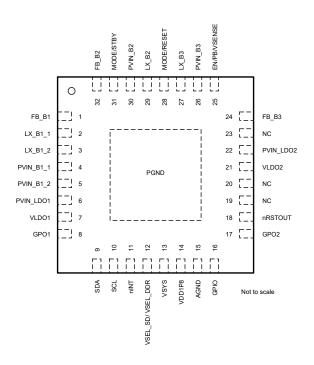


Figure 4-1. TPS65215-Q1 RHB Package, 32-pin QFN (Top View)

**Table 4-1. Pin Functions** 

PIN NAME	PIN NO.	TYPE	DESCRIPTION	CONNECTION if not used (output rails must be permanently disabled)
FB_B1	1	I	Feedback Input for Buck1. Connect to Buck1 output filter. Nominal output voltage is configured in EEPROM.	Connect to GND
LX_B1_1	2	PWR	Switch Pin for Buck1. Connect one side of the Buck1-inductor to this pin.	Leave floating
LX_B1_2	3	PWR	2nd Switch Pin for Buck1. Connect one side of the Buck1-inductor to this pin. Connect to LX_B1_1.	Leave floating
PVIN_B1_1	4	PWR	Power Input for BUCK1. Bypass this pin to ground with a 4.7µF or greater ceramic capacitor. Voltage on PVIN_B1_1 pin must not exceed voltage on VSYS pin.	Connect to VSYS
PVIN_B1_2	5	PWR	2nd Power Input for BUCK1. This pin shares the bypass capacitor from pin 4. Voltage on PVIN_B1_2 pin must not exceed voltage on VSYS pin.	Connect to VSYS
PVIN_LDO1	6	PWR	Power Input for LDO1. Voltage on PVIN_LDO1 pin must not exceed voltage on VSYS pin.	Connect to VSYS
VLDO1	7	PWR	Output Voltage of LDO1. Nominal output voltage is configured in EEPROM. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.	Leave floating
GPO1	8	0	General Purpose Open-Drain Output. Configurable in the power-up and power-down-sequence to enable an external rail.	Leave floating

**Table 4-1. Pin Functions (continued)** 

	Table 4-1. Pin Functions (continued)						
PIN NAME	PIN NO.	TYPE	DESCRIPTION	CONNECTION if not used (output rails must be permanently disabled)			
SDA	9	I/O	Data Pin for the I2C Serial Port. The I2C logic levels depend on the external pull-up voltage.	Connect to VIO			
SCL	10	1	Clock Pin for the I2C Serial Port. The I2C logic levels depend on the external pull-up voltage.	Connect to VIO			
nINT	11	0	Interrupt Request Output. Open-drain driver is pulled low for fault conditions. Released if bit is cleared	Leave floating			
VSEL_SD/ VSEL_DDR	12	I	Multi-Function-Pin: Configured as VSEL_SD: SD-card-IO-voltage select. Connected to SoC. Trigger a voltage change between 1.8V and register-based VOUT on LDO1 or LDO2. Polarity is configurable. Configured as VSEL_DDR: DDR-voltage selection. Hard-wired pull-up (1.35V), pull-down (register based VOUT) or floating (1.2V)	n/a (connect to GND)			
VSYS	13	PWR	Input supply pin for reference system. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor (optionally share this capacitor with PVIN-capacitors).	n/a			
VDD1P8	14	PWR	Internal Reference Voltage: For Internal Use Only. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.	n/a			
AGND	15	GND	Ground pin for Analog GND	n/a			
GPIO	16	I/O	GPO-configuration: General Purpose Open-Drain Output. Configurable in the power-up and power-down-sequence to enable an external rail. GPIO-configuration: Synchronizing I/O. Used to synchronize two or more TPS65215-Q1. The pin is level-sensitive.	Leave floating			
GPO2	17	0	General Purpose Open-Drain Output. Configurable in the power-up and power-down-sequence to enable an external rail.	Leave floating			
nRSTOUT	18	0	Reset-output to SoC. Controlled by sequencer. High in ACTIVE and STBY state.	Leave floating			
NC	19	N/A	No connect: leave floating on PCB.	Leave floating			
NC	20	N/A	No connect: connect to ground on PCB.	Connect to ground			
VLDO2	21	PWR	Output Voltage of LDO2. Nominal output voltage is configured in EEPROM. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.	Leave floating			
PVIN_LDO2	22	PWR	Power Input for LDO2. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor. Voltage on PVIN_LDO2 pin must not exceed voltage on VSYS pin.	Connect to VSYS			
NC	23	N/A	No connect: leave floating on PCB.	Leave floating			
FB_B3	24	I	Feedback Input for Buck3. Connect to Buck3 output filter. Nominal output voltage is configured in EEPROM.	Connect to GND			



**Table 4-1. Pin Functions (continued)** 

Table 4-1. Pin Functions (continued)					
PIN NAME	PIN NO.	TYPE	DESCRIPTION	CONNECTION if not used (output rails must be permanently disabled)	
EN/PB/ VSENSE	25	I	ON-request input. Configured as EN: Device enable pin, high level is ON-request, low-level is OFF-request. Configured as PB: Push-button monitor input. 600ms low-level is an ON-request, 8s low-level is an OFF-request. Configured as VSENSE: Power-fail comparator input. Set sense voltage using a resistor divider connected from the input to the pre-regulator to this pin to ground. Detects rising/falling voltage on pre-regulator and triggers ON- / OFF-request. The pin is edge-sensitive with a wait-time in PB-configuration and deglitch time for EN- and VSENSE-configuration.	n/a (configure as EN and connect to VSYS)	
PVIN_B3	26	PWR	Power Input for BUCK3. Bypass this pin to ground with a 4.7µF or greater ceramic capacitor. Voltage on PVIN_B3 pin must not exceed voltage on VSYS pin.	Connect to VSYS	
LX_B3	27	PWR	Switch Pin for Buck3. Connect one side of the Buck3-inductor to this pin.	Leave floating	
MODE/RESET	28	I	Multi-Function-Pin: Configured as MODE: Connected to SoC or hard- wired pull-up/-down. Forces the Buck-converters into PWM or permits auto-entry in PFM-mode. Configured as RESET: Connected to SoC. Forces a WARM or COLD reset (configurable), WARM reset resetting output voltages to defaults, COLD reset sequencing down all enabled rails and power up again. Polarity is configurable. The pin is level-sensitive for MODE-configuration, edge-sensitive for RESET-configuration.	n/a (tie high or low, dependent on configuration, see 'PWM/PFM and Reset (MODE/RESET)'	
LX_B2	29	PWR	Switch Pin for Buck2. Connect one side of the Buck2-inductor to this pin.	Leave floating	
PVIN_B2	30	PWR	Power Input for BUCK2. Bypass this pin to ground with a 4.7µF or greater ceramic capacitor. Voltage on PVIN_B2 pin must not exceed voltage on VSYS pin.	Connect to VSYS	
MODE/STBY	31	I	Multi-Function-Pin: Configured as MODE: Connected to SoC or hard-wired pull-up/-down. Forces the Buck-converters into PWM or permits auto-entry in PFM-mode. Configured as STBY: Low-power-mode command, disables selected rails. Both functions, MODE and STBY, are able to be combined. The pin is level-sensitive.	n/a (tie high or low, dependent on configuration, see 'PWM/PFM and Low Power Modes (MODE/ STBY)'	
FB_B2	32	1	Feedback Input for Buck2. Connect to Buck2 output filter. Nominal output voltage is configured in EEPROM.	Connect to GND	



# **Table 4-1. Pin Functions (continued)**

PIN NAN	IE PIN NO.	TYPE	DESCRIPTION	CONNECTION if not used (output rails must be permanently disabled)
PGND	PowerPad	GND	Power-Ground. The exposed pad must be connected to a continuous ground plane of the printed circuit board by multiple interconnect vias directly under the TPS65215-Q1 to maximize electrical and thermal conduction.	n/a

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

POS			MIN	MAX	UNIT
1.1.1	Input voltage	VSYS	-0.3	6	V
1.1.2	Input voltage	PVIN_B1, PVIN_B2, PVIN_B3, PVIN_LDO1, PVIN_LDO2	-0.3	6	V
1.1.3	Input voltage vs. VSYS for Bucks	PVIN_B1, PVIN_B2, PVIN_B3 maximum voltage exceeding VSYS		200	mV
1.1.4	Input voltage vs. VSYS for LDOs	PVIN_LDO1, PVIN_LDO2 maximum voltage exceeding VSYS		20	mV
1.1.5	Input voltage	FB_B1, FB_B2, FB_B3	-0.3	6	V
1.1.6	Input voltage	EN/PB/VSENSE, MODE/STBY, MODE/RESET, VSEL_SD/VSEL_DDR	-0.3	6	V
1.2.1	Output voltage	LX_B1, LX_B2, LX_B3	-0.3	PVIN_Bx + 0.3 V, up to 6 V	V
1.2.2	Output voltage	LX_B1, LX_B2, LX_B3 spikes for maximum 10ns	-2	10	V
1.2.3	Output voltage	GPO1, GPO2, GPIO	-0.3	6	V
1.2.4	Output voltage	VLDO1, VLDO2	-0.3	PVIN_LDOx + 0.3 V, up to 6 V	V
1.2.5	Output voltage	VDD1P8	-0.3	2	V
1.2.6	Output voltage	SDA, SCL	-0.3	6	V
1.2.7	Output voltage	nINT, nRSTOUT	-0.3	6	V
1.4.1	Operating junction temperatu	re, T <sub>J</sub>	-40	125	°C
1.4.2	Storage temperature, T <sub>stg</sub>		-40	150	°C

<sup>(1)</sup> Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

# 5.2 ESD Ratings

POS				VALUE	UNIT
2.3	V <sub>(ESD)</sub>	Electrostatic discharge, Human Body Model Automotive	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	٧
2.4	V <sub>(ESD)</sub>	Electrostatic discharge, Charged Device Model, Automotive, Corner pins (1, 8, 9, 16, 17, 24, 25, 32)	Charged device model (CDM), per AEC Q100-011	±750	V
2.5	V <sub>(ESD)</sub>	Electrostatic discharge, Charged Device Model, Automotive, other pins	Charged device model (CDM), per AEC Q100-011	±500	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## **5.3 Recommended Operating Conditions**

POS			MIN	NOM MAX	UNIT
3.1.1	V <sub>VSYS</sub>	Input voltage	2.5 <sup>(1)</sup>	5.5	V
3.1.2	V <sub>PVIN_B1</sub> , V <sub>PVIN_B2</sub> , V <sub>PVIN_B3</sub> V <sub>LX_B1</sub> , V <sub>LX_B2</sub> , V <sub>LX_B3</sub>	BUCKx Pins	2.5	5.5 <sup>(2)</sup>	V

# **5.3 Recommended Operating Conditions (continued)**

over operating free-air temperature range (unless otherwise noted)

POS			MIN	NOM	MAX	UNIT
3.1.3	ΔV <sub>VSYS_PVIN_Bx</sub>	Voltage differential from V <sub>PVIN_Bx</sub> to V <sub>VSYS</sub>			0	mV
3.1.4	ΔV <sub>VSYS_PVIN_LDO1</sub>	Voltage differential from V <sub>PVIN_LDO1</sub> to V <sub>VSYS</sub>			0	mV
3.1.5	ΔV <sub>VSYS_VLDO2</sub>	Voltage by which $V_{VSYS}$ must exceed LDO output voltage (VLDO2); $V_{VSYS}$ = 2.5V to 3.45V; LDO mode	150			mV
3.1.6	$\Delta V_{VSYS\_VLDO2}$	Voltage by which $V_{VSYS}$ must exceed LDO output voltage (VLDO2); $V_{VSYS}$ = 3.45V to 5.5V in LDO-mode or $V_{VSYS}$ = 2.5V to 5.5V in LSW-mode	n/a			mV
3.1.7	C <sub>PVIN_B1</sub> , C <sub>PVIN_B2</sub> , C <sub>PVIN_B3</sub>	BUCKx Input Capacitance	3.9	4.7		μF
3.1.8	L <sub>B1</sub> , L <sub>B2</sub> , L <sub>B3</sub>	BUCKx Output Inductance	330	470	611	nH
3.1.9a	C <sub>OUT_B1</sub> , C <sub>OUT_B2</sub> , C <sub>OUT_B3</sub>	BUCKx Output Capacitance, forced PWM or auto-PFM, low bandwidth case	10		75	μF
3.1.9b	C <sub>OUT_B1</sub> , C <sub>OUT_B2</sub> , C <sub>OUT_B3</sub>	BUCKx Output Capacitance, fixed frequency, low BW case	12		36	μF
3.1.10a	C <sub>OUT_B1</sub> , C <sub>OUT_B2</sub> , C <sub>OUT_B3</sub>	BUCKx Output Capacitance, forced PWM or auto-PFM, high bandwidth case	30		220	μF
3.1.10b	C <sub>OUT_B1</sub> , C <sub>OUT_B2</sub> , C <sub>OUT_B3</sub>	BUCKx Output Capacitance, fixed frequency, high BW case	48		144	μF
3.1.11	V <sub>FB_B1</sub> , V <sub>FB_B2</sub> , V <sub>FB_B3</sub>	BUCKx FB Pins	0		5.5 <sup>(2)</sup>	V
3.1.12	V <sub>PVIN_LDO1</sub>	LDO Input Voltage	1.5		5.5 <sup>(2)</sup>	V
3.1.13	V <sub>PVIN_LDO1</sub>	LDO Input Voltage in bypass mode	1.5		3.6	V
3.1.14	V <sub>PVIN_LDO1</sub>	Allowable delta between V <sub>PVIN_LDOx</sub> and configured V <sub>VLDOx</sub> in bypass mode	-200		200	mV
3.1.15	V <sub>VLDO1</sub>	LDO Output Voltage Range	0.6		3.4	V
3.1.16	C <sub>PVIN_LDO1</sub> , C <sub>PVIN_LDO2</sub>	LDO Input Capacitance	1.6	2.2		μF
3.1.17	C <sub>VLDO1</sub>	LDO Output Capacitance	1.6	2.2	20	μF
3.1.18	V <sub>PVIN_LDO2</sub>	LDO Input Voltage	2.2		5.5 <sup>(2)</sup>	V
3.1.19	V <sub>VLDO2</sub>	LDO Output Voltage Range	1.2		3.3	V
3.1.21	C <sub>VLDO2</sub>	LDO Output Capacitance	1.6	2.2	30 (3)	μF
3.1.22	V <sub>VDD1P8</sub>	VDD1P8 pin	0		1.8	V
3.1.23	C <sub>VDD1P8</sub>	Internal Regulator Decoupling Capacitance	1	2.2	4	μF
3.1.24	C <sub>VSYS</sub>	VSYS Input Decoupling Capacitance	1	2.2		μF
3.1.25	V <sub>nINT</sub> , V <sub>nRSTOUT</sub>	Digital Outputs	0		3.4	V
3.1.26	V <sub>GPO1</sub> , V <sub>GPO2</sub> , V <sub>GPIO</sub>	Digital Outputs	0		5.5 <sup>(2)</sup>	V
3.1.27	V <sub>SCL</sub> , V <sub>SDA</sub>	I2C Interface	0		3.4	V
3.1.28	V <sub>EN/PB/VSENSE</sub> , V <sub>MODE/STBY</sub> , V <sub>MODE/RESET</sub> , V <sub>VSEL_SD/VSEL/DDR</sub>	Digital Inputs	0		5.5 <sup>(2)</sup>	V
3.2.1	tvsys_ramp_rise	Input voltage rising ramp Time, Input voltage controlled by a pre-regulator. V <sub>VSYS</sub> = V <sub>PVIN_Bx</sub> = V <sub>PVIN_LDOx</sub> = 0V to 5V	0.1		600000	ms
3.2.2	t <sub>VSYS_RAMP_FALL</sub>	Input voltage falling Ramp Time, V <sub>VSYS</sub> = V <sub>PVIN_Bx</sub> = V <sub>PVIN_LDOx</sub> = 5V to 2.5V	0.4		600000	ms
3.3.1	T <sub>A</sub> _	Operating free-air temperature	-40		125	°C
3.3.2	T <sub>J_</sub>	Operating junction temperature	-40		150	°C

(1) For EEPROM programming, VSYS(min)=3.3V



- Must not exceed VSYS
- In slow-ramp-mode. Fast-ramp supports 15µF maximum (3)

#### **5.4 Thermal Information**

		TPS65215-Q1	
	THERMAL METRIC(1)	RHB (QFN)	UNIT
		32 PINS	
R <sub>OJA</sub>	Junction-to-ambient thermal resistance	31.3	°C/W
R <sub>ΘJC(top)</sub>	Junction-to-case (top) thermal resistance	20.4	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	10.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	10.8	°C/W
R <sub>OJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.8	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

# 5.5 System Control Thresholds

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the AGND ground of the device.

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electric	al Characteristics	<b>.</b>					
4.1.1	VSYS	Operating Input Voltage		2.5		5.5	V
4.1.2	VSYS <sub>POR_Rising</sub>	VSYS POR rising threshold	Measured on VSYS pin, untrimmed	2.2		2.5	V
4.1.3	VSYS <sub>UVLO_Falling</sub>	VSYS UVLO falling threshold	Measured on VSYS pin, trimmed	2.175		2.25	V
4.1.4	VSYS <sub>POR_Hyst</sub>	VSYS UVLO/POR hysteresis	VSYS <sub>POR_Rising_untrimmed</sub> - VSYS <sub>UVLO_Falling_trimmed</sub>		130		mV
4.1.5	V <sub>VSYS_OVP_Rise</sub>	VSYS OVP rising threshold, trimmed	Measured on VSYS pin, trimmed	5.9		6.1	V
4.1.6	V <sub>VSYS_OVP_Fall</sub>	VSYS OVP falling threshold, trimmed	Measured on VSYS pin, trimmed	5.7		5.95	V
4.1.7	V <sub>VSYS_OVP_Hyst</sub>	VSYS OVP hysteresis	VSYS <sub>OVP_Rising_trimmed</sub> VSYS <sub>OVP_falling_trimmed</sub>	100	140	180	mV
4.1.8	V <sub>VDD1P8</sub>	VDD1P8 voltage		1.7	1.8	1.9	V
4.2.1a	I <sub>INITIALIZE</sub>	Current Consumption in INITIALIZE state, at 25°C	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. All Monitors are off. T <sub>J</sub> = 25°C		15	22	μΑ
4.2.1b	I <sub>INITIALIZE</sub>	Current Consumption in INITIALIZE state, -40°C to 150°C	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. All Monitors are off.  T <sub>J</sub> = -40°C to 150°C		15	37	μΑ
4.2.2a	I <sub>ACTIVE</sub>	ACTIVE State Current Consumption, all rails on, at 25°C	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. T <sub>J</sub> = 25°C		175	200	μΑ
4.2.2b	I <sub>ACTIVE</sub>	ACTIVE State Current Consumption, all rails on, -40°C to 150°C	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. T <sub>J</sub> = -40°C to 150°C		175	400	μΑ



# 5.5 System Control Thresholds (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the AGND ground of the device.

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.2.3a	І <sub>ЅТВУ</sub>	STBY State Current Consumption, only LDO1 on, at 25°C	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. Only LDO1 on in LDO-mode. No Load. $T_J = 25^{\circ}C$		105	125	μΑ
4.2.3b	І <sub>ЅТВУ</sub>	STBY State Current Consumption, only LDO1 on, -40°C to 150°C	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. Only LDO1 on in LDO-mode. No Load. T <sub>J</sub> = -40°C to 150°C		105	150	μΑ
4.2.4a	І <sub>ЅТВҮ</sub>	STBY State Current Consumption, all rails on, VMON on at 25°C	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. Output-voltage Monitors are on, VSYS-monitor (UV/OVP) are on. T <sub>J</sub> = 25°C		175	200	μΑ
4.2.4b	І <sub>ЅТВҮ</sub>	STBY State Current Consumption, all rails on, VMON on, -40°C to 150°C	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. All Outputs are on, all LDOs in LDO-mo, Bucks in PFM mode. No Load. Output-voltage Monitors are on, VSYS-monitor (UV/OVP) are on. T <sub>J</sub> = -40°C to 150°C		175	400	μΑ
Timing	Requirements						
4.3.1	toff_to_init	Time from VSYS passing VSYS_POR until entering INITIALIZE state, including EEPROM-read, ready for ON- request	Time from VSYS passing VSYS_POR until entering INITIALIZE state. On request execution gated by HOT and RV			3.2	ms
4.3.2a	tтімеоит_uv	UV-detection in case a rail does not reach UV-threshold during ramp-up				end of t <sub>RAMP</sub> + sample- and deglitch time	
4.3.2b	t <sub>TIMEOUT_UV_</sub> SLOT	Timeout in case a rail does not reach UV-threshold during ramp-up, applicable in Multi-PMIC- configuration only				end of slot- extensi on time (3ms, 4ms or 13ms)	
4.3.3	t <sub>TIMEOUT_Discharge</sub>	Timeout in case a rail cannot be discharged when transitioning from STBY to ACTIVE state		72	80	88	ms

## 5.6 BUCK1 Converter

over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
Electrica	al Characteristics					
5.1.1a	V <sub>IN_BUCK1</sub>	Input voltage <sup>(1)</sup>	Buck supply voltage, maximum VSYS	2.5	5.5	V

Product Folder Links: TPS65215-Q1



POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.1.1b	V <sub>OUT_ВИСК1</sub>	Buck Output Voltage configurable Range	Output voltage configurable in 25mV-steps for $0.6V \le V_{OUT} \le 1.4V$ , in 100mV steps for $1.4V < V_{OUT} \le 3.4V$	0.6		3.4	V
5.1.2a	I <sub>Q_BUCK1</sub>	Quiescent Current at 25°C, PFM, low BW case	PFM, BUCK1 enabled, no load, V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, T <sub>J</sub> =25°C		10	13	μΑ
5.1.2b	I <sub>Q_BUCK1</sub>	Quiescent Current -40°C to 125°C, PFM, low BW case	PFM, BUCK1 enabled, no load, V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, T <sub>J</sub> =-40°C to 125°C		15	44	μA
5.1.2c	I <sub>Q_BUCK1</sub>	Quiescent Current -40°C to 150°C, PFM, low BW case	PFM, BUCK1 enabled, no load, V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, T <sub>J</sub> =-40°C to 150°C		20	63	μA
5.1.3a	V <sub>HEADROOM_PWM</sub>	Input to Output Voltage Headroom <sup>(2)</sup>	Corner cases at maximum load I <sub>OUT</sub> = 2.5A	500			mV
5.1.3b	V <sub>HEADROOM_PWM</sub>	Input to Output Voltage Headroom at I <sub>OUT</sub> = I <sub>OUT_MAX</sub> (2)	Corner cases at I <sub>OUT</sub> = I <sub>OUT_MAX</sub>	700			mV
5.1.3c	V <sub>HEADROOM_FF</sub>	Input to Output Voltage Headroom <sup>(2)</sup>	Corner cases at maximum load I <sub>OUT</sub> = 0.7A	500			mV
5.1.3d	V <sub>HEADROOM_FF</sub>	Input to Output Voltage Headroom at I <sub>OUT</sub> = I <sub>OUT_MAX</sub> (2)	Corner cases at I <sub>OUT</sub> = I <sub>OUT_MAX</sub>	1000			mV
5.1.4	V <sub>OUT_STEP_LOW</sub>	Output voltage Steps	$0.6V \le V_{OUT} \le 1.4V$		25		mV
5.1.5	V <sub>OUT_STEP_HIGH</sub>	Output voltage Steps	1.5V ≤ V <sub>OUT</sub> ≤ 3.4V		100		mV
5.1.6a	VOUT_ACC_DC_PW	DC Output Voltage Accuracy in forced PWM mode, low and high BW case	$I_{OUT} = I_{OUT\_MAX},$ $V_{OUT} \ge 0.7 \overline{V}$ to 3.4V, $V_{IN} - V_{OUT} > 700 \text{ mV}$ forced PWM, low BW case	-1.5%		1.5%	
5.1.6b	VOUT_ACC_DC_PW	DC Output Voltage Accuracy in forced PWM mode, low and high BW case	$\begin{split} I_{OUT} &= I_{OUT\_MAX}, \\ V_{OUT} &= 0.6 \text{V to } 0.7 \text{V}, \\ V_{\text{IN}} &- V_{OUT} > 700 \text{ mV} \\ \text{forced PWM, low BW case} \end{split}$	-10		10	mV
5.1.6c	Vout_acc_dc_pfm	DC Output Voltage Accuracy in auto-PFM mode, low and high BW case	$I_{OUT}$ = 1mA, $V_{OUT}$ = 0.6V to 3.4V, $V_{IN}$ - $V_{OUT}$ > 500 mV auto-PFM, low BW case	-3.0%		3.5%	
5.1.6d	Vout_acc_dc_ff	DC Output Voltage Accuracy in Fixed Frequency mode, low and high BW case	$I_{OUT} = I_{OUT\_MAX},$ $V_{OUT} \ge 0.7 \overline{V}$ to 3.4V, $V_{IN} - V_{OUT} > 1000 \text{ mV}$ fixed frequency, low BW case	-1.5%		1.5%	
5.1.6e	Vout_acc_dc_ff	DC Output Voltage Accuracy in Fixed Frequency mode, low and high BW case	$\begin{split} I_{OUT} &= I_{OUT\_MAX}, \\ V_{OUT} &= 0.6 \text{V to } 0.7 \text{V}, \\ V_{\text{IN}} - V_{OUT} &> 1000 \text{ mV} \\ \text{fixed frequency, low BW case} \end{split}$	-10		10	mV
5.1.7	R <sub>FB_INPUT</sub>	Feedback input impedance	Converter enabled	2.3	3.75	5.0	МΩ
5.2.1a	V <sub>LOAD_REG_PWM</sub>	DC Load Regulation, forced PWM, low BW case	$V_{\text{IN}}$ = 5.0V, $V_{\text{OUT}}$ = 1.2V, $I_{\text{OUT}}$ = 0 to $I_{\text{OUT\_MAX}}$ , forced PWM, low BW case, $C_{\text{OUT}}$ = 40 $\mu$ F		0.1	0.16	%/A
5.2.1b	VLOAD_REG_FF	DC Load Regulation, fixed frequency, low BW case	$V_{\text{IN}}$ = 5.0V, $V_{\text{OUT}}$ = 1.2V, $I_{\text{OUT}}$ = 0 to $I_{\text{OUT\_MAX}}$ , fixed frequency, low BW case, $C_{\text{OUT}}$ = 40 $\mu\text{F}$		0.1	0.16	%/A



over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.2.2a	V <sub>LINE_REG</sub>	DC Line Regulation, forced PWM, low BW case	$\begin{aligned} &V_{IN}=3.3V \text{ to } 5.5V,\\ &V_{OUT}=1.2V,\\ &I_{OUT}=1\text{mA and }I_{OUT\_MAX}\\ &\text{forced PWM, low BW case, }C_{OUT}=\\ &40\mu\text{F} \end{aligned}$		0.1	0.16	%/V
5.2.2b	V <sub>LINE_REG</sub>	DC Line Regulation, fixed frequency, low BW case	$\begin{split} &V_{IN}=3.3V \text{ to } 5.5V,\\ &V_{OUT}=1.2V,\\ &I_{OUT}=1\text{mA and }I_{OUT\_MAX}\\ &\text{fixed frequency, low $\overline{B}$W case, $C_{OUT}$}\\ &=12\mu F \end{split}$		0.1	0.16	%/V
5.2.3a	V <sub>LOAD_</sub> TRANSIENT	Load Transient, V <sub>OUT</sub> =0.75V, auto-PFM, high BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V, } V_{\text{OUT}} = 0.75\text{V,} \\ &I_{\text{OUT}} = 100\text{mA to } 1100\text{mA to } 100\text{mA,} \\ &t_{\text{R}} = t_{\text{F}} = 500\text{ns,} \\ &\text{auto-PFM, high BW case, } C_{\text{OUT}} = \\ &80\mu\text{F} \end{aligned}$	-27.5		27.5	mV
5.2.3b	V <sub>LOAD_</sub> TRANSIENT	Load Transient, V <sub>OUT</sub> =0.75V, forced PWM, high BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V},  V_{\text{OUT}} = 0.75\text{V}, \\ &I_{\text{OUT}} = 100\text{mA to } 1100\text{mA to } 100\text{mA}, \\ &t_{\text{R}} = t_{\text{F}} = 500\text{ns}, \\ &\text{forced PWM, high BW case, } C_{\text{OUT}} = \\ &80 \; \mu\text{F} \end{aligned}$	-27.5		27.5	mV
5.2.3c	V <sub>LOAD_</sub> TRANSIENT	Load Transient, V <sub>OUT</sub> =0.75V, fixed frequency, high BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V},  V_{\text{OUT}} = 0.75\text{V}, \\ &I_{\text{OUT}} = I_{\text{OUT}} = 100\text{mA to } 1100\text{mA to} \\ &100\text{mA}, \\ &I_{\text{R}} = I_{\text{F}} = 500\text{ns}, \\ &\text{fixed frequency, high BW case,} \\ &C_{\text{OUT}} = 60 \; \mu\text{F} \end{aligned}$	-27.5		27.5	mV
5.2.4a	VLOAD_TRANSIENT	Load Transient, V <sub>OUT</sub> =1.8V, auto- PFM, low BW case	$V_{IN} = 5.0V, V_{OUT} = 1.8V, \\ I_{OUT} = 1 mA to 1A to 1 mA, \\ t_R = t_F = 1 \mu s, \\ auto-PFM, C_{OUT} = 40 \mu F$	-90		90	mV
5.2.4b	VLOAD_TRANSIENT	Load Transient, V <sub>OUT</sub> =1.8V, forced PWM, low BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V, } V_{\text{OUT}} = 1.8\text{V,} \\ &I_{\text{OUT}} = 1\text{mA to 1A to 1mA,} \\ &I_{\text{R}} = I_{\text{F}} = 1\mu\text{s,} \\ &\text{forced PWM, } C_{\text{OUT}} = 40\mu\text{F} \end{aligned}$	-60		60	mV
5.2.4c	VLOAD_TRANSIENT	Load Transient, V <sub>OUT</sub> =1.8V, fixed frequency, low BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V},  V_{\text{OUT}} = 1.8\text{V}, \\ &I_{\text{OUT}} = 1\text{mA to 1A to 1mA}, \\ &t_{\text{R}} = t_{\text{F}} = 1\mu\text{s}, \\ &\text{fixed frequency, low BW case, } C_{\text{OUT}} \\ &= 12\mu\text{F} \end{aligned}$	-180		180	mV
5.2.5a	V <sub>LINE_TRANSIENT</sub>	Line Transient, V <sub>OUT</sub> =1.2V, forced PWM, low BW case	$V_{\text{IN}}$ = 3.3V to 5.5V in 50µs, $V_{\text{OUT}}$ = 1.2V, $I_{\text{OUT}}$ = 1mA and $I_{\text{OUT\_MAX}}$ , forced PWM, low BW case, $C_{\text{OUT}}$ = $40\mu\text{F}$	<b>–</b> 50		50	mV
5.2.5b	V <sub>LINE_</sub> TRANSIENT	Line Transient, V <sub>OUT</sub> =1.2V, fixed frequency, low BW case	$V_{IN}$ = 3.3V to 5.5V in 50µs, $V_{OUT}$ = 1.2V, $I_{OUT}$ = 1mA and $I_{OUT\_MAX}$ , fixed frequency, low BW case, $C_{OUT}$ = 12µF	-50		50	mV
5.2.6a	V <sub>RIPPLE_PP_PWM</sub>	Forced PWM Mode, low BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V, } V_{\text{OUT}} = 2.5\text{V,} \\ &\text{forced PWM, low BW case, } C_{\text{OUT}} = \\ &40\text{uF, X5R, ESR} = 10\text{mOhm,} \\ &L = 470\text{nH, DCR} = 50\text{m}\Omega \\ &I_{\text{OUT}} = 1\text{A} \end{aligned}$		10	20	$mV_PP$

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated



POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.2.6b	V <sub>RIPPLE_PP_PFM</sub>	Auto PFM Mode, low BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V, } V_{\text{OUT}} = 2.5\text{V,} \\ &\text{auto PFM, low BW case, } C_{\text{OUT}} = \\ &40\text{uF, X5R, ESR} = 10\text{mOhm,} \\ &L = 470\text{nH, DCR} = 50\text{m}\Omega \\ &I_{\text{OUT}} = 20\text{mA} \end{aligned}$		20	40	mV <sub>PP</sub>
5.2.6c	VRIPPLE_PP_FF	Fixed Frequency Mode, low BW case, spread spectrum disabled	$\begin{split} &V_{\text{IN}} = 5.0\text{V},  V_{\text{OUT}} = 2.5\text{V}, \\ &\text{fixed frequency, low BW case, } C_{\text{OUT}} \\ &= 12\text{uF, X5R, ESR} = 10\text{mOhm,} \\ &\text{L} = 470\text{nH, DCR} = 50\text{m}\Omega, \\ &\text{I}_{\text{OUT}} = 1\text{A}, \\ &\text{Spread-Spectrum disabled} \end{split}$		10	20	mV <sub>PP</sub>
5.2.6d	VRIPPLE_PP_FF_SS	Fixed Frequency Mode, low BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V}, V_{\text{OUT}} = 2.5\text{V}, \\ &\text{fixed frequency, low BW case, } C_{\text{OUT}} \\ &= 12\text{uF, X5R, ESR} = 10\text{mOhm,} \\ &\text{L} = 470\text{nH, DCR} = 50\text{m}\Omega, \\ &\text{I}_{\text{OUT}} = 1\text{A,} \\ &\text{Spread-Spectrum enabled} \end{aligned}$		20	40	mV <sub>PP</sub>
5.3.1	I <sub>OUT_MAX</sub>	Maximum Operating Current				3.5	Α
5.3.2	I <sub>CURRENT_LIMIT</sub>	Peak Current Limit	V <sub>IN</sub> = 2.5V to 5.5V	4.6	5.7	6.9	Α
5.3.3	I <sub>REV_CUR_LIMIT</sub>	Reverse Peak Current Limit	V <sub>IN</sub> = 2.5V to 5.5V	-2.0	-1.5	-1.0	Α
5.3.4a	R <sub>DSON_HS</sub>	High Side MOSFET On Resistance, 5V-supply	Measured Pin to Pin, V <sub>IN</sub> = 5V			70	mΩ
5.3.4b	R <sub>DSON_HS</sub>	High Side MOSFET On Resistance, 3.3V-supply	Measured Pin to Pin, V <sub>IN</sub> = 3.3V			80	mΩ
5.3.5a	R <sub>DSON_LS</sub>	Low Side MOSFET On Resistance, 5V-supply	Measured Pin to Pin, V <sub>IN</sub> = 5V			40	mΩ
5.3.5b	R <sub>DSON_LS</sub>	Low Side MOSFET On Resistance, 3.3V-supply	Measured Pin to Pin, V <sub>IN</sub> = 3.3V		·	50	mΩ
5.3.6	R <sub>DISCHARGE</sub>	Output Discharge Resistance	Active only when converter is disabled	60	125	200	Ω
5.4.1	L <sub>SW</sub>	Output Inductance	DCR = 50mΩ max	330	470	611	nH
5.4.2a	C <sub>OUT</sub>	Output Capacitance in auto-PFM or forced PWM for low BW case	ESR = 10mΩ max	10		75	μF
5.4.2b	C <sub>OUT_FF</sub>	Output Capacitance in fixed frequency for low BW case	ESR = 10mΩ max	12		36	μF
5.4.3a	C <sub>OUT_HIGH_BW</sub>	Output Capacitance in auto-PFM or forced PWM for high BW case	ESR = 10mΩ max	30		220	μF
5.4.3b	C <sub>OUT_HIGH_BW_FF</sub>	Output Capacitance in fixed frequency for high BW case	ESR = 10mΩ max	48		144	μF
Timing	Requirements						
5.5.1	t <sub>RAMP</sub>	Ramp Time in forced PWM, low BW case	Time from enable to 98% of target value, assuming no residual voltage	0.3		1.65	ms
5.5.2a	DVFS_RISE_ QFF	DVFS timing requirements in forced PWM, rising slope	Step-duration during DVFS voltage adjustments from 0.6V to 1.4V	2.9	3.2	3.5	mV/μs
5.5.2b	DVFS_RISE_ FF	DVFS timing requirements in fixed-frequency mode, rising slope	Step-duration during DVFS voltage adjustments from 0.6V to 1.4V	1.8	2.1	2.5	mV/μs
5.5.2c	DVFS_FALL	DVFS timing requirements in forced PWM or fixed-frequency mode, falling slope	Step-duration during DVFS voltage adjustments from 1.4V to 0.6V	0.45	0.53	0.61	mV/μs
Switchi	ng Characteristics	<b>.</b>					
5.6.1a	f <sub>SW</sub>	Switching Frequency, forced PWM, high or low BW case	Forced PWM, V <sub>IN</sub> = 3.3V to 5V, V <sub>OUT</sub> = 0.8V to 1.8V, I <sub>OUT</sub> = 1A to 3A		2.3		MHz



over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.6.1b	f <sub>SW</sub>		Fixed - Frequency, $V_{IN}$ = 3.3V to 5V, $V_{OUT}$ = 0.8V to 1.8V, $I_{OUT}$ = 1A to 3A	2.18	2.3	2.42	MHz
5.6.2	fsw_ss_en	Switching Frequency, fixed frequency, high or low BW case, with Spread Spectrum enabled	Fixed - Frequency, $V_{\rm IN}$ = 3.3V to 5V, $V_{\rm OUT}$ = 0.8V to 1.8V, $I_{\rm OUT}$ = 1A to 3A Spread spectrum enabled	1.95		2.65	MHz

<sup>(1)</sup> PVIN\_Bx must not exceed VSYS

# 5.7 BUCK2, BUCK3 Converter

over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electric	al Characteristics						
6.1.1a	V <sub>IN_BUCK23</sub>	Input Voltage <sup>(1)</sup>	Buck supply voltage, maximum VSYS	2.5		5.5	V
6.1.1b	V <sub>OUT_ВИСК23</sub>	Buck Output Voltage configurable Range	Output voltage configurable in 25mV-steps for 0.6V ≤ V <sub>OUT</sub> ≤ 1.4V, in 100mV steps for 1.4V < V <sub>OUT</sub> ≤ 3.4V	0.6		3.4	V
6.1.2a	I <sub>Q_BUCK23</sub>	Quiescent Current at 25°C, PFM	PFM, BUCKx enabled, no load, V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, T <sub>J</sub> =25°C		10	13	μΑ
6.1.2b	I <sub>Q_BUCK23</sub>	Quiescent Current -40°C to 125°C, PFM, low BW case	PFM, BUCKx enabled, no load, V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, T <sub>J</sub> =-40°C to 125°C		15	43	μA
6.1.2c	I <sub>Q_BUCK23</sub>	Quiescent Current -40°C to 150°C, PFM, low BW case	PFM, BUCKx enabled, no load, V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, T <sub>J</sub> =-40°C to 150°C		20	63	μA
6.1.3a	V <sub>HEADROOM_PWM</sub>	Input to Output Voltage Headroom <sup>(2)</sup>	Corner cases at maximum load I <sub>OUT</sub> = 85% of I <sub>OUT_MAX</sub>	500			mV
6.1.3b	V <sub>HEADROOM_PWM</sub>	Input to Output Voltage Headroom at I <sub>OUT</sub> = I <sub>OUT_MAX</sub> (2)	Corner cases at I <sub>OUT</sub> = I <sub>OUT_MAX</sub>	700			mV
6.1.3c	V <sub>HEADROOM_FF</sub>	Input to Output Voltage Headroom <sup>(2)</sup>	Corner cases at maximum load I <sub>OUT</sub> = 0.5A	500			mV
6.1.3d	V <sub>HEADROOM_FF</sub>	Input to Output Voltage Headroom at I <sub>OUT</sub> = I <sub>OUT_MAX</sub> (2)	Corner cases at I <sub>OUT</sub> = I <sub>OUT_MAX</sub>	1000			mV
6.1.4	V <sub>OUT_STEP_LOW</sub>	Output voltage Steps Buck2 and Buck3	0.6V ≤ V <sub>OUT</sub> ≤ 1.4V		25		mV
6.1.5	V <sub>OUT_STEP_HIGH</sub>	Output voltage Steps Buck2, Buck3	1.5V ≤ V <sub>OUT</sub> ≤ 3.4V		100		mV
6.1.6a	VOUT_ACC_DC_PW	DC Output Voltage Accuracy in forced PWM mode, low and high BW case	$\begin{split} &I_{OUT} = I_{OUT\_MAX}, \\ &V_{OUT} \ge 0.7 \text{V to } 3.4 \text{V}, \\ &V_{\text{IN}} - V_{OUT} > 700 \text{ mV} \\ &\text{forced PWM, low BW case} \end{split}$	-1.5%		1.5%	
6.1.6b	VOUT_ACC_DC_PW	DC Output Voltage Accuracy in forced PWM mode, low and high BW case	$\begin{split} I_{OUT} &= I_{OUT\_MAX}, \\ V_{OUT} &= 0.6 \text{V to } 0.7 \text{V}, \\ V_{\text{IN}} &- V_{OUT} > 700 \text{ mV} \\ \text{forced PWM, low BW case} \end{split}$	-10		10	mV
6.1.6c	V <sub>OUT_ACC_DC_PFM</sub>	DC Output Voltage Accuracy in auto-PFM mode, low and high BW case	$I_{OUT}$ = 1mA, $V_{OUT}$ = 0.6V to 3.4V, $V_{IN}$ - $V_{OUT}$ > 500 mV auto-PFM, low BW case	-3.0%		3.5%	

Product Folder Links: TPS65215-Q1

Refers to DC-regulation only. Transient response typically improves with more headroom. With low headroom, the frequency variation increases for quasi-fixed frequency.



# 5.7 BUCK2, BUCK3 Converter (continued)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.1.6d	Vout_ACC_DC_FF	DC Output Voltage Accuracy in Fixed Frequency mode, low and high BW case	$I_{OUT} = I_{OUT\_MAX}$ , $V_{OUT} \ge 0.7V$ to 3.4V, $V_{IN} - V_{OUT} > 1000$ mV fixed frequency, low BW case	-1.5%		1.5%	
6.1.6e	Vout_acc_dc_ff	DC Output Voltage Accuracy in Fixed Frequency mode, low and high BW case	$\begin{split} I_{OUT} &= I_{OUT\_MAX}, \\ V_{OUT} &= 0.6 \overline{V} \text{ to } 0.7 V, \\ V_{IN} - V_{OUT} &> 1000 \text{ mV} \\ \text{fixed frequency, low BW case} \end{split}$	-10		10	mV
6.1.9	R <sub>FB_INPUT</sub>	Feedback input impedance	Converter enabled	2.3	3.75	5.0	МΩ
6.2.1a	V <sub>LOAD_REG_PWM</sub>	DC Load Regulation, forced PWM, low BW case	$V_{\text{IN}}$ = 5.0V, $V_{\text{OUT}}$ = 1.2V, $I_{\text{OUT}}$ = 0 to $I_{\text{OUT\_MAX}}$ , forced PWM, low BW case		0.1	0.16	%/A
6.2.1b	VLOAD_REG_FF	DC Load Regulation, fixed frequency, low BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V, } V_{\text{OUT}} = 1.2\text{V,} \\ &I_{\text{OUT}} = 0 \text{ to } I_{\text{OUT\_MAX,}} \\ &\text{fixed frequency, low BW case, } C_{\text{OUT}} \\ &= 40\mu\text{F} \end{aligned}$		0.1	0.16	%/A
6.2.2a	V <sub>LINE_REG</sub>	DC Line Regulation, forced PWM, low BW case	$\begin{array}{l} V_{IN}=3.3V~to~5.5V,\\ V_{OUT}=1.2V,\\ I_{OUT}=1mA~and~I_{OUT~MAX}\\ forced~PWM,~low~BW~case,~C_{OUT}=\\ 40\mu F \end{array}$		0.1	0.16	%/V
6.2.2b	V <sub>LINE_REG</sub>	DC Line Regulation, fixed frequency, low BW case	$V_{IN}$ = 3.3V to 5.5V, $V_{OUT}$ = 1.2V, $I_{OUT}$ = 1mA and $I_{OUT\_MAX}$ fixed frequency, low $\overline{B}W$ case, $C_{OUT}$ = 12 $\mu F$		0.1	0.16	%/V
6.2.3a	V <sub>LOAD_</sub> TRANSIENT	Load Transient, V <sub>OUT</sub> =0.75V, auto-PFM, high BW case	$\begin{aligned} &V_{IN} = 5.0V,  V_{OUT} = 0.75V, \\ &I_{OUT} = 100mA \text{ to } 750mA \text{ to } 100mA, \\ &t_R = t_F = 500ns, \\ &auto\text{-PFM},  high BW case,  C_{OUT} = \\ &80\muF \end{aligned}$	-27.5		27.5	mV
6.2.3b	VLOAD_TRANSIENT	Load Transient, V <sub>OUT</sub> =0.75V, forced PWM, high BW case	$\begin{array}{l} V_{\text{IN}} = 5.0\text{V}, V_{\text{OUT}} = 0.75\text{V}, \\ I_{\text{OUT}} = 100\text{mA to }750\text{mA to }100\text{mA}, \\ t_{\text{R}} = t_{\text{F}} = 500\text{ns}, \\ \text{forced PWM, high BW case, } C_{\text{OUT}} = \\ 80~\mu\text{F} \end{array}$	-27.5		27.5	mV
6.2.3c	V <sub>LOAD_</sub> TRANSIENT	Load Transient, V <sub>OUT</sub> =0.75V, fixed frequency, high BW case	$ \begin{vmatrix} V_{\text{IN}} = 5.0\text{V}, V_{\text{OUT}} = 0.75\text{V}, \\ I_{\text{OUT}} = 100\text{mA to } 750\text{mA to } 100\text{mA}, \\ t_{\text{R}} = t_{\text{F}} = 500\text{ns}, \\ \text{fixed frequency, high BW case,} \\ C_{\text{OUT}} = 60~\mu\text{F} $	-27.5		27.5	mV
6.2.4a	VLOAD_TRANSIENT	Load Transient, V <sub>OUT</sub> =1.8V, auto- PFM, low BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V, } V_{\text{OUT}} = 1.8\text{V,} \\ &I_{\text{OUT}} = 1\text{mA to 1A to 1mA,} \\ &t_{\text{R}} = t_{\text{F}} = 1\mu\text{s,} \\ &\text{auto-PFM, } C_{\text{OUT}} = 40\mu\text{F} \end{aligned}$	-90		90	mV
6.2.4b	VLOAD_TRANSIENT	Load Transient, V <sub>OUT</sub> =1.8V, forced PWM, low BW case	$V_{\text{IN}}$ = 5.0V, $V_{\text{OUT}}$ = 1.8V, $I_{\text{OUT}}$ = 1mA to 1A to 1mA, $t_{\text{R}}$ = $t_{\text{F}}$ = 1 $\mu$ s, forced PWM, $C_{\text{OUT}}$ = 40 $\mu$ F	-60		60	mV
6.2.4c	V <sub>LOAD_TRANSIENT</sub>	Load Transient, V <sub>OUT</sub> =1.8V, fixed frequency, low BW case	$V_{IN}$ = 5.0V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 1mA to 1A to 1mA, $t_R$ = $t_F$ = 1 $\mu$ s, fixed frequency, low BW case, $C_{OUT}$ = 12 $\mu$ F	-180		180	mV



# 5.7 BUCK2, BUCK3 Converter (continued)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.2.5a	V <sub>LINE_</sub> TRANSIENT	Line Transient, V <sub>OUT</sub> =1.2V, forced PWM, low BW case	$V_{IN}$ = 3.3V to 5.5V in 50μs, $V_{OUT}$ = 1.2V, $I_{OUT}$ = 1mA and $I_{OUT\_MAX}$ , forced PWM, low BW case, $C_{OUT}$ = 40μF	-50		50	mV
6.2.5b	V <sub>LINE_</sub> TRANSIENT	Line Transient, V <sub>OUT</sub> =1.2V, fixed frequency, low BW case	$V_{IN}$ = 3.3V to 5.5V in 50µs, $V_{OUT}$ = 1.2V, $I_{OUT}$ = 1mA and $I_{OUT\_MAX}$ , fixed frequency, low BW case, $C_{OUT}$ = 12µF	<b>–</b> 50		50	mV
6.2.6a	V <sub>RIPPLE_PP_PWM</sub>	Forced PWM Mode, low BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V},  V_{\text{OUT}} = 2.5\text{V}, \\ &\text{forced PWM, low BW case, } C_{\text{OUT}} = \\ &40\text{uF, X5R, ESR} = 10\text{mOhm,} \\ &\text{L} = 470\text{nH, DCR} = 50\text{m}\Omega \\ &\text{I}_{\text{OUT}} = 1\text{A} \end{aligned}$		10	20	${\sf mV}_{\sf PP}$
6.2.6b	VRIPPLE_PP_PFM	Auto PFM Mode, low BW case	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V}, V_{\text{OUT}} = 2.5\text{V},\\ &\text{auto PFM, low BW case, C}_{\text{OUT}} = \\ &40\text{uF, X5R, ESR} = 10\text{mOhm,}\\ &\text{L} = 470\text{nH, DCR} = 50\text{m}\Omega\\ &\text{I}_{\text{OUT}} = 20\text{mA} \end{aligned}$		20	40	${\sf mV_{PP}}$
6.2.6c	V <sub>RIPPLE_PP_FF</sub>	Fixed Frequency Mode, low BW case, spread spectrum disabled	$\begin{aligned} &V_{\text{IN}} = 5.0\text{V, } V_{\text{OUT}} = 2.5\text{V,} \\ &\text{fixed frequency, low BW case, } C_{\text{OUT}} \\ &= 12\text{uF, X5R, ESR} = 10\text{mOhm,} \\ &\text{L} = 470\text{nH, DCR} = 50\text{m}\Omega, \\ &\text{I}_{\text{OUT}} = 1\text{A,} \\ &\text{Spread-Spectrum disabled} \end{aligned}$		10	20	$mV_PP$
6.2.6d	V <sub>RIPPLE_PP_FF_SS</sub>	Fixed Frequency Mode, low BW case, spread spectrum enabled	$V_{\text{IN}}$ = 5.0V, $V_{\text{OUT}}$ = 2.5V, fixed frequency, low BW case, $C_{\text{OUT}}$ = 12uF, X5R, ESR = 10mOhm, L = 470nH, DCR = 50m $\Omega$ , $I_{\text{OUT}}$ = 1A, Spread-Spectrum enabled		20	40	$mV_PP$
6.3.1	I <sub>OUT_MAX</sub>	Maximum Operating Current				1.5	Α
6.3.2	I <sub>CURRENT_LIMIT</sub>	Peak Current Limit	V <sub>IN</sub> = 2.5V to 5.5V	3.1	3.9	4.7	Α
6.3.3	I <sub>REV_CUR_LIMIT</sub>	Reverse Peak Current Limit	V <sub>IN</sub> = 2.5V to 5.5V	-2.0	-1.5	-1.0	Α
6.3.4a	R <sub>DSON_HS</sub>	High Side MOSFET On Resistance, 5V-supply	Measured Pin to Pin, V <sub>IN</sub> = 5V			110	mΩ
6.3.4b	R <sub>DSON_HS</sub>	High Side MOSFET On Resistance, 3.3V-supply	Measured Pin to Pin, V <sub>IN</sub> = 3.3V			135	mΩ
6.3.5a	R <sub>DSON_LS</sub>	Low Side MOSFET On Resistance, 5V-supply	Measured Pin to Pin, V <sub>IN</sub> = 5V			110	mΩ
6.3.5b	R <sub>DSON_LS</sub>	Low Side MOSFET On Resistance, 3.3V-supply	Measured Pin to Pin, V <sub>IN</sub> = 3.3V			130	mΩ
6.3.6	R <sub>DISCHARGE</sub>	Output Discharge Resistance	Active only when converter is disabled	60	125	200	Ω
6.4.1	L <sub>SW</sub>	Output Inductance	DCR = 50mΩ max	330	470	611	nΗ
6.4.2a	C <sub>OUT</sub>	Output Capacitance in auto-PFM or forced PWM for low BW case	ESR = 10mΩ max	10		75	μF
6.4.2b	C <sub>OUT_FF</sub>	Output Capacitance in fixed frequency for low BW case	ESR = 10mΩ max	12		36	μF
6.4.3a	C <sub>OUT_HIGH_BW</sub>	Output Capacitance in auto-PFM or forced PWM for high BW case	ESR = 10mΩ max	30		220	μF
	C <sub>OUT_HIGH_BW_FF</sub>	Output Capacitance in fixed	ESR = 10mΩ max	48		144	μF



# 5.7 BUCK2, BUCK3 Converter (continued)

over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.5.1	t <sub>RAMP</sub>	Ramp Time in quasi-fixed-frequency mode	Time from enable to 98% of target value, assuming no residual voltage	0.3		1.65	ms
6.5.2a	DVFS_SLOPE_ QFF	DVFS timing requirements in forced PWM, low BW case	Step-duration during DVFS voltage adjustments from 0.6V to 1.4V	2.9	3.2	3.5	mV/μs
6.5.2b	DVFS_SLOPE_ FF	DVFS timing requirements in fixed-frequency mode, low BW case	Step-duration during DVFS voltage adjustments from 0.6V to 1.4V	1.8	2.1	2.5	mV/μs
Switchi	ing Characteristic	s					
6.5.2c	DVFS_FALL	DVFS timing requirements in forced PWM or fixed-frequency mode, falling slope	Step-duration during DVFS voltage adjustments from 1.4V to 0.6V	0.45	0.53	0.61	mV/μs
6.6.1a	f <sub>SW</sub>	Switching Frequency, forced PWM, high or low BW case	Forced PWM, V <sub>IN</sub> = 3.3V to 5V, V <sub>OUT</sub> = 0.8V to 1.8V, I <sub>OUT</sub> = 1A		2.3		MHz
6.6.1b	f <sub>SW</sub>	Switching Frequency, fixed frequency, high or low BW case, no Spread Spectrum	Fixed - Frequency, $V_{IN}$ = 3.3V to 5V, $V_{OUT}$ = 0.8V to 1.8V, $I_{OUT}$ = 1A	2.18	2.3	2.42	MHz
6.6.2	f <sub>SW_SS_EN</sub>	Switching Frequency, fixed frequency, high or low BW case, with Spread Spectrum enabled	Fixed - Frequency, $V_{IN}$ = 3.3V to 5V, $V_{OUT}$ = 0.8V to 1.8V, $I_{OUT}$ = 1A Spread spectrum enabled	1.95		2.65	MHz

PVIN\_Bx must not exceed VSYS

# 5.8 General Purpose LDOs (LDO1)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electric	al Characteristics					'	
7.1.1	V <sub>IN_LDO</sub>	Input Voltage (LDO-mode) <sup>(1)</sup>	LDO-mode, maximum VSYS	1.5		5.5	V
7.1.2	V <sub>IN_LDO_BYP</sub>	Input Voltage (bypass-mode) <sup>(1) (5)</sup>	Bypass-mode, maximum VSYS	1.5		3.4	V
7.1.3	V <sub>IN_LDO_LSW</sub>	Input Voltage (LSW-mode) <sup>(1)</sup>	LSW-mode, maximum VSYS	1.5		5.5	V
7.1.4	V <sub>OUT_LDO</sub>	LDO Output Voltage configurable Range	LDO mode, with 50-mV steps, $V_{IN}$ - $V_{OUT}$ > 300 mV	0.6		3.4	V
7.1.5	V <sub>OUT_LDO_BYP</sub>	LDO Output Voltage configurable Range in bypass-mode	Bypass mode, configurable V <sub>OUT</sub> range with 50-mV steps	1.5		3.4	V
7.1.6	V <sub>OUT_STEP</sub>	Output Voltage Steps	LDO mode, 0.6V ≤ V <sub>OUT</sub> ≤ 3.4V		50		mV
7.1.7	V <sub>DROPOUT</sub>	Dropout Voltage	$V_{INmin} \le V_{IN} \le V_{INmax}$ , $I_{OUT} = 400$ mA		150	300	mV
7.1.8	Vout_accuracy_	Total DC Output Voltage accuracy, including Voltage References, DC load and line regulations, process and temperature variations	LDO-mode, V <sub>IN</sub> - V <sub>OUT</sub> > 300 mV, V <sub>OUT</sub> ≥ 1V	-1%		1%	
7.1.9	Vout_accuracy_L	Total DC Output Voltage accuracy, including Voltage References, DC load and line regulations, process and temperature variations	LDO-mode, V <sub>IN</sub> - V <sub>OUT</sub> > 300 mV, V <sub>OUT</sub> < 1V	-10		10	mV
7.1.10	R <sub>BYPASS_H</sub>	Bypass Resistance, high output voltage	$2.5 \text{ V} \le \text{V}_{\text{IN}} \le 3.6 \text{ V}, \text{V}_{\text{IN}} \le \text{VSYS},$ $\text{I}_{\text{OUT}} = 400 \text{ mA}, \text{ bypass-mode}$			200	mΩ
7.1.11	R <sub>BYPASS_L</sub>	Bypass Resistance, low output voltage	$1.5 \text{ V} \le \text{V}_{\text{IN}} \le 2.5 \text{ V}, \text{V}_{\text{IN}} \le \text{VSYS},$ $\text{I}_{\text{OUT}} = 400 \text{ mA}, \text{ bypass-mode}$			250	mΩ

Refers to DC-regulation only. Transient response typically improves with more headroom. With low headroom, the frequency variation (2) increases for quasi-fixed frequency.



# 5.8 General Purpose LDOs (LDO1) (continued)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.1.12	R <sub>LSW_H</sub>	LSW Resistance, high output voltage	$2.5 \text{ V} \le \text{V}_{\text{IN}} \le 5.5 \text{ V}, \text{V}_{\text{IN}} \le \text{VSYS},$ $\text{I}_{\text{OUT}} = 400 \text{ mA, LSW-mode}$			200	mΩ
7.1.13	R <sub>LSW_L</sub>	LSW Resistance, low output voltage	$1.5~\text{V} \leq \text{V}_{\text{IN}} \leq 2.5~\text{V},~\text{V}_{\text{IN}} \leq \text{VSYS},\\ \text{I}_{\text{OUT}} = 400~\text{mA, LSW-mode}$			250	mΩ
7.2.1	V <sub>LOAD_TRANSIENT</sub>	Transient Load Regulation, ΔVOUT	$I_{OUT}$ = 20% to 80% to 20% of $I_{OUT\_MAX}$ , $t_r$ = $t_f$ = 1 $\mu s$	-35		35	mV
7.2.2	V <sub>LINE_TRANSIENT</sub>	Transient Line Regulation	$V_{\rm IN}$ step = 600 mV <sub>PP</sub> , $t_{\rm R}$ = $t_{\rm F}$ = 10 $\mu$ s, LDO not in dropout condition, LDO-mode	-25		25	mV
7.2.3	NOISE <sub>RMS</sub>	RMS Noise	100 Hz < f $\leq$ 100 kHz, V <sub>IN</sub> = 3.3 V, V <sub>OUT</sub> = 1.8 V, I <sub>OUT</sub> = 300 mA		600		μV <sub>RMS</sub>
7.2.4	V <sub>RIPPLE</sub>	Voltage Ripple				5	$mV_{PP}$
7.3.1	I <sub>OUT_MAX</sub>	Output Current	V <sub>PVIN_LDOxmin</sub> ≤ V <sub>IN</sub> ≤ V <sub>PVIN_LDOxmax</sub> , Applies to LDO-, bypass- and LSW- mode			400	mA
7.3.2	I <sub>CURRENT_LIMIT</sub>	Short Circuit Current Limit	V <sub>IN</sub> = 3.6V, V <sub>OUT</sub> = 0V	600	980	1600	mA
7.3.3	I <sub>IN_RUSH_LDO</sub>	LDO Inrush Current	LDO-mode, with maximum 20- $\mu$ F load connected to VLDOx, , I <sub>OUT</sub> = 0 mA or 400mA			1500	mA
7.3.4	I <sub>IN_RUSH_LDO_BYP</sub>	LDO Inrush Current in bypass-mode	Bypass-mode, with maximum 50-μF load connected to VLDOx			1500	mA
7.3.5	I <sub>IN_RUSH_LDO_LSW</sub>	LDO Inrush Current in LSW-mode	LSW-mode, with maximum 50-µF load connected to VLDOx			1500	mA
7.3.6	R <sub>DISCHARGE</sub>	Pulldown Discharge Resistance at LDO Output	Active only when converter is disabled. Applies to LDO-, bypass- and LSW-mode	100	200	300	Ω
7.3.7a	I <sub>Q_ACTIVE_LDO</sub>	Quiescent Current in ACTIVE state at 25°C, LDO-mode	LDO-mode, I <sub>OUT</sub> = 0 mA, T <sub>J</sub> = 25°C		50	62	μΑ
7.3.7b	I <sub>Q_ACTIVE_LDO</sub>	Quiescent Current in ACTIVE state -40°C to 125°C, LDO-mode	LDO-mode, I <sub>OUT</sub> = 0 mA, T <sub>J</sub> = -40°C to 125°C		50	65	μΑ
7.3.7b	I <sub>Q_</sub> ACTIVE_LDO	Quiescent Current in ACTIVE state -40°C to 150°C, LDO-mode	LDO-mode, I <sub>OUT</sub> = 0 mA, T <sub>J</sub> = -40°C to 150°C		50	66	μA
7.3.8a	I <sub>Q_ACTIVE_LDO_BY</sub>	Quiescent Current in ACTIVE state at 25°C, bypass-mode	bypass-mode, I <sub>OUT</sub> = 0 mA, T <sub>J</sub> = 25°C		43	48	μΑ
7.3.8b	I <sub>Q_ACTIVE_LDO_BY</sub>	Quiescent Current in ACTIVE state -40°C to 125°C, bypass-mode	bypass-mode, I <sub>OUT</sub> = 0 mA, T <sub>J</sub> = -40°C to 125°C		43	50	μΑ
7.3.8b	IQ_ACTIVE_LDO_BY	Quiescent Current in ACTIVE state -40°C to 150°C, bypass-mode	bypass-mode, I <sub>OUT</sub> = 0 mA, T <sub>J</sub> = -40°C to 150°C		43	50	μА
7.3.9a	I <sub>Q_ACTIVE_LDO_LS</sub>	Quiescent Current in ACTIVE state at 25°C, LSW-mode	LSW-mode, I <sub>OUT</sub> = 0 mA, T <sub>J</sub> = 25°C		46	53	μΑ
7.3.9b	I <sub>Q_ACTIVE_LDO_LS</sub>	Quiescent Current in ACTIVE state -40°C to 125°C, LSW-mode	LSW-mode, I <sub>OUT</sub> = 0 mA, T <sub>J</sub> = -40°C to 125°C		46	53	μΑ



## 5.8 General Purpose LDOs (LDO1) (continued)

over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.3.9b	IQ_ACTIVE_LDO_LS	Quiescent Current in ACTIVE state -40°C to 150°C, LSW-mode	LSW-mode, I <sub>OUT</sub> = 0 mA, T <sub>J</sub> = -40°C to 150°C		46	54	μA
7.4.1	C <sub>IN</sub>	Input Filtering Capacitance (2)	Connected from PVIN_LDOx to GND Applies to LDO-, bypass- and LSW-mode	1.6	2.2		μF
7.4.2	C <sub>OUT</sub>	Output Filtering Capacitance <sup>(3)</sup>	Connected from VLDOx to GND, LDO-mode	1.6	2.2	4	μF
7.4.3	C <sub>OUT_TOTAL</sub>	Total Capacitance at Output (Local + POL), LDO-mode <sup>(4)</sup>	1 MHz < f < 10 MHz			20	μF
7.4.4	C <sub>OUT_TOTAL_BYP</sub>	Total Capacitance at Output (Local + POL), bypass-mode <sup>(4)</sup>	1 MHz < f < 10 MHz			50	μF
7.4.5	C <sub>OUT_TOTAL_LSW</sub>	Total Capacitance at Output (Local + POL), LSW-mode <sup>(4)</sup>	1 MHz < f < 10 MHz			50	μF
7.4.6	C <sub>ESR</sub>	Filtering capacitor ESR max	1 MHz < f < 10 MHz		10	20	mΩ
Timing	Requirements						
7.5.1	t <sub>RAMP</sub>	Ramp Time LDO in LDO- and bypass-mode	Measured from enable to 98% of target value, LDO-mode or bypass-mode, measured when enabled individually, assuming no residual voltage			950	μs
7.5.2	t <sub>RAMP_SLEW</sub>	Ramp up Slew Rate in LDO- and bypass-mode	V <sub>OUT</sub> from 0.3 V to 90% of V <sub>OUT</sub>			12	mV/µs
7.5.3	t <sub>RAMP_LSW</sub>	Ramp Time LSW-mode	Measured from enable to target value, LSW-mode, assuming no residual voltage			1250	μs
7.5.4	t <sub>RAMP_SLEW</sub>	Ramp up Slew Rate in LSW-mode	V <sub>OUT</sub> from 0.3 V to 90% of V <sub>OUT</sub>			12	mV/μs
7.5.5	t <sub>TRANS_1P8_3P3</sub>	Transition Time 1.8V - 3.3V	V <sub>IN</sub> = 4.0V, I <sub>OUT</sub> = 300mA		2		ms
7.5.6	t <sub>TRANS_3P3_1P8</sub>	Transition Time 3.3V - 1.8V	V <sub>IN</sub> = 4.0V, I <sub>OUT</sub> = 300mA		2		ms

- (1) PVIN\_LDOx must not exceed VSYS
- (2) Input capacitors must be placed as close as possible to the device pins.
- (3) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor must be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.
- (4) Additional capacitance, including local and POL, beyond the specified value impacts the LDO's stability.
- (5) PVIN\_LDOx voltage must be within (configured VOUT) and (configured VOUT + 200mV), maximum 3.6V.

## 5.9 General Purpose LDOs (LDO2)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electric	al Characteristi	ics					
8.1.1	V <sub>IN</sub>	Input Voltage (LDO-mode) (1)	LDO-mode, maximum V <sub>VSYS</sub>	2.2		5.5	V
8.1.2	V <sub>IN</sub>	Input Voltage (LSW-mode) (1)	LSW-mode, maximum V <sub>VSYS</sub>	2.2		5.5	V
8.1.3	V <sub>OUT</sub>	LDO Output Voltage configurable Range	$V_{IN}$ = 2.2V to 5.5V, maximum $V_{VSYS}$	1.2		3.3	V
8.1.4	V <sub>OUT_STEP</sub>	Output voltage Steps	1.2V ≤ V <sub>OUT</sub> ≤ 3.3V		50		mV
8.1.5	V <sub>DROPOUT</sub>	Dropout Voltage	$V_{INmin} \le V_{IN} \le V_{INmax}, I_{OUT} = I_{OUT\_MAX}$		150	300	mV





# 5.9 General Purpose LDOs (LDO2) (continued)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
8.1.6	V <sub>OUT_DC_ACCURA</sub>	Total DC accuracy including DC load and line regulation for all valid output voltages	LDO-mode, V <sub>IN</sub> - V <sub>OUT</sub> > 300 mV	-1%		1%	
8.1.7	R <sub>BYPASS</sub>	Bypass resistance in LSW-mode	V <sub>IN</sub> = 3.3V, I <sub>OUT</sub> = 100mA, Loadswitch-mode enabled			1	Ω
8.2.1	V <sub>LOAD_TRANSIENT</sub>	Transient load regulation, ΔV <sub>OUT</sub>	$V_{IN}$ = 3.3V, $V_{OUT}$ = 1.80V, $I_{OUT}$ = 20% of $I_{OUT\_MAX}$ to 80% of $I_{OUT\_MAX}$ in 1µs, $C_{OUT}$ = 2.2µF	-25		25	mV
8.2.2	V <sub>LINE_TRANSIENT</sub>	Transient line regulation, ΔVOUT / VOUT	On mode, not under dropout condition, $V_{IN}$ step = 600 m $V_{PP}$ , $t_r$ = $t_f$ = 10 $\mu$ s	-25		25	mV
8.2.3	NOISE <sub>RMS</sub>	RMS Noise	LDO-mode, f=100Hz to 100KHz, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA		15		μV <sub>RMS</sub>
8.2.4	PSRR <sub>1KHZ</sub>	Power Supply Ripple Rejection	LDO-mode, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA		71		db
8.2.5	PSRR <sub>10KHZ</sub>	Power Supply Ripple Rejection	LDO-mode, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA		64		db
8.2.6	PSRR <sub>100KHZ</sub>	Power Supply Ripple Rejection	LDO-mode, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA		61		db
8.2.7	PSRR <sub>1MHZ</sub>	Power Supply Ripple Rejection	LDO-mode, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA		26		db
8.3.1	I <sub>OUT_MAX</sub>	Output Current				300	mA
8.3.2	I <sub>CURRENT_LIMIT</sub>	Short Circuit Current Limit	V <sub>IN</sub> = 3.6V, V <sub>OUT</sub> = 0V, Tested under a pulsed load condition	400		900	mA
8.3.3	I <sub>IN_RUSH</sub>	LDO inrush current	LDO- or LSW-mode, $V_{IN}$ = 3.3V and then LDO is enabled, $C_{OUT}$ = 4 $\mu$ F, $I_{OUT}$ = 0 mA or 300mA			650	mA
8.3.4	R <sub>DISCHARGE</sub>		Active only when converter is disabled	120	250	400	Ω
8.3.5a	I <sub>Q_ACTIVE</sub>	Quiescent Current in ACTIVE state at 25°C	$V_{VSYS} = V_{IN} = 3.3 \text{ V}, I_{OUT} = 0 \text{ mA}$ Applies to LDO-mode, $T_J = 25^{\circ}\text{C}$		25	30	μА
8.3.5b	I <sub>Q_ACTIVE</sub>	Quiescent Current in ACTIVE state -40°C to 125°C	$V_{VSYS} = V_{IN} = 3.3 \text{ V}, I_{OUT} = 0 \text{ mA}$ Applies to LDO-mode, $T_J = -40^{\circ}\text{C}$ to 125°C		25	40	μΑ
8.3.5b	I <sub>Q_ACTIVE</sub>	Quiescent Current in ACTIVE state -40°C to 150°C	$V_{VSYS} = V_{IN} = 3.3 \text{ V}, I_{OUT} = 0 \text{ mA},$ Applies to LDO-mode, $T_J = -40^{\circ}\text{C}$ to 150°C		25	40	μΑ
8.3.5c	I <sub>Q_ACTIVE</sub>	Quiescent Current in ACTIVE state at 25°C	$V_{VSYS} = V_{IN} = 3.3 \text{ V}, I_{OUT} = 0 \text{ mA}$ Applies to LSW-mode, $T_J = 25^{\circ}\text{C}$		60	112	μΑ
8.3.5d	I <sub>Q_ACTIVE</sub>	Quiescent Current in ACTIVE state -40°C to 125°C	$V_{VSYS} = V_{IN} = 3.3 \text{ V}, I_{OUT} = 0 \text{ mA}$ Applies to LSW-mode, $T_J = -40^{\circ}\text{C}$ to 125°C		70	145	μА
8.3.5d	I <sub>Q_ACTIVE</sub>	Quiescent Current in ACTIVE state -40°C to 150°C	$V_{VSYS} = V_{IN} = 3.3 \text{ V}, I_{OUT} = 0 \text{ mA},$ Applies to LSW-mode, $T_J = -40^{\circ}\text{C}$ to 150°C		70	145	μA
8.4.1	C <sub>IN</sub>	Input Filtering Capacitance (2)		2.2	4.7		μF
8.4.2	C <sub>OUT</sub>	Output Filtering Capacitance (2)	Connected from VLDOx to GND, LDO-mode	1.6	2.2	4	μF
8.4.3a	C <sub>OUT_TOTAL_FAST</sub>	Total Capacitance at Output (Local + POL), fast ramp-time (3)	1 MHz < f < 10 MHz, impedance between output and point-of-load maximum 6nH			15	μF

## Instruments www.ti.com

## 5.9 General Purpose LDOs (LDO2) (continued)

over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
8.4.3b	C <sub>OUT_TOTAL_SLOW</sub>	Total Capacitance at Output (Local + POL), slow ramp-time (3)	1 MHz < f < 10 MHz, impedance between output and point-of-load maximum 6nH			30	μF
8.4.4	C <sub>ESR</sub>	Filtering capacitor ESR max	1MHz to 10MHz		10	20	mΩ
Timing	Requirements						
8.5.1a	tramp_fast	Ramp Time fast	Measured from enable to 98% of target value, LDO- mode, measured when enabled individually, assuming no residual voltage			660	μs
8.5.1b	tramp_slow	Ramp Time slow	Measured from enable to 98% of target value, LDO- mode, measured when enabled individually, assuming no residual voltage			2.3	ms
8.5.2a	t <sub>RAMP_SLEW_FAST</sub>	Ramp Up Slew Rate fast	LDO- or LSW-mode, measured from 0.5V to target value			25	mV/μs
8.5.2b	t <sub>RAMP_SLEW_SLOW</sub>	Ramp Up Slew Rate slow	LDO- or LSW-mode, measured from 0.5V to target value			9	mV/μs

- (1) PVIN\_LDOx must not exceed VSYS
- When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor must be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.
- Additional capacitance, including local and POL, beyond the specified value impacts the LDO's stability.

# 5.10 GPIOs and multi-function pins (EN/PB/VSENSE, nRSTOUT, nINT, GPO1, GPO2, GPIO, MODE/RESET, MODE/STBY, VSEL\_SD/VSEL\_DDR)

over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electric	al Characteristic	cs					
9.1.1	V <sub>OL</sub>	Low-level Output Voltage (open-drain)	VIO = 3.6V, I <sub>OL</sub> = 2mA, GPO1, GPO2, GPIO, nRSTOUT, nINT			0.40	V
9.1.2	V <sub>IL</sub>	Low-level Input Voltage	EN/PB, MODE/STBY, MODE/ RESET and VSEL_SD/VSEL_DDR, GPIO			0.4	V
9.1.3	V <sub>IH</sub>	High-level Input Voltage	EN/PB, MODE/STBY, MODE/ RESET and VSEL_SD/VSEL_DDR, GPIO	1.26			V
9.1.4	V <sub>VSENSE</sub>	VSENSE Comparator Threshold (EN/PB/VSENSE)		1.08	1.20	1.32	V
9.1.5	V <sub>VSENSE_HYS</sub>	VSENSE Comparator Hysteresis (EN/PB/VSENSE)		8	30	55	mV
9.1.6	I <sub>LKG</sub>	Input leakage current (GPIO, EN/PB/VSENSE, MODE/STBY, MODE/RESET, VSEL_SD/VSEL/ DDR)	V <sub>IN</sub> = 3.3 V			1.0	μΑ
9.1.7	C <sub>IN</sub>	Internal input pin capacitance (GPIO, EN/PB/ VSENSE, MODE/STBY, MODE/ RESET, VSEL_SD/VSEL/DDR)				10	pF

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback



# 5.10 GPIOs and multi-function pins (EN/PB/VSENSE, nRSTOUT, nINT, GPO1, GPO2, GPIO, MODE/RESET, MODE/STBY, VSEL\_SD/VSEL\_DDR) (continued)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
9.1.8	I <sub>PD</sub>	pull-down current, available 100us after VSYS is applied	on pins GPO1, GPO2, GPIO, MODE/STBY, MODE/RESET, VSEL_SD/VSEL_DDR, nINT, nRSTOUT	18	25	35	nA
9.1.9	I <sub>LKG_VSYS_ONLY</sub>	Pin leakage when VSYS is present, but digital supply VDD1P8 is not	SDA only			1	μΑ
9.1.10	V <sub>PIN_VSYS_ONLY</sub>	Pin voltage when VSYS is present, but digital supply VDD1P8 is not	GPO1, GPO2, GPIO, nRSTOUT, nINT, I <sub>OL</sub> =2mA			0.4	V
Timing	Requirements						
9.2.1a	t <sub>FALL</sub>	Output buffer fall time (90% to 10%)	GPO1, GPO2, GPIO, nRSTOUT, nINT, C <sub>OUT</sub> = 10pF			50	ns
9.2.1b	t <sub>RISE</sub>	GPIO Output buffer rise time (10% to 90%)	GPIO, applicable in Multi-PMIC-configuration			5	μs
9.2.1.1	t <sub>DLY_FALL</sub>	Output buffer falling time delay (input crossing 50% to output crossing 50%)	C <sub>OUT</sub> = 10pF			50	ns
9.2.2.1	t <sub>DLY_RISE</sub>	Open Drain Output buffer rising time delay (digital input to output crossing 50%)	C <sub>OUT</sub> = 10pF, R <sub>PU</sub> =1k (external pull up), VIO = 1.8V			300	ns
9.2.2.3	FLT_HIGH <sub>Duration</sub>	Time the digital has allotted for the test to see if the pin is able to be pulled high internally	C <sub>OUT</sub> = 10pF	15			μs
9.2.2.4	FLT_LOW <sub>Duration</sub>	Time the digital has allotted for the test to see if the pin is able to be pulled low internally	C <sub>OUT</sub> = 10pF	15			μs
9.2.2a	t <sub>PB_ON_SLOW</sub>	EN/PB/VSENSE, Wait Time PB, ON request, slow	PB, falling Edge	540	600	660	ms
9.2.2b	t <sub>PB_ON_FAST</sub>	EN/PB/VSENSE, Wait Time PB, ON request, fast	PB, falling Edge	180	200	220	ms
9.2.3	t <sub>PB_OFF</sub>	EN/PB/VSENSE, Wait Time PB, OFF request	PB, falling Edge	7.2	8.0	8.8	s
9.2.4	t <sub>PB_RISE_DEGL</sub>	EN/PB/VSENSE, Deglitch time PB, rising edge	PB, rising Edge, applicable after the successful long-press-OFF-request	115	200	275	ms
9.2.5	t <sub>PB_INT_DEGL</sub>	EN/PB/VSENSE, Deglitch time PB, rising or falling edge	PB, rising or falling Edge	59	100	137	ms
9.2.6	t <sub>DEGL_EN_Rise_Slow</sub>	EN/PB/VSENSE, DeglitchTime EN slow, rising	EN, rising Edge	45	50	55	ms
9.2.7	t <sub>DEGL_EN_Rise_Fast</sub>	EN/PB/VSENSE, DeglitchTime EN fast, rising	EN, rising Edge	60	120	150	μs
9.2.8	t <sub>DEGL_EN_Fall</sub>	EN/PB/VSENSE, DeglitchTime EN, falling	EN, falling Edge	50	70	93	μs
9.2.9	t <sub>DEGL_VSENSE_Rise</sub>	VSENSE rising: only gated by VSYS <sub>POR_Rising</sub> and VSENSE-voltage	VSENSE, rising Edge		N/A		
9.2.10	t <sub>DEGL_VSENSE_Fall</sub>	EN/PB/VSENSE, DeglitchTime VSENSE, falling, regardless of fast/ slow setting	VSENSE, falling Edge	50	70	93	μs
9.2.11	t <sub>DEGL_EN/</sub> VSENSE_I2C	EN/VSENSE falling edge deglitch time after I2C-triggered shutdown	EN/VSENSE falling edge after previous shutdown request by I2C (shorter than 9.2.8)	12.5	25	37.5	μs
9.2.12	t <sub>DEGL_RESET</sub>	MODE/RESET, Deglitch Time RESET	RESET, rising and falling Edge	90	120	150	μs

# 5.10 GPIOs and multi-function pins (EN/PB/VSENSE, nRSTOUT, nINT, GPO1, GPO2, GPIO, MODE/RESET, MODE/STBY, VSEL\_SD/VSEL\_DDR) (continued)

over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
9.2.13	t <sub>DEGL_MFP</sub>	Deglitch Time MODE/STBY, MODE(not/RESET), VSEL_SD/ VSEL_DDR	Rising and falling Edge	90	120	150	μs
9.2.14	t <sub>DEGL_GPIO</sub>	Deglitch Time GPIO	Rising and falling Edge	6.6	15.6	18	μs
9.2.15	t <sub>REACTION_ON</sub>	ON-request propagation delay (after deglitch)	Includes oscillator startup, sampling delay and reaction delay (excluding deglitch)		75	103	μs
9.2.16	t <sub>REACTION_OFF</sub>	OFF-request propagation delay (after deglitch)	Includes sampling delay and reaction delay (excluding deglitch)	39	56	73.5	μs

## **5.11 Voltage and Temperature Monitors**

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electric	al Characteristics						
10.1.1	V <sub>BUCKx_UV_TH_5</sub> , V <sub>LDOx_UV_TH_5</sub>	Undervoltage monitoring for buck output, programable low-going threshold accuracy	UV_THR = 0x0		-5%		
10.1.2	VBUCKX_UV_TH_10, VLDOX_UV_TH_10	Undervoltage monitoring for buck output and LDO output, programable low-going threshold accuracy	UV_THR = 0x1		-10%		
10.1.3	V <sub>BUCKx_UV_H_ACC</sub> , V <sub>LDOx_UV_H_ACC</sub>	Undervoltage Threshold Accuracy, V <sub>OUT</sub> ≥ 1V	V <sub>OUT</sub> ≥ 1V	-1.5%		+1.5%	
10.1.4	V <sub>BUCKx_UV_L_ACC</sub> , V <sub>LDOx_UV_L_ACC</sub>	Undervoltage Threshold Accuracy, V <sub>OUT</sub> < 1V	V <sub>OUT</sub> < 1V	-10		+10	mV
10.1.5	V <sub>BUCKx_UV_HYS</sub> , V <sub>LDOx_UV_HYS</sub>	Undervoltage Hysteresis		0.25%	1%	1.75%	
10.1.6	V <sub>BUCKx_SCG_TH</sub> , V <sub>LDOx_SCG_TH</sub>	Short-circuit (SCG) and residual voltage (RV) detection low-going threshold		220	260	300	mV
10.1.7	VBUCKX_SCG_HYS, VLDOX_SCG_HYS	Short-circuit (SCG) and residual voltage (RV) detection threshold hysteresis			75		mV
10.2.1a	T <sub>WARM_Rising</sub>	Temperature rising Warning Threshold (WARM)	for each of the four sensors	110	120	130	°C
10.2.1b	T <sub>WARM_Falling</sub>	Temperature falling Warning Threshold (WARM)	for each of the four sensors	105	115	125	°C
10.2.2a	T <sub>HOT_Rising</sub>	Temperature rising Shutdown Threshold (TSD, HOT)	for each of the four sensors	130	140	150	°C
10.2.2b	T <sub>HOT_Falling</sub>	Temperature falling Shutdown Threshold (TSD, HOT)	for each of the four sensors	125	135	145	°C
10.2.3	T <sub>HYS</sub>	Temperature Hysteresis for WARM	for each of the four sensors		-5		°C
Timing	Requirements			,	,	'	
10.3.1a	t <sub>DEGLITCH</sub>	Fault Detection Deglitch Time for Undervoltage (UV) and Short to GND (SCG)	Measured from UV/SCG event	13	20	27	μs



# **5.11 Voltage and Temperature Monitors (continued)**

over operating free-air temperature range (unless otherwise noted)

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
10.3.1b	tDEGLITCH_OC_short	Fault Detection Deglitch Time for Over Current (OC), rising edge, short	Measured from OC event, rising edge	26	35	45	μs
10.3.1c	tDEGLITCH_OC_long	Fault Detection Deglitch Time for Over Current (OC), rising edge, long	Measured from OC event, rising edge	1.6	2	2.2	ms
10.3.2a	t <sub>REACTION</sub>	Fault Reaction Time for Undervoltage (UV) and Short to GND (SCG) (including deglitch time)	Measured from UV/SCG event to nINT pulled low	26	40	54	μs
10.3.2b	tREACTION_OC_shor	Fault Reaction Time for Over Current (OC) (including deglitch time)	Measured from UV/OC/SCG event to nINT pulled low	45	65	81	μs
10.3.2c	tREACTION_OC_long	Fault Detection Deglitch Time for Over Current (OC), rising edge, long	Measured from OC event, rising edge	1.6	2	2.2	ms
10.3.2d	treaction_warm	Fault Reaction Time for Temperature Warning (WARM), Thermal Shutdown (TSD / HOT)	Measured from WARM/HOT event to nINT pulled low			525	μs

# 5.12 I<sup>2</sup>C Interface

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3V or 1.8V.

POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electric	cal Characteri	stics					
11.1.1	V <sub>OL</sub>	Low-level Output Voltage	VIO = 3.6V, I <sub>OL</sub> = 3mA for Standard mode and Fast mode, I <sub>OL</sub> = 20mA for Fast mode+, SDA			0.40	V
11.1.2	V <sub>IL</sub>	Low-level Input Voltage	SDA, SCL			0.40	V
11.1.3	V <sub>IH</sub>	High-level Input Voltage	SDA, SCL	1.26			V
11.1.4	V <sub>HYST</sub>	Input buffer Hysteresis	EN_BP/VSENSE, MODE_RESET, MODE_STBY, SDA, SCL, GPIO	100		500	mV
11.1.5	СВ	Capacitive Load for SDA and SCL				400	pF
Timing	Requirement	s					
11.2.1			Standard mode			100	kHz
11.2.2	f <sub>SCL</sub>	Serial Clock Frequency	Fast mode			400	KΠZ
11.2.3			Fast mode+			1	MHz
11.3.1			Standard mode	4.7			
11.3.2	$t_{LOW}$	SCL low Time	Fast mode	1.3			μs
11.3.3			Fast mode+	0.50			
11.4.1			Standard mode	4.0			
11.4.2	t <sub>HIGH</sub>	SCL high Time	Fast mode	0.60	·		μs
11.4.3			Fast mode+	0.26			
11.5.1			Standard mode	250			
11.5.2	t <sub>SU;DAT</sub>	Data setup Time	Fast mode	100			ns
11.5.3			Fast mode+	50			
11.6.1			Standard mode	10		3450	
11.6.2	t <sub>HD;DAT</sub>	Data hold Time	Fast mode	10		900	ns
11.6.6			Fast mode+	10			

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated



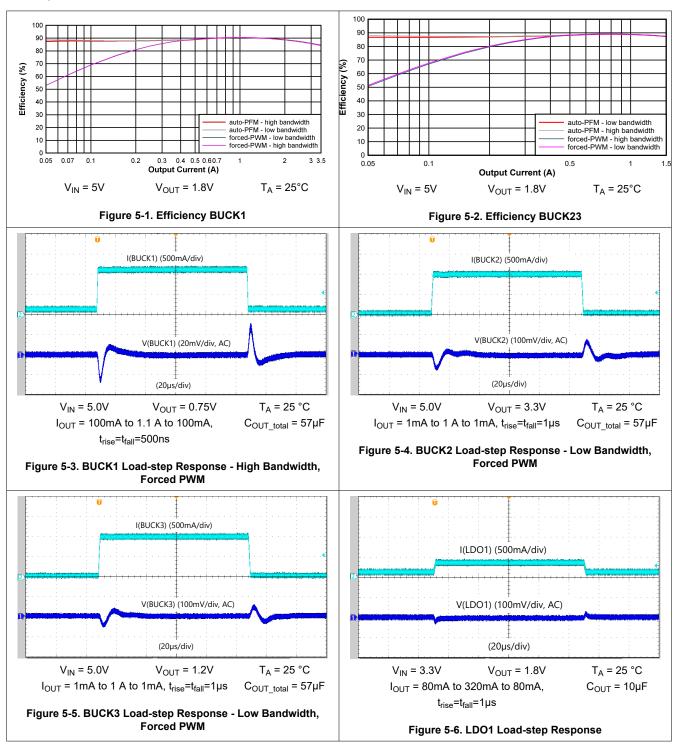
# 5.12 I<sup>2</sup>C Interface (continued)

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3V or 1.8V.

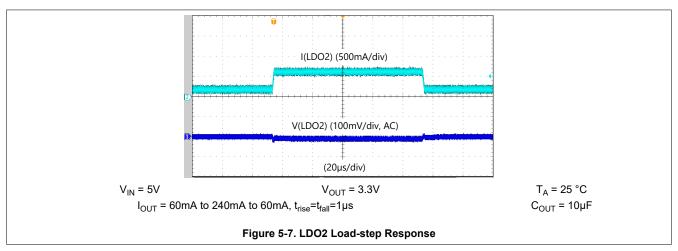
POS		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
11.7.1			Standard mode	4.7			
11.7.2	t <sub>SU;STA</sub>	Setup Time for a Start or a REPEATED Start Condition	Fast mode	0.60			μs
11.7.3		THE EATED Start Condition	Fast mode+	0.26			
11.8.1			Standard mode	4.7			
11.8.2	t <sub>HD;STA</sub>	Hold Time for a Start or a REPEATED Start Condition	Fast mode	0.60			μs
11.8.3		THE EXTED Start Container	Fast mode+	0.26			
11.9.1			Standard mode	4.7			
11.9.2	t <sub>BUF</sub>	Bus free Time between a STOP and Start Condition	Fast mode	1.3			μs
11.9.3		Start Cornation	Fast mode+	0.50			
11.10.1			Standard mode	0.60			
11.10.2	t <sub>su;sto</sub>	Setup Time for a STOP Condition	Fast mode	0.60			μs
11.10.3			Fast mode+	0.26			
11.10.1			Standard mode, VIO = 1.8V, $R_{PU}$ = 10 k $\Omega$ and $C_B$ = 400 pF			1000	
11.10.2	t <sub>rDA</sub>	Rise Time of SDA Signal	Fast mode, VIO = 1.8V, $R_{PU}$ = 1 k $\Omega$ and $C_B$ = 400 pF	20		300	ns
11.10.3			Fast mode+, VIO = 1.8V, $R_{PU}$ = 330 $\Omega$ and $C_B$ = 400 pF			120	
11.12.1			Standard mode, VIO = 1.8V, $R_{PU}$ = 10 k $\Omega$ and $C_{B}$ = 400 pF			300	
11.12.2	t <sub>fDA</sub>	Fall Time of SDA Signal	Fast mode, VIO = 1.8V, $R_{PU}$ = 1 k $\Omega$ and $C_B$ = 400 pF	6.5		300	ns
11.12.3			Fast mode+, VIO = 1.8V, $R_{PU}$ = 330 $\Omega$ and $C_B$ = 400 pF	6.5		120	
11.13.1			Standard mode, VIO = 1.8V, $R_{PU}$ = 10 k $\Omega$ and $C_{B}$ = 400 pF			1000	
11.13.2	t <sub>rCL</sub>	Rise Time of SCL Signal	Fast mode, VIO = 1.8V, $R_{PU}$ = 1 k $\Omega$ and $C_B$ = 400 pF	20		300	ns
11.13.3			Fast mode+, VIO = 1.8V, $R_{PU}$ = 330 $\Omega$ and $C_B$ = 400 pF			120	
11.14.1			Standard mode, VIO = 1.8V, $R_{PU}$ = 10 k $\Omega$ and $C_B$ = 400 pF			300	
11.14.2	t <sub>fCL</sub> Fall Time of SCL Signal	Fall Time of SCL Signal	Fast mode, VIO = 1.8V, $R_{PU}$ = 1 k $\Omega$ and $C_B$ = 400 pF	6.5		300	ns
11.14.3		F	Fast mode+, VIO = 1.8V, $R_{PU}$ = 330 $\Omega$ and $C_B$ = 400 pF	6.5		120	
11.15.1	t <sub>SP</sub>	Pulse Width of Spike suppressed (SCL and SDA Spikes that are less than the indicated Width are suppressed)	Fast mode, and fast mode+			50	ns



## 5.13 Typical Characteristics



# **5.13 Typical Characteristics (continued)**





# 6 Detailed Description

#### 6.1 Overview

The TPS65215-Q1 provides three step-down converters, two LDOs, three general-purpose I/Os and three multi-Function pins. The system is able to be supplied with a single cell Li-Ion battery, two primary cells or a regulated supply. The device is characterized across a -40°C to +125°C temperature range, which makes the PMIC an excellent choice for various automotive applications.

The I2C interface provides comprehensive features for using TPS65215-Q1. All rails, the GPOs and the GPIO are configurable as enabled or disabled. Voltage thresholds for the undervoltage monitoring are customizable.

The integrated voltage supervisor monitors Buck1-3 and LDO1-2 for undervoltage. The monitor has two sensitivity settings. A power good signal is provided to report the successful ramp of the power rails and GPIOs. The nRSTOUT pin is pulled low until the device enters ACTIVE state. When powering down from ACTIVE-or STBY-state, nRSTOUT is pulled low again. The nRSTOUT pin has an open-drain output. A fault-pin, nINT, notifies the SoC about faults.

Buck1 step-down converter supplies up to 3.5A of current, Buck2 and Buck3 supplies up to 1.5A each. The default output voltages for each converter are adjustable through the I2C interface. All three buck-converters feature dynamic voltage scaling. The step-down converters operate in a low power mode at light load or in a forced into PWM operation for noise sensitive applications.

LDO1 supports output currents of 400mA at an output voltage range of 0.6V to 3.4V. This LDO supports bypass mode, acting as a load-switch, and allowing voltage-changes during operation for applications like SD-card-supply, adjusting the IO-supply of the SD-card from 3.3V to 1.8V after initialization.

LDO2 supports output currents of 300mA at an output voltage range of 1.2V to 3.3V. This LDO supports load-switch-mode, but not bypass mode.

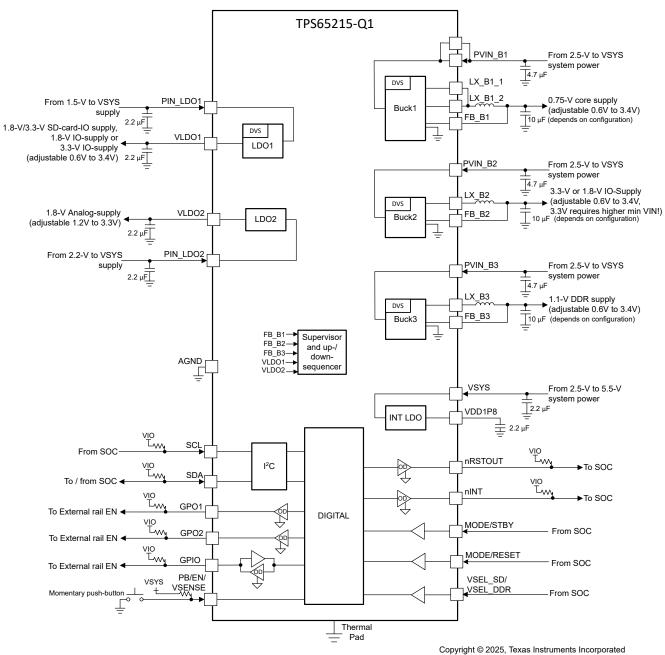
The I2C-interface, IOs, GPIOs, and multi-function-pins (MFP) allow a seamless interface to a wide range of SoCs.

All configurations of the rails, for example output-voltages, sequencing, are backed up by EEPROM. Please refer to the Technical Reference Manual (TRM) of the chosen configuration.

Product Folder Links: TPS65215-Q1



## 6.2 Functional Block Diagram



1, 3

Figure 6-1. Functional Block Diagram

#### Note

VIO is the external pull-up supply that must be selected within the recommended operating voltage range.



## **6.3 Feature Description**

#### 6.3.1 Power-Up Sequencing

The TPS65215-Q1 allows flexible sequencing of the rails. The order of the rails, including GPO1, GPO2, GPIO for the external rails, and the nRSTOUT pin is defined by the NVM. Prior to starting the power-up sequence, the device checks if the voltage on all rails fell below the SCG-threshold to avoid starting into a pre-biased rail. The sequence is timing based. In addition, the previous rail must have passed the UV-threshold to enable the subsequent rail. If UV is masked, the sequence proceeds even if the UV-threshold is not reached. GPO1, GPO2, GPIO, and LDOs configured in bypass- or LSW-mode are not monitored for undervoltage, thus these outputs do not gate subsequent rails.

In case the sequence is interrupted due to an unmasked fault on a rail, the device powers down. The TPS65215-Q1 attempts to power up two more times. If both of those re-tries fail to enter ACTIVE state, the device remains in INITIALIZE state until VSYS is power-cycled. While encouraged to keep this retry-counter active, the retry-counter is maskable by setting bit MASK\_RETRY\_COUNT in INT\_MASK\_UV register.

To disable the retry-counter, set bit MASK\_RETRY\_COUNT in INT\_MASK\_UV register. When set, the device attempts to retry infinitely.

The TPS65215-Q1 allows to configure the power-down sequence independent from the power-up sequence. The sequences are configured in the non-volatile memory.

At initial power-up, the device monitors the VSYS supply voltage and allows power-up and transition to INITIALZE state only if VSYS passed the VSYS $_{POR}$  $_{Rising}$  threshold.

The power-up sequence is configured as follows:

- The slot (respectively the position in the sequence) for each rail and GPO1, GPO2, GPIO, and nRSTOUT is
  defined using the corresponding \*\_SEQUENCE\_SLOT registers, the four MSB for the power-up sequence,
  the four LSB for the power-down sequence.
- The duration of each slot is defined in the POWER\_UP\_SLOT\_DURATION\_x registers and are configurable as 0ms, 1.5ms, 3ms or 10ms. In total, 16 slots are available, allowing the sequence to span over multiple TPS65215-Q1-devices if more rails need to be supported.
- In addition to the timing as defined above, the power-up-sequence is also gated by the UV-monitor: a subsequent rail only gets enabled after the previous one passed the undervoltage threshold (unless UV is masked). If a rail has not reached the UV-threshold by the end of t<sub>RAMP</sub> (respectively t<sub>RAMP\_LSW</sub>, t<sub>RAMP\_SLOW</sub>, t<sub>RAMP\_FAST</sub>), the sequence is aborted and the device sequences down at the end of the slot-duration. For the respective rail, the device sets INT\_BUCK\_x\_y\_IS\_SET respectively INT\_LDO\_x\_y\_IS\_SET bit in INT\_SOURCE register and BUCKx\_UV respectively LDOx\_UV bit in INT\_BUCK\_x\_y respectively INT\_LDO\_x\_y register as well as bit TIMEOUT in the INT\_TIMEOUT\_RV\_SD register.
- The initiation of the sequence is gated by the successful discharge of all rails, irrespective if enabled during
  the sequence or not. If the device is unable to discharge all rails below the SCG-threshold, the device sets
  INT\_BUCK\_x\_y\_IS\_SET respectively INT\_LDO\_x\_y\_IS\_SET bit in INT\_SOURCE register and BUCKx\_RV
  respectively LDOx\_RV bit if the residual voltage is still present after 4ms to 5ms and the device remains in
  INITIALIZE state.
- The initiation of the sequence is gated by the die-temperature: if any one of the WARM detections is
  unmasked, the device does not power-up until the temperature on all sensors fell below T<sub>WARM\_falling</sub>
  threshold if INITIALIZE state was entered due to a thermal event, respectively until the temperature on
  all sensors is below T<sub>WARM\_rising</sub> threshold if INITIALIZE state was entered from OFF-state. If all thermal
  sensors are masked (WARM detection not causing a power-down), the device does not power-up until the
  temperature on all sensors is below T<sub>HOT\_falling</sub> threshold

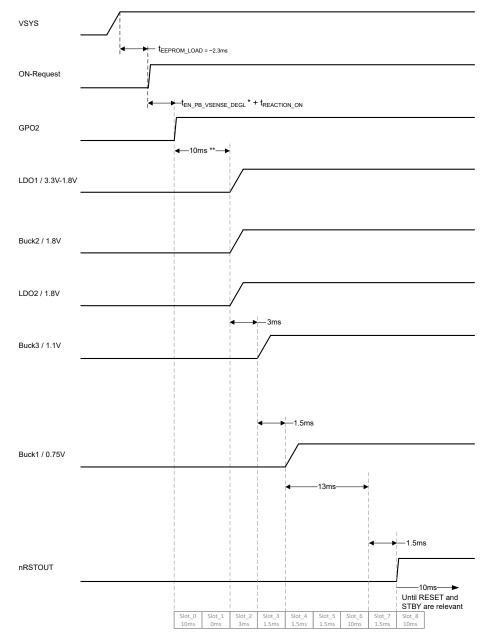
#### Note

All rails get discharged prior to enable (irrespective if discharge-function is disabled).

Product Folder Links: TPS65215-Q1

An ON-request is deglitched to not trigger on noise. After the deglitch time, the device takes approximately 300µs until the first slot of the sequence starts. In case discharging of pre-biased rails is not completed by that time, the start of the sequence is further gated until all rails have discharged below SCG-voltage level.

Figure 6-2 shows an example of a power up sequence. The power up sequence is triggered through a valid on request.



<sup>\*</sup> depends on EN / PB / VSENSE and long/short configuration, ~0 if FSD is enabled

Figure 6-2. Power-up Sequencing (example)

For details on ON-requests please see Push Button and Enable Input (PB/EN/VSENSE).

<sup>\*\*</sup> if applicable, slot-duration needs to adopt for enable- & ramp-time of external rail

#### **CAUTION**

I2C commands must only be issued after EEPROM-load completed.

### 6.3.2 Power-Down Sequencing

An OFF-request or a shut-down-fault triggers the power-down sequence. The OFF-request is triggered by a falling edge on EN/PB/VSENSE if configured for EN or VSENSE respectively a long press of the push-button if configured as PB or by an I2C-command to I2C\_OFF\_REQ in MFP\_CTRL register. This bit self-clears.

An I2C-triggered shut-down requires a renewed ON-request on the EN/PB/VSENSE pin. In case of EN- or VSENSE-configuration, a low-going edge followed by a high-going-edge is required on the EN/PB/VSENSE-pin. The falling-edge deglitch time for EN or VSENSE configuration  $t_{DEGL\_EN/VSENSE\_I2C}$  is shorter than the deglitch-time for pin-induced OFF-requests ( $t_{DEGL\_EN\_Fall}$  and  $t_{DEGL\_VSENSE\_Fall}$ ). The deglitch-times for PB-configuration remain.

In many cases, the power-down sequence follows the reverse power-up sequence. In some applications, all rails are required to shut down at the same time with no delay between rails or require wait-times to allow discharging of rail.

The power-down sequence is configured as follows:

- The slot (respectively the position in the sequence) for each rail and GPO1, GPO2, GPIO, and nRSTOUT is
  defined using the corresponding \*\_SEQUENCE\_SLOT registers, the four MSB for the ON-sequence, the four
  LSB for the down-sequencing.
- The duration of each slot is defined in the POWER\_DOWN\_SLOT\_DURATION\_x registers and are configurable as 0 ms, 1.5ms, 3ms or 10ms. In total, 16 slots are available, allowing the sequence to span over multiple TPS65215-Q1-devices if more rails need to be supported.
- In addition to the slot-duration, the power-down sequence is also gated by the previous rail being discharged below the SCG-threshold, unless active discharge is disabled on the previous rail. If that does not occur, the power-down of subsequent rails is paused. To allow for power-down in case of biased or shorted rails, the sequence continues despite an incomplete discharge of the previous rail after eight times the slot-duration (or 12ms in case of slot-duration of 0ms).
- To bypass the discharge-check, set the bit BYPASS\_RAILS\_DISCHARGED\_CHECK in register GENERAL\_CONFIG to '1'.

#### Note

In case active discharge on a rail is disabled, unsuccessful discharge of the rail within the slot duration does not gate the disable of the subsequent rail, but the sequence is purely timing based. In case of residual voltage, the RV-bit is be set regardless.

Active discharge is enabled by default and not NVM based. Thus, if desired, discharge need to be disabled after each VSYS-power-cycle. During RESET or OFF-request, the discharge configuration is not reset, as long as VSYS is present. However, in INITIALIZE state and prior to the power-up-sequence, all rails get discharged, regardless of the setting.

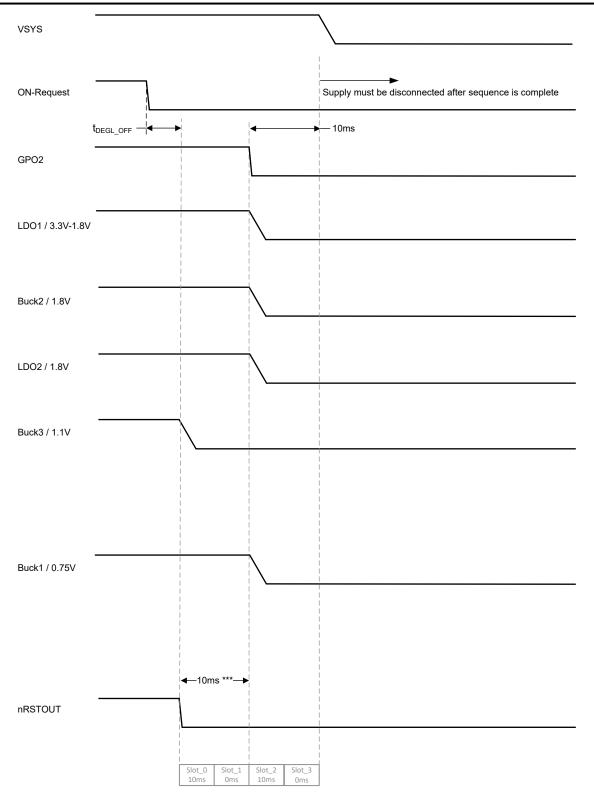
During the power-down-sequence, non-EEPROM-backed bits get reset, with the exception of unmasked interrupt bits and \*\_DISCHARGE\_EN bits.

Below graphic shows the power-down-sequence for NVM-ID 0x01, revision 0x2 as an example:

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated





<sup>\*\*\*</sup> discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.

Figure 6-3. Power-down Sequencing (example)

SLVSHQ9 – JUNE 2025



#### **CAUTION**

Do not change the registers related to an ongoing sequence by I2C-command!

Non-NVM-bits are not accessible for approximately 80µs after starting a transition into INITIALIZE state.

### 6.3.3 Push Button and Enable Input (EN/PB/VSENSE)

The EN/PB/VSENSE pin is used to enable the PMIC. The pin is configurable to three different functions:

- Device enable (EN):
  - This pin needs to be pulled high to enable the device. Pulling this pin low disables the device.
  - The deglitch-time of the EN-pin is configured by EN\_PB\_VSENSE\_DEGL in MFP\_2\_CONFIG register.
  - The power-up sequence starts if the EN input is above the V<sub>IL</sub>-threshold low for the configured t<sub>DEGL</sub> EN Rise.
  - To signify the power-up based on an EN/PB/VSENSE pin-event, the device sets bit POWER\_UP\_FROM\_EN\_PB\_VSENSE in POWER\_UP\_STATUS\_REG register. This bit does not assert the nINT pin. Write W1C to clear the bit.
  - The power-down sequence starts if the EN input is below the V<sub>IH</sub>-threshold for t<sub>DEGL EN Fall</sub>.
  - In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power-up sequence if EN input is still above the V<sub>IH</sub>-threshold. (EN considered level-sensitive)
  - In case of a cold reset (regardless if by RESET-pin or I2C-request), no renewed on-request is required.
     The device automatically executes the power-up sequence if EN input is still above the V<sub>IH</sub>-threshold. (EN considered level-sensitive)
- Push-Button (PB):
  - The PB pin is a CMOS-type input used to power-up the PMIC. Typically, the PB pin is connected to a momentary switch to ground and an external pullup resistor.
  - The hold-time of the push-button is configured by EN\_PB\_VSENSE\_DEGL in MFP\_2\_CONFIG register.
  - The power-up sequence starts if the PB input is below the V<sub>IL</sub>-threshold low for the configured t<sub>PB ON</sub>.
  - To signify the power-up based on an EN/PB/VSENSE pin-event, the device sets bit
     POWER\_UP\_FROM\_EN\_PB\_VSENSE in POWER\_UP\_STATUS\_REG register. This bit does not assert the nINT pin. Write W1C to clear the bit.
  - The PB pin has a rising-edge deglitch t<sub>PB RISE DEGL</sub> to filter bouncing of the switch
  - The power-down sequence starts if the PB input is held low for t<sub>PB OFF</sub>-time (not configurable).
  - In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power-up sequence without a PB-press.
  - In case of a cold reset (regardless if by RESET-pin or I2C-request), no renewed on-request is required.
     The device automatically executes the power-up sequence without a PB-press.
  - A push-button press is only recognized after VSYS is above VSYS\_POR-threshold or the PB must be held long enough after VSYS is above VSYS POR-threshold.
  - Following bits in the signify the PB-press events:
    - PB\_FALLING\_EDGE\_DETECTED: PB was pressed for a time-interval longer than t<sub>PB\_INT\_DEGL</sub> since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK\_INT\_FOR\_PB='0'). Write W1C to clear.
    - PB\_RISING\_EDGE\_DETECTED: PB was released for a time-interval longer than t<sub>PB\_INT\_DEGL</sub> since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK\_INT\_FOR\_PB='0'). Write W1C to clear.
    - PB\_REAL\_TIME\_STATUS: Deglitched (t<sub>PB\_INT\_DEGL</sub>) real-time status of PB pin. Valid only when EN/PB/VSENSE pin is configured as PB. This bit does not assert the nINT pin.
- Power-fail comparator input (VSENSE):
  - Connected to a resistor divider from the supply-line of the pre-regulator, use this pin as a precision enable that senses the supply-voltage to the pre-regulator.
  - The deglitch-time of the VSENSE-pin is configurable by EN\_PB\_VSENSE\_DEGL in MFP\_2\_CONFIG register.

Product Folder Links: TPS65215-Q1



- Power-up is gated by VSYS being above the VSYS<sub>POR Rising</sub>-threshold and the VSENSE input is above the V<sub>VSENSE</sub>-threshold (not deglitched)
- The power-up sequence starts if the VSENSE input rises above V<sub>VSENSE</sub>.
- To signify the power-up based on an EN/PB/VSENSE pin-event, the device sets bit POWER UP FROM EN PB VSENSE in POWER UP STATUS REG register. This bit does not assert the nINT pin. Write W1C to clear the bit.
- The power-down sequence starts if the VSENSE input falls below the V<sub>VSENSE</sub>-threshold for t<sub>DEGL\_VSENSE\_Fall</sub>, to avoid an un-sequenced power-off due to the loss of VSYS-supply-voltage.
- In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power-up sequence if VSENSE input is still above the V<sub>VSENSE</sub>-threshold.
- In case of a cold reset (regardless if by RESET-pin or I2C-request), no renewed on-request is required. The device automatically executes the power-up sequence if VSENSE input is still above the V<sub>VSENSE</sub>threshold.
- OFF-request by I2C-command
  - An I2C-command to I2C\_OFF\_REQ in MFP\_CTRL register triggers an OFF-request.
  - After an OFF-request, a new ON-request is required:
    - In case of EN-configuration, the EN input requires a rising edge (EN considered edge-sensitive)
    - In case of PB-configuration, the PB needs to be pressed for a valid ON-request
    - In case of VSENSE-configuration, the VSENSE input requires a rising edge (VSENSE considered edge-sensitive). Trigger a valid ON-request by power cycling the pre-regulator.
    - The falling-edge deglitch time for EN or VSENSE configuration  $t_{DEGL\ EN/VSENSE\ I2C}$  is shorter than the deglitch-time for pin-induced OFF-requests (t<sub>DEGL</sub> EN Fall and t<sub>DEGL</sub> VSENSE Fall). The deglitch-times for PB-configuration remain.
- First Supply detection (FSD)
  - First Supply detection (FSD) allows power-up as soon as supply voltage is applied, even if EN/PB/ VSENSE pin is at OFF\_REQ status.
  - Use FSD in combination with any ON-request configuration, EN, PB or VSENSE.
  - Enable FSD by setting PU\_ON\_FSD bit in MFP\_2\_CONFIG.
  - At first power-up the EN/PB/VSENSE pin is treated as if the pin had a valid ON request.
  - Once VSYS is above the VSYS<sub>POR Rising</sub>-threshold, the PMIC
    - · loads the EEPROM
    - enters INITIALIZE state
    - perform the discharge-check
    - initiates the power-up-sequence, regardless of the EN/PB/VSENSE-pin-state.
  - To signify the power-up based on FSD, the device sets bit POWER UP FROM FSD in POWER UP STATUS REG register. The nINT-pin does not toggle based on this bit. Write W1C to clear
  - Thereafter, the EN/PB/VSENSE-pin is treated as if the pin had a valid ON-request, until we enter ACTIVE state (at the expiration of the last slot in the power-up-sequence).
  - After that the device adheres to post-deglitch EN/PB/VSENSE-pin-status: if pin status has changed prior to entering ACTIVE state or in ACTIVE state, the device does adhere to the pin state. For example, if the EN/PB/VSENSE-pin is configured for EN, the device does power down in case the EN-pin is low (for longer than the deglitch time) at the time the device enters ACTIVE state.
  - The duration for how long the ON-request is considered valid, regardless of the pin-state, is controlled by the length of the nRSTOUT slot (and any empty slots thereafter), as the PMIC enters ACTIVE state only after the last slot of the sequence expired.

#### 6.3.4 Reset to SoC (nRSTOUT)

The reset output (nRSTOUT) is an open-drain output, intended to release the reset to the SoC or FPGA at the end of the power-up sequence. The timing for nRSTOUT is configured in the sequence. nRSTOUT is driven low until the device enters ACTIVE state or when powering-down from ACTIVE- or STBY-state. The pin is driven high during ACTIVE- and STBY-state.



## 6.3.5 Buck Converters (Buck1, Buck2, and Buck3)

The TPS65215-Q1 integrates three buck converters. Buck1 is capable of supporting up to 3.5 A and Buck2/Buck3 are capable of supporting up to 1.5A of load current. The buck converters have an input voltage range from 2.5V to 5.5V. Connect the input voltage of the buck converters either directly to the system power or to the output of another buck converter. The output voltage is programmable in the range of 0.6V to 3.4V: in 25mV-steps up to 1.4V, in 100mV-steps between 1.4V and 3.4V.

- The ON/OFF state of the buck converters in ACTIVE state is controlled by the corresponding BUCKx\_EN bit in the ENABLE\_CTRL register.
- The ON/OFF state of the buck converters in STBY state is controlled by the corresponding BUCKx\_STBY\_EN bit in the STBY\_1\_CONFIG register.
- In INITIALIZE state, the buck converters are off, regardless of bit-settings.

#### **CAUTION**

In case of buck-regulators that are not to be used at all, the FB\_Bx pin must be tied to GND and the LX\_Bx pin must be left floating.

• Control the converters' activity with the sequencer or through I2C communication.

#### **Buck-switch-modes:**

#### Fixed Frequency Mode

Configure the converters into fixed frequency mode for best EMI-control by setting bit BUCK\_FF\_ENABLE bit in BUCKS\_CONFIG register. If fixed-frequency mode is enabled, the regulators also support optional spread-spectrum. Enable spread-spectrum by setting bit BUCK\_SS\_ENABLE in BUCKS\_CONFIG register. Both of these settings are global for all three buck converters. If fixed-frequency mode is enabled, the regulators support individual out-of-phase switching: configure the phase-relation of the buck rails in 90°-steps relative to the phase of Buck1 by BUCKx\_PHASE\_CONFIG in the BUCKS\_CONFIG register. This bit must only change when this regulator is disabled.

#### Quasi-fixed Frequency Mode

- The converters are operable in forced-PWM mode, irrespective of load-current, or in pulse-frequency-modulation (PFM) mode for low load-currents. The mode is controlled by either the MODE/STBY pin or the MODE/RESET pin if either of those is configured as 'MODE', or by an I2C-command to MODE\_I2C\_CTRL bit in MFP\_1\_CONFIG register (see pin-configuration and I2C-command in 'PWM/PFM and Low Power Modes (MODE/STBY)' and PWM/PFM and Reset (MODE/RESET)' section.
- During a transition to ACTIVE state or to INITIALIZE state, the buck converters are forced to PWM, irrespective of the pin-state. PFM-entry is only allowed when the device enters ACTIVE state, upon completion of the sequence and expiration of the last power-up-slot.
- In case of a DVFS-induced output voltage change, the TPS65215-Q1 temporarily forces the buck-regulators into PWM until the voltage change completed. If PFM is allowed, the entry and exit into PFM is load-current dependent. PFM starts when the inductor current reaches 0A, which is the case at a load current approximately calculated by:
- $I_{LOAD} = \{ [(V_{PVIN Bx} V_{BUCKx}) / L] \times (V_{BUCKx} / V_{PVIN Bx}) \times (1 / f_{SW}) \} / 2$

#### **CAUTION**

The user MUST NOT CHANGE the BUCK\_FF\_ENABLE! The bit is pre-configured by the manufacturer.

- The converters are individually configurable for a high-bandwidth-mode for optimum transient-response or lower bandwidth, allowing minimum output filter capacitance. The selection is done by the BUCKx\_BW\_SEL bits in GENERAL\_CONFIG register and is available for both configurations, fixed-frequency and quasi-fixed-frequency. This bit must only change if this regulator is disabled. Please note the higher output-capacitance requirements for high bandwidth use case!
- If VSEL\_SD/VSEL\_DRR is configured as 'VSEL\_DDR' by the VSEL\_DDR\_SD bit in MFP\_1\_CONFIG
  register, configure the output voltage of Buck3 by pulling the VSEL\_SD/VSEL\_DDR pin high, low or leaving

Product Folder Links: TPS65215-Q1

the pin floating. These settings supports DDR3LV, DDR4, and DDR4LV supply voltages without an EEPROM change.

#### CAUTION

The VSEL DDR-pin needs to be hard-wired and must not change during operation.

- The buck converters have an active discharge function. The discharge function for each rail is configurable as
  enabled of disabled in the DISCHARGE\_CONFIG register. If discharge is enabled, the device discharges the
  output is discharged to ground whenever a rail is disabled.
- Prior to a sequence into ACTIVE state (from INITIALIZE or STBY state), the device discharges the disabled rails regardless of the discharge-configuration to avoid starting into a pre-biased output.
- If a rail is enabled by an I2C-command, active discharge is not enforced, but the rail is only enabled if the output voltage is below the SCG-threshold.
- This register is not EEPROM-backed and does reset if the device enters OFF-state.
- When in INITIALIZE state (during RESET or an I2C-OFF-request), the discharge configuration is not reset.
   Note: when disabling the discharge function, consider the possibility of the TIMEOUT fault during the power-down-sequence.

All Buck Converters support Dynamic Voltage Frequency Scaling (DVFS). This allows dynamically changing the output-voltage during the operation to optimize the operating voltage for the operation point of the SoC in the lower output voltage range between 0.6V and 1.4V. The voltage change is controlled by writing to BUCK1\_VOUT respectively BUCK2\_VOUT or BUCK3\_VOUT registers. During a DVFS-induced voltage transition, the active discharge function is temporarily enabled, irrespective of the discharge-configuration.

#### **Output Capacitance Requirements**

The buck converters require sufficient output-capacitance for stability. The required minimum and supported maximum capacitance depends on the configuration:

- for fixed-frequency, low-bandwidth configuration, a minimum capacitance of 12uF is required and a maximum total capacitance of 36uF is supported
- for quasi-fixed-frequency, low-bandwidth configuration, a minimum capacitance of 10uF is required and a maximum total capacitance of 75uF is supported
- for fixed-frequency, high-bandwidth configuration, a minimum capacitance of 48uF is required and a maximum total capacitance of 144uF is supported
- for quasi-fixed-frequency, high-bandwidth configuration, a minimum capacitance of 30uF is required and a maximum total capacitance of 220uF is supported

## **Buck Fault Handling**

The TPS65215-Q1 detects undervoltages on the buck converter outputs. The reaction to the detection of an
undervoltage is dependent on the configuration of the respective BUCKx\_UV bit and the MASK\_EFFECT
bit in INT\_MASK\_BUCKS. If not masked, the device sets bit INT\_BUCK\_1\_2\_IS\_SET respectively
INT\_BUCK\_3\_IS\_SET bit in INT\_SOURCE register and bit BUCKx\_UV in INT\_BUCK\_1\_2 respectively
INT\_BUCK\_3 register.

During a voltage transition (for example, when triggered by a DVFS induced voltage change), the device blanks the undervoltage detection by default and activates the undervoltage detection when the voltage transition completed.

If the device detects an undervoltage during the sequence into ACTIVE state (from INITIALIZE or STBY) and UV is not masked, the power-down-sequence starts at the end of the current slot.

If the device detects an undervoltage in ACTIVE-state or STBY-state and UV is not masked, the power-down sequence starts immediately. OC-detection is not maskable.

The TPS65215-Q1 provides cycle-by-cycle current-limit on the buck converter outputs. If the device detects
over-current for t<sub>DEGLITCH\_OC\_short</sub>, respectively for t<sub>DEGLITCH\_OC\_long</sub> (configurable individually per rail with
EN\_LONG\_DEGL\_FOR\_OC\_BUCKx in OC\_DEGL\_CONFIG register; applicable for rising-edge only), the
device sets INT\_BUCK\_1\_2\_IS\_SET respectively INT\_BUCK\_3\_IS\_SET bit in INT\_SOURCE register and



bit BUCKx\_OC (for positive over-current) respectively BUCKx\_NEG\_OC (for negative over-current) in INT\_BUCK\_1\_2 respectively INT\_BUCK\_3 register.

During a voltage transition (for example, when triggered by a DVFS induced voltage change), the over current detection is blanked and only gets activated when the voltage transition is completed.

If the over-current occurs during the sequence into ACTIVE state (from INITIALIZE or STBY), the device disables the affected rail immediately and starts the power-down-sequence at the end of the current slot.

If the over-current occurs in ACTIVE-state or STBY-state, the device disables the affected rail immediately and starts the power-down sequence.

OC-detection is not maskable, but the deglitch-time is configurable. TI strongly recommends to use t<sub>DEGLITCH OC short</sub>. Extended over-current leads to increased aging or overshoot upon recovery.

The TPS65215-Q1 detects short-to-ground (SCG) faults on the buck-outputs. The reaction to the detection
of an SCG event is to set INT\_BUCK\_1\_2\_IS\_SET respectively INT\_BUCK\_3\_IS\_SET bit in INT\_SOURCE
register and bit BUCKx\_SCG in INT\_BUCK\_1\_2 respectively INT\_BUCK\_3 register. The affected rail is
disabled immediately. The device sequences down all outputs and transitions into the INITIALIZE state.

SCG-detection is not maskable.

If a rail gets enabled, the device blanks SCG detection initially to allow the rail to ramp above the SCG-threshold.

- The TPS65215-Q1 detects residual voltage (RV) faults on the buck-outputs. The reaction to the detection
  of an RV event is to set INT\_RV\_IS\_SET bit in INT\_SOURCE register and bit BUCKx\_RV in INT\_RV
  register. The RV-detection is not maskable, but the nINT-reaction is globally configurable for all rails by
  MASK\_INT\_FOR\_RV in INT\_MASK\_WARM register. The BUCKx\_RV-flag is set regardless of masking,
  INT\_RV\_IS\_SET bit is only set if nINT is asserted. The fault-reaction time and potential state-transition
  depends on the situation when residual voltage is detected:
  - If the device detects residual voltage during an ON-request in the INITIALIZE state, the device gates
    power-up and the device remains in INITIALIZE state. If the RV-condition exists for more than 4ms to
    5ms, the device sets BUCKx\_RV-bit. If the RV-condition is not present any more, the device transitions to
    ACTIVE state.
  - If the device detects residual voltage during power-up, ACTIVE\_TO\_STANDBY, or STANDBY\_TO\_ACTIVE sequences, the sequence is aborted and the device powers down.
  - If the device detects residual voltage for more than 80ms on any rail that was disabled during STBY state during a request to leave STBY state, the device transitions into INITIALIZE state. The device sets the BUCKx RV-bit if the condition persists for 4ms to 5ms, but less than 80ms.
  - If the device detects residual voltage during power-up, ACTIVE\_TO\_STANDBY, or STANDBY\_TO\_ACTIVE sequences, the sequence is aborted and the device powers down.
  - If residual voltage is detected during an EN-command of the rail by I2C, the BUCKx\_RV-flag is set immediately, but no state transition occurs.
- The buck converters have a local over-temperature sensor. The reaction to a temperature warning is dependent on the configuration of the respective SENSOR\_x\_WARM\_MASK bit in MASK\_CONFIG register and the MASK\_EFFECT bits in INT\_MASK\_BUCKS register. If the temperature at the sensor exceeds Twarm and is not masked, the device sets INT\_SYSTEM\_IS\_SET bit in INT\_SOURCE register and SENSOR\_x\_WARM bit in INT\_SYSTEM register. In case the sensor detects a temperature exceeding Thot\_Rising, the converters power dissipation and junction temperature exceeds safe operating value. The device powers down all active outputs immediately and sets INT\_SYSTEM\_IS\_SET bit in INT\_SOURCE register and SENSOR\_x\_HOT bit in INT\_SYSTEM register. The TPS65215-Q1 automatically recovers once the temperature drops below the Twarm\_Falling threshold value (or below the Thot\_Falling threshold value in case T\_WARM is masked). The \_HOT bit remains set and needs to be cleared by writing '1'. The HOT-detection is not maskable.

Product Folder Links: TPS65215-Q1



#### **CAUTION**

The buck only supplies output currents up to the respective current limit, including during start-up. Depending on the charge-current into the filter- and load-capacitance, the device is potentially unable to drive the full output current to the load while ramping. For a total load-capacitance exceeding  $50\mu F$ , the load current must not exceed approximately 25% of the rated output current. This limit applies also for dynamic output-voltage changes.

#### CAUTION

The TPS65215-Q1 does not offer differential feedback pins. The device does not support remote sensing. To minimize noise in the single-ended sense trace, minimize the trace length from the respective FB pin to the direct connection at the output filter.

**Table 6-1. BUCK Output Voltage Settings** 

BUCKx_VSET [decimal]	BUCKx_VSET [binary]	BUCKx_VSET [hexadecimal]	VOUT (Buck1 & Buck2 and Buck3) [V]
0	000000	00	0.600
1	000001	01	0.625
2	000010	02	0.650
3	000011	03	0.675
4	000100	04	0.700
5	000101	05	0.725
6	000110	06	0.750
7	000111	07	0.775
8	001000	08	0.800
9	001001	09	0.825
10	001010	0A	0.850
11	001011	ОВ	0.875
12	001100	0C	0.900
13	001101	0D	0.925
14	001110	0E	0.950
15	001111	0F	0.975
16	010000	10	1.000
17	010001	11	1.025
18	010010	12	1.050
19	010011	13	1.075
20	010100	14	1.100
21	010101	15	1.125
22	010110	16	1.150
23	010111	17	1.175
24	011000	18	1.200
25	011001	19	1.225
26	011010	1A	1.250
27	011011	1B	1.275
28	011100	1C	1.300
29	011101	1D	1.325
30	011110	1E	1.350
31	011111	1F	1.375
32	100000	20	1.400



Table 6-1, BUCK Output Voltage Settings (continued)

BUCKx_VSET [decimal]	BUCKx_VSET [binary]	BUCKx_VSET [hexadecimal]	VOUT (Buck1 & Buck2 and Buck3) [V]
33	100001	21	1.500
34	100010	22	1.600
35	100011	23	1.700
36	100100	24	1.800
37	100101	25	1.900
38	100110	26	2.000
39	100111	27	2.100
40	101000	28	2.200
41	101001	29	2.300
42	101010	2A	2.400
43	101011	2B	2.500
44	101100	2C	2.600
45	101101	2D	2.700
46	101110	2E	2.800
47	101111	2F	2.900
48	110000	30	3.000
49	110001	31	3.100
50	110010	32	3.200
51	110011	33	3.300
52	110100	34	3.400
53	110101	35	3.400
54	110110	36	3.400
55	110111	37	3.400
56	111000	38	3.400
57	111001	39	3.400
58	111010	3A	3.400
59	111011	3B	3.400
60	111100	3C	3.400
61	111101	3D	3.400
62	111110	3E	3.400
63	111111	3F	3.400

#### 6.3.5.1 Dual Random Spread Spectrum (DRSS)

The bucks provide a digital spread spectrum which reduces the EMI of the power supply over a wide frequency range. Setting BUCK\_SS\_ENABLE to 1 enables the spread spectrum on all three bucks. Spread Spectrum is only applicable if the bucks are configured for fixed frequency, BUCK\_FF\_ENABLE set to 1. The internal modulator dithers the internal clock when the spread spectrum is enabled.

DRSS (a) combines a low-frequency triangular modulation profile (b) with a high frequency cycle-by-cycle random modulation profile (c). The low frequency triangular modulation improves performance in lower radio frequency bands (for example, the AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example, the FM band). In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled. See Figure 6-4 as an example of the modulation.



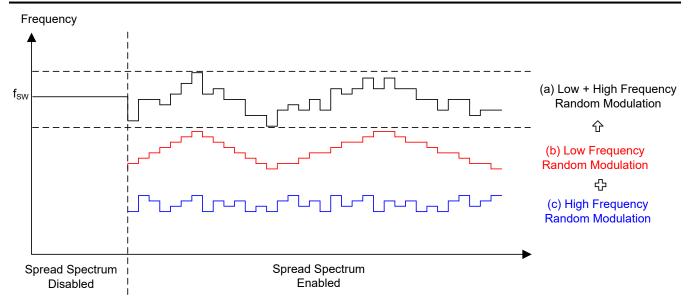


Figure 6-4. Dual Random Spread Spectrum

### 6.3.6 Linear Regulators (LDO1 and LDO2)

The TPS65215-Q1 offers a total of two linear regulators, LDO1 and LDO2.

#### LDO1: 400mA, 0.6V .. 3.4V

LDO1 is a general-purpose LDO intended to provide power to analog circuitry on the SOC or peripherals. The LDO has an input voltage range from 1.5V to 5.5V, and must be connected either directly to the system power or to the output of another converter. The output voltage is programmable in the range of 0.6V to 3.4V in 50mV-steps. The LDO supports up to 400mA. The LDO is configurable to operate in bypass-mode, acting as load-switches. If configured in bypass-mode, the desired output voltage still needs to be specified in LDOx\_VOUT register. The LDOs also support output-voltage changes while enabled, supporting functions like SD-card-IO-supply, changing from 3.3V to 1.8V after initialization, either in LDO-mode at a supply-voltage above 3.3V or with a 3.3V supply changing between bypass-mode and LDO-mode. The LDO also supports Load-switch mode (LSW\_mode): in this case, output voltages of 1.5V up to 5.5V are supported. The desired voltage does not need to be configured in the LDOx\_VOUT register.

- In case of SD-card-supply, control LDO1 by the VSEL\_SD/VSEL\_DDR pin, configured as VSEL\_SD. The polarity of the pin is configurable via VSEL\_SD\_POLARITY bit in MFP\_1\_CONFIG register.
  - Alternatively, an I2C communication to VSEL\_SD\_I2C\_CTRL in MFP\_1\_CONFIG register controls the change of the LDO1 output voltage.
- The LDO is operable as a linear regulator, or in bypass-mode, or as a load-switch (LSW-mode). The mode is configured by LDOx\_LSW\_CONFIG and LSW\_BYP\_CONFIG bits in LDOx\_VOUT register.

#### **CAUTION**

If the LDO is configured in bypass-mode, the output voltage must be configured and the PVIN\_LDOx supply voltage must match the configured output voltage. PVIN\_LDOx voltage must be within (configured VOUT) and (configured VOUT + 200mV). Violation of this impacts the LDO's stability.

In bypass- or LSW-mode, the LDO acts as a switch, where VOUT is VIN minus the drop over the FET-resistance ( $R_{BYPASS}$ ,  $R_{LSW}$ ).

## **Output Capacitance Requirements**

The LDO1 regulator requires sufficient output-capacitance for stability. The required minimum and supported maximum capacitance depends on the configuration:



- in LDO-mode, a minimum capacitance of 1.6 uF is required and a maximum total load capacitance (output filter and point-of-load combined) of 20 uF is supported
- in LSW- or bypass-mode, a minimum capacitance of 1.6 uF is required and a maximum total capacitance (output filter and point-of-load combined) of 50 uF is supported

## LDO2: 300mA, 1.2V .. 3.3V

LDO2 is a general-purpose LDOs intended to provide power to analog circuitry on the SoC or peripherals. The LDO has an input voltage range from 2.2V to 5.5V, connected either directly to the system power or to the output of another converter. Note, the LDO needs a headroom between VSYS and the LDO-output voltage of minimum 150mV. The output voltage is programmable in the range of 1.2V to 3.3V in 50 mV-steps. The LDO supports up to 300mA. The LDO is configurable to act as a load-switch. In this case, output voltages of 2.2V up to 5.5V are supported. The desired voltage does not need to be configured in the LDOx\_VOUT register.

The LDO supports a fast-ramp-mode with limited output capacitance and a slow-ramp-mode, allowing for larger total load capacitance.

#### **Output Capacitance Requirements**

The LDO2 regulator requires sufficient output-capacitance for stability. The required minimum and supported maximum capacitance depends on the configuration:

- for slow-ramp LDO-mode or LSW-mode, a minimum capacitance of 1.6 uF is required and a maximum total capacitance (output filter and point-of-load combined) of 30 uF is supported
- for fast-ramp LDO-mode or LSW-mode, a minimum capacitance of 1.6 uF is required and a maximum total capacitance (output filter and point-of-load combined) of 15 uF is supported

#### LDO1 and LDO2

- The ON/OFF state of the LDOs in ACTIVE state is controlled by the corresponding LDOx\_EN bit in the ENABLE CTRL register.
- The ON/OFF state of the LDOs in STBY state is controlled by the corresponding LDOx\_STBY\_EN bit in the STBY 1 CONFIG register.
- In INITIALIZE state, the LDOs are off, regardless of bit-settings.

### **CAUTION**

In case of linear regulators that are not to be used at all, the VLDOx pin must be left floating.

Each of the LDOs is configurable as a linear regulator or load-switch (LSW-mode). LDO1 is also
operable in bypass-mode. The mode is configured by LDOx\_LSW\_CONFIG and LSW\_BYP\_CONFIG bits
in LDOx\_VOUT register individually per regulator.

#### CAUTION

A mode change between LDO(/bypass) and LSW-mode must only be performed, when the regulator is disabled!

(A change between LDO and bypass-mode (supported by LDO1 only) is supported during operation.)

- The LDOs have an active discharge function. Whenever LDOx is disabled, the output is discharged
  to ground. The discharge function for each rail is configurable as enabled of disabled in the
  DISCHARGE CONFIG register.
- Prior to a sequence into ACTIVE state (from INITIALIZE or STBY state), the device discharges the disabled rails regardless of the discharge-configuration to avoid starting into a pre-biased output.
- If a rail is enabled by an I2C-command, active discharge is not enforced, but the rail is only enabled if the output voltage is below the SCG-threshold.
- This register is not EEPROM-backed and is reset if the device enters OFF-state.
- When in INITIALIZE state (during RESET or an I2C-OFF-request), the discharge configuration is not reset.
   Note: when disabling the discharge function, consider the possibility of the TIMEOUT fault during the power-down-sequence.

Product Folder Links: TPS65215-Q1



#### **LDO Fault Handling**

The TPS65215-Q1 detects undervoltages on the LDO-outputs. The reaction to the detection of an undervoltage is dependent on the configuration of the LDOx\_UV\_MASK bit in INT\_MASK\_LDOS register and the MASK\_EFFECT in INT\_MASK\_BUCKS register. If not masked, the device sets bit INT\_LDO\_1\_IS\_SET respectively INT\_LDO\_2\_IS\_SET bit in INT\_SOURCE register and bit LDOx\_UV in INT\_LDO\_1 register respectively INT\_LDO\_2 register.

During a voltage transition (at power-up or triggered by toggling VSEL\_SD-pin or an I2C-command), the device blanks the undervoltage detection by default and activates the undervoltage detection when the voltage transition completed.

If the device detects an undervoltage during the sequence into ACTIVE state (from INITIALIZE or STBY) and UV is not masked, the power-down-sequence starts at the end of the current slot.

If the device detects an undervoltage in ACTIVE-state or STBY-state and UV is not masked, the power-down sequence starts immediately. OC-detection is not maskable.

#### **CAUTION**

If a LDO is configured in bypass-mode or LSW-mode, UV-detection is not supported.

The TPS65215-Q1 provides current-limit on the LDO-outputs. If the PMIC detects over-current
for t<sub>DEGLITCH\_OC\_short</sub>, respectively for t<sub>DEGLITCH\_OC\_long</sub> (configurable individually per rail with
EN\_LONG\_DEGL\_FOR\_OC\_LDOx in OC\_DEGL\_CONFIG register; applicable for rising-edge only), the
device sets INT\_LDO\_1\_IS\_SET respectively INT\_LDO\_2\_IS\_SET bit in INT\_SOURCE register and bit
LDOx\_OC in INT\_LDO\_1 respectively INT\_LDO\_2 register. The effected rail is disabled immediately.

During a voltage transition (at power-up or triggered by toggling VSEL\_SD-pin or an I2C-command), the overcurrent detection is blanked and gets activated when the voltage transition completed.

If the over-current occurs during the sequence into ACTIVE state (from INITIALIZE or STBY), the device disables the affected rail immediately and starts the power-down-sequence at the end of the current slot.

If the over-current occurs in ACTIVE-state or STBY-state, the device disables the affected rail immediately and starts the power-down sequence.

OC-detection is not maskable, but the deglitch-time is configurable. TI strongly recommends to use  $t_{\text{DEGLITCH}\ OC\ \text{short}}$ . Extended over-current leads to increased aging or overshoot upon recovery.

 The TPS65215-Q1 detects short-to-ground (SCG) faults on the LDO-outputs. The reaction to the detection of an SCG event is to set INT\_LDO\_1\_IS\_SET respectively INT\_LDO\_2\_IS\_SET bit in INT\_SOURCE register and bit LDOx\_SCG in INT\_LDO\_1 register respectively INT\_LDO\_2 register. The affected rail is disabled immediately. The device sequences down all outputs and transitions into INTIALIZE state.

SCG-detection is not maskable.

If a rail gets enabled, the device blanks SCG detection initially to allow the rail to ramp above the SCG-threshold.

- The TPS65215-Q1 detects residual voltage (RV) faults on the LDO-outputs. The reaction to the detection
  of an RV event is to set INT\_RV\_IS\_SET bit in INT\_SOURCE register and bit LDOx\_RV in INT\_RV
  register. The RV-detection is not maskable, but the nINT-reaction is globally configurable for all rails
  by MASK\_INT\_FOR\_RV in INT\_MASK\_WARM register. The device sets the LDOx\_RV-flag regardless of
  masking, INT\_RV\_IS\_SET bit is only set if nINT is asserted. The fault-reaction time and potential statetransition depends on the situation when the faults are detected:
  - If the device detects residual voltage during an ON-request in the INITIALIZE state, the PMIC gates power-up and the device remains in INITIALIZE state. If the RV-condition is detected for more than 4ms to 5ms, the device sets the LDOx\_RV-bit but remains in INITIALIZE state as long as the RV-condition exists. If the RV-condition is not present any more, the device transitions to ACTIVE state, provided the ON-request is still valid.



- If the device detects residual voltage during power-up, ACTIVE\_TO\_STANDBY, or STANDBY TO ACTIVE sequences, the sequence is aborted and the device powers down.
- If the device detects residual voltage for more than 80ms on any rail that was disabled during STBY state during a request to leave STBY state, the device transitions into INITIALIZE state. The device sets the LDOx RV-bit if the condition persists for 4ms to 5ms, but less than 80ms.
- If the device detects residual voltage during power-up, ACTIVE\_TO\_STANDBY, or STANDBY\_TO\_ACTIVE sequences, the sequence is aborted and the device powers down.
- If the device detects residual voltage during an EN-command of the rail by I2C, the LDOx\_RV-bit is set immediately, but no state transition occurs.
- The LDOs have a local over-temperature sensor. The reaction to a temperature warning is dependent on the configuration of the respective SENSOR\_x\_WARM\_MASK bit in and the MASK\_EFFECT bit in INT\_MASK\_BUCKS register. If the temperature at the sensor exceeds T<sub>WARM\_Rising</sub> and is not masked, the device sets INT\_SYSTEM\_IS\_SET bit in INT\_SOURCE register and SENSOR\_x\_WARM bit in INT\_SYSTEM register. In case the sensor detects a temperature exceeding T<sub>HOT\_Rising</sub>, the converters power dissipation and junction temperature exceeds safe operating value. The device powers down all active outputs immediately and sets INT\_SYSTEM\_IS\_SET bit in INT\_SOURCE register and SENSOR\_x\_HOT bit in INT\_SYSTEM register. The TPS65215-Q1 automatically recovers once the temperature drops below the T<sub>WARM\_FAlling</sub> threshold value (or below the T<sub>HOT\_FAlling</sub> threshold value in case T\_WARM is masked). The HOT bit remains set and needs to be cleared by writing '1'. The HOT-detection is not maskable.

Table 6-2. LDO output voltage settings

LDOx_VSET [decimal]		LDOx_VSET [hexadecimal]	VOUT (LDO1, LDO mode) [V]	VOUT (LDO1, bypass-mode) [V]	VOUT (LDO2, LDO mode) [V]
0	000000	00	0.60	reserved	1.20
1	000001	01	0.65	reserved	1.20
2	000010	02	0.70	reserved	1.20
3	000011	03	0.75	reserved	1.20
4	000100	04	0.80	reserved	1.20
5	000101	05	0.85	reserved	1.20
6	000110	06	0.90	reserved	1.20
7	000111	07	0.95	reserved	1.20
8	001000	08	1.00	reserved	1.20
9	001001	09	1.05	reserved	1.20
10	001010	0A	1.10	reserved	1.20
11	001011	ОВ	1.15	reserved	1.20
12	001100	0C	1.20	reserved	1.20
13	001101	0D	1.25	reserved	1.25
14	001110	0E	1.30	reserved	1.30
15	001111	0F	1.35	reserved	1.35
16	010000	10	1.40	reserved	1.40
17	010001	11	1.45	reserved	1.45
18	010010	12	1.50	1.50	1.50
19	010011	13	1.55	1.55	1.55
20	010100	14	1.60	1.60	1.60
21	010101	15	1.65	1.65	1.65
22	010110	16	1.70	1.70	1.70
23	010111	17	1.75	1.75	1.75

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated



Table 6-2. LDO output voltage settings (continued)

LDOx_ VSET [decimal]	LDOx_VSET [binary]	LDOx_ VSET [hexa-decimal]	VOUT (LDO1, LDO mode) [V]	VOUT (LDO1, bypass-mode) [V]	VOUT (LDO2, LDO mode) [V]
24	011000	18	1.80	1.80	1.80
25	011001	19	1.85	1.85	1.85
26	011010	1A	1.90	1.90	1.90
27	011011	1B	1.95	1.95	1.95
28	011100	1C	2.00	2.00	2.00
29	011101	1D	2.05	2.05	2.05
30	011110	1E	2.10	2.10	2.10
31	011111	1F	2.15	2.15	2.15
32	100000	20	2.20	2.20	2.20
33	100001	21	2.25	2.25	2.25
34	100010	22	2.30	2.30	2.30
35	100011	23	2.35	2.35	2.35
36	100100	24	2.40	2.40	2.40
37	100101	25	2.45	2.45	2.45
38	100110	26	2.50	2.50	2.50
39	100111	27	2.55	2.55	2.55
40	101000	28	2.60	2.60	2.60
41	101001	29	2.65	2.65	2.65
42	101010	2A	2.70	2.70	2.70
43	101011	2B	2.75	2.75	2.75
44	101100	2C	2.80	2.80	2.80
45	101101	2D	2.85	2.85	2.85
46	101110	2E	2.90	2.90	2.90
47	101111	2F	2.95	2.95	2.95
48	110000	30	3.00	3.00	3.00
49	110001	31	3.05	3.05	3.05
50	110010	32	3.10	3.10	3.10
51	110011	33	3.15	3.15	3.15
52	110100	34	3.20	3.20	3.20
53	110101	35	3.25	3.25	3.25
54	110110	36	3.30	3.30	3.30
55	110111	37	3.35	3.35	3.30
56	111000	38	3.40	3.40	3.30
57	111001	39	3.40	3.40	3.30
58	111010	ЗА	3.40	3.40	3.30
59	111011	3B	3.40	3.40	3.30
60	111100	3C	3.40	3.40	3.30
61	111101	3D	3.40	3.40	3.30



## Table 6-2. LDO output voltage settings (continued)

LDOx_ VSET [decimal]	LDOx_VSET [binary]			VOUT (LDO1, bypass-mode) [V]	VOUT (LDO2, LDO mode) [V]
62	111110	3E	3.40	3.40	3.30
63	111111	3F	3.40	3.40	3.30

#### 6.3.7 Interrupt Pin (nINT)

During power-up, the output of the nINT pin does depend on whether any INT\_SOURCE flags are set and the configuration of the MASK EFFECT bit in INT MASK BUCKS register-. If one or more flags are set, then nINT pin is pulled low and is only released high after those flags have been cleared by writing '1' to them. Note, the nINT-pin only transitions 'high' if a VIO-voltage for the pull-up is available.

In ACTIVE or STBY state, the nINT pin signals any event or fault condition to the host processor. Whenever a fault or event occurs in the IC, the corresponding interrupt bit is set in the INT register, and the open-drain output is driven low. In case the device transitions to INITIALIZE state, the nINT pin is pulled low as well, regardless if the transition is triggered by an OFF-request or a fault.

If the fault is no longer present, a W1C (write '1' to clear) needs to be performed on the failure bits. This command also allows the nINT-pin to release (return to Hi-Z state).

If a failure persists, the corresponding bit remains set and the INT pin remains low.

The UV-faults are individually maskable per rail in INT MASK UV registers. The thermal sensors are individually maskable by SENSOR x WARM MASK in the MASK CONFIG register. The effect of the masking for UV and WARM is defined globally by MASK EFFECT bits in MASK CONFIG register.

The nINT reaction for RV-faults is defined globally by MASK INT FOR RV bits in MASK CONFIG register.

- 00b = no state change, no nINT reaction, no bit set
- 01b = no state change, no nINT reaction, bit set
- 10b = no state change, nINT reaction, bit set (same as 11b)
- 11b = no state change, nINT reaction, bit set (same as 10b)

#### **CAUTION**

Masking poses a risk to the device or the system. In case the masking is performed by I2Ccommand, the masking bits do get reset to EEPROM-based default after transitioning to INITIALIZE state. Bits corresponding to faults newly configured via I2C as SD-faults do not get cleared.

It is strongly discouraged to mask OC- and UV-detection on the same rail.

#### 6.3.8 PWM/PFM and Low Power Modes (MODE/STBY)

The TPS65215-Q1 supports low power modes through the I2C-control or through the MODE/STBY pin. The configuration of the pin is selected by MODE STBY CONFIG in MFP 2 CONFIG register. Configure the polarity of this pin by writing to MODE STBY POLARITY in MFP 1 CONFIG register. The polarity-configuration must not change after power-up. Only either MODE/RESET or MODE/STBY must be configured as MODE. If both are configured as MODE, MODE/RESET takes priority and MODE/STBY is ignored.

#### MODE/STBY configured as 'MODE':

- If configured as 'MODE', the pin-status determines the switching-mode of the buck-converters. This selection is only applicable in quasi-fixed-frequency mode.
- Forcing this pin for longer than toped tree forces the buck-regulators into PWM-mode (irrespective of load current). De-asserting this pin low allows the buck regulators to enter PFM-mode. The entry into PFM and exit from PFM is governed by the load current. Only one pin, either MODE/STBY or MODE/RESET must be configured as 'MODE'.

Product Folder Links: TPS65215-Q1

- Control the selection of auto-PFM/forced-PWM by writing to the bit MODE I2C CTRL in MFP 1 CONFIG reaister.
- A change of the MODE does not cause a state-transition.
- During power-up of any one of the three bucks, a MODE change is blanked on this rail and only takes effect after the ramp completed.

## MODE/STBY configured as 'STBY':

- Forcing this pin for longer than t<sub>DEGLITCH\_MFP</sub> sequences down the rails selected to turn off in the STBY\_1\_CONFIG respectively the STBY\_2\_CONFIG register. De-asserting this pin sequences the selected rails on again.
- Another method to transition into and out of STBY state is writing to the bit STBY I2C CTRL in MFP CTRL register, provided I2C communication is supported during STBY state.
- A change of the MODE/STBY pin configured as 'STBY' does cause a state-transition by definition.
- Regardless of the pin-setting, the device always powers up into ACTIVE state. The device reacts to the STBY-pin-state or I2C-commands only after entering ACTIVE state.

## MODE/STBY configured as 'MODE & STBY':

- The pin is configurable to perform both functions, MODE and STBY simultaneously
- Forcing this pin for longer than  $t_{\mathsf{DEGLITCH\_MFP}}$  sequences down the rails selected to turn off in the STBY\_1\_CONFIG respectively the STBY\_2\_CONFIG register and allows auto-PFM entry (only applicable in quasi-fixed-frequency mode). De-asserting this pin sequences the selected rails on again and forces the buck-regulators to forced-PWM. Polarity settings need to be harmonized for this configuration.
- If a transition into and out of STBY state is commanded by writing to the bit STBY I2C CTRL in MFP CTRL register (provided I2C communication is supported during STBY state), a separate command for the MODEchange is required by writing to the bit MODE\_I2C\_CTRL in MFP\_1\_CONFIG register.
- A change of the MODE/STBY pin configured as 'MODE&STBY' does cause a state-transition by definition.
- By default STBY is deasserted and the pin is ignored until the device completed the power-up-sequence. During power-up of any one of the three bucks, a MODE-change is blanked on this rail and only takes effect after the ramp completed. A state-change commanded by STBY-pin is reacted to even during the ramp of rails (except during INITIALIZE-to-ACTIVE transition).

Please see below truth-table for pin- and I2C-commands.

Table 6-3. MODE/STBY Configuration

	Pin Configuration (MODE_STBY_CON FIG)	Pin Polarity (MODE_STBY_POL ARITY)	Pin state (schematic)	I2C control (MODE_I2C_CTRL)	Resulting Function
MODE/STBY	MODE	x	x	1h	forced PWM
MODE/STBY	MODE	0h	L	0h	auto-PFM
MODE/STBY	MODE	0h	Н	0h	forced PWM
MODE/STBY	MODE	1h	L	0h	forced PWM
MODE/STBY	MODE	1h	Н	0h	auto-PFM
MODE/STBY	STBY	0	L	х	STBY
MODE/STBY	STBY	0	Н	х	ACTIVE
MODE/STBY	STBY	1	L	х	ACTIVE
MODE/STBY	STBY	1	Н	х	STBY

#### 6.3.9 PWM/PFM and Reset (MODE/RESET)

This pin is configurable as an alternative MODE pin (in case MODE/STBY is configured for STBY-function) or as a RESET pin. The configuration of the pin is selected by MODE\_RESET\_CONFIG in MFP\_2\_CONFIG register. Configure the polarity of this pin by writing to MODE RESET POLARITY in MFP 1 CONFIG register. The SLVSHQ9 – JUNE 2025



polarity-configuration must not change after power-up. Only MODE/RESET or MODE/STBY must be configured as MODE. If both are configured as MODE, MODE/RESET takes priority and MODE/STBY is ignored.

#### MODE/RESET configured as 'MODE':

- If configured as 'MODE', the pin-status determines the switching-mode of the buck-converters. This selection is only applicable in quasi-fixed-frequency mode.
- Forcing this pin for longer than t<sub>DEGLITCH\_MFP</sub> forces the buck-regulators into PWM-mode (irrespective of load current). De-asserting this pin low allows the buck regulators to enter PFM-mode. The entry into PFM and exit from PFM is governed by the load current. Only one pin, either MODE/STBY or MODE/RESET must be configured as 'MODE'.
- Another method to control the selection of auto-PFM/forced-PWM is writing to the bit MODE\_I2C\_CTRL in MFP 1 CONFIG register.
- A change of the MODE does not cause a state-transition.
- During power-up of any one of the three bucks, a MODE-change is blanked on this rail and only takes effect after the ramp completed.

#### MODE/RESET configured as 'RESET':

- In RESET configuration, this pin is edge sensitive, but still applies the deglitch time. Consequently, toggling this pin and holding the pin for longer than t<sub>DEGLITCH</sub> RESET causes a reset.
- By default, RESET is deasserted and RESET requests, via pin or I2C, are only serviced if the device is in ACTIVE state, STBY state, or transitions between these 2 states.
- The TPS65215-Q1 supports WARM or COLD reset. The configuration is made by bit WARM\_COLD\_RESET\_CONFIG in MFP\_2\_CONFIG register.
  - If configured for COLD reset, the device executes the power down sequence and transitions to INITIALIZE state. Then, EEPROM is reloaded and rails power-up again in normal power-up-sequence, provided there are no faults and no OFF-request. The execution of a COLD-reset sets the bit COLD\_RESET\_ISSUED in POWER\_UP\_STATUS\_REG register. The read-out of this bit allows to track if a COLD-reset was performed. The bit gets set regardless if the reset was commanded by I2C or by the pin. The nINT-pin does not toggle based on this bit. Write W1C to clear the bit.
  - If configured for WARM reset, all enabled rails remain on, but the output voltage of rails that support
    dynamic voltage change is reset to the boot-voltage. Specifically, following configurations get reset to
    the respective boot-values: BUCK1\_VSET, BUCK2\_VSET, BUCK3\_VSET, LDO1\_VSET, LDO2\_VSET,
    LDO1\_BYP\_CONFIG, LDO2\_BYP\_CONFIG and VSEL\_SD\_I2C\_CTRL.

All other bits, even in the same register, remain at the respective state. For example, LDOx\_LSW\_CONFIG, BUCKx\_BW\_SEL, BUCKx\_UV\_THR\_SEL and the MFP\_1\_CONFIG register bits do NOT get reset during a WARM-reset.

WARM Reset doesnot override the VSEL\_SD-pin command. In other words: even if a WARM Reset occurs, if the VSEL\_SD pin is commanding 1.8V-LDO mode, that remain in effect.

Writing to the bit WARM\_RESET\_I2C\_CTRL respectively the bit COLD\_RESET\_I2C\_CTRL in MFP\_CTRL register also triggers a reset.

### Note

Shut-down-faults and OFF-requests take priority over a RESET-request. If a RESET-requests occurs simultaneously with one of those, the device enters INITIALIZE state and requires a new ON-request to start up.

Reset requests, via pin or I2c, are only serviced in ACTIVE state, STBY state, or a transition between these two states.

Please see below truth-table for pin- and I2C-commands.

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated



## Table 6-4. MODE/RESET Configuration

	Pin Configuration (MODE_RESET_CO NFIG)	Pin Polarity (MODE_RESET_POL ARIT Y)	Pin state (schematic)	I2C control (MODE_I2C_CTRL)	Resulting Function
MODE/RESET	MODE*	x	x	1h	forced PWM
MODE/RESET	MODE*	0h	L	0h	auto-PFM
MODE/RESET	MODE*	0h	Н	0h	forced PWM
MODE/RESET	MODE*	1h	L	0h	forced PWM
MODE/RESET	MODE*	1h	Н	0h	auto-PFM
MODE/RESET	RESET	0	L	х	RESET
MODE/RESET	RESET	0	Н	х	normal operation
MODE/RESET	RESET	1	L	х	normal operation
MODE/RESET	RESET	1	Н	х	RESET

The \* for MODE indicates that the MODE/RESET pin takes priority in case both, MODE/RESET and MODE/STBY are configured as 'MODE', and thus the respective pin to be observed is MODE/RESET.

### 6.3.10 Voltage Select Pin (VSEL\_SD/VSEL\_DDR)

The function of this pin is configured by VSEL\_DDR\_SD in MFP\_1\_CONFIG.

When configured as VSEL\_SD, LDO1 is controlled by the pin. The configuration must not change after power-up.

## VSEL\_SD/VSEL\_DDR configured as 'VSEL\_SD': SD-card-IO-select:

Configure the polarity of this pin by writing to VSEL\_SD\_POLARITY in MFP\_1\_CONFIG register. Toggling the pin changes the output voltage of the selected LDO between hard-coded 1.8V and the voltage configured in LDOx\_VOUT. For the SD-card-IO-supply, LDOx\_VOUT must be configured for 3.3V. A change of the VSEL\_SD status does not cause a state-transition.

## **CAUTION**

In SD-card-configuration, customer must configure the pin-polarity and drive the pin so that the LDO delivers 3.3V at start-up.

## VSEL\_SD/VSEL\_DDR configured as 'VSEL\_DDR':

Pulling this pin high sets the output voltage of Buck3 to 1.35V (DDR3LV), leaving the pin floating sets the output voltage of Buck3 to 1.2V (DDR4, LP-DDR3, some LP-DDR2), pulling the pin low sets the output voltage of the Buck3 voltage configured in BUCK3 VOUT. For LP-DDR4, BUCK3 VOUT must be configured to 1.1V.

#### **CAUTION**

This function needs to be hard-wired and must not change during operation.

#### **CAUTION**

When using an I2C-command to toggle LDO1 for the SD-card, LDO1 must be configured in the application to supply the SD-card-IO-voltage. The VSEL\_SD\_POLARITY bit has no effect if the pin is configured as VSEL\_DDR.

The Table below shows the various combinations.



## Table 6-5. VSEL\_SD/VSEL\_DDR Configuration Options

Pin Configuration (VSEL_DDR_SD)	Pin Polarity (VSEL_SD_POLARITY)	Rail selection	PIN state (schematic)	I2C control (VSEL_SD_I2C_ CTRL)	Resulting Function
DDR	n/a	LDO1 (via I2C control)	L	0h: LDOx = 1.8V 1h: LDOx = LDOx_VSET	BUCK3 = Buck3_VSET
DDR	n/a	LDO1 (via I2C control)	open	0h: LDOx = 1.8V 1h: LDOx = LDOx_VSET	BUCK3 = 1.2V
DDR	n/a	LDO1 (via I2C control)	Н	0h: LDOx = 1.8V 1h: LDOx = LDOx_VSET	BUCK3 = 1.35
SD	0	LDO1	L	х	LDO1 = 1.8V (LDO mode)
SD	0	LDO1	Н	х	LDO1 = LDO1_VSET
SD	1	LDO1	L	x	LDO1 = LDO1_VSET
SD	1	LDO1	Н	x	LDO1 = 1.8V (LDO mode)

## 6.3.11 General Purpose Inputs or Outputs (GPO1, GPO2, and GPIO)

GPO1 and GPO2 pins are always configured as an output.

The GPIO-pin is an input/output, however, the input-functionality is only used in multi-PMIC configuration. In single-PMIC configuration, the pin is typically used as an output. Read the state by polling the bit GPIO\_STATUS bit in MFP\_CTRL register.

The I/O-configuration of the GPIO-pin is done by the MULTI DEVICE ENABLE bit in MFP 1 CONFIG register.

If configured as outputs, these pins are able to sequence external rails. Include the GP(I)Os in the power sequence, or control them via I2C-interface, writing to GPOx\_EN respectively GPIO\_EN bit in GENERAL CONFIG register. The GPO is released high if activated.

The GPIO function is to be used if multiple TPS65215-Q1 need to be synchronized, in case more rails need to be supplied. See application section on usage. See section "Multi-PMIC operation" for details.

The polarity of these pins is not changeable.

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated



### 6.3.12 I<sup>2</sup>C-Compatible Interface

The default  $I^2C1$  7-bit device address of the TPS65215-Q1 is set to 0x30 (0b0110000 in binary), but is changeable if needed, for example for multi-PMIC-operation.

The I<sup>2</sup>C-compatible synchronous serial interface provides access to the configurable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a controller or a target depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. The TPS65215-Q1 supports standard mode (100kHz), fast mode (400kHz), and fast mode plus (1MHz) when VIO is 3.3V or 1.8V.

## 6.3.12.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line must only be changed when clock signal is LOW.

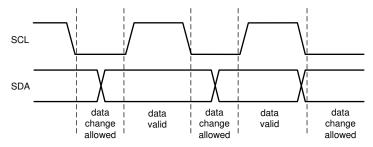


Figure 6-5. Data Validity Diagram

#### 6.3.12.2 Start and Stop Conditions

The device is controlled through an I<sup>2</sup>C-compatible interface. START and STOP conditions classify the beginning and end of the I<sup>2</sup>C session. A START condition is defined as the SDA signal going from HIGH to LOW while the SCL signal is HIGH. A STOP condition is defined as the SDA signal going from LOW to HIGH while the SCL signal is HIGH. The I<sup>2</sup>C controller device always generates the START and STOP conditions.

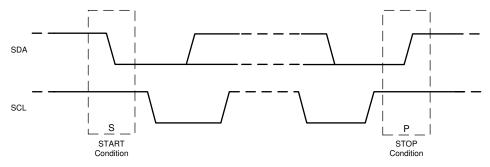


Figure 6-6. Start and Stop Sequences

The  $I^2C$  bus is considered busy after a START condition and free after a STOP condition. The  $I^2C$  controller device is permitted to generate repeated START conditions during data transmission. A START and a repeated START condition are equivalent function-wise. Figure 6-7 shows the SDA and SCL signal timing for the  $I^2C$ -compatible bus. For timing values, see the *Specification* section.

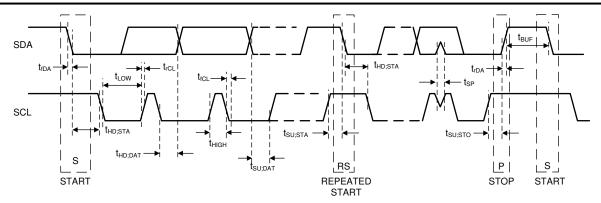


Figure 6-7. I<sup>2</sup>C-Compatible Timing

### 6.3.12.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the controller device. The controller device releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the controller device is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the target device. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the controller device), but the SDA line is not pulled down.

After the START condition, the bus controller device sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register. Figure 6-8 shows an example bit format of device address 110000-Bin = 60Hex.

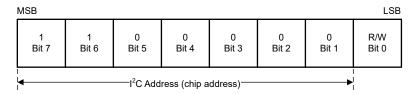


Figure 6-8. Example Device Address

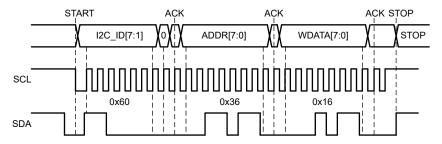
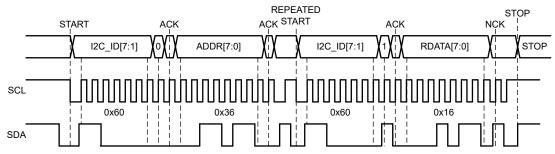


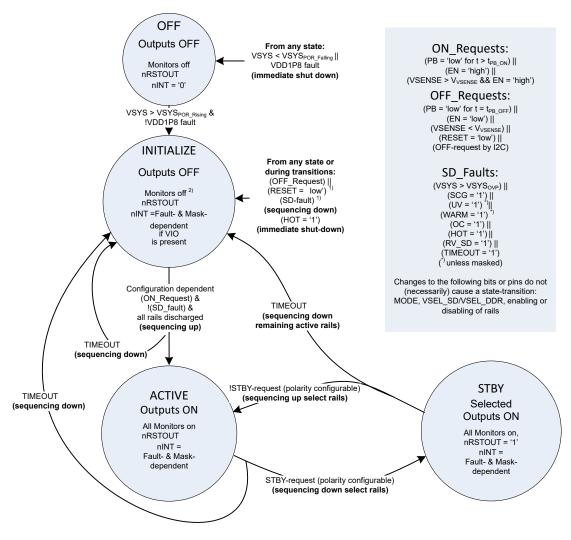
Figure 6-9. I<sup>2</sup>C Write Cycle Without CRC



When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 6-10. I<sup>2</sup>C Read Cycle Without CRC

#### 6.4 Device Functional Modes



- 1) in case of a RESET or a SD-fault, the device transitions from INITIALIZE state to the ACTIVE state without a new Push-button-ON\_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.
- 2) If INITIALIZE state was entered due to a Thermal-Shut-Down, the temperature monitors remain active until the temperature on all sensors fell below T<sub>WARM</sub> threshold. Thermal-Shut-Down causes immediate shut-shutdown, no sequencing down

Figure 6-11. State Diagram

SLVSHQ9 - JUNE 2025



## 6.4.1 Modes of Operation

#### 6.4.1.1 OFF State

In OFF state, the PMIC is insufficiently supplied. Neither internal logic nor external rails are available. If VSYS exceeds VSYS\_POR voltage and the internal 1.8V-rail (VDD1P8) is in regulation, the device enters the INITIALIZE state.

#### 6.4.1.2 INITIALIZE State

In INITIALIZE state, the device is completely shut down with the exception of a few circuits to monitor the EN/PB/VSENSE input. Whenever entering the INITIALIZE state, the PMIC reads the memory and loads the registers to their EEPROM-default values. The I<sup>2</sup>C communication interface is turned off.

Entry to INITIALIZE state is gated if any one of the thermal sensors is above the  $T_{WARM\_Rising}$  threshold and WARM-detection is not masked.

The EEPROM loading takes approximately 2.3ms. The power-up sequence begins after the EEPROM-load and if all rails are discharged below the  $V_{BUCKx\ SCG\ TH}$  respectively  $V_{LDOx\ SCG\_TH}$  threshold.

If INITIALIZE state was entered from OFF state, bit POWER\_UP\_FROM\_OFF in POWER\_UP\_STATUS\_REG register is set and remains set until a write-1-clear is issued. Read-out of this bit allows to determine if INITIALZE state was entered from OFF state or due to a Shut-down-fault or OFF-request.

In INITIALIZE state, the nINT pin status is dependent if faults are and masking thereof. If no faults are present or nINT-reaction for those are masked, nINT-pin is pulled high, provided a VIO-voltage for the pull-up is available.

To transition from the INITIALIZE state to the ACTIVE state, one of the ON-requests must occur:

- The EN input is 'high' (if EN/PB/VSENSE is configured as 'EN' or 'VSENSE')
- The PB input is pulled low for at least t<sub>PB\_ON\_SLOW</sub> respectively t<sub>PB\_ON\_FAST</sub> (if EN/PB/VSENSE is configured as 'PB')

#### Note

The DISCHARGE\_CONFIG register is purposefully omitted from RESET when entering INITIALIZE state from ACTIVE or STBY state. When entering INITIALIZE state from OFF state, the EEPROM content is loaded. If the discharge configuration changed after power-up, a different start-up behavior occurs, depending if the INITIALIZE state was entered from OFF state or from ACTIVE/STBY.

## 6.4.1.3 ACTIVE State

The ACTIVE state is the normal mode of operation when the system is up and running. All enabled buck converters and LDOs are operational and controllable through the I2C interface. After a wake-up event, the PMIC discharges potential residual voltages on the outputs, regardless of the discharge-configuration. ACTIVE state is directly enterable from STBY state by de-asserting the STBY pin high or by an I2C command. See STBY state description for details. To transition to STBY, the STBY pin must be forced or an I2C command to STBY I2C CTRL in MFP CTRL register must be issued.

To transition to INITIALIZE state, one of the following OFF\_Requests must occur:

- The EN input is 'low' (if EN/PB/VSENSE is configured as 'EN' or 'VSENSE')
- The PB input is pulled low for at least t<sub>PB OFF</sub> (if EN/PB/VSENSE is configured as 'PB')
- An I2C OFF-request is issued

If a shut-down-fault (SD\_Fault) occurs while in the ACTIVE state, TPS65215-Q1 sequences down the active outputs and transition to the INITIALIZE state. The device does transition to ACTIVE state without a new Push-button-ON\_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.

### 6.4.1.4 STBY State

STBY state is a low-power mode of operation intended to support system standby. Enter this mode by the MODE/STBY pin, if configured as 'STBY' or by an I2C-command to STBY\_I2C\_CTRL in MFP\_CTRL

Product Folder Links: TPS65215-Q1



register. Typically, the majority of power rails are turned off with the exception of rails required by the SoC during this state. The power rails that remain on in STBY state are configurable in STBY\_1\_CONFIG and STBY\_2\_CONFIG register.

The monitoring functions are all available: Undervoltage- (UV), Short-to-GND- (SCG) and Over-current- (OC) detection, thermal warning (WARM) and thermal-shutdown (TSD/HOT) remain active.

The device enters ACTIVE state if STBY is de-asserted or an I2C command is received (provided VIO-supply remained active). Before starting the STBY to ACTIVE sequence, disabled rails are discharged. In case this fails to complete within 80ms, the device also runs into a timeout-condition and transitions to INITIALIZE state. The device sets bit TIMEOUT in the INT\_TIMEOUT\_RV\_SD register and the fault flags for the rail that caused the shut-down.

The sequence into and out of STBY state is the same as for power-down respectively for power-up. Rails that remain on in STBY are skipped, but the respective slots for those rails are still executed.

#### **CAUTION**

The device must first enter ACTIVE state before STBY, and is not capable of transitioning from INITIALIZE state to STBY state directly.

#### CAUTION

The device does not turn on previously disabled rails in STBY-state. Activity in STBY-state requires a AND-combination of LDOx EN / BUCKx EN and LDOx STBY EN/BUCKx STBY EN.

#### **CAUTION**

Do not change the registers related to an ongoing sequence by I2C-command!

Non-NVM-bits are not accessible for approximately 80us after starting a transition into INITIALIZE state.

## 6.4.1.5 Fault Handling

#### **Detectable Faults**

The TPS65215-Q1 offers various fault-detections. Per default, all of them lead to a sequenced shut-down. Some of them are maskable and the reaction to masked faults is configurable.

The device provides the following fault-detections on the supply voltage (VSYS) and internal voltage supply (VDD1P8):

- Undervoltage on VSYS, resulting in transition to OFF state or gating start-up
- Overvoltage-protection on VSYS, resulting in transition to OFF state
- Under- or Overvoltage on internal 1.8V-supply (VDD1P8), resulting in transition to OFF state or gating start-up.

None of these faults are maskable.

The TPS65215-Q1 provides the following fault-detections on the buck- and LDO-outputs:

- Undervoltage detection (UV)
- Over Current detection (OC), triggering on positive as well as (for buck-converters) negative current-limit
- Short-to-GND detection (SCG)
- Temperature warning (WARM) and Thermal Shut Down (TSD / HOT)
- Residual Voltage (RV) and Residual Voltage Shutdown (RV\_SD)
- Timeout (TO)



SCG, OC, HOT, RV\_SD and TO are not maskable. If any one of those occurs, the device powers down. Positive and negative current limit share the same mask-bit per regulator.

The reaction to UV, RV and WARM faults is configurable. If not masked, a fault triggers a sequenced shut-down. UV, RV and WARM are maskable individually per regulator in INT\_MASK\_BUCKS, INT\_MASK\_LDOS and INT\_MASK\_WARM registers. No state-transition occurs in case of a masked fault. Whether bits are set and if nINT is pulled low are globally configurable by MASK\_EFFECT bits in MASK\_CONFIG register. Positive and negative current limit share the same mask-bit per regulator.

- 00b = no state change, no nINT reaction, no bit set
- 01b = no state change, no nINT reaction, bit set
- 10b = no state change, nINT reaction, bit set (same as 11b)
- 11b = no state change, nINT reaction, bit set (same as 10b)

For any fault that corresponds to a shut-down condition, the fault-bit remains asserted until a W1C (write-one-clear) operation is performed via I2C (assuming the fault is not present any more). In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power up sequence if the fault is no longer present as long as EN/VSENSE is still high and no PB-press is required for a restart.

For any fault that is not a shut-down condition (for example because the fault is masked), the bit is cleared when going to the INITIALIZE state.

#### Thermal Warning and Shutdown

There are two thermal thresholds: Thermal-warning (WARM) and Thermal Shutdown (TSD / HOT).

- Thermal Warning, WARM-threshold:
- if the temperature exceeds T<sub>WARM\_Rising</sub> threshold, the SENSOR\_x\_WARM-bit is set and the PMIC sequences down (unless masked).
- if the temperature fell below T<sub>WARM\_Falling</sub> threshold, the device powers up again, without a new Push-button-ON\_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.
- if the temperature exceeds T<sub>WARM\_Rising</sub> threshold, but SENSOR\_x\_WARM\_MASK bit is /bits are set, the PMIC remains in ACTIVE state. Fault-reporting occurs as configured by MASK\_EFFECT bits. The processor makes the decision to either sequence the power down or throttles back on the running applications to reduce the power consumption and hopefully avoiding a Thermal Shutdown situation.
- Thermal Shutdown, HOT-threshold, applicable if WARM-threshold is masked:
- if the temperature exceeds T<sub>HOT\_Rising</sub> threshold, the SENSOR\_x\_HOT-bit is set and the PMIC powers off all rails immediately. This power down is simultaneously and not sequenced.
- in case ALL sensors are masked for WARM-detection (all SENSOR\_x\_WARM\_MASK bits are set), the PMIC does power back up once the temperature drops below the T<sub>HOT\_Falling</sub> threshold, provided a valid ON-request is present.
- in case any one of the sensors is unmasked for WARM-detection, the PMIC does power back up once the temperature drops below the T<sub>WARM\_Falling</sub> threshold, without a new Push-button-ON\_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.

## **Residual Voltage**

Residual voltage checks are performed at various occasions: before starting the INITIALIZE- to ACTIVE-transition and any time before a rail is enabled, regardless if during the sequence, by I2C-command or during the STBY- to ACTIVE-transition. RV-checks are also performed during the sequences, to detect if a rail that is supposed to be disabled is pulled up by another rail. The treatment of RV-faults depends on the situation when the fault occurs:

- INITIALIZE to ACTIVE:
  - if residual voltage is detected for more than 4ms to 5ms prior to the execution of the sequence, the respective INT\_RV\_IS\_SET bit in INT\_SOURCE register and LDOx\_RV respectively BUCKx\_RV bit in

Product Folder Links: TPS65215-Q1

INT\_RV register is set and remains set, even if the discharge is successful at a later time and the ON-request is executed.

if the residual voltage is detected during the sequence, this constitutes a shutdown-fault: the
device initiates the power-down-sequence at the end of the slot-duration. The device sets the
respective INT\_TIMEOUT\_RV\_SD\_IS\_SET bit in INT\_SOURCE register, LDOx\_RV\_SD respectively
BUCKx\_RV\_SD bit and bit TIMEOUT in INT\_TIMEOUT\_RV\_SD register.

## ACTIVE to STBY:

- if active discharge is enabled and residual voltage is detected after eight times the power-down slot-duration, this constitutes a shutdown-fault: the device sequences down at the end of the slot. The device sets INT\_TIMEOUT\_RV\_SD\_IS\_SET bit in INT\_SOURCE register, the LDOx\_RV\_SD respectively BUCKx\_RV\_SD bit and the bit TIMEOUT in INT\_TIMEOUT\_RV\_SD register.
- if the residual voltage is detected during the sequence, this constitutes a shutdown-fault: the device sequences down at the end of the slot-duration and sets bit INT\_TIMEOUT\_RV\_SD\_IS\_SET in INT\_SOURCE register and LDOx\_RV\_SD respectively BUCKx\_RV\_SD bit in INT\_TIMEOUT\_RV\_SD register.

#### STBY to ACTIVE:

- if residual voltage is detected prior to the execution of the sequence for more than 4ms to 5ms, the
  device sets INT\_RV\_IS\_SET bit in INT\_SOURCE register and LDOx\_RV respectively BUCKx\_RV bit in
  INT\_RV register. The bit remains set, even if the discharge is successful before timeout expires and the
  STBY-to-ACTIVE-sequence is executed.
- if residual voltage is detected for more than 80ms prior to the execution of the sequence, this constitutes
  a shutdown-fault: the device sequences down and sets the bit INT\_TIMEOUT\_RV\_SD\_IS\_SET in
  INT\_SOURCE register and LDOx\_RV\_SD respectively BUCKx\_RV\_SD bit in INT\_TIMEOUT\_RV\_SD
  register. In addition, the device sets the bit TIMEOUT in INT\_TIMEOUT\_RV\_SD register.
- if the residual voltage is detected during the sequence, this constitutes a shutdown-fault: the device sequences down at the end of the slot-duration and sets the INT\_TIMEOUT\_RV\_SD\_IS\_SET bit in INT\_SOURCE register and LDOx\_RV\_SD respectively BUCKx\_RV\_SD bit in INT\_TIMEOUT\_RV\_SD register. The TIMEOUT bit is not set in this case.

## ACTIVE to INITIALIZE or STBY to INITIALIZE

if the residual voltage is detected at the end of the power-down slot-duration of the respective rail,
 this gates the disabling of the subsequent rail for up to eight times the slot-duration, but then the power-sequence continues regardless of the residual voltage. No bit is set in this case.

## MASKING of RV-bits

- the reaction of the nINT-pin reaction in case of residual voltage detection is maskable for LDOx\_RV respectively BUCKx\_RV bits by MASK\_INT\_FOR\_RV bit in MASK\_CONFIG register.
- neither the bit nor the shutdown-fault-reaction in case of residual voltage detection is maskable for LDOx\_RV\_SD respectively BUCKx\_RV\_SD bits.

## Timeout

Timeout occurs if residual voltage is not discharged in time. The bit TIMEOUT in INT\_TIMEOUT\_RV\_SD register is set. See details above.

#### Note

In case active discharge on a rail is disabled, the unsuccessful discharge of that rail within the slot duration does not gate the disable of the subsequent rail.

During power-down, the device sets neither RV-bits nor RV\_SD-bits for rails with disabled discharge.

#### **CAUTION**

For every detected Shut-Down fault, irrespective if prior to the sequence due to unsuccessful discharge, during the power-up-sequence or in ACTIVE or STBY state, the retry counter (RETRY\_COUNT in POWER\_UP\_STATUS\_REG register) is incremented. The device attempts two retries to power-up. If both fail, a power-cycle on VSYS is required to reset the retry counter. Any successful power-up also resets the retry counter.

If faults are masked and do not cause a shut-down, the retry counter does not increment.

To disable the retry-counter, set bit MASK\_RETRY\_COUNT in INT\_MASK\_UV register. When set, the device attempts to retry infinitely.

Below table gives an overview of the fault-behavior in ACTIVE and STBY states if unmasked and whether a fault is maskable.

#### **CAUTION**

Masking of faults poses a risk to the device or the system, including but not limited to starting into a pre-biased output.

TI strongly recommends not to mask OC- and UV-detection on the same rail.

#### Table 6-6. Fault Handling

Block	Fault	ACTIVE or STBY state (if fault NOT masked)	ACTIVE or STBY state (if fault IS masked)
BUCK & LDO	Residual voltage - shutdown- Fault - RV_SD *)	Fault triggers a sequenced shut- down to INITIALIZE state	Not maskable
BUCK & LDO	Residual voltage - RV	Fault does not trigger state- change	Fault does not trigger state-change
BUCK & LDO	Timeout - TO *)	Fault triggers a sequenced shut- down to INITIALIZE state	Fault does not trigger state-change
BUCK & LDO	Undervoltage - UV	Fault triggers a sequenced shut- down to INITIALIZE state	Fault does not trigger state-change
BUCK & LDO	Overcurrent - OC	Fault triggers a sequenced shut- down to INITIALIZE state	Not maskable
BUCK & LDO	Short-to-GND - SCG	Fault triggers a sequenced shut- down to INITIALIZE state	Not maskable
BUCK & LDO	Temperature warning - WARM	Fault triggers a sequenced shut- down to INITIALIZE state	Yes
BUCK & LDO	Temperature shut-down - HOT	Fault triggers an immediate shut-down to INITIALIZE state (not sequenced)	Not maskable
VSYS	Undervoltage - UV	Fault triggers an immediate shut-down to OFF state (not sequenced)	Not maskable
VSYS	Overvoltage - OV	Fault triggers an immediate shut-down to OFF state (not sequenced)	Not maskable

Product Folder Links: TPS65215-Q1



#### Table 6-6. Fault Handling (continued)

Block		ACTIVE or STBY state (if fault NOT masked)	ACTIVE or STBY state (if fault IS masked)
VDD1P8	Undervoltage or Overvoltage - UV or OV	Fault triggers an immediate shut-down to OFF state (not sequenced)	Not maskable

<sup>\*)</sup> RV\_SD and TIMEOUT faults only occur during a sequence

## 6.5 Multi-PMIC Operation

The GPIO (pin#16) is an input/output digital pin, however, the input-functionality is only used in multi-PMIC configuration. This pin behaves as GPO (general purpose output) when configured for single PMIC and behaves as GPIO (general purpose input-output) when configured for multi-device. Set this configuration on register field MULTI\_DEVICE\_ENABLE (address 0x1F). When configured for "multi-device", GPIO allows to synchronize the power-up and power-down sequence of multiple TPS65215-Q1 devices for applications requiring additional rails. The GPIO pin is used to indicate the status of each PMIC to maintain each in the same state and sequence slot. At the beginning of each sequence slot, all the TPS65215-Q1 PMICs drive GPIO pin low. After the sequence slot duration finishes, and all rails for that slot have reached the UV threshold, device releases the GPIO pin. Once both devices release the GPIO high, the internal sequencers advance to the next sequence slot together. Since both PMICs are always in the same power-up or power-down slot, multiple rails from each PMIC are synchronized to the same sequence slot. Figure 6-12 shows an example PDN of two TPS65215-Q1 devices sharing the same input supply (VSYS), EN pin and GPIO for multi-PMIC operation.

## Requirements When Synchronizing Multiple TPS65215-Q1 PMICs

- The GPIO from each PMIC must be tied together, sharing the same pull-up resistor. The pull-up resistance needs to be chosen to meet the maximum allowable rise-time t<sub>RISE\_GPIO</sub> in combination with the capacitance on the GPIO-line to allow for synchronization.
- The EN/PB/VSENSE pin must be tied together sharing the same external ON request. This pin must have the same configuration (same pin config, deglitch, FSD).
- All the TPS65215-Q1 PMICs must share the same VSYS supply.
- Each of the TPS65215-Q1 PMICs must have a different I2C address if connected to the same I2C bus.
  The I2C address for the second PMIC is changeable on register field I2C\_ADDRESS. Once the address
  is changed, the new value must be stored permanently into the NVM. Refer to NVM Programming for
  programming instructions.

Copyright © 2025 Texas Instruments Incorporated



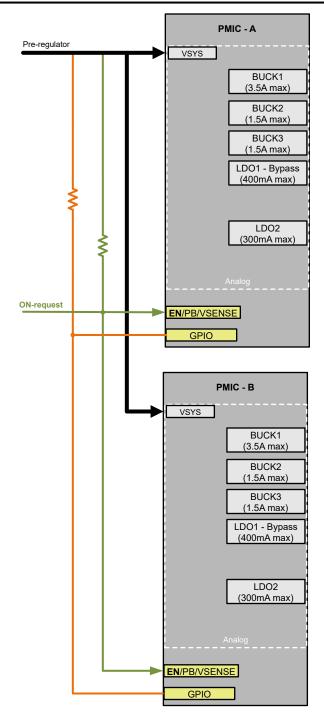


Figure 6-12. Multi-PMIC Configuration Example

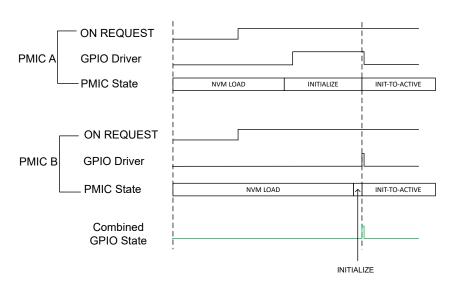
#### Note

- The synchronization-times between the PMICs add to the slot-duration-timeout described in the Power-up and Power-Down sections: If power-up fails, the timeout tTIMEOUT\_UV\_SLOT occurs 3ms to 4ms later in multi-PMIC-configurations. If power-down fails due to discharge failing, the timeout occurs 20ms to 26ms later in multi-PMIC configurations.
- GPIO\_EN and GPIO\_STBY\_EN bits are ignored in multi-PMIC configuration.



Figure 6-13 shows the synchronization between two PMICs in Initialize state, before the power-up sequence is executed. While in INITIALIZE state, before the ON request is received, devices hold GPIO low. GPIO is only released when the ON request is received. The external signal driving the ON request must be connected to EN/PB/VSENSE pin of both devices. The PMICs proceed to execute the power-up sequence once both devices are in INITIALIZE state and both devices have received the ON request. This technique enables both devices start the power-up sequence at the same time, even if the respective internal boot-up times are different.

On request before devices are in INITIALIZE:



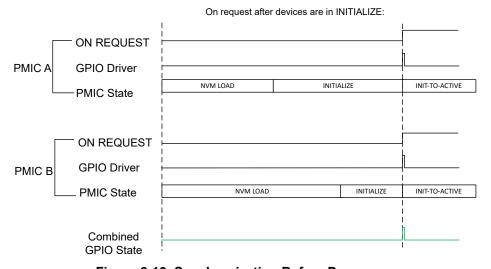


Figure 6-13. Synchronization Before Power-up

Figure 6-14 shows the synchronization between two PMICs during the power-up sequence. An open-drain GPIO is connected between both PMICs, and used as an indicator that the sequence slot has finished for the device. At the beginning of each sequence slot, both PMICs pull down this GPIO. After the device slot timer has expired, and all rails for that slot have reach UV threshold, the GPIO is released high. The combined GPIO goes high when both PMICs have released the GPIO. Once both devices release the GPIO high, both PMICs advance to the next sequence slot. Both PMICs are always in the same sequence slot at the same time.



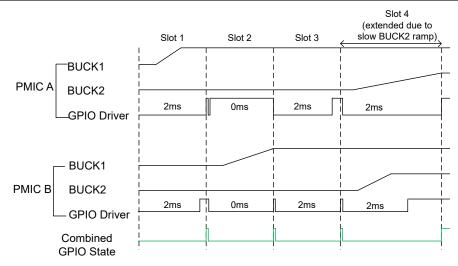


Figure 6-14. Synchronization During Power-up Sequence

Figure 6-15 shows the synchronization between two PMICs when transitioning from Active to Standby. In active or standby, GPIO default state is high. When a device wants to change states, GPIO is driven low for a specific low duration. The low duration determines the type of request. For STANDBY/ACTIVE request, GPIO is set low approximately 38-52us and for OFF request approximately 180-243us. Times are chosen such that devices always see the same state transition, accounting for clock variation and requests happening right after each other. While GPIO is low, devices are counting the time the GPIO remains low. On GPIO rising edge, devices start the state transition based on low duration. If GPIO stays low longer than the timeout duration, the devices indicate a GPIO fault and transition to INITIALIZE state.

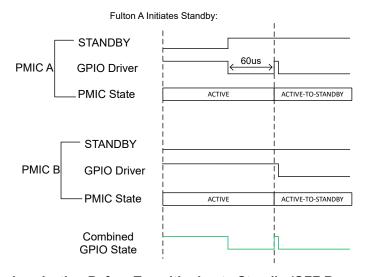


Figure 6-15. Synchronization Before Transitioning to Standby/OFF Request/COLD RESET

Figure 6-16 shows the synchronization between two PMICs during power-down sequence. Power-down sequence works similarly. If active discharge is enabled for a rail, the sequence slot is extended until rail is discharged below SCG threshold, unless the slot timeout occurs or register field BYPASS RAILS DISCHA RGED CHECK is set. If discharge is disabled for all rails in current slot, the actual slot time is only based on selected slot duration. Once the slot duration expires and rails with active discharge are discharged, devices release the GPIO high. Once all devices release GPIO high, they advance to the next power-down step.

Submit Document Feedback Product Folder Links: TPS65215-Q1

62

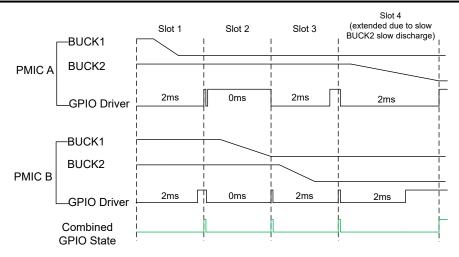


Figure 6-16. Synchronization During Power-down Sequence

Figure 6-17 shows the timeout synchronization between two PMICs. In case of a fault on an output rail, GPIO is not released. After a timeout, device goes to "timeout synchronization" state, and wait for 3ms before setting GPIO high. Once the combined GPIO goes high, both devices start the power-down sequence. For example: If BUCK1 from PMIC A is shorted to GND, after the slot duration expires, the regulator does not have hit UV and GPIO is not released. If Slot#1 duration is 10ms and PMIC A is 10% fast, it only takes 9ms to timeout. After timeout, device goes to timeout-sync state, at which point GPIO is set high after 3ms. PMIC B rails ramp up properly, but a high state on GPIO from PMIC A is initially not detected due to the fault on BUCK1. PMIC B also goes to timeout-sync state and sets GPIO high after 3ms. After the timeout sync of PMIC B, the combined GPIO is high and both PMICs start power-down together.

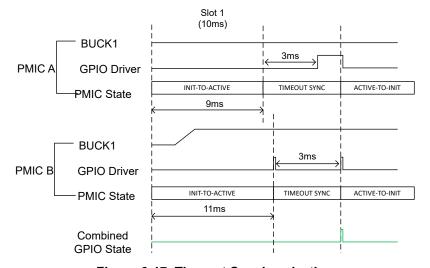


Figure 6-17. Timeout Synchronization

### 6.6 User Registers

The registers up to register 27h, USER\_GENERAL\_NVM\_STORAGE\_REG are backed up by EEPROM. The reset value corresponds to the configuration of the orderable part number and is signified by an 'X' herein. Please refer to the Technical Reference Manual (TRM) of the respective orderable part-number.

The registers 28h through 37h are not EEPROM-backed and reset to the value shown in the register map.

Registers 00h, TI\_DEV\_ID, 01h, NVM\_ID, 28h, MANUFACTURING\_VER and 41h, FACTORY\_CONFIG\_2 are hard-wired and are not changeable by the user.



## 6.7 Device Registers

Table 6-7 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 6-7 should be considered as reserved locations and the register contents should not be modified.

## **Table 6-7. DEVICE Registers**

Offset	Acronym	Register Name	Section
0h	TI_DEV_ID	Device ID	Go
1h	NVM_ID	NVM configuration ID	Go
2h	ENABLE_CTRL	Enable/Push-Button/Vsense Control	Go
3h	BUCKS_CONFIG	Generic Buck Configuration	Go
5h	LDO2_VOUT	LDO2 Configuration	Go
7h	LDO1_VOUT	LDO1 Configuration	Go
8h	BUCK3_VOUT	Buck3 Configuration	Go
9h	BUCK2_VOUT	Buck2 Configuration	Go
Ah	BUCK1_VOUT	Buck1 Configuration	Go
Ch	LDO2_SEQUENCE_SLOT	Power-up and -down slot for LDO2	Go
Eh	LDO1_SEQUENCE_SLOT	Power-up and -down slot for LDO1	Go
Fh	BUCK3_SEQUENCE_SLOT	Power-up and -down slot for Buck3	Go
10h	BUCK2_SEQUENCE_SLOT	Power-up and -down slot for Buck2	Go
11h	BUCK1_SEQUENCE_SLOT	Power-up and -down slot for Buck1	Go
12h	nRST_SEQUENCE_SLOT	Power-up and -down slot for nRSTOUT	Go
13h	GPIO_SEQUENCE_SLOT	Power-up and -down slot for GPIO	Go
14h	GPO2_SEQUENCE_SLOT	Power-up and -down slot for GPO2	Go
15h	GPO1_SEQUENCE_SLOT	Power-up and -down slot for GPO1	Go
16h	POWER_UP_SLOT_DURATION_1	Slot-duration at power-up for slot0-3	Go
17h	POWER_UP_SLOT_DURATION_2	Slot-duration at power-up for slot4-7	Go
18h	POWER_UP_SLOT_DURATION_3	Slot-duration at power-up for slot8-11	Go
19h	POWER_UP_SLOT_DURATION_4	Slot-duration at power-up for slot12-15	Go
1Ah	POWER_DOWN_SLOT_DURATION_1	Slot-duration at power-down for slot0-3	Go
1Bh	POWER_DOWN_SLOT_DURATION_2	Slot-duration at power-down for slot4-7	Go
1Ch	POWER_DOWN_SLOT_DURATION_3	Slot-duration at power-down for slot8-11	Go
1Dh	POWER_DOWN_SLOT_DURATION_4	Slot-duration at power-down for slot12-15	Go
1Eh	GENERAL_CONFIG	LDO-undervoltage and GPO-enable	Go
1Fh	MFP_1_CONFIG	Multi-Function pin configuration1	Go
20h	MFP_2_CONFIG	Multi-Function pin configuration2	Go
21h	STBY_1_CONFIG	STBY configuration LDOs and Bucks	Go
22h	STBY_2_CONFIG	STBY configuration GPIO and GPO	Go
23h	OC_DEGL_CONFIG	Overcurrent deglitch time per rail	Go
24h	INT_MASK_UV	Undervoltage fault-masking	Go
25h	MASK_CONFIG	WARM-masking and mask-effect	Go
26h	I2C_ADDRESS_REG	I2C-address	Go
27h	USER_GENERAL_NVM_STORAGE_REG	User-configurable register (NVM-backed)	Go
28h	MANUFACTURING_VER	Silicon-revision (read-only)	Go
29h	MFP_CTRL	I2C-control for RESET, STBY, OFF	Go
2Ah	DISCHARGE_CONFIG	Discharge configuration per rail	Go
2Bh	INT_SOURCE	Interrupt source	Go
2Ch	INT_LDO_2	OC, UV, SCG for LDO2	Go

**Table 6-7. DEVICE Registers (continued)** 

Table of The Extract Regional (Continuou)				
Offset	Acronym	Register Name	Section	
2Dh	INT_LDO_1	OC, UV, SCG for LDO1	Go	
2Eh	INT_BUCK_3	OC, UV, SCG for Buck3	Go	
2Fh	INT_BUCK_1_2	OC, UV, SCG for Buck1 and Buck2	Go	
30h	INT_SYSTEM	WARM and HOT fault flags	Go	
31h	INT_RV	RV (residual voltage) per rail	Go	
32h	INT_TIMEOUT_RV_SD	RV (residual voltage) per rail causing shut-down	Go	
33h	INT_PB	PushButton status and edge-detection	Go	
34h	USER_NVM_CMD_REG	DIY - user programming commands	Go	
35h	POWER_UP_STATUS_REG	Power-up status and STATE	Go	
36h	SPARE_2	Spare register (not NVM-backed)	Go	
37h	SPARE_3	Spare register (not NVM-backed)	Go	
41h	FACTORY_CONFIG_2	Revision of NVM-configuration (read only)	Go	

Complex bit access types are encoded to fit into small table cells. Table 6-8 shows the codes that are used for access types in this section.

**Table 6-8. Device Access Type Codes** 

Access Type	Code	Description				
Read Type						
R	R	Read				
Write Type						
W	W	Write				
W1C	W 1C	Write 1 to clear				
Reset or Default Value						
-n		Value after reset or the default value				

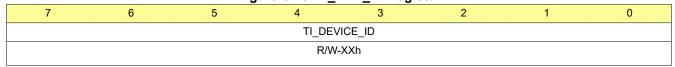


## 6.7.1 TI\_DEV\_ID Register (Offset = 0h) [Reset = XXh]

TI\_DEV\_ID is shown in Figure 6-18 and described in Table 6-9.

Return to the Summary Table.

# Figure 6-18. TI\_DEV\_ID Register



## Table 6-9. TI DEV ID Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	TI_DEVICE_ID	R/W	X	TI_DEVICE_ID[7:6]: 00h = TA: -40°C to 105°C, TJ: -40°C to 125°C 10h = TA: -40°C to 125°C, TJ: -40°C to 150°C TI_DEVICE_ID[5:0]: Device GPN Note: This register can be programmed only by the manufacturer! Refer to Technical Reference Manual / User's Guide for specific numbering and associated configuration. (Default from NVM memory)

Product Folder Links: TPS65215-Q1

Submit Document Feedback

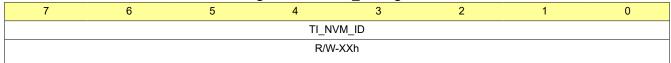


## 6.7.2 NVM\_ID Register (Offset = 1h) [Reset = XXh]

NVM\_ID is shown in Figure 6-19 and described in Table 6-10.

Return to the Summary Table.

# Figure 6-19. NVM\_ID Register



## Table 6-10. NVM\_ID Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	TI_NVM_ID	R/W	X	NVM ID of the IC Note: This register can be programmed only by the manufacturer! Refer to Technical Reference Manual / User's Guide for specific numbering and associated configuration. (Default from NVM memory)



## 6.7.3 ENABLE\_CTRL Register (Offset = 2h) [Reset = XXh]

ENABLE\_CTRL is shown in Figure 6-20 and described in Table 6-11.

Return to the Summary Table.

## Figure 6-20. ENABLE\_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDO2_EN	RESERVED	LDO1_EN	BUCK3_EN	BUCK2_EN	BUCK1_EN
R-0h	R-0h	R/W-Xh	R-0h	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh

## Table 6-11. ENABLE\_CTRL Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	LDO2_EN	R/W	Х	Enable LDO2 regulator (Default from NVM memory) 0h = Disabled 1h = Enabled
4	RESERVED	R	0h	
3	LDO1_EN	R/W	Х	Enable LDO1 regulator (Default from NVM memory) 0h = Disabled 1h = Enabled
2	BUCK3_EN	R/W	Х	Enable BUCK3 regulator (Default from NVM memory) 0h = Disabled 1h = Enabled
1	BUCK2_EN	R/W	Х	Enable BUCK2 regulator (Default from NVM memory) 0h = Disabled 1h = Enabled
0	BUCK1_EN	R/W	Х	Enable BUCK1 regulator (Default from NVM memory) 0h = Disabled 1h = Enabled

Product Folder Links: TPS65215-Q1



## 6.7.4 BUCKS\_CONFIG Register (Offset = 3h) [Reset = XXh]

BUCKS\_CONFIG is shown in Figure 6-21 and described in Table 6-12.

Return to the Summary Table.

## Figure 6-21. BUCKS\_CONFIG Register

7	6	5	4	3	2	1	0
USER_NVM_S PARE_2	USER_NVM_S PARE_1	BUCK_SS_EN ABLE	BUCK_FF_ENA BLE	BUCK3_PH	ASE_CONFIG	BUCK2_PHA	SE_CONFIG
R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/\	N-Xh	R/W	-Xh

# Table 6-12. BUCKS\_CONFIG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	USER_NVM_SPARE_2	R/W	Х	Spare bit in user NVM space (Default from NVM memory)
6	USER_NVM_SPARE_1	R/W	Х	Spare bit in user NVM space (Default from NVM memory)
5	BUCK_SS_ENABLE	R/W	Х	Spread spectrum enabled on Bucks (only applicable in FF-mode) (Default from NVM memory) 0h = Spread spectrum disabled 1h = Spread spectrum enabled
4	BUCK_FF_ENABLE	R/W	X	All Bucks set into fixed frequency mode NOTE: MUST NOT CHANGE AT ANY TIME! (Default from NVM memory) 0h = Quasi-fixed frequency mode 1h = Fixed frequency mode
3-2	BUCK3_PHASE_CONFIG	R/W	X	Phase of BUCK3 clock. Applicable if Bucks are configured for fixed frequency. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)  0h = 0 degrees 1h = 90 degrees 2h = 180 degrees 3h = 270 degrees
1-0	BUCK2_PHASE_CONFIG	R/W	X	Phase of BUCK2 clock. Applicable if Bucks are configured for fixed frequency. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)  0h = 0 degrees 1h = 90 degrees 2h = 180 degrees 3h = 270 degrees



## 6.7.5 LDO2\_VOUT Register (Offset = 5h) [Reset = XXh]

LDO2\_VOUT is shown in Figure 6-22 and described in Table 6-13.

Return to the Summary Table.

## Figure 6-22. LDO2\_VOUT Register



## Table 6-13. LDO2\_VOUT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	LDO2_SLOW_PU_RAMP	R/W	X	LDO2 Power-up ramp When set high, slows down the power-up ramp to ~3ms. Cout max 30uF When set low, ramp time is ~660us. Cout max 15uF (Default from NVM memory) 0h = Fast ramp for power-up (~660us) 1h = Slow ramp for power-up (~3ms)
6	LDO2_LSW_CONFIG	R/W	Х	LDO2 LDO or LSW Mode. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory) 0h = LDO Mode 1h = LSW Mode

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated



Table 6-13. LDO2\_VOUT Register Field Descriptions (continued)

D;4		_		Pr Field Descriptions (continued)
Bit	Field	Туре	Reset	Description
5-0	LDO2_VSET	R/W	X	Voltage selection for LDO2. The output voltage range is from 1.2V to 3.3V. (Default from NVM memory)
				0h = 1.200V
				1h = 1.200V
				2h = 1.200V
				3h = 1.200V
				4h = 1.200V
				5h = 1.200V
				6h = 1.200V 7h = 1.200V
				8h = 1.200V
				9h = 1.200V
				Ah = 1.200V
				Bh = 1.200V
				Ch = 1.200V
				Dh = 1.250V Eh = 1.300V
				Fh = 1.350V
				10h = 1.400V
				11h = 1.450V
				12h = 1.500V
				13h = 1.550V
				14h = 1.600V   15h = 1.650V
				16h = 1.700V
				17h = 1.750V
				18h = 1.800V
				19h = 1.850V
				1Ah = 1.900V
				1Bh = 1.950V
				1Ch = 2.000V 1Dh = 2.050V
				1Eh = 2.100V
				1Fh = 2.150V
				20h = 2.200V
				21h = 2.250V
				22h = 2.300V
				23h = 2.350V 24h = 2.400V
				25h = 2.450V
				26h = 2.500V
				27h = 2.550V
1				28h = 2.600V
1				29h = 2.650V
				2Ah = 2.700V 2Bh = 2.750V
				2Ch = 2.800V
				2Dh = 2.850V
				2Eh = 2.900V
				2Fh = 2.950V
				30h = 3.000V
				31h = 3.050V  32h = 3.100V
				32h = 3.100V 33h = 3.150V
				34h = 3.200V
				35h = 3.250V
				36h = 3.300V
				37h = 3.300V
				38h = 3.300V
1				39h = 3.300V
1				3Ah = 3.300V 3Bh = 3.300V
1				3Ch = 3.300V
				3Dh = 3.300V
				3Eh = 3.300V
1	I	I	I	ı

**TPS65215-Q1**SLVSHQ9 – JUNE 2025



## Table 6-13. LDO2\_VOUT Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
				3Fh = 3.300V



### 6.7.6 LDO1\_VOUT Register (Offset = 7h) [Reset = XXh]

LDO1\_VOUT is shown in Figure 6-23 and described in Table 6-14.

Return to the Summary Table.

### Figure 6-23. LDO1\_VOUT Register



### Table 6-14. LDO1\_VOUT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	LDO1_LSW_CONFIG	R/W	X	LDO1 LDO/Bypass or LSW Mode. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory) 0h = Not Applicable (LDO1 not configured as load-switch) 1h = LDO1 configured as Load-switch
6	LDO1_BYP_CONFIG	R/W		LDO1 LDO or Bypass Mode. (Default from NVM memory) 0h = LDO1 configured as LDO (only applicable if LDO1_LSW_CONFIG 0x0) 1h = LDO1 configured as Bypass (only applicable if LDO1_LSW_CONFIG 0x0)



#### Table 6-14. LDO1 VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	er Field Descriptions (continued) Description
		R/W		
5-0	LDO1_VSET	TX/ V V	X	Voltage selection for LDO1. The output voltage range is from 0.6V to 3.4V in LDO-mode and 1.5V to 3.4V in bypass-mode. (Default from
				NVM memory)
				0h = 0.600V
				1h = 0.650V
				2h = 0.700V
				3h = 0.750V 4h = 0.800V
				5h = 0.850V
				6h = 0.900V
				7h = 0.950V
				8h = 1.000V
				9h = 1.050V
				Ah = 1.100V Bh = 1.150V
				Ch = 1.200V
				Dh = 1.250V
				Eh = 1.300V
				Fh = 1.350V
				10h = 1.400V
				11h = 1.450V   12h = 1.500V
				13h = 1.550V
				14h = 1.600V
				15h = 1.650V
				16h = 1.700V
				17h = 1.750V
				18h = 1.800V  19h = 1.850V
				1Ah = 1.900V
				1Bh = 1.950V
				1Ch = 2.000V
				1Dh = 2.050V
				1Eh = 2.100V
				1Fh = 2.150V 20h = 2.200V
				21h = 2.250V
				22h = 2.300V
				23h = 2.350V
				24h = 2.400V
				25h = 2.450V
				26h = 2.500V 27h = 2.550V
				28h = 2.600V
				29h = 2.650V
				2Ah = 2.700V
				2Bh = 2.750V
				2Ch = 2.800V 2Dh = 2.850V
				2Eh = 2.900V
				2Fh = 2.950V
				30h = 3.000V
				31h = 3.050V
				32h = 3.100V
				33h = 3.150V 34h = 3.200V
				35h = 3.250V
				36h = 3.300V
				37h = 3.350V
				38h = 3.400V
				39h = 3.400V
				3Ah = 3.400V
				3Bh = 3.400V 3Ch = 3.400V
				3Dh = 3.400V
I		l	l	(SEII 0.100 V







#### Table 6-14. LDO1 VOUT Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description		
				3Eh = 3.400V 3Eh = 3.400V		

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback



### 6.7.7 BUCK3\_VOUT Register (Offset = 8h) [Reset = XXh]

BUCK3\_VOUT is shown in Figure 6-24 and described in Table 6-15.

Return to the Summary Table.

### Figure 6-24. BUCK3\_VOUT Register



# Table 6-15. BUCK3\_VOUT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	BUCK3_BW_SEL	R/W	X	BUCK3 Bandwidth selection. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory) 0h = low bandwidth 1h = high bandwidth
6	BUCK3_UV_THR_SEL	R/W	X	UV threshold selection for BUCK3. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated



#### Table 6-15. BUCK3 VOUT Register Field Descriptions (continued)

<b>D</b> **				er Field Descriptions (continued)
Bit	Field	Туре	Reset	Description
5-0	BUCK3_VSET	R/W	X	Voltage selection for BUCK3. The output voltage range is from 0.6V
				to 3.4V. (Default from NVM memory)
				0h = 0.600V 1h = 0.625V
				2h = 0.650V
				3h = 0.675V
				4h = 0.700V
				5h = 0.725V
				6h = 0.750V
				7h = 0.775V
				8h = 0.800V
				9h = 0.825V
				Ah = 0.850V
				Bh = 0.875V Ch = 0.900V
				Dh = 0.925V
				Eh = 0.950V
				Fh = 0.975V
				10h = 1.000V
				11h = 1.025V
				12h = 1.050V
				13h = 1.075V
				14h = 1.100V 15h = 1.125V
				15h = 1.125V  16h = 1.150V
				17h = 1.175V
				18h = 1.200V
				19h = 1.225V
				1Ah = 1.250V
				1Bh = 1.275V
				1Ch = 1.300V
				1Dh = 1.325V
				1Eh = 1.350V
				1Fh = 1.375V 20h = 1.400V
				21h = 1.500V
				22h = 1.600V
				23h = 1.700V
				24h = 1.800V
				25h = 1.900V
				26h = 2.000V
				27h = 2.100V
				28h = 2.200V 29h = 2.300V
				2Ah = 2.400V
				2Bh = 2.500V
				2Ch = 2.600V
				2Dh = 2.700V
				2Eh = 2.800V
				2Fh = 2.900V
				30h = 3.000V
				31h = 3.100V 32h = 3.200V
				32n = 3.200V  33h = 3.300V
				34h = 3.400V
				35h = 3.400V
				36h = 3.400V
				37h = 3.400V
				38h = 3.400V
				39h = 3.400V
				3Ah = 3.400V
				3Bh = 3.400V
				3Ch = 3.400V
				3Dh = 3.400V 3Eh = 3.400V
				JULII - 3.400 V

**TPS65215-Q1**SLVSHQ9 – JUNE 2025



### Table 6-15. BUCK3\_VOUT Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
				3Fh = 3.400V



### 6.7.8 BUCK2\_VOUT Register (Offset = 9h) [Reset = XXh]

BUCK2\_VOUT is shown in Figure 6-25 and described in Table 6-16.

Return to the Summary Table.

### Figure 6-25. BUCK2\_VOUT Register



### Table 6-16. BUCK2\_VOUT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	BUCK2_BW_SEL	R/W		BUCK2 Bandwidth selection. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory) 0h = low bandwidth 1h = high bandwidth
6	BUCK2_UV_THR_SEL	R/W		UV threshold selection for BUCK2. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection



#### Table 6-16. BUCK2 VOUT Register Field Descriptions (continued)

Bit         Field         Type         Reset         Description           5-0         BUCK2_VSET         R/W         X         Voltage selection for BUCK2. The of to 3.4V. (Default from NVM memory 0h = 0.600V 1h = 0.625V 2h = 0.625V 2h = 0.650V 3h = 0.675V	
to 3.4V. (Default from NVM memory 0h = 0.600V 1h = 0.625V 2h = 0.650V	
0h = 0.600V 1h = 0.625V 2h = 0.650V	у)
1h = 0.625V 2h = 0.650V	
2h = 0.650V	
4h = 0.700V	
5h = 0.725V	
6h = 0.750V	
7h = 0.775V	
8h = 0.800V	
9h = 0.825V	
Ah = 0.850V	
Bh = 0.875V	
Ch = 0.900V	
Dh = 0.925V	
Eh = 0.950V   Fh = 0.975V	
10h = 1.000V	
11h = 1.005V	
12h = 1.050V	
13h = 1.075V	
14h = 1.100V	
15h = 1.125V	
16h = 1.150V	
17h = 1.175V	
18h = 1.200V	
19h = 1.225V	
1Ah = 1.250V 1Bh = 1.275V	
1Ch = 1.300V	
1Dh = 1.325V	
1Eh = 1.350V	
1Fh = 1.375V	
20h = 1.400V	
21h = 1.500V	
22h = 1.600V	
23h = 1.700V	
24h = 1.800V	
25h = 1.900V	
26h = 2.000V	
27h = 2.100V 28h = 2.200V	
2811 – 2.200V 29h = 2.300V	
2511 - 2.500V 2Ah = 2.400V	
2Bh = 2.500V	
2Ch = 2.600V	
2Dh = 2.700V	
2Eh = 2.800V	
2Fh = 2.900V	
30h = 3.000V	
31h = 3.100V	
32h = 3.200V	
33h = 3.300V 34h = 3.400V	
34n = 3.400V 35h = 3.400V	
351 - 3.400V 36h = 3.400V	
37h = 3.400V	
38h = 3.400V	
39h = 3.400V	
3Ah = 3.400V	
3Bh = 3.400V	
3Ch = 3.400V	
3Dh = 3.400V	
3Eh = 3.400V	







# Table 6-16. BUCK2\_VOUT Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
				3Fh = 3.400V

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback



### 6.7.9 BUCK1\_VOUT Register (Offset = Ah) [Reset = XXh]

BUCK1\_VOUT is shown in Figure 6-26 and described in Table 6-17.

Return to the Summary Table.

### Figure 6-26. BUCK1\_VOUT Register



### Table 6-17. BUCK1\_VOUT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	BUCK1_BW_SEL	R/W		BUCK1 Bandwidth selection. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory) 0h = low bandwidth 1h = high bandwidth
6	BUCK1_UV_THR_SEL	R/W		UV threshold selection for BUCK1. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection

Product Folder Links: TPS65215-Q1

Submit Document Feedback



#### Table 6-17. BUCK1 VOUT Register Field Descriptions (continued)

D'4				er Field Descriptions (continued)
Bit	Field	Туре	Reset	Description
5-0	BUCK1_VSET	R/W	X	Voltage selection for BUCK1. The output voltage range is from 0.6V
				to 3.4V. (Default from NVM memory)
				0h = 0.600V 1h = 0.625V
				2h = 0.650V
				3h = 0.675V
				4h = 0.700V
				5h = 0.725V
				6h = 0.750V
				7h = 0.775V
				8h = 0.800V
				9h = 0.825V
				Ah = 0.850V
				Bh = 0.875V Ch = 0.900V
				Dh = 0.925V
				Eh = 0.950V
				Fh = 0.975V
				10h = 1.000V
				11h = 1.025V
				12h = 1.050V
				13h = 1.075V
				14h = 1.100V
				15h = 1.125V  16h = 1.150V
				17h = 1.175V
				18h = 1.200V
				19h = 1.225V
				1Ah = 1.250V
				1Bh = 1.275V
				1Ch = 1.300V
				1Dh = 1.325V
				1Eh = 1.350V
				1Fh = 1.375V 20h = 1.400V
				21h = 1.500V
				22h = 1.600V
				23h = 1.700V
				24h = 1.800V
				25h = 1.900V
				26h = 2.000V
				27h = 2.100V
				28h = 2.200V 29h = 2.300V
				2Ah = 2.400V
				2Bh = 2.500V
				2Ch = 2.600V
				2Dh = 2.700V
				2Eh = 2.800V
				2Fh = 2.900V
				30h = 3.000V
				31h = 3.100V
				32h = 3.200V 33h = 3.300V
				34h = 3.400V
				35h = 3.400V
				36h = 3.400V
				37h = 3.400V
				38h = 3.400V
				39h = 3.400V
				3Ah = 3.400V
				3Bh = 3.400V
I				3Ch = 3.400V
				3Dh = 3.400V
				3Eh = 3.400V

**TPS65215-Q1**SLVSHQ9 – JUNE 2025



### Table 6-17. BUCK1\_VOUT Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
				3Fh = 3.400V

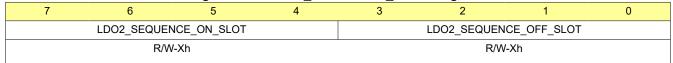


### 6.7.10 LDO2\_SEQUENCE\_SLOT Register (Offset = Ch) [Reset = XXh]

LDO2\_SEQUENCE\_SLOT is shown in Figure 6-27 and described in Table 6-18.

Return to the Summary Table.

### Figure 6-27. LDO2\_SEQUENCE\_SLOT Register



#### Table 6-18. LDO2\_SEQUENCE\_SLOT Register Field Descriptions

Bit	Field	Туре	Reset	Description Descriptions
7-4	LDO2_SEQUENCE_ON_ SLOT	R/W	X	LDO2 slot number for power-up (Default from NVM memory)  0h = slot 0  1h = slot 1  2h = slot 2  3h = slot 3  4h = slot 4  5h = slot 5  6h = slot 6  7h = slot 7  8h = slot 8  9h = slot 9  Ah = slot 10  Bh = slot 11  Ch = slot 12  Dh = slot 13  Eh = slot 14  Fh = slot 15
3-0	LDO2_SEQUENCE_OFF_ SLOT	R/W	X	LDO2 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15

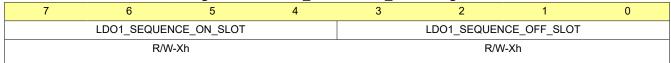


### 6.7.11 LDO1\_SEQUENCE\_SLOT Register (Offset = Eh) [Reset = XXh]

LDO1\_SEQUENCE\_SLOT is shown in Figure 6-28 and described in Table 6-19.

Return to the Summary Table.

### Figure 6-28. LDO1\_SEQUENCE\_SLOT Register



### Table 6-19. LDO1\_SEQUENCE\_SLOT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	LDO1_SEQUENCE_ON_ SLOT	R/W	X	LDO1 slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 9 Ah = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15
3-0	LDO1_SEQUENCE_OFF_ SLOT	R/W	X	LDO1 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 9 Ah = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15

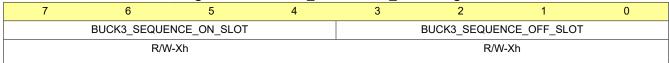


### 6.7.12 BUCK3\_SEQUENCE\_SLOT Register (Offset = Fh) [Reset = XXh]

BUCK3\_SEQUENCE\_SLOT is shown in Figure 6-29 and described in Table 6-20.

Return to the Summary Table.

### Figure 6-29. BUCK3\_SEQUENCE\_SLOT Register



#### Table 6-20. BUCK3\_SEQUENCE\_SLOT Register Field Descriptions

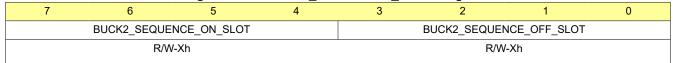
Bit	Field	Туре	Reset	Description
7-4	BUCK3_SEQUENCE_ON _SLOT	R/W	X	BUCK3 slot number for power-up (Default from NVM memory)  0h = slot 0  1h = slot 1  2h = slot 2  3h = slot 3  4h = slot 4  5h = slot 5  6h = slot 6  7h = slot 7  8h = slot 8  9h = slot 9  Ah = slot 10  Bh = slot 11  Ch = slot 12  Dh = slot 13  Eh = slot 14  Fh = slot 15
3-0	BUCK3_SEQUENCE_OF F_SLOT	R/W	X	BUCK3 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 9 Ah = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15

### 6.7.13 BUCK2\_SEQUENCE\_SLOT Register (Offset = 10h) [Reset = XXh]

BUCK2\_SEQUENCE\_SLOT is shown in Figure 6-30 and described in Table 6-21.

Return to the Summary Table.

### Figure 6-30. BUCK2\_SEQUENCE\_SLOT Register



#### Table 6-21. BUCK2\_SEQUENCE\_SLOT Register Field Descriptions

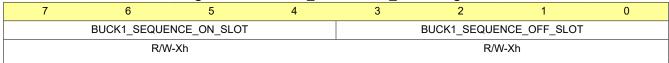
Bit	Field	Туре	Reset	Description
7-4	BUCK2_SEQUENCE_ON _SLOT	R/W	X	BUCK2 Slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 9 Ah = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15
3-0	BUCK2_SEQUENCE_OF F_SLOT	R/W	X	BUCK2 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 9 Ah = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15

### 6.7.14 BUCK1\_SEQUENCE\_SLOT Register (Offset = 11h) [Reset = XXh]

BUCK1\_SEQUENCE\_SLOT is shown in Figure 6-31 and described in Table 6-22.

Return to the Summary Table.

### Figure 6-31. BUCK1\_SEQUENCE\_SLOT Register



#### Table 6-22. BUCK1\_SEQUENCE\_SLOT Register Field Descriptions

Bit	Field	Туре	Reset	Description Descriptions
7-4	BUCK1_SEQUENCE_ON _SLOT	R/W	X	BUCK1 Slot number for power-up (Default from NVM memory)  0h = slot 0  1h = slot 1  2h = slot 2  3h = slot 3  4h = slot 4  5h = slot 5  6h = slot 6  7h = slot 7  8h = slot 8  9h = slot 9  Ah = slot 10  Bh = slot 11  Ch = slot 12  Dh = slot 13  Eh = slot 14  Fh = slot 15
3-0	BUCK1_SEQUENCE_OF F_SLOT	R/W	X	BUCK1 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 9 Ah = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15



### 6.7.15 nRST\_SEQUENCE\_SLOT Register (Offset = 12h) [Reset = XXh]

nRST\_SEQUENCE\_SLOT is shown in Figure 6-32 and described in Table 6-23.

Return to the Summary Table.

### Figure 6-32. nRST\_SEQUENCE\_SLOT Register



#### Table 6-23. nRST\_SEQUENCE\_SLOT Register Field Descriptions

Bit	Field	Туре	Reset	Description Descriptions
7-4	nRST_SEQUENCE_ON_ SLOT	R/W	X	nRST slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 9 Ah = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15
3-0	nRST_SEQUENCE_OFF_ SLOT	R/W	X	nRST slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 9 Ah = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15

Product Folder Links: TPS65215-Q1

ibmit Document Feedback

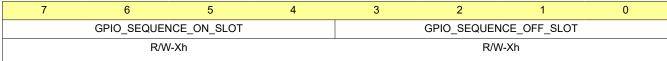


### 6.7.16 GPIO\_SEQUENCE\_SLOT Register (Offset = 13h) [Reset = XXh]

GPIO\_SEQUENCE\_SLOT is shown in Figure 6-33 and described in Table 6-24.

Return to the Summary Table.

### Figure 6-33. GPIO\_SEQUENCE\_SLOT Register



### Table 6-24. GPIO\_SEQUENCE\_SLOT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	GPIO_SEQUENCE_ON_ SLOT	R/W	X	GPIO slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 9 Ah = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15
3-0	GPIO_SEQUENCE_OFF_ SLOT	R/W	X	GPIO slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7 8h = slot 8 9h = slot 10 Bh = slot 11 Ch = slot 12 Dh = slot 13 Eh = slot 14 Fh = slot 15

# 6.7.17 GPO2\_SEQUENCE\_SLOT Register (Offset = 14h) [Reset = XXh]

GPO2\_SEQUENCE\_SLOT is shown in Figure 6-34 and described in Table 6-25.

Return to the Summary Table.

### Figure 6-34. GPO2\_SEQUENCE\_SLOT Register



#### Table 6-25. GPO2\_SEQUENCE\_SLOT Register Field Descriptions

Bit	Field	Туре	Reset	Description
				-
7-4	GPO2_SEQUENCE_ON_ SLOT	R/W	X	GPO2 slot number for power-up (Default from NVM memory) 0h = slot 0
	SLOT			1h = slot 1
				2h = slot 2
				3h = slot 3
				4h = slot 4
				5h = slot 5
				6h = slot 6
				7h = slot 7
				8h = slot 8
				9h = slot 9
				Ah = slot 10
				Bh = slot 11
				Ch = slot 12
				Dh = slot 13
				Eh = slot 14
				Fh = slot 15
3-0	GPO2_SEQUENCE_OFF	R/W	x	GPO2 slot number for power-down (Default from NVM memory)
	_SLOT			0h = slot 0
				1h = slot 1
				2h = slot 2
				3h = slot 3
				4h = slot 4
				5h = slot 5
				6h = slot 6 7h = slot 7
				8h = slot 8
				9h = slot 9
				Ah = slot 10
				Bh = slot 11
				Ch = slot 12
				Dh = slot 13
				Eh = slot 14
				Fh = slot 15
	l.	l .		

Submit Document Feedback

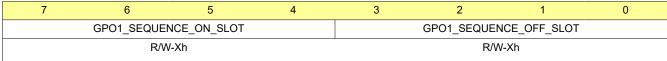
Copyright © 2025 Texas Instruments Incorporated

# 6.7.18 GPO1\_SEQUENCE\_SLOT Register (Offset = 15h) [Reset = XXh]

GPO1\_SEQUENCE\_SLOT is shown in Figure 6-35 and described in Table 6-26.

Return to the Summary Table.

### Figure 6-35. GPO1\_SEQUENCE\_SLOT Register



#### Table 6-26. GPO1 SEQUENCE SLOT Register Field Descriptions

Bit	Field		Reset	Description
-		Туре		Description
7-4	GPO1_SEQUENCE_ON_	R/W	X	GPO1 slot number for power-up (Default from NVM memory)
	SLOT			0h = slot 0
				1h = slot 1
				2h = slot 2
				3h = slot 3
				4h = slot 4
				5h = slot 5
				6h = slot 6
				7h = slot 7
				8h = slot 8
				9h = slot 9
				Ah = slot 10
				Bh = slot 11
				Ch = slot 12
				Dh = slot 13
				Eh = slot 14
				Fh = slot 15
3-0	GPO1_SEQUENCE_OFF	R/W	Х	GPO1 slot number for power-down (Default from NVM memory)
	_SLOT			0h = slot 0
	_			1h = slot 1
				2h = slot 2
				3h = slot 3
				4h = slot 4
				5h = slot 5
				6h = slot 6
				7h = slot 7
				8h = slot 8
				9h = slot 9
				Ah = slot 10
				Bh = slot 11
				Ch = slot 12
				Dh = slot 13
				Eh = slot 14
				Fh = slot 15

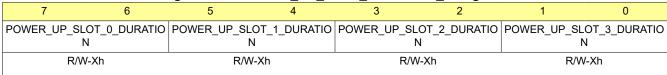


### 6.7.19 POWER\_UP\_SLOT\_DURATION\_1 Register (Offset = 16h) [Reset = XXh]

POWER\_UP\_SLOT\_DURATION\_1 is shown in Figure 6-36 and described in Table 6-27.

Return to the Summary Table.

### Figure 6-36. POWER\_UP\_SLOT\_DURATION\_1 Register



#### Table 6-27. POWER\_UP\_SLOT\_DURATION\_1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	POWER_UP_SLOT_0_D URATION	R/W	X	Duration of slot 0 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_UP_SLOT_1_D URATION	R/W	X	Duration of slot 1 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
3-2	POWER_UP_SLOT_2_D URATION	R/W	X	Duration of slot 2 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_UP_SLOT_3_D URATION	R/W	X	Duration of slot 3 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms

### 6.7.20 POWER\_UP\_SLOT\_DURATION\_2 Register (Offset = 17h) [Reset = XXh]

POWER\_UP\_SLOT\_DURATION\_2 is shown in Figure 6-37 and described in Table 6-28.

Return to the Summary Table.

#### Figure 6-37. POWER\_UP\_SLOT\_DURATION\_2 Register

	_			<u>_</u>		· <del>-</del>	
7	6	5	4	3	2	1	0
POWER_UP_SI	LOT_4_DURATIO	POWER_UP_SL	OT_5_DURATIO	POWER_UP_	SLOT_6_DURATIO	POWER_UP_SLOT	_7_DURATIO
R/V	V-Xh	R/W	-Xh	 R	R/W-Xh	R/W-XI	h

#### Table 6-28. POWER\_UP\_SLOT\_DURATION\_2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	POWER_UP_SLOT_4_D URATION	R/W	X	Duration of slot 4 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_UP_SLOT_5_D URATION	R/W	X	Duration of slot 5 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
3-2	POWER_UP_SLOT_6_D URATION	R/W	X	Duration of slot 6 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_UP_SLOT_7_D URATION	R/W	Х	Duration of slot 7 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms

# 6.7.21 POWER\_UP\_SLOT\_DURATION\_3 Register (Offset = 18h) [Reset = XXh]

POWER\_UP\_SLOT\_DURATION\_3 is shown in Figure 6-38 and described in Table 6-29.

Return to the Summary Table.

### Figure 6-38. POWER\_UP\_SLOT\_DURATION\_3 Register

7	6	5	4	3	2	1	0
POWER_UP_S	LOT_8_DURATIO	POWER_UP_S	LOT_9_DURATIO	POWER_UP	_		_11_DURATI
	N		N		ON	ON	
R/\	V-Xh	R/	W-Xh	F	R/W-Xh	R/W-Xh	1

#### Table 6-29. POWER\_UP\_SLOT\_DURATION\_3 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	POWER_UP_SLOT_8_D URATION	R/W	X	Duration of slot 8 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_UP_SLOT_9_D URATION	R/W	X	Duration of slot 9 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms
3-2	POWER_UP_SLOT_10_D URATION	R/W	X	Duration of slot 10 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_UP_SLOT_11_D URATION	R/W	X	Duration of slot 11 during the power-up and standby-to-active sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms

# 6.7.22 POWER\_UP\_SLOT\_DURATION\_4 Register (Offset = 19h) [Reset = XXh]

POWER\_UP\_SLOT\_DURATION\_4 is shown in Figure 6-39 and described in Table 6-30.

Return to the Summary Table.

#### Figure 6-39. POWER\_UP\_SLOT\_DURATION\_4 Register

		J		_			
7	6	5	4	3	2	1	0
POWER_UP_SLO		POWER_UP_	SLOT_13_DURATI ON	POWER_UP_	SLOT_14_DURATI ON	POWER_UP_SLOTON	Γ_15_DURATI
R/W	-Xh	R	/W-Xh	F	R/W-Xh	R/W-X	h

#### Table 6-30. POWER\_UP\_SLOT\_DURATION\_4 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	POWER_UP_SLOT_12_D URATION	R/W	X	Duration of slot 12 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_UP_SLOT_13_D URATION	R/W	X	Duration of slot 13 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
3-2	POWER_UP_SLOT_14_D URATION	R/W	X	Duration of slot 14 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_UP_SLOT_15_D URATION	R/W	X	Duration of slot 15 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms



### 6.7.23 POWER\_DOWN\_SLOT\_DURATION\_1 Register (Offset = 1Ah) [Reset = XXh]

POWER\_DOWN\_SLOT\_DURATION\_1 is shown in Figure 6-40 and described in Table 6-31.

Return to the Summary Table.

### Figure 6-40. POWER\_DOWN\_SLOT\_DURATION\_1 Register

7	6	5	4	3	2	1	0
POWER_DOWN_ ATIO			N_SLOT_1_DUR TON	POWER_DO	DWN_SLOT_2_DUR ATION	POWER_DOWN ATIO	
R/W-Xh		RΛ	V-Xh		R/W-Xh	R/W	-Xh

#### Table 6-31. POWER\_DOWN\_SLOT\_DURATION\_1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	POWER_DOWN_SLOT_0 _DURATION	R/W	×	Duration of slot 0 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_DOWN_SLOT_1 _DURATION	R/W	X	Duration of slot 1 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms
3-2	POWER_DOWN_SLOT_2 _DURATION	R/W	x	Duration of slot 2 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms
1-0	POWER_DOWN_SLOT_3 _DURATION	R/W	x	Duration of slot 3 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms



### 6.7.24 POWER\_DOWN\_SLOT\_DURATION\_2 Register (Offset = 1Bh) [Reset = XXh]

POWER\_DOWN\_SLOT\_DURATION\_2 is shown in Figure 6-41 and described in Table 6-32.

Return to the Summary Table.

### Figure 6-41. POWER\_DOWN\_SLOT\_DURATION\_2 Register

7	6	5	4	3	2	1	0
POWER_DOWN ATI	N_SLOT_4_DUR ON	POWER_DO	OWN_SLOT_5_DUR ATION		N_SLOT_6_DUR TON		N_SLOT_7_DUR
R/W-Xh			R/W-Xh	R/\	V-Xh	R/W	/-Xh

#### Table 6-32. POWER\_DOWN\_SLOT\_DURATION\_2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	POWER_DOWN_SLOT_4 _DURATION	R/W	X	Duration of slot 4 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_DOWN_SLOT_5 _DURATION	R/W	X	Duration of slot 5 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms
3-2	POWER_DOWN_SLOT_6 _DURATION	R/W	X	Duration of slot 6 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_DOWN_SLOT_7 _DURATION	R/W	Х	Duration of slot 7 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback



# 6.7.25 POWER\_DOWN\_SLOT\_DURATION\_3 Register (Offset = 1Ch) [Reset = XXh]

POWER\_DOWN\_SLOT\_DURATION\_3 is shown in Figure 6-42 and described in Table 6-33.

Return to the Summary Table.

### Figure 6-42. POWER\_DOWN\_SLOT\_DURATION\_3 Register

7	6	5	4	3	2	1	0
POWER_DOWN ATIO		_	N_SLOT_9_DUR TION	POWER_	DOWN_SLOT_10_DU RATION	POWER_DOWN_ ATIO	
R/W-	Xh	R/	W-Xh		R/W-Xh	R/W	-Xh

#### Table 6-33. POWER\_DOWN\_SLOT\_DURATION\_3 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	POWER_DOWN_SLOT_8 _DURATION	R/W	X	Duration of slot 8 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms
5-4	POWER_DOWN_SLOT_9 _DURATION	R/W	X	Duration of slot 9 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms
3-2	POWER_DOWN_SLOT_1 0_DURATION	R/W	X	Duration of slot 10 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_DOWN_SLOT_1 1_DURATION	R/W	X	Duration of slot 11 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms



### 6.7.26 POWER\_DOWN\_SLOT\_DURATION\_4 Register (Offset = 1Dh) [Reset = XXh]

POWER\_DOWN\_SLOT\_DURATION\_4 is shown in Figure 6-43 and described in Table 6-34.

Return to the Summary Table.

#### Figure 6-43. POWER DOWN SLOT DURATION 4 Register

				_			
7	6	5	4	3	2	1	0
POWER_DOWN RAT	N_SLOT_12_DU TON		N_SLOT_13_DU TON	_	OWN_SLOT_14_DU RATION	POWER_DOWN RAT	N_SLOT_15_DU TON
R/W	/-Xh	R/W	/-Xh	1	R/W-Xh	R/W	/-Xh

#### Table 6-34. POWER\_DOWN\_SLOT\_DURATION\_4 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	POWER_DOWN_SLOT_1 2_DURATION	R/W	X	Duration of slot 12 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_DOWN_SLOT_1 3_DURATION	R/W	X	Duration of slot 13 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms
3-2	POWER_DOWN_SLOT_1 4_DURATION	R/W	X	Duration of slot 14 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_DOWN_SLOT_1 5_DURATION	R/W	X	Duration of slot 15 during the power-down and active-to-standby sequences. (Default from NVM memory)  0h = 0ms  1h = 1.5ms  2h = 3ms  3h = 10ms

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback

### 6.7.27 GENERAL\_CONFIG Register (Offset = 1Eh) [Reset = XXh]

GENERAL\_CONFIG is shown in Figure 6-44 and described in Table 6-35.

Return to the Summary Table.

### Figure 6-44. GENERAL\_CONFIG Register

					_		
7	6	5	4	3	2	1	0
BYPASS_RAIL S_DISCHARGE D_CHECK	RESERVED	LDO2_UV_THR	RESERVED	LDO1_UV_THR	GPIO_EN	GPO2_EN	GPO1_EN
R/W-Xh	R-0h	R/W-Xh	R-0h	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh

### Table 6-35. GENERAL\_CONFIG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	BYPASS_RAILS_DISCHA RGED_CHECK	R/W	X	Bypass the all-rails discharged check to commence a transition to ACTIVE state, and the rails-in-slot discharged check executed in each slot during a power-down to INITIALIZE state. Does not bypass the check for RV(Pre-biased) condition prior to enabling a regulator. (Default from NVM memory)  0h = Discharged checks enforced 1h = Discharged checks bypassed
6	RESERVED	R	0h	
5	LDO2_UV_THR	R/W	X	UV threshold selection bit for LDO2. Only applicable if configured as LDO. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection
4	RESERVED	R	0h	
3	LDO1_UV_THR	R/W	Х	UV threshold selection bit for LDO1. Only applicable if configured as LDO. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection
2	GPIO_EN	R/W	Х	Both an enable and state control of GPIO. This bit enables the GPIO function and also controls the state of the GPIO pin. (Default from NVM memory)  0h = The GPIO function is disabled. The output state is 'low'.  1h = The GPIO function is enabled. The output state is 'high'.
1	GPO2_EN	R/W	Х	Both an enable and state control of GPO. This bit enables the GPO function and also controls the state of the GPO pin. (Default from NVM memory)  0h = GPO2 disabled. The output state is low.  1h = GPO2 enabled. The output state is Hi-Z.
0	GPO1_EN	R/W	Х	Both an enable and state control of GPO1. This bit enables the GPO1 function and also controls the state of the GPO1 pin. (Default from NVM memory)  0h = GPO1 disabled. The output state is low.  1h = GPO1 enabled. The output state is Hi-Z.



# 6.7.28 MFP\_1\_CONFIG Register (Offset = 1Fh) [Reset = XXh]

MFP\_1\_CONFIG is shown in Figure 6-45 and described in Table 6-36.

Return to the Summary Table.

### Figure 6-45. MFP\_1\_CONFIG Register

7	6	5	4	3	2	1	0
MODE_I2C_CT RL	VSEL_SD_I2C_ CTRL	MODE_RESET _POLARITY	MODE_STBY_ POLARITY	MULTI_DEVICE _ENABLE	RESERVED	VSEL_SD_POL ARITY	VSEL_DDR_SD
R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R-0h	R/W-Xh	R/W-Xh

#### Table 6-36. MFP\_1\_CONFIG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	MODE_I2C_CTRL	R/W	Х	MODE control using I2C. Consolidated with MODE control via MODE/RESET and/or MODE/STBY pins. Refer to table in the data sheet. (Default from NVM memory) 0h = Auto PFM 1h = Forced PWM
6	VSEL_SD_I2C_CTRL	R/W	X	VSEL_SD control using I2C. Applicable only if VSEL_SD/ VSEL_DDR pin is configured as "VSEL_DDR". (Default from NVM memory) 0h = 1.8V 1h = LDOx_VOUT register setting
5	MODE_RESET_POLARIT Y	R/W	X	MODE_RESET Pin Polarity configuration. Note: Ok to change during operation, but consider immediate reaction: MODE-change or RESET-entry! (Default from NVM memory)  0h = [if configured as MODE] LOW - auto-PFM / HIGH - forced PWM. [if configured as RESET] LOW - reset / HIGH - normal operation.  1h = [if configured as MODE] HIGH - auto-PFM / LOW - forced PWM. [if configured as RESET] HIGH - reset / LOW - normal operation.
4	MODE_STBY_POLARITY	R/W	X	MODE_STBY Pin Polarity configuration. Note: Ok to change during operation, but consider immediate reaction: MODE-change or STATE-change! (Default from NVM memory)  0h = [if configured as MODE] LOW - auto-PFM / HIGH - forced PWM. [if configured as a STBY] LOW - STBY state / HIGH - ACTIVE state.  1h = [if configured as MODE] HIGH - auto-PFM / LOW - forced PWM. [if configured as a STBY] HIGH - STBY state / LOW - ACTIVE state.
3	MULTI_DEVICE_ENABLE	R/W	Х	Configures the device as a single device where GPO is used as GPO function, or as a multi-device configuration where GPO is used for synchronization with other devices. NOTE: ONLY CHANGE IN INITIALIZE STATE! (Default from NVM memory)  0h = Single-device configuration, GPIO pin configured as GPO  1h = Multi-device configuration, GPIO pin configured as GPIO
2	RESERVED	R	Х	
1	VSEL_SD_POLARITY	R/W	Х	SD Card Voltage Select Note: Ok to change during operation, but consider immediate reaction: change of SD-card supply voltage! (Default from NVM memory)  0h = LOW - 1.8V / HIGH - LDOx_VOUT register setting  1h = HIGH - 1.8V / LOW - LDOx_VOUT register setting
0	VSEL_DDR_SD	R/W	X	VSEL_SD/VSEL_DDR Configuration NOTE: ONLY CHANGE IN INITIALIZE STATE! (Default from NVM memory) 0h = VSEL pin configured as DDR to set the voltage on Buck3 1h = VSEL pin configured as SD to set the voltage on LDO1



# 6.7.29 MFP\_2\_CONFIG Register (Offset = 20h) [Reset = XXh]

MFP\_2\_CONFIG is shown in Figure 6-46 and described in Table 6-37.

Return to the Summary Table.

#### Figure 6-46. MFP\_2\_CONFIG Register

					9.2.2.		
7	6	5	4	3	2	1	0
PU_ON_FSD	WARM_COLD_ RESET_CONFI G	EN_PB_VSENSE	_CONFIG	EN_PB_VSENS E_DEGL	MODE_RESET _CONFIG	MODE_STB	Y_CONFIG
R/W-Xh	R/W-Xh	R/W-Xh		R/W-Xh	R/W-Xh	R/W-	-Xh

# Table 6-37. MFP\_2\_CONFIG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	PU_ON_FSD	R/W	X	Power up upon First Supply Detected (FSD). So when VSYS is applied, device does power up to ACTIVE state even if EN/PB/ VSENSE pin is at OFF_REQ status. (Default from NVM memory) 0h = First Supply Detection (FSD) Disabled. 1h = First Supply Detection (FSD) Enabled.
6	WARM_COLD_RESET_C ONFIG	R/W	X	Selection between WARM or COLD Reset, when a RESET event is triggered via MODE/RESET pin (does not apply to RESET via I2C) (Default from NVM memory)  0h = COLD RESET  1h = WARM RESET
5-4	EN_PB_VSENSE_CONFI	R/W	X	Enable / Push-Button / VSENSE Configuration. Do not change via I2C after NVM load (except as a precursor before programming NVM) (Default from NVM memory) 0h = Device Enable Configuration 1h = Push Button Configuration 2h = VSENSE Configuration 3h = Device Enable Configuration
3	EN_PB_VSENSE_DEGL	R/W	X	Enable / Push-Button / VSENSE Deglitch NOTE: ONLY CHANGE IN INITIALIZE STATE! Consider immediate reaction when changing from EN/VSENSE to PB or vice versa: power-up! (Default from NVM memory)  0h = short (typ: 120us for EN/VSENSE and 200ms for PB)  1h = long (typ: 50ms for EN/VSENSE and 600ms for PB)
2	MODE_RESET_CONFIG	R/W	Х	MODE/RESET Configuration (Default from NVM memory) 0h = MODE 1h = RESET
1-0	MODE_STBY_CONFIG	R/W	X	MODE_STDBY Configuration (Default from NVM memory) 0h = MODE 1h = STBY 2h = MODE and STBY 3h = MODE



# 6.7.30 STBY\_1\_CONFIG Register (Offset = 21h) [Reset = XXh]

STBY\_1\_CONFIG is shown in Figure 6-47 and described in Table 6-38.

Return to the Summary Table.

### Figure 6-47. STBY\_1\_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDO2_STBY_E N	RESERVED	LDO1_STBY_E N	BUCK3_STBY_ EN	BUCK2_STBY_ EN	BUCK1_STBY_ EN
R-0h	R-0h	R/W-Xh	R-0h	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh

#### Table 6-38. STBY\_1\_CONFIG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	LDO2_STBY_EN	R/W	Х	Enable LDO2 in STANDBY state. (Default from NVM memory) 0h = Disabled in STBY Mode 1h = Enabled in STBY Mode
4	RESERVED	R	0h	
3	LDO1_STBY_EN	R/W	Х	Enable LDO1 in STANDBY state. (Default from NVM memory) 0h = Disabled in STBY Mode 1h = Enabled in STBY Mode
2	BUCK3_STBY_EN	R/W	Х	Enable BUCK3 in STANDBY state. (Default from NVM memory)  0h = Disabled in STBY Mode  1h = Enabled in STBY Mode
1	BUCK2_STBY_EN	R/W	Х	Enable BUCK2 in STANDBY state. (Default from NVM memory) 0h = Disabled in STBY Mode 1h = Enabled in STBY Mode
0	BUCK1_STBY_EN	R/W	Х	Enable BUCK1 in STANDBY state. (Default from NVM memory) 0h = Disabled in STBY Mode 1h = Enabled in STBY Mode



# 6.7.31 STBY\_2\_CONFIG Register (Offset = 22h) [Reset = 0Xh]

STBY\_2\_CONFIG is shown in Figure 6-48 and described in Table 6-39.

Return to the Summary Table.

### Figure 6-48. STBY\_2\_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPIO_STBY_E N	GPO2_STBY_E N	GPO1_STBY_E N
R-0h	R-0h	R-0h	R-0h	R-0h	R/W-Xh	R/W-Xh	R/W-Xh

#### Table 6-39. STBY\_2\_CONFIG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	GPIO_STBY_EN	R/W	Х	Enable GPIO in STANDBY state. (Default from NVM memory) 0h = Disabled in STBY Mode 1h = Enabled in STBY Mode
1	GPO2_STBY_EN	R/W	Х	Enable GPO2 in STANDBY state. (Default from NVM memory) 0h = Disabled in STBY Mode 1h = Enabled in STBY Mode
0	GPO1_STBY_EN	R/W	Х	Enable GPO1 in STANDBY state. (Default from NVM memory) 0h = Disabled in STBY Mode 1h = Enabled in STBY Mode

Product Folder Links: TPS65215-Q1

106



### 6.7.32 OC\_DEGL\_CONFIG Register (Offset = 23h) [Reset = XXh]

OC\_DEGL\_CONFIG is shown in Figure 6-49 and described in Table 6-40.

Return to the Summary Table.

# Figure 6-49. OC\_DEGL\_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	EN_LONG_DE GL_FOR_OC_L DO2	RESERVED	EN_LONG_DE GL_FOR_OC_L DO1	EN_LONG_DE GL_FOR_OC_ BUCK3	EN_LONG_DE GL_FOR_OC_ BUCK2	EN_LONG_DE GL_FOR_OC_ BUCK1
R-0h	R-0h	R/W-Xh	R-0h	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh

### Table 6-40. OC\_DEGL\_CONFIG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	EN_LONG_DEGL_FOR_ OC_LDO2	R/W	Х	When set, enables the long-deglitch option for OverCurrent signal of LDO2. When clear, enables the short-deglitch option for OverCurrent signal of LDO2. (Default from NVM memory)  0h = Deglitch duration for OverCurrent signals of LDO2 is ~20us  1h = Deglitch duration for OverCurrent signals of LDO2 is ~2ms
4	RESERVED	R	0h	
3	EN_LONG_DEGL_FOR_ OC_LDO1	R/W	Х	When set, enables the long-deglitch option for OverCurrent signal of LDO1. When clear, enables the short-deglitch option for OverCurrent signal of LDO1. (Default from NVM memory)  0h = Deglitch duration for OverCurrent signals of LDO1 is ~20us  1h = Deglitch duration for OverCurrent signals of LDO1 is ~2ms
2	EN_LONG_DEGL_FOR_ OC_BUCK3	R/W	x	When set, enables the long-deglitch option for OverCurrent signals of BUCK3. When clear, enables the short-deglitch option for OverCurrent signals of BUCK3. (Default from NVM memory) 0h = Deglitch duration for OverCurrent signals for BUCK3 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us 1h = Deglitch duration for OverCurrent signals for BUCK3 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~2ms
1	EN_LONG_DEGL_FOR_ OC_BUCK2	R/W	X	When set, enables the long-deglitch option for OverCurrent signals of BUCK2. When clear, enables the short-deglitch option for OverCurrent signals of BUCK2. (Default from NVM memory) 0h = Deglitch duration for OverCurrent signals for BUCK2 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us 1h = Deglitch duration for OverCurrent signals for BUCK2 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~2ms
0	EN_LONG_DEGL_FOR_ OC_BUCK1	R/W	X	When set, enables the long-deglitch option for OverCurrent signals of BUCK1. When clear, enables the short-deglitch option for OverCurrent signals of BUCK1. (Default from NVM memory) 0h = Deglitch duration for OverCurrent signals for BUCK1 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us 1h = Deglitch duration for OverCurrent signals for BUCK1 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~2ms



# 6.7.33 INT\_MASK\_UV Register (Offset = 24h) [Reset = XXh]

INT\_MASK\_UV is shown in Figure 6-50 and described in Table 6-41.

Return to the Summary Table.

### Figure 6-50. INT\_MASK\_UV Register

7	6	5	4	3	2	1	0
MASK_RETRY _COUNT	BUCK3_UV_M ASK	BUCK2_UV_M ASK	BUCK1_UV_M ASK	RESERVED	LDO2_UV_MA SK	RESERVED	LDO1_UV_MA SK
R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R-0h	R/W-Xh	R-0h	R/W-Xh

### Table 6-41. INT\_MASK\_UV Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	MASK_RETRY_COUNT	R/W	Х	When set, device powers up even after two retries. (Default from NVM memory)  0h = Device does retry up to 2 times, then stay off  1h = Device does retry infinitely
6	BUCK3_UV_MASK	R/W	X	BUCK3 Undervoltage Mask. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
5	BUCK2_UV_MASK	R/W	Х	BUCK2 Undervoltage Mask. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
4	BUCK1_UV_MASK	R/W	X	BUCK1 Undervoltage Mask. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
3	RESERVED	R	0h	
2	LDO2_UV_MASK	R/W	Х	LDO2 Undervoltage Mask - Always masked in BYP or LSW modes. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
1	RESERVED	R	0h	
0	LDO1_UV_MASK	R/W	Х	LDO1 Undervoltage Mask - Always masked in BYP or LSW modes. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)



# 6.7.34 MASK\_CONFIG Register (Offset = 25h) [Reset = XXh]

MASK\_CONFIG is shown in Figure 6-51 and described in Table 6-42.

Return to the Summary Table.

# Figure 6-51. MASK\_CONFIG Register

7	6	5	4	3	2	1	0
MASK_INT_FO R_PB	MASK_EI	FECT	MASK_INT_FO R_RV	SENSOR_0_W ARM_MASK	SENSOR_1_W ARM_MASK	SENSOR_2_W ARM_MASK	SENSOR_3_W ARM_MASK
R/W-Xh	R/W-	Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh

### Table 6-42. MASK\_CONFIG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	MASK_INT_FOR_PB	R/W	X	Masking bit to control whether nINT pin is sensitive to PushButton (PB) press/release events or not. (Default from NVM memory) 0h = un-masked (nINT pulled low for any PB events) 1h = masked (nINT not sensitive to any PB events)
6-5	MASK_EFFECT	R/W	X	Effect of masking (global) (Default from NVM memory) 0h = no state change, no nINT reaction, no bit set for Faults 1h = no state change, no nINT reaction, bit set for Faults 2h = no state change, nINT reaction, bit set for Faults (same as 11b) 3h = no state change, nINT reaction, bit set for Faults (same as 11b)
4	MASK_INT_FOR_RV	R/W	X	Masking bit to control whether nINT pin is sensitive to RV (Residual Voltage) events or not. (Default from NVM memory) 0h = un-masked (nINT pulled low for any RV events during transition to ACTIVE state or during enabling of rails) 1h = masked (nINT not sensitive to any RV events)
3	SENSOR_0_WARM_MAS	R/W	Х	Die Temperature Warm Fault Mask, Sensor 0. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
2	SENSOR_1_WARM_MAS	R/W	X	Die Temperature Warm Fault Mask, Sensor 1. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
1	SENSOR_2_WARM_MAS	R/W	X	Die Temperature Warm Fault Mask, Sensor 2. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
0	SENSOR_3_WARM_MAS K	R/W	X	Die Temperature Warm Fault Mask, Sensor 3. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback

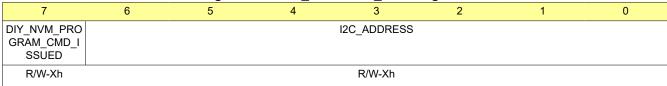


# 6.7.35 I2C\_ADDRESS\_REG Register (Offset = 26h) [Reset = XXh]

I2C\_ADDRESS\_REG is shown in Figure 6-52 and described in Table 6-43.

Return to the Summary Table.

# Figure 6-52. I2C\_ADDRESS\_REG Register



### Table 6-43. I2C\_ADDRESS\_REG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	DIY_NVM_PROGRAM_C MD_ISSUED	R/W	X	Bit that indicates whether a DIY program command was attempted. Once set, remains always set. (Default from NVM memory) 0h = NVM data not changed 1h = NVM data attempted to be changed via DIY program command
6-0	I2C_ADDRESS	R/W	Х	I2C secondary address. Note: Ok to change during operation, but consider immediate reaction: new address for read/write! (Default from NVM memory)

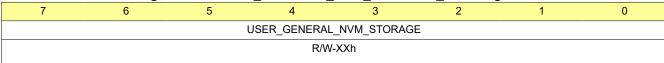


# 6.7.36 USER\_GENERAL\_NVM\_STORAGE\_REG Register (Offset = 27h) [Reset = XXh]

USER\_GENERAL\_NVM\_STORAGE\_REG is shown in Figure 6-53 and described in Table 6-44.

Return to the Summary Table.

Figure 6-53. USER\_GENERAL\_NVM\_STORAGE\_REG Register



### Table 6-44. USER\_GENERAL\_NVM\_STORAGE\_REG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	USER_GENERAL_NVM_ STORAGE	R/W		8-bit NVM-based register available to the user to use to store user- data, for example NVM-ID of customer-modified NVM-version or other purposes. (Default from NVM memory)

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback

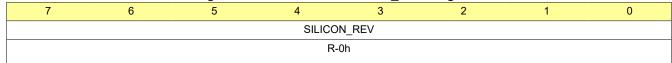


# 6.7.37 MANUFACTURING\_VER Register (Offset = 28h) [Reset = 00h]

MANUFACTURING\_VER is shown in Figure 6-54 and described in Table 6-45.

Return to the Summary Table.

# Figure 6-54. MANUFACTURING\_VER Register



# Table 6-45. MANUFACTURING\_VER Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	SILICON_REV	R		SILICON_REV[7:6] - Reserved SILICON_REV[5:3] - ALR SILICON_REV[2:0] - Metal Silicon Revision - Hard wired (not under NVM control)



# 6.7.38 MFP\_CTRL Register (Offset = 29h) [Reset = 00h]

MFP\_CTRL is shown in Figure 6-55 and described in Table 6-46.

Return to the Summary Table.

# Figure 6-55. MFP\_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPIO_STATUS	WARM_RESET _I2C_CTRL	COLD_RESET_ I2C_CTRL	STBY_I2C_CT RL	I2C_OFF_REQ
R-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

# Table 6-46. MFP\_CTRL Register Field Descriptions

	Table 6 46 mm i _5 mc_ register i loia 2000 iptione							
Bit	Field	Туре	Reset	Description				
7	RESERVED	R	0h					
6	RESERVED	R	0h					
5	RESERVED	R	0h					
4	GPIO_STATUS	R	Oh	Indicates the real-time value of GPIO pin 0h = The GPIO pin is currently '0' 1h = The GPIO pin is currently '1'				
3	WARM_RESET_I2C_CTR L	R/W	0h	Triggers a WARM RESET when written as '1'. Note: This bit self- clears automatically, so cannot be read as '1' after the write. 0h = normal operation 1h = WARM_RESET				
2	COLD_RESET_I2C_CTR L	R/W	0h	Triggers a COLD RESET when set high. Cleared upon entry to INITIALIZE.  0h = normal operation 1h = COLD_RESET				
1	STBY_I2C_CTRL	R/W	0h	STBY control using I2C. Consolidated with STBY control via MODE/ STBY pin. Refer to table in spec. 0h = normal operation 1h = STBY mode				
0	I2C_OFF_REQ	R/W	0h	When '1' is written to this bit: Trigger OFF request. When '0': No effect. Does self-clear. 0h = No effect 1h = Trigger OFF Request				



# 6.7.39 DISCHARGE\_CONFIG Register (Offset = 2Ah) [Reset = 7Fh]

DISCHARGE\_CONFIG is shown in Figure 6-56 and described in Table 6-47.

Return to the Summary Table.

# Figure 6-56. DISCHARGE\_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDO2_DISCHA RGE_EN	RESERVED	LDO1_DISCHA RGE_EN	BUCK3_DISCH ARGE_EN	BUCK2_DISCH ARGE_EN	BUCK1_DISCH ARGE_EN
R-0h	R-0h	R/W-1h	R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

# Table 6-47. DISCHARGE\_CONFIG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	LDO2_DISCHARGE_EN	R/W	1h	Discharge setting for LDO2 $0h = No$ Discharge $1h = 250 \Omega$
4	RESERVED	R	0h	
3	LDO1_DISCHARGE_EN	R/W	1h	Discharge setting for LDO1 $0h = No$ Discharge $1h = 200 \Omega$
2	BUCK3_DISCHARGE_EN	R/W	1h	Discharge setting for BUCK3 0h = No Discharge $1h = 125 \Omega$
1	BUCK2_DISCHARGE_EN	R/W	1h	Discharge setting for BUCK2 $0h = No$ Discharge $1h = 125 \Omega$
0	BUCK1_DISCHARGE_EN	R/W	1h	Discharge setting for BUCK1 $0h = No$ Discharge $1h = 125 \Omega$

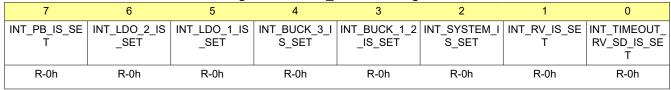


# 6.7.40 INT\_SOURCE Register (Offset = 2Bh) [Reset = 00h]

INT\_SOURCE is shown in Figure 6-57 and described in Table 6-48.

Return to the Summary Table.

# Figure 6-57. INT\_SOURCE Register



## Table 6-48. INT\_SOURCE Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	INT_PB_IS_SET	R	0h	One or more sources of the INT present in register INT_PB 0h = No bits set in INT_PB 1h = One or more bits set in INT_PB
6	INT_LDO_2_IS_SET	R	0h	One or more sources of the INT present in register INT_LDO_2 0h = No bits set in INT_LDO_2 1h = One or more bits set in INT_LDO_2
5	INT_LDO_1_IS_SET	R	0h	One or more sources of the INT present in register INT_LDO_1 0h = No bits set in INT_LDO_1 1h = One or more bits set in INT_LDO_1
4	INT_BUCK_3_IS_SET	R	0h	One or more sources of the INT present in register INT_BUCK_3  0h = No bits set in INT_BUCK_3  1h = One or more bits set in INT_BUCK_3
3	INT_BUCK_1_2_IS_SET	R	0h	One or more sources of the INT present in register INT_BUCK_1_2 0h = No bits set in INT_BUCK_1_2 1h = One or more bits set in INT_BUCK_1_2
2	INT_SYSTEM_IS_SET	R	0h	One or more sources of the INT present in register INT_SYSTEM  0h = No bits set in INT_SYSTEM  1h = One or more bits set in INT_SYSTEM
1	INT_RV_IS_SET	R	0h	One or more sources of the INT present in register INT_RV 0h = No bits set in INT_RV 1h = One or more bits set in INT_RV
0	INT_TIMEOUT_RV_SD_I S_SET	R	Oh	One or more sources of the INT present in register INT_TIMEOUT_RV_SD 0h = No bits set in INT_TIMEOUT_RV_SD 1h = One or more bits set in INT_TIMEOUT_RV_SD



# 6.7.41 INT\_LDO\_2 Register (Offset = 2Ch) [Reset = 00h]

INT\_LDO\_2 is shown in Figure 6-58 and described in Table 6-49.

Return to the Summary Table.

# Figure 6-58. INT\_LDO\_2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO2_UV	LDO2_OC	LDO2_SCG
R-0h	R-0h	R-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

# Table 6-49. INT\_LDO\_2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	LDO2_UV	R/W1C	Oh	LDO2 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1' 0h = No Fault detected 1h = Fault detected
1	LDO2_OC	R/W1C	0h	LDO2 Overcurrent Fault 0h = No Fault detected 1h = Fault detected
0	LDO2_SCG	R/W1C	0h	LDO2 Short Circuit to Ground Fault 0h = No Fault detected 1h = Fault detected



# 6.7.42 INT\_LDO\_1 Register (Offset = 2Dh) [Reset = 00h]

INT\_LDO\_1 is shown in Figure 6-59 and described in Table 6-50.

Return to the Summary Table.

# Figure 6-59. INT\_LDO\_1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO1_UV	LDO1_OC	LDO1_SCG
R-0h	R-0h	R-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

### Table 6-50. INT\_LDO\_1 Register Field Descriptions

	Table 5 do. htt_Ebg_1 Register Field Besonptions								
Bit	Field	Type	Reset	Description					
7	RESERVED	R	0h						
6	RESERVED	R	0h						
5	RESERVED	R	0h						
4	RESERVED	R	0h						
3	RESERVED	R	0h						
2	LDO1_UV	R/W1C	0h	LDO1 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'  0h = No Fault detected  1h = Fault detected					
1	LDO1_OC	R/W1C	0h	LDO1 Overcurrent Fault 0h = No Fault detected 1h = Fault detected					
0	LDO1_SCG	R/W1C	0h	LDO1 Short Circuit to Ground Fault 0h = No Fault detected 1h = Fault detected					



# 6.7.43 INT\_BUCK\_3 Register (Offset = 2Eh) [Reset = 00h]

INT\_BUCK\_3 is shown in Figure 6-60 and described in Table 6-51.

Return to the Summary Table.

# Figure 6-60. INT\_BUCK\_3 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	BUCK3_UV	BUCK3_NEG_ OC	BUCK3_OC	BUCK3_SCG
R-0h	R-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

# Table 6-51. INT\_BUCK\_3 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	BUCK3_UV	R/W1C	0h	BUCK3 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1' 0h = No Fault detected 1h = Fault detected
2	BUCK3_NEG_OC	R/W1C	Oh	BUCK3 Negative Overcurrent Fault 0h = No Fault detected 1h = Fault detected
1	BUCK3_OC	R/W1C	Oh	BUCK3 Positive Overcurrent Fault 0h = No Fault detected 1h = Fault detected
0	BUCK3_SCG	R/W1C	Oh	BUCK3 Short Circuit to Ground Fault 0h = No Fault detected 1h = Fault detected



# 6.7.44 INT\_BUCK\_1\_2 Register (Offset = 2Fh) [Reset = 00h]

INT\_BUCK\_1\_2 is shown in Figure 6-61 and described in Table 6-52.

Return to the Summary Table.

### Figure 6-61. INT\_BUCK\_1\_2 Register

		J -	_		•		
7	6	5	4	3	2	1	0
BUCK2_UV	BUCK2_NEG_ OC	BUCK2_OC	BUCK2_SCG	BUCK1_UV	BUCK1_NEG_ OC	BUCK1_OC	BUCK1_SCG
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

# Table 6-52. INT\_BUCK\_1\_2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	BUCK2_UV	R/W1C	Oh	BUCK2 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'  Oh = No Fault detected  1h = Fault detected
6	BUCK2_NEG_OC	R/W1C	0h	BUCK2 Negative Overcurrent Fault  0h = No Fault detected  1h = Fault detected
5	BUCK2_OC	R/W1C	0h	BUCK2 Positive Overcurrent Fault 0h = No Fault detected 1h = Fault detected
4	BUCK2_SCG	R/W1C	0h	BUCK2 Short Circuit to Ground Fault  0h = No Fault detected  1h = Fault detected
3	BUCK1_UV	R/W1C	Oh	BUCK1 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'  Oh = No Fault detected  1h = Fault detected
2	BUCK1_NEG_OC	R/W1C	0h	BUCK1 Negative Overcurrent Fault 0h = No Fault detected 1h = Fault detected
1	BUCK1_OC	R/W1C	0h	BUCK1 Positive Overcurrent Fault 0h = No Fault detected 1h = Fault detected
0	BUCK1_SCG	R/W1C	0h	BUCK1 Short Circuit to Ground Fault 0h = No Fault detected 1h = Fault detected

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback



# 6.7.45 INT\_SYSTEM Register (Offset = 30h) [Reset = 00h]

INT\_SYSTEM is shown in Figure 6-62 and described in Table 6-53.

Return to the Summary Table.

# Figure 6-62. INT\_SYSTEM Register

7	6	5	4	3	2	1	0
SENSOR_0_H OT	SENSOR_1_H OT	SENSOR_2_H OT	SENSOR_3_H OT	SENSOR_0_W ARM	SENSOR_1_W ARM	SENSOR_2_W ARM	SENSOR_3_W ARM
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

# Table 6-53. INT\_SYSTEM Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	SENSOR_0_HOT	R/W1C	0h	TSD Hot detection for sensor 0 0h = No Fault detected 1h = Fault detected
6	SENSOR_1_HOT	R/W1C	Oh	TSD Hot detection for sensor 1 0h = No Fault detected 1h = Fault detected
5	SENSOR_2_HOT	R/W1C	Oh	TSD Hot detection for sensor 2 0h = No Fault detected 1h = Fault detected
4	SENSOR_3_HOT	R/W1C	Oh	TSD Hot detection for sensor 3 0h = No Fault detected 1h = Fault detected
3	SENSOR_0_WARM	R/W1C	0h	TSD Warm detection for sensor 0. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1' 0h = No Fault detected 1h = Fault detected
2	SENSOR_1_WARM	R/W1C	0h	TSD Warm detection for sensor 1. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1'  0h = No Fault detected  1h = Fault detected
1	SENSOR_2_WARM	R/W1C	0h	TSD Warm detection for sensor 2. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1'  0h = No Fault detected  1h = Fault detected
0	SENSOR_3_WARM	R/W1C	0h	TSD Warm detection for sensor 3. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1'  0h = No Fault detected  1h = Fault detected



# 6.7.46 INT\_RV Register (Offset = 31h) [Reset = 00h]

INT\_RV is shown in Figure 6-63 and described in Table 6-54.

Return to the Summary Table.

# Figure 6-63. INT\_RV Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDO2_RV	RESERVED	LDO1_RV	BUCK3_RV	BUCK2_RV	BUCK1_RV
R-0h	R-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

### Table 6-54. INT RV Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	LDO2_RV	R/W1C	0h	RV event detected on LDO2 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state  0h = No RV detected  1h = RV detected
4	RESERVED	R	0h	
3	LDO1_RV	R/W1C	0h	RV event detected on LDO1 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state  0h = No RV detected  1h = RV detected
2	BUCK3_RV	R/W1C	0h	RV event detected on BUCK3 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state  0h = No RV detected  1h = RV detected
1	BUCK2_RV	R/W1C	0h	RV event detected on BUCK2 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state  0h = No RV detected  1h = RV detected
0	BUCK1_RV	R/W1C	0h	RV event detected on BUCK1 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state  0h = No RV detected  1h = RV detected



# 6.7.47 INT\_TIMEOUT\_RV\_SD Register (Offset = 32h) [Reset = 00h]

INT\_TIMEOUT\_RV\_SD is shown in Figure 6-64 and described in Table 6-55.

Return to the Summary Table.

# Figure 6-64. INT\_TIMEOUT\_RV\_SD Register

7	6	5	4	3	2	1	0
TIMEOUT	RESERVED	LDO2_RV_SD	RESERVED	LDO1_RV_SD	BUCK3_RV_SD	BUCK2_RV_SD	BUCK1_RV_SD
R/W1C-0h	R-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

# Table 6-55. INT\_TIMEOUT\_RV\_SD Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	TIMEOUT	R/W1C	Oh	Is set if ShutDown occurred due to a TimeOut while: 1. Transitioning to ACTIVE state, and one or more rails did not rise past the UV level at the end of the assigned slot (and UV on this rail is configured as a SD fault). Which rail(s) is/are indicated by the *_UV bits in the INT_* registers. 2. Transitioning to STANDBY state, and one or more rails did not fall below the SCG level at the end of the assigned slot and discharge is enabled for that rail (which rail(s) is/are indicated by the corresponding RV_SD bit(s) in this register).  0h = No SD due to TimeOut occurred 1h = SD due to TimeOut occurred
6	RESERVED	R	0h	
5	LDO2_RV_SD	R/W1C	0h	RV on LDO2 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)  0h = No SD due to RV/DISCHARGE_TIMEOUT on LDO2 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on LDO2 occurred
4	RESERVED	R	0h	
3	LDO1_RV_SD	R/W1C	Oh	RV on LDO1 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)  0h = No SD due to RV/DISCHARGE_TIMEOUT on LDO1 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on LDO1 occurred
2	BUCK3_RV_SD	R/W1C	0h	RV on BUCK3 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)  0h = No SD due to RV/DISCHARGE_TIMEOUT on BUCK3 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on BUCK3 occurred

Product Folder Links: TPS65215-Q1

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated



# Table 6-55. INT\_TIMEOUT\_RV\_SD Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
1	BUCK2_RV_SD	R/W1C	Oh	RV on BUCK2 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)  0h = No SD due to RV/DISCHARGE_TIMEOUT on BUCK2 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on BUCK2 occurred
0	BUCK1_RV_SD	R/W1C	Oh	RV on BUCK1 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)  0h = No SD due to RV/DISCHARGE_TIMEOUT on BUCK1 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on BUCK1 occurred



# 6.7.48 INT\_PB Register (Offset = 33h) [Reset = 04h]

INT\_PB is shown in Figure 6-65 and described in Table 6-56.

Return to the Summary Table.

# Figure 6-65. INT\_PB Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PB_REAL_TIM E_STATUS	PB_RISING_E DGE_DETECT ED	PB_FALLING_E DGE_DETECT ED
R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R/W1C-0h	R/W1C-0h

# Table 6-56. INT\_PB Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	PB_REAL_TIME_STATUS	R	1h	Deglitched (64-128ms) real-time status of PB pin. Valid only when EN/PB/VSENSE pin is configured as PB.  0h = Current deglitched status of PB: PRESSED  1h = Current deglitched status of PB: RELEASED
1	PB_RISING_EDGE_DET ECTED	R/W1C	0h	PB was released for > deglitch period (64-128ms) since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK_INT_FOR_PB='0').  0h = No PB-release detected  1h = PB-release detected
0	PB_FALLING_EDGE_DE TECTED	R/W1C	0h	PB was pressed for > deglitch period (64-128ms) since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK_INT_FOR_PB='0').  0h = No PB-press detected 1h = PB-press detected



# 6.7.49 USER\_NVM\_CMD\_REG Register (Offset = 34h) [Reset = 00h]

USER\_NVM\_CMD\_REG is shown in Figure 6-66 and described in Table 6-57.

Return to the Summary Table.

# Figure 6-66. USER\_NVM\_CMD\_REG Register

7	6	5	4	3	2	1	0
NVM_VERIFY_ RESULT	CUST_NVM_V ERIFY_DONE	CUST_PROG_ DONE	I2C_OSC_ON		USER_N\	/M_CMD	
R-0h	R/W1C-0h	R/W1C-0h	R-0h		R-0	Oh	

### Table 6-57. USER\_NVM\_CMD\_REG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	NVM_VERIFY_RESULT	FY_RESULT R 0h		After an CUST_NVM_VERIFY_CMD is executed, this bit gives the result of the operation. (1 = fail, 0= pass). If '1', this bit is only cleared if a subsequent CUST_NVM_VERIFY_CMD passes.  0h = PASS 1h = FAIL
6	CUST_NVM_VERIFY_DO	R/W1C	Oh	Is set to '1' after a CUST_NVM_VERIFY_CMD is executed. Remains '1' until W1C by user.  0h = Not yet done / not in progress 1h = Done
5	CUST_PROG_DONE	R/W1C	Oh	Is set to '1' after a CUST_PROG_CMD is executed. Remains '1' until W1C by user.  0h = Not yet done / not in progress 1h = Done
4	I2C_OSC_ON	R	Oh	This register field is set to '1' if an EN_OSC_DIY is received.  0h = OSC not controlled via I2C  1h = OSC unconditionally ON due to I2C command EN_OSC_DIY
3-0	USER_NVM_CMD	R	Oh	Commands to enter DIY programming mode and program user NVM space. Always reads as 0. 6h = DIS_OSC_DIY 7h = CUST_NVM_VERIFY_CMD 9h = EN_OSC_DIY Ah = CUST_PROG_CMD



# 6.7.50 POWER\_UP\_STATUS\_REG Register (Offset = 35h) [Reset = 00h]

POWER\_UP\_STATUS\_REG is shown in Figure 6-67 and described in Table 6-58.

Return to the Summary Table.

# Figure 6-67. POWER\_UP\_STATUS\_REG Register

7	6	5	4	3	2	1	0
POWER_UP_F ROM_FSD	POWER_UP_F ROM_EN_PB_ VSENSE	COLD_RESET_ ISSUED	STATE		RETRY_	COUNT	POWER_UP_F ROM_OFF
R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h		R-0	)h	R/W1C-0h

# Table 6-58. POWER\_UP\_STATUS\_REG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	POWER_UP_FROM_FSD	R/W1C	0h	Is set if ON_REQ was triggered due to FSD  0h = No power-up via FSD detected  1h = Power-up via FSD detected
6	POWER_UP_FROM_EN_ PB_VSENSE	R/W1C	0h	Is set if ON_REQ was triggered due to EN/PB/VSENSE pin 0h = No power-up via pin detected 1h = Power-up via pin detected
5	COLD_RESET_ISSUED	R/W1C	0h	Is set if we received a COLD_RESET over pin or over I2C 0h = No COLD RESET received 1h = COLD RESET received either through pin or I2C
4-3	STATE	R	0h	Indicates the current device state  0h = Transition state  1h = INITIALIZE  2h = STANDBY  3h = ACTIVE
2-1	RETRY_COUNT	R	0h	Reads the current retry count in the state machine. If RETRY_COUNT = 3 and is not masked, device does not power up.
0	POWER_UP_FROM_OFF	R/W1C	0h	Indicates if we powered up from OFF state (POR was asserted) 0h = OFF state not entered since the previous clearing of this bit 1h = OFF state was entered since the previous clearing of this bit

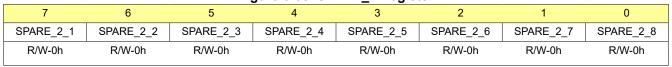


# 6.7.51 SPARE\_2 Register (Offset = 36h) [Reset = 00h]

SPARE\_2 is shown in Figure 6-68 and described in Table 6-59.

Return to the Summary Table.

# Figure 6-68. SPARE\_2 Register



### Table 6-59. SPARE\_2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	SPARE_2_1	R/W	0h	Spare bit in user non-NVM space
6	SPARE_2_2	R/W	0h	Spare bit in user non-NVM space
5	SPARE_2_3	R/W	0h	Spare bit in user non-NVM space
4	SPARE_2_4	R/W	0h	Spare bit in user non-NVM space
3	SPARE_2_5	R/W	0h	Spare bit in user non-NVM space
2	SPARE_2_6	R/W	0h	Spare bit in user non-NVM space
1	SPARE_2_7	R/W	0h	Spare bit in user non-NVM space
0	SPARE_2_8	R/W	0h	Spare bit in user non-NVM space

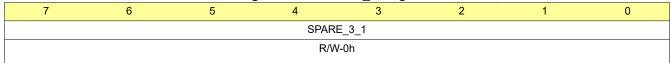


# 6.7.52 SPARE\_3 Register (Offset = 37h) [Reset = 00h]

SPARE\_3 is shown in Figure 6-69 and described in Table 6-60.

Return to the Summary Table.

# Figure 6-69. SPARE\_3 Register



# Table 6-60. SPARE\_3 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	SPARE_3_1	R/W	0h	Spare bit in user non-NVM space

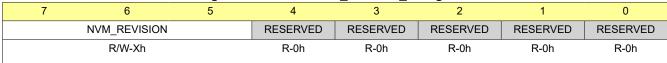


# 6.7.53 FACTORY\_CONFIG\_2 Register (Offset = 41h) [Reset = XXh]

FACTORY\_CONFIG\_2 is shown in Figure 6-70 and described in Table 6-61.

Return to the Summary Table.

# Figure 6-70. FACTORY\_CONFIG\_2 Register



# Table 6-61. FACTORY\_CONFIG\_2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	NVM_REVISION	R/W	Х	Specifies the version of the NVM configuration Note: This register can be programmed only by the manufacturer. $0h = V0$ $1h = V1$
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	



## 7 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

The following sections provide more detail on the proper utilization of the PMIC. Each orderable part number has unique default non-volatile memory (NVM) settings and the relevant Technical Reference Manual (TRM) for that orderable is available in the product folder, under Technical Documentation. Refer to these TRMs for specific application information. More generic topics and some examples are outlined here.

To help with new designs, a variety of tools and documents are available in the product folder. Some examples are:

- Evaluation module and user guide.
- GUI to communicate with the PMIC
- Schematic and layout checklist
- User's guide describing how to power specific processors and SoCs with the PMIC.
- Technical Reference Manual (TRM) describing the default register settings on each orderable.

### 7.2 Typical Application

The TPS65215-Q1 PMIC contains five regulators; 3 Buck converters and 2 Low Drop-out Regulators (LDOs). In addition to the power resources, it also integrates 3 configurable multi-function pins, 1 GPIO, 2 GPOs and I2C communication making this power management IC a cost and size optimized solution to power multiple processors and SoCs. There are several considerations to take into account when designing the TPS65215-Q1 to power a processor and peripherals. The number of regulators needed, the required sequencing, the load current requirements, and the voltage characteristics are all critical in determining the number of supply rails as well as the external components used with it. The following section provides a generic case. For specific cases, refer to the relevant user's guide and TRM based on the orderable part number.

#### 7.2.1 Typical Application Example

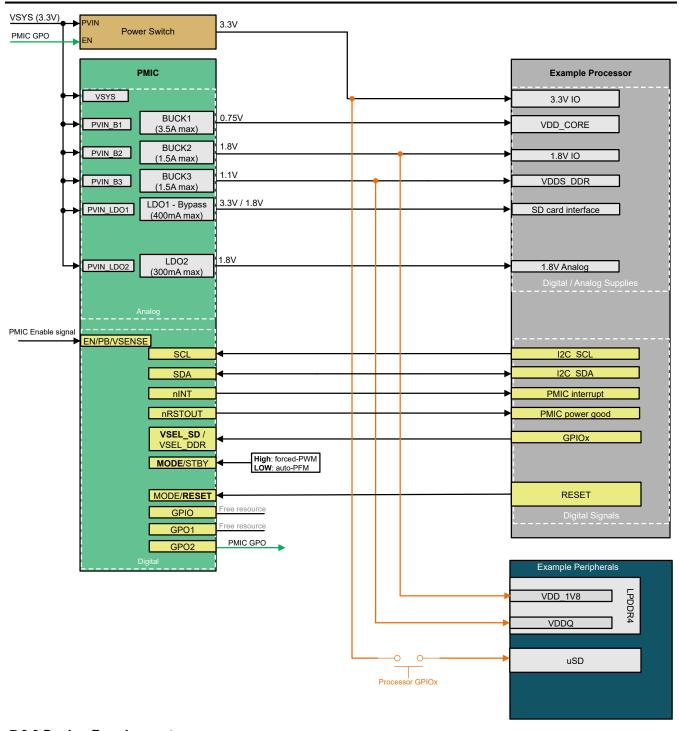
In this example, a single TPS65215-Q1 PMIC is used to power a generic processor. This power distribution network (PDN) shows a 3.3V input supply. LDO1 is configured as bypass and assigned to supply the SD card interface. The bypass mode allows voltage change between VSET LDO1 and 1.8V to meet the SD spec for UHS speed which requires 3.3V to initialize the card before the voltage is optionally lowered to 1.8V for faster rise/fall time and lower electromagnetic interference. The VSEL SD multifunction pin is configurable to trigger the voltage change during operation. Since Buck1 is the regulator with the highest current capability, it is assigned to supply the CORE rail of the processor. Each of the Buck regulators have the option to be configured for high bandwidth to support higher load transients and higher total capacitance (local + point of load). Since the PMIC is being supplied by a 3.3V rail, an external load switch is used to supply the 3.3V IO domain on the processor. One of the PMIC GPOs (GPO2) is configured to be part of the power-up/power-down sequence and enables the external power-switch.

### Note

If an external discrete is used to supply the 3.3V IO, it must be chosen with active discharge so the voltage discharges after the PMIC GPO2 disables it.

Figure 7-1. Example Power Map





### 7.2.2 Design Requirements

The design requirements for the typical application described on this section are outlined below:

- VDD CORE rail requires 0.75V rail with high loadtransient response.
- Low noise 1.8V required to supply the analog.
- 3.3V and 1.8V required to supply processor IO domains and peripherals.
- LPDDR4 requires a 1.1V rail.



### 7.2.3 Detailed Design Procedure

This section describes the design procedure for each of the power modules integrated in the TPS65215-Q1 PMIC. Please note, most of the external component values that are mentioned in this section are based on the typical spec. For minimum and maximum values, refer to the corresponding parameter in the Specifications section.

### 7.2.3.1 Buck1, Buck2, Buck3 Design Procedure

### Input Capacitance - Buck1, Buck2, Buck3

Each of the Buck converters require an input capacitor on the corresponding PVIN Bx pin. The capacitor value must be selected taking into account the voltage and temperature de-rating. Due to the nature of the switching converter, a low ESR ceramic capacitor is required for best input voltage filtering. The typical recommended capacitance is 4.7uF, 10V capacitor. Higher input capacitance is acceptable if the PCB size allows larger footprint.

### Output Capacitance - Buck1, Buck2, Buck3

Every Buck output requires a local output capacitor to form the capacitive part of the LC output filter. Ceramic capacitor with X7 temperature coefficient are recommended. Cost optimize for non-automotive applications by using X6 or lower based on the operating temperature. The Buck converters have multiple switching modes and bandwidth configuration that impact the output capacitor selection. The switching mode configuration (BUCK FF ENABLE) is a global register field that applies to the three Buck converters and must not be changed at any point. The bandwidth selection is an independent register field for each Buck converter. Refer to the Technical Reference Manual (TRM) for the specific orderable part number to identify the NVM configuration and the corresponding output capacitance requirements. Table 7-1 shows the required minimum and maximum capacitance (after derating) for each switching mode and bandwidth configuration. DC bias voltage characteristics of ceramic capacitors, tolerance, aging and temperature effects must be considered. ESR must be  $10m\Omega$  or lower.

**Switching Mode Selection Bandwidth Selection** Spec parameter Capacitance Register fields: Max Register Field: BUCK1\_BW\_SEL, (Includes local + point of Min BUCK\_FF\_ENABLE BUCK2 BW SEL, load) **BUCK3 BW SEL** COUT 75uF Low Bandwidth 10uF Quasi-fixed frequency (auto-PFM or forced-PWM) 30uF High Bandwidth COUT HIGH BW 220uF Fixed Frequency Low Bandwidth COUT FF 12uF 36uF (supported on TPS65220, High Bandwidth COUT HIGH BW FF 48uF 144uF TPS65220-EP, TPS65219-Q1, and TPS65215-Q1)

Table 7-1. Buck Output Capacitance

### Inductor Selection - Buck1, Buck2, Buck3

Internal parameters for the buck converters are optimized for 0.47uH inductor. DCR must be 50mΩ or lower. TI recommends that the selected inductor is rated to support saturation current of at least 7.4A for Buck1 and 5.4A for Buck2/Buck3.



### 7.2.3.2 LDO1 Design Procedure

### Input Capacitance - LDO1

LDO inputs require an input decoupling capacitor to minimize input ripple voltage. Using a typical of 2.2µF capacitance for each LDO is recommended. Depending on the input voltage of the LDO, use a 6.3V or higher rated capacitor. The same input capacitance requirements applies when the LDO is configured as LDO, bypass or "load-switch.

### **Output Capacitance - LDO1**

LDO outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. Using a  $2.2\mu F$  local capacitance for each LDO output with ESR of  $10m\Omega$  or less is recommended. Local capacitance must not exceed 4uF (after derating). This requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. The total capacitance (local + point of load) that each LDO supports depends on the NVM configuration. Table 7-2 shows the maximum total output capacitance allowed based on the rail configuration. Refer to the Technical Reference Manual (TRM) for the specific orderable part number to identify the LDO configuration based on the register settings and the applicable max total capacitance.

Table 7-2. LDO1 Output Capacitance

Registe	er setting	LDO config	Max total capacitance (2.2uF local +	
LDOx_LSW_CONFIG	LDOx_BYP_CONFIG	LDO comig	point of load)	
0	0	LDO	20uF	
0	1	Bypass	50uF	
1	X	Load-switch	50uF	

#### 7.2.3.3 LDO2 Design Procedure

#### Input Capacitance - LDO2

The input supply pin for LDO2 requires an input decoupling capacitor to minimize input ripple voltage. Using a minimum of 2.2µF input capacitance is recommended. Depending on the input voltage of the LDO, use a 6.3V or higher rated capacitor. The same input capacitance requirements applies when the LDO is configured as LDO or load-switch.

#### **Output Capacitance - LDO2**

LDO outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. Using a 2.2μF local capacitance for each LDO output with ESR of 10mΩ or less is recommended. Local capacitance must not exceed 4uF (after derating). This requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. The total capacitance (local + point of load) that each LDO supports depends on the NVM configuration. Table 7-3 shows the maximum total output capacitance allowed. Refer to the Technical Reference Manual (TRM) for the specific orderable part number to identify the LDO configuration based on the register settings and the applicable maximum total capacitance.

Table 7-3. LDO2 output capacitance

Register setting  LDOx_SLOW_PU_RAMP	LDO ramp config	Max total capacitance (2.2uF local + point of load)
0	fast ramp	15uF
1	slow ramp	30uF



#### 7.2.3.4 VSYS, VDD1P8

The VSYS pin provides power to the internal VDD1P8 LDO and other internal functions. This pin requires a typical of 2.2uF ceramic capacitor. Increase the input capacitance without any limit for better input-voltage filtering. On a typical application, this pin is connected to the same pre-regulator that supplies the PVIN Bx pins.

VDD1P8 in an internal reference LDO and must not have any load. This pin requires a 2.2uF ceramic capacitor.

#### 7.2.3.5 Digital Signals Design Procedure

This section describes the external connections required for the digital pins. A VIO supply of 3.3V or 1.8V supply is commonly used as the voltage level for the digital signals that require an external pull-up. However, the device also supports any higher voltage up to the maximum spec. The VIO supply for the digital pins on the PMIC must be the same as the IO domain for the digital signal that is connected to on the processor.  $100k\Omega$  is the recommended pull-up resistor for EN/PB/VSENSE. Calculate the pull-up resistor for I2C pins based on system requirements.  $10k\Omega$  is recommended for all other digital pins.

If GPIO, GPO1 or GPO2 is assigned to the first slot of the power-up sequence to enable an external discrete, pull the pin up to VSYS.

Externally drive the EN/PB/VSENSE pin to enable or disable the PMIC. If the application does not have an external signal dedicated to drive this pin, pull the pin up to VSYS.

#### Note

Driving the EN/PB/VSENSE pin with an external signal is needed to wake-up the PMIC after an I2C OFF request is sent by I2C (I2C\_OFF\_REQ). If an OFF request is sent by I2C and the EN/PB/ VSENSE is not driven by an external signal, a power cycle on VSYS must be performed to transfer the PMIC from Initialize state to Active.

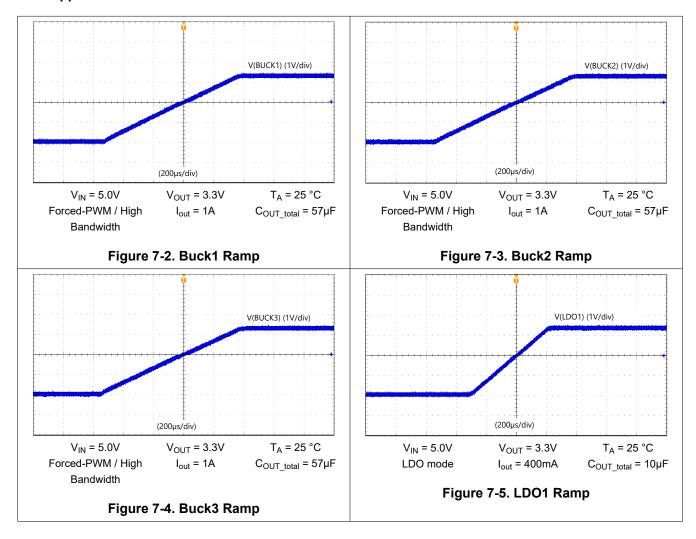
Table 7-4. Digital Signals Requirements

Digital Pin	External Connection
nINT	Open-drain output. Requires external pull-up.
nRSTOUT	Open-drain output. Requires external pull-up.
EN/PB/VSENSE	When configured as EN, drive this signal with external logic to enable or disable the PMIC, or pull this pin up to VSYS.  When configured as PB, this signal requires a pull-up resistor connected to the VSYS pin. Push-button is optional.  When configured as VSENSE, this signal requires an external resistor divider to monitor the pre-regulator.
SDA	I2C clock signal. Requires external pull-up.
SCL	I2C data signal. Requires external pull-up.
GPIO	When configured as GPIO (for multi-PMIC), this pin shares the external pull-up resistor with the second TPS65215-Q1 PMIC. When configured as GPO (for single PMIC), requires external pull-up.
GPO1	Open-drain general purpose output. Requires external pull-up.
GPO2	Open-drain general purpose output. Requires external pull-up.
VSEL_SD / VSEL_DDR	Input digital pin. The initial state (pull-up or pull-down) must be set before the assigned PMIC rail ramps up. For example, if this pin is used to set the voltage on LDO1, the state must be set before LDO1 powers up.
MODE / STBY	Input digital pin. The initial state (pull-up or pull-down) must be set before the power-up sequence is complete.

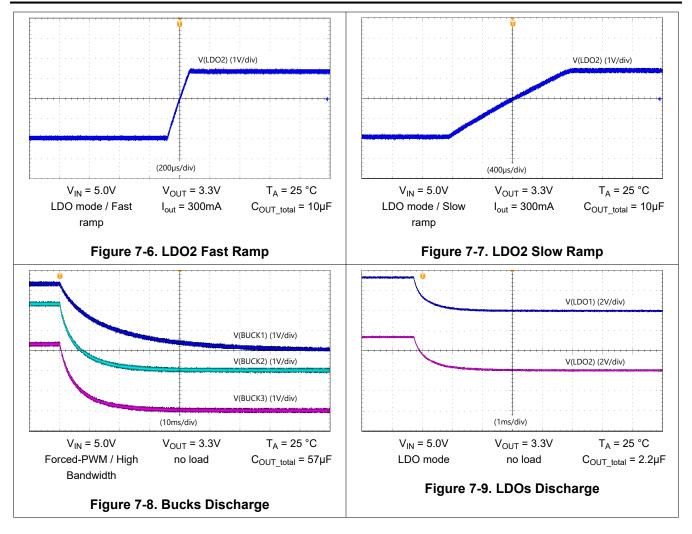
Table 7-4. Digital Signals Requirements (continued)

Digital Pin	External Connection
	Input digital pin. The initial state (pull-up or pull-down) must be set before the power-up sequence is complete.

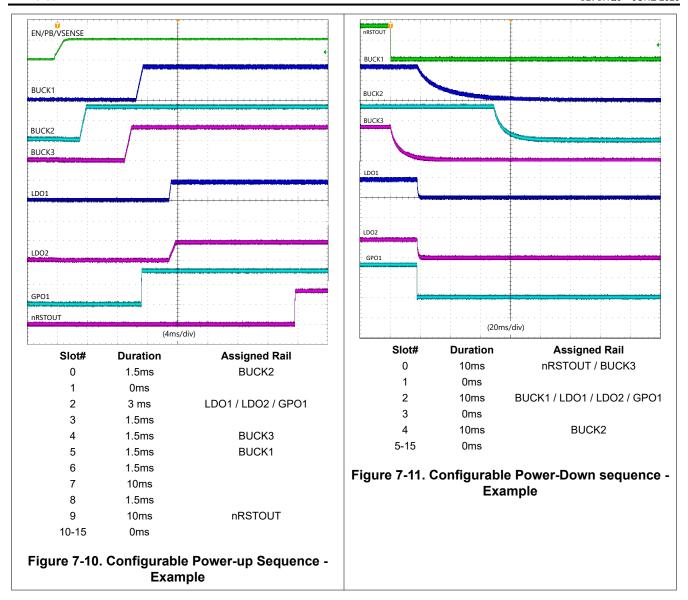
### 7.2.4 Application Curves











### 7.3 Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 2.5V and 5.5V. Examples of input supplies include a single cell Li-Ion battery, two primary cells or a regulated pre-regulator. The voltage headroom required for each of the PMIC regulators must be taken into account when defining selecting the supply voltage. For example, if the Bucks require 700mV head room and the output voltage is configured as 3.3V, then the input supply must be at least 4V to allow sufficient headroom. Design the resistance of the input supply rail low enough such that the input current transient does not cause too high of a drop in the device supply voltage. This drop has the ability to cause a false UVLO fault triggering. If the input supply is located more than a few inches from the device, consider additional bulk capacitance in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of  $47\mu\text{F}$  is a typical choice. When using a pre-regulator to supply the PMIC, it is recommended to select the pre-regulator without active discharge to hold the voltage at the input of the PMIC for as long as possible during a uncontrolled power-down.

### **CAUTION**

Sequencing and Voltage requirements: The voltage on PVIN\_Bx, and PVIN\_LDOx must not exceed VSYS. The Pull-up supply for the digital signals must not exceed VSYS at any point.



### 7.4 Layout

### 7.4.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design. If the layout is not carefully done, the regulators' stability and EMI is impacted. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitors, output capacitors, and inductors must be placed as close as possible to the device. The output capacitors must have a low impedance to ground. Use multiple VIAS (at least three) directly at the ground landing pad of the capacitor. Here are some layout guidelines:

- PVIN\_Bx: Place the input capacitor as close to the IC as allowed by the layout DRC rules. Any extra parasitic inductance between the input cap and the PVIN Bx pin increases the voltage spike. TI recommends to have wide a short trace or polygon to help minimize trace inductance. Do not route any sensitive signals close to the input cap and the device pin as this node has high frequency switching currents. Add 3-4 vias per amp of current on the GND pads for each DCDC. If the space is limited and does not allow to place the input capacitors on the same layer as the PMIC, then place the input capacitors on the opposite layer with VIAS, close to the IC, and add a small input capacitor (0.1uF) on the same layer as the PMIC. This small capacitor must be placed close to the PVIN Bx pin.
- LX Bx: Place the inductor close to the PMIC without compromising the PVIN input caps and use short a wide traces or polygons to connect the pin to the inductor. Do not route any sensitive signals close to this node. The inductor must be placed in the same layer as the IC to prevent having to use VIAS in the SW node. Since the SW-node voltage swings from the input voltage to ground with very fast rise and fall times, this node is the main generator of EMI. If needed, to reduce EMI, add a RC snubber to the SW node.
- FB Bx: Route each of the FB Bx pins as a trace to the output capacitor. Do not extend the output voltage polygon to the FB Bx pin as this pin requires to be routed as a trace. The trace resistance from the output capacitor to the FB Bx pin must be less than 1Ω. The TPS65215-Q1 does not support remote sensing so the FB Bx pins must be connected to the local capacitor of the PMIC. Avoid routing the FB Bx close to any noisy signals such as the switch node or under the inductor to avoid coupling. If space is a constraint, route the FB Bx pin through an inner layer. See example layout.
- Bucks Cout: The local output capacitors must be placed as close to the inductor as possible to minimize electromagnetic emissions.
- **PVIN LDOx**: Place the input capacitor as close as possible to the PVIN LDOx pin.
- VLDOx: Place the output capacitor close to the VLDOx pin. For the LDO regulators, the feedback connection is internal. Therefore, keep the PCB resistance between LDO output and target load in the range of the acceptable voltage, IR, drop for LDOs.
- VSYS: Connect VSYS directly to a quiet system voltage node. Place the decoupling capacitor as close as possible to the VSYS pin.
- **VDD1P8**: Place the 2.2uF cap as close as possible to the VDD1P8 pin. This capacitor needs to be placed in the same layer as the IC. Use two to three VIAS to connect the GND side of the capacitor to the GND plane of the PCB.
- **Power Pad:** The thermal pad must be connected to the PCB ground plane with a minimum of nine VIAS.
- AGND: Do not connect AGND to the power pad (or thermal pad). The AGDN pin must be connected to the PCB ground planes through a VIA. Keep the trace from the AGDN pin to the VIA short.

# 7.4.2 Layout Example

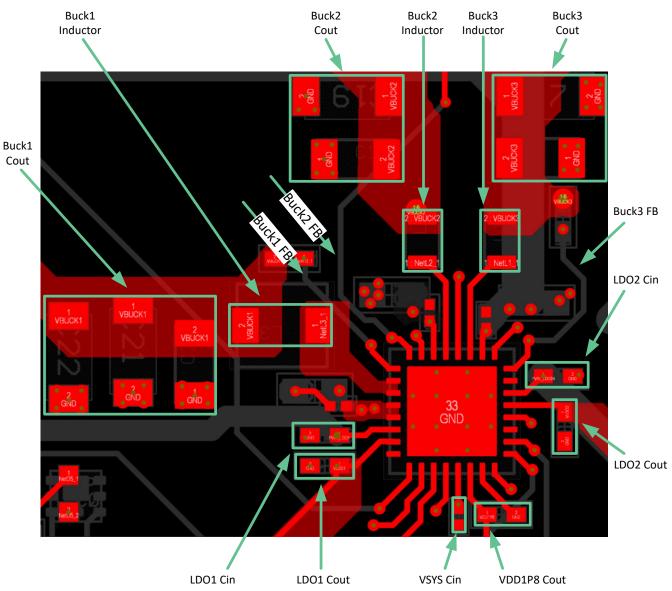


Figure 7-12. Example PMIC Layout

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 8.3 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

### 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2025	*	Initial Release

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback

www.ti.com 14-Oct-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
TPS6521501WRHBRQ1	Active	Production	VQFN (RHB)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65215Q NVM 01

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

# PACKAGE MATERIALS INFORMATION

www.ti.com 11-Oct-2025

### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6521501WRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

# PACKAGE MATERIALS INFORMATION

www.ti.com 11-Oct-2025



### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6521501WRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



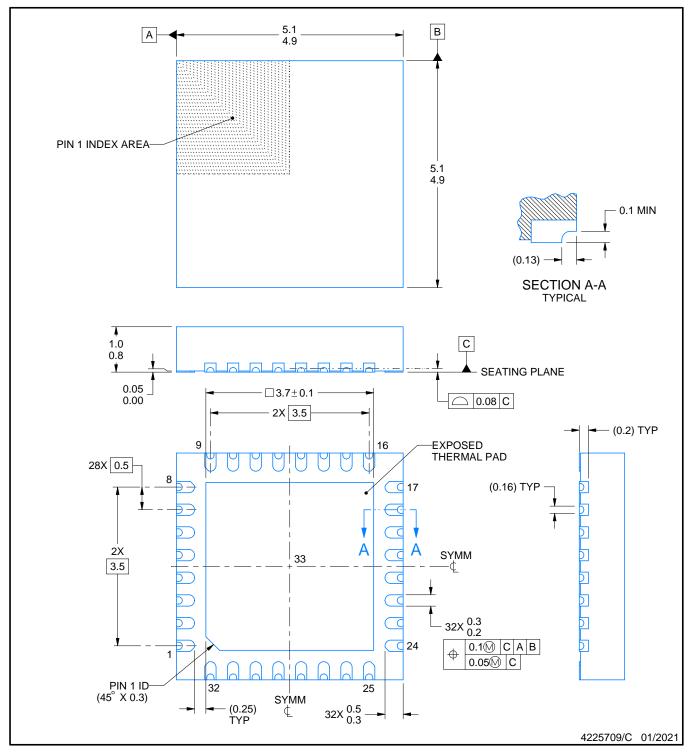
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4224745/A





PLASTIC QUAD FLATPACK - NO LEAD



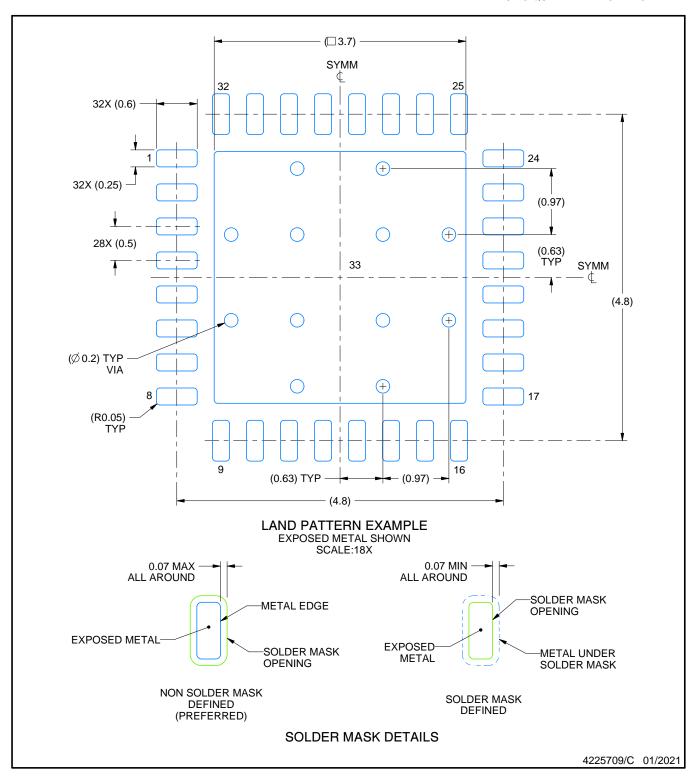
### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

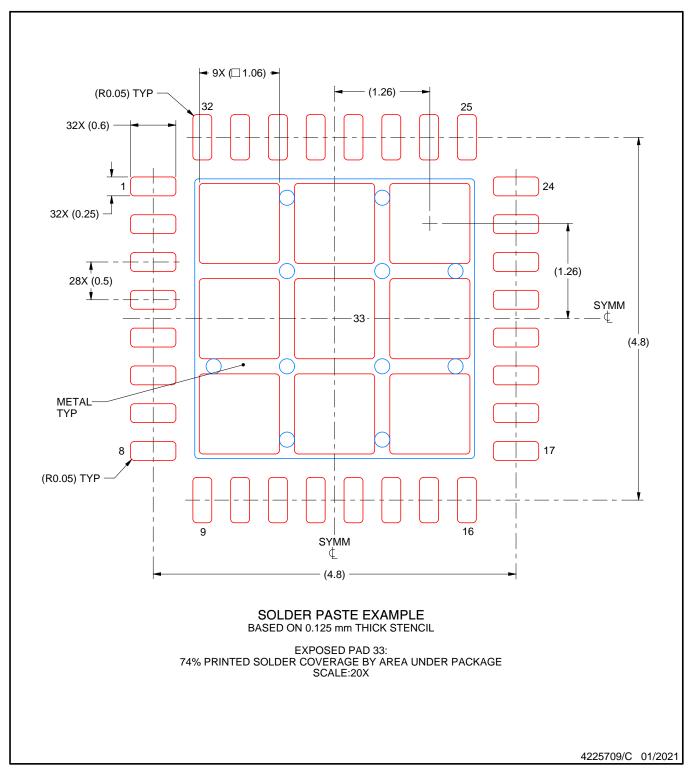


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025. Texas Instruments Incorporated