

Dual High-Voltage Scan Driver for TFT-LCD

Check for Samples: [TPS65193](#)

FEATURES

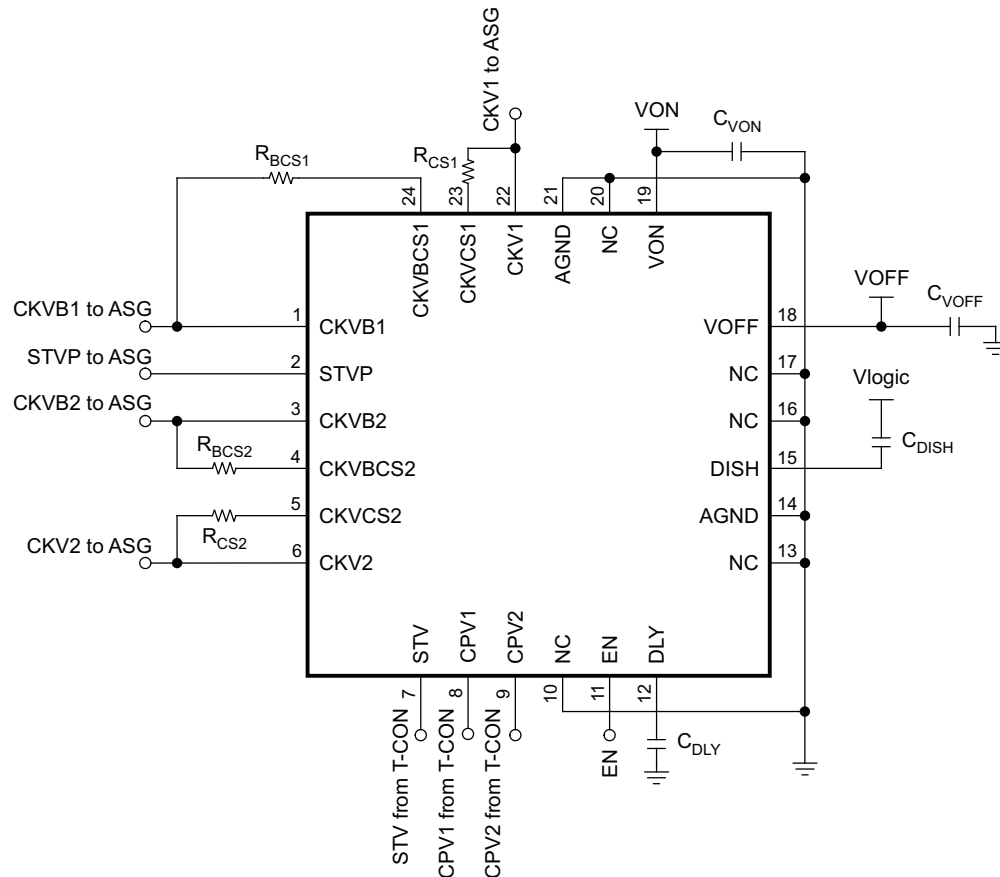
- Dual High-Voltage Scan Driver
- Scan Driver Output Charge Share
- High Output-Voltage Level: Up to 35 V
- Low Output-Voltage Level: Down to –28 V
- Logic-Level Inputs
- 24-Pin 4-mm × 4-mm QFN package

APPLICATIONS

- TFT LCD Using Amorphous Silicon Gate (ASG) Technology

DESCRIPTION

The TPS65193 is dual high-voltage scan driver to drive an amorphous-silicon-gate (ASG) circuit on TFT glass. Each single high-voltage scan driver receives logic-level inputs of CPVx and generates two high-voltage outputs of CKVx and CKVBx. The device receives a logic-level input of STV and generates a high-voltage output of STVP. These outputs are swings from Voff (–28 V) to Von (35 V) and are used to drive the ASG circuit and charge/discharge the capacitive loads of the TFT LCD. In order to reduce the power dissipation of the device, a charge-share function is implemented. The device features a discharge function, which shorts Voff to GND in order to shut down the panel faster when the LCD is turned off.



S0418-01



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TPS65193

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _A	ORDERING P/N	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65193RGE	24-Pin 4-mm x 4-mm QFN	TPS65193

(1) The RGE package is available taped and reeled and shipped in quantities of 2500 devices per reel.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Voltage on pins CPVx, STV	–0.3 to 5.5	V
Voltage on pins EN	–0.3 to 5.5	V
Input voltage on VON ⁽²⁾	40	V
Input voltage on VOFF ⁽²⁾	–30	V
Voltage on CKVx, CKVBx, CKVCSx, CKVBCSx	–30 to 40	V
VON–VOFF	62	V
Voltage on STVP	–30 to 40	V
Voltage on DISH	–3.6 to 5.5	V
ESD rating HBM	2	kV
ESD rating MM	200	V
ESD rating CDM	700	V
Continuous power dissipation	See <i>Dissipation Ratings</i> table	
Operating junction temperature range	–40 to 150	°C
Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	R _{θJA}	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
24-pin 4-mm x 4-mm QFN	88°C/ W (Low-K board)	1.13 W	0.62 W	0.45 W

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
VON Positive high-voltage range	15		35	V
VOFF Negative low-voltage range	–28		–3	V
VON–VOFF VON to VOFF voltage range			60	V
f _{CPV} CPV input frequency			150	kHz
T _A Operating ambient temperature	–40		85	°C
T _J Operating junction temperature	–0		125	°C

ELECTRICAL CHARACTERISTICS

VOFF = –10 V, VON = 30 V, EN = 3.3 V, TA = –40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{QIN}	Quiescent current into VON	CPVx = GND, STV = 3.3 V		600	800	μA
	Quiescent current out of VOFF			120	200	
I _{SD}	Shutdown current into VON	CPVx = GND, STV = 3.3 V EN = GND		520	800	μA
	Shutdown current out of VOFF			260	400	
UNDERVOLTAGE LOCKOUT						
V _{UVLO}	Undervoltage lockout threshold on VON	VON rising		10	13	V
		Hysteresis		250		mV
LOGIC SIGNALS EN, CPVx, STV						
V _{IH}	High-level input voltage of CPVx, STV, EN			2		V
V _{IL}	Low-level input voltage of CPVx, STV, EN				0.5	V
OUTPUT CKVx, CKVBx, STVP, CKVCSx						
V _{OH}	Output high voltage of CKVx, CKVBx	I _{OH} = 10 mA		VON – 0.3		V
	Output high voltage of STVP			VON – 0.8		
V _{OL}	Output low voltage of CKVx, CKVBx	I _{OL} = –10 mA			VOFF + 0.2	V
	Output low voltage of STVP				VOFF + 0.4	
R _{CHSH}	Charge-sharing on-resistance	I _{CHSH} = 10 mA		120		Ω
DISCHARGING CIRCUIT						
R _{DSCHG}	Discharging resistance	DISH = –2 V		1.5		kΩ
R _{BIAS}	Resistance DISH to GND			100		kΩ
CONTROL DELAY						
V _{DLYREF}	Reference voltage for comparator			2.9		V
I _{DLYREF}	Delay charge current			15		μA
R _{DLY}	Delay resistor		140	200	260	kΩ

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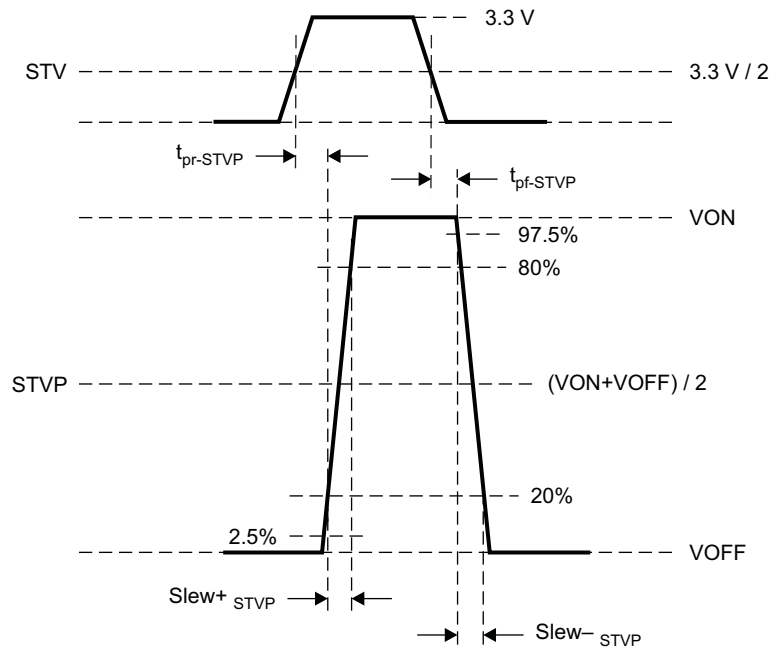
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ELECTRICAL CHARACTERISTICS (continued)

VOFF = -10 V, VON = 30 V, EN = 3.3 V, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS						
Slew-	Slew rate, Slew- _{STVP}	Load = 4.7 nF (See Figure 1)	30	55		V/ μ s
Slew+	Slew rate, Slew+ _{STVP}		20	35		V/ μ s
t_{pf}	Propagation delay, $t_{pf-STVP}$			40	100	ns
t_{pr}	Propagation delay, $t_{pr-STVP}$			30	100	ns



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Figure 1. Switching Characteristics of STVP

CKVx, CKVBx SWITCHING CHARACTERISTICS

VOFF = -10 V, VON = 30 V, EN = 3.3 V, $T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{csf}	t _{csf-CPVx_CKVx} , t _{csf-CPVx_CKVBx}	f _{CPVx} = 85 kHz, STV = GND, See Figure 2, load = 4.7 nF, R _{CS1} = R _{B_{CS1}} = R _{CS2} = R _{B_{CS2}} = 50 Ω		80	150	ns
t _{csr}	t _{csr-CPVx_CKVx} , t _{csr-CPVx_CKVBx}			80	150	ns
t _f	t _{f-CPVx_CKVx} , t _{f-CPVx_CKVBx}			40	100	ns
t _r	t _{r-CPVx_CKVx} , t _{r-CPVx_CKVBx}			30	100	ns

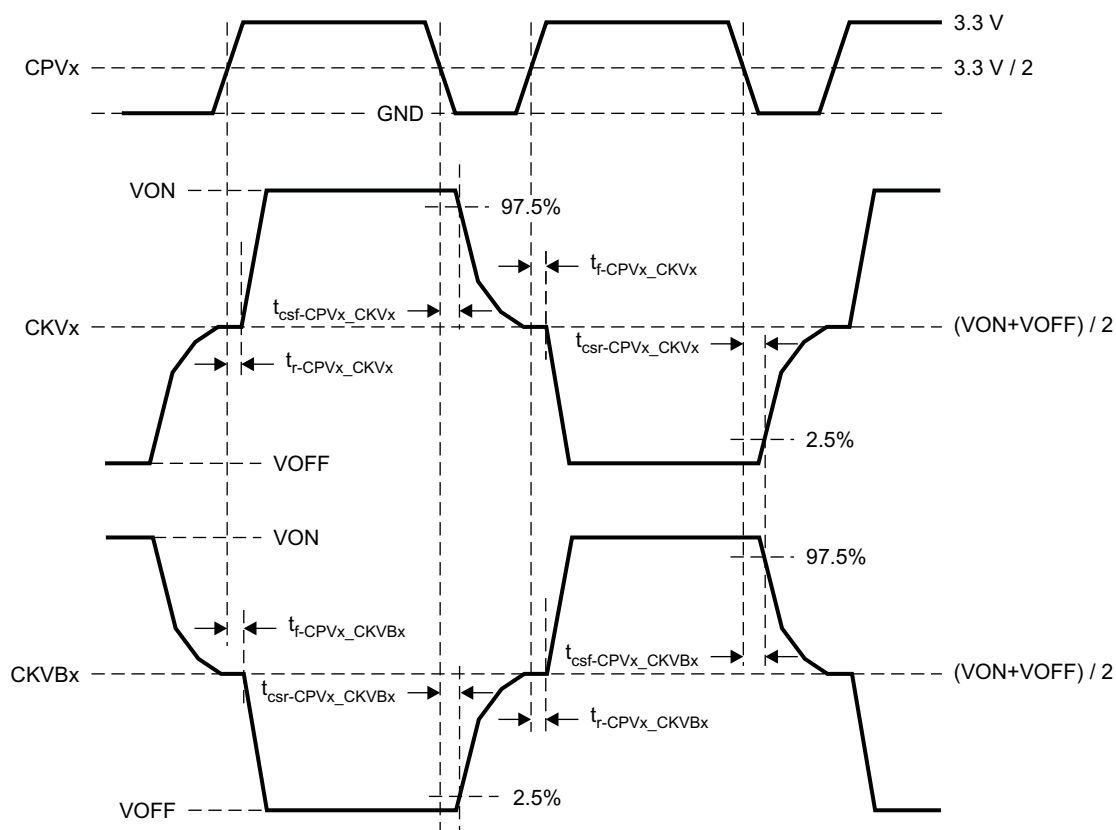


Figure 2. Switching Characteristics of CKVx, CKVBx (STV = GND)

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CKVx, CKVBx SWITCHING CHARACTERISTICS (Continued)

 $V_{OFF} = -10\text{ V}$, $V_{ON} = 30\text{ V}$, $EN = 3.3\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew+ Slew+ CKVx, Slew+ CKVBx	$f_{CPVx} = 85\text{ kHz}$, $STV = 3.3\text{ V}$, See Figure 3 , load = 4.7 nF , $R_{CSx} = R_{BCSx} = 50\ \Omega$	50	100		$\text{V}/\mu\text{s}$
Slew– Slew– CKVx, Slew– CKVBx	$f_{CPVx} = 85\text{ kHz}$, $STV = 3.3\text{ V}$, See Figure 3 , load = 4.7 nF , $R_{CSx} = R_{BCSx} = 50\ \Omega$	70	130		$\text{V}/\mu\text{s}$

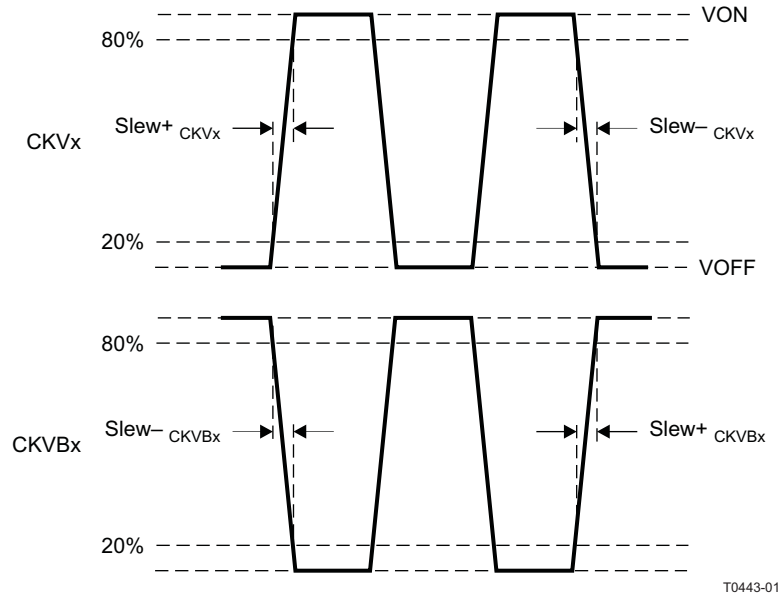
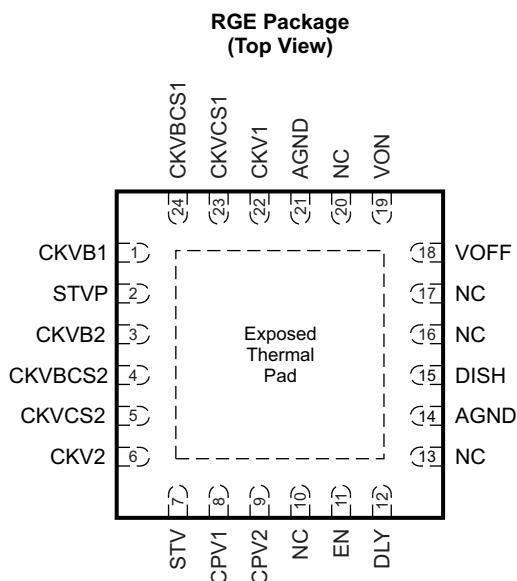


Figure 3. CKVx, CKVBx Output Rise and Fall Times (STV = 3.3 V)

DEVICE INFORMATION



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Exposed thermal pad and NC pins are recommended to be connected with ground on the PCB for better thermal dissipation.

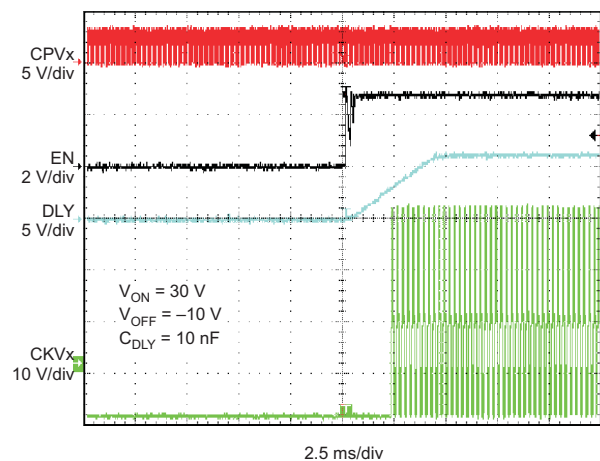
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
CKV1	22	O	Output vertical-scan clock 1 for ASG
CKV2	6	O	Output vertical-scan clock 2 for ASG
CKVB1	1	O	Inverted-output vertical-scan clock 1 for ASG
CKVB2	3	O	Inverted-output vertical-scan clock 2 for ASG
CKVBCS1	24	I	Charge-share input for CKVB1
CKVBCS2	4	I	Charge-share input for CKVB2
CKVCS1	23	I	Charge-share input for CKV1
CKVCS2	5	I	Charge-share input for CKV2
CPV1	8	I	Input vertical-scan clock 1
CPV2	9	I	Input vertical-scan clock 2
DISH	15	I	VOFF discharge control
DLY	12	O	Connecting a capacitor from this pin to GND allows the setting of the start-up delay.
EN	11	I	Enable pin of device. When this pin is pulled high, the device starts up after a delay time set by DLY has passed.
GND	14, 21	–	Ground
NC	10, 13, 16, 17, 20	–	Not connected
STV	7	I	Input vertical-scan start signal
STVP	2	O	Output vertical-scan start signal
VOFF	18	I	Negative low-supply voltage
VON	19	I	Positive high-supply voltage
Thermal pad		–	Not connected

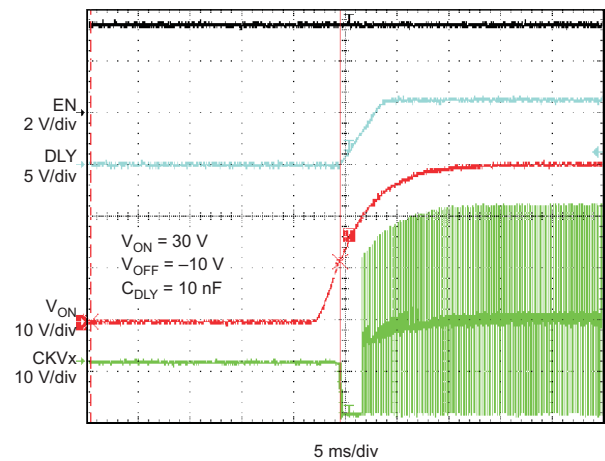
TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

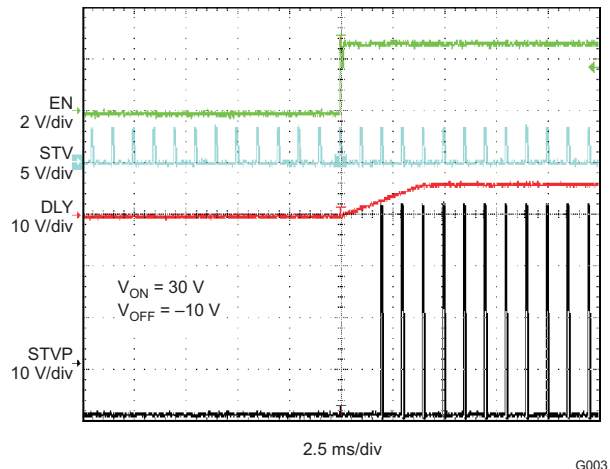
		FIGURE
SYSTEM PERFORMANCE		
Start-up sequence CKVx	EN = HIGH after UVLO, C _{DLY} = 10 nF, STV = LOW	Figure 4
	EN = HIGH before UVLO, C _{DLY} = 10 nF, STV = LOW	Figure 5
Start-up sequence STVP	EN = HIGH after UVLO, C _{DLY} = 10 nF, CPVx = LOW	Figure 6
	EN = HIGH before UVLO, C _{DLY} = 10 nF, CPVx = LOW	Figure 7
OUTPUT CKVx, CKVBx, and STVP		
Rise time / propagation delay of CKVx	STV = HIGH, load = 4.7 nF	Figure 8
	STV = LOW, load = 4.7 nF	Figure 9
Fall time / propagation delay of CKVx	STV = HIGH, load = 4.7 nF	Figure 10
	STV = LOW, load = 4.7 nF	Figure 11
Rise time / propagation delay of STVP	CPV1 = LOW, load = 4.7 nF	Figure 12
Fall time / propagation delay of STVP	CPV1 = LOW, load = 4.7 nF	Figure 13
STVP output	CPV1 = HIGH	Figure 14
	CPV1 = LOW	Figure 15
CKVx, CKVBx outputs	STV = HIGH	Figure 16
	STV = LOW	Figure 17



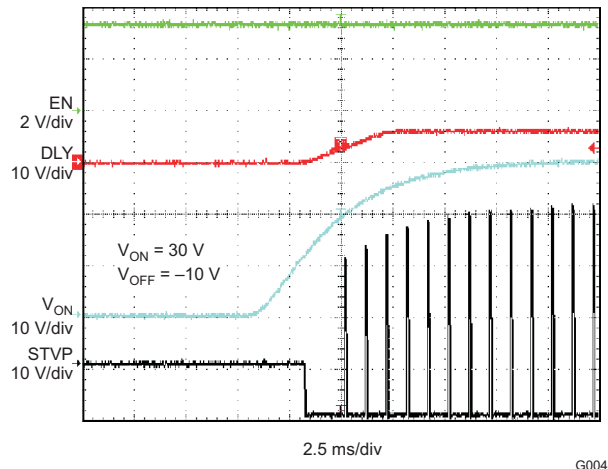
**Figure 4. Start-Up Sequence CKVx,
EN = HIGH After UVLO**



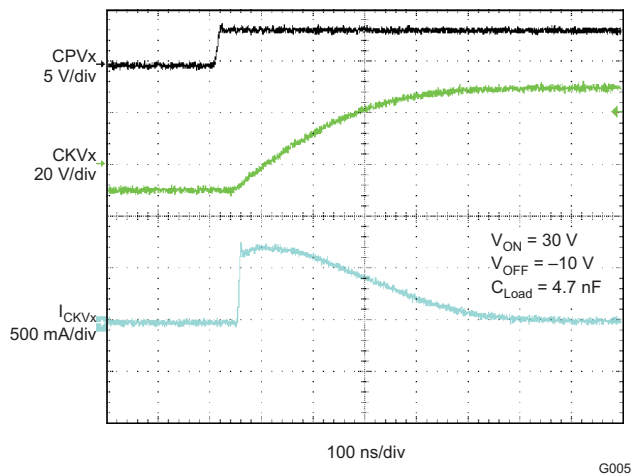
**Figure 5. Start-Up Sequence CKVx,
EN = HIGH Before UVLO**



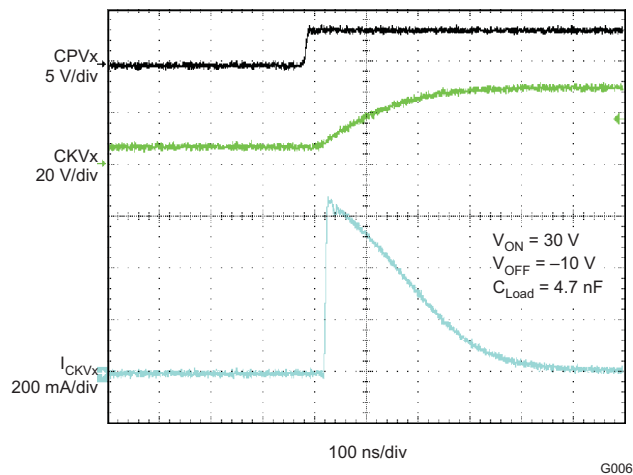
**Figure 6. Start-Up Sequence STVP,
EN = HIGH After UVLO**



**Figure 7. Start-Up Sequence STVP,
EN = HIGH After UVLO**



**Figure 8. Rise Time / Propagation Delay of CKVx,
STV = HIGH**



**Figure 9. Rise Time / Propagation Delay of CKVx,
STV = LOW**

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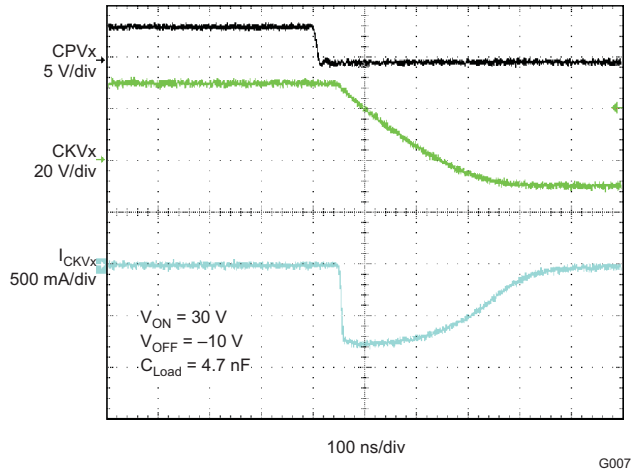


Figure 10. Fall Time / Propagation Delay of CKVx, STV = HIGH

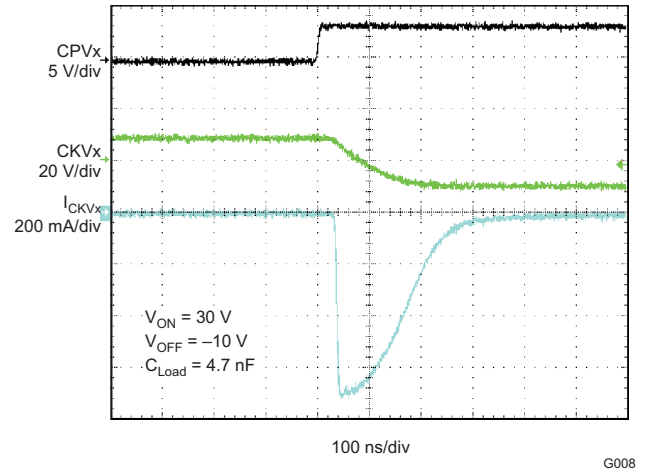


Figure 11. Fall Time / Propagation Delay of CKVx, STV = LOW

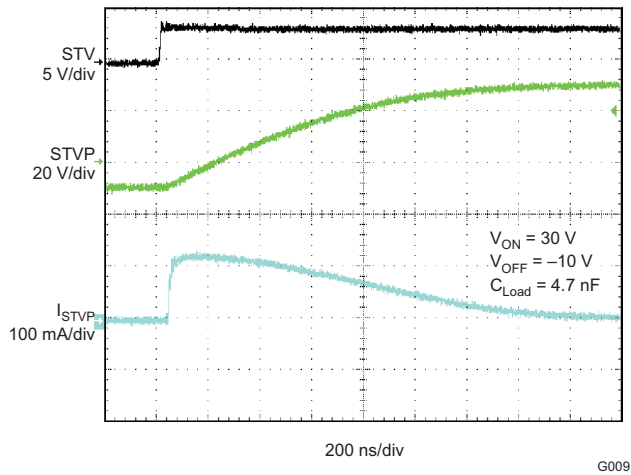


Figure 12. Rise Time / Propagation Delay of STVP, CPV1 = LOW

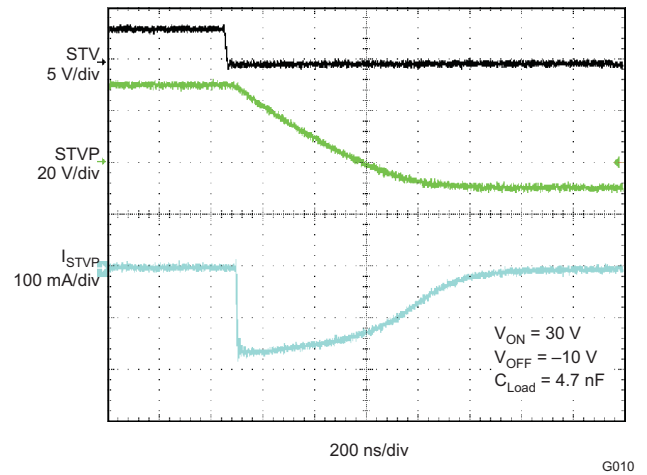


Figure 13. Fall Time / Propagation Delay of STVP, CPV1 = LOW

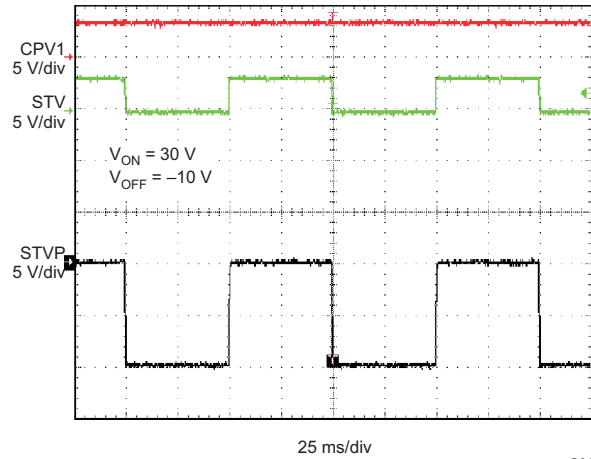


Figure 14. STVP Output, CPV1 = HIGH

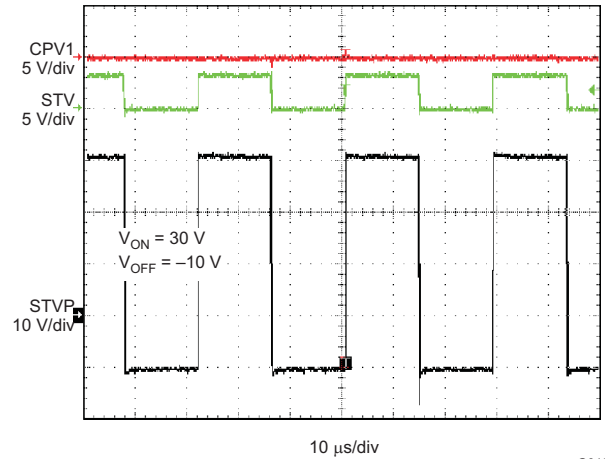


Figure 15. STVP Output, CPV1 = LOW

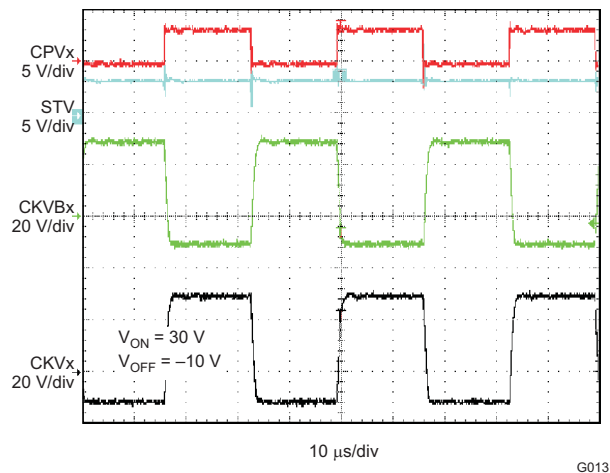


Figure 16. CKVx, CKVBx Outputs, STV = HIGH

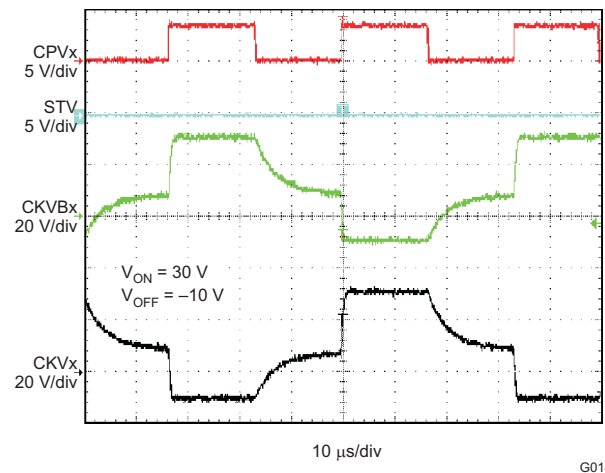
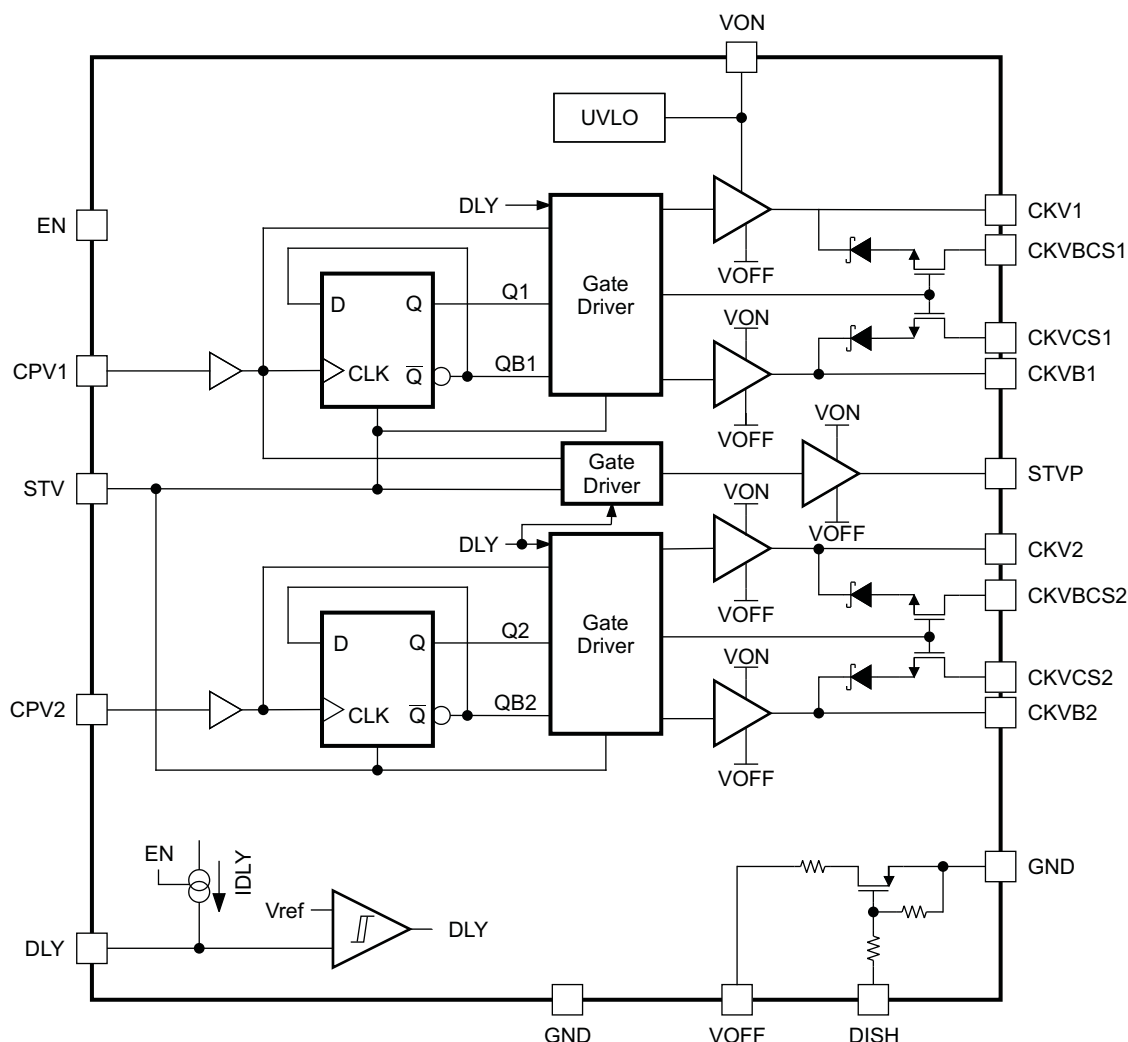


Figure 17. CKVx, CKVBx Outputs, STV = LOW

BLOCK DIAGRAM



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DETAILED DESCRIPTION

UNDERVOLTAGE LOCKOUT

The device has an undervoltage lockout feature to avoid improper operation of the device when input voltage VON is low. When VON is lower than 10 V, the device shuts down, and outputs CKVx, CKVBx, and STVP enter the high-impedance state.

INPUT SIGNALS

The timing controller in the system provides input signals to the TPS65193. STV is the synchronous signal for picture frames, and its frequency depends on the frame rate. CPVx are the synchronous signals for horizontal lines, and their frequency depends on the frame rate and vertical resolution.

OUTPUT SIGNALS

The STVP, CKVx, and CKVBx scan-driver outputs are generated with internal switches. [Table 1](#) and [Table 2](#) show the logic diagrams of the scan-driver outputs.

Table 1. STVP Logic Diagram

INPUT		OUTPUT
STV	CPV1	STVP
LOW	Don't care	VOFF
HIGH	LOW	VON
HIGH	HIGH	High impedance

Table 2. CKVx, CKVBx, and Output Charge-Share Logic

INPUT		OUTPUT		
STV	CPVx	CKVx	CKVBx	CHARGE SHARE
LOW	LOW	High impedance	High impedance	Enable
LOW	Rising edge	Toggle state	Toggle state	Disable
LOW	HIGH	Previous state	Previous state	Disable
HIGH	LOW	VOFF	VON	Disable
HIGH	HIGH	VON	VOFF	Disable

OUTPUT CHARGE SHARE

Power dissipation can be reduced by the output charge share. Figure 18 shows the current flows when the charge share is enabled. CKVCSx and CKVBCSx are charge-share inputs. When the charge share is enabled, the charge that is in the capacitor of the positive voltage line is transferred to the capacitor of the negative voltage line. Charge-sharing resistors RCSx and RBCSx reduce the peak current into the charge-share inputs, CKVCSx and CKVBCSx, during the output charge share. These resistors also control the slope of the output charge-share waveform. The smaller RCSx and RBCSx, the bigger the peak current into the charge-share inputs and the steeper the slope of output charge-share waveform. The power dissipation in charge-sharing resistors should be taken into consideration. With 0603 size resistors, the power rating of two in parallel is good for most applications.

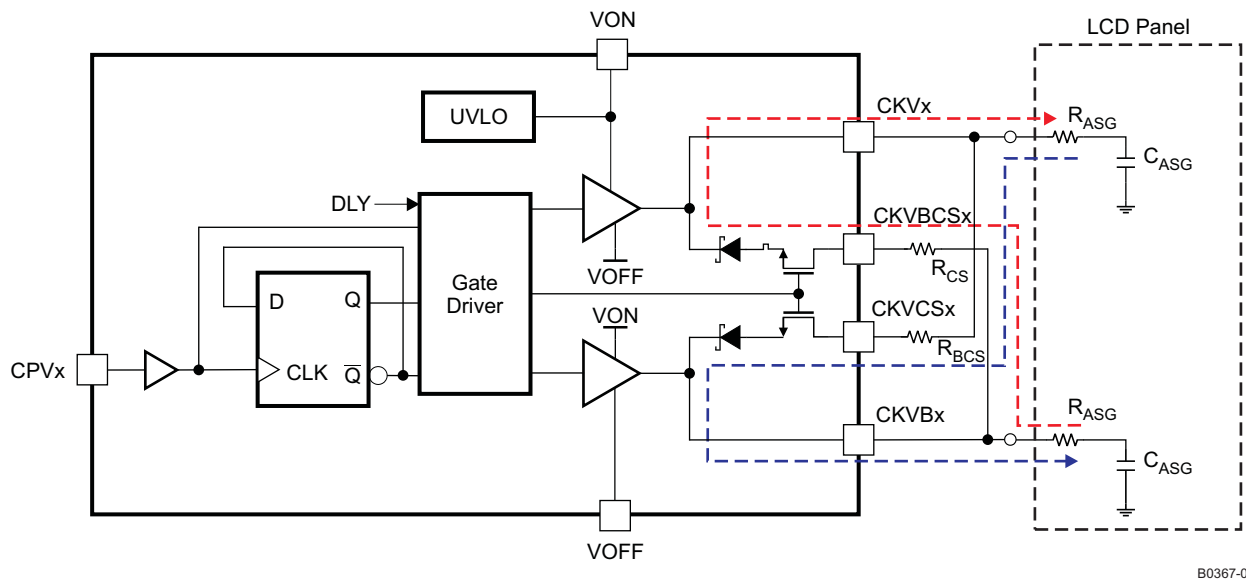


Figure 18. Single-Scan Driver Block Diagram

START-UP SEQUENCE (EN, DLY)

The TPS65193 has adjustable start-up sequencing that is set by EN and DLY. When VON is below the UVLO threshold, all outputs are at high impedance. When EN is pulled LOW after the UVLO threshold is reached, all

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outputs follow VOFF. Pulling EN high enables the device after a delay time set by the capacitor connected to DLY, and the delay time starts with EN = HIGH. If EN is pulled high before the UVLO threshold is reached, the delay starts when VON reaches the UVLO threshold. Pulling EN low disables the device and outputs CKVx, CKVBx, and STVP follow VOFF as long as VON is higher than the UVLO threshold. For the typical start-up sequence, see [Figure 19](#) and [Figure 20](#).

SETTING THE DELAY TIME (DLY)

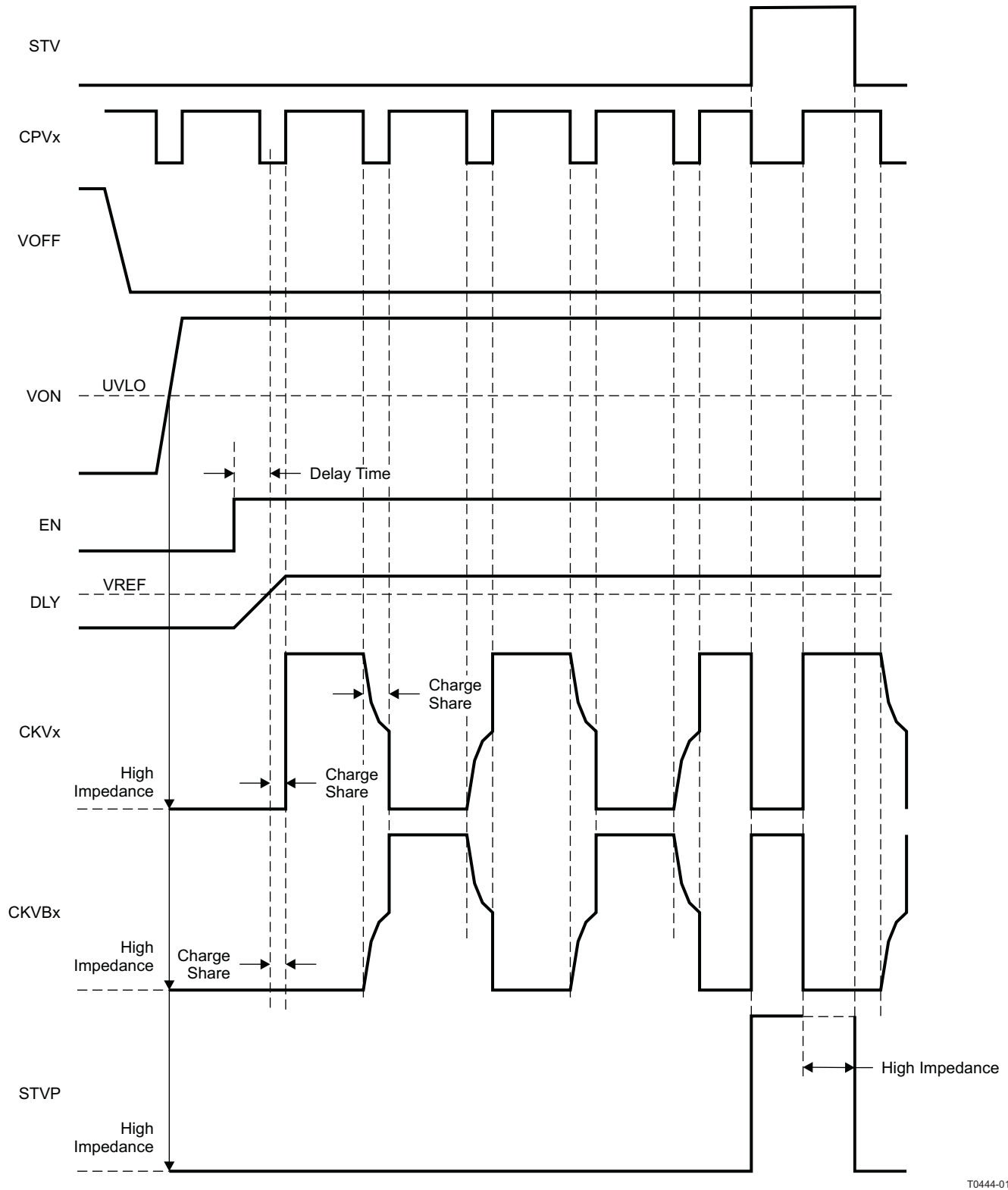
Connecting an external capacitor to the DLY pin sets the delay time. If no delay time is required, the DLY pin can be left floating. The external capacitor is charged with a constant-current source of typically 15 μ A. The delay time is terminated when the capacitor voltage reaches the internal reference voltage of 2.9 V, and the final DLY voltage on an external capacitor is maximum 8 V. The voltage rating of the external capacitor must be higher than 8 V.

The external delay capacitor is calculated using the following formula:

$$C_{DLY} = \frac{\text{Delay time}}{R_{DLY}} = \frac{\text{Delay time}}{200 \text{ k}\Omega} \quad (1)$$

Example for setting a delay time of 10 ms:

$$C_{DLY} = \frac{10 \text{ ms}}{200 \text{ k}\Omega} = 50 \text{ nF} \approx 47 \text{ nF} \quad (2)$$



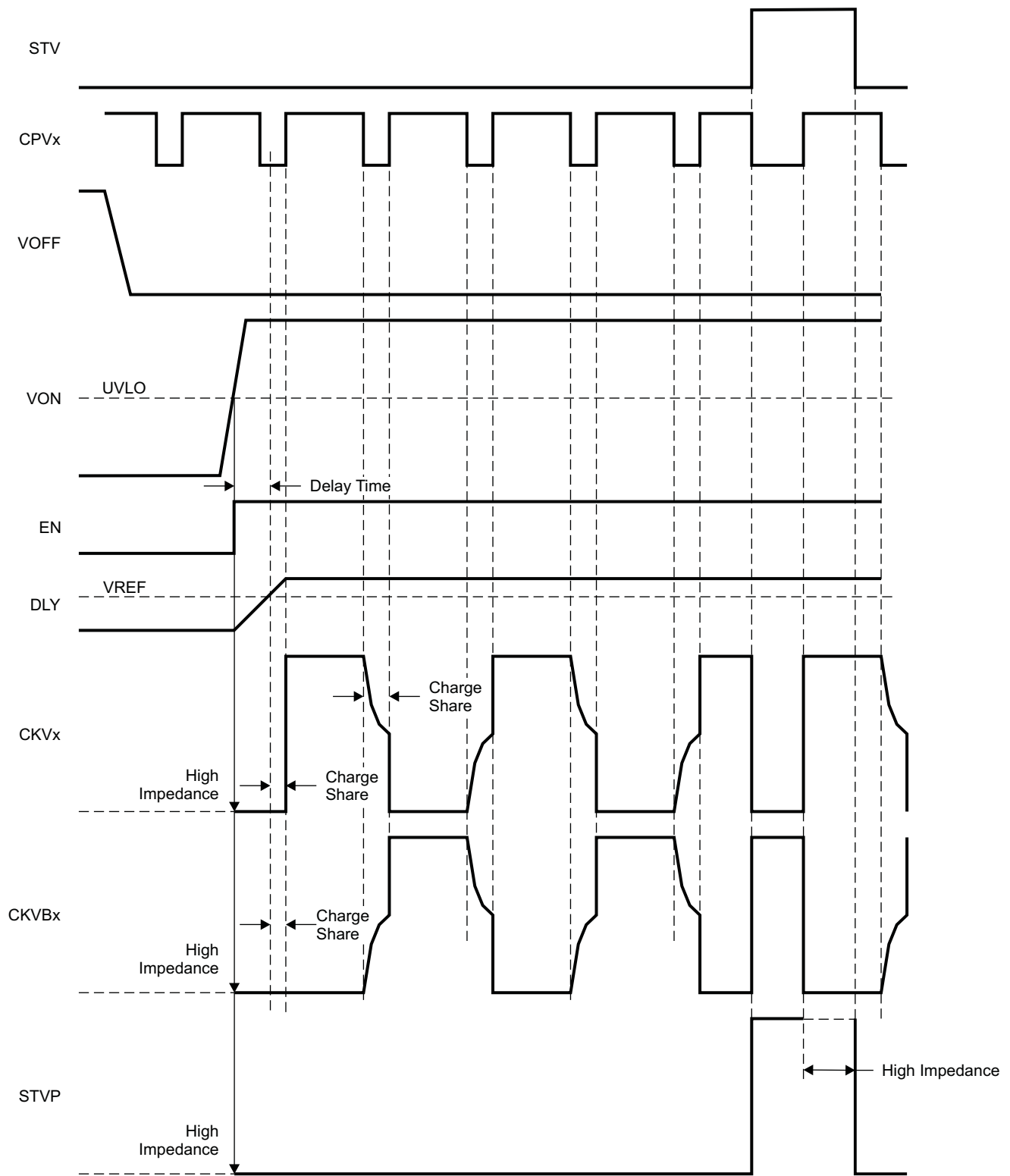
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Figure 19. Start-Up Sequence With EN = High After UVLO Threshold

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Figure 20. Start-Up Sequence With EN = High Before UVLO Threshold

TIMING DIAGRAM OF SCAN DRIVER

Figure 21 shows the typical timing diagram of the TPS65193.

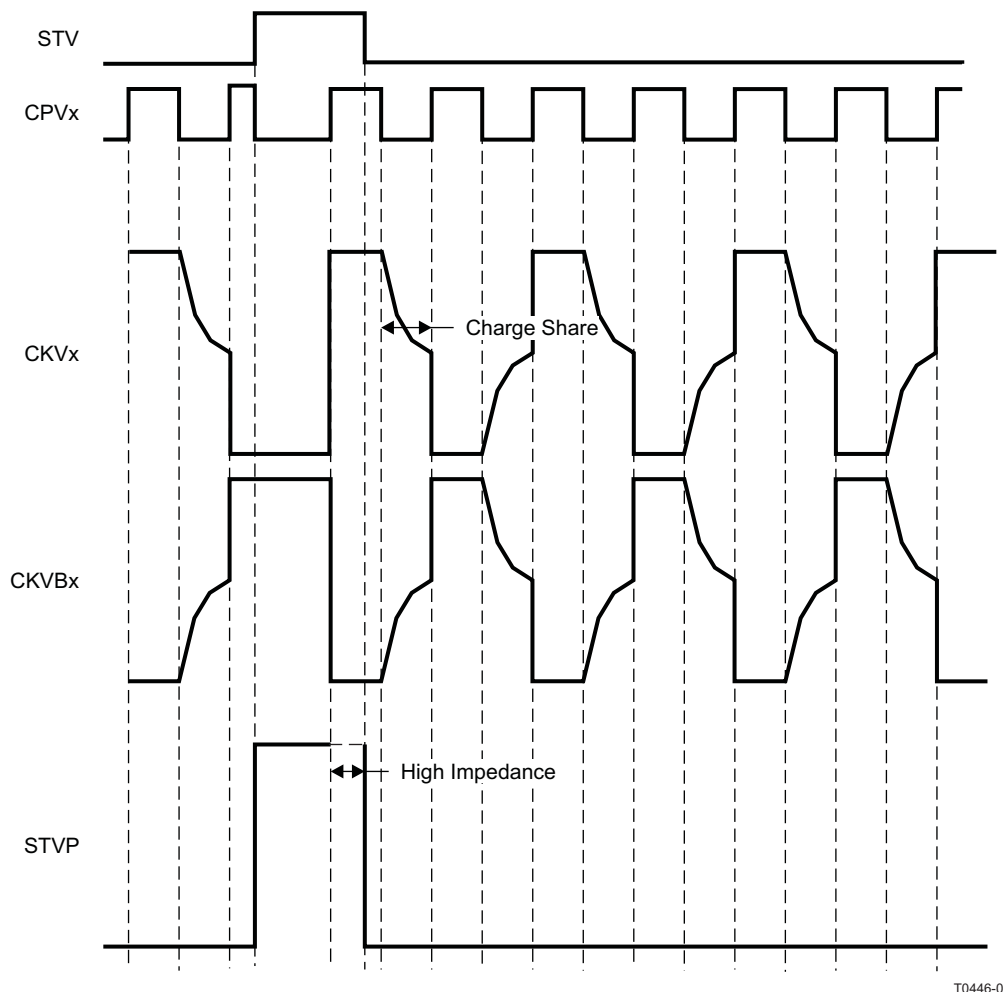


Figure 21. Scan Driver Timing Diagram

SUPPLY VOLTAGE, VON and VOFF

The TPS65193 drives the capacitive load. The high peak currents should be supplied from VON on the rising edges of the outputs and VOFF on the falling edges of the outputs, respectively. Bypass capacitors of 1 μ F must be placed as close as possible on both VON and VOFF supplies. Depending on the peak current that the TPS65193 must deliver, the bypass capacitor can be bigger than 1 μ F.

VOFF DISCHARGE

DISH controls the VOFF discharging time during the system power off. Figure 22 shows a typical application for VOFF discharge. DISH is connected to the system logic voltage through a capacitor. During power off, the system logic voltage falls, and the voltage on DISH falls below ground level. An internal switch turns on when DISH is below -0.6 V and VOFF is connected to ground through 1 k Ω , which helps VOFF discharge. A 1- μ F DISH capacitor is good for most applications. Figure 23 shows the typical power-off sequence of VOFF discharging. VOFF discharge can be disabled by connecting DISH to GND directly.

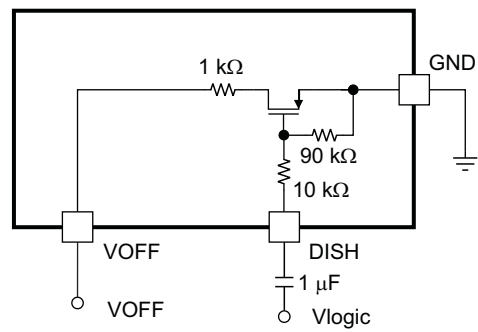


Figure 22. Typical Application for VOFF Discharge

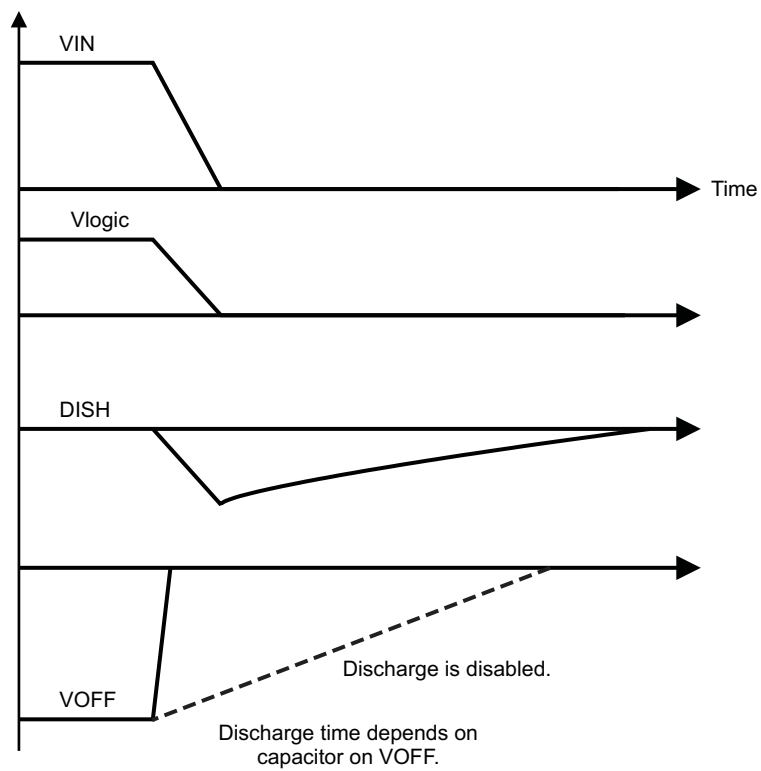
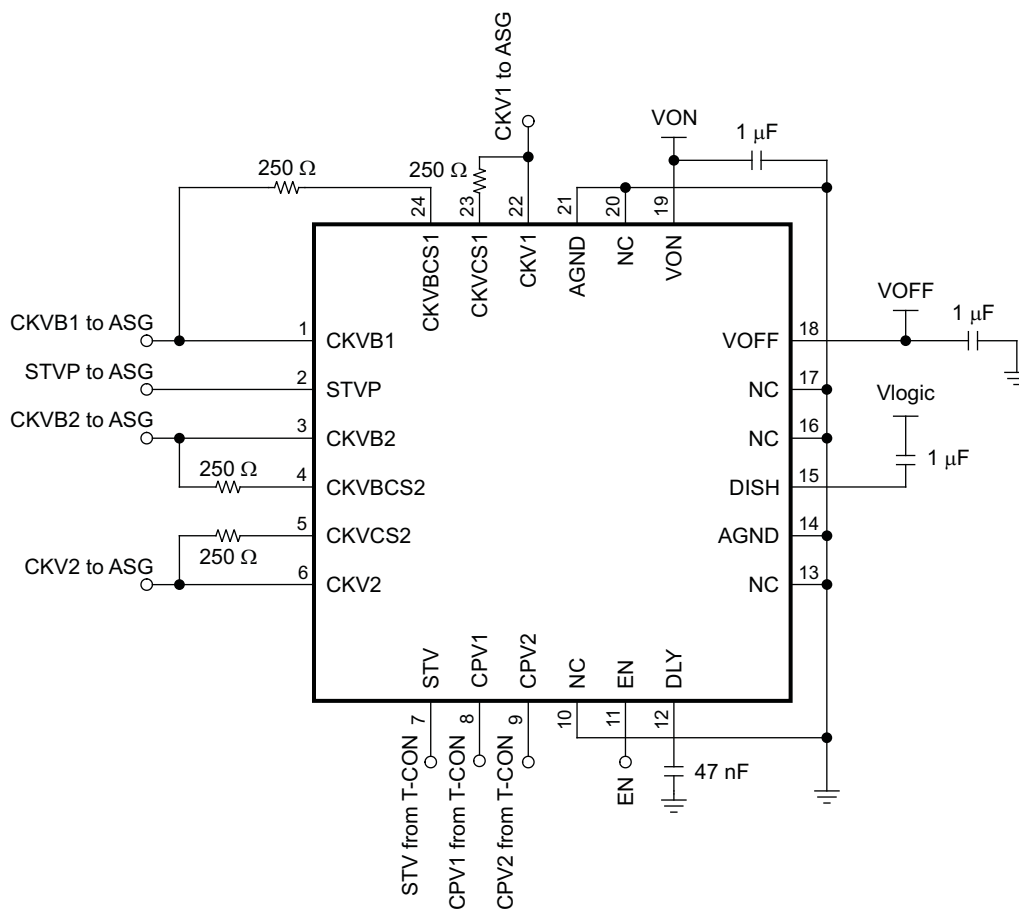


Figure 23. Power-Off Sequence of VOFF Discharge

TYPICAL APPLICATION



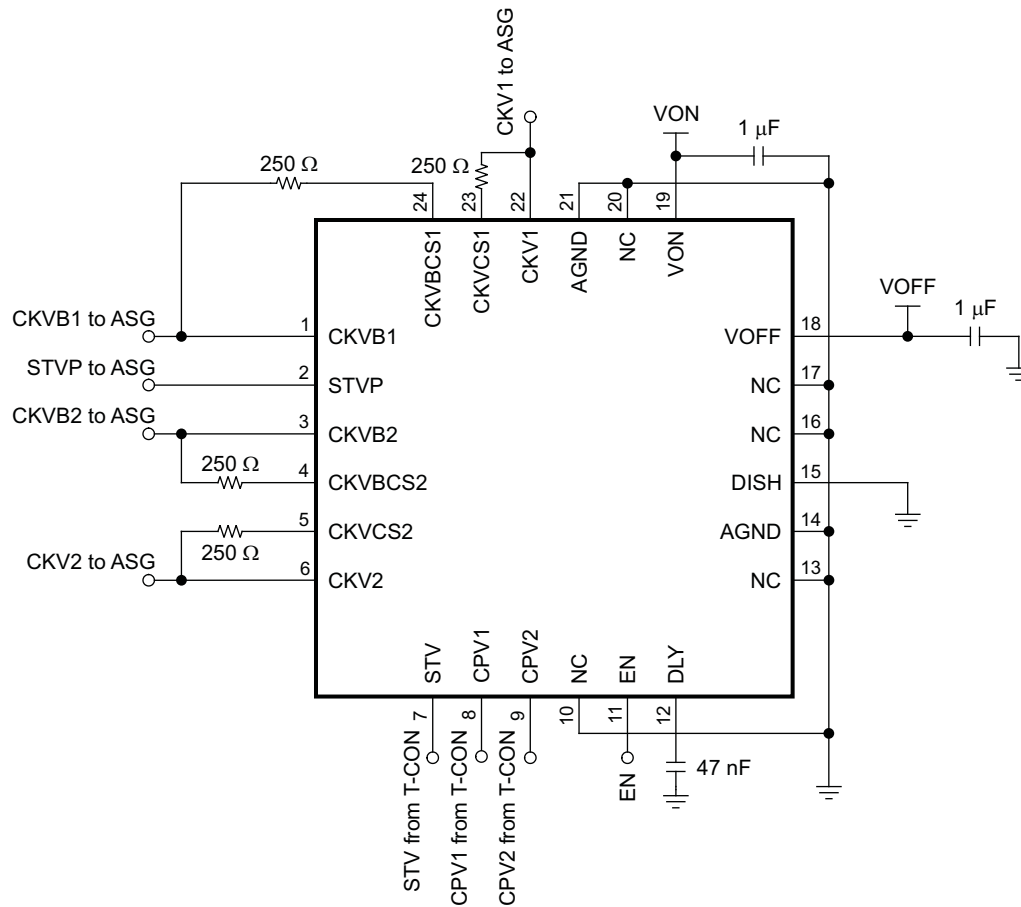
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Figure 24. Typical Application With VOFF Discharge Enabled

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Figure 25. Typical Application With VOFF Discharge Disabled

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65193RGER	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TPS 65193
TPS65193RGER.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TPS 65193

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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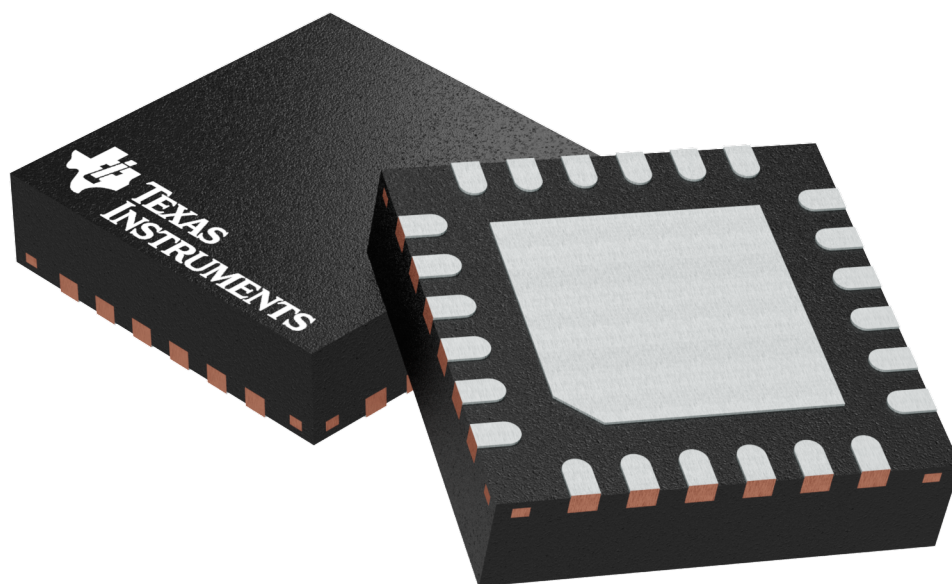
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGE 24

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

VQFN - 1 mm max height

Top View Dimensions:

- Overall Width: 4.1
- Overall Height: 4.1
- Pin 1 Index Area: Indicated by a shaded square in the top-left corner.

Side View Dimensions:

- Overall Height: 1.0 MAX
- Flatness: 0.05

Terminal Details:

- Terminal Pitch: 2.5
- Terminal Width: 0.5
- Terminal Spacing: 2.5
- Terminal Height: 0.3
- Terminal Width: 0.18
- Terminal Spacing: 0.05

Other Features:

- Exposed Thermal Pad: Indicated by a dashed line in the center of the footprint.
- Seating Plane: Indicated by a horizontal line in the side view.
- Pin 1 ID (Optional): Indicated by a small circle in the bottom-left corner.

Table:

0.1	0.05	C	A	B
0.05	0.05			

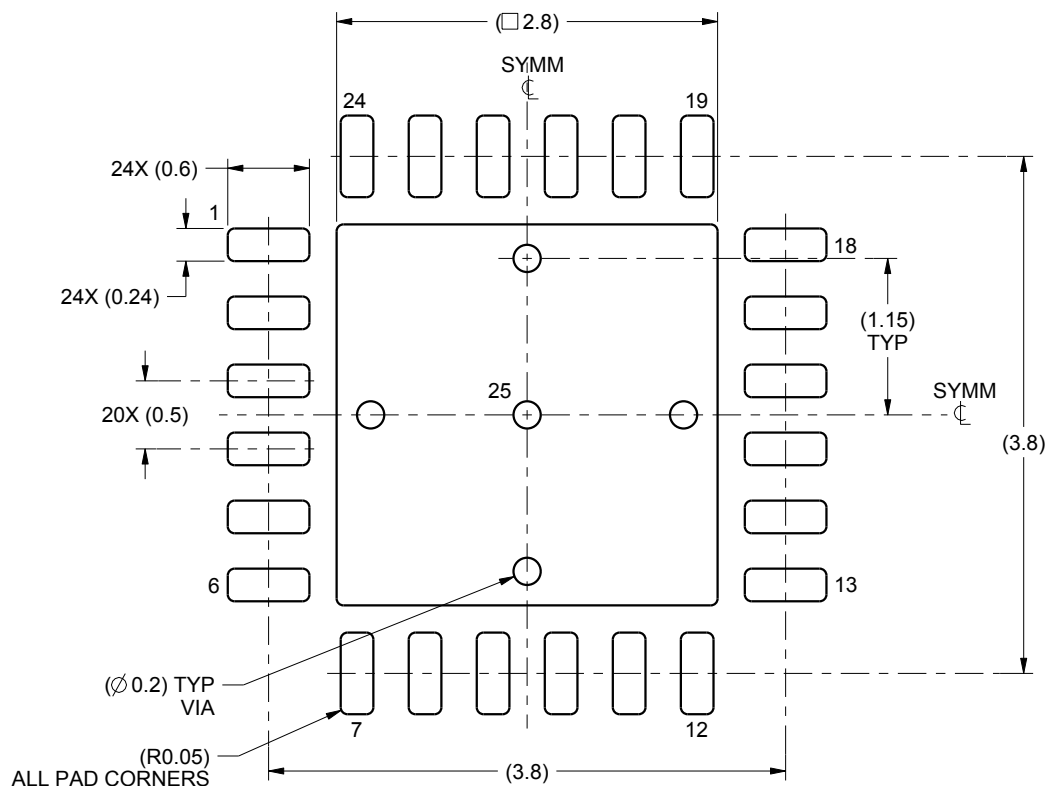
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.

EXAMPLE BOARD LAYOUT

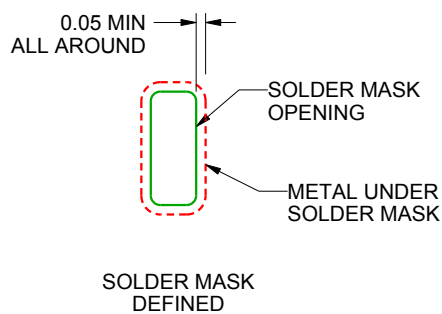
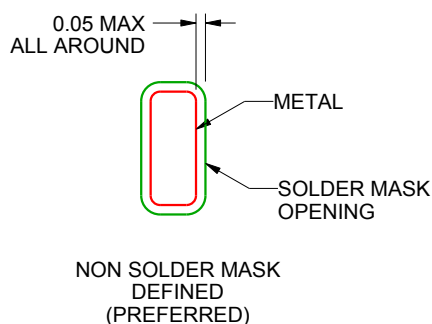
RGE0024F

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4222437/A 12/2015

NOTES: (continued)

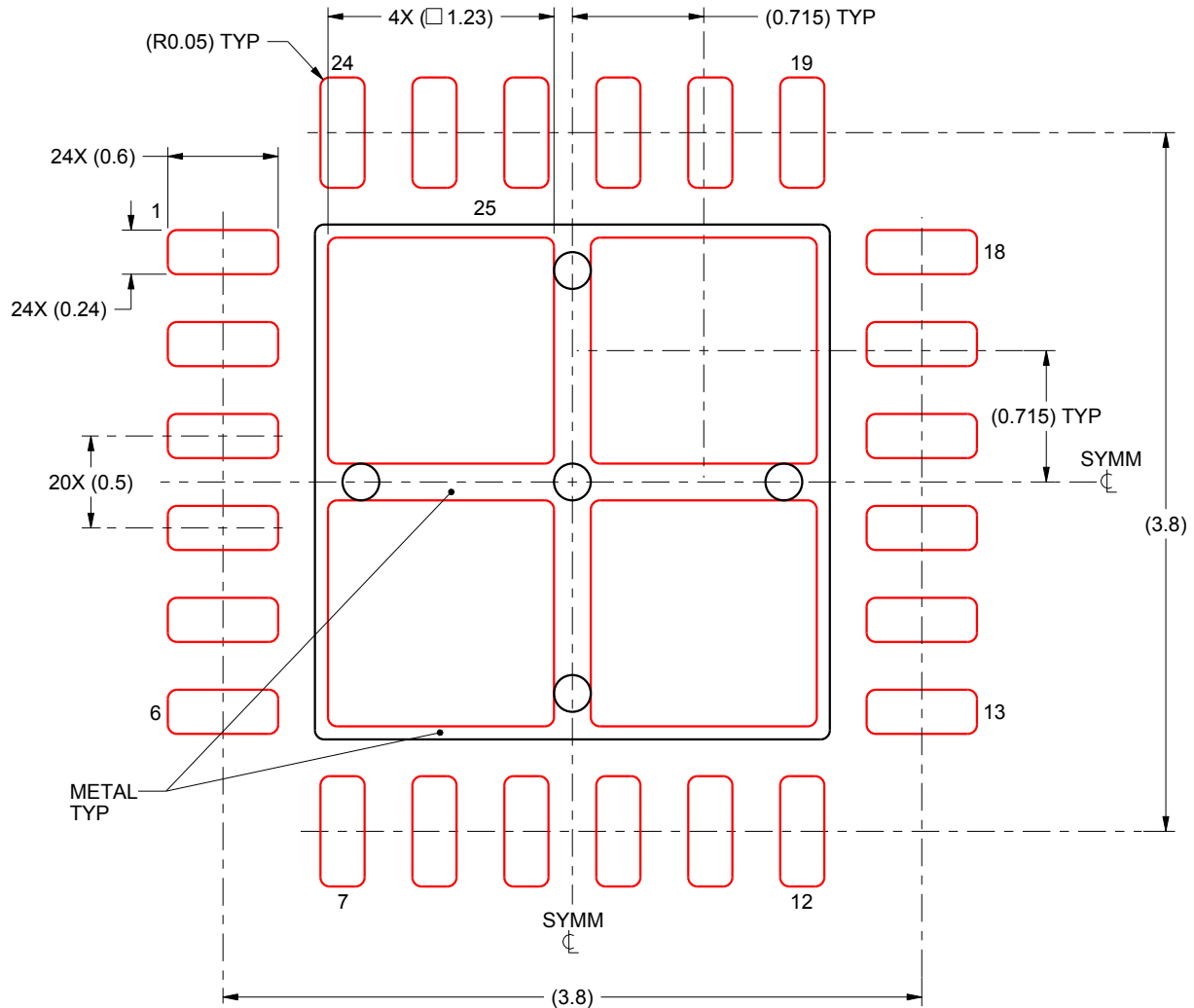
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

RGE0024F

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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