TPS65053-Q1 5-Channel Power Management IC With Two Step-Down Converters and Three Low-Input Voltage LDOs

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 3: –40°C to +85°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Up To 95% Efficiency
- Output Current for DC-DC Converters:
  - DCDC1 = 1 A; DCDC2 = 0.6 A
- DC-DC Converters Externally Adjustable
- V_{IN} Range for DC-DC Converters From 2.5 V to 6 V
- 2.25-MHz Fixed Frequency Operation
- Power Save Mode at Light-Load Current
- 180° Out-of-Phase Operation
- Output Voltage Accuracy in PWM Mode ±1%
- Total Typical 32-µA Quiescent Current for Both DC-DC Converters
- 100% Duty Cycle for Lowest Dropout
- One General-Purpose 400-mA LDO
- Two General-Purpose 200-mA LDOs
- V_{IN} Range for LDOs from 1.5 V to 6.5 V
- Output Voltage for LDO3:
  - VLDO3 = 1.3 V
- Available in a 4-mm × 4-mm 24-Pin VQFN Package

2 Applications

- Automotive Li-Ion Battery-Powered Devices
  - GPS, Emergency Cell Phone
  - Digital Cameras
  - Satellite Radio Modules
  - OMAP™ and Low-Power DSP

3 Description

The TPS65053-Q1 device is integrated power management IC (PMIC) for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. The TPS65053-Q1 device provides two highly efficient, 2.25-MHz step-down converters targeted at providing the core voltage and I/O voltage in a processor-based system. Both step-down converters enter a low power mode at light loads for maximum efficiency across the widest possible range of load currents. For low-noise applications, the devices can be forced into fixed-frequency PWM mode by pulling the MODE pin high. Both converters allow the use of small inductors and capacitors to achieve a small solution size.

The TPS65053-Q1 device provides an output current of up to 1 A on the DCDC1 converter and up to 0.6 A on the DCDC2 converter. The device also integrates one 400-mA LDO and two 200-mA LDO voltage regulators, which can be turned on and off using separate enable pins on each LDO. Each LDO operates with an input voltage range from 1.5 V to 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the main battery. LDO1 and LDO2 are externally adjustable, while LDO3 has a fixed output voltage of 1.3 V.

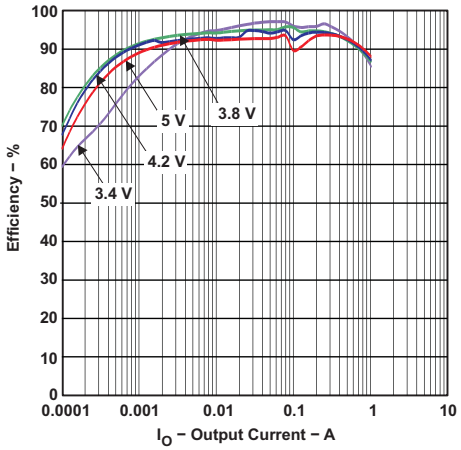
The TPS65053-Q1 device is available in a small 24-pin leadless package (4-mm × 4-mm VQFN) with a 0,5-mm pitch.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65053-Q1	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency of DCDC1



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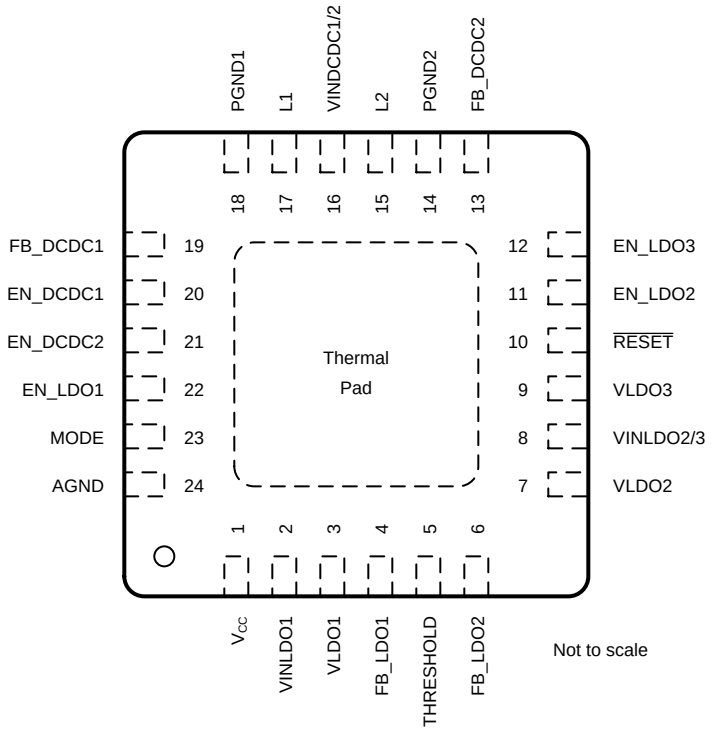
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2011) to Revision A	Page
• Added the *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted all references to TPS650531-Q1 and TPS650532-Q1 devices	1
• Changed values in the *Thermal Information* table to align with JEDEC standards	5

5 Pin Configuration and Function

RGE Package
24-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	24	I	Analog GND, connect to PGND and thermal pad
EN_DCDC1	20	I	Enable Input for converter 1, active high
EN_DCDC2	21	I	Enable Input for converter 2, active high
EN_LDO1	22	I	Enable input for LDO1. Logic high enables the LDO, logic low disables the LDO.
EN_LDO2	11	I	Enable input for LDO2. Logic high enables the LDO, logic low disables the LDO.
EN_LDO3	12	I	Enable input for LDO3. Logic high enables the LDO, logic low disables the LDO.
FB_DCDC1	19	I	Input to adjust output voltage of converter 1 between 0.6 V and V_I. Connect external resistor divider between VOUT1, this pin and GND.
FB_DCDC2	13	I	Input to adjust output voltage of converter 2 between 0.6 V and VIN. Connect external resistor divider between VOUT2, this pin and GND.
FB_LDO1	4	I	Feedback input for the external voltage divider.
FB_LDO2	6	I	Feedback input for the external voltage divider.
L1	17	O	Switch pin of converter 1. Connected to Inductor
L2	15	O	Switch Pin of converter 2. Connected to Inductor.
MODE	23	I	Select between Power Save Mode and forced PWM Mode for DCDC1 and DCDC2. In Power Save Mode, PFM is used at light loads, PWM for higher loads. If PIN is set to high level, forced PWM Mode is selected. If Pin has low level, then the device operates in Power Save Mode.
PGND1	18	I	GND for converter 1
PGND2	14	I	GND for converter 2
$\overline{\text{RESET}}$	10	O	Open drain active low reset output, 100-ms reset delay time.
THRESHOLD	5	I	Reset input
V_{CC}	1	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. This pin must be connected to the same voltage supply as VINDCDC1/2.
VINDCDC1/2	16	I	Input voltage for VDCDC1 and VDCDC2 step-down converter. This must be connected to the same voltage supply as V_{CC}.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VINLDO1	2	I	Input voltage for LDO1
VINLDO2/3	8	I	Input voltage for LDO2 and LDO3
VLDO1	3	O	Output voltage of LDO1
VLDO2	7	O	Output voltage of LDO2
VLDO3	9	O	Output voltage of LDO3
Thermal Pad		—	Connect to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage	All pins except AGND, PGND, and EN_LDO1 pins with respect to AGND	–0.3	7	V
		EN_LDO1 pin with respect to AGND	–0.3	V_{CC} + 0.5	
V_O	Output voltage for LDO1, LDO2 and LDO3		–0.3	4	V
I_I	Current	VINDCDC1/2, L1, PGND1, L2, PGND2		1800	mA
		All other pins		1000	
T_A	Operating free-air temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 6, 7, 12, 13, 18, 19, and 24)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{INDCDC1/2}$	Input voltage for step-down converters	2.5		6	V
V_{INLDO1}, $V_{INLDO2/3}$	Input voltage range for LDOs	1.5		6.5	V
V_{DCDC1}	Output voltage range for externally adjustable VDCDC1 step-down converter	0.6		$V_{INDCDC1}$	V
V_{DCDC2}	Output voltage range for externally adjustable VDCDC2 step-down converter	0.6		$V_{INDCDC2}$	V
V_{LDO1-2}	Output voltage range for externally adjustable LDO1 and LDO2	1		3.6	V
V_{LDO3}	Output voltage for LDO3		1.3		V
$I_{OUTDCDC1}$	Output current at L1			1000	mA
$I_{OUTDCDC2}$	Output current at L2			600	mA
I_{LDO1}	Output current at VLDO1			400	mA
$I_{LDO2,3}$	Output current at VLDO2 and VLDO3			200	mA
$C_{INDCDC1/2}$	Input capacitor at $V_{INDCDC1/2}$(1)	22			µF
C_{VCC}	Input capacitor at V_{CC} (1)	1			µF
C_{in1-2}	Input capacitor at VINLDO1, VINLDO2/3 (1)	2.2			µF

(1) See the *Application and Implementation* section of this data sheet for more details.

Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
$C_{OUTDCDC1}$	Output capacitor at V_{DCDC1} (1)	10	22		µF
$C_{OUTDCDC2}$	Output capacitor at V_{DCDC2} (1)	10	22		µF
C_{OUT1}	Output capacitor at VLDO1 (1)	4.7			µF
C_{OUT2-3}	Output capacitor at VLDO2-3 (1)	2.2			µF
L1	Inductor at L1 (1)	1.5	2.2		µH
L2	Inductor at L2 (1)	1.5	2.2		µH
R_{CC}	Resistor from battery voltage to V_{CC} used for filtering (2)		1	10	Ω
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(2) Up to 2 mA can flow into V_{CC} when both converters are running in PWM, this resistor causes the UVLO threshold to be shifted accordingly.

6.4 Thermal Information

THERMAL METRIC (1)		TPS65053-Q1 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_{OUT} = 22 µF, T_A = –40°C to +85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{CC}	Input voltage range		2.5		6	V
I_Q	Operating quiescent current Total current into V_{CC}, VINDCDC1/2, VINLDO1, VINLDO2/3	One converter, I_{OUT} = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = VIN OR EN_DCDC2 = VIN; EN_LDO1= EN_LDO2 = EN_LDO3 = GND			30	µA
		One converter, I_{OUT} = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = VIN OR EN_DCDC2 = VIN; EN_LDO1= EN_LDO2 = EN_LDO3 = GND, T_A = 25°C		20		
		Two converters, I_{OUT} = 0 mA, PFM mode enabled (Mode = 0) device not switching, EN_DCDC1 = VIN AND EN_DCDC2 = VIN; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND			40	
		Two converters, I_{OUT} = 0 mA, PFM mode enabled (Mode = 0) device not switching, EN_DCDC1 = VIN AND EN_DCDC2 = VIN; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND, T_A = 25°C		32		
		One converter, I_{OUT} = 0 mA, PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = VIN OR EN_DCDC2 = VIN; EN_LDO1 = EN_LDO2 = EN_LDO3 = VIN			210	
		One converter, I_{OUT} = 0 mA, PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = VIN OR EN_DCDC2 = VIN; EN_LDO1 = EN_LDO2 = EN_LDO3 = VIN, T_A = 25°C		145		
I_Q	Operating quiescent current into V_{CC}	One converter, I_{OUT} = 0 mA, Switching with no load (Mode = VIN), PWM operation, EN_DCDC1 = VIN OR EN_DCDC2 = VIN; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND, T_A = 25°C		0.85		mA
		Two converters, I_{OUT} = 0 mA, Switching with no load (Mode = VIN), PWM operation, EN_DCDC1 = VIN AND EN_DCDC2 = VIN; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND, T_A = 25°C		1.25		mA

Electrical Characteristics (continued)

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_{OUT} = 22 µF, T_A = –40°C to +85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SD)}$	Shutdown current	EN_DCDC1 = EN_DCDC2 = GND, EN_LDO1 = EN_LDO2 = EN_LDO3 = GND			12	µA
		EN_DCDC1 = EN_DCDC2 = GND, EN_LDO1 = EN_LDO2 = EN_LDO3 = GND, T_A = 25°C		9		
UVLO	Undervoltage lockout threshold for DC-DC converters and LDOs	Voltage at V_{CC}			2	V
		Voltage at V_{CC}, T_A = 25°C		1.8		
EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, MODE						
V_{IH}	High-level input voltage	MODE, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3	1.2		V_{CC}	V
V_{IL}	Low-level input voltage	MODE, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3	0		0.4	V
I_{IN}	Input bias current	MODE, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, MODE = GND or VIN, T_A = 25°C		0.01	1	µA
POWER SWITCH						
$r_{DS(on)}$	P-channel MOSFET on resistance, DCDC1, DCDC2	VINDCDC1/2 = 3.6 V			630	mΩ
		VINDCDC1/2 = 3.6 V, T_A = 25°C		280		
		VINDCDC1/2 = 2.5 V, T_A = 25°C		400		
I_{LD_PMOS}	P-channel leakage current	$V_{(DS)}$ = 6 V			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance, DCDC1, DCDC2	VINDCDC1/2 = 3.6 V			450	mΩ
		VINDCDC1/2 = 3.6 V, T_A = 25°C		220		
		VINDCDC1/2 = 2.5 V, T_A = 25°C		320		
I_{LK_NMOS}	N-channel leakage current	$V_{(DS)}$ = 6 V			10	µA
		$V_{(DS)}$ = 6 V, T_A = 25°C		7		
$I_{(LIMF)}$	Forward current limit PMOS (high side) and NMOS (low side)	DCDC1, 2.5 V ≤ V_{IN} ≤ 6 V	1.1		1.8	A
		DCDC1, 2.5 V ≤ V_{IN} ≤ 6 V, T_A = 25°C		1.4		
		DCDC2, 2.5 V ≤ V_{IN} ≤ 6 V	0.85		1.15	
		DCDC2, 2.5 V ≤ V_{IN} ≤ 6 V, T_A = 25°C		1		
$T_{SD,DCDC}$	Thermal shutdown	Increasing junction temperature, T_A = 25°C		150		°C
$T_{SDhys,DCDC}$	Thermal shutdown hysteresis	Decreasing junction temperature below $T_{SD,DCDC}$ for resuming normal operation, T_A = 25°C		20		°C
OSCILLATOR						
f_{SW}	Oscillator frequency		2.025		2.475	MHz
		T_A = 25°C		2.25		
OUTPUT						
V_{OUT}	Output voltage range		0.6		V_{IN}	V
V_{ref}	Reference voltage	T_A = 25°C		600		mV
V_{OUT}	DC output voltage accuracy	V_{IN} = 2.5 V to 6 V, Mode = GND, PFM operation, 0 mA < I_{OUT} < I_{OUTmax}	-2%	0	2%	
		V_{IN} = 2.5 V to 6 V, Mode = V_{IN}, PWM operation, 0 mA < I_{OUT} < I_{OUTmax}	–1%	0	1%	
ΔV_{OUT}	Power save mode ripple voltage(1)	I_{OUT} = 1 mA, Mode = GND, V_O = 1.3 V, Bandwidth = 20 MHz, T_A = 25°C		25		mV_{PP}
t_{Start}	Start-up time	Time from active EN to start switching, T_A = 25°C		170		µs
t_{Ramp}	V_{OUT} ramp up time	Time to ramp from 5% to 95% of V_{OUT}, T_A = 25°C		750		µs
	$\overline{RESET}$ delay time	Input voltage at threshold pin rising	80		120	ms
		Input voltage at threshold pin rising, T_A = 25°C		100		
V_{OL}	$\overline{RESET}$ output low voltage	I_{OL} = 1 mA, V_{th} < 1 V			0.2	V
	$\overline{RESET}$ sink current	T_A = 25°C		1		mA
	$\overline{RESET}$ output leakage current	V_{th} > 1 V, T_A = 25°C		10		nA
V_{th}	Threshold voltage	Falling voltage	0.98		1.02	V
		Falling voltage, T_A = 25°C		1		

(1) In Power Save Mode, operation is typically entered at I_{PSM} = V_{IN} / 32 Ω.

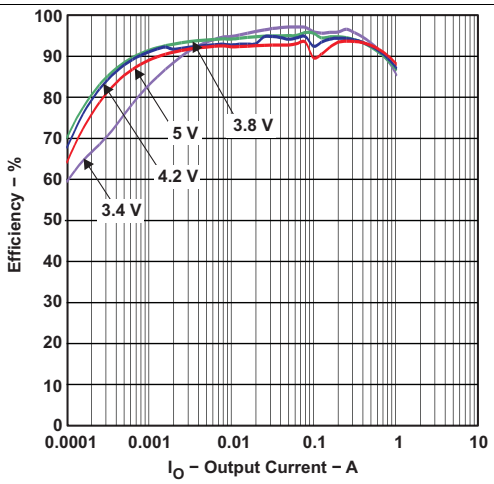
Electrical Characteristics (continued)

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_{OUT} = 22 µF, T_A = –40°C to +85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VLDO1, VLDO2, VLDO3 LOW DROPOUT REGULATORS						
V_{INLDO}	Input voltage range for LDO1, LDO2, LDO3		1.5		6.5	V
V_{LDO1}	LDO1 output voltage range		1		3.6	V
V_{LDO2}	LDO2 output voltage range		1		3.6	V
V_{LDO3}	LDO3 output voltage	T_A = 25°C		1.3		V
$V_{(FB)}$	Feedback voltage for FB_LDO1, FB_LDO2	T_A = 25°C		1		V
I_O	Maximum output current for LDO1		400			mA
	Maximum output current for LDO2, LDO3		200			mA
$I_{(SC)}$	LDO1 short-circuit current limit	V_{LDO1} = GND			850	mA
	LDO2 and LDO3 short-circuit current limit	V_{LDO2} = GND, V_{LDO3} = GND			420	mA
	Dropout voltage at LDO1	I_O = 400 mA, V_{INLDO1} = 1.8 V			280	mV
	Dropout voltage at LDO2, LDO3	I_O = 200 mA, VINLDO2/3 = 1.8 V			280	mV
	Output voltage accuracy for LDO1, LDO2, LDO3(2)	I_O = 10 mA	–2%		1%	
	Line regulation for LDO1, LDO2, LDO3	$V_{INLDO1,2}$ = $V_{LDO1,2}$ + 0.5 V (min. 2.5 V) to 6.5 V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2, LDO3	I_O = 0 mA to 400 mA for LDO1, I_O = 0 mA to 200 mA for LDO2, LDO3	–1%		1%	
	Regulation time for LDO1, LDO2, LDO3	Load change from 10% to 90%, T_A = 25°C		25		µs
$R_{(DIS)}$	Internal discharge resistor at VLDO1, VLDO2, VLDO3	Active when LDO is disabled, T_A = 25°C		350		Ω
$T_{SD,LDO}$	Thermal shutdown	Increasing junction temperature		140		°C
$T_{SDhys,LDO}$	Thermal shutdown hysteresis	Decreasing junction temperature below $T_{SD,LDO}$ for resuming normal operation		20		°C

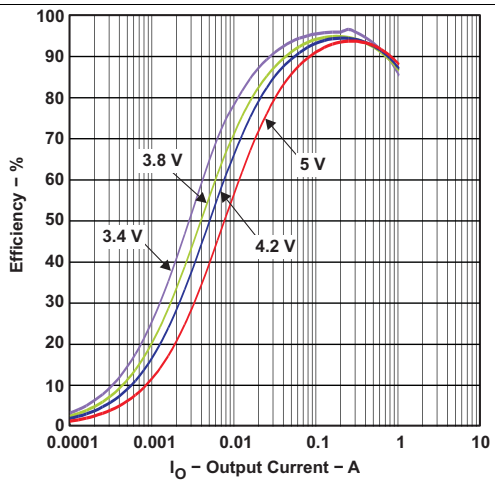
(2) Output voltage specification does not include tolerance of external voltage programming resistors.

6.6 Typical Characteristics



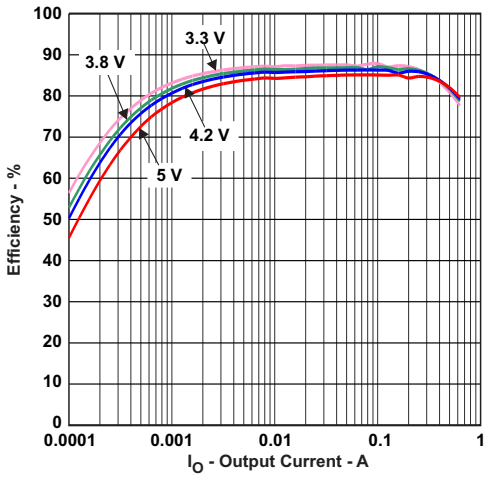
V_{DCDC1} = 2.85 V $V_{INDCDC1/2}$ = 3.4, 3.8, 4.2, and 5 V

Figure 1. Efficiency (η) of DCDC1 in PWM/PFM Mode



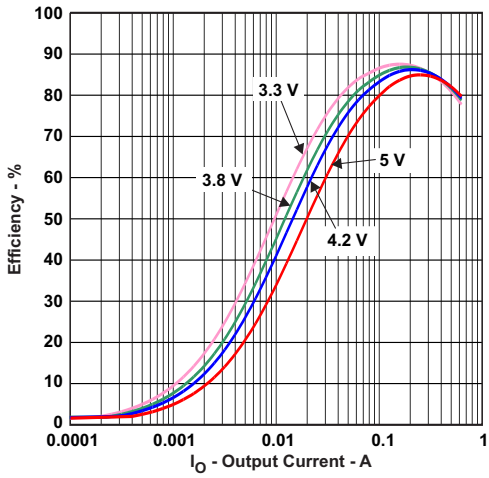
V_{DCDC1} = 2.85 V $V_{INDCDC1/2}$ = 3.4, 3.8, 4.2, and 5 V

Figure 2. Efficiency (η) of DCDC1 in PWM Mode



V_{DCDC2} = 1.8 V $V_{INDCDC1/2}$ = 3.4, 3.8, 4.2, and 5

Figure 3. Efficiency (η) of DCDC2 in PWM/PFM Mode



V_{DCDC2} = 1.8 V $V_{INDCDC1/2}$ = 3.4, 3.8, 4.2, and 5 V

Figure 4. Efficiency (η) of DCDC2 in PWM Mode

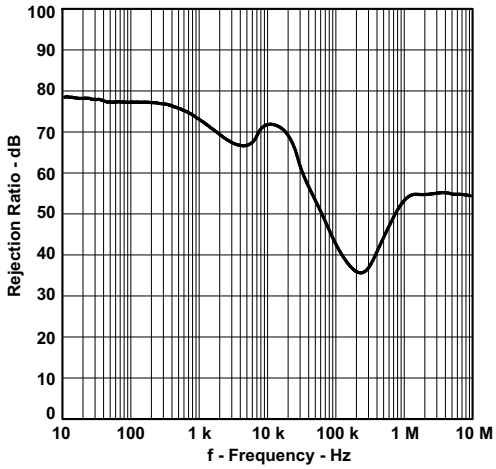


Figure 5. LDO1 Power-Supply Rejection Ratio

7 Detailed Description

7.1 Overview

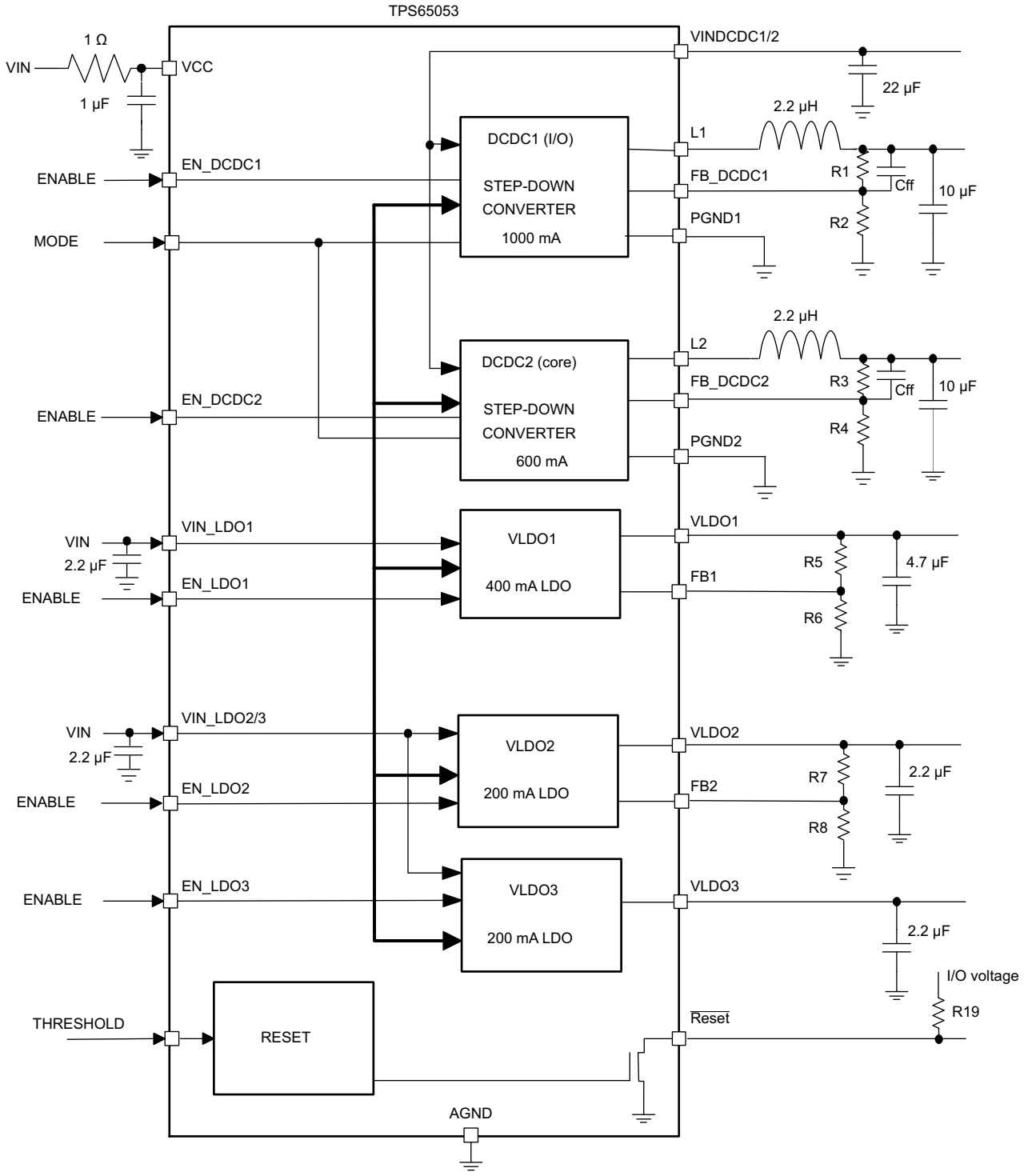
The TPS65053-Q1 device includes two synchronous step-down converters. The converters operate with 2.25-MHz fixed frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents the converters automatically enter Power Save Mode and operate with PFM (pulse frequency modulation).

During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator will also turn off the switch in case the current limit of the P-channel switch is exceeded. After the adaptive dead time prevents shoot-through current, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The two DC-DC converters operate synchronized to each other, with converter 1 as the master. A 180° phase shift between Converter 1 and Converter 2 decreases the input RMS current. Therefore smaller input capacitors can be used.

The converters output voltage is set by an external resistor divider connected to FB_DCDC1 or FB_DCDC2, respectively. See the *Application and Implementation* section for more details.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Mode Selection

The MODE pin allows mode selection between forced PWM Mode and Power Save Mode for both converters. Connecting this pin to GND enables the automatic PWM and Power Save Mode operation. The converters operate in fixed-frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load current range.

Pulling the MODE pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the Power Save Mode during light loads. For additional flexibility, switch from Power Save Mode to forced PWM mode during operation ehich allows efficient power management by adjusting the operation of the converter to the specific system requirements.

7.3.2 Enable

The device has a separate enable pin for each of the DC-DC converters and for each of the LDO to start up independently. If EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3 are set to high, the corresponding converter starts up with soft start as previously described.

Pulling the enable pin low forces the device into shutdown, with a shutdown quiescent current as defined in the *Electrical Characteristics* table. In this mode, the P and N-Channel MOSFETs are turned-off, the and the entire internal control circuitry is switched-off. If disabled, the outputs of the LDOs are pulled low by internal 350-Ω resistors, actively discharging the output capacitor. For proper operation the enable pins must be terminated and must not be left unconnected.

7.3.3 Reset

The TPS65053-Q1 device contains circuitry that can generate a reset pulse for a processor with a 100-ms delay time. The input voltage at a comparator is sensed at an input called THRESHOLD. When the voltage exceeds the 1-V threshold, the output goes high after a 100-ms delay time. This circuitry is functional as soon as the supply voltage at V_{CC} exceeds the undervoltage lockout threshold. The RESET circuitry is active even if all DC-DC converters and LDOs are disabled.

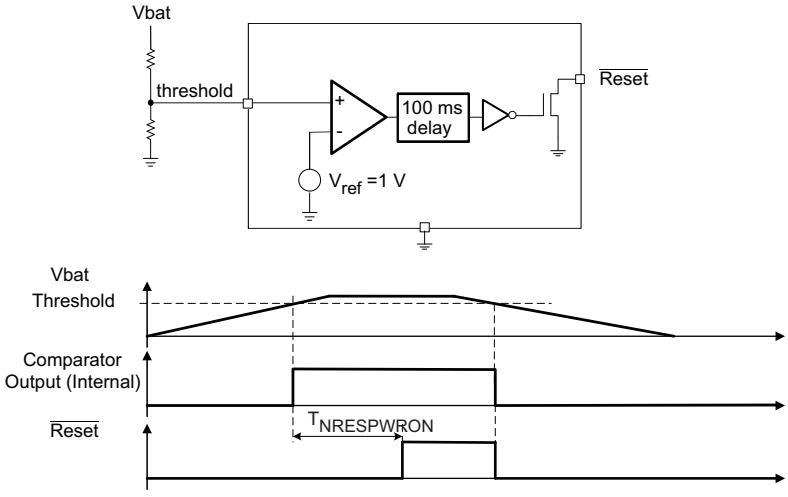


Figure 6. $\overline{\text{RESET}}$ Pulse Circuit

7.3.4 Short-Circuit Protection

All outputs are short circuit protected with a maximum output current as defined in the *Electrical Characteristics* table.

Feature Description (continued)

7.3.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical) for the DC-DC converters, the device goes into thermal shutdown. In this mode, the P and N-Channel MOSFETs are turned-off. The device continues operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for one of the DC-DC converters will disable both converters simultaneously.

The thermal shutdown temperature for the LDOs are set to typically 140°C. Therefore an LDO that can be used to power an external voltage will never heat up the chip high enough to turn off the DC-DC converters. If one LDO exceeds the thermal shutdown temperature, all LDOs will turn off simultaneously.

7.3.5.1 Low Dropout Voltage Regulators

The low dropout (LDO) voltage regulators are designed to be stable with low value ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 280 mV at rated output current. Each LDO supports a current limit feature. The LDOs are enabled by the EN_LDO1, EN_LDO2, and EN_LDO3 pin. The output voltage of LDO1 and LDO2 is set using an external resistor divider whereas LDO3 has a fixed output voltage of 1.3 V.

7.4 Device Functional Modes

7.4.1 Power Save Mode

The Power Save Mode is enabled with the MODE pin set to low. If the load current decreases, the converters enter Power Save Mode operation automatically. During Power Save Mode the converters operate with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

To optimize the converter efficiency at light load the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then Power Save Mode is entered. The typical threshold can be calculated according to Equation 1 and Equation 2.

$$I_{PFM\_enter} = \frac{V_{INDCDC1/2}}{32\ \Omega} \quad (1)$$

where

- I_{PFM_enter} is the average output current threshold to enter PFM mode.

$$I_{PFM\_leave} = \frac{V_{INDCDC1/2}}{24\ \Omega} \quad (2)$$

where

- I_{PFM_leave} is the average output current threshold to leave PFM mode.

During the Power Save Mode the output voltage is monitored with a comparator. As the output voltage falls below the skip comparator threshold (skip comp) of $V_{OUTnominal}$ +1%, the P-channel switch will turn on and the converter effectively delivers a constant current as defined above. If the load is below the delivered current then the output voltage will rise until the same threshold is crossed again, whereupon all switching activity ceases, hence reducing the quiescent current to a minimum until the output voltage has dropped below the threshold again. If the load current is greater than the delivered current then the output voltage will fall until it crosses the skip comparator low (Skip Comp Low) threshold set to 1% below nominal V_{OUT}, whereupon Power Save Mode is exited and the converter returns to PWM mode.

These control methods reduce the quiescent current typically to 12 μA per converter and the switching frequency to a minimum thereby achieving the highest converter efficiency. The PFM mode operates with very low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor; increasing capacitor values will make the output ripple tend to zero.

The Power Save Mode can be disabled by driving the MODE pin high. Both converters will operate in fixed PWM mode. Power Save Mode Enable/Disable applies to both converters.

Device Functional Modes (continued)

7.4.1.1 Dynamic Voltage Positioning

This feature reduces the voltage undershoot and overshoot at load steps from light to heavy load and vice versa. It is activated in Power Save Mode operation when the converter runs in PFM Mode. It provides more headroom for both the voltage drop at a load step increase and the voltage increase at a load throw-off which improves load transient behavior.

At light loads, in which the converters operate in PFM Mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage will drop until it reaches the skip comparator low threshold set to –1% below the nominal value and enters PWM mode. During a load throw off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel switch.

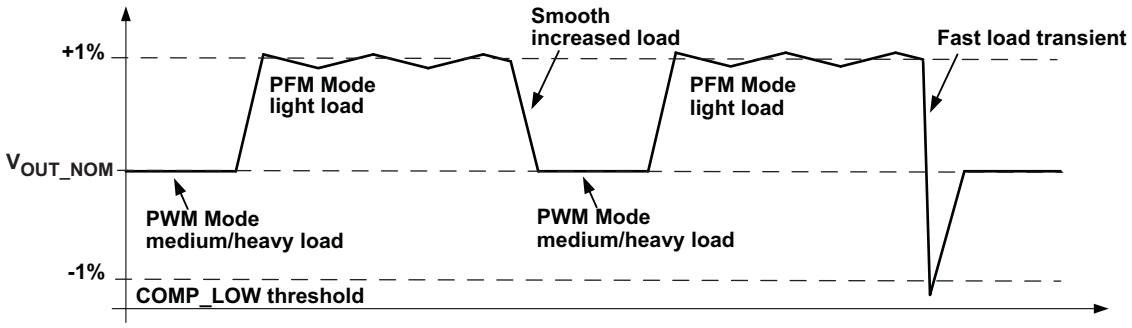


Figure 7. Dynamic Voltage Positioning

7.4.1.2 Soft Start

The two converters have an internal soft start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp up is controlled as shown in Figure 8.

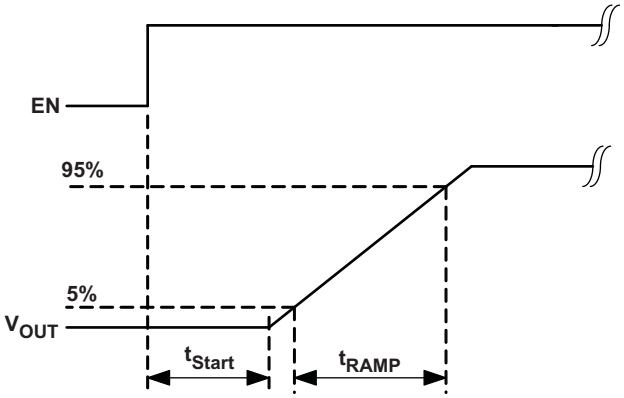


Figure 8. Soft Start

Device Functional Modes (continued)

7.4.1.3 100% Duty-Cycle Low Dropout Operation

The converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range; essentially the minimum input voltage to maintain regulation depends on the load current and output voltage and can be calculated as shown in Equation 3.

$$V_{INmin} = V_{OUTmax} + I_{OUTmax} \times (RDSon_{max} + R_L) \quad (3)$$

where

- I_{OUTmax} = maximum output current plus inductor ripple current
- $RDSon_{max}$ = maximum P-channel switch $r_{DS(on)}$
- R_L = DC resistance of the inductor
- V_{OUTmax} = nominal output voltage plus maximum output voltage tolerance

With decreasing load current, the device automatically switches into pulse skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically the switching losses are minimized and the device runs with a minimum quiescent current maintaining high efficiency.

In Power Save Mode the converter only operates when the output voltage trips below its nominal output voltage. It ramps up the output voltage with several pulses and goes again into Power Save Mode when the output voltage exceeds the nominal output voltage.

7.4.1.4 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning by disabling the converter at low input voltages and from excessive discharge of the battery. The undervoltage lockout threshold is 1.8 V (typical) and 2 V (maximum).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65053-Q1 PMIC integrates two step-down converters and three LDOs which can be used to power the voltage rails needed by a processor or another application. The PMIC can be controlled via the ENABLE and MODE pins or sequenced from the VIN using RC delay circuits. There is a logic output, $\overline{\text{RESET}}$, to provide the application processor or load a logic signal indicating power good or reset.

8.2 Typical Application

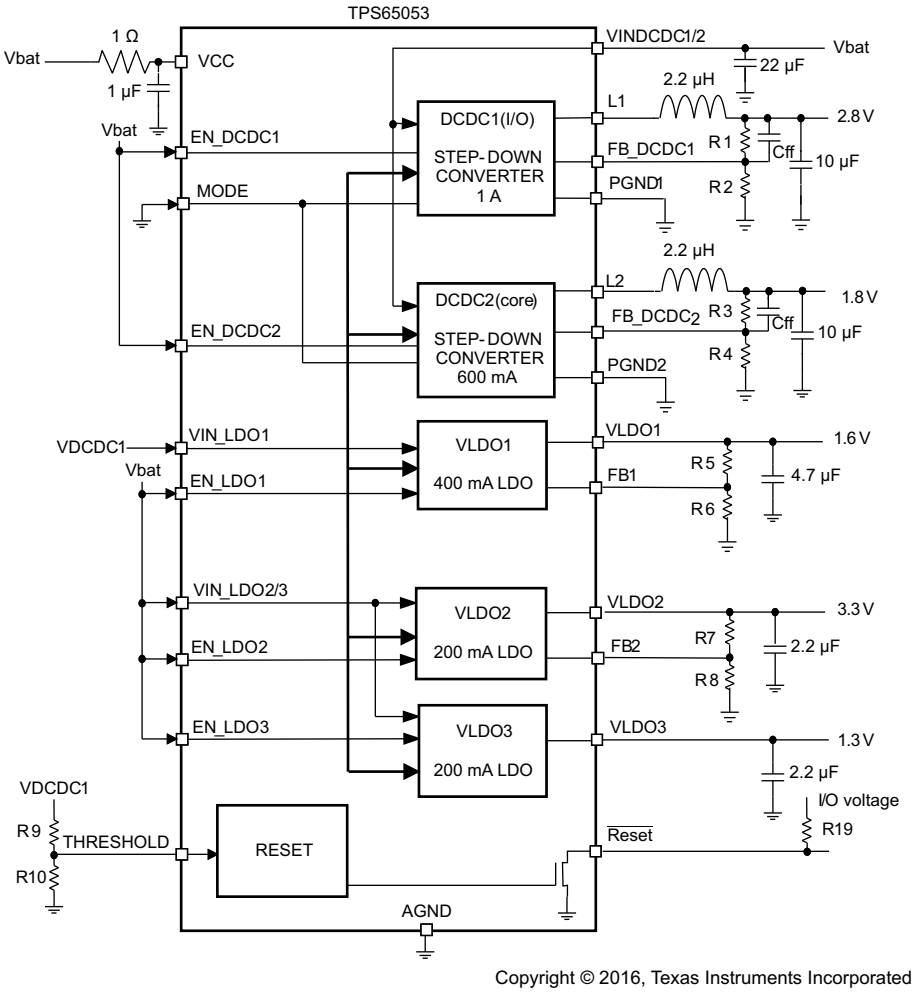


Figure 9. Typical Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the design parameters for this application example.

Table 1. Power Design Requirements

PARAMETER	VALUE
Buck 1 and 2 Input voltage, $V_{INDCDC1/2}$	2.9 to 6 V (labeled V_{bat} in Figure 9)
Buck 1 Output voltage, V_{DCDC1}	2.85 V (see Table 2 for FB_DCDC1 resistor divider selection)
Buck 1 Output current, $I_{OUTDCDC1}$	1 A
Buck 2 Output voltage, V_{DCDC2}	1.8 V (see Table 2 for FB_DCDC2 resistor divider selection)
Buck 2 Output current, $I_{OUTDCDC2}$	600 mA
Linear Regulator 1 Input voltage, V_{INLDO1}	2.85 V (from V_{DCDC1}, as shown in Figure 9)
Linear Regulator 1 Output voltage, V_{LDO1}	1.6 V (see Table 5 for FB_LDO1 resistor divider selection)
Linear Regulator 1 Output current, I_{LDO1}	400 mA
Linear Regulator 2 and 3 Input voltage, $V_{INLDO2/3}$	2.9 to 6 V (labeled V_{bat} in Figure 9)
Linear Regulator 2 Output voltage, V_{LDO2}	3.3 V (see Table 5 for FB_LDO2 resistor divider selection)
Linear Regulator 2 Output current, I_{LDO2}	200 mA
Linear Regulator 3 Output voltage, V_{LDO3}	1.3 V (fixed)
Linear Regulator 3 Output current, I_{LDO3}	200 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Setting

Use Equation 4 to calculate the output voltage of the DC-DC converters, with an internal reference voltage V_{ref}, 0.6 V (typical). This voltage can be set by an external resistor network.

$$V_{OUT} = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{4}$$

TI recommends setting the total resistance of R1 + R2 to less than 1 MΩ. The resistor network connects to the input of the feedback amplifier; therefore, requiring some small feed-forward capacitor in parallel to R1. A typical value of 47 pF is sufficient.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{(FB\_DCDC1)}}\right) - R2 \tag{5}$$

Table 2. Typical DC-DC Feedback Resistor Values

OUTPUT VOLTAGE	R1	R2	NOMINAL VOLTAGE	TYPICAL Cff
3.3 V	680 kΩ	150 kΩ	3.32 V	47 pF
3 V	510 kΩ	130 kΩ	2.95 V	47 pF
2.85 V	560 kΩ	150 kΩ	2.84 V	47 pF
2.5 V	510 kΩ	160 kΩ	2.51 V	47 pF
1.8 V	300 kΩ	150 kΩ	1.8 V	47 pF
1.6 V	200 kΩ	120 kΩ	1.6 V	47 pF
1.5 V	300 kΩ	200 kΩ	1.5 V	47 pF
1.2 V	330 kΩ	330 kΩ	1.2 V	47 pF

8.2.2.2 Output Filter Design (Inductor and Output Capacitor)

8.2.2.2.1 Inductor Selection

The two converters operate typically with a 2.2-µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For output voltages higher than 2.8 V, an inductor value of 3.3 µH minimum should be selected, otherwise the inductor current will ramp down too fast causing imprecise internal current measurement and therefore increased output voltage ripple under some operating conditions in PFM mode.

The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

Use Equation 6 to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 6. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \qquad I_{L\,max} = I_{OUT\,max} + \frac{\Delta I_L}{2}$$

where

- f = Switching Frequency (2.25-MHz typical)
- L = Inductor Value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum Inductor current (6)

The highest inductor current occurs at the maximum V_{IN}. Open core inductors have a soft saturation characteristic, and they can normally handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. The fact that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies must be considered. Refer to Table 3 and the typical applications for possible inductors.

Table 3. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER
LPS3010	2.2 µH	Coilcraft
LPS3015	3.3 µH	Coilcraft
LPS4012	2.2 µH	Coilcraft
VLF4012	2.2 µH	TDK

8.2.2.2.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the two converters allow the use of small ceramic capacitors with a typical value of 10 µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended. See the recommended components in Table 5.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. Use Equation 7 to calculate the rms ripple current.

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (7)$$

At nominal load current, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor as shown in Equation 8.

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (8)$$

Where the highest output voltage ripple occurs at the highest input voltage, V_{IN}.

At light load currents, the converters operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

8.2.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter, having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 4. Possible Capacitors for DC-DC Converters and LDOs

CAPACITOR VALUE	SIZE	SUPPLIER	TYPE
2.2 µF	0805	TDK C2012X5R0J226MT	Ceramic
2.2 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic

8.2.2.3 Low Dropout Voltage Regulators (LDOs)

The output voltage of LDO1 and LDO2 can be set by an external resistor network and can be calculated as shown in Equation 9 with an internal reference voltage, V_{ref}, typical 1 V.

$$V_{OUT} = V_{ref} \times \left(1 + \frac{R5}{R6} \right) \quad (9)$$

TI recommends setting the total resistance of R5 + R6 to less than 1 MΩ. Typically, no feedforward capacitor is required at the voltage dividers for the LDOs.

$$V_{OUT} = V_{(FB)} \times \frac{R5 + R6}{R6} \qquad R5 = R6 \times \left(\frac{V_{OUT}}{V_{(FB)}} \right) - R6 \quad (10)$$

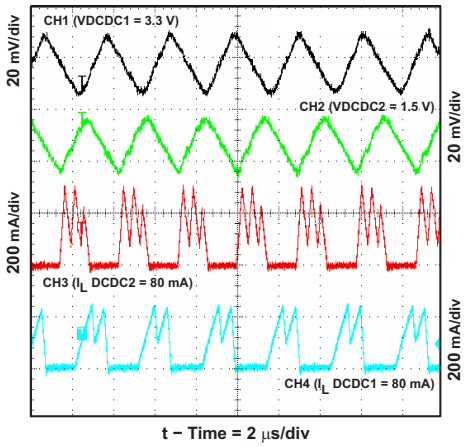
Table 5. Typical LDO Feedback Resistor Values

OUTPUT VOLTAGE	R5	R6	NOMINAL VOLTAGE
3.3 V	300 kΩ	130 kΩ	3.31 V
3 V	300 kΩ	150 kΩ	3 V
2.85 V	240 kΩ	130 kΩ	2.85 V
2.8 V	360 kΩ	200 kΩ	2.8 V
2.5 V	300 kΩ	200 kΩ	2.5 V
1.8 V	240 kΩ	300 kΩ	1.8 V
1.5 V	150 kΩ	300 kΩ	1.5 V
1.3 V	36 kΩ	120 kΩ	1.3 V
1.2 V	100 kΩ	510 kΩ	1.19 V
1.1 V	33 kΩ	330 kΩ	1.1 V

8.2.2.3.1 Input Capacitor and Output Capacitor Selection for the LDOs

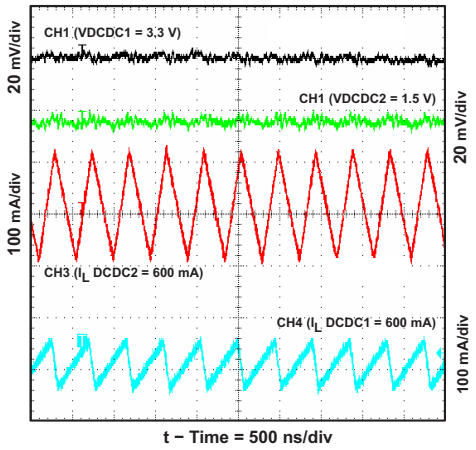
The minimum input capacitor on VIN_LDO1 and on VIN_LDO2/3 is 2.2 µF minimum. LDO1 is designed to be stable with an output capacitor of 4.7 µF minimum; whereas, LDO2 and LDO3 are stable with a minimum capacitor value of 2.2 µF.

8.2.3 Application Curves



PWM/PFM Mode = Low

Figure 10. Output Voltage Ripple of DCDC1/2 in PFM Mode



PWM Mode = High

Figure 11. Output Voltage Ripple of DCDC1/2 in PWM Mode

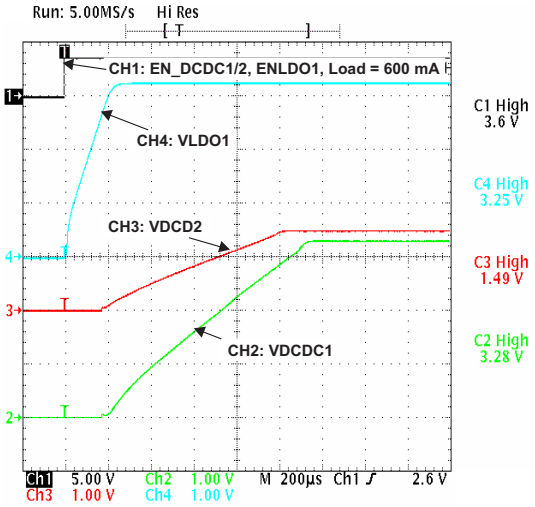


Figure 12. DCDC1, DCDC2, LDO1 Startup Timing

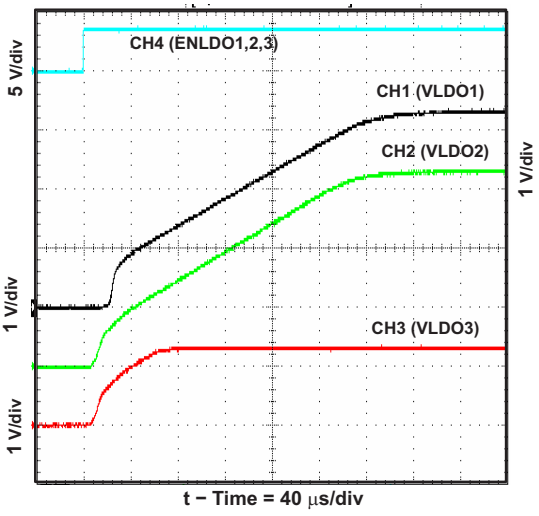


Figure 13. LDO1 to LDO3 Startup Timing

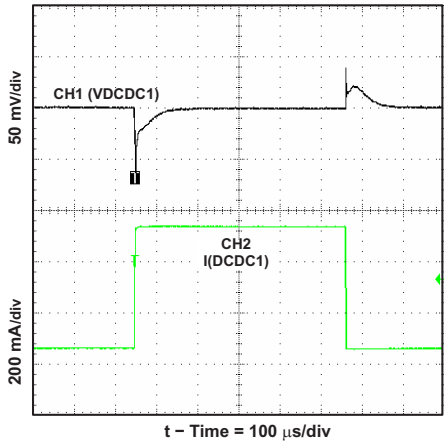


Figure 14. DCDC1 Load Transient Response in PWM Mode

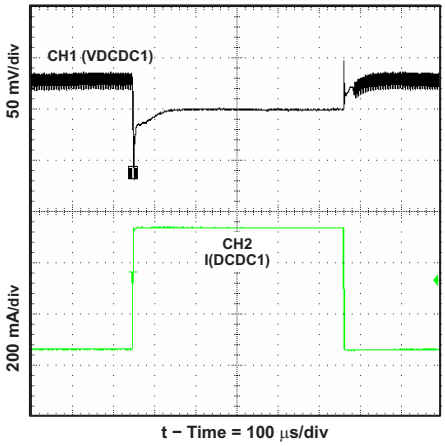


Figure 15. DCDC1 Load Transient Response in PFM Mode

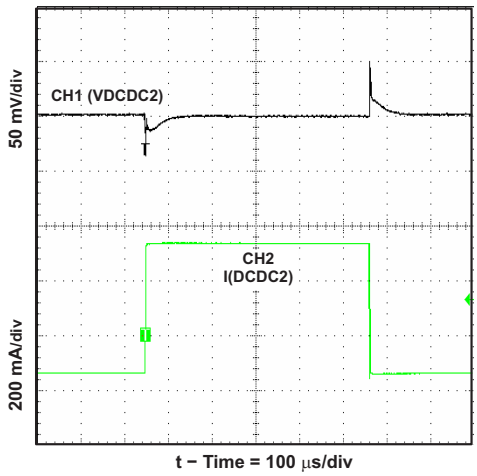


Figure 16. DCDC2 Load Transient Response in PWM Mode

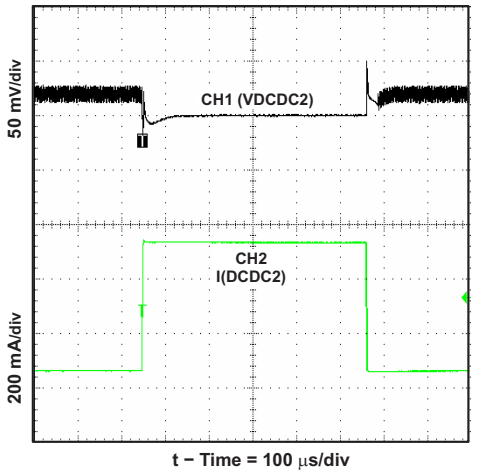


Figure 17. DCDC2 Load Transient Response in PFM Mode

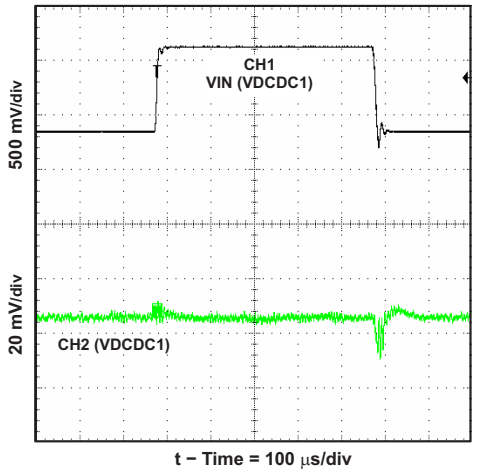


Figure 18. DCDC1 Line Transient Response in PWM Mode

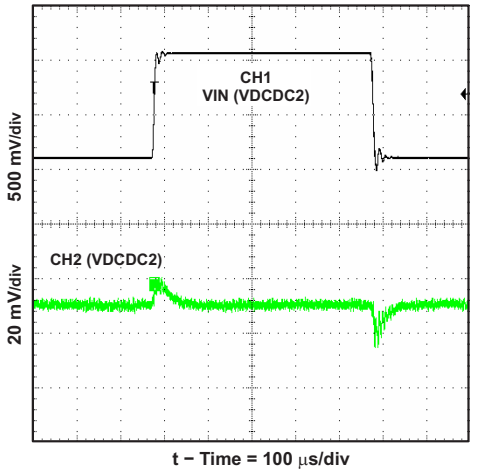


Figure 19. DCDC2 Line Transient Response in PWM Mode

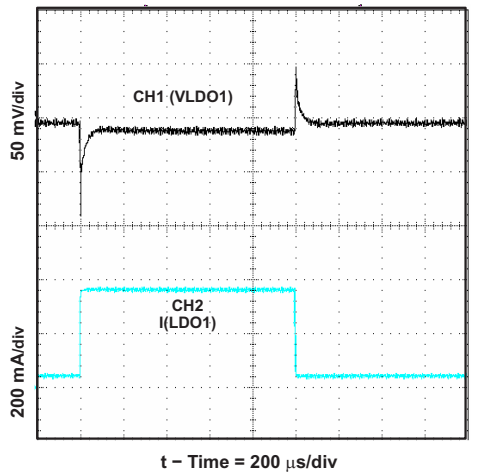


Figure 20. LDO1 Load Transient Response

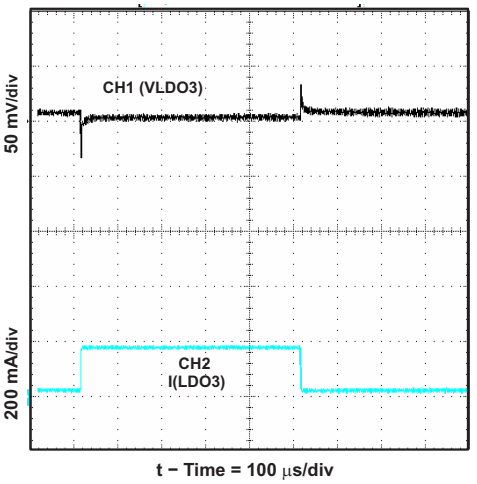


Figure 21. LDO3 Load Transient Response

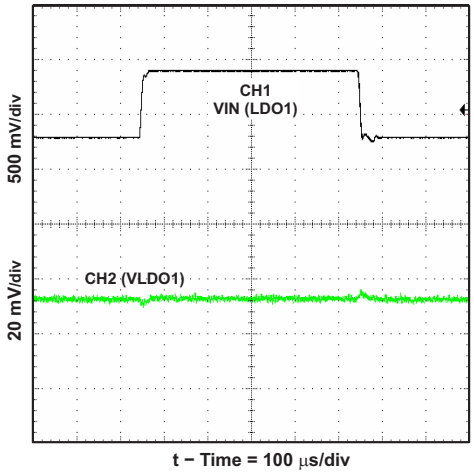


Figure 22. LDO1 Line Transient Response

9 Power Supply Recommendations

The TPS65053-Q1 has only a few power supply recommendations in addition to adhering to the minimum and maximum values in the *Recommended Operating Conditions*. The following check list provides power supply recommendations that should be used in conjunction with complying to the Recommended Operating Conditions of the device.

- 1-µF Bypass cap on VCC, located as close as possible to the VCC pin to ground.
- VCC and VINDCDC1/2 must be connected to the same voltage supply with minimal voltage difference.
- Input capacitors must be present on the VINDCDC1/2, VIN_LDO1, and VIN_LDO2/3 supplies if used.
- Output filters must be used on the outputs of the DCDC converters if used.
- Output capacitors must be used on the outputs of the LDOs if used.

10 Layout

10.1 Layout Guidelines

The following check list provides layout guidelines that have been followed in the *Layout Example* shown in Figure 23.

- The input capacitors for the DC-DC converters should be placed as close as possible to the VINDCDC1/2 pin and the PGND1 and PGND2 pins.
- The inductor of the output filter should be placed as close as possible to the device to provide the shortest switch node possible, reducing the noise emitted into the system and increasing the efficiency.
- Sense the feedback voltage from the output at the output capacitors to ensure the best DC accuracy. Feedback should be routed away from noisy sources such as the inductor. If possible route on the opposing side as the switch node and inductor and place a GND plane between the feedback and the noisy sources or keep-out underneath them entirely.
- Place the output capacitors as close as possible to the inductor to reduce the feedback loop as much as possible. This will ensure best regulation at the feedback point.
- Place the device as close as possible to the most demanding or sensitive load. The output capacitors should be placed close to the input of the load. This will ensure the best AC performance possible.
- The input and output capacitors for the LDOs should be placed close to the device for best regulation performance.
- The use a one common ground plane is recommended for the device layout. The AGND can be separated from the PGND, but a large low parasitic PGND is required to connect the PGND1/2 pins to the CIN and external PGND connections.

10.2 Layout Example

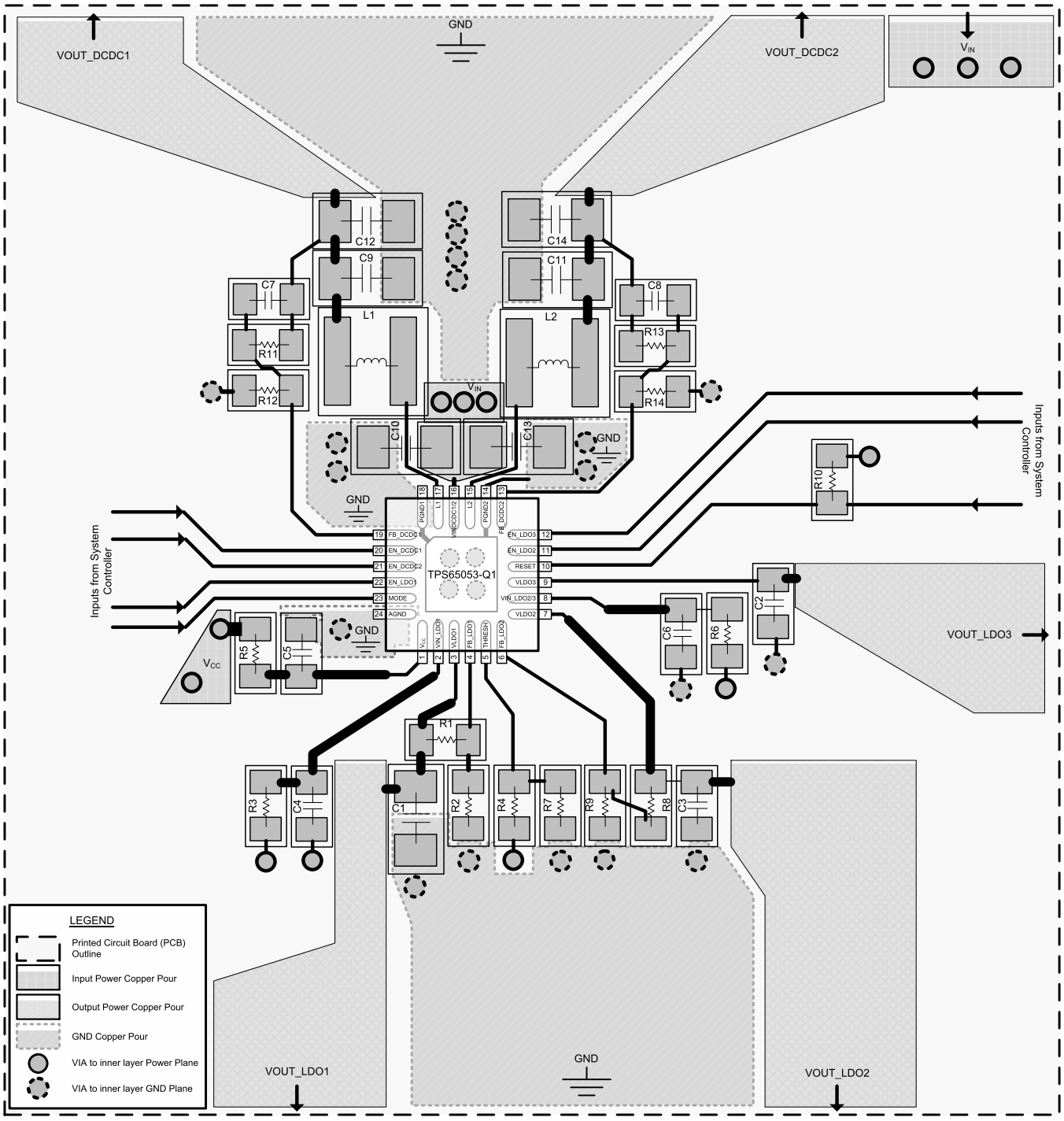


Figure 23. Layout Example for TPS65053-Q1

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Choosing an Appropriate Pull-up/Pull-down Resistor for Open Drain Outputs

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65053IRGERQ1	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65053Q
TPS65053IRGERQ1.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65053Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS65053-Q1 :

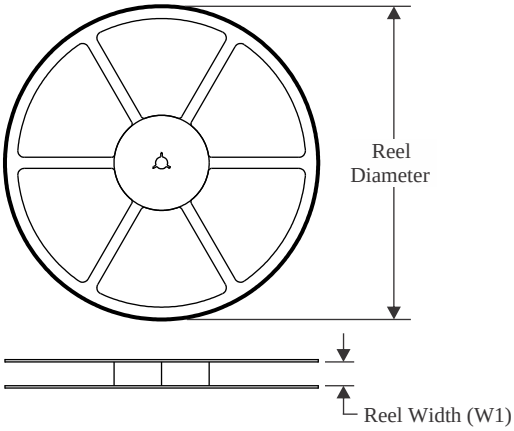
- Catalog : TPS65053

NOTE: Qualified Version Definitions:

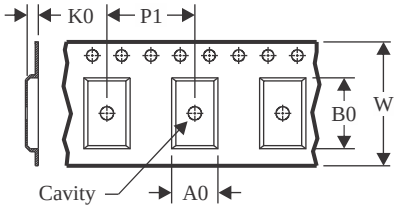
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

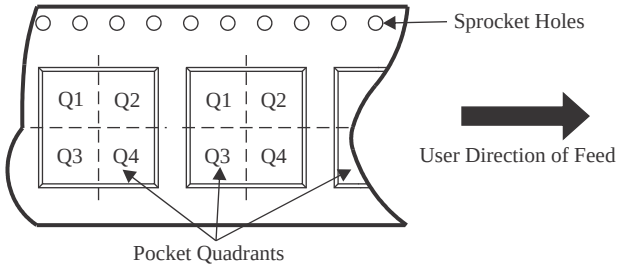


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

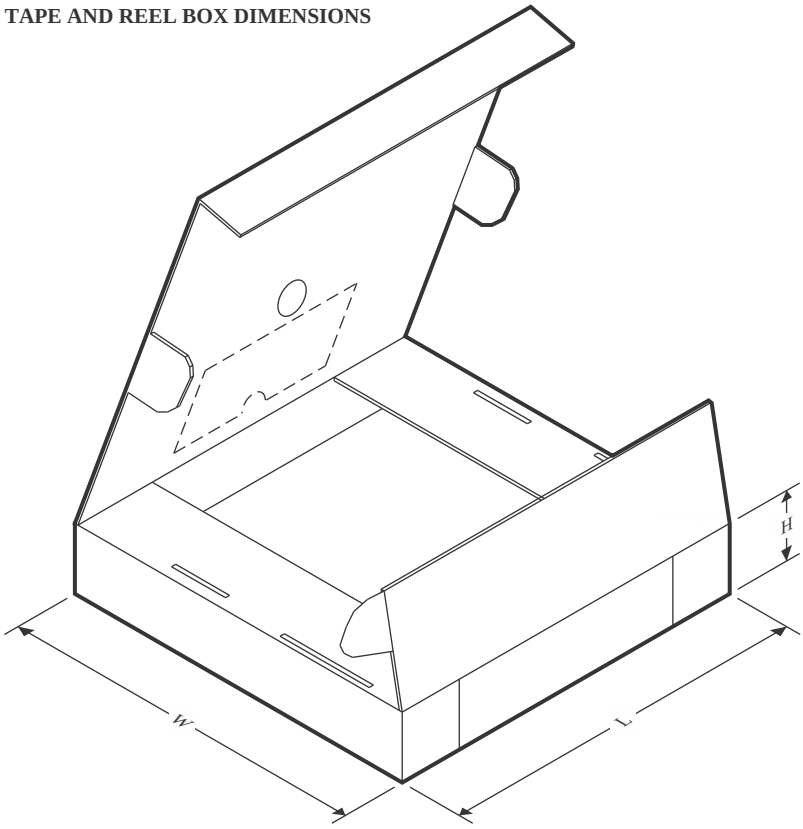
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65053IRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



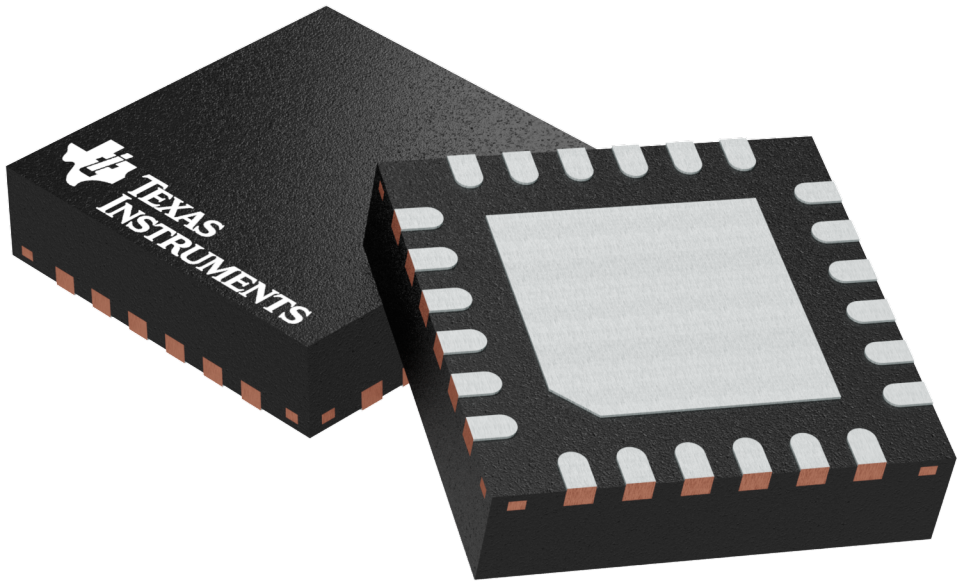
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65053IRGERQ1	VQFN	RGE	24	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

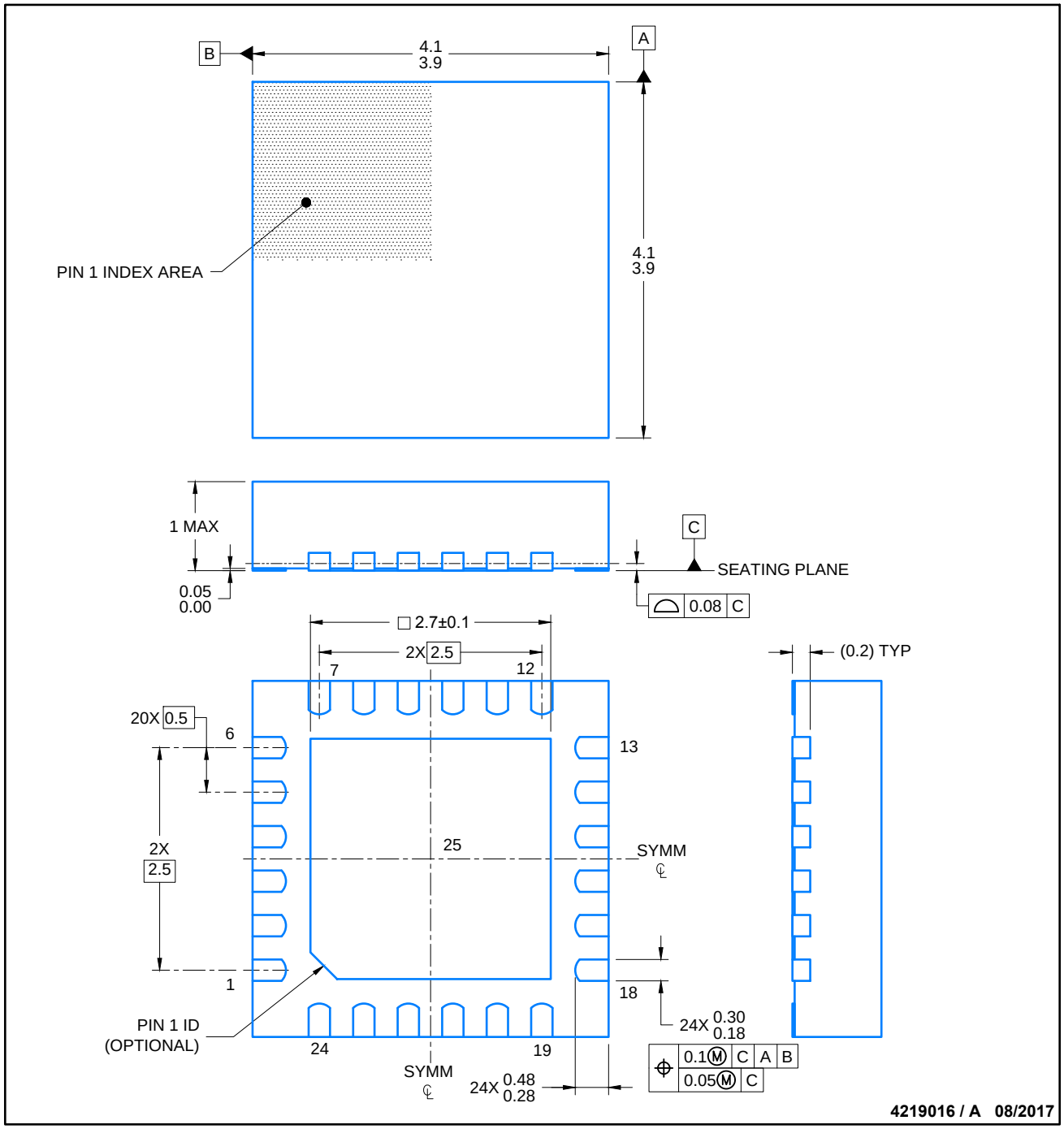
4204104/H

PACKAGE OUTLINE

RGE0024H

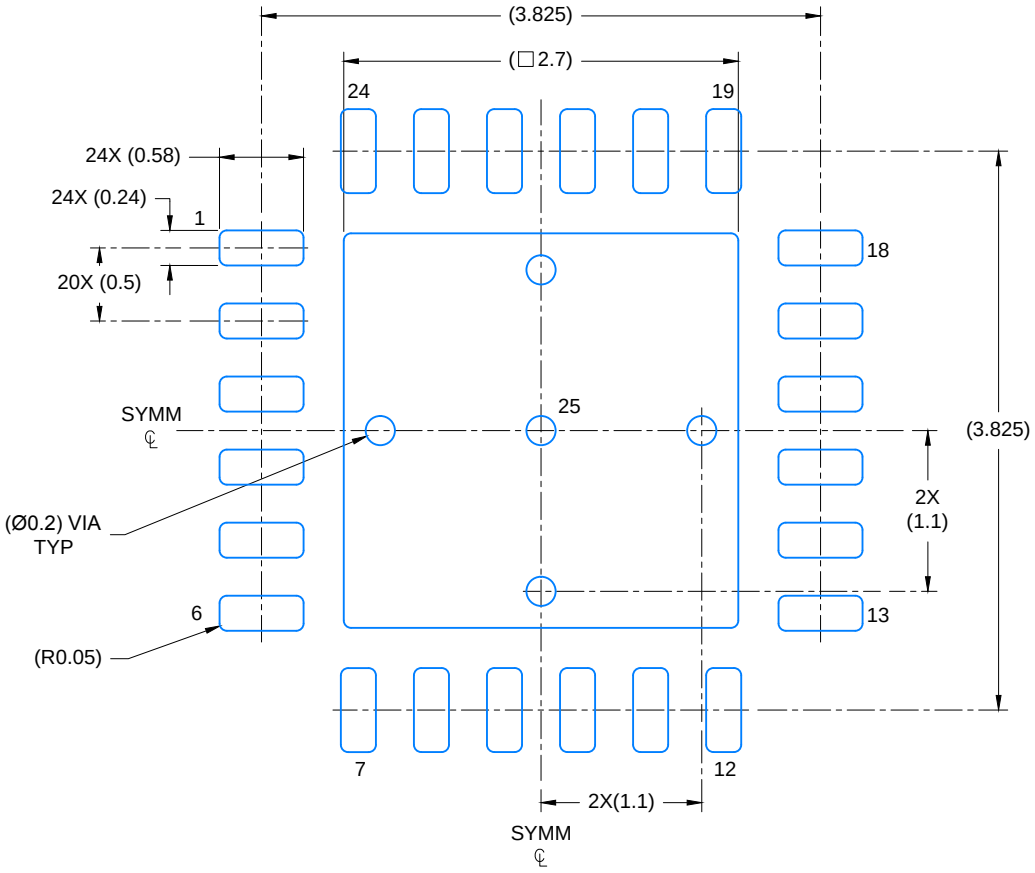
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



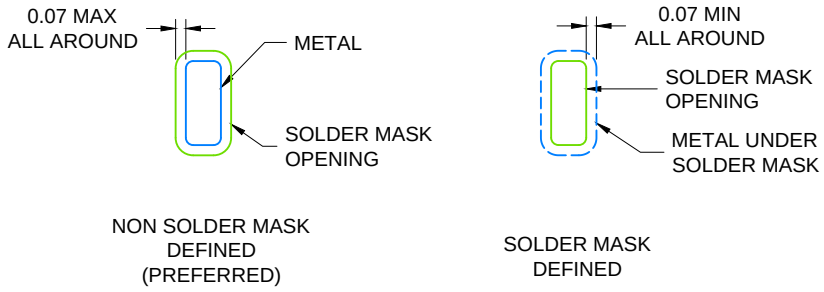
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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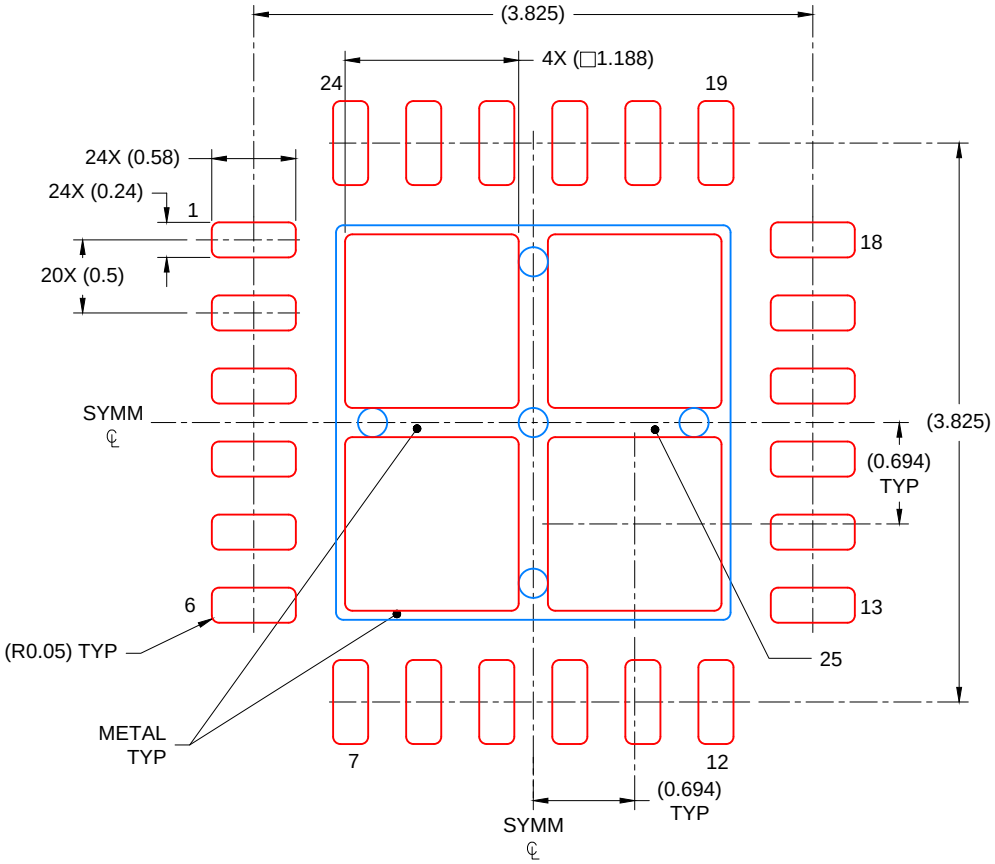
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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