

TPS650333-Q1 Automotive Camera PMIC

1 Features

- Qualified for automotive applications
- Systematic capability of up to ASIL D and SIL 3 targeted
- Hardware integrity up to ASIL B and SIL 2 targeted
- Advanced diagnostics and protection
- AEC-Q100 grade 1 qualified
 - -40°C to $+125^{\circ}\text{C}$ ambient operating temperature range
- Three step-down converters:
 - BUCK1 V_{IN} range from 4.0 V to 18.3 V
 - BUCK1 V_{OUT} range from 2.5 V to 4.0 V
 - BUCK1 output current up to 1500-mA
 - BUCK2 and BUCK3 V_{IN} range from 2.5 V to 5.5 V
 - BUCK2 and BUCK3 V_{OUT} range from 0.9 V to 1.9 V
 - BUCK2 and BUCK3 output current up to 1200-mA
 - Spread-spectrum clock (SSC) generation for reduced EMI
 - 2.3-MHz forced fixed switching frequency PWM operation
- One low dropout (LDO) regulator:
 - V_{IN} range from 2.5 V to 5.5 V
 - V_{OUT} range from 1.8 V to 3.3 V
 - Low noise and high PSRR
 - Adjustable output voltage through $I^2\text{C}$
 - Up to 300-mA output current
- 4.0-mm \times 4.0-mm 24-pin VQFN with wettable flanks

2 Applications

- Automotive camera modules
 - Surround view camera modules
 - Rear view camera modules
 - Driver monitor camera modules
 - Power over coax (POC) camera modules
 - E-mirror camera modules
 - Front view camera modules

3 Description

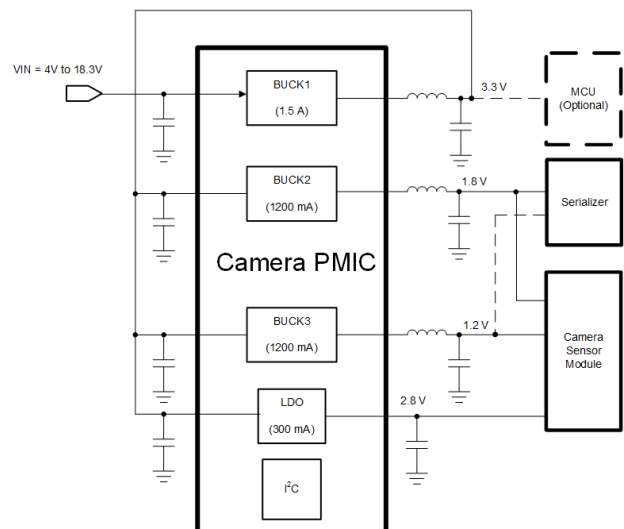
The TPS650333-Q1 device is a highly integrated power management IC for automotive camera modules. This device combines three step-down converters and one low-dropout (LDO) regulator. The BUCK1 step-down converter has an input voltage range up to 18.3 V for connections to power over coax (PoC). All converters operate in a forced fixed-frequency PWM mode. The LDO can supply 300 mA and operate with an input voltage range from 2.5 V to 5.5 V. The step-down converters and the LDO have separate voltage inputs that enable maximum design and sequencing flexibility.

The TPS650333-Q1 is available in a 24-pin VQFN package (4.00 mm \times 4.00 mm).

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
TPS650333-Q1	VQFN (24)	4.00 mm \times 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TPS650333-Q1 Application Circuit



Table of Contents

1 Features	1	5.2 Receiving Notification of Documentation Updates.....	3
2 Applications	1	5.3 Support Resources.....	3
3 Description	1	5.4 Trademarks.....	3
4 Revision History	2	5.5 Electrostatic Discharge Caution.....	3
5 Device and Documentation Support	3	5.6 Glossary.....	3
5.1 Device Support.....	3	6 Mechanical, Packaging, and Orderable Information	3

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2023	*	Initial Release

5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.4 Trademarks

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5.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65033302RGERQ1	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU SN	Level-3-260C-168 HR	-40 to 125	TPS6503 3302-Q1
TPS65033302RGERQ1.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS6503 3302-Q1
TPS65033303RGERQ1	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU SN	Level-3-260C-168 HR	-40 to 125	TPS6503 3303-Q1
TPS65033303RGERQ1.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS6503 3303-Q1
TPS65033304RGERQ1	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU SN	Level-3-260C-168 HR	-40 to 125	TPS6503 3304-Q1
TPS65033304RGERQ1.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS6503 3304-Q1

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

RGE 24

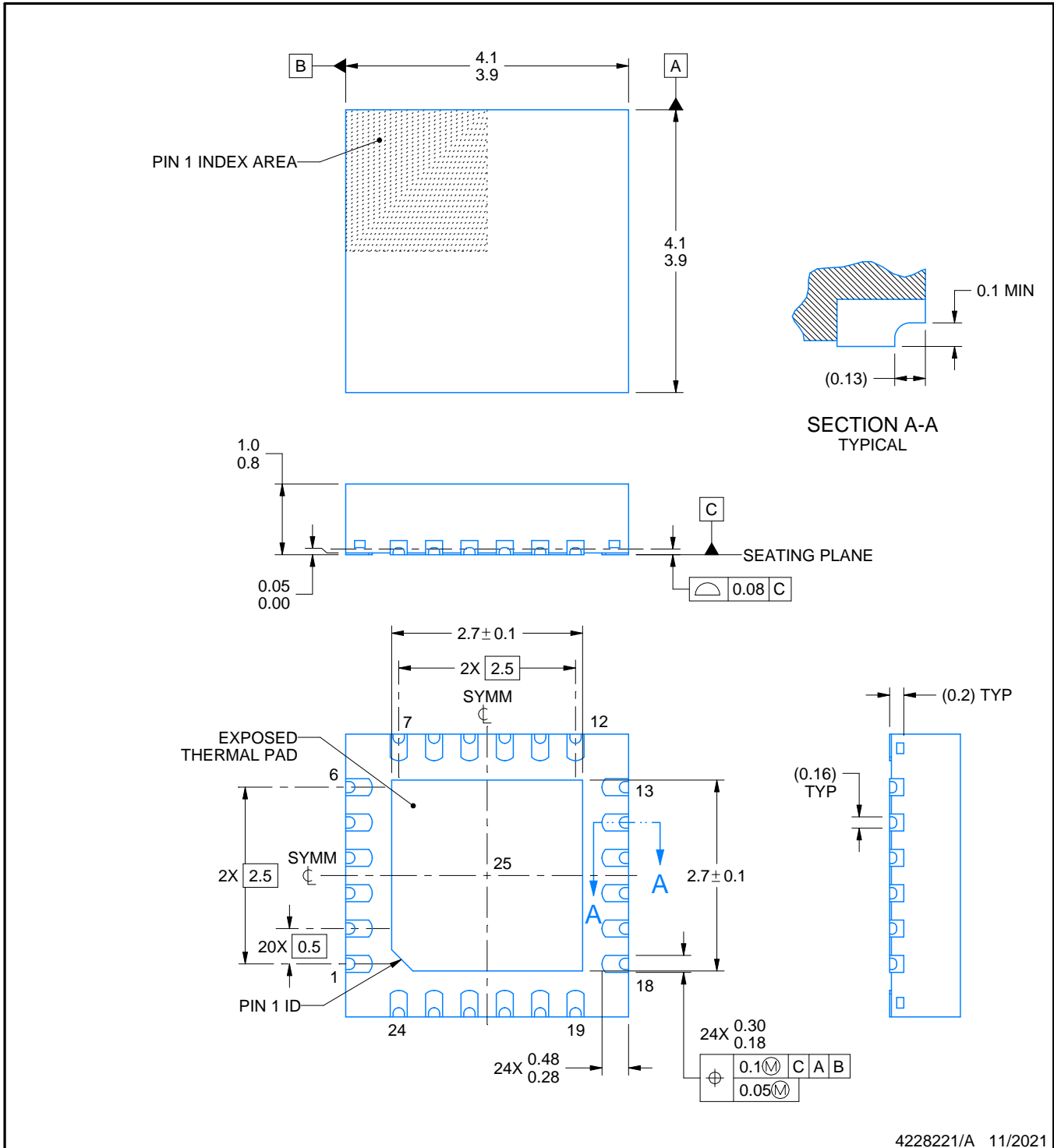
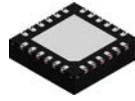
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



NOTES:

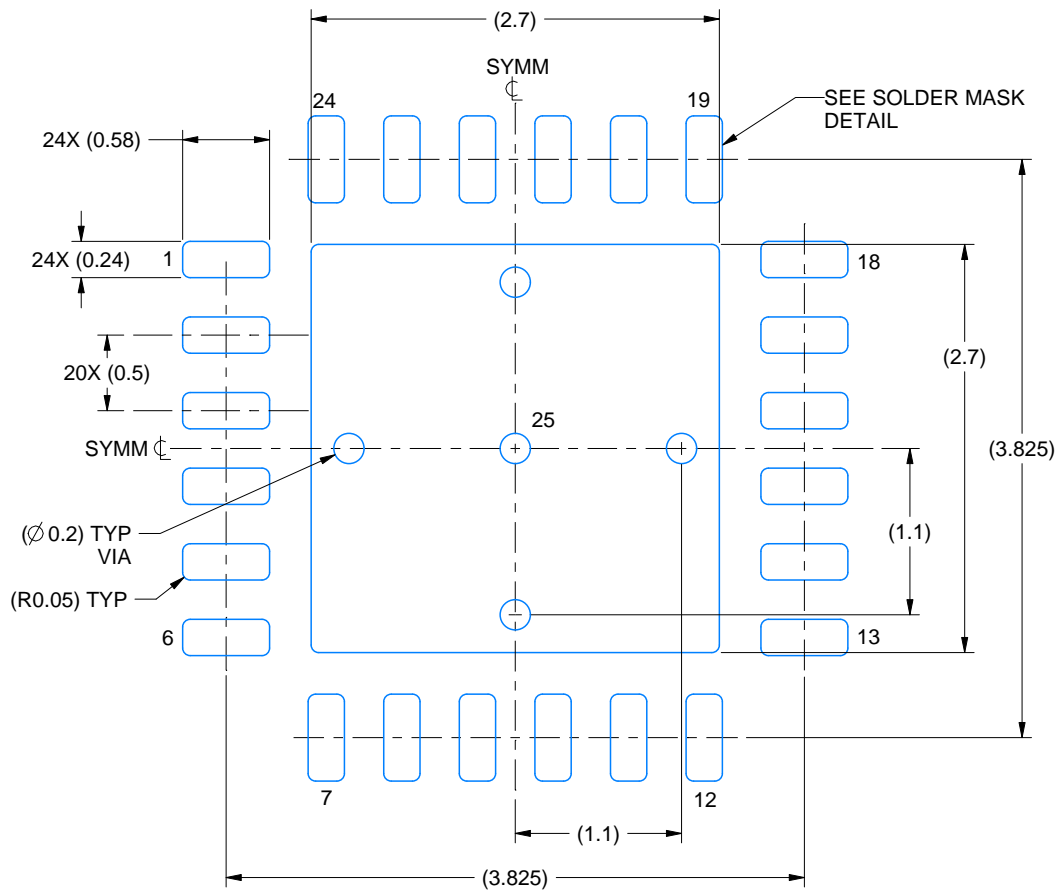
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

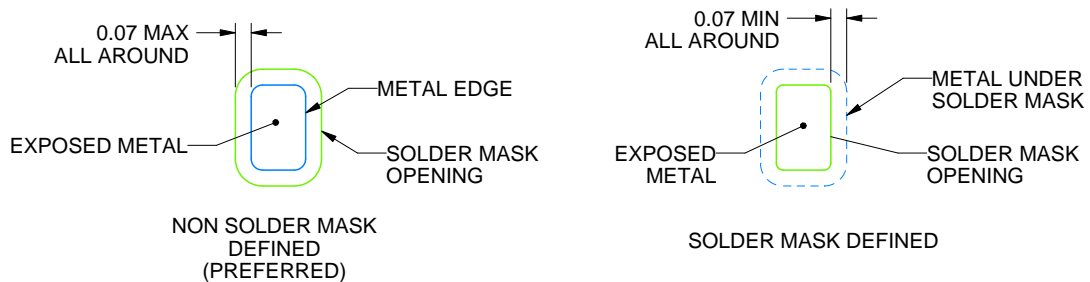
RGE0024U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4228221/A 11/2021

NOTES: (continued)

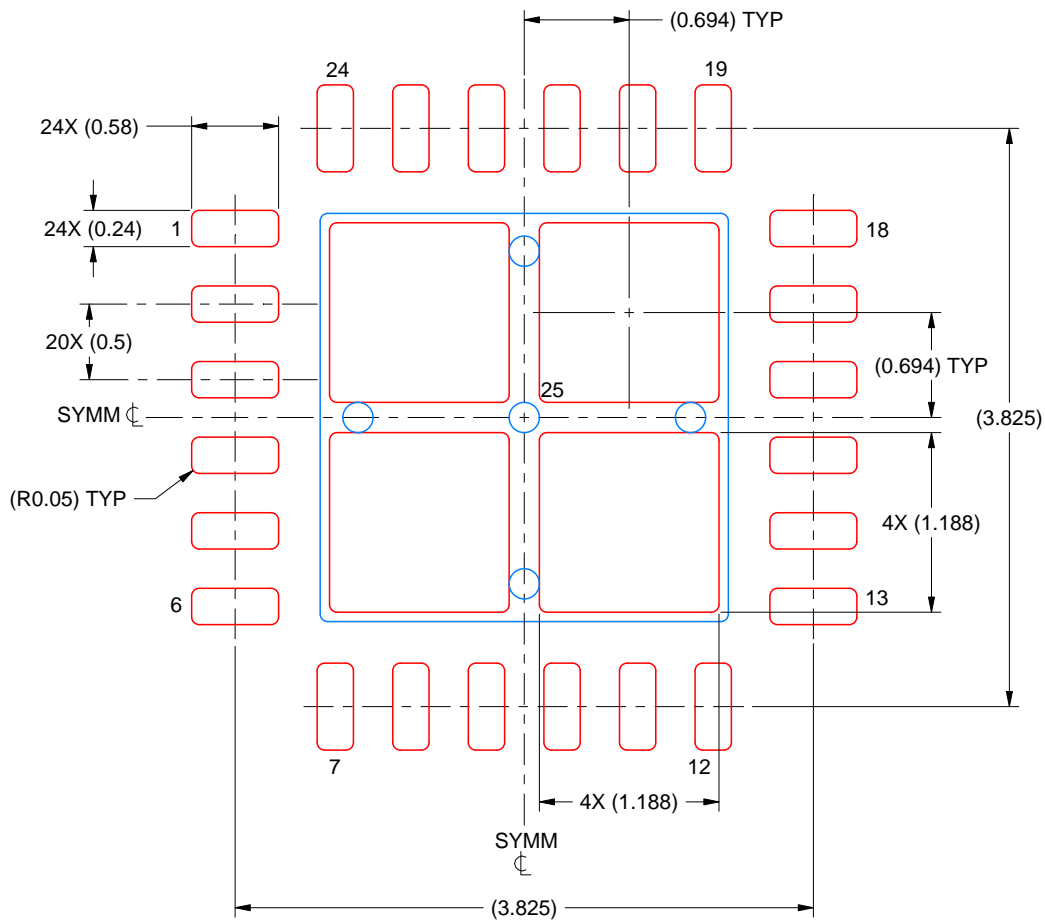
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



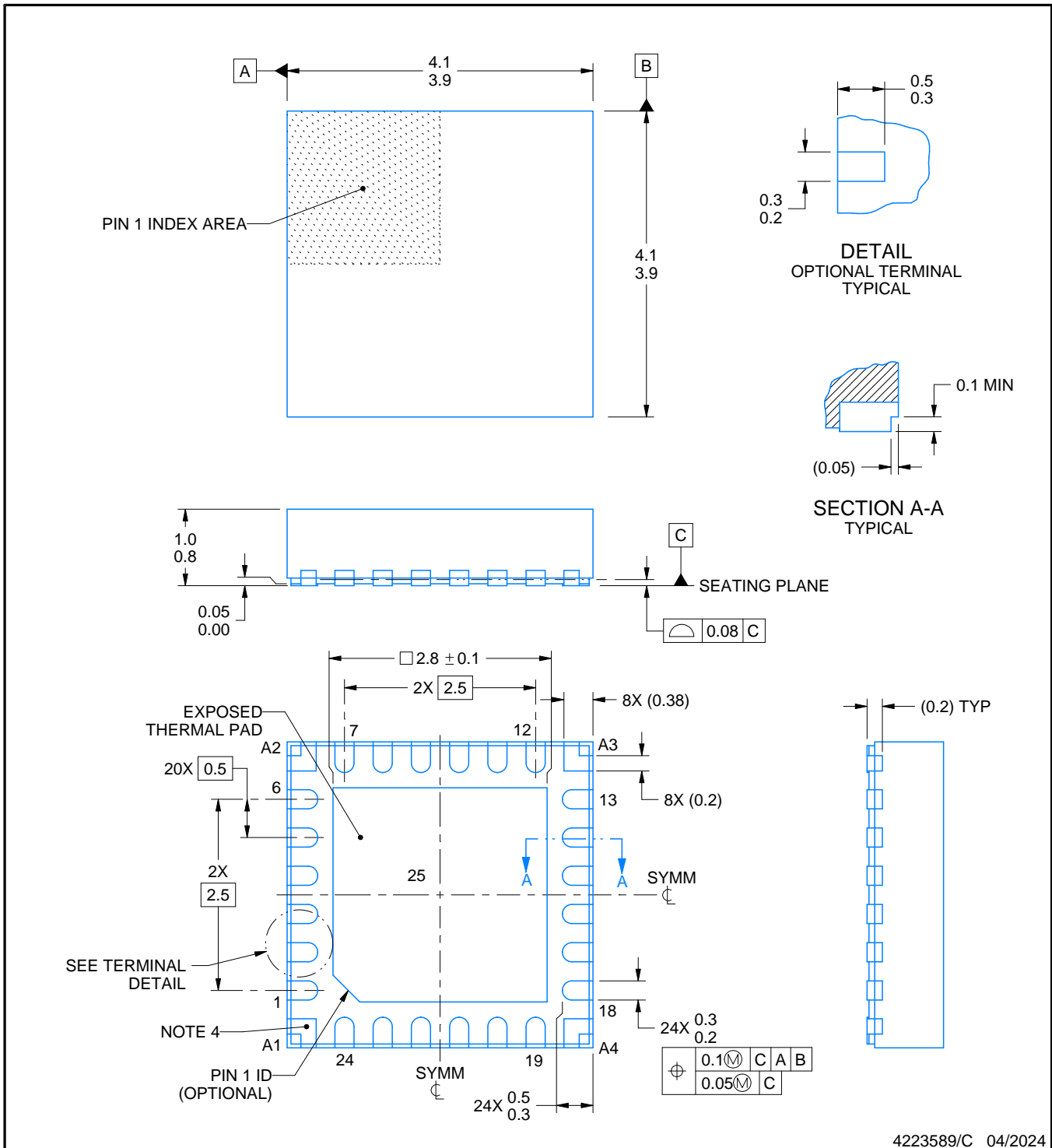
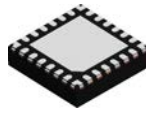
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 25
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4228221/A 11/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4223589/C 04/2024

NOTES:

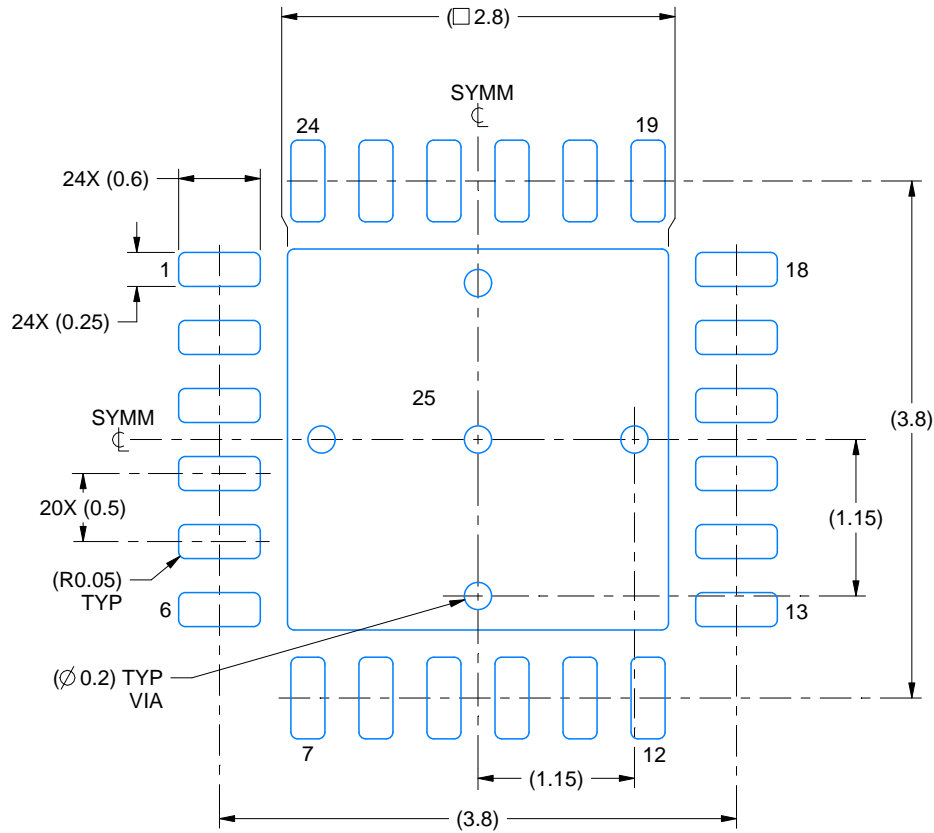
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Corner pins A1-A4 are physically connected to exposed thermal pad internally. Soldering these is optional, but would require customer to supply land design and stencil.

EXAMPLE BOARD LAYOUT

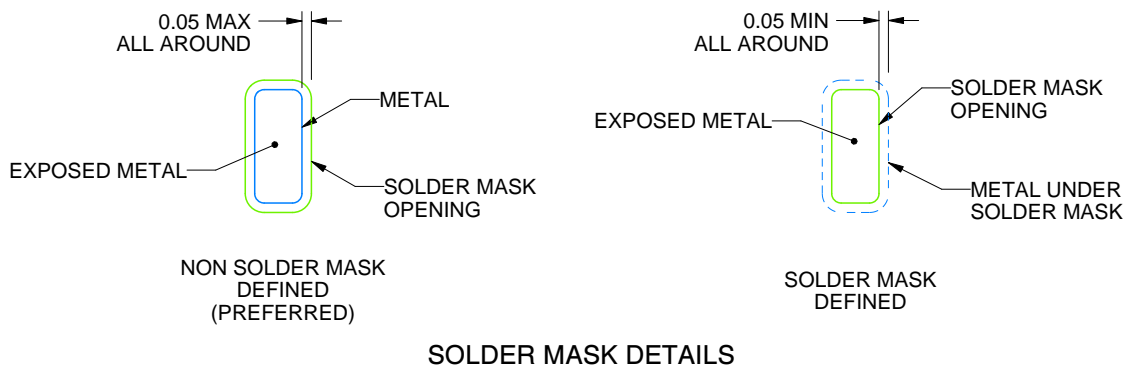
RGE0024K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



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NOTES: (continued)

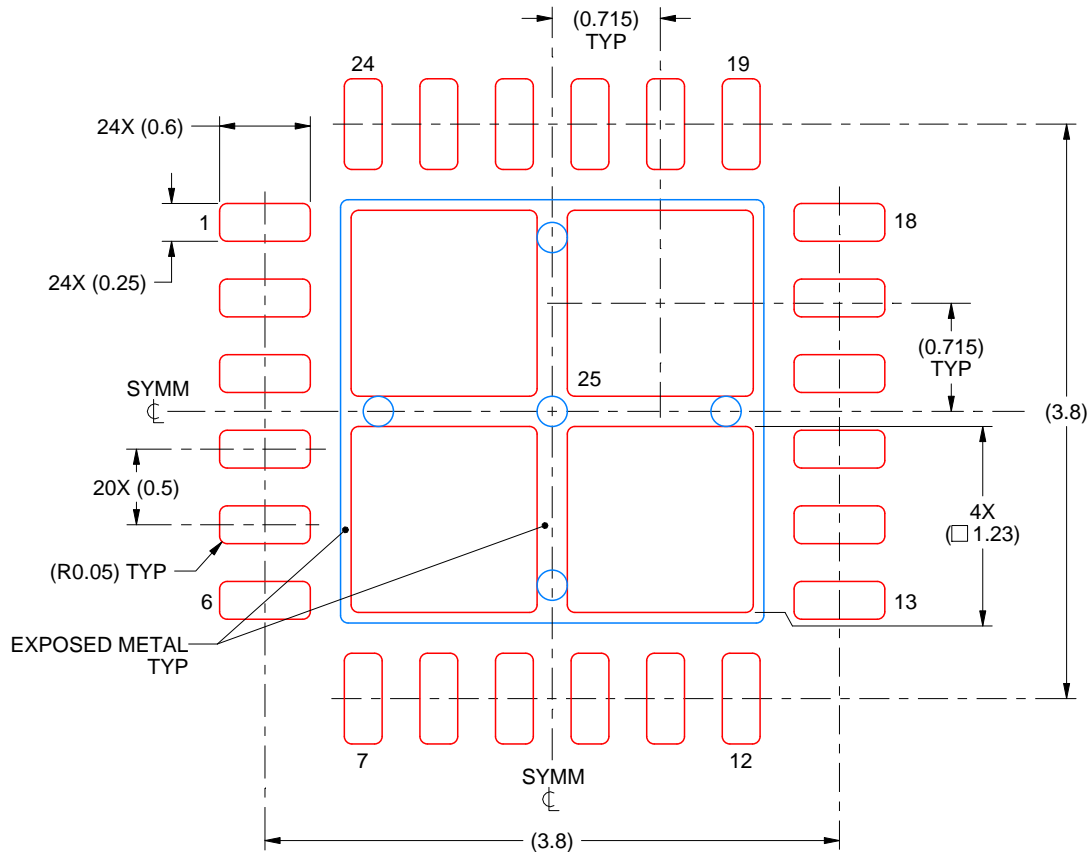
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 25:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223589/C 04/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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