TPS62A03x 3A, High-Efficiency, Synchronous, Buck Converter in a SOT563 Package

1 Features

- 42mΩ and 27.5mΩ low R_{DSON} switches
- 2.5V to 5.5V input voltage range
- 0.6V to V_{IN} adjustable output voltage range
- 28µA (typical) quiescent current ($V_{FB} > V_{REF}$)
- 150nA (typical) shutdown current (EN = Low)
- 1.2V I/O compatible EN input
- 1% feedback accuracy (0°C to 125°C)
- 100% mode operation
- 2.2MHz switching frequency
- Power save mode or forced PWM option available
- Power-good output pin
- Short-circuit protection (HICCUP)
- Internal soft start-up
- Active output discharge
- Thermal shutdown protection
- Improved drop-in replacement for TLV62585 (DRL)

2 Applications

- Set top box, TV applications
- IP network camera, Multi-function printer
- Wireless router, solid state drive
- Battery-powered applications
- General purpose point-of-load supply

3 Description

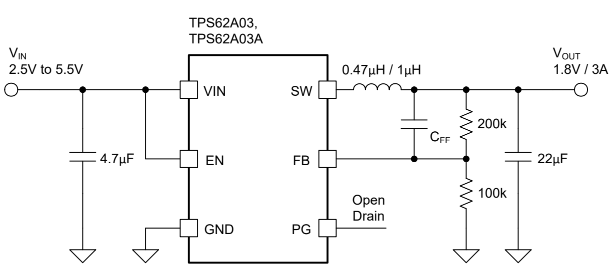
The TPS62A03 and TPS62A03A are synchronous, step-down, buck DC/DC converters designed for high efficiency and compact design size. The devices integrate switches capable of delivering an output current up to 3A. At medium to heavy loads, the devices operate in pulse width modulation (PWM) mode with 2.2MHz switching frequency. At light load, the TPS62A03 automatically enters power save mode (PSM) maintaining high efficiency over the entire load current range. The TPS62A03A variant of this device operates in PWM mode across the whole load current range with a fixed switching frequency. In shutdown, the current consumption is minimal for both devices.

The TPS62A03 and TPS62A03A provide an adjustable output voltage through an external resistor divider. An internal soft-start circuit limits the inrush current during start-up. Overcurrent protection and thermal shutdown protect device and application under fault conditions. A power good signal indicates that the output voltage is in correct regulation. The devices are available in a SOT563 package. The TPS62A03 and TPS62A03A can upgrade existing TLV62585 based power supply circuits if better efficiency or higher accuracy over a wider temperature range is needed.

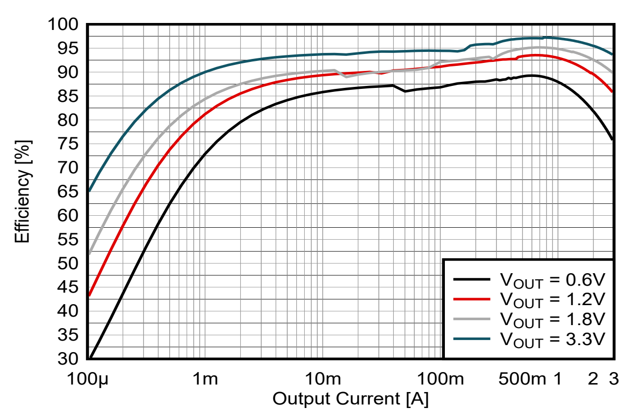
Device Information

PART NUMBER	MODE	PACKAGE[1]	PACKAGE SIZE[2]
TPS62A03	PSM, PWM	DRL (SOT-563, 6)	1.60mm × 1.60mm × 0.6mm
TPS62A03A	FPWM		

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable. The height is a maximum value.



Typical Application



Efficiency vs Output Current at $5V_{IN}$

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4 Device Comparison Table

Device Number	Output Current	Package	Operation Mode
TPS62A03DRLR	3A	SOT-563	PSM, PWM
TPS62A03ADRLR	3A	SOT-563	FPWM

5 Pin Configuration and Functions

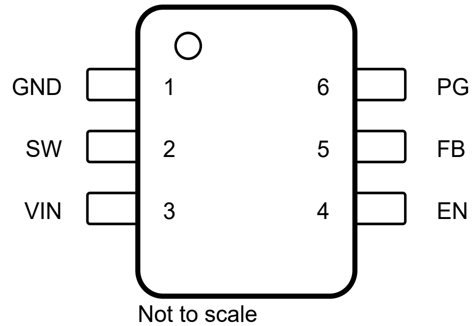


Figure 5-1. 6-Pin DRL SOT-563 Package (Top View)

Table 5-1. Pin Functions

SOT563-6		TYPE[1]	DESCRIPTION
NAME	NO.		
EN	4	I	Device enable logic input. Logic high enables the device. Logic low disables the device and turns the device into shutdown. Do not leave the pin floating.
FB	5	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	1	G	Ground pin
PG	6	O	Power-good open-drain output pin. The pullup resistor cannot be connected to any voltage higher than 5.5V. If unused, leave the pin open or connect to GND.
SW	2	O	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	3	I	Power supply voltage pin

(1) I = Input, O = Output, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, EN, PG	–0.3	6	V
	SW, DC	–0.3	V_{IN} + 0.3	V
	SW, transient < 10ns	–3.0	10	V
	FB	–0.3	3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		2.5		5.5	V
V_{OUT}	Output voltage range		0.6		V_{IN}	V
I_{OUT}	Output current range	TPS62A03			3	A
L	Effective inductance		0.3	1.0	1.2	µH
C_{OUT}	Output capacitance	V_{OUT} < 1.2V		44		µF
C_{OUT}	Output capacitance	1.2V ≤ V_{OUT} < 1.8V		22		µF
C_{OUT}	Output capacitance	V_{OUT} ≥ 1.8V		22		µF
I_{PG}	Power-Good input current capability		0		1	mA
T_J	Operating junction temperature	Operating junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS62A03x	UNIT
		DRL (SOT-563)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 2.5V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{EN} = High, V_{FB} = 610mV		28		μA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = Low; T_J = –40°C to 85°C		0.15	2	μA
UVLO						
$V_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising	2.3	2.4	2.5	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	2.2	2.3	2.4	V
ENABLE						
$V_{EN(R)}$	EN high-level input voltage	EN rising, enable switching			0.8	V
$V_{EN(F)}$	EN low-level input voltage	EN falling, disable switching	0.4			V
$V_{EN(LKG)}$	EN Input leakage current	V_{EN} = 5V			100	nA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	T_J = 0°C to 125°C, PWM mode	594	600	606	mV
V_{FB}	FB voltage	PWM mode	591	600	609	mV
	Load dependent output voltage drop (load regulation)	PWM mode		0.15		%/A
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.6V			100	nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FPWM operation	V_{IN} = 5V, V_{OUT} = 1.8V		2200		kHz
STARTUP						
	Internal fixed soft-start time	From EN = High to V_{FB} = 0.56V; V_{OUT} = 0.6V; T_J = 0°C to 85°C			1	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 5V		42		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{IN} = 5V		28		mΩ
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	TPS62A03; VIN = 3.3V	3.9	5		A
$I_{LS(OC)}$	Low-side valley current limit	TPS62A03; VIN = 3.3V		4.2		A
$IL_{PEAK(min)}$	Peak inductor current in PSM			0.5		A
POWER GOOD						
V_{PGTH}	Power Good threshold	PG high to low (falling edge), FB falling		93.5		%
V_{PGTH}	Power Good threshold	PG low to high (rising edge), FB rising		96		%
	PG delay falling			35		μs
	PG delay rising			10		μs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 5V			100	nA
	PG pin output low-level voltage	I_{PG} = 1mA			400	mV
OUTPUT DISCHARGE						
	Output discharge current on SW pin	V_{IN} = 3V, V_{OUT} = 2.0V		120		mA
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		165		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

6.6 Typical Characteristics

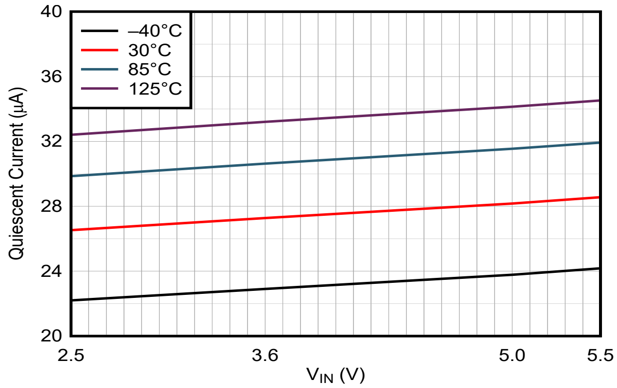


Figure 6-1. Quiescent Current vs Input Voltage

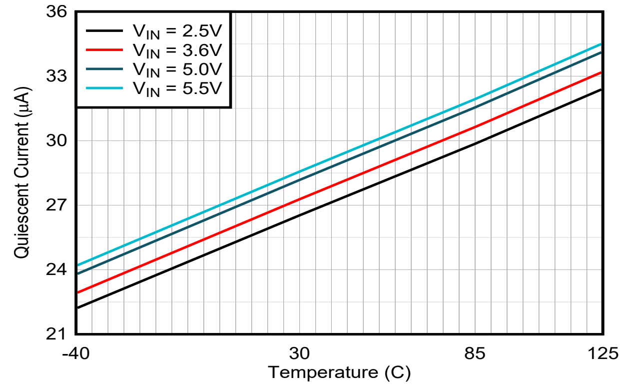


Figure 6-2. Quiescent Current vs Junction Temperature

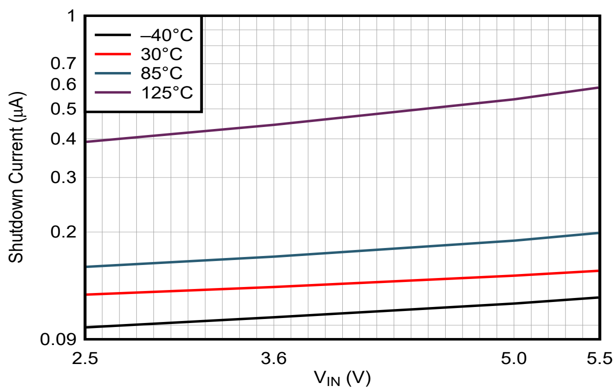


Figure 6-3. Shutdown Current vs Input Voltage

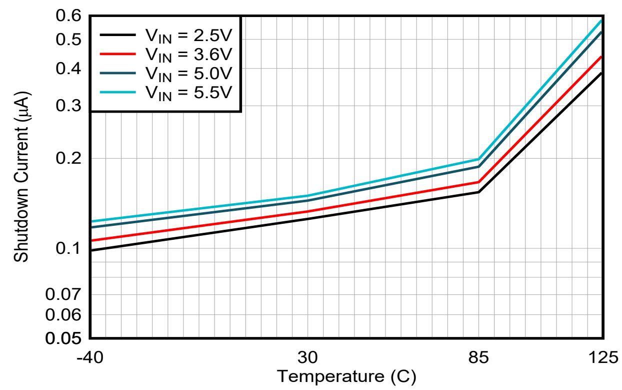


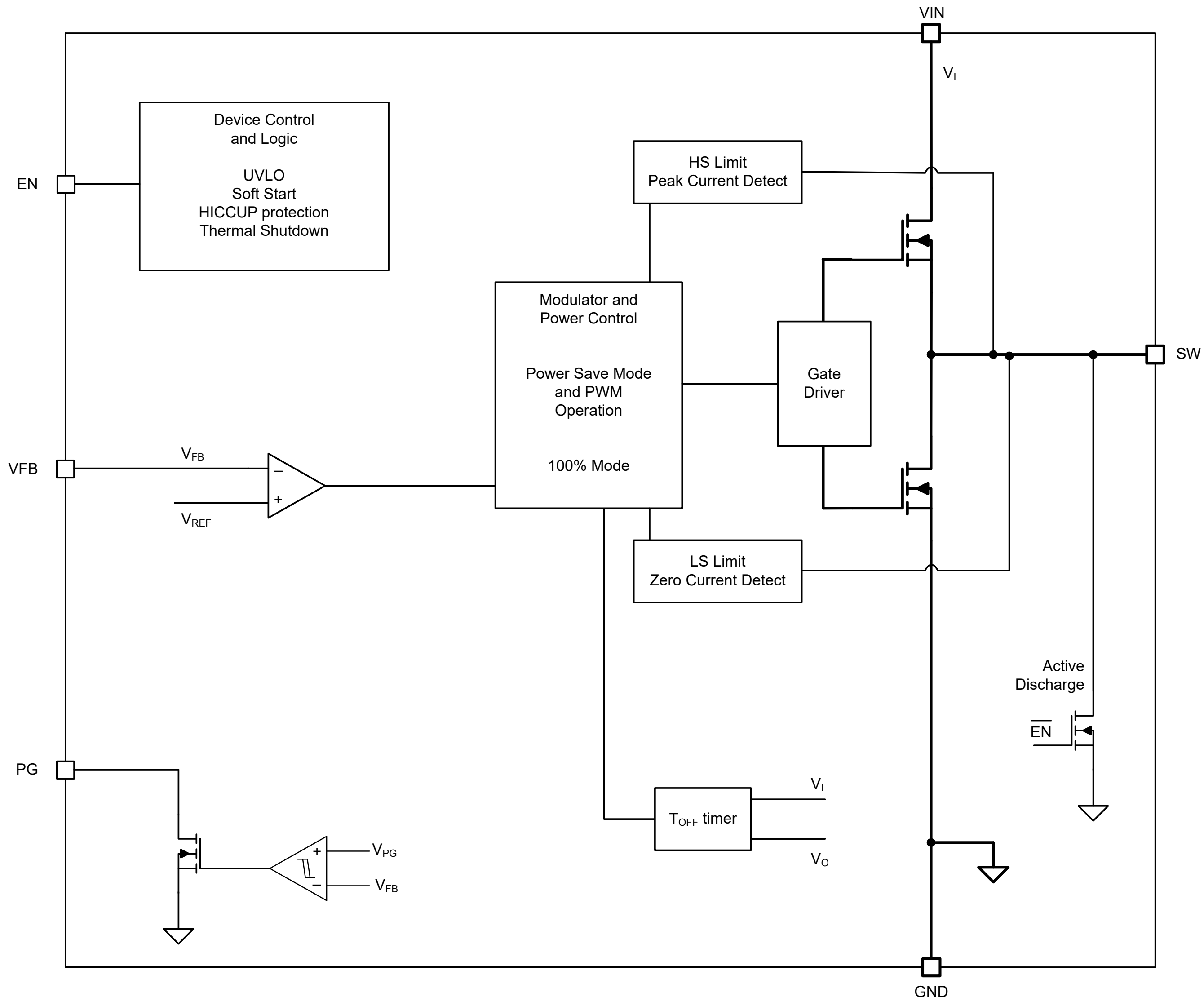
Figure 6-4. Shutdown Current vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS62A03x is a high-efficiency, synchronous, step-down converter. The device operates with an adaptive off time with a peak current control scheme. The device operates typically at 2.2MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

The TPS62A03 version of the device automatically enters power save mode to improve efficiency at light load when the inductor current becomes discontinuous. In power save mode, the converter reduces the switching frequency and minimizes current consumption. In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or adding a feedforward capacitor.

The TPS62A03A version of the device does not have the power saving functionality and preserves the switching frequency at all load conditions.

7.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High-side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.3 Soft Start

After enabling the device, internal soft-start circuitry ramps up the output voltage, which reaches the nominal output voltage during start-up time, avoiding excessive inrush current and creating a smooth voltage rise slope. Internal soft-start circuitry also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TPS62A03 is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.3.4 Switch Current Limit and Short-Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or an overload or shorted output circuit condition. If the inductor current reaches the threshold ILIM, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off time.

When this switch current limit is triggered 32 times, the device stops switching to protect the output. The device then automatically starts a new start-up after a typical delay time of 100μs has passed. This action is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears. HICCUP protection is also enabled during the start-up.

7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO}.

7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and not be left floating.

7.4.2 Power Good

The TPS62A03 has a built-in power-good (PG) feature to indicate whether the output voltage has reached the target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. VIN must remain present for the PG pin to stay low. If not used, the power-good can be tie to GND or left open. The PG indicator has a deglitch to avoid the signal indicating glitches or transient responses from the loop.

Table 7-1. Power-Good indicator Functional Table

<table>
<tr><th colspan="4">Logic Signals</th><th rowspan="2">PG Status</th></tr>
<tr><th>V_I</th><th>EN Pin</th><th>Thermal Shutdown</th><th>V_O</th></tr>
<tr><td rowspan="4">V_I > UVLO</td><td rowspan="3">HIGH</td><td rowspan="2">NO</td><td>V_O on target</td><td>High Impedance</td></tr>
<tr><td>V_O < target</td><td>LOW</td></tr>
<tr><td>YES</td><td>x</td><td>LOW</td></tr>
<tr><td>LOW</td><td>x</td><td>x</td><td>LOW</td></tr>
<tr><td>V_I < 1.8V</td><td>x</td><td>x</td><td>x</td><td>Undefined</td></tr>
</table>

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

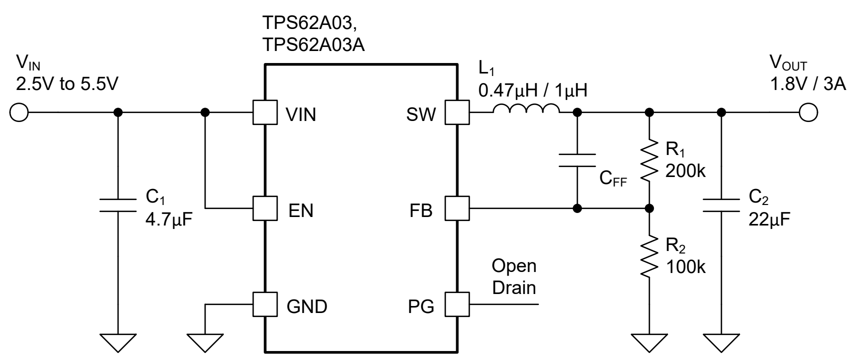


Figure 8-1. TPS62A03 Typical Application Circuit

*C_{FF} is optional

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters

Table 8-1. Design Parameters

Design Parameter	Example Value
Input voltage	2.5V to 5.5V
Output voltage	1.8V
Maximum output current	3.0A

Table 8-2 lists the components used for the example.

Table 8-2. List of Components

Reference	Description	Manufacturer (1)
C1	4.7µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	22µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
L1	1µH, Power Inductor, XGL3520-102MEC	Coilcraft
R1, R2	Chip resistor, 1%, size 0603	Std.
C_{FF}	Optional. If needed, then use up to 120pF, 10pF for 3.3V, 15pF for 1.8V, and 22pF for 1.2V VOUT. Make sure of a phase margin of > 45 degrees.	Std.

(1) See the *Third-Party Products Disclaimer*.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to Equation 2.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1\right) \tag{2}$$

R2 must not be higher than 100kΩ to provide acceptable noise sensitivity.

8.2.2.2 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, Table 8-3 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Check further combinations for each individual application.

Table 8-3. Matrix of Output Capacitor and Inductor Combinations for TPS62A03

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)	
		22	2 × 22
$0.6 \le V_{OUT} < 1.2$	1	+	++(3)
$1.2 \le V_{OUT} < 1.8$	1	++(3)	+
$1.8 \le V_{OUT}$	1	++(3)	+

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by +20% and –30%. A 0.47uH inductor can also be used with the same recommended output capacitors for the TPS62A03.
(2) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by +20% and –50%. In case a lower output ripple is desired, higher output capacitance can help reduce the ripple.
(3) This LC combination is the standard value and recommended for most applications.

8.2.2.3 Input and Output Capacitor Selection

The architecture of the TPS62A03 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep resistance up to high frequencies and to achieve narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. TI recommends a low-ESR multilayer ceramic capacitor for best filtering. For most applications, a 4.7µF input capacitor is sufficient; a larger value reduces input voltage ripple.

The TPS62A03 is designed to operate with an output capacitor of 22µF to 47µF, depending on the selected output voltage, as outlined in Section 8.2.2.2.

A feedforward capacitor reduces the output ripple in PSM. The capacitance has to be selected such that enough phase margin is available for stability. Smaller capacitance of the forward capacitor results in larger phase margin but also in larger ripple. Good starting points for capacitor values at a VIN of 5V are 10pF for VOUT = 3.3V, 15pF for VOUT = 1.8V, and 22pF for VOUT = 1.2V.

8.2.3 Application Curves

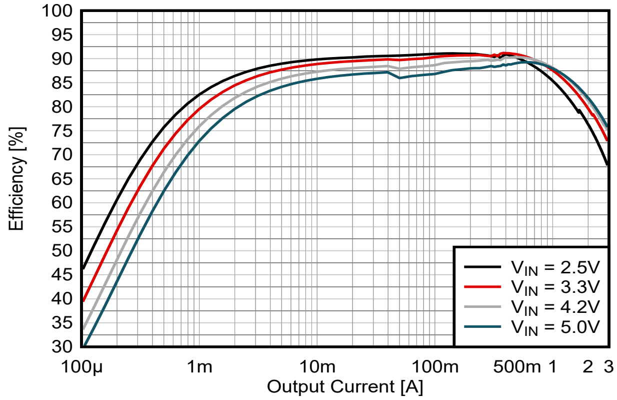


Figure 8-2. 0.6V Output Efficiency (TPS62A03)

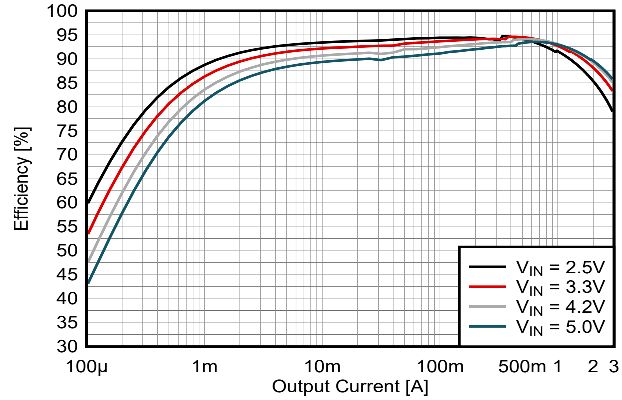


Figure 8-3. 1.2V Output Efficiency (TPS62A03)

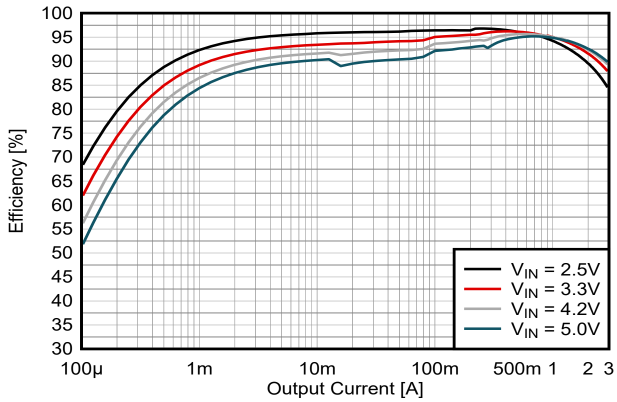


Figure 8-4. 1.8V Output Efficiency (TPS62A03)

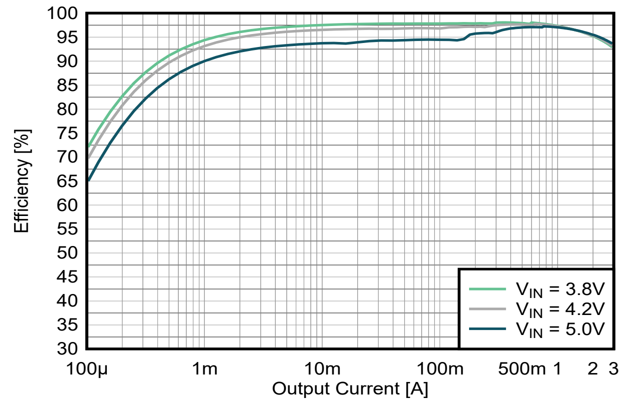


Figure 8-5. 3.3V Output Efficiency (TPS62A03)

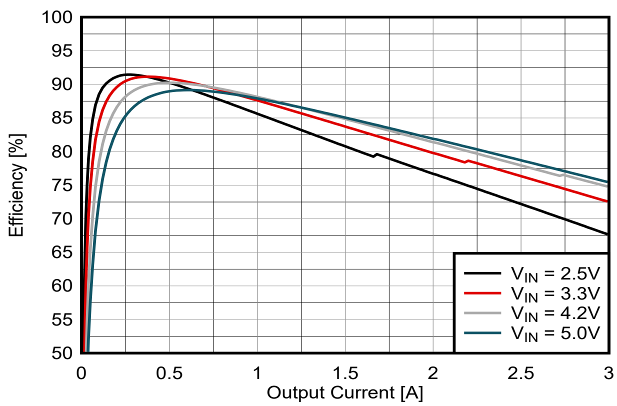


Figure 8-6. 0.6V Output Efficiency (TPS62A03A)

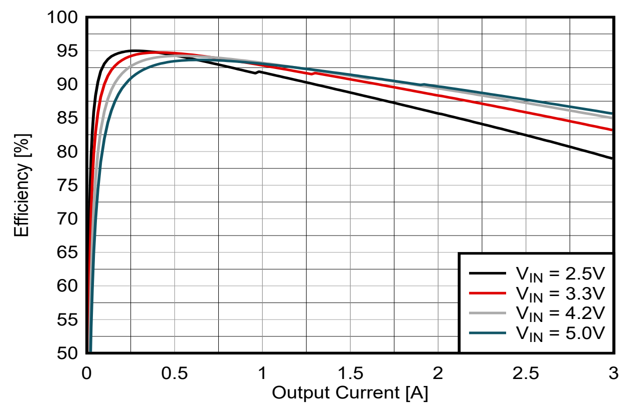


Figure 8-7. 1.2V Output Efficiency (TPS62A03A)

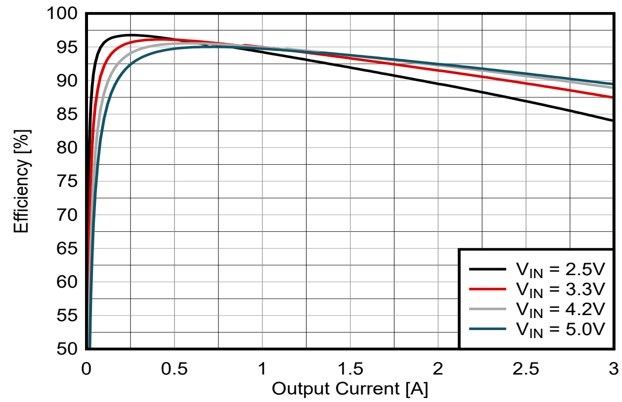


Figure 8-8. 1.8V Output Efficiency (TPS62A03A)

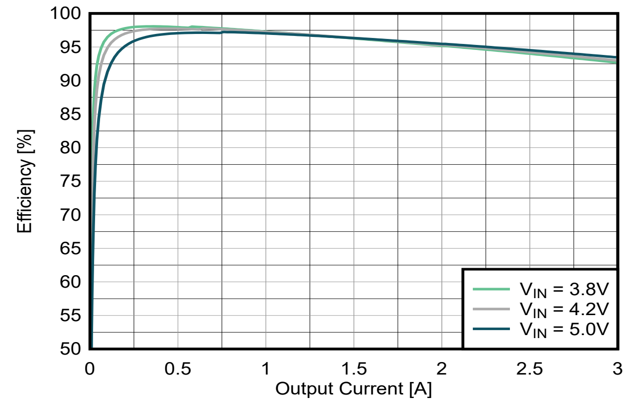


Figure 8-9. 3.3V Output Efficiency (TPS62A03A)

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5V to 5.5V. Make sure that the input power supply has a sufficient current rating for the application.

8.4 Layout

8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TPS62A0x device.

- Place the input and output capacitors and the inductor as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Take special care to avoid noise being induced. Keep these traces away from SW nodes.
- Use a common ground. Use GND layers for shielding.

See Figure 8-10 for the recommended PCB layout.

8.4.2 Layout Example

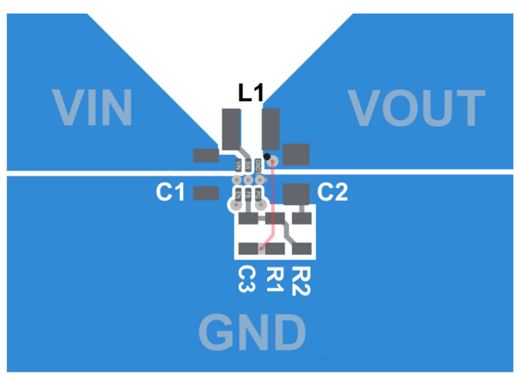


Figure 8-10. TPS62A0x PCB Layout Recommendation

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2024) to Revision A (October 2024)	Page
• Changed document status from Advance Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62A03ADRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	1PL
TPS62A03ADRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1PL
TPS62A03DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	1PK
TPS62A03DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1PK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

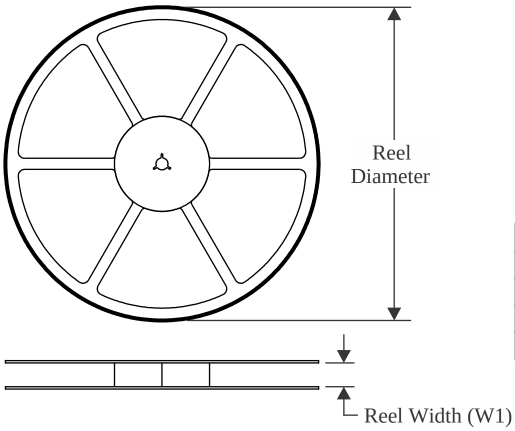
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

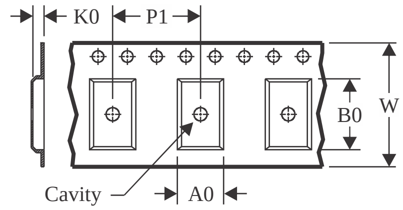
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

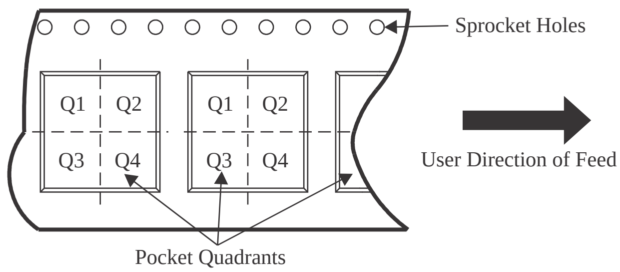


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

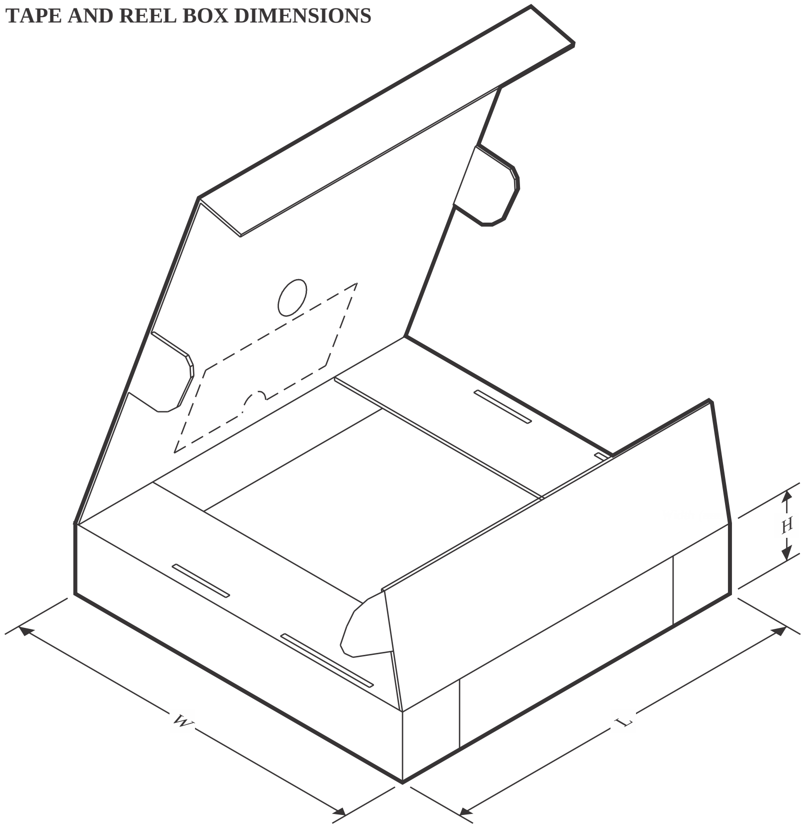
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

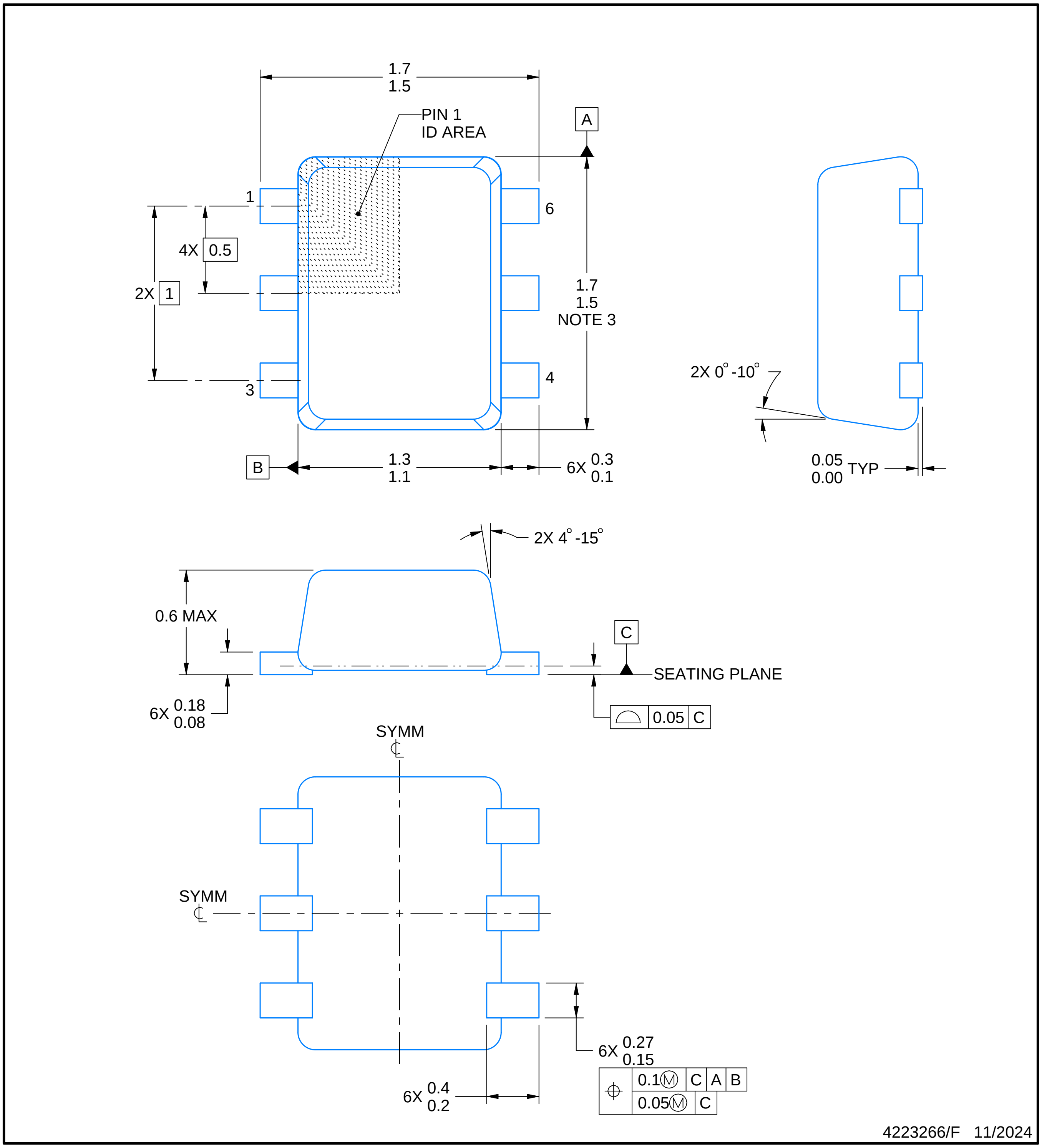
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62A03ADRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A03DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



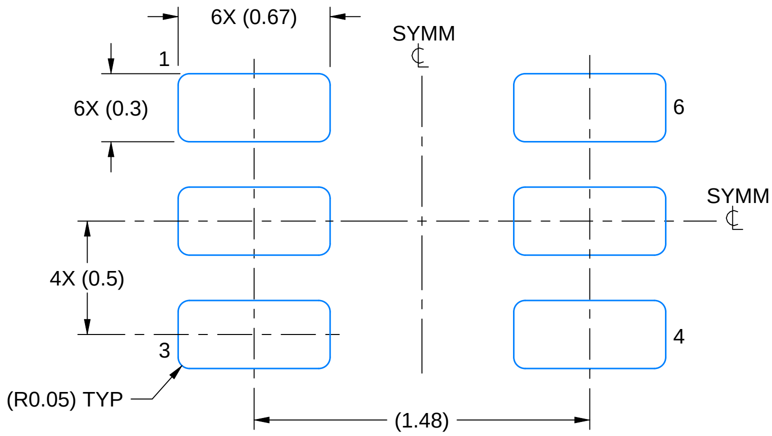
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62A03ADRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A03DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

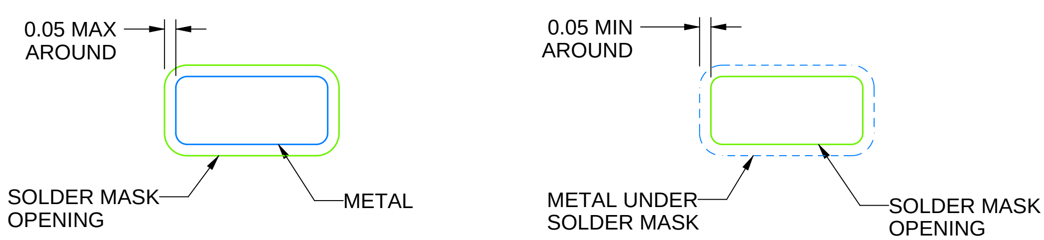


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDERMASK DETAILS

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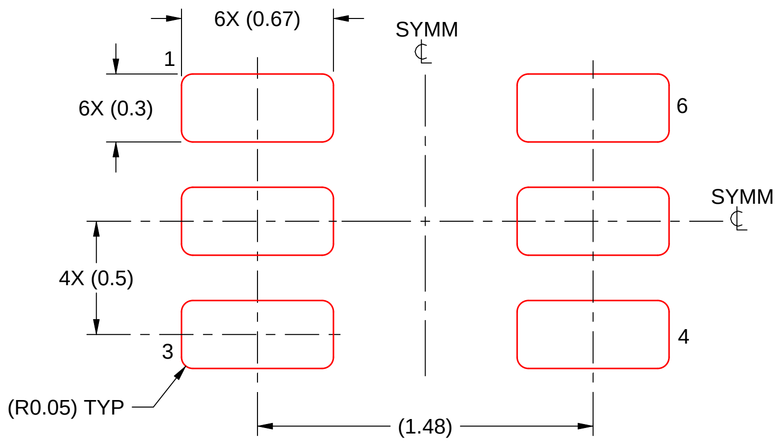
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.