TPS6286A06D 2.4V to 5.5V Input, 6A, Synchronous Step-Down Converter in a 2mm × 3mm QFN Package

1 Features

- 2.4V to 5.5V input voltage range
- 8mΩ and 8mΩ internal power MOSFETs
- 5.1µA operating quiescent current
- Multisource with other industry standard devices
- 1.2MHz switching frequency
- 100% duty cycle mode
- 0.7% output voltage accuracy
- Forced PWM or power save mode
- DCS-Control topology (constant on-time)
- Output voltage:
  - Adjustable from 0.6V to Vin (with external FB divider)
  - Fixed (by external resistor) from 0.4V to 1.6V
- Output voltage discharge
- Hiccup short-circuit protection
- Power-good indicator with internal pull-up
- Thermal shutdown
- Adjustable soft start
- –40°C to 125°C operating temperature range
- Also available as 8A and 10A versions without I^2C interface (TPS6286A08, TPS6286A10) and with I^2C interface (TPS6286B08 and TPS6286B10)

2 Applications

- WLAN/Wi-Fi access point
- IP network cameras
- Machine vision cameras
- Core supply for FPGAs, CPUs, ASICs, and DSPs

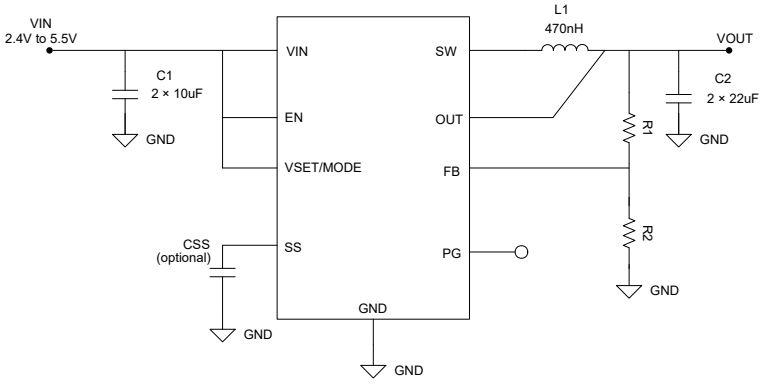
3 Description

The TPS6286A06D device is a high-frequency, synchronous, step-down converter which provides an efficient, flexible, and high power-density design. At medium to heavy loads, the converter operates in pulse width modulation (PWM) mode and automatically enters power save mode operation at light load to maintain high efficiency over the entire load current range. The device can also be forced in PWM mode operation to minimize output voltage ripple. Together with the DCS-Control architecture, excellent load transient performance and tight output voltage accuracy is achieved. The device features a Power-Good signal with internal pull-up resistor to VIN (for external pull up resistor option, use TPS6286A06) and an adjustable soft-start feature. The device is able to operate in 100% mode. For fault protection, the device incorporates a HICCUP short-circuit protection as well as a thermal shutdown.

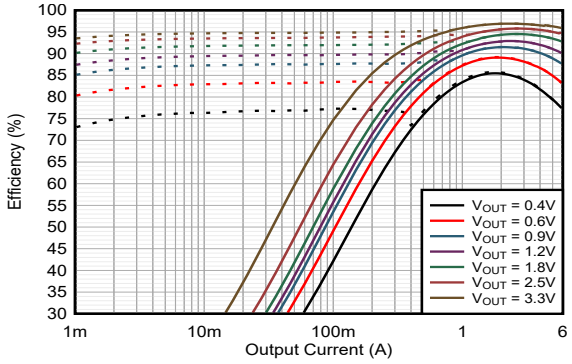
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS6286A06D	VBM (VQFN-HR, 13)	2mm × 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic - TPS6286A06D



Efficiency Curve vs Output Current, V_{IN} = 5V

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4 Pin Configuration and Functions

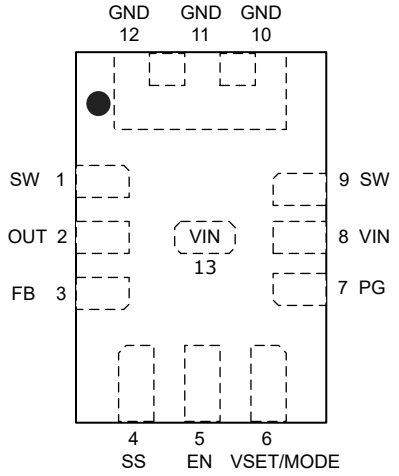


Figure 4-1. 13-Pin VBM VQFN-HR Package for FB Version (Top View)

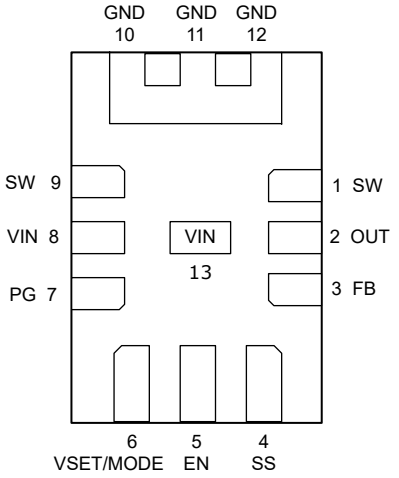


Figure 4-2. 13-Pin VBM VQFN-HR Package for FB Version (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN	5	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low or leaving floating disables the device.
FB	3	I	Voltage feedback input. Connect the output voltage resistor divider to this pin. When using a fixed output voltage, connect directly to OUT.
GND	10,11,12	GND	Power ground pin
OUT	2	I	Output voltage sense pin. This pin must be directly connected to the output capacitor.
PG	7	O	Power-good open-drain output pin. This output pin is internally pulled up to VIN with a 500kΩ resistor. If unused, leave this pin floating. This pin is pulled to GND when the device is in shutdown.
SS	4	I	Soft-start pin. An external capacitor can adjust the soft-start time. If unused, leave this pin floating to set a default SS time.
SW	1, 9	P	Switch pin of the power stage
VIN	8,13	P	Power supply input voltage pin
VSET/MODE	6	I	Connecting a resistor to GND selects one of the fixed output voltages. Tying the pin high or low or floating selects an adjustable output voltage. After the device has started up, the pin operates as a MODE input. Applying a high level selects forced PWM mode operation and a low level or floating selects power save mode operation.

(1) I = input, O = output, P = power, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin Voltage(2)	VIN, EN, OUT, FB, PG, VSET/MODE, SS	–0.3	6	V
	SW (DC)	–0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns)(3)	–2.5	10	
Sink current at PG	I_{SINK_PG}		1	mA
Junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage range	2.4		5.5	V
V_{OUT}	Output voltage range	0.4		V_{IN}	V
V_{IN_SR}	Falling transition time at VIN(1)			10	mV/µs
I_{OUT}	Output current			6	A
T_J	Junction temperature	–40		125	°C

(1) The falling slew rate of V_{IN} must be limited if V_{IN} goes below V_{UVLO}.

5.4 Thermal Information

THERMAL METRIC(1)		TPS6286A06D		UNIT
		VBM (JEDEC 51-7)	VBM (EVM)	
		13 PINS	13 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.2	43.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.3	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.6	n/a(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	6.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.6	10.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

(2) Not applicable to an EVM.

5.5 Electrical Characteristics

T_J = –40°C to 125°C, and V_{IN} = 2.4V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{Q_VIN}	Quiescent current	EN = High, no load, device not switching, T_J = 25℃		5.1	9	µA
I_{Q_OUT}	Operating quiescent current into OUT pin	EN = High, no load, device not switching, V_{OUT} = 1.8V, T_J = 25℃		18		µA
I_{SD}	Shutdown current	EN = Low, T_J = 25℃, EN has not been triggered once		0.24	0.75	µA
I_{SD}	Shutdown current	V_{IN}=5V, T_J = 25℃, EN = Low, after EN has been triggered once		6.5		µA
V_{UVLO}	Undervoltage lock out threshold	V_{IN} rising	2.2	2.3	2.4	V
		V_{IN} falling	2.1	2.2	2.3	V
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE						
V_{IH}	High-level input threshold voltage at EN and VSET/MODE		0.9			V
V_{IL}	Low-level input threshold voltage at EN and VSET/MODE				0.4	V
$R_{Pull\_down\_VSET\_MODE}$	Pull-down resistor on VSET/MODE pin	T_J=25 ℃ , V_{IN}= 5V, $V_{VSET/MODE}$= 5V, After R2D read is completed.		3.3		MΩ
$I_{EN,LKG}$	Input leakage current into EN pin	T_J = 25℃, V_{IN}= 5.0V, V_{EN}= 0.4V		0.01	0.1	µA
$R_{Pull\_down\_EN}$	Pull-down resistor on EN pin	T_J=25 ℃ , V_{IN}= 5V, V_{EN}= 5V		2.25		MΩ
STARTUP, POWER GOOD						
t_{Delay}	Enable delay time	Time from EN high to device starts switching 249kΩ resistor connected between VSET/MODE and GND	420	840	1200	µs
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good (no external capacitor connected)	1	1.5	1.85	ms
$R_{Pull\_up\_PG}$	PG INTERNAL Pull Up Resistor to VIN	T_J=25 ℃		500		kΩ
V_{PG}	Power-good lower threshold	V_{OUT} referenced to V_{OUT} nominal	85	91	96	%
	Power-good upper threshold	V_{OUT} referenced to V_{OUT} nominal	103	111	120	%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1mA			0.36	V
Iss	SS pin source current			20		µA
$t_{PG,DLY}$	Power-good deglitch delay	Rising and falling edges		34		µs
OUTPUT						
V_{OUT}	Output voltage accuracy	Fixed voltage operation, FPWM, no load, T_J = 25°C	–0.7		0.7	%
V_{OUT}	Output voltage accuracy	Fixed voltage operation, FPWM, no load	–1		1	%
V_{FB}	Feedback voltage	Adjustable voltage operation	594	600	606	mV
$I_{FB,LKG}$	Input leakage into FB pin	Adjustable voltage operation, V_{FB} = 0.6V, T_J = 25℃		0.01	0.1	µA
R_{DIS}	Output discharge resistor at OUT pin			4.3		Ω
	Load regulation	V_{OUT} = 0.9V, FPWM		0.04		%/A
POWER SWITCH						

5.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, and V_{IN} = 2.4V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	High-side FET on-resistance			8		mΩ
	Low-side FET on-resistance			8		mΩ
I_{LIM}	High-side FET forward current limit		7.3	8	9	A
I_{LIM}	Low-side FET forward current limit			6.5		A
I_{LIM}	Low-side FET negative current limit			–3		A
f_{SW}	PWM switching frequency	I_{OUT} = 1A, V_{OUT} = 0.9V		1.2		MHz

6 Typical Characteristics

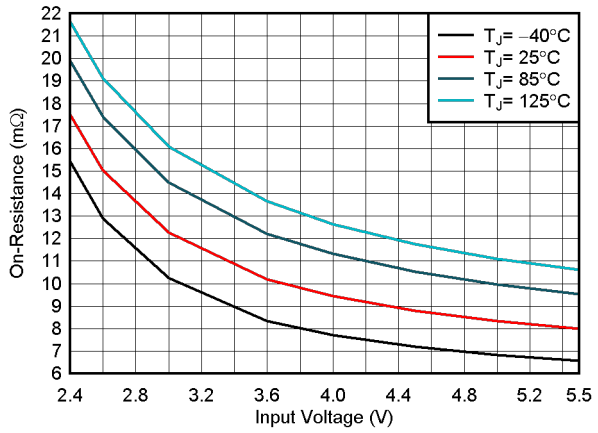


Figure 6-1. High-Side FET On-Resistance $R_{DS(on)}$

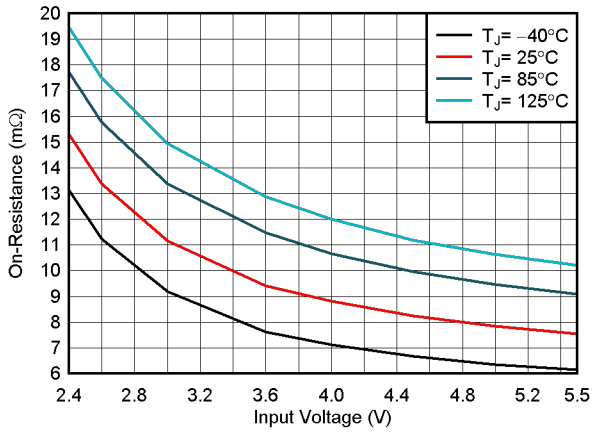


Figure 6-2. Low-Side FET On-Resistance $R_{DS(on)}$

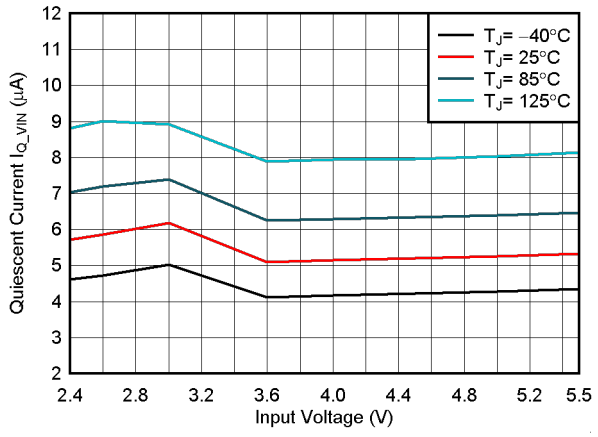


Figure 6-3. Quiescent Current into V_{IN} I_{Q_VIN}

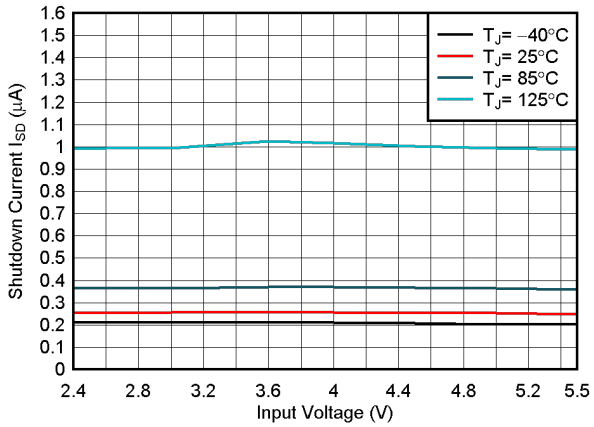


Figure 6-4. Shutdown Current I_{SD}

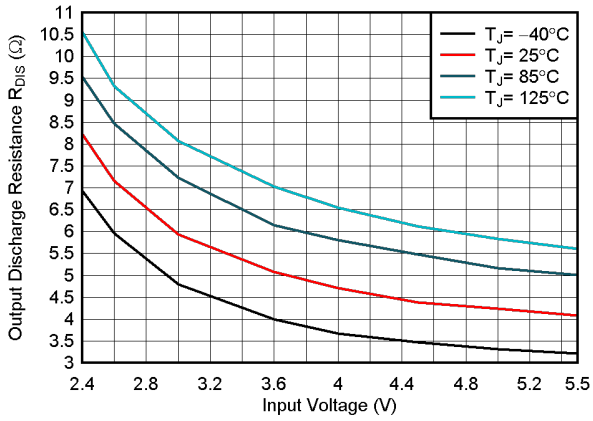


Figure 6-5. Output Discharge Resistance R_{DIS}

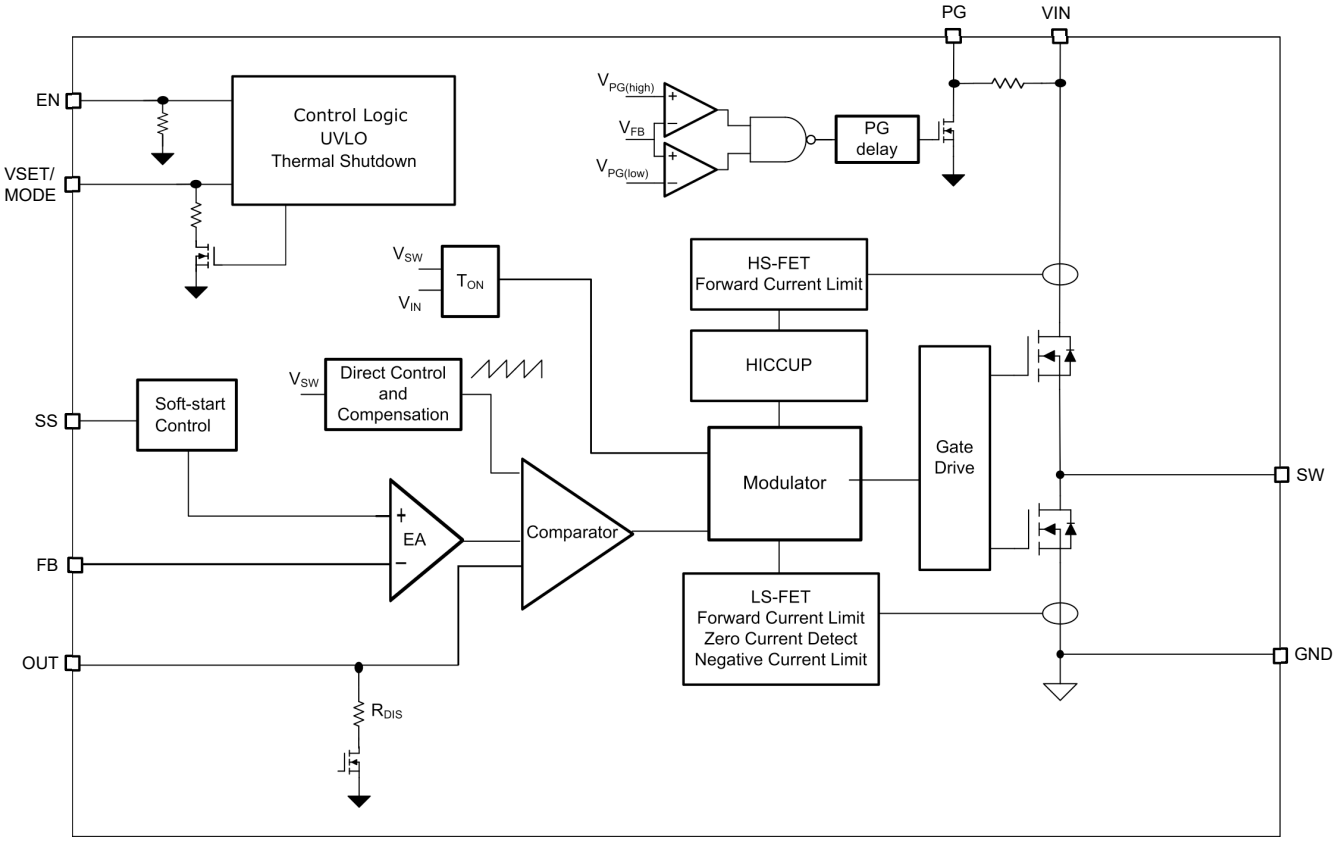
7 Detailed Description

7.1 Overview

The TPS6286A06D synchronous step-down converter uses the DCS-Control (Direct Control with seamless transition into power save mode) topology. This topology is an advanced regulation topology that combines the advantages of hysteretic and current-mode control schemes.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in power save mode at light load currents. In PWM mode, the converter operates with the 1.2MHz nominal switching frequency, having a controlled frequency variation over the input voltage range. Because DCS-Control supports both PWM and PFM (Pulse Frequency Modulation) within a single building block, the transition from PWM mode to power save mode is seamless and does not affect the output voltage. The TPS6286A06D device offers both excellent DC voltage and load transient regulation combined with very low output voltage ripple.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode (PFM)

As the load current decreases, the device enters power save mode or pulse frequency modulation (PFM) operation when MODE pin is tied to a low level or left floating. PFM occurs when the inductor current becomes discontinuous, which is when the inductor current reaches 0A during a switching cycle. Power save mode is based on a fixed on-time architecture, as shown in the following equation.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 833\text{ns} \quad (1)$$

In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

When V_{IN} decreases to typically 15% above V_{OUT}, the TP6286A06D does enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

7.3.2 Forced PWM Mode

After the device has powered up and ramped up VOUT, the VSET/MODE pin acts as a digital input. With a high level on the VSET/MODE pin, the device enters forced PWM (FPWM) mode and operates with a constant switching frequency over the entire load range, even at very light loads. This action reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications but lowers efficiency at light loads.

7.3.3 Low Dropout Operation (100% Duty Cycle)

The device offers a low dropout operation by entering 100% duty cycle mode if the input voltage comes close to the target output voltage. In this mode, the high-side MOSFET switch is constantly turned on. This mode is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN,MIN} = V_{OUT} + \left(R_{DS(ON)} + R_L\right) I_{OUT,MAX} \quad (2)$$

where

- $V_{IN,MIN}$ is the minimum input voltage to maintain an output voltage.
- $I_{OUT,MAX}$ is the maximum output current.
- $R_{DS(on)}$ is the high-side FET ON-resistance.
- R_L is the inductor ohmic resistance (DCR).

7.3.4 Soft Start

After enabling the device, there is an enable delay (t_{delay}) before the device starts switching. After the enable delay, if the SS pin is left not connected, an internal soft start-up circuit controls the output voltage ramp up with a period of 1.5ms (t_{Ramp}) for TPS6286A06D. Leaving the SS pin disconnected provides the fastest start-up ramp. Soft start avoids excessive inrush current and creates a smooth output voltage ramp up while also preventing excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. An external soft-start capacitor connected from SS to GND is charged by an internal 20µA current source during soft start until reaching the reference voltage of 0.9V. The capacitance required to set a certain ramp-time (t_{RAMP}) therefore is:

$$C_{SS} = \frac{20\mu A \times t_{ramp}[ms]}{0.9V} \quad (3)$$

If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS pin to GND. Returning from those states causes a new start-up sequence.

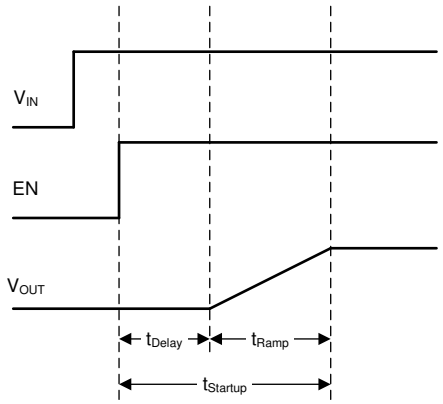


Figure 7-1. Start-Up Sequence

The device is able to start into a prebiased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.3.5 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, cycle by cycle, the high-side MOSFET is turned off and the low-side MOSFET is turned on, the inductor current ramps down to the low-side MOSFET current limit.

When the high-side MOSFET current limit is triggered 32 times, the device stops switching. The device then automatically restarts with soft start after a typical delay time of 128µs has passed. HICCUP short-circuit protection repeats this mode until the high load condition disappears.

7.3.6 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, undervoltage lockout (UVLO) is implemented when the input voltage is lower than V_{UVLO}. The device stops switching and the output voltage discharge is active. When the input voltage recovers, the device automatically returns to operation with a soft start.

7.3.7 Thermal Warning and Shutdown

When the junction temperature exceeds T_{JSD}, the device goes into thermal shutdown, stops switching, and activates the output voltage discharge. When the device temperature falls below the threshold by the hysteresis, the device returns to normal operation automatically with an internal soft start-up.

7.4 Device Functional Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic high. In shutdown mode (EN = low or floating), the internal power switches and the entire control circuitry are turned off. An internal switch smoothly discharges the output through the OUT pin in shutdown mode.

7.4.2 Output Discharge

The purpose of the output discharge function is to make sure of a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0V. The output discharge is active when the EN pin is pulled low, when the input voltage is below the UVLO threshold, or during thermal shutdown. The discharge is active down to an input voltage of 1.6V (typical).

7.4.3 Power Good (PG)

The device has an open-drain power-good (PG) output pin, which is specified to sink up to 1mA. The PG has a deglitch delay of 34µs.

The PG signal can be used for sequencing of multiple rails by connecting the PG signal to the EN pin of other converters. Leave the PG pin unconnected when not used.

Table 7-1. PG Function Table

DEVICE CONDITIONS		PG PIN
Enable	$0.9 \times V_{OUT\_NOM} \le V_{OUT} \le 1.1 \times V_{OUT\_NOM}$	VIN
	$V_{OUT} < 0.9 \times V_{OUT\_NOM}$ or $V_{OUT} > 1.1 \times V_{OUT\_NOM}$	Low
Shutdown	EN = low	Low
Thermal shutdown	$T_J > T_{JSD}$	Low
UVLO	$1.8V < V_{IN} < V_{UVLO}$	Low
Power supply removal	$V_{IN} < 1.8V$	Undefined

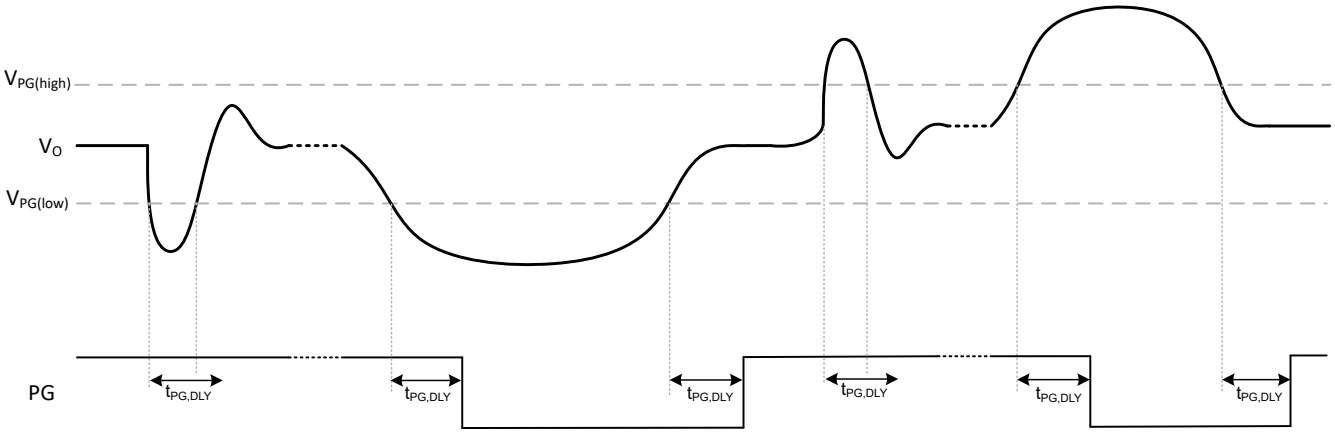


Figure 7-2. Power-Good Transient and Delay Behavior

After EN pin has been triggered once, the Power-Good pulldown is enabled along with the internal pullup resistor (500kΩ typical) connected to V_{IN} resulting in increased shutdown current.

7.4.4 Voltage Setting and Mode Selection (VSET/MODE)

The TPS6286A06D device is configurable as either an adjustable output voltage or a fixed output voltage, depending on the needs of each individual application. This feature simplifies the logistics during mass production, as one part number offers several fixed output voltage options as well as an adjustable output voltage option.

If an external resitor to ground is connected to the VSET/MODE pin, the device configuration is set by the value of this external resistor through an internal R2D (resistor to digital) converter during the enable delay (t_{Delay}) time-interval. If the VSET/MODE pin left unconnected, connected to ground or connected to VIN, the output voltage is adjustable through a resistive divider on the FB pin. Table 7-2 shows the options. The R2D read out configures the positive input to the error amplifier (EA) to be either the VFB voltage (0.6V typical) or the selected output voltage.

Table 7-2. Voltage Selection Table

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/MODE PIN, 200ppm/°C OR BETTER	FIXED OR ADJUSTABLE OUTPUT VOLTAGE
249kΩ, logic high or floating	Adjustable (through a resistive divider on the FB pin)
205kΩ	1.60V
162kΩ	1.50V
133kΩ	1.35V
105kΩ	1.20V
86.6kΩ	Reserved
68.1kΩ	1.00V
56.2kΩ	0.90V
44.2kΩ	0.85V
36.5kΩ	0.80V

Table 7-2. Voltage Selection Table (continued)

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/MODE PIN, 200ppm/°C OR BETTER	FIXED OR ADJUSTABLE OUTPUT VOLTAGE
28.7kΩ	0.70V
23.7kΩ	0.60V
18.7kΩ	0.50V
15.4kΩ	0.45V
12.1kΩ	0.40V
10kΩ or logic low	Adjustable (through a resistive divider on the FB pin)

The R2D converter has an internal current source that applies current through the external resistor and an internal ADC that reads back the resulting voltage level. Depending on the level, the output voltage is set. After this R2D conversion is finished, the current source is turned off to avoid current flowing through the external resistor. Make sure that the additional leakage current path is less than 20nA and the capacitance is less than 30pF from this pin to GND during R2D conversion. Otherwise, a false value is set. For more details, refer to *Benefits of a Resistor-to-Digital Converter in Ultra-Low Power Supplies* white paper.

When the device is set as a fixed output voltage converter, then FB pin must be connected to the output directly. Refer to Figure 7-3.

After the start-up period ($t_{Startup}$), a different operation mode can be selected. When VSET/MODE is pulled high, the device operates in forced PWM mode. When VSET/MODE is pulled low or left floating, the device operates in Power Save mode.

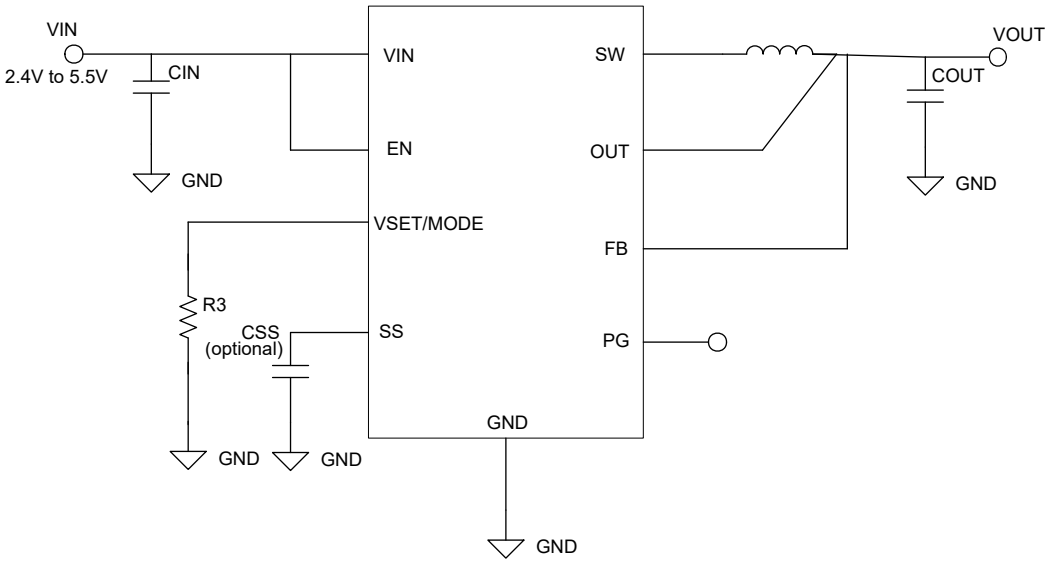


Figure 7-3. TPS6286A06D Typical Application - Fixed Output Voltage

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

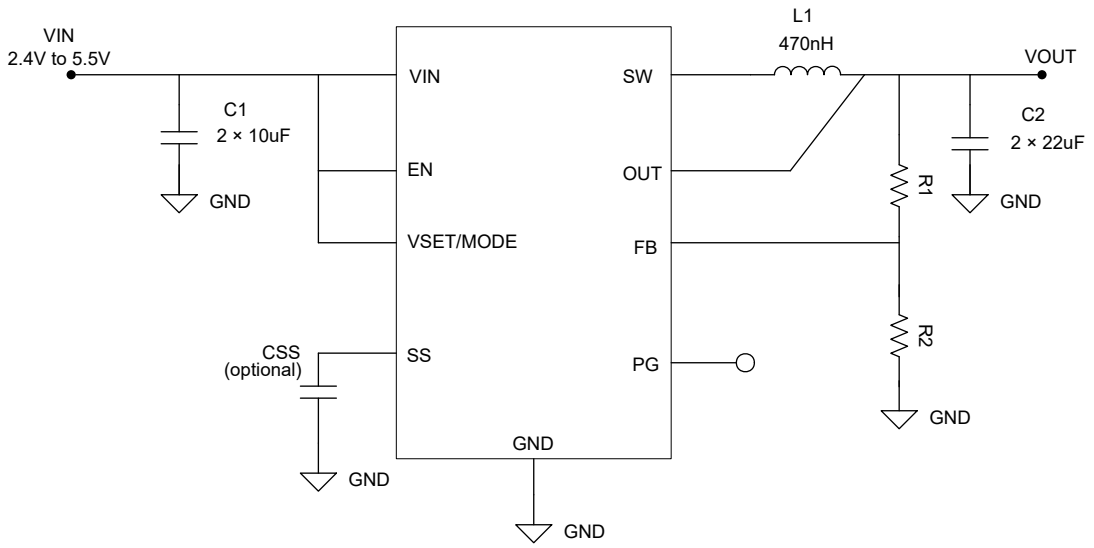


Figure 8-1. Typical Application Circuit- TPS6286A06D

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4V to 5.5V
Output voltage	1.2V
Maximum output current	6A

Table 8-2 lists the components used for the example.

Table 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	CAP, CERM, 10uF, 10V, +/– 10%, X7R, 0805, GCM21BR71A106KE22L	MURATA
C2	CAP, CERM, 22uF, 10V, +/– 20%, X7R, 0805, GRM21BZ71A226ME15L	MURATA
L1	470 nH Shielded Molded Inductor 15.7A 3.7mOhm, XGL5020-471MEC	Coilcraft
CSS	Open	Any
R1	100kΩ, chip resistor, 1/16 W, 1%, size 0402	Std
R2	100kΩ, chip resistor, 1/16 W, 1%, size 0402	Std

(1) See the Third-party Products disclaimer.

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS6286A06D device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting the Output Voltage

With the VSET/MODE pin set high or low, an adjustable output voltage is set by an external resistor divider according to Equation 4:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R_2 \times \left(\frac{V_{OUT}}{0.6V} - 1\right) \quad (4)$$

To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100kΩ to have at least 6µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity but lower light-load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* technical brief.

When a fixed output voltage is selected, connect the FB pin directly to the output. R1 and R2 are not needed, as V_{OUT} is set through a resistor on the VSET/MODE pin. Select the recommended resistor value from the list in Table 7-2.

8.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, Table 8-3 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab testing. Further combinations must be checked for each individual application.

Table 8-3. Matrix of Output Capacitor and Inductor Combinations for TPS6286A06D

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)		
	2 × 22 or 47	3 × 22	150
0.47	+(1)	+(4)	+

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary from 30µF up to 200µF.
(4) This LC combination is recommended for V_{OUT} > 1.6V

8.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value, then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, the following equations are given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (5)$$

$$\Delta I_L = V_{OUT}\left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}\right) \quad (6)$$

where

- $I_{OUT,MAX}$ is the maximum output current
- ΔI_L is the inductor current ripple
- f_{SW} is the switching frequency
- L is the inductor value

TI recommends to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. Table 8-4 lists recommended inductors.

Table 8-4. List of Recommended Inductors

INDUCTANCE [µH](1)	CURRENT RATING [A]	DIMENSIONS [L × W × H mm]	DC RESISTANCE [mΩ]	PART NUMBER
0.47	15.7	5.48 × 5.28 × 2	3.7	Coilcraft, XGL5020-471ME
0.47	17.1	4.3 × 4.3 × 3	3.9	Wuerth Elektronik, 744393240047
0.47	13.4	4 × 4 × 2	4.2	Coilcraft, XGL4020-471ME
0.47	12.7	4.1 × 4.1 × 2	7	Wuerth Elektronik, 744383560047HT

(1) See the Third-party Products disclaimer.

8.2.2.5 Capacitor Selection

The input capacitor is the low-impedance energy source for the converters, which helps to provide stable operation. TI recommends a low-ESR multilayer ceramic capacitor for the best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, 10µF of *effective* [1] capacitance is sufficient, however, a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep the low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. For operations up to 6A output current, the recommended typical output capacitor value is 30µF of *effective* capacitance. Values over 200µF can degrade the loop stability of the converter.

[1] The effective capacitance is the capacitance after tolerance, temperature, and DC bias effects have been considered.

8.2.3 Application Curves

V_{IN} = 5.0V, V_{OUT} = 1.2V, T_A = 25°C, BOM = Table 8-2, unless otherwise noted. Solid lines show the FPWM mode and dashed lines show PFM.

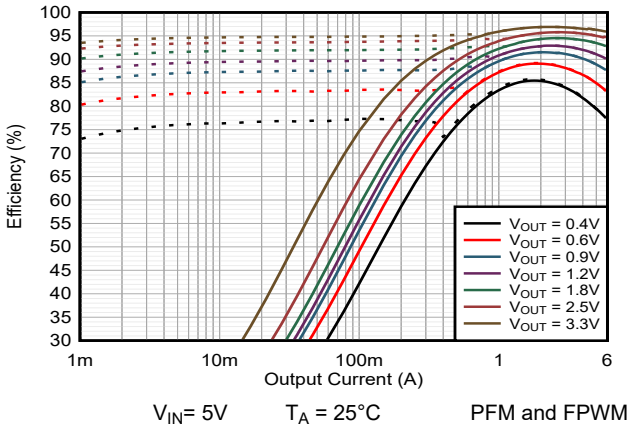


Figure 8-2. Efficiency vs Output Current

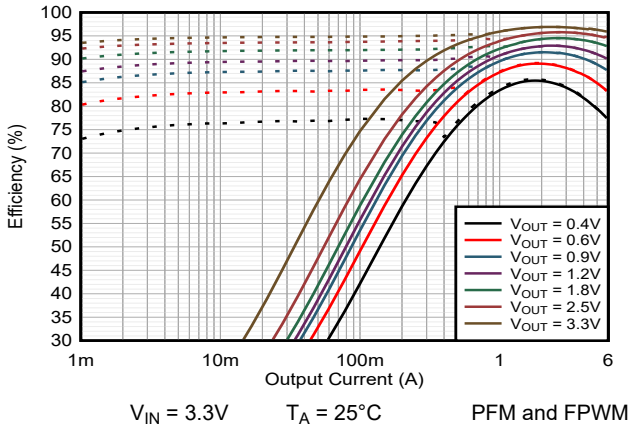


Figure 8-3. Efficiency vs Output Current

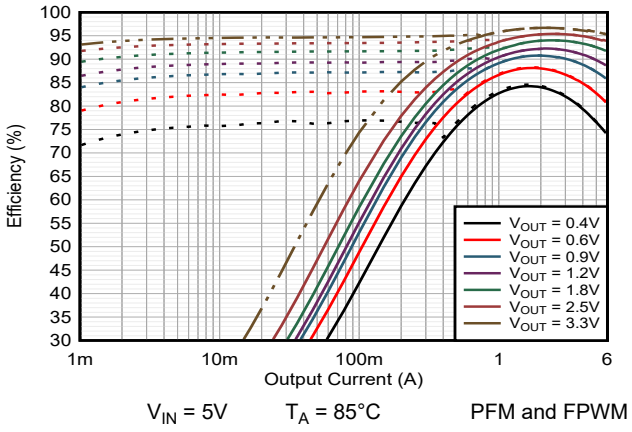


Figure 8-4. Efficiency vs Output Current

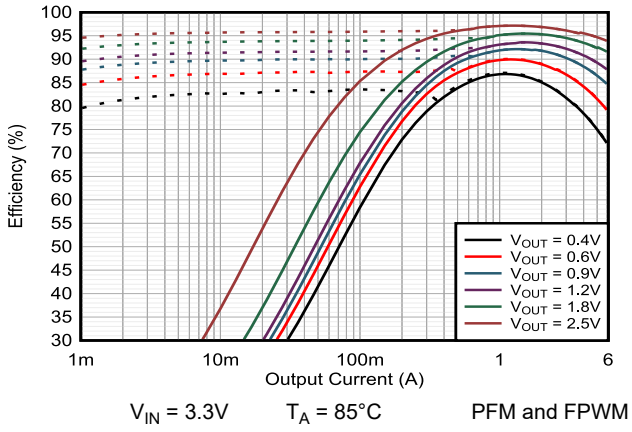


Figure 8-5. Efficiency vsOutput Current

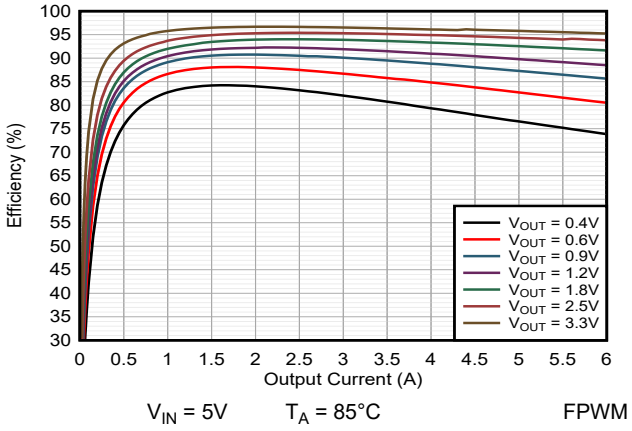


Figure 8-6. Efficiency vs Output Current

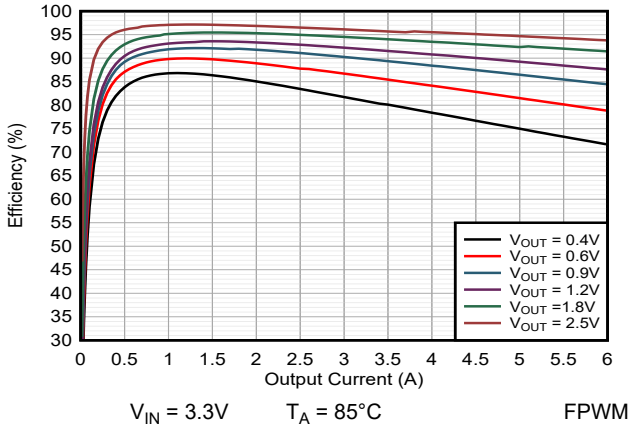
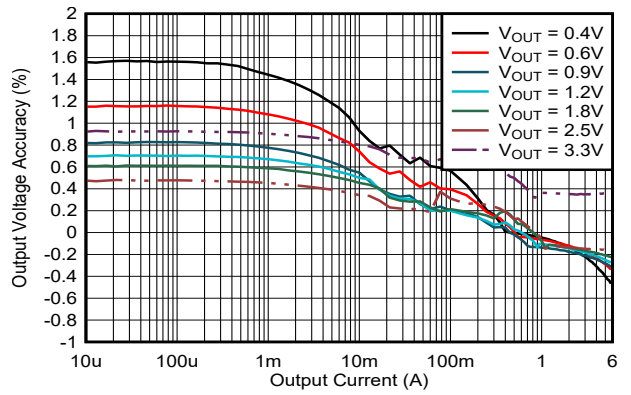
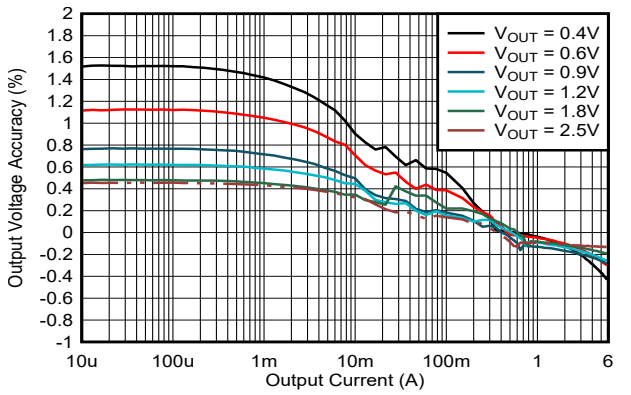


Figure 8-7. Efficiency vs Output Current



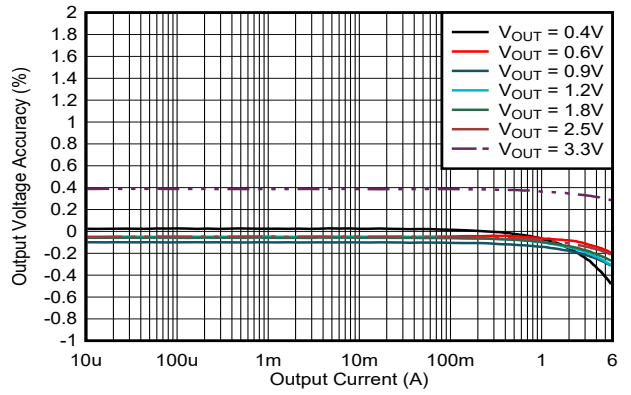
V_{IN} = 5V T_A = 25°C PFM

Figure 8-8. Load Regulation



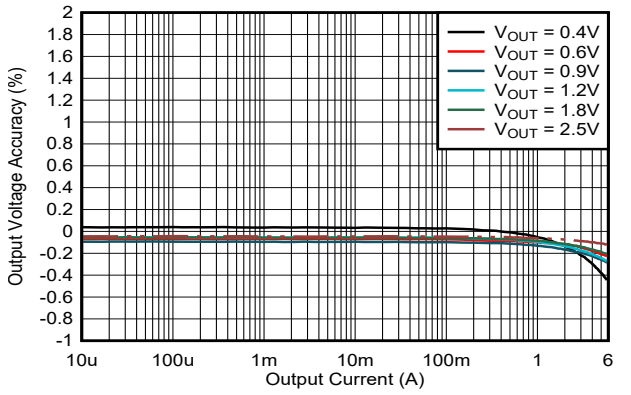
V_{IN} = 3.3V T_A = 25°C PFM

Figure 8-9. Load Regulation



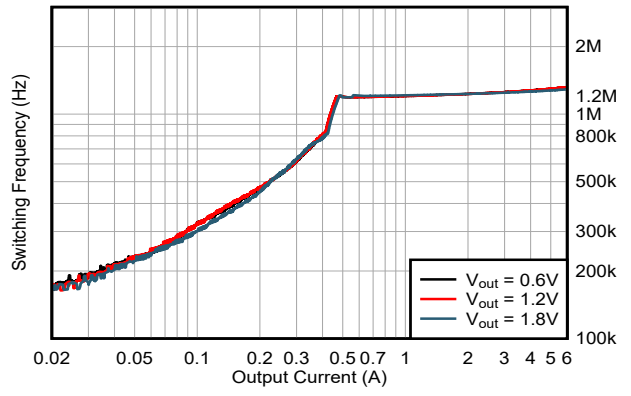
V_{IN} = 5V T_A = 25°C FPWM

Figure 8-10. Load Regulation



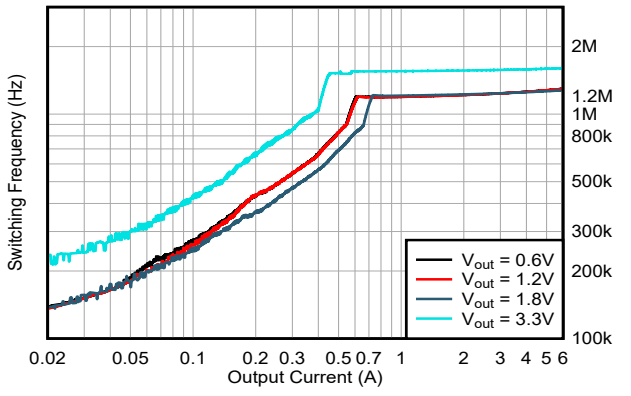
V_{IN} = 3.3V T_A = 25°C FPWM

Figure 8-11. Load Regulation



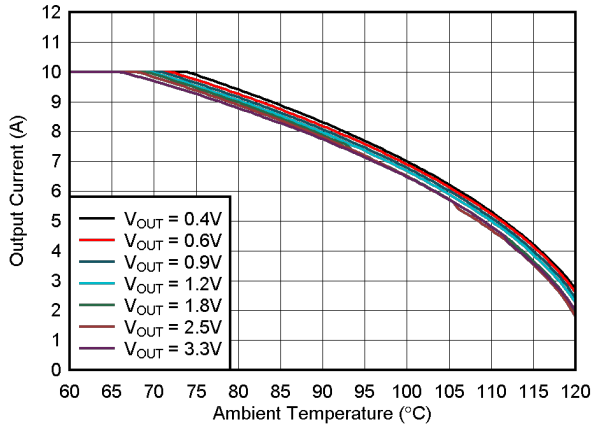
V_{IN} = 3.3V T_A = 25°C PFM

Figure 8-12. Switching Frequency



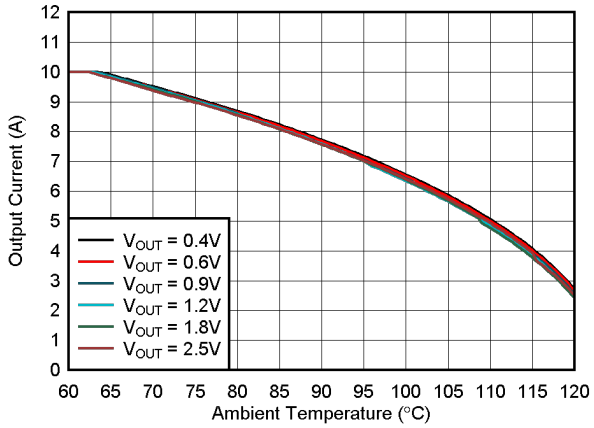
V_{IN} = 5.0V T_A = 25°C PFM

Figure 8-13. Switching Frequency



V_{IN} = 5.0V $R_{\theta JA}$ = 43.2°C/W T_{JMAX}= 125°C

Figure 8-14. Safe Operating Area



V_{IN} = 3.3V $R_{\theta JA}$ = 43.2°C/W T_{JMAX} = 125°C

Figure 8-15. Safe Operating Area

V_{IN} = 2.4V to 5.5V to 2.4V in 1V/us V_{OUT} = 1.2V Load = 10mA

Figure 8-16. Line Regulation

V_{IN} = 2.4V to 5.5V to 2.4V in 1V/us V_{OUT} = 1.2V Load = 6A

Figure 8-17. Line Regulation

V_{IN} = 5.0V V_{OUT} = 1.2V BOM = 2 × 22uF PFM, No Load

Figure 8-18. PFM Operation

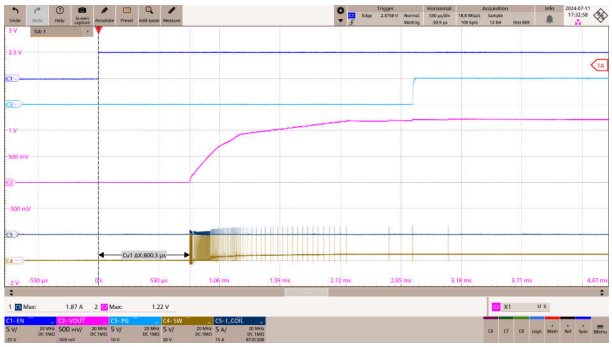
V_{IN} = 5.0V V_{OUT} = 1.2V BOM = 2 × 22uF FPWM, No Load

Figure 8-19. FPWM Operation

V_{IN} = 5.0V
V_{OUT} = 1.2V

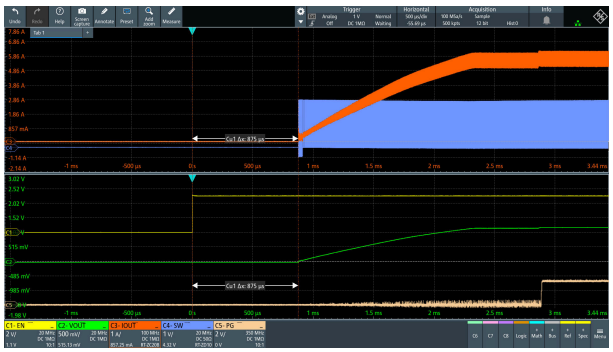
BOM = 2 × 22uF
FPWM, I_{OUT} = 6A

Figure 8-20. FPWM Operation



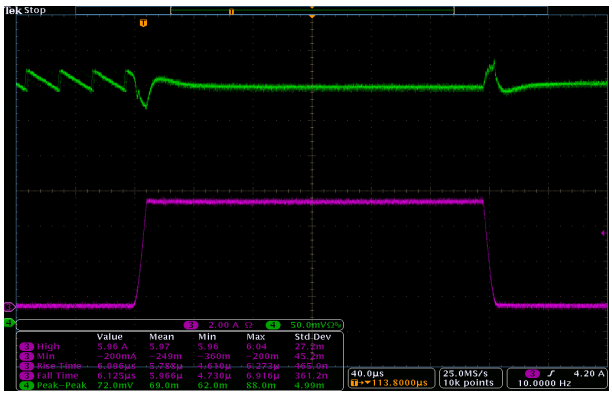
TPS6286A06D V_{OUT} = 1.2V No Load

Figure 8-21. Start-Up With No Load



TPS6286A06D V_{OUT} = 1.2V Load = 6A

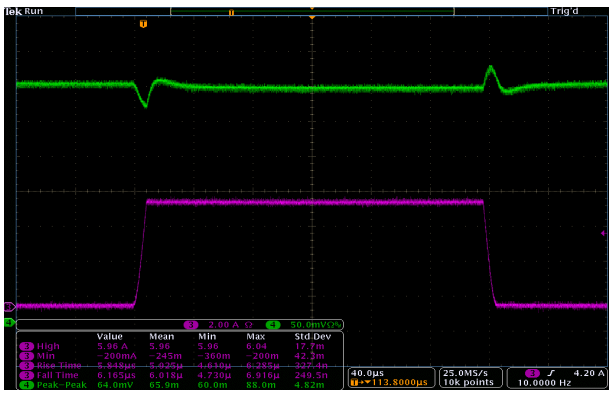
Figure 8-22. Start-Up into Full Load



V_{IN} = 5.0V
V_{OUT} = 1.2V

BOM = 2 × 22uF
I_{OUT} = 10mA to 6A

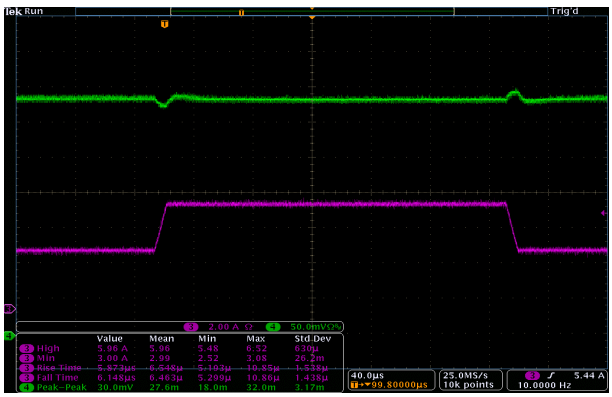
Figure 8-23. Load Transient in PFM Operation - TPS6286A06D



V_{IN} = 5.0V
V_{OUT} = 1.2V

BOM = 2 × 22uF
I_{OUT} = 10mA to 6A

Figure 8-24. Load Transient in FPWM Operation - TPS6286A06D



V_{IN} = 5.0V
V_{OUT} = 1.2V

BOM = 2 × 22uF
I_{OUT} = 3A to 6A

Figure 8-25. Load Transient in FPWM Operation - TPS6286A06D

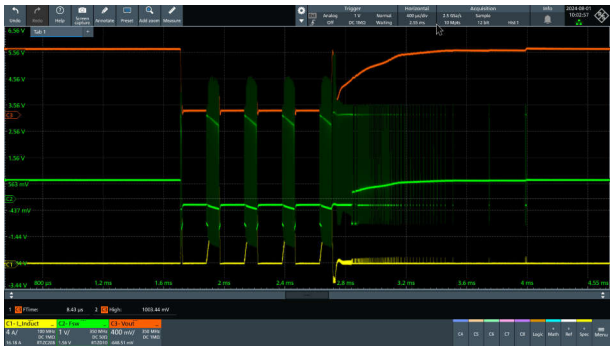


Figure 8-26. HICCUP Short-Circuit Protection

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4V to 5.5V. Make sure that the input power supply has a sufficient current rating for the application.

8.4 Layout

8.4.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. The PCB layout of the TPS6286A06D device requires careful attention to make sure of best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal for a detailed discussion of general best practices. The following are specific recommendations for the TPS6286A06D:

- Place the input capacitor as close as possible to the VIN and GND pins of the device. This placement is the most critical component placement. Route the input capacitor or capacitors directly to the VIN and GND pins.
- Place the output inductor close to the SW pins. Minimize the copper area at the switch node.
- Place the output capacitor ground close to the GND pin and route directly. Minimize the length of the connection from the inductor to the output capacitor. Connect the OUT pin directly to the output capacitor.
- Place the FB resistors R1 and R2 close to the FB pin and place R3 close to the VSET/MODE pin to minimize noise pickup.
- Make the connections from the input voltage of the system and the connection to the load as wide as possible to minimize voltage drops.
- Have a solid ground plane between GND and the input and output capacitor ground connections.

8.4.2 Layout Example

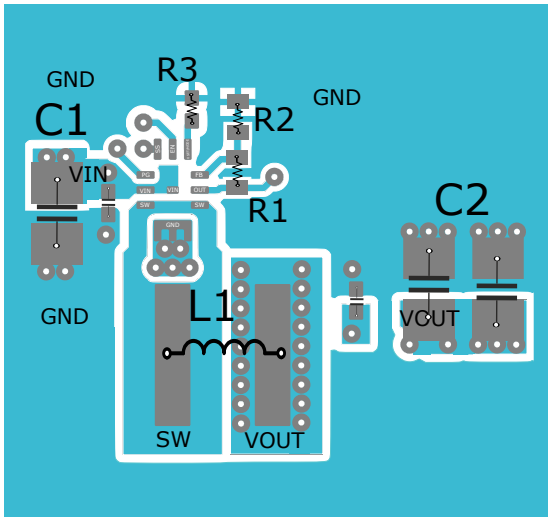


Figure 8-27. Layout Example TPS6286A06D

8.4.2.1 Thermal Considerations

After the layout recommendations for component placement and routing have been followed, the PCB design must focus on thermal performance. Thermal design is important and must be considered to remove the heat generated in the device during operation. The device junction temperature must stay below the maximum rated temperature of 125°C for correct operation.

Use wide traces and planes, especially to the GND and VIN pins, and use vias to internal planes to improve the power dissipation capability of the design. If the application allows, use airflow in the system to further improve cooling.

The *Thermal Information* table provides the thermal parameters of the device and the package based on the JEDEC standard 51-7. See the *Semiconductor and IC Package Thermal Metrics* application note for a detailed explanation of each parameter. In addition to the JEDEC standard, the thermal information table also contains the thermal parameters of the EVM. The EVM better reflects a real-world PCB design with thicker traces connecting to the device.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS6286A06D device with the WEBENCH® Power Designer.

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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal
- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* technical brief
- Texas Instruments, *Benefits of a Resistor-to-Digital Converter in Ultra-Low Power Supplies* white paper

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
May 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS6286A06DVBMR	Active	Production	VQFN-HR (VBM) | 13	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1W3

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

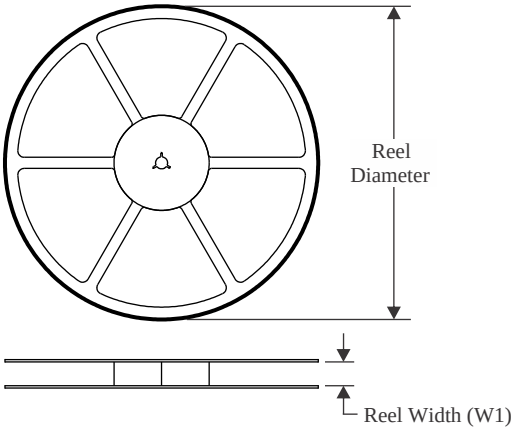
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

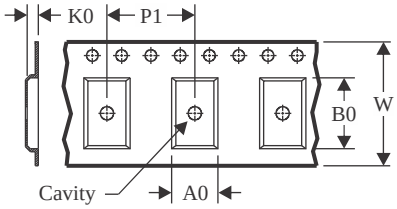
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

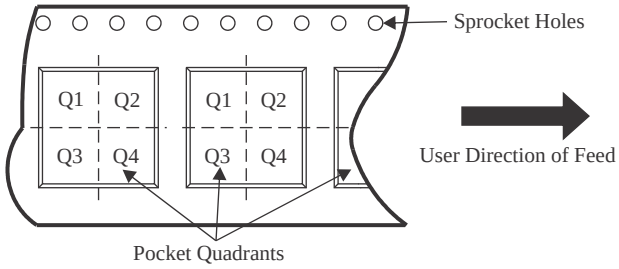


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

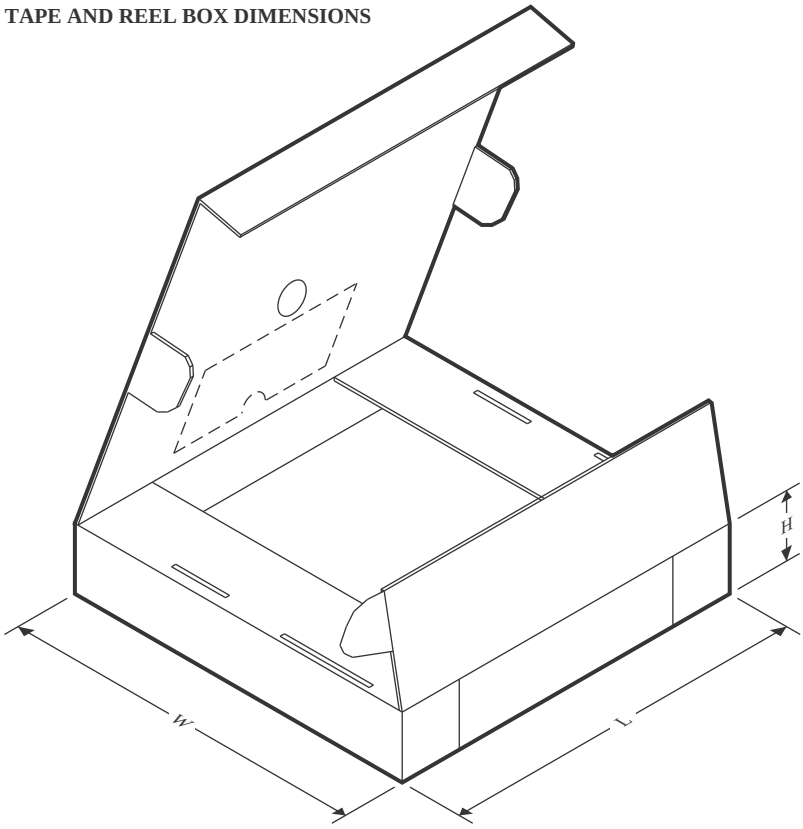
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6286A06DVBMR	VQFN-HR	VBM	13	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

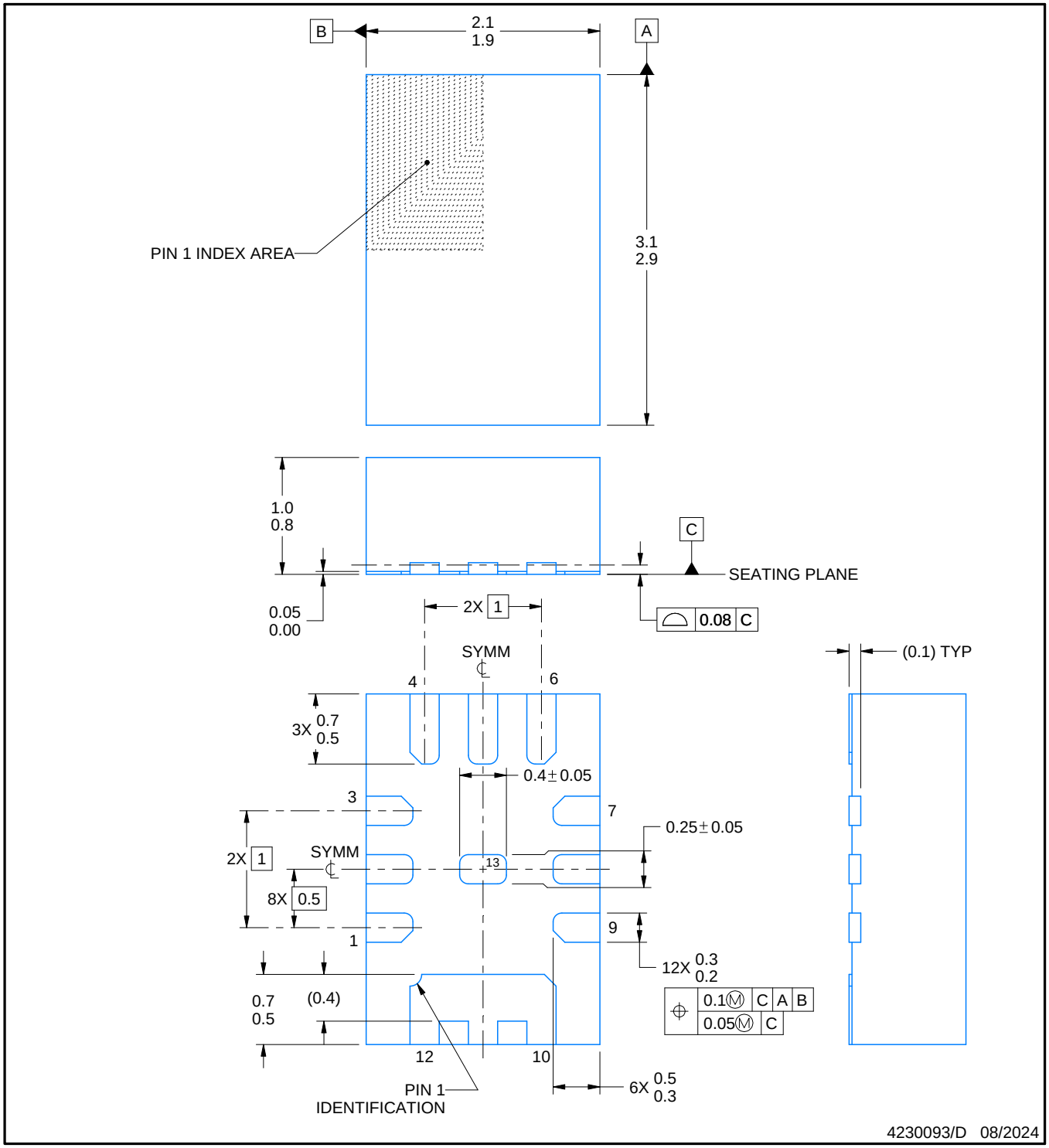
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6286A06DVBMR	VQFN-HR	VBM	13	3000	210.0	185.0	35.0

VBM0013A

PACKAGE OUTLINE

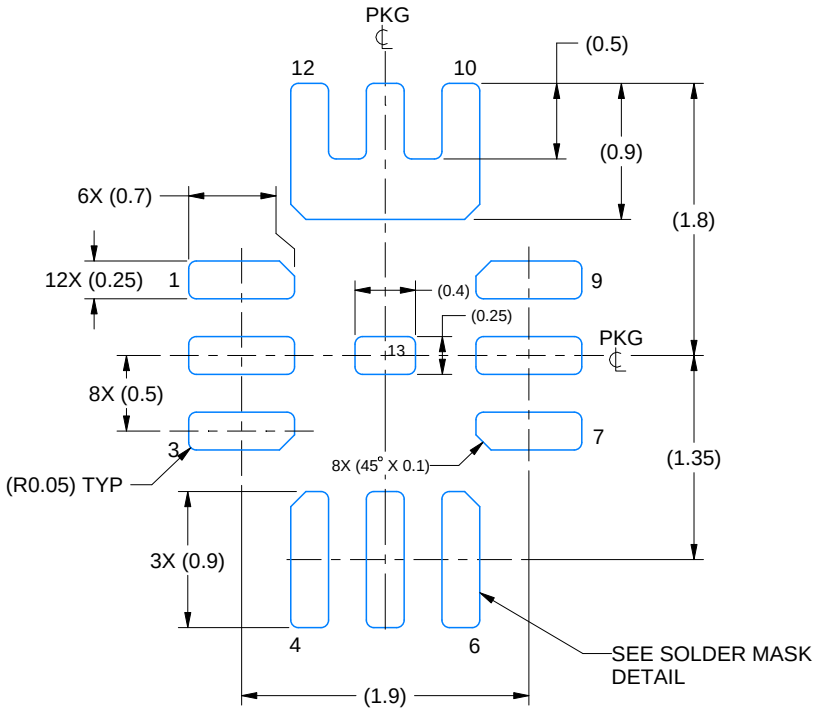
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

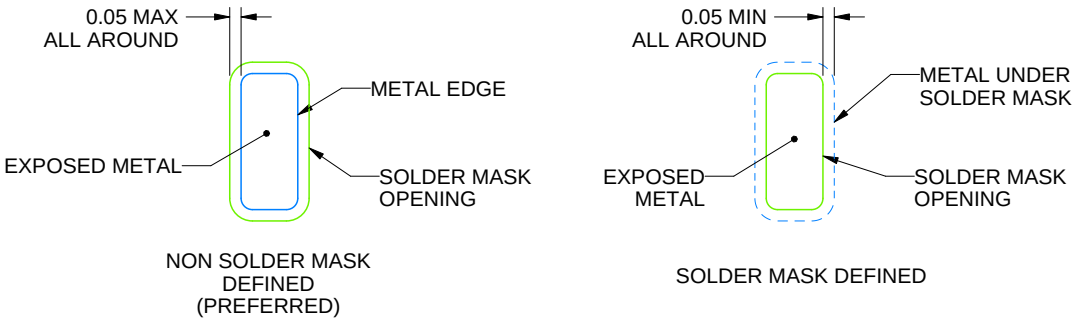


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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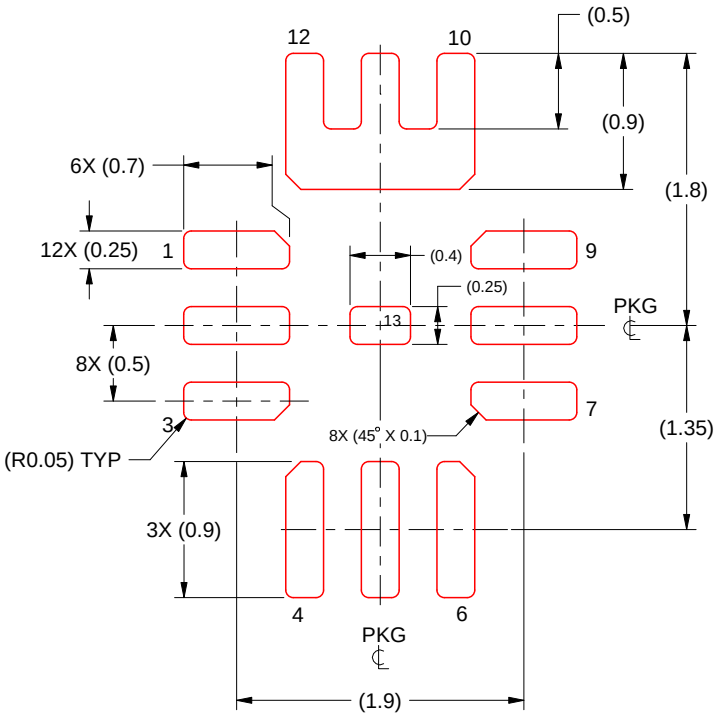
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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