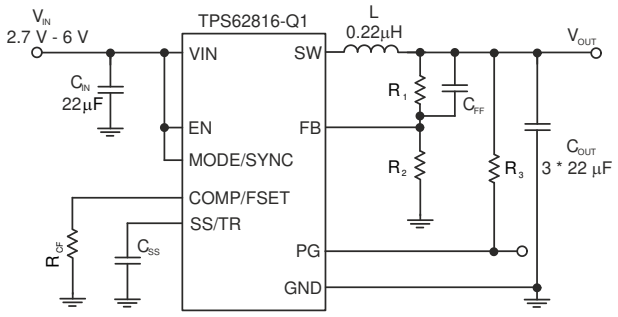
TPS62816-Q1 2.7-V to 6-V, 6-A Automotive Step-Down Converter in 3-mm × 2-mm QFN Package with Wettable Flanks

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Input voltage range: 2.7 V to 6 V
- Quiescent current: 26 µA typical
- Output voltage from 0.6 V to 5.5 V
- Output voltage accuracy ±1% (PWM operation)
- Adjustable soft start
- Forced PWM or PWM/PFM operation
- Adjustable switching frequency of 1.8 MHz to 4 MHz
- Precise ENABLE input allows
  - User-defined undervoltage lockout
  - Exact sequencing
- 100% duty cycle mode
- Active output discharge
- Spread spectrum clocking — optional
- Power-good output with window comparator
- Package with wettable flanks
- T_J = –40°C to 150°C

2 Applications

- ADAS sensor fusion
- Surround view ECU
- Digital cockpit
- External amplifier



Typical Application Schematic

3 Description

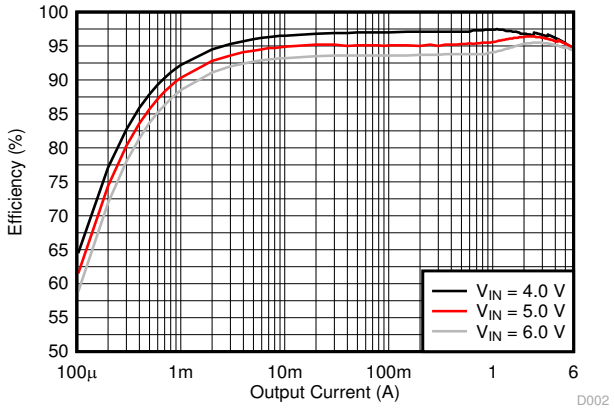
The TPS62816-Q1 is a pin-to-pin high efficiency, easy-to-use synchronous step-down DC/DC converter. It is based on a peak current mode control topology. It is designed for automotive applications such as infotainment and advanced driver assistance systems. Low resistive switches allow up to 6-A continuous output current. The switching frequency is externally adjustable from 1.8 MHz to 4 MHz and can also be synchronized to an external clock in the same frequency range. In PWM/PFM mode, the TPS62816-Q1 automatically enters power save mode at light loads to maintain high efficiency across the whole load range. The TPS62816-Q1 provides a 1% output voltage accuracy in PWM mode, which helps design a power supply with high output voltage accuracy. The SS/TR pin allows setting the start-up time or tracking of the output voltage to an external source. This allows external sequencing of different supply rails and limiting the inrush current during start-up.

The TPS62816-Q1 is available as an adjustable version, packaged in a 3-mm × 2-mm VQFN package with wettable flanks.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS62816-Q1	VQFN	3.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency Versus Output Current; V_{OUT} = 3.3 V; PWM/PFM; f_S = 2.25 MHz

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2020) to Revision A (December 2021)	Page
• Changed document status from Advance Information to Production Data	1

5 Device Comparison Table

DEVICE NUMBER	V_{OUT} DISCHARGE	FOLDBACK CURRENT LIMIT	SPREAD SPECTRUM CLOCKING (SSC)	OUTPUT VOLTAGE
TPS62816QWRWYRQ1	ON	OFF	by COMP/FSET pin	adjustable

6 Pin Configuration and Functions

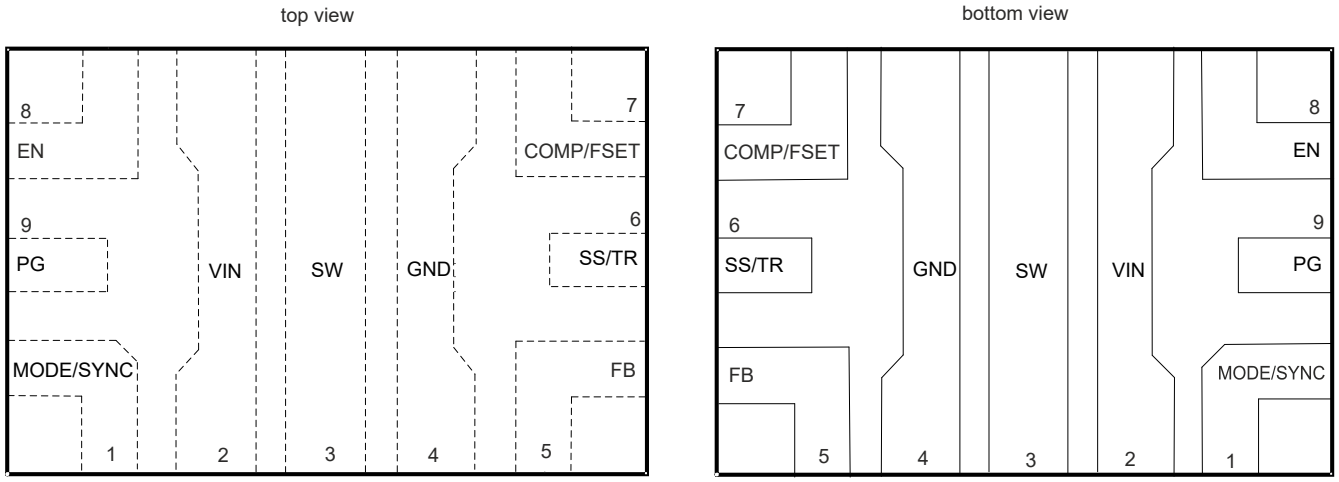


Figure 6-1. 9-Pin VQFN RWY Package (Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	8	I	This is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB	5	I	Voltage feedback input. Connect the resistive output voltage divider to this pin.
GND	4		Ground pin
MODE/SYNC	1	I	The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external frequency. See the *Electrical Characteristics* for the detailed specification for the digital signal applied to this pin for external synchronization.
COMP/FSET	7	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized.
PG	9	O	Open-drain power-good output
SS/TR	6	I	Soft-start / tracking pin. An external capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing. See Section 10.
SW	3	O	This is the switch pin of the converter and is connected to the internal power MOSFETs.
VIN	2		Power supply input. Make sure the input capacitor is connected as close as possible between the VIN pin and PGND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	6.5	V
	SW (DC)	–0.3	V_{IN} + 0.3	
	SW (AC, less than 10 ns)(3)	–3	10	
	FB	–0.3	4	
	COMP/FSET, PG, SS/TR	–0.3	V_{IN} + 0.3	
	EN, MODE/SYNC	–0.3	6.5	
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD classification level 2 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		6	V
V_{OUT}	Output voltage range	0.6		5.5	V
L	Effective inductance	0.15	0.22	0.3	µH
C_{OUT}	Effective output capacitance(1)	32	66	470	µF
C_{IN}	Effective input capacitance(1)	5	10		µF
R_{CF}		4.5		100	kΩ
I_{SINK_PG}	Sink current at PG pin	0		2	mA
T_J	Junction temperature	–40		150	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer's DC bias curves for the effective capacitance versus DC voltage applied. Further restrictions may apply. Please see the feature description for COMP/FSET about the output capacitance versus compensation setting and output voltage.

7.4 Thermal Information

THERMAL METRIC[1]		TPS62816-Q1 RWY (JEDEC) 9 PINS	TPS62816-Q1 RWY (EVM) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71	48	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	n/a	°C/W
Y_{JB}	Junction-to-board characterization parameter	16.1	n/a	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to +150°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = V_{IN}, no load, device not switching, T_J = 125°C, MODE = GND			36	µA
I_Q	Quiescent current	EN = V_{IN}, no load, device not switching, MODE = GND, V_{OUT} = 0.6 V		26	50	µA
I_{SD}	Shutdown current	EN = GND, at T_J = 125°C			90	µA
I_{SD}	Shutdown current	EN = GND, nominal value at T_J = 25°C, max value at T_J = 150°C		2.2	230	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.45	2.6	2.7	V
		V_{IN} falling	2.1	2.5	2.6	V
T_{JSD}	Thermal shutdown threshold	T_J rising		180		°C
	Thermal shutdown hysteresis	T_J falling		15		°C
CONTROL and INTERFACE						
$V_{IH,EN}$	Input threshold voltage at EN, rising edge		1.05	1.1	1.15	V
$V_{IL,EN}$	Input threshold voltage at EN, falling edge		0.96	1.0	1.05	V
V_{IH}	High-level input-threshold voltage at MODE/SYNC		1.1			V
$I_{IH,EN}$	Input leakage current into EN	V_{IH} = V_{IN} or V_{IL} = GND			125	nA
V_{IL}	Low-level input-threshold voltage at MODE/SYNC				0.3	V
I_{IH}	Input leakage current into MODE/SYNC				250	nA
t_{Delay}	Enable delay time	Time from EN high to device starts switching; V_{IN} applied already	135	270	520	µs
t_{Ramp}	Output voltage ramp time, SS/TR pin open	I_{OUT} = 0 mA, time from device starts switching to power good; device not in current limit	90	150	220	µs
$I_{SS/TR}$	SS/TR source current		8	10	12	µA
R_{DIS}	Internal discharge resistance on SS/TR when EN = low		0.7	1.1	1.5	kΩ
	Tracking gain	V_{FB} / $V_{SS/TR}$		1		
	Tracking offset	V_{FB} when $V_{SS/TR}$ = 0 V		±1		mV
f_{SYNC}	Frequency range on MODE/SYNC pin for synchronization		1.8		4	MHz

Over operating junction temperature range (T_J = –40°C to +150°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Duty cycle of synchronization signal at MODE/SYNC		20		80	%
	Time to lock to external frequency			50		µs
	resistance from COMP/FSET to GND for logic low	Internal frequency setting with f = 2.25 MHz	0		2.5	kΩ
	Voltage on COMP/FSET for logic high	internal frequency setting with f = 2.25 MHz		V_{IN}		V
V_{TH_PG}	UVP power good threshold voltage; dc level	rising (%V_{FB})	92%	95%	98%	
V_{TH_PG}	UVP power good threshold voltage; dc level	falling (%V_{FB})	87%	90%	93%	
V_{TH_PG}	OVP power good threshold voltage; dc level	rising (%V_{FB})	107%	110%	113%	
	OVP power good threshold voltage; dc level	falling (%V_{FB})	104%	107%	111%	
$V_{OL,PG}$	Low-level output voltage at PG	I_{SINK_PG} = 2 mA		0.01	0.3	V
$I_{IH,PG}$	Input leakage current into PG	V_{PG} = 5 V			100	nA
t_{PG}	PG deglitch time	For a high level to low level transition on the power good output		40		µs
OUTPUT						
V_{FB}	Feedback voltage			0.6		V
$I_{IH,FB}$	Input leakage current into FB	V_{FB} = 0.6 V		1	70	nA
V_{FB}	Feedback voltage accuracy	PWM, $V_{IN} \geq V_{OUT}$ + 1 V	–1%		1%	
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, $V_{OUT} \geq$ 1.5 V, Co,eff ≥ 47 µF	–1%		2%	
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, V_{OUT} < 1.5 V, Co,eff ≥ 68 µF	–1%		2.5%	
V_{FB}	Feedback voltage accuracy with voltage tracking	$V_{IN} \geq V_{OUT}$ + 1 V, $V_{SS/TR}$ = 0.3 V, PWM mode	–5%		5%	
	Load regulation	PWM		0.05		%/A
	Line regulation	PWM, I_{OUT} = 1 A, $V_{IN} \geq V_{OUT}$ + 1 V		0.02		%/V
R_{DIS}	Output discharge resistance				50	Ω
f_{SW}	PWM switching frequency range	MODE = high, see the FSET pin functionality about setting the switching frequency	1.8	2.25	4	MHz
f_{SW}	PWM switching frequency	With COMP/FSET tied to GND or V_{IN}	2.08	2.25	2.4	MHz
f_{SW}	PWM switching frequency tolerance	using a resistor from COMP/FSET to GND	–12%		12%	
$t_{on,min}$	Minimum on time of high-side FET	$V_{IN} \geq$ 3.3 V, T_J = –40°C to 125°C		45	67	ns
$t_{on,min}$	Minimum on time of low-side FET			15		ns
$R_{DS(ON)}$	High-side FET on-resistance	$V_{IN} \geq$ 5 V		11	26	mΩ
	Low-side FET on-resistance	$V_{IN} \geq$ 5 V		9	19	mΩ
I_{IH}	High-side MOSFET leakage current			0.01	230	µA
I_{IH}	Low-side MOSFET leakage current	V(SW) = 6 V		0.01	290	µA
I_{IH}	SW leakage	V(SW) = 0.6V, current into SW pin	-0.05		30	µA
I_{LIMH}	High-side FET switch current limit	DC value, V_{IN} = 3 V to 6 V	7.3	9.2	10.4	A
I_{LIMNEG}	Low-side FET negative current limit	DC value		-3		A

7.6 Typical Characteristics

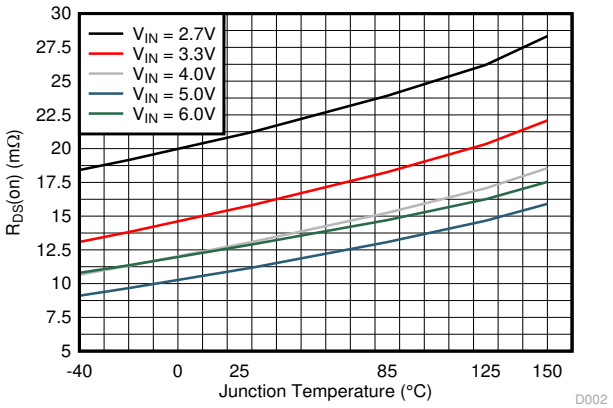


Figure 7-1. $R_{DS(ON)}$ of High-Side Switch

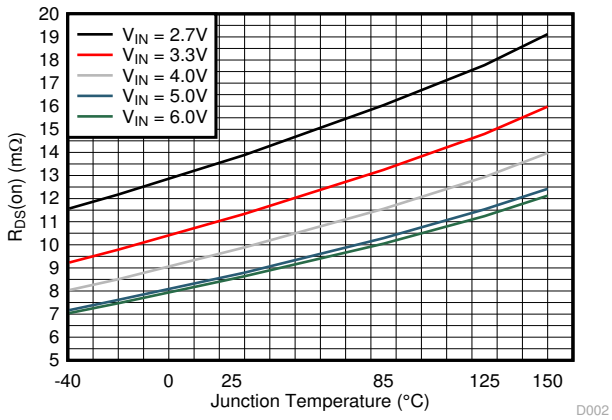


Figure 7-2. $R_{DS(ON)}$ of Low-Side Switch

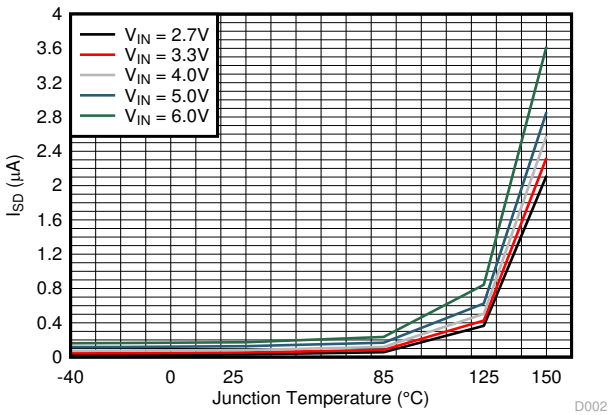


Figure 7-3. Shutdown Current vs Temperature

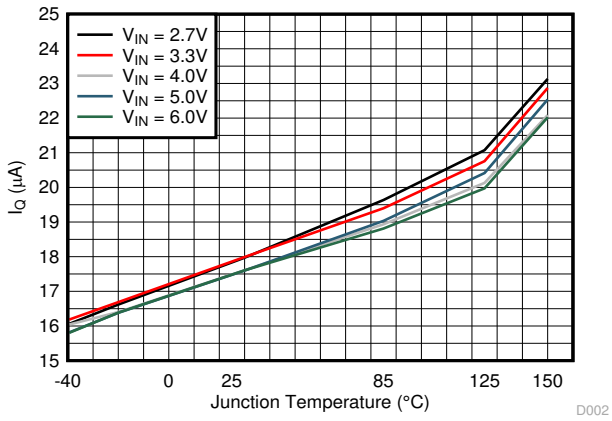


Figure 7-4. Quiescent Current vs Temperature

8 Parameter Measurement Information

The graphs in this data sheet have been taken based on the schematic and BOM as listed in Table 8-1 if not otherwise mentioned in the plots.

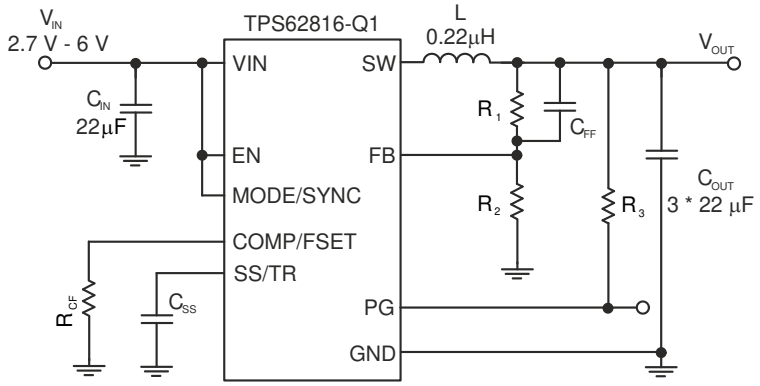


Figure 8-1. Measurement Setup for TPS62816-Q1

Table 8-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPS62816-Q1	Texas Instruments
L	0.25-µH inductor; XGL4020-251ME	Coilcraft
C_{IN}	22 µF / 10 V; GCM31CR71A226KE02L	Murata
C_{OUT} for V_{OUT} = 0.6 V	5 × 22 µF / 10 V; GCM31CR71A226KE02L	Murata
C_{OUT} for V_{OUT} ≥ 1 V	3 × 22 µF / 10 V; GCM31CR71A226KE02L	Murata
C_{SS}	15 nF (equal to 0.9-ms start-up ramp)	any
R_{CF}	8.06 kΩ	any
C_{FF}	10 pF	any
R_1	Depending on V_{OUT}	any
R_2	Depending on V_{OUT}	any
R_3	100 kΩ	any

(1) See the *Third Party-Products Disclaimer*.

9 Detailed Description

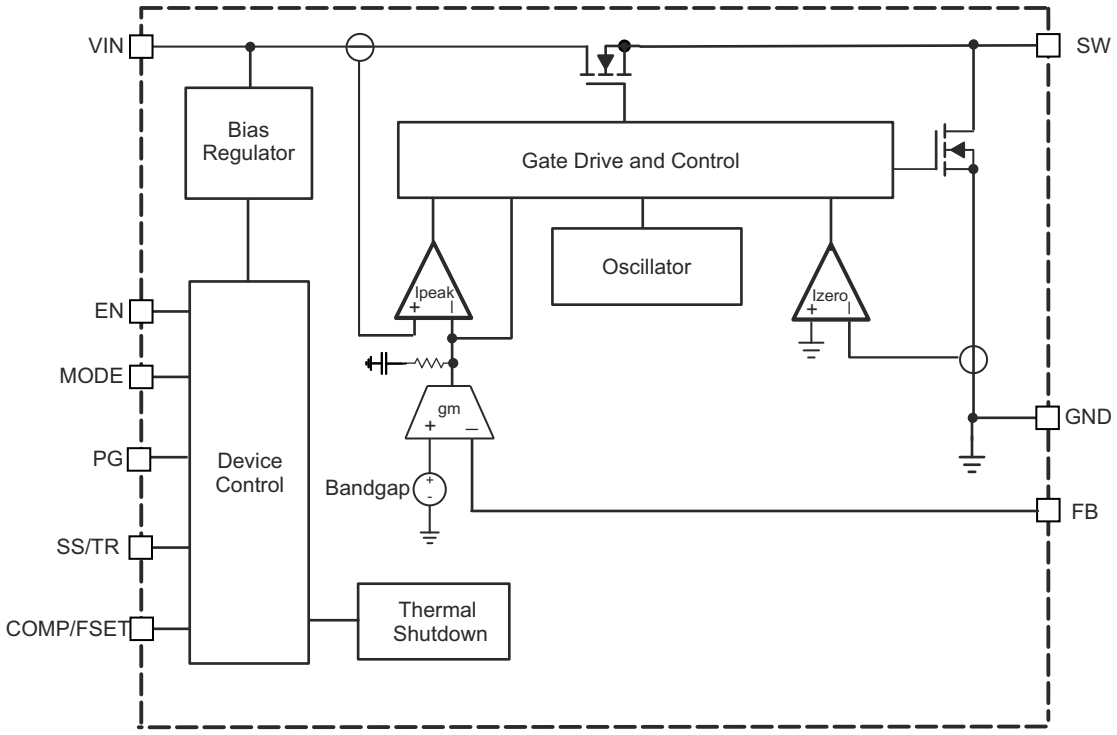
9.1 Overview

The TPS62816-Q1 synchronous switch mode power converter is based on a peak current mode control topology. The control loop is internally compensated.

To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with the TPS62816-Q1, the internal compensation has two settings. See Section 9.3.2. One out of the two compensation settings is chosen either by a resistor from COMP/FSET to GND, or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors. The device requires a small feedforward capacitor on the output voltage divider for best transient response. See Table 10-2.

The device supports forced fixed frequency PWM operation with the MODE pin tied to a logic high level. The frequency is defined as either 2.25 MHz internally fixed when COMP/FSET is tied to GND or VIN, or in a range of 1.8 MHz to 4 MHz defined by a resistor from COMP/FSET to GND. Alternatively, the devices can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz, applied to the MODE pin with no need for additional passive components. An internal PLL allows the device to change from internal clock to external clock during operation. The synchronization to the external clock is done on a falling edge of the clock applied at MODE to the rising edge on the SW pin. This allows a roughly 180° phase shift when the SW pin is used to generate the synchronization signal for a second converter. When the MODE pin is set to a logic low level, the device operates in power save mode (PFM) at low output current and automatically transfers to fixed-frequency PWM mode at higher output current. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Precise Enable

The voltage applied at the Enable (EN) pin of the TPS62816-Q1 is compared to a fixed threshold of 1.1 V for a rising voltage. This allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The precise enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the EN pin.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS62816-Q1 starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown, with a shutdown current of typically 1 µA. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

9.3.2 COMP/FSET

This pin allows the user to set two different parameters independently:

- Internal compensation settings for the control loop (three settings available)
- The switching frequency in PWM mode from 1.8 MHz to 4 MHz
- Enable/ disable spread spectrum clocking (SSC)

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows the user to adopt the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at the start-up of the converter, so a change in the resistor during operation only has an effect on the switching frequency, but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined switching frequency or compensation. Do not leave the pin floating.

The switching frequency has to be selected based on the input voltage and the output voltage to meet the specifications for the minimum on time and minimum off time.

Example: V_{IN} = 5 V, V_{OUT} = 1 V --> duty cycle (DC) = 1 V / 5 V = 0.2

- with t_{on} = DC × T --> $t_{on,min}$ = 1/$f_{s,max}$ × DC
- --> $f_{s,max}$ = 1/$t_{on,min}$ × DC = 1/0.075 µs × 0.2 = 2.6 MHz

The compensation range has to be chosen based on the minimum capacitance used. The capacitance can be increased from the minimum value as given in Table 9-1, up to the maximum of 470 µF in all of the three compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1 with spread spectrum clocking (SSC) disabled:

$$R_{CF}(k\Omega) = \frac{18MHz \cdot k\Omega}{f_S(MHz)} \quad (1)$$

For compensation (comp) setting 1 with spread spectrum clocking (SSC) enabled:

$$R_{CF}(k\Omega) = \frac{60MHz \cdot k\Omega}{f_S(MHz)} \quad (2)$$

For compensation (comp) setting 2 with spread spectrum clocking (SSC) disabled:

$$R_{CF}(k\Omega) = \frac{180MHz \cdot k\Omega}{f_S(MHz)} \quad (3)$$

Table 9-1. Switching Frequency and Compensation

COMPENSATION	R_{CF}	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE
for smallest output capacitance (comp setting 1) SSC disabled	10 kΩ ... 4.5 kΩ	1.8 MHz (10 kΩ) ... 4 MHz (4.5 kΩ) according to Equation 1	32 µF × V / V_{OUT}[V]
for smallest output capacitance (comp setting 1) SSC enabled	33 kΩ ... 15 kΩ	1.8 MHz (33 kΩ) ... 4 MHz (15 kΩ) according to Equation 2	32 µF × V / V_{OUT}[V]
for best transient response (larger output capacitance) (comp setting 2) SSC disabled	100 kΩ ... 45 kΩ	1.8 MHz (100 kΩ) ... 4 MHz (45 kΩ) according to Equation 3	72 µF × V / V_{OUT}[V]
for smallest output capacitance (comp setting 1) SSC disabled	tied to GND	internally fixed 2.25 MHz	32 µF × V / V_{OUT}[V]
for best transient response (larger output capacitance) (comp setting 2) SSC enabled	tied to V_{IN}	internally fixed 2.25 MHz	72 µF × V / V_{OUT}[V]

The minimum output capacitance required for stability depends on the output voltage as stated in Table 9-1. Refer to Section 10.1.2.2.2 for further details on the output capacitance required depending on the output voltage.

A too-high resistor value for R_{CF} is decoded as "tied to V_{IN}" and a value below the lowest range is decoded as "tied to GND". The minimum output capacitance in Table 9-1 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

9.3.3 MODE/SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode depending on the output current. The MODE/SYNC pin forces PWM mode when set high. The pin also allows the user to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. Similar to COMP/FSET, the specifications for the minimum on time and minimum off time have to be observed when setting the external frequency. For use with external synchronization on the MODE/SYNC pin, the internal switching frequency must be set by R_{CF} to a similar value than the externally applied clock. This ensures that if the external clock fails, the switching frequency stays in the same range. When there is no resistor from COMP/FSET to GND but the pin is pulled high or low, external synchronization is not possible.

9.3.4 Spread Spectrum Clocking (SSC)

The device offers spread spectrum clocking as an option, set by the COMP/FSET pin. When SSC is enabled, the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288 kHz above the nominal switching frequency. When the device is externally synchronized by applying a clock signal to the MODE/SYNC pin, the TPS62816-Q1 follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

9.3.5 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both of the power FETs. When enabled, the device is fully operational for input voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

9.3.6 Power Good Output (PG)

Power good is an open-drain output driven by a window comparator. PG is held low when the device is disabled, in undervoltage lockout, and thermal shutdown. When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the output is high impedance.

Table 9-2. PG Status

EN	DEVICE STATUS	PG STATE
X	V_{IN} < 2 V	undefined
low	V_{IN} ≥ 2 V	low
high	2 V ≤ V_{IN} ≤ UVLO OR in thermal shutdown OR V_{OUT} not in regulation	low
high	V_{OUT} in regulation	high impedance

9.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 170°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During a PFM pause, the thermal shutdown is not active. After a PFM pause, the device needs up to 9 µs to detect a too-high junction temperature. If the PFM burst is shorter than this delay, the device does not detect a too-high junction temperature.

9.4 Device Functional Modes

9.4.1 Pulse Width Modulation (PWM) Operation

The TPS62816-Q1 has two operating modes: Forced PWM mode as discussed in this section and PWM/PFM as discussed in Section 9.4.2.

With the MODE/SYNC pin set to high, the TPS62816-Q1 operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP pin to GND or by an external clock signal applied to the MODE/SYNC pin. With an external clock applied to MODE/SYNC, the TPS62816-Q1 follows the frequency applied to the pin. In general, the frequency range in forced PWM mode is 1.8 MHz to 4 MHz. However, the frequency needs to be in a range the TPS62816-Q1 can operate at, taking the minimum on time into account.

9.4.2 Power Save Mode Operation (PWM/PFM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of approximately 1.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency. In addition, the frequency set with the resistor on COMP/FSET must be in a range of 1.8 MHz to 3.5 MHz. The high-side switch in a PFM pulse is turned on until the inductor current reaches its peak current limit.

9.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as D = VOUT / VIN. The duty cycle increases as the input voltage comes close to the output voltage and the off time gets smaller. When the minimum off time of typically 10 ns is reached, the TPS62816-Q1 skips switching cycles while it approaches 100% mode. In 100% mode, it keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. In 100% mode, the low-side switch is turned off. The maximum dropout voltage in 100% mode is the product of the on-resistance of the high-side switch plus the series resistance of the inductor and the load current.

9.4.4 Current Limit and Short Circuit Protection

The TPS62816-Q1 is protected against overload and short circuit events. If the inductor current exceeds the current limit I_{LIMH}, the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side switch turns on again only if the current in the low-side switch has decreased

below the low-side current limit. Due to internal propagation delay, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \cdot t_{PD} \quad (4)$$

where:

- I_{LIMH} is the static current limit as specified in the electrical characteristics
- L is the effective inductance at the peak current
- V_L is the voltage across the inductor (V_{IN} - V_{OUT})
- t_{PD} is the internal propagation delay of typically 50 ns

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \cdot 50ns \quad (5)$$

9.4.5 Foldback Current Limit and Short Circuit Protection

This is valid for devices where foldback current limit is enabled.

When the device detects current limit for more than 1024 subsequent switching cycles, it reduces the current limit from its nominal value to a typical peak current of 3.7 A. Foldback current limit is left when the current limit indication goes away. For the case that device operation continues in current limit, it would, after 3072 switching cycles, try again full current limit for again 1024 switching cycles.

9.4.6 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled, but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active once the TPS62816-Q1 has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V. Output discharge is not activated during a current limit or foldback current limit event.

9.4.7 Soft Start/Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay of about 200 µs, then the internal reference and hence V_{OUT} rises with a slope controlled by an external capacitor connected to the SS/TR pin.

Leaving the SS/TR pin disconnected provides the fastest start-up ramp with 150 µs typically. A capacitor connected from SS/TR to GND is charged with 10 µA by an internal current source during soft start until it reaches the reference voltage of 0.6 V. The capacitance required to set a certain ramp-time (t_{ramp}), therefore, is:

$$Css[nF] = 10\mu A * t_{ramp}[ms] / 0.6V \quad (6)$$

If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin to GND to ensure a proper low level. Returning from those states causes a new startup sequence.

A voltage applied at SS/TR can be used to track a master voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current. The SS/TR pin must not be connected to the SS/TR pin of other devices. An external voltage applied on SS/TR is internally clamped to the feedback voltage (0.6 V). It is recommended to set the target for the external voltage on SS/TR slightly above the feedback voltage. Given the tolerances of the resistor divider R_5 and R_6 on

SS/TR, this makes sure the device "switches" to the internal reference voltage when the power-up sequencing is finished. See Figure 10-57.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Programming the Output Voltage

The output voltage of the TPS62816-Q1 is adjustable. It can be programmed for output voltages from 0.6 V to 5.5 V using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from Equation 7. It is recommended to choose resistor values that allow a current of at least 2 µA, meaning the value of R_2 must not exceed 400 kΩ. Lower resistor values are recommended for the highest accuracy and most robust design.

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{7}$$

10.1.2 External Component Selection

10.1.2.1 Inductor Selection

The TPS62816-Q1 is designed for a nominal 0.22-µH inductor with a switching frequency of typically 2.25 MHz. Larger values can be used to achieve a lower inductor current ripple, but they can have a negative impact on efficiency and transient response. Smaller values than 0.22 µH cause a larger inductor current ripple, which causes larger negative inductor current in forced PWM mode at low or no output current. For a higher or lower nominal switching frequency, the inductance must be changed accordingly. See the *Recommended Operating Conditions* for details.

The inductor selection is affected by several effects like the following:

- Inductor ripple current
- Output ripple voltage
- PWM-to-PFM transition point
- Efficiency

In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 8 calculates the maximum inductor current.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{8}$$

$$\Delta I_{L(\max)} = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{L \min} \cdot \frac{1}{f_{SW}} \tag{9}$$

where:

- $I_{L(max)}$ is the maximum inductor current.
- $\Delta I_{L(max)}$ is the peak-to-peak inductor ripple current.
- Lmin is the minimum inductance at the operating point.

Table 10-1. Typical Inductors

TYPE	INDUCTANCE [µH]	CURRENT [A](1)	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [L × W × H] mm	MANUFACTURER(2)
XEL4020-201ME	0.20 µH, ±20%	14	2.25 MHz	4 × 4 × 2.1	Coilcraft
XGL4020-251ME	0.25 µH, ±20%	12	2.25 MHz	4 × 4 × 2.1	Coilcraft
XEL4030-201ME	0.20 µH, ±20%	17	2.25 MHz	4 × 4 × 3.2	Coilcraft

(1) Lower of I_{RMS} at 20°C rise or I_{SAT} at 20% drop.
(2) See the *Third Party-Products Disclaimer*.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well.

10.1.2.2 Capacitor Selection

10.1.2.2.1 Input Capacitor

For most applications, 22 µF nominal is sufficient and is recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for the best filtering and must be placed between VIN and GND as close as possible to those pins.

10.1.2.2.2 Output Capacitor

The architecture of the TPS62816-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use dielectric X7R, X7T, or equivalent. Using a higher value has advantages, like smaller voltage ripple and a tighter DC output accuracy in Power Save mode. The COMP/FSET pin allows the user to select two different compensation settings based on the minimum capacitance used on the output. The maximum capacitance is 470 µF in any of the compensation settings.

The minimum capacitance required on the output depends on the compensation setting and output voltage.

For output voltages below 1 V, the minimum increases linearly from 32 µF at 1 V to 53 µF at 0.6 V with the compensation setting for smallest output capacitance. Other compensation ranges are equivalent. See Table 9-1 for details.

10.2 Typical Application

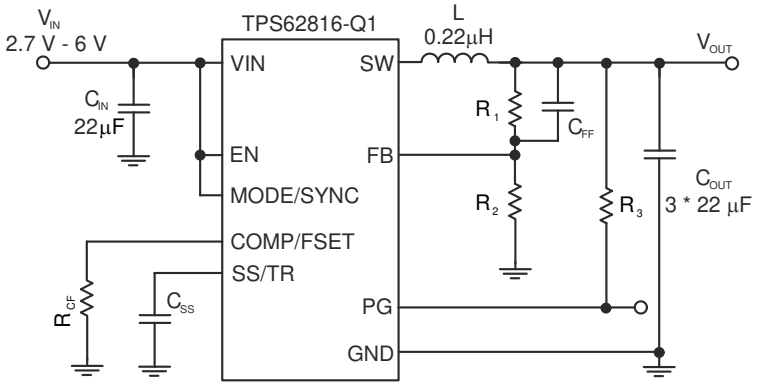


Figure 10-1. Typical Application

10.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

10.2.2 Detailed Design Procedure

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (10)$$

With V_{FB} = 0.6 V:

Table 10-2. Setting the Output Voltage

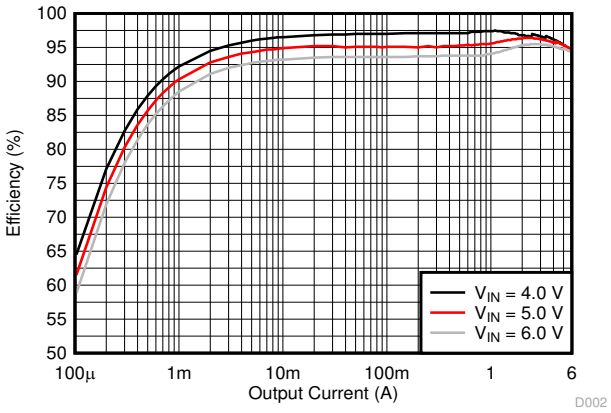
NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	C_{FF}	EXACT OUTPUT VOLTAGE
0.8 V	16.9 kΩ	51 kΩ	15 pF	0.7988 V
1.0 V	20 kΩ	30 kΩ	13 pF	1.0 V
1.1 V	39.2 kΩ	47 kΩ	6.8 pF	1.101 V
1.2 V	68 kΩ	68 kΩ	3.9 pF	1.2 V
1.5 V	76.8 kΩ	51 kΩ	3.3 pF	1.5 V
1.8 V	80.6 kΩ	40.2 kΩ	3.3 pF	1.803 V
2.5 V	47.5 kΩ	15 kΩ	5.6 pF	2.5 V
3.3 V	88.7 kΩ	19.6 kΩ	3 pF	3.315 V

The maximum value for the feedforward capacitor C_{FF} at minimum output capacitance is determined by Equation 11:

$$C_{FF,max}(F) = 2.661 \times 10^{-7}\ F \times \Omega\ /\ R1\ (\Omega) \quad (11)$$

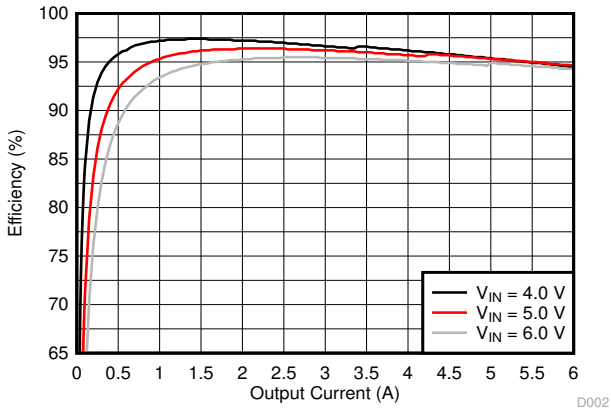
10.2.3 Application Curves

All plots have been taken with a nominal switching frequency of 2.25 MHz when set to PWM mode, unless otherwise noted. The BOM is according to Table 8-1.



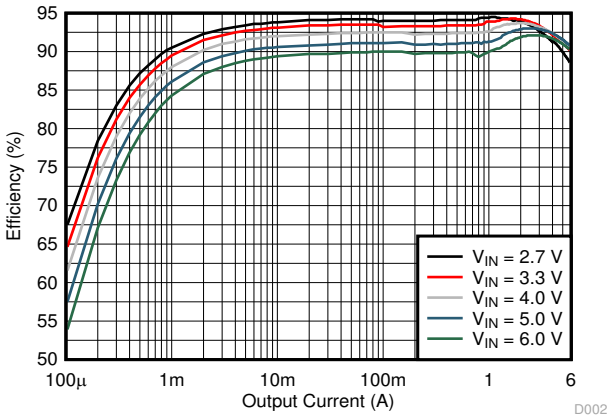
V_{OUT} = 3.3 V PFM T_A = 25°C

Figure 10-2. Efficiency Versus Output Current



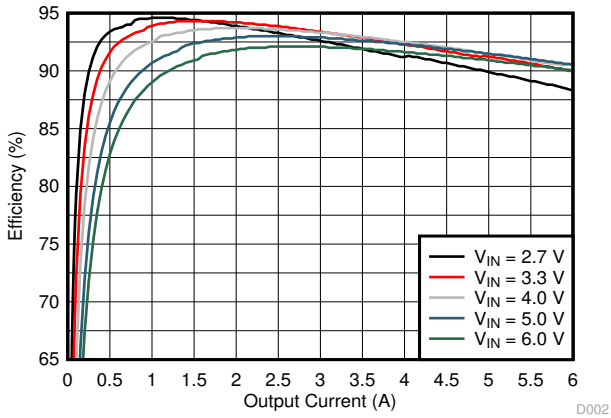
V_{OUT} = 3.3 V PWM T_A = 25°C

Figure 10-3. Efficiency Versus Output Current



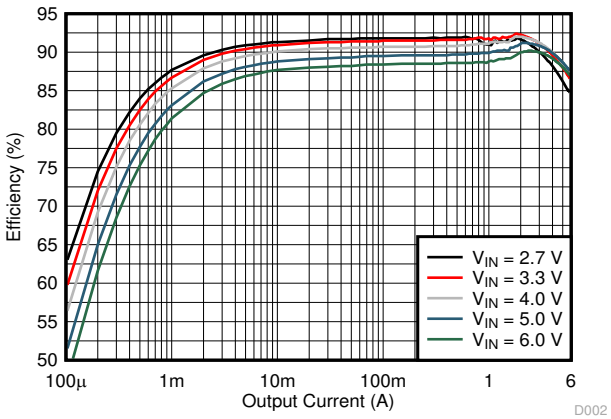
V_{OUT} = 1.8 V PFM T_A = 25°C

Figure 10-4. Efficiency Versus Output Current



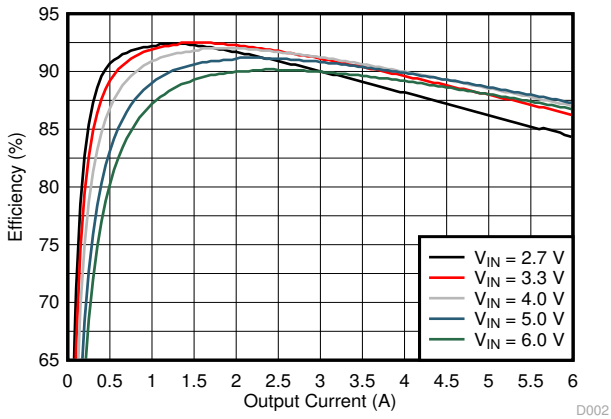
V_{OUT} = 1.8 V PWM T_A = 25°C

Figure 10-5. Efficiency Versus Output Current



V_{OUT} = 1.2 V PFM T_A = 25°C

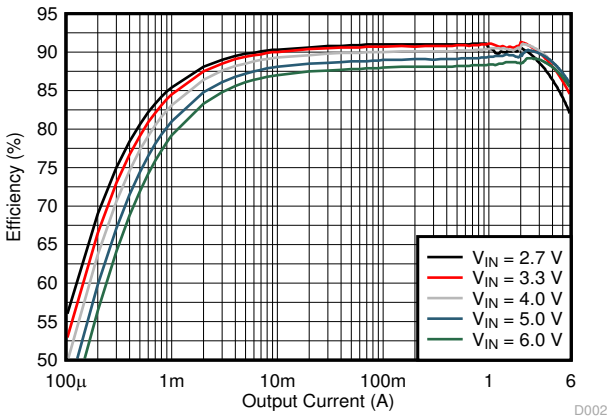
Figure 10-6. Efficiency Versus Output Current



V_{OUT} = 1.2 V PWM T_A = 25°C

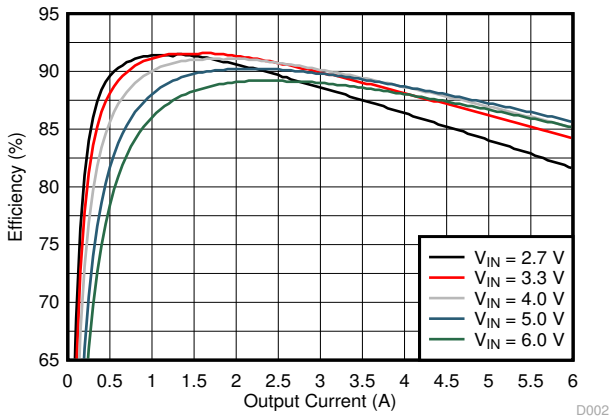
Figure 10-7. Efficiency Versus Output Current

10.2.3 Application Curves (continued)



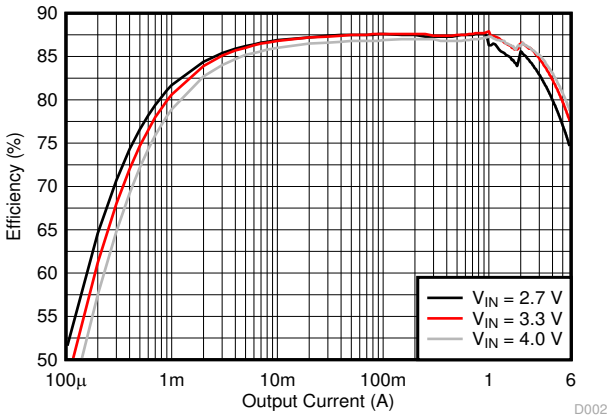
V_{OUT} = 1.0 V PFM T_A = 25°C

Figure 10-8. Efficiency Versus Output Current



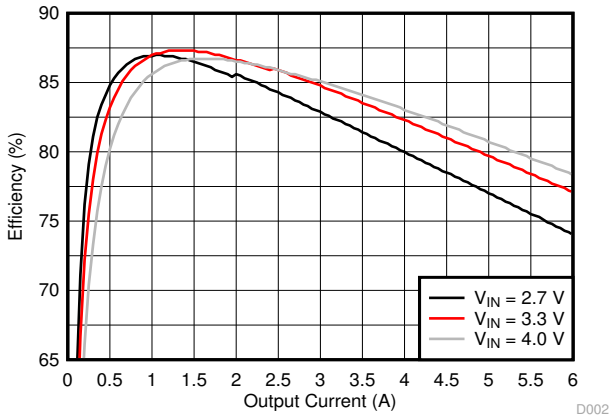
V_{OUT} = 1.0 V PWM T_A = 25°C

Figure 10-9. Efficiency Versus Output Current



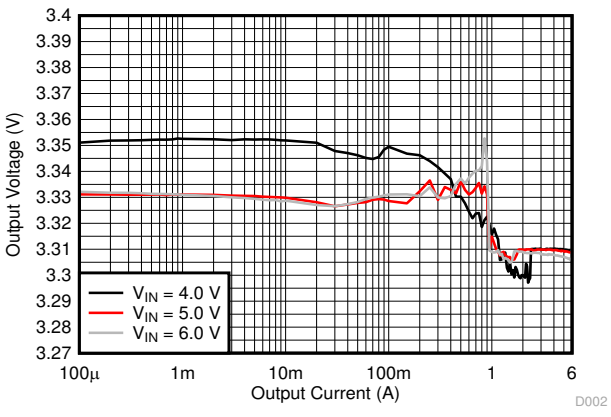
V_{OUT} = 0.6 V PFM T_A = 25°C

Figure 10-10. Efficiency Versus Output Current



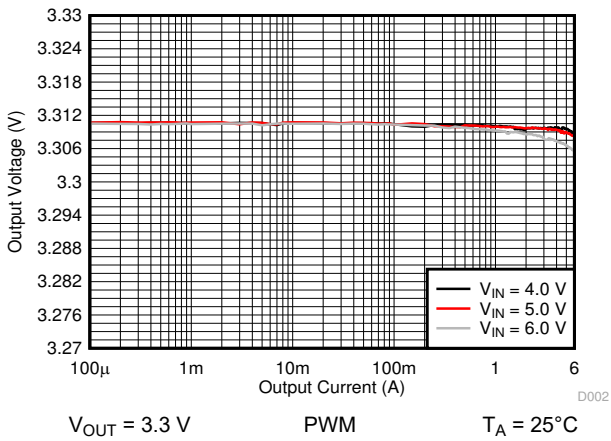
V_{OUT} = 0.6 V PWM T_A = 25°C

Figure 10-11. Efficiency Versus Output Current



V_{OUT} = 3.3 V PFM T_A = 25°C

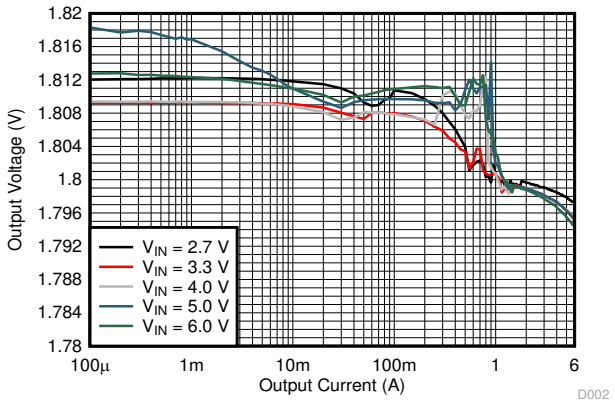
Figure 10-12. Output Voltage Versus Output Current



V_{OUT} = 3.3 V PWM T_A = 25°C

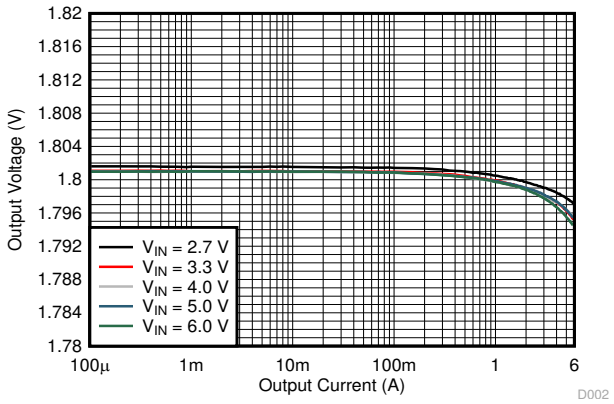
Figure 10-13. Output Voltage Versus Output Current

10.2.3 Application Curves (continued)



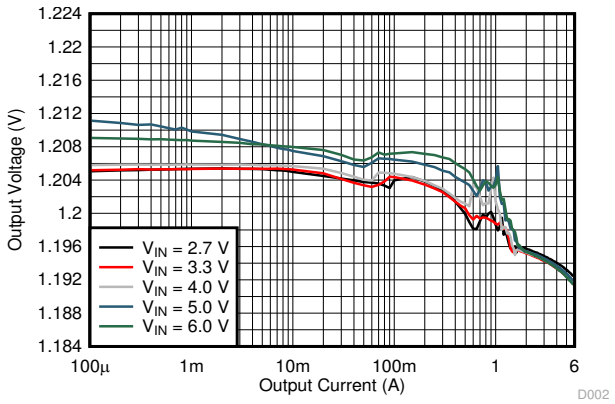
V_{OUT} = 1.8 V PFM T_A = 25°C

Figure 10-14. Output Voltage Versus Output Current



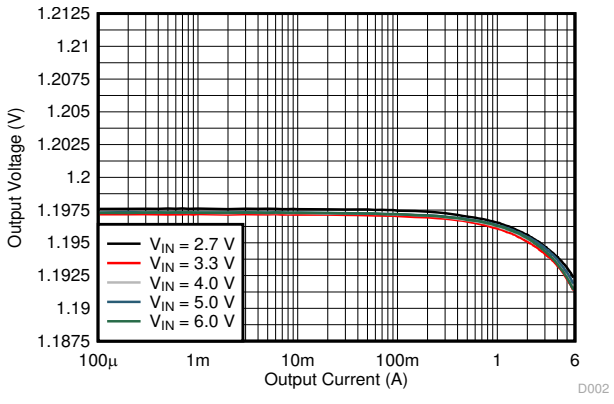
V_{OUT} = 1.8 V PWM T_A = 25°C

Figure 10-15. Output Voltage Versus Output Current



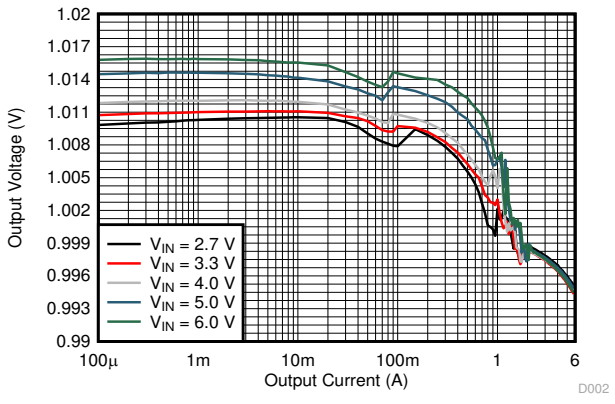
V_{OUT} = 1.2 V PFM T_A = 25°C

Figure 10-16. Output Voltage Versus Output Current



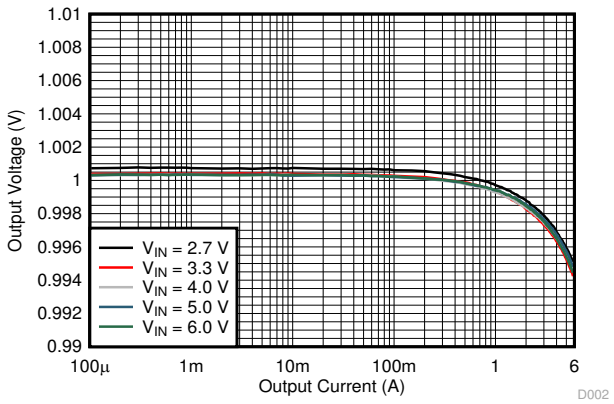
V_{OUT} = 1.2 V PWM T_A = 25°C

Figure 10-17. Output Voltage Versus Output Current



V_{OUT} = 1.0 V PFM T_A = 25°C

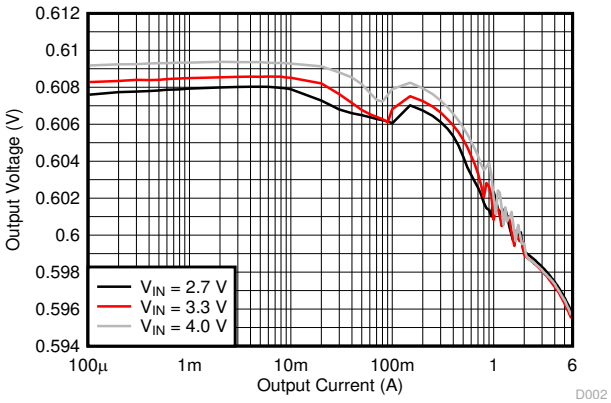
Figure 10-18. Output Voltage Versus Output Current



V_{OUT} = 1.0 V PWM T_A = 25°C

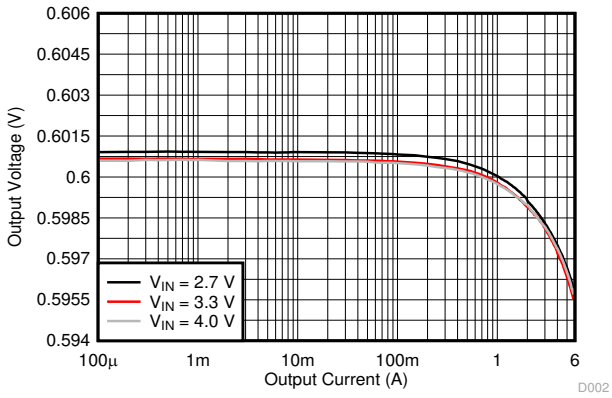
Figure 10-19. Output Voltage Versus Output Current

10.2.3 Application Curves (continued)



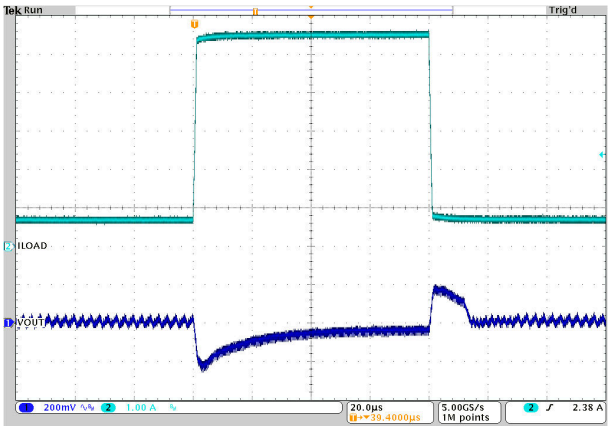
V_{OUT} = 0.6 V PFM T_A = 25°C

Figure 10-20. Output Voltage Versus Output Current



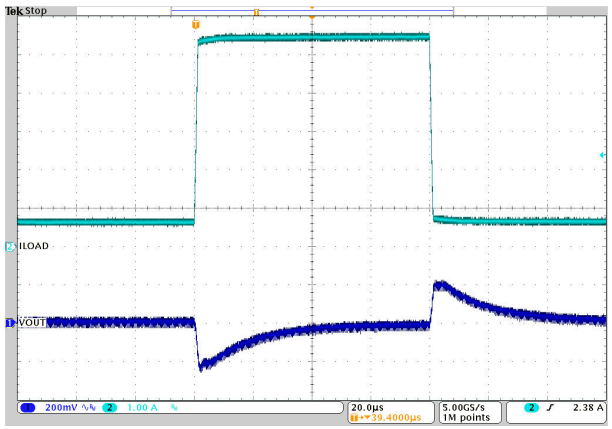
V_{OUT} = 0.6 V PWM T_A = 25°C

Figure 10-21. Output Voltage Versus Output Current



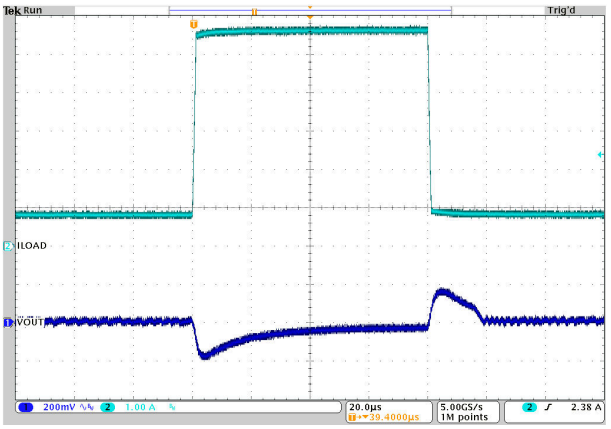
V_{OUT} = 3.3 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

Figure 10-22. Load Transient Response



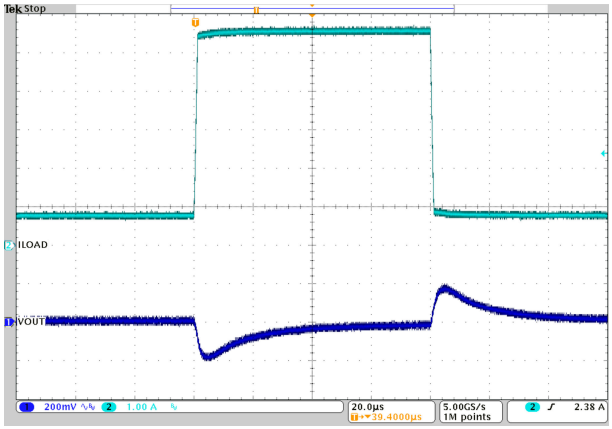
V_{OUT} = 3.3 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

Figure 10-23. Load Transient Response



V_{OUT} = 1.8 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

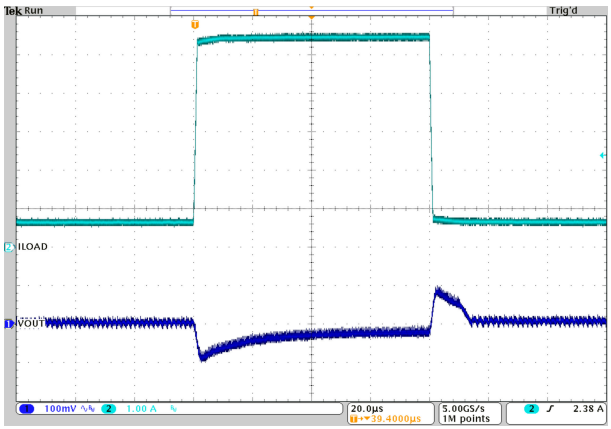
Figure 10-24. Load Transient Response



V_{OUT} = 1.8 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

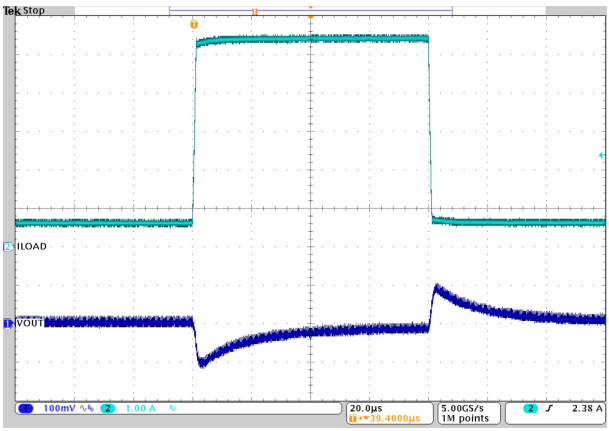
Figure 10-25. Load Transient Response

10.2.3 Application Curves (continued)



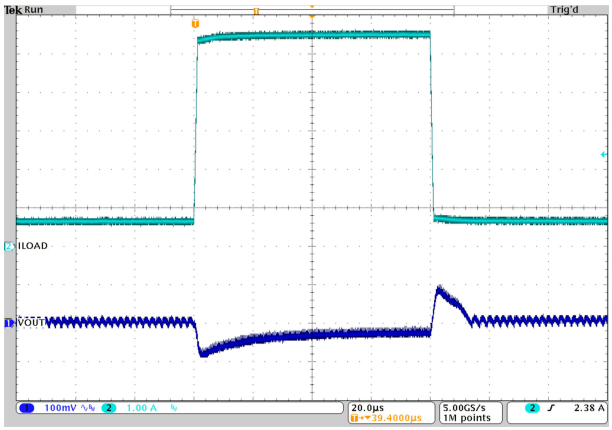
V_{OUT} = 1.2 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

Figure 10-26. Load Transient Response



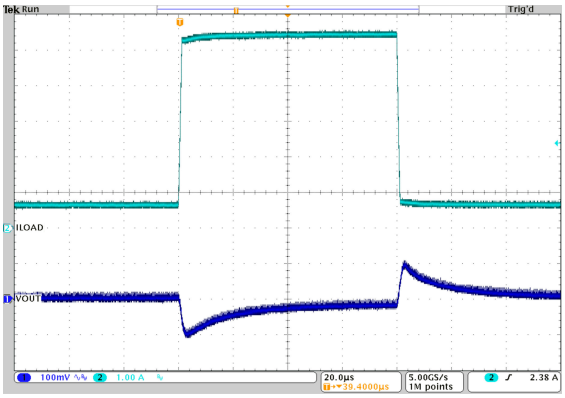
V_{OUT} = 1.2 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

Figure 10-27. Load Transient Response



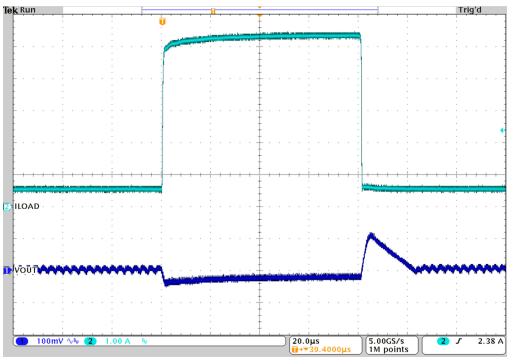
V_{OUT} = 1.0 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

Figure 10-28. Load Transient Response



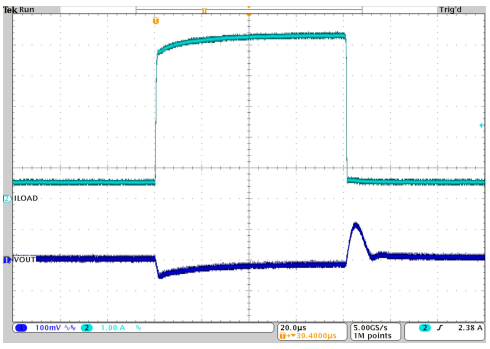
V_{OUT} = 1.0 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

Figure 10-29. Load Transient Response



V_{OUT} = 0.6 V PFM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

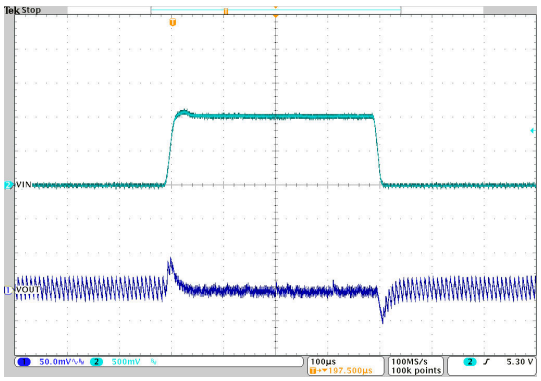
Figure 10-30. Load Transient Response



V_{OUT} = 0.6 V PWM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

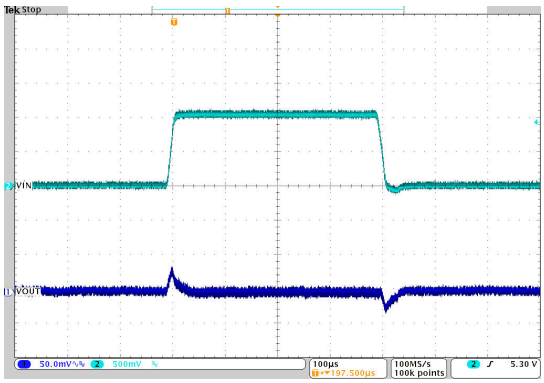
Figure 10-31. Load Transient Response

10.2.3 Application Curves (continued)



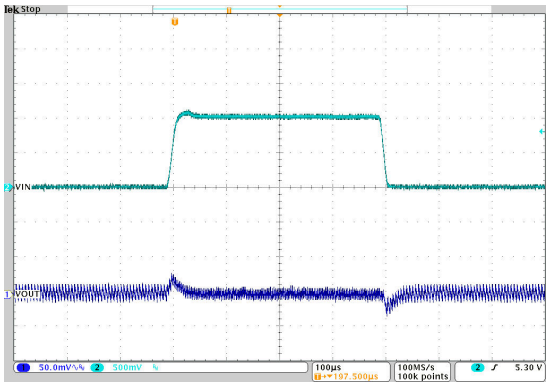
V_{OUT} = 3.3 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-32. Line Transient Response



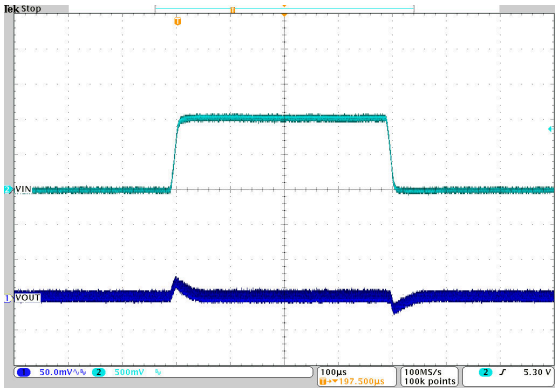
V_{OUT} = 3.3 V PWM T_A = 25°C
I_{OUT} = 6 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-33. Line Transient Response



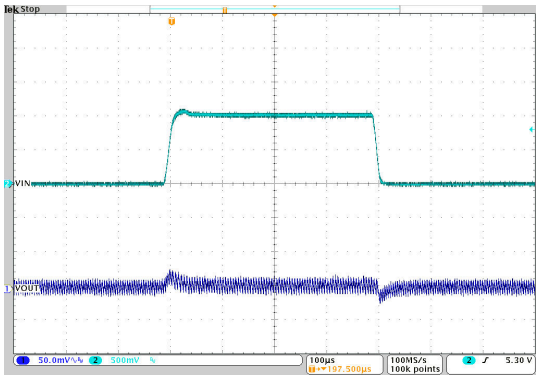
V_{OUT} = 1.8 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-34. Line Transient Response



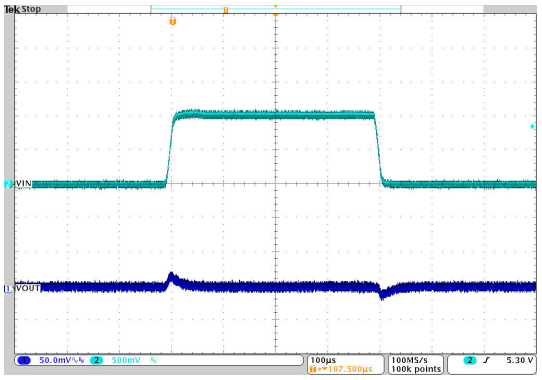
V_{OUT} = 1.8 V PWM T_A = 25°C
I_{OUT} = 6 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-35. Line Transient Response



V_{OUT} = 1.2 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

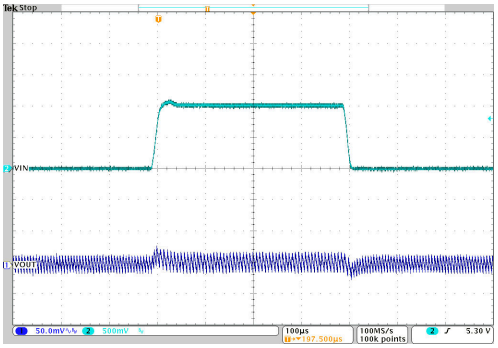
Figure 10-36. Line Transient Response



V_{OUT} = 1.2 V PWM T_A = 25°C
I_{OUT} = 6 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

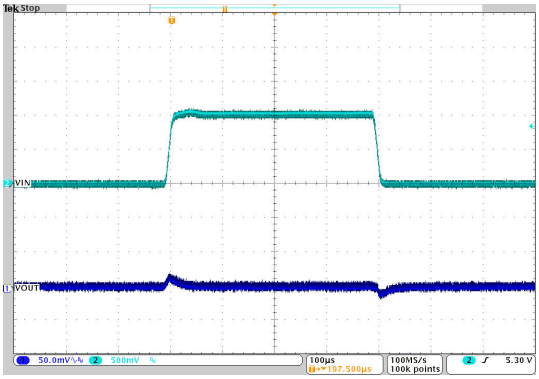
Figure 10-37. Line Transient Response

10.2.3 Application Curves (continued)



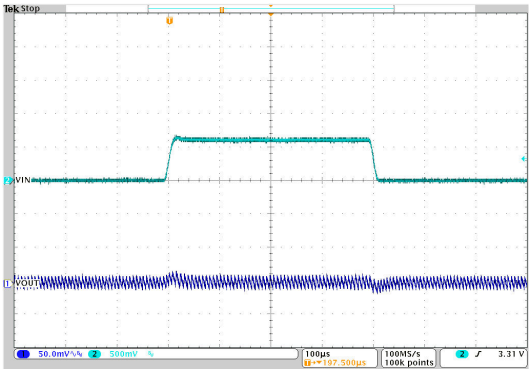
V_{OUT} = 1.0 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-38. Line Transient Response



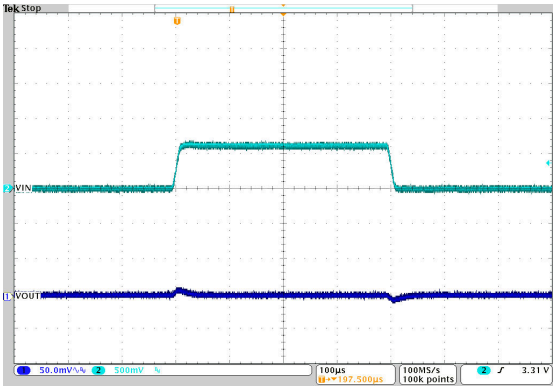
V_{OUT} = 1.0 V PWM T_A = 25°C
I_{OUT} = 6 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-39. Line Transient Response



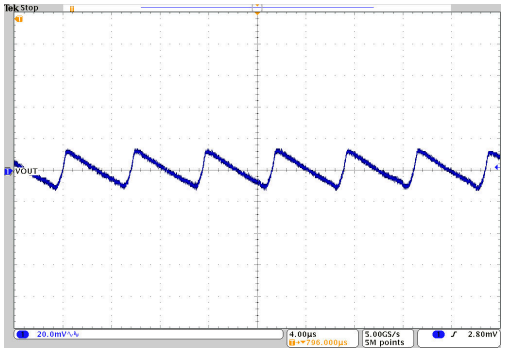
V_{OUT} = 0.6 V PFM T_A = 25°C
I_{OUT} = 0.2 A V_{IN} = 3.0 V to 3.6 V to 3.0 V

Figure 10-40. Line Transient Response



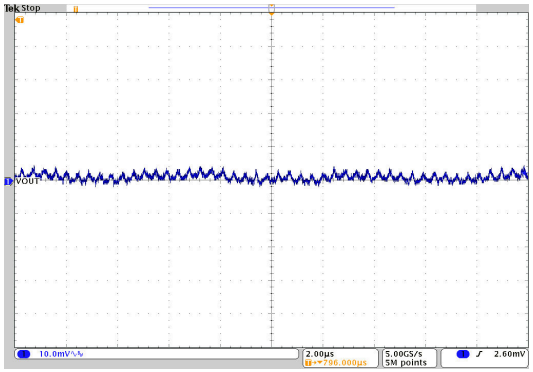
V_{OUT} = 0.6 V PWM T_A = 25°C
I_{OUT} = 6 A V_{IN} = 3.0 V to 3.6 V to 3.0 V

Figure 10-41. Line Transient Response



V_{OUT} = 3.3 V PFM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 0.2 A

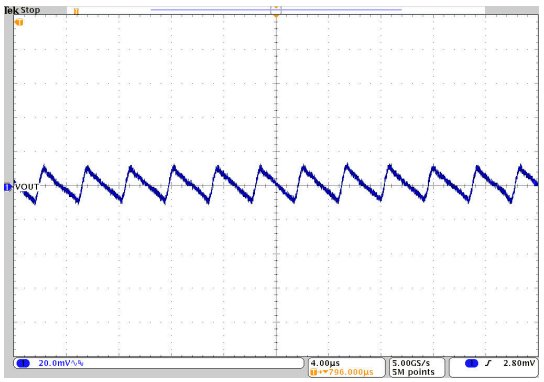
Figure 10-42. Output Voltage Ripple



V_{OUT} = 3.3 V PWM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 6 A

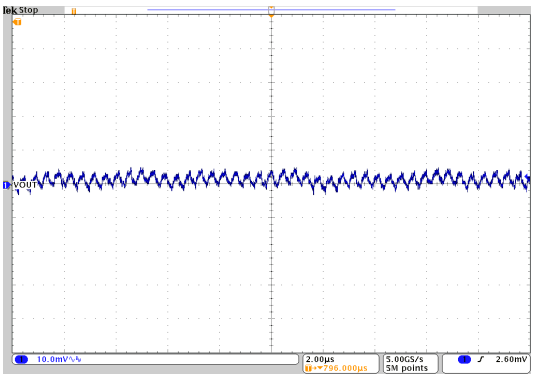
Figure 10-43. Output Voltage Ripple

10.2.3 Application Curves (continued)



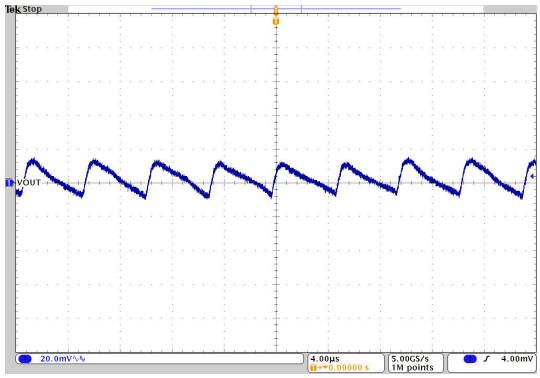
V_{OUT} = 1.8 V PFM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 0.2 A

Figure 10-44. Output Voltage Ripple



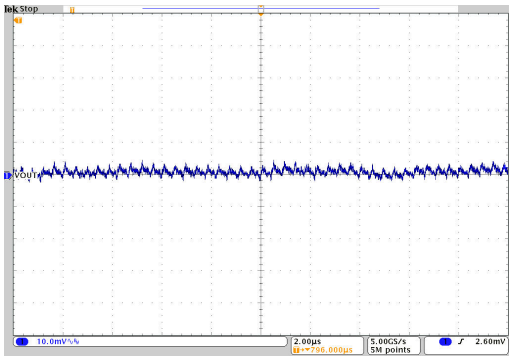
V_{OUT} = 1.8 V PWM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 6 A

Figure 10-45. Output Voltage Ripple



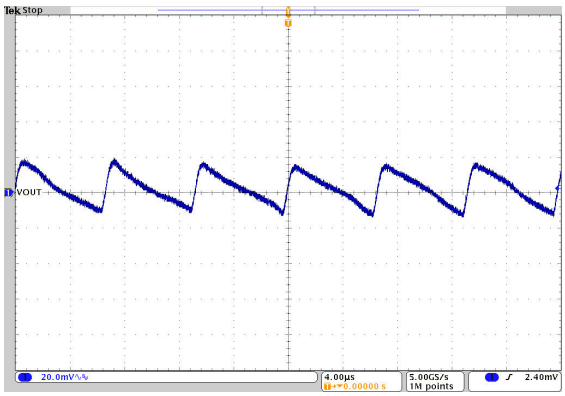
V_{OUT} = 1.2 V PFM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 0.2 A

Figure 10-46. Output Voltage Ripple



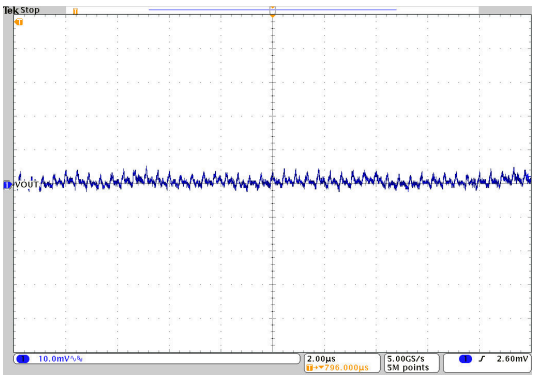
V_{OUT} = 1.2 V PWM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 6 A

Figure 10-47. Output Voltage Ripple



V_{OUT} = 1.0 V PFM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 0.2 A

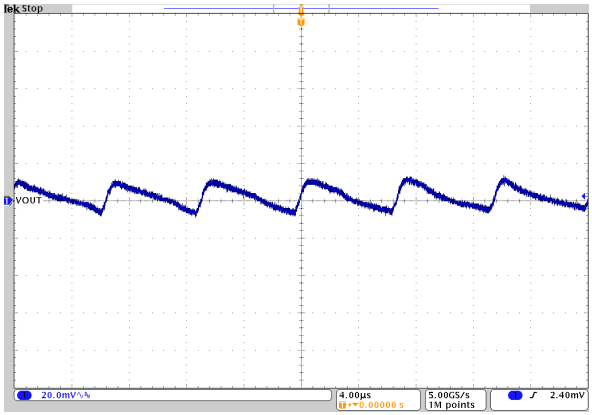
Figure 10-48. Output Voltage Ripple



V_{OUT} = 1.0 V PWM T_A = 25°C
V_{IN} = 5 V I_{OUT} = 6 A

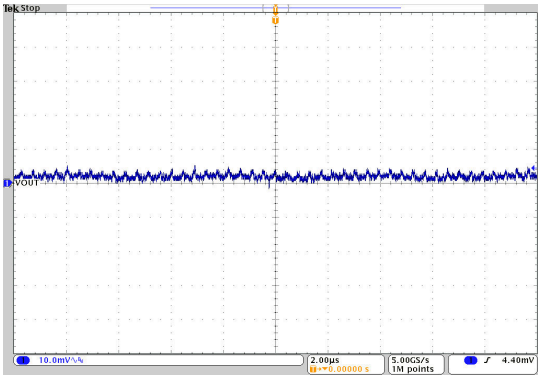
Figure 10-49. Output Voltage Ripple

10.2.3 Application Curves (continued)



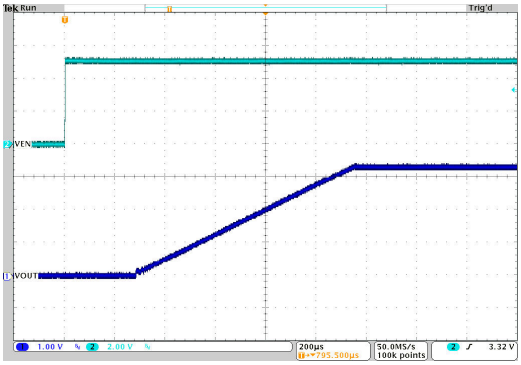
V_{OUT} = 0.6 V PFM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.2 A

Figure 10-50. Output Voltage Ripple



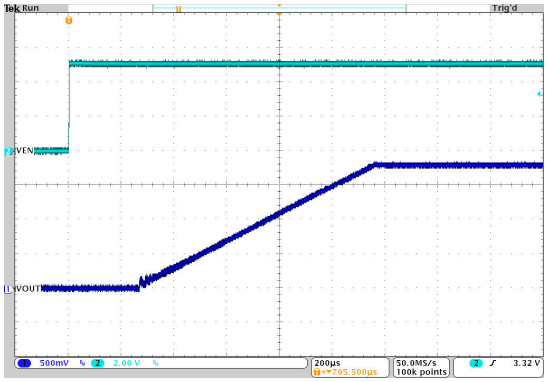
V_{OUT} = 0.6 V PWM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 6 A

Figure 10-51. Output Voltage Ripple



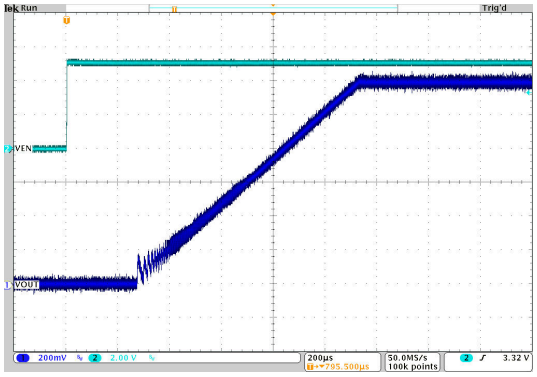
V_{OUT} = 3.3 V PWM or PFM T_A = 25°C
V_{IN} = 5 V C_{SS} = 15 nF I_{OUT} = 6 A

Figure 10-52. Start-Up Timing



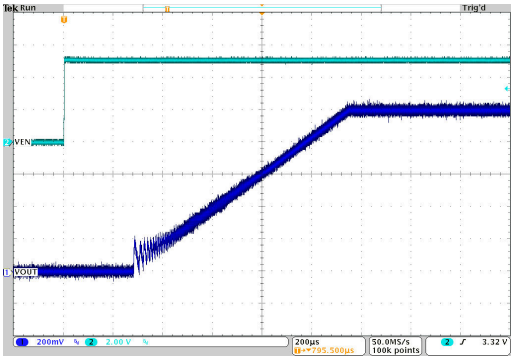
V_{OUT} = 1.8 V PWM or PFM T_A = 25°C
V_{IN} = 5 V C_{SS} = 15 nF I_{OUT} = 6 A

Figure 10-53. Start-Up Timing



V_{OUT} = 1.2 V PWM or PFM T_A = 25°C
V_{IN} = 5 V C_{SS} = 15 nF I_{OUT} = 6 A

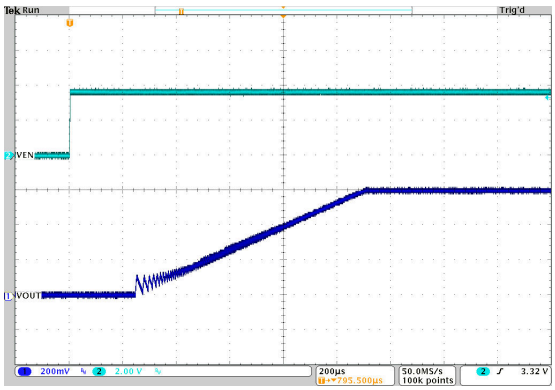
Figure 10-54. Start-Up Timing



V_{OUT} = 1.0 V PWM or PFM T_A = 25°C
V_{IN} = 5 V C_{SS} = 15 nF I_{OUT} = 6 A

Figure 10-55. Start-Up Timing

10.2.3 Application Curves (continued)



V_{OUT} = 0.6 V	PWM or PFM	T_A = 25°C
V_{IN} = 3.3 V	C_{SS} = 15 nF	I_{OUT} = 6 A

Figure 10-56. Start-Up Timing

10.3 System Examples

10.3.1 Voltage Tracking

The TPS62816-Q1 follows the voltage applied to the SS/TR pin. A voltage ramp on SS/TR to 0.6 V ramps the output voltage according to the 0.6-V feedback voltage.

Tracking the 3.3 V of the primary device such that both rails reach their target voltage at the same time, requires a resistor divider on SS/TR of the secondary device equal to the output voltage divider of the primary device. The output current of 10 µA on the SS/TR pin causes an offset voltage on the resistor divider formed by R_5 and R_6. The equivalent resistance of R_5 // R_6 must therefore be kept below 4 kΩ. The current from SS/TR causes a slightly higher voltage across R6 than 0.6 V, which is desired because the secondary device switches to its internal reference as soon as the voltage at SS/TR is higher than 0.6 V.

In case both devices need to run in forced PWM mode, it is recommended to tie the MODE pin of the secondary device to the output voltage or the power good signal of the primary device. The TPS62816-Q1 has a duty cycle limitation defined by the minimum on time. For tracking down to low output voltages, the secondary device cannot follow once the minimum duty cycle is reached. Enabling PFM mode while tracking is in progress allowsthe user to ramp down the output voltage close to 0 V.

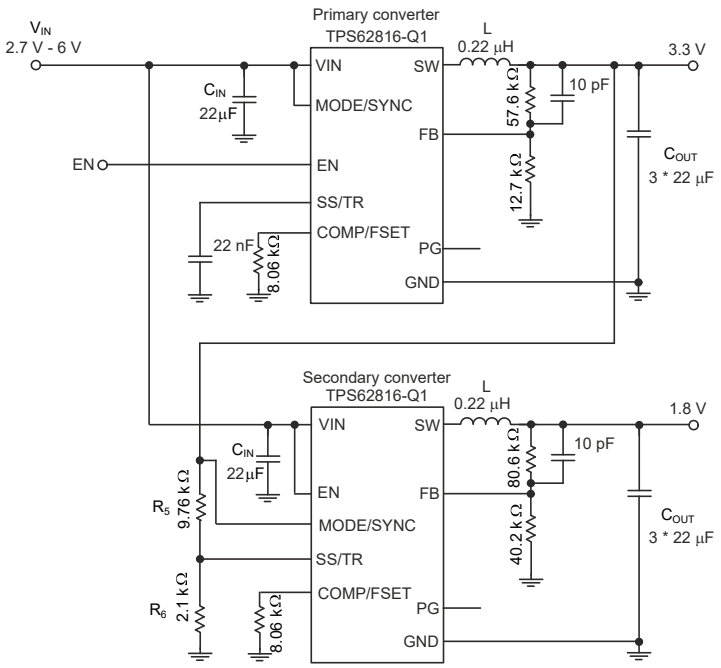


Figure 10-57. Schematic for Output Voltage Tracking

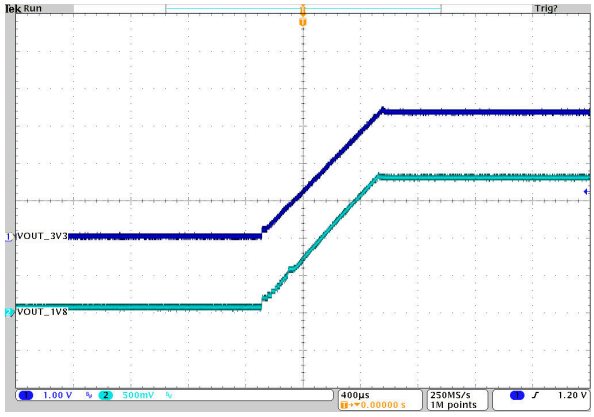


Figure 10-58. Scope Plot for Output Voltage Tracking

10.3.2 Synchronizing to an External Clock

The TPS62816-Q1 can be externally synchronized by applying an external clock on the MODE/SYNC pin. There is no need for any additional circuitry as long as the input signal meets the requirements given in the electrical specifications. The clock can be applied or removed during operation, allowing the user to switch from an externally defined fixed frequency to power save mode or to internal fixed-frequency operation. The value of the R_{CF} resistor must be chosen such that the internally defined frequency and the externally applied frequency are close to each other. This ensures a smooth transition from internal to external frequency and vice versa.

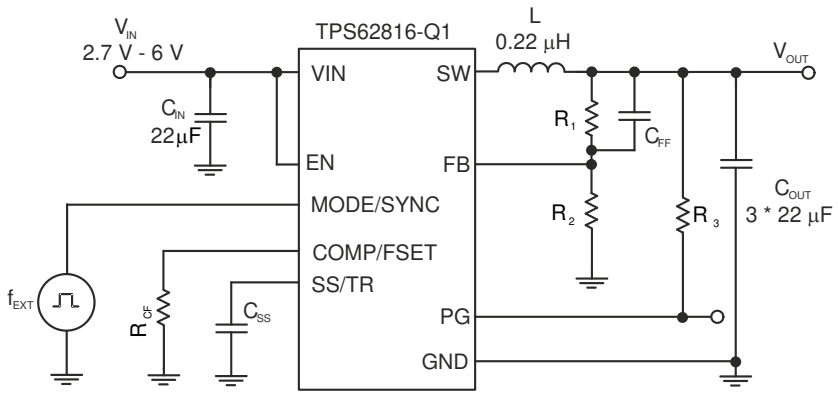
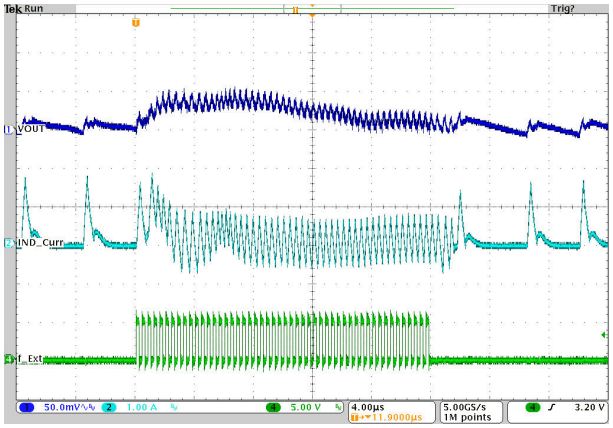
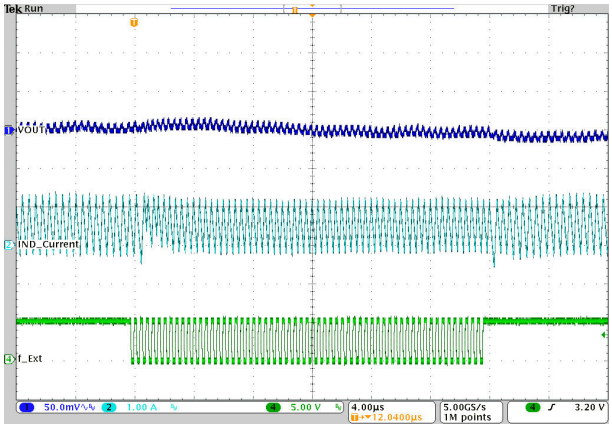


Figure 10-59. Schematic Using External Synchronization



V_{IN} = 5 V R_{CF} = 8.06 kΩ I_{OUT} = 0.2 A
V_{OUT} = 1.8 V f_{EXT} = 2.5 MHz

Figure 10-60. Switching from External Synchronization to Power Save Mode (PFM)



V_{IN} = 5 V R_{CF} = 8.06 kΩ I_{OUT} = 2 A
V_{OUT} = 1.8 V f_{EXT} = 2.5 MHz

Figure 10-61. Switching from External Synchronizaion to Internal Fixed Frequency

10.3.3 Compensation Settings

The TPS62816-Q1 offers two different compensations settings using the COMP/FSET pin. This allows the user to optimize the device regarding its transient response. For applications with no high requirements on transient response, a small output capacitance is desired for small size and low cost. In such cases, COMP1 must used so the TPS62816-Q1 is stable with as low as 32 µF of output capacitance. When the load is very dynamic, adding output capacitance improves transient response, but its effect is limited since this also reduces the cross-over frequency of the control loop. For such cases, COMP2 must be used as it increases the bandwidth, but requires a larger output capacitance for stable operation. The following scope plots are taken for the same conditions, but differ in the compensation setting. Since COMP2 demands 72-µF minimum output capacitance for stability, both plots were both taken with 72 µF on the output to allow the user to compare the results. One plot was taken for the COMP1 (R_{CF} = 8.06 kΩ) and one for the COMP2 (R_{CF} = 80.6 kΩ) compensation setting. The scope plots show that for the same output capacitance of 72 µF, the transient response for COMP2 is improved over the COMP1 setting.

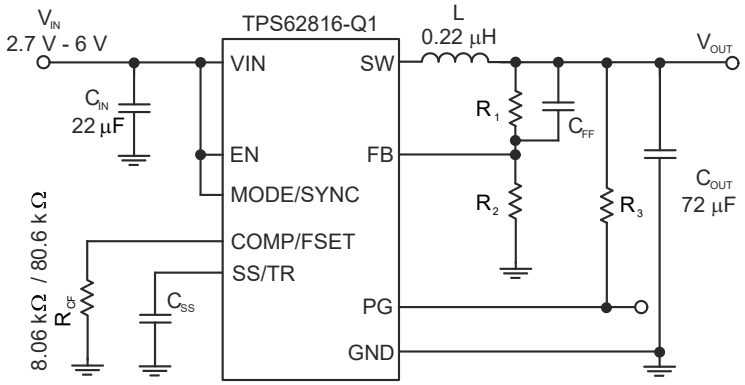
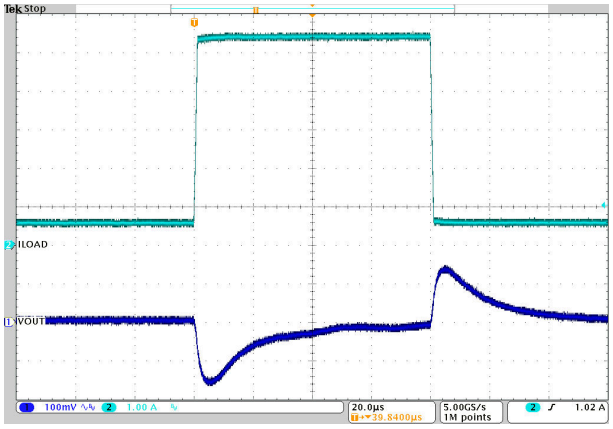
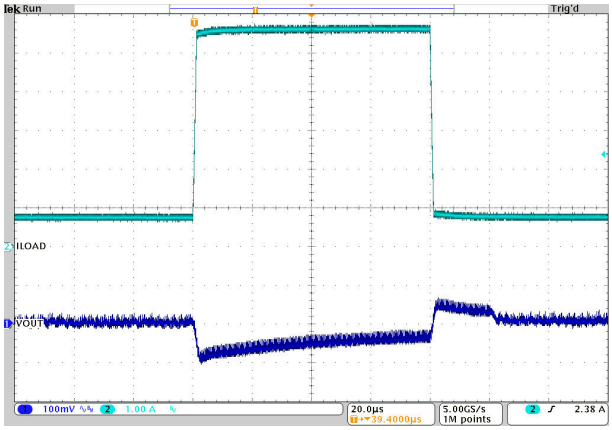


Figure 10-62. Schematic



V_{IN} = 5 V R_{CF} = 8.06 kΩ C_{OUT} = 72 µF
V_{OUT} = 1.8 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

Figure 10-63. Load Transient Response with Setting COMP1



V_{IN} = 5 V R_{CF} = 80.6 kΩ C_{OUT} = 72 µF
V_{OUT} = 1.8 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

Figure 10-64. Load Transient Response with Setting COMP2

11 Power Supply Recommendations

The TPS62816-Q1 device family does not have special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPS62816-Q1.

12 Layout

12.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS62816-Q1 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like the following:

- Poor regulation (both line and load)
- Stability and accuracy weaknesses
- Increased EMI radiation
- Noise sensitivity

See Section 12.2 for the recommended layout of the TPS62816-Q1, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances and narrow traces must be avoided. Loops that conduct an alternating current must outline an area as small as possible, since this area is proportional to the energy radiated.

Sensitive nodes like FB need to be connected with short wires and not nearby high dv/dt signals (for example, SW). Since they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin as well as the FB resistors, R_1 and R_2, must be kept close to the IC and connect directly to those pins and the system ground plane.

The package uses the pins for power dissipation. Thermal vias on the VIN and GND pins help to spread the heat into the PCB.

The recommended layout is implemented on the EVM and shown in the *TPS62816EVM-140 Evaluation Module User's Guide*.

12.2 Layout Example

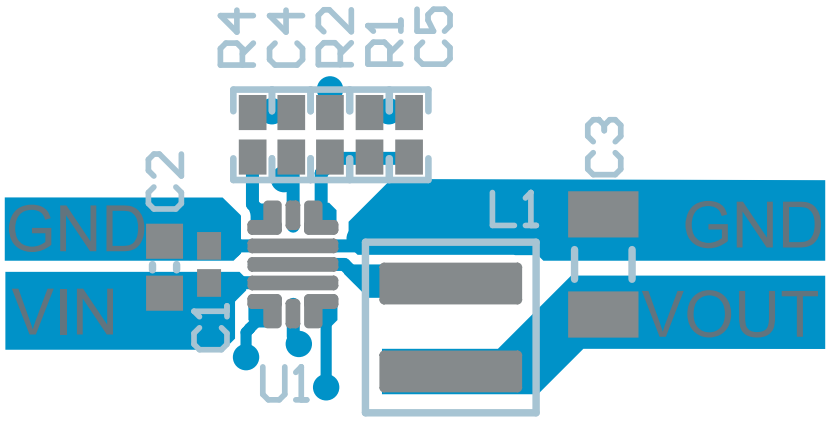


Figure 12-1. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *TPS62816EVM-140 Evaluation Module User's Guide*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62816QWRWYRQ1	Active	Production	VQFN-HR (RWY) | 9	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	816Q
TPS62816QWRWYRQ1.A	Active	Production	VQFN-HR (RWY) | 9	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	816Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

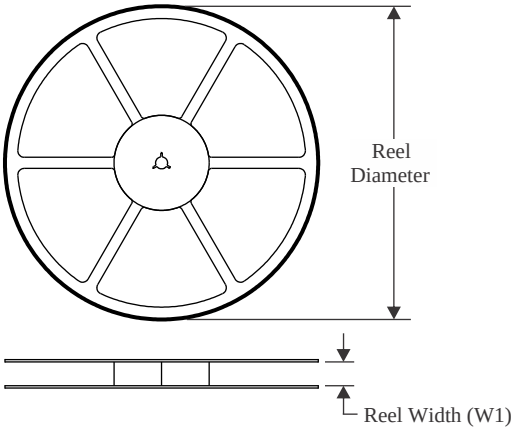
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

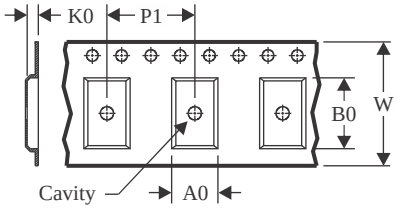
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

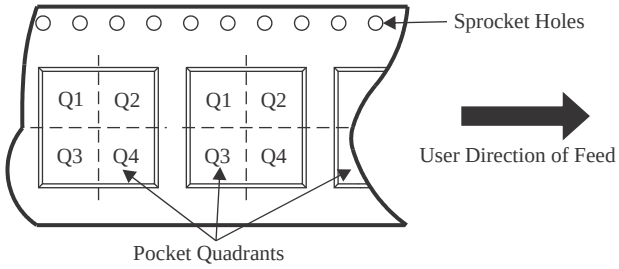


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

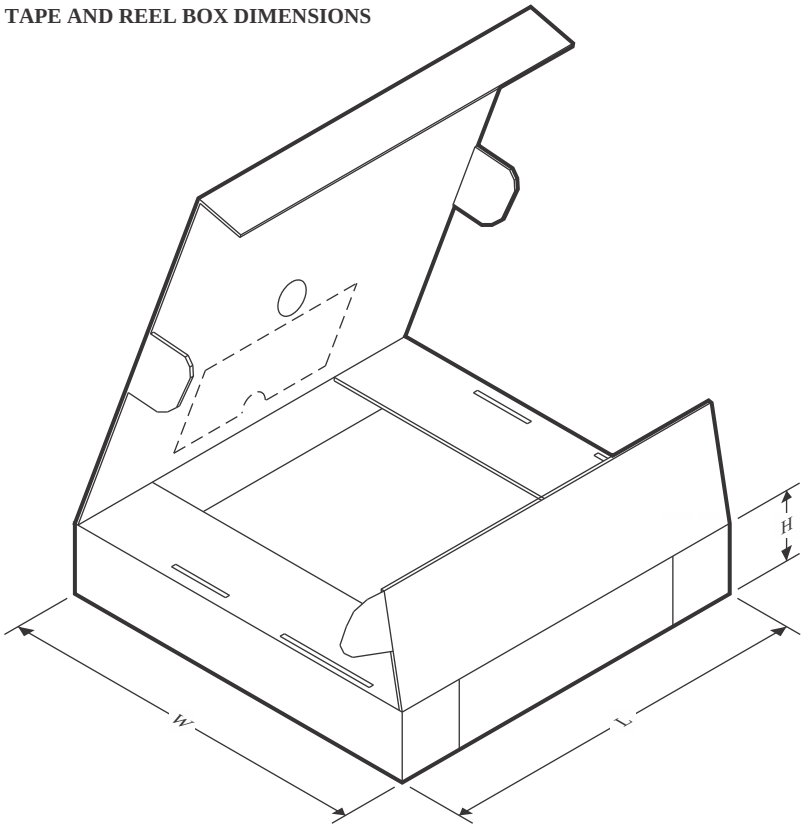
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62816QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62816QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

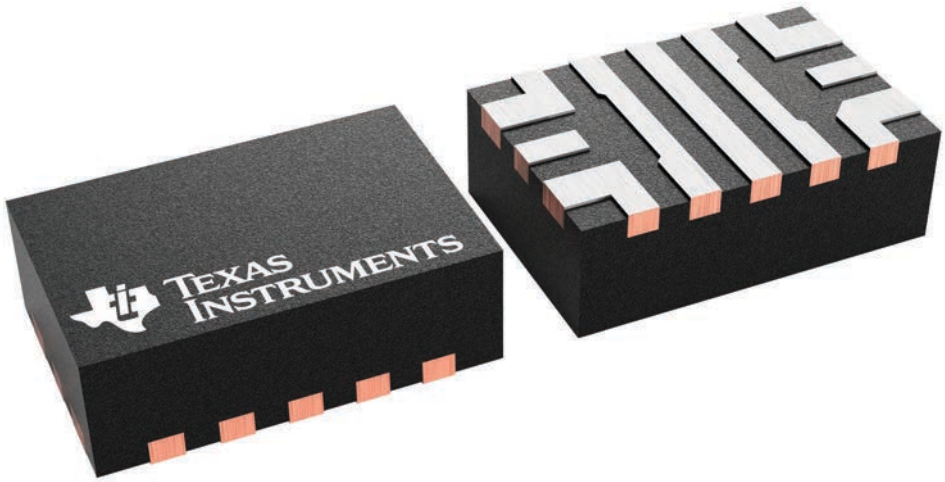
RWY 9

VQFN-HR - 1 mm max height

2 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



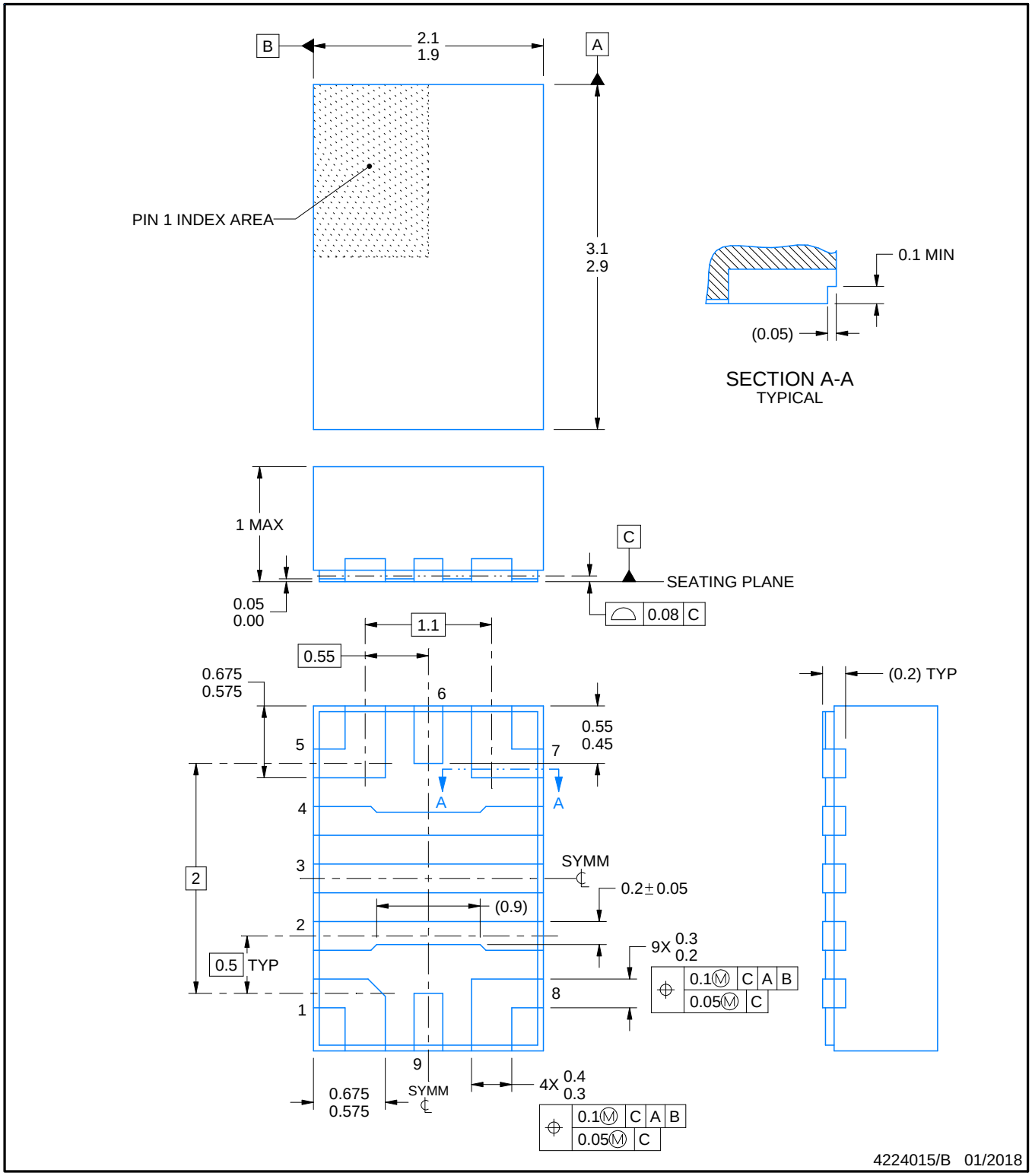
4226729/A

PACKAGE OUTLINE

RWY0009A

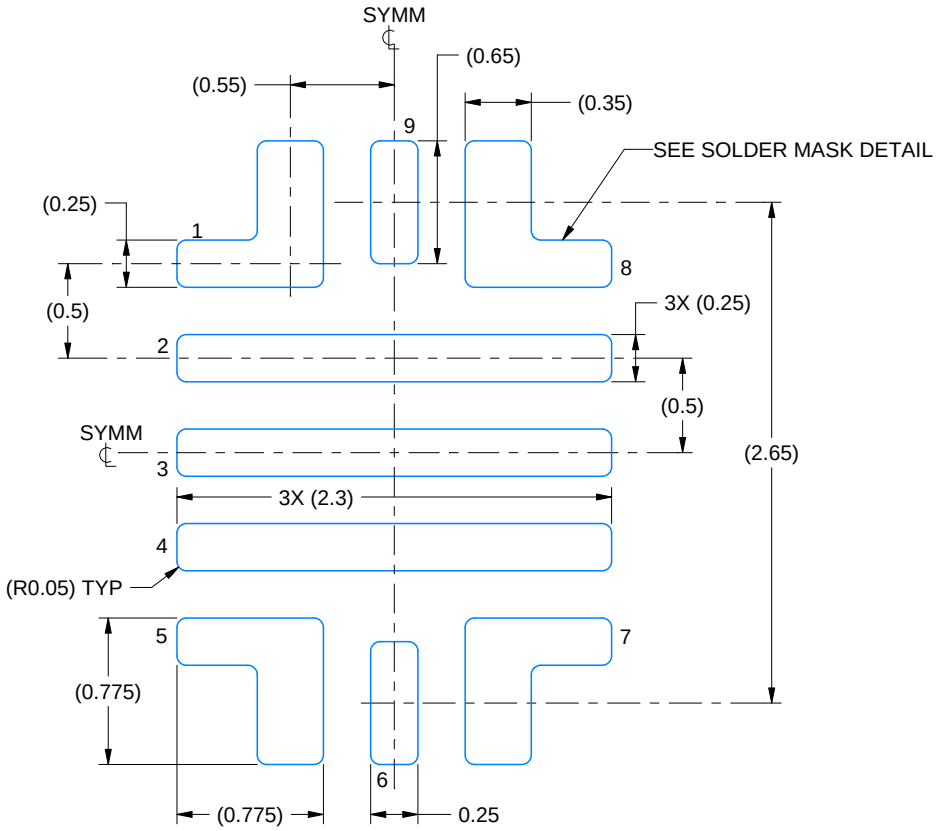
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

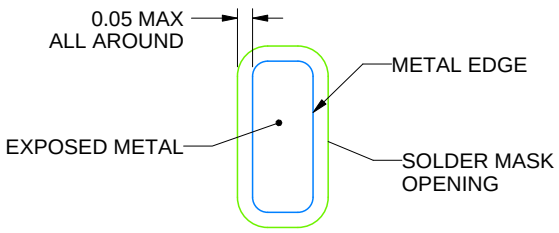


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



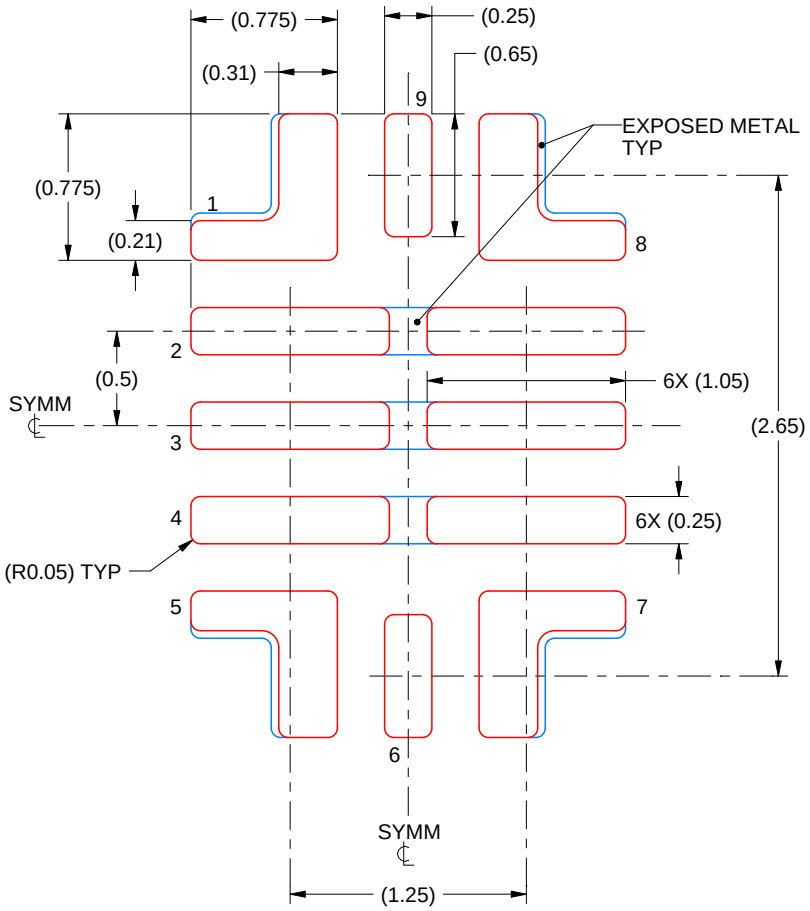
NON SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4224015/B 01/2018

NOTES: (continued)

3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
PADS 1, 5, 7 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

4224015/B 01/2018

NOTES: (continued)

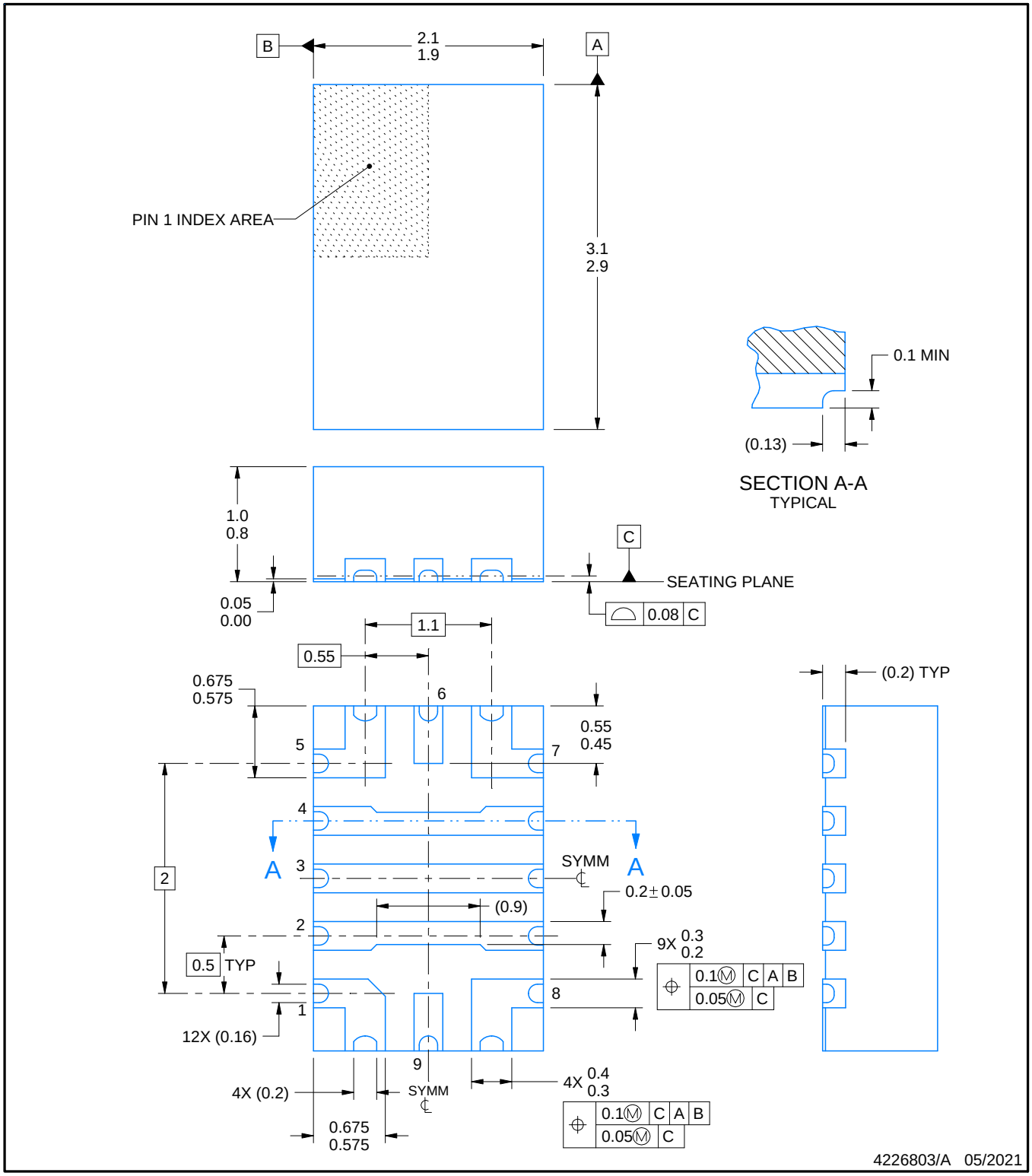
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RWY0009C

PACKAGE OUTLINE

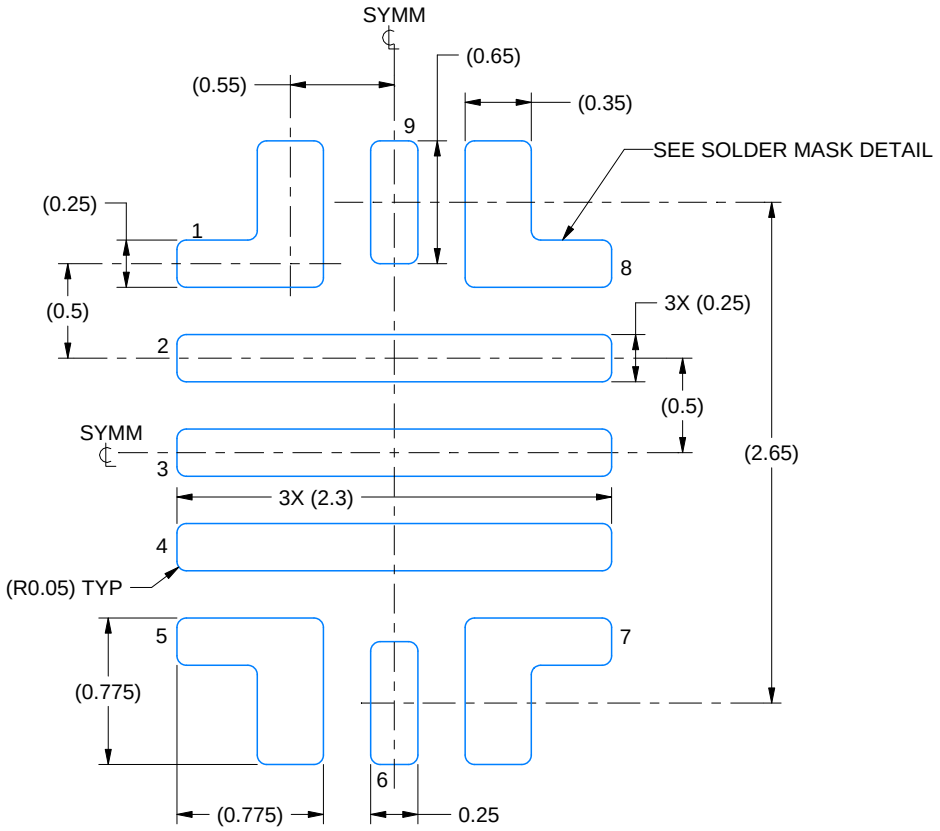
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

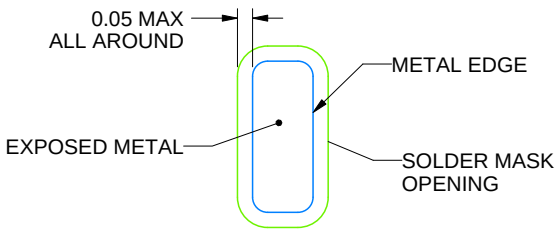


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



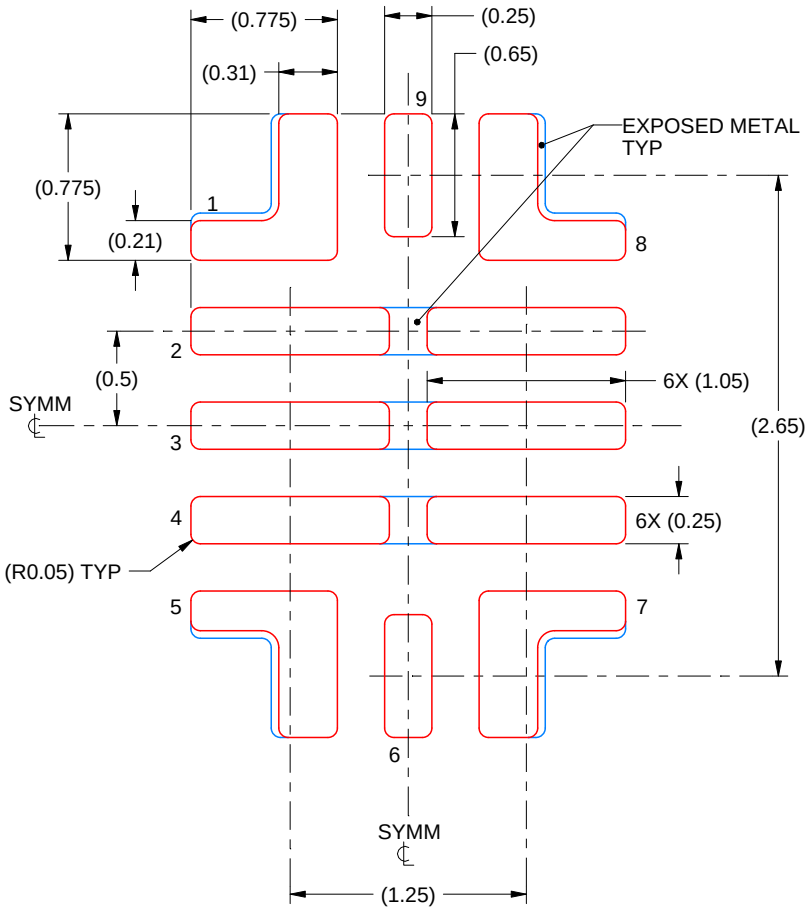
NON SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4226803/A 05/2021

NOTES: (continued)

3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
PADS 1, 5, 7 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

4226803/A 05/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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