TPS6240x-Q1 2.25-MHz 400-mA and 600-mA Dual Step-Down Converter

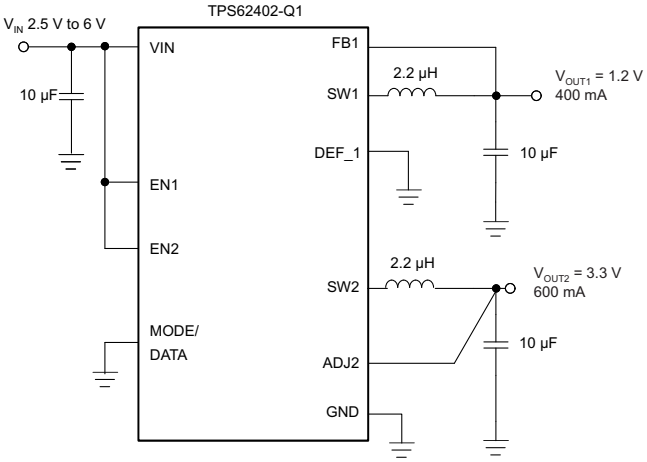
1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C operating junction temperature range
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C4B
- High efficiency—up to 95%
- V_{IN} Range from 2.5 V to 6 V
- 2.25-MHz Fixed-frequency operation
- Output current 400 mA and 600 mA
- Adjustable output voltage from 0.6 V to V_{IN}
- Pin selectable output voltage supports simple dynamic voltage scaling
- EasyScale™ optional one-pin serial interface
- Power-save mode at light load currents
- 180° Out-of-phase operation
- Output-voltage accuracy in PWM mode ±1%
- Typical 32-µA quiescent current for both converters
- 100% Duty cycle for lowest dropout

2 Applications

- Infotainment and cluster
- ADAS

Simplified Schematic



3 Description

The TPS6240x-Q1 family of devices are synchronous dual step-down DC-DC converters optimized for battery-powered portable applications and automotive systems. They provide two independent output voltage rails powered by rechargeable batteries or standard 3.3-V or 5-V voltage rail.

The EasyScale™ serial interface allows output-voltages modification during operation. The fixed-output-voltage versions, TPS62402-Q1, TPS62404-Q1, and TPS62405-Q1 support one-pin-controlled simple dynamic voltage scaling for low-power processors.

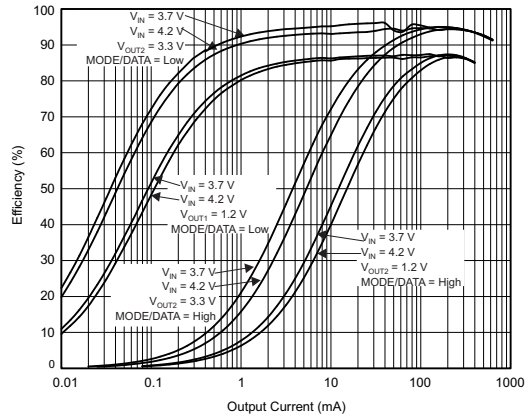
The TPS6240x-Q1 operates at 2.25-MHz fixed switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load-current range. For low-noise applications, one can force the devices into fixed-frequency PWM mode by pulling the MODE/DATA pin high. The shutdown mode reduces the current consumption to 1.2-µA, typical. The devices allow the use of small inductors and capacitors to achieve a small solution size.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62400-Q1	VSON (10)	3.00 mm × 3.00 mm
TPS62402-Q1		
TPS62404-Q1		
TPS62405-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

TPS62402-Q1 Efficiency versus Output Current, V_{OUT1} and V_{OUT2}



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2015) to Revision F	Page
• Changed TPS62404-Q1, OUT1 from DEF_1 = Low 1.575 V to DEF_1 = Low 1.2 V	4

Changes from Revision D (October 2014) to Revision E	Page
• Changed the *Handling Ratings* table to the *ESD Ratings* table and move storage temperature to the *Absolute Maximum Ratings* table	6
• Changed test conditions and MIN, TYP, and MAX values for the TPS62405-Q1 oscillator frequency in the *Switching Characteristics* table	8

Changes from Revision C (October 2014) to Revision D	Page
• Changed oscillator specification from 1.6 MHz to 2 MHz minimum switching frequency and to 1.7 MHz for $V_{IN} \leq 3$ V	8

Changes from Revision B (May 2013) to Revision C	Page
• Changed the data sheet to meet the new TI standard format	1
• Changed the V_{DEF_1H} and V_{DEF_1L} Test Conditions	7
• Changed f_{SW} 2.5 V ≤ V_{IN} ≤ 6 V MIN value From: 2 MHz to 1.6 MHz	8
• Added f_{SW} with Test Conditions 3.25 V ≤ V_{IN} ≤ 6 V	8

Changes from Revision A (March, 2013) to Revision B	Page
• Changed TPS62405-Q1, OUT1 from DEF_1 = High 1.9 V to DEF_1 = High 1.925 V and DEF_1 = Low 1.575 V to DEF_1 = Low 1.215 V. Changed OUT2 from Fixed default 5 V to Fixed default 3.35 V.	4
• Added the part number to the Device column of Table 1	17

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- Added 1.215 (default TPS62405-Q1) in row 16, Table 4 20
- Added part number to Table 4 20
- Removed TPS62405-Q1 from Table 4. 20
- Added 1.925 (default TPS62405-Q1) in row 31, Table 4. 20
- Added part number to row 31, Table 4 22
- Added part number to *Converter 1 Fixed Default Output-Voltage Setting* heading 24
- Added voltage for TPS62402-Q1 to Converter 1 Fixed for DEF_1 = low 24
- Changed voltage from 1.2 V to 1.215 V for Pin DEF_1 = low 24
- Added part number TPS62405-Q1 for Pin DEF_1 = high 24
- Added part number and voltage to *Converter 2 Fixed Default Output-Voltage Setting* section 24
- Changed TPS62405-Q1, V_{OUT2} default = 5 V to 3.35 V. 24

5 Device Comparison Table

PART NUMBER	DEFAULT OUTPUT VOLTAGE(1)			OUTPUT CURRENT	
TPS62400-Q1	V_{OUT1}	Adjustable		I_{OUT1}	400 mA
	V_{OUT2}			I_{OUT2}	600 mA
TPS62402-Q1	V_{OUT1}	Fixed default	DEF_1 = High 1.8 V	I_{OUT1}	400 mA
			DEF_1 = Low 1.2 V		
	V_{OUT2}	Fixed default 3.3 V		I_{OUT2}	600 mA
TPS62404-Q1	V_{OUT1}	Fixed default	DEF_1 = High 1.9 V	I_{OUT1}	400 mA
			DEF_1 = Low 1.2 V		
	V_{OUT2}	Fixed default 3.3 V		I_{OUT2}	600 mA
TPS62405-Q1	V_{OUT1}	Fixed default	DEF_1 = High 1.925 V	I_{OUT1}	400 mA
			DEF_1 = Low 1.215 V		
	V_{OUT2}	Fixed default 3.35 V		I_{OUT2}	600 mA

(1) Contact TI for other fixed-output-voltage options.

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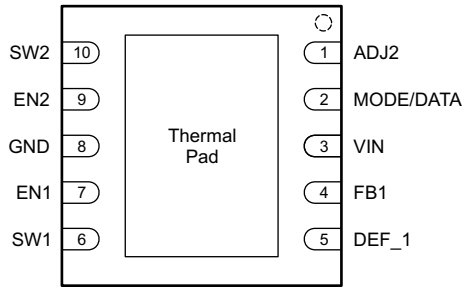
6 Pin Configuration and Functions

DRC Package
10-Pin VSON With Thermal Pad
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADJ2	1	I	Input to adjust output voltage of converter 2. In the adjustable-output version (TPS62400-Q1), an external resistor network must connect to this pin to set the V_{OUT2} output voltage between 0.6 V and V_{IN} (see Figure 6). In the fixed-output-voltage version (TPS62402-Q1, TPS62404-Q1, and TPS62405-Q1), this pin must connect directly to the output. If using the EasyScale interface-on converter 2, this pin must also connect directly to the output.
DEF_1	5	I	This pin defines the output voltage of converter 1. The pin acts either as analog input for output voltage setting via external resistors (TPS62400-Q1), or digital input to select between two fixed default output voltages (TPS62402-Q1, TPS62404-Q1, and TPS62405-Q1). For the TPS62400-Q1, an external resistor network must connect to this pin to adjust the default output voltage (see Figure 6). When using the fixed-output-voltage device options, this pin selects between two fixed default output voltages, see the *Device Comparison Table* .
EN1	7	I	Enable input for converter 1, active-high
EN2	9	I	Enable input for converter 2, active-high
FB1	4	I	Direct feedback voltage sense input of converter 1, connect directly to V_{OUT1}. An internal feedforward capacitor connects between this pin and the error amplifier. In the case of fixed-output-voltage versions or when using the EasyScale interface, this pin connects to an internal resistor divider network.
GND	8	—	GND for both converters; connect this pin to the thermal pad.
MODE/DATA	2	I/O	This pin has two functions: 1. Operation-mode selection: With low level, enables power-save mode where the device operates in PFM mode at light loads and automatically enters PWM mode at heavy loads. Pulling this PIN to high forces the device to operate in PWM mode over the whole load range. 2. EasyScale interface function: One-wire serial interface to change the output voltage of both converters. The pin has an open-drain output to provide an acknowledge condition if requested. The current into the open-drain output stage may not exceed 500 µA. The EasyScale interface is active if either EN1 or EN2 is high.
SW1	6	I/O	Switch pin of converter 1. Connect to inductor
SW2	10	I/O	Switch pin of converter 2. Connect to inductor
VIN	3	I	Input pin, connect to supply or battery voltage, 2.5 V to 6 V
Thermal pad		—	Connect to GND

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage[2]	VIN	–0.3	7	V
Voltage	EN, MODE/DATA, DEF_1	–0.3	V_{IN} + 0.3, ≤ 7	V
	SW1, SW2	–0.3	7	V
	ADJ2, FB1	–0.3	V_{IN} + 0.3, ≤ 7	V
Current	MODE/DATA		≤ 0.5	mA
Maximum operating junction temperature, $T_J$max			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 5, 6, and 10)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply voltage	2.5	6	V
	Output voltage range for adjustable voltage	0.6	V_{IN}	V
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS6240x-Q1 DRC (10 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	18.1	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	18.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

V_{IN} = 3.6 V, V_{OUT1} = V_{OUT2} = 1.8 V, EN1 = EN2 = V_{IN}, MODE = GND, L1 = L2 = 2.2 µH, C_{OUT1} = C_{OUT2} = 20 µF, T_J = –40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_{IN}	Input voltage range			2.5		6	V
I_Q	Operating quiescent current		One converter, no load on the output. PFM mode enabled (MODE/DATA = GND) device not switching, EN1 = 1 or EN2 = 1		19	29	µA
			Two converters, no load on the output. PFM mode enabled (MODE/DATA = GND) device not switching, EN1 = EN2 = 1		32	48	
			No load on the output, MODE/DATA = GND, for one converter, V_{OUTx} = 1.575 V(1)		23		
			No load on the output, MODE/DATA = V_{IN}, for one converter, V_{OUTx} = 1.575 V(1)		3.6		mA
I_{SD}	Shutdown current		EN1, EN2 = GND, V_{IN} = 3.6 V(2)		1.2	3	µA
			EN1, EN2 = GND, V_{IN} ramped from 0 V to 3.6 V(3)		0.1	1	
V_{UVLO}	Undervoltage lockout threshold		Falling		1.5	2.35	V
			Rising			2.4	
ENABLE EN1, EN2							
V_{IH}	High-level input voltage range, EN1, EN2			1.2		V_{IN}	V
V_{IL}	Low-level input voltage range, EN1, EN2			0		0.4	V
I_{IN}	Input bias current, EN1, EN2		EN1, EN2 = GND or V_{IN}		0.05	1	µA
DEF_1 INPUT							
V_{DEF_1H}	DEF_1 high-level digital input voltage range		TPS62402-Q1, TPS62404-Q1, TPS62405-Q1 only	0.9		V_{IN}	V
V_{DEF_1L}	DEF_1 low-level digital input voltage range			0		0.4	V
I_{IN}	Input bias current DEF_1		DEF_1 = GND or V_{IN}		0.01	1	µA
MODE/DATA							
V_{IH}	High-level input voltage range, MODE/DATA			1.2		V_{IN}	V
V_{IL}	Low-level input voltage range, MODE/DATA			0		0.4	V
I_{IN}	Input bias current, MODE/DATA		MODE/DATA = GND or V_{IN}		0.01	1	µA
V_{OH}	Acknowledge output voltage high		Open drain, through external pullup resistor			V_{IN}	V
V_{OL}	Acknowledge output voltage low		Open drain, sink current 500 µA	0		0.4	V
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on-resistance, converter 1,2		V_{IN} = V_{GS} = 3.6 V		280	620	mΩ
I_{LK_PMOS}	P-channel leakage current		V_{DS} = 6 V			1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance converter 1,2		V_{IN} = V_{GS} = 3.6 V		200	450	mΩ
$I_{LK_SW1/SW2}$	Leakage current into SW1 or SW2 pin		Includes N-channel leakage current, V_{IN} = open, V_{SW} = 6 V, EN = GND(4)		6	7.5	µA
I_{LIMF}	Forward current limit PMOS and NMOS	V_{OUT1}	2.5 V ≤ V_{IN} ≤ 6 V	0.68	0.8	0.92	A
		V_{OUT2}		0.85	1	1.15	
T_{SD}	Thermal shutdown		Increasing junction temperature		150		ºC
	Thermal shutdown hysteresis		Decreasing junction temperature		20		ºC
OUTPUT							
V_{OUTx}	Adjustable output 1 or output 2 voltage range			0.6		V_{IN}	V
V_{ref}	Reference voltage				600		mV

(1) Device is switching with no load on the output, L1 = L2 = 3.3 µH, value includes losses of the coil.
(2) These values are valid after enabling the device one time (EN1 or EN2 = high) and maintaining supply voltage V_{IN}.
(3) These values are valid when the device is disabled (EN1 and EN2 low) and supply voltage V_{IN} is powered up. The values remain valid until enabling the device the first time (EN1 or EN2 = high). After the first enable, Note 3 becomes valid.
(4) An internal resistor of 1 MΩ connects pins SW1 and SW2 to GND.

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Electrical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT1} = V_{OUT2} = 1.8 V, EN1 = EN2 = V_{IN}, MODE = GND, L1 = L2 = 2.2 µH, C_{OUT1} = C_{OUT2} = 20 µF, T_J = –40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUTx(PFM)}$	DC output voltage accuracy adjustable and fixed output voltage(5)	Voltage positioning active, MODE/DATA = GND, device operating in PFM mode, V_{IN} = 2.5 V to 5 V(6)(7)	–1.5%	1%	2.5%	
$V_{OUTx(PWM)}$		MODE/DATA = GND; device operating in PWM mode, V_{IN} = 2.5 V to 6 V(7)	–1%	0%	1%	
		V_{IN} = 2.5 V to 6 V, MODE/DATA = V_{IN} , Fixed PWM operation, 0 mA < I_{OUT1} < 400 mA ; 0 mA < I_{OUT2} < 600 mA(8)	–1%	0%	1%	
	DC output voltage load regulation	PWM operation mode			0.5	%/A

(5) Output voltage specification does not include tolerance of external voltage-programming resistors.
(6) Configuration L1 or L2 typ. 2.2 µH, C_{OUTx} typ 20 µF. See parameter measurement information, the output voltage ripple in PFM mode depends on the effective capacitance of the output capacitor; larger output capacitors lead to tighter output voltage tolerance.
(7) In power-save mode, the device typically enters PWM operation at I_{PSM} = V_{IN} / 32 Ω.
(8) For V_{OUTx} > 2 V, V_{IN} min = V_{OUTx} + 0.5 V

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
INTERFACE TIMING						
t_{Start}	Start time		2			µs
t_{H_LB}	High-time low bit, logic 0 detection	Signal level on MODE/DATA pin is > 1.2 V	2		200	µs
t_{L_LB}	Low-time low bit, logic 0 detection	Signal level on MODE/DATA pin < 0.4 V	2 x t_{H_LB}		400	µs
t_{L_HB}	Low-time high bit, logic 1 detection	Signal level on MODE/DATA pin < 0.4 V	2		200	µs
t_{H_HB}	High-time high bit, logic 1 detection	Signal level on MODE/DATA pin is > 1.2 V	2 x t_{L_HB}		400	µs
t_{EOS}	End of stream		2			µs
t_{ACKN}	Duration of acknowledge condition (MODE/DATE line pulled low by the device)	V_{IN} 2.5 V to 6 V	400		520	µs
t_{valACK}	Acknowledge valid time				2	µs
$t_{timeout}$	Time-out for entering power-save mode	MODE/DATA pin changes from high to low			520	µs

7.7 Switching Characteristics

V_{IN} = 3.6 V, V_{OUT1} = V_{OUT2} = 1.8 V, EN1 = EN2 = V_{IN}, MODE = GND, L1 = L2 = 2.2 µH, C_{OUT1} = C_{OUT2} = 20 µF, T_J = –40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_{SW}	Oscillator frequency	2.5 V ≤ V_{IN} ≤ 6 V; TPS62400-Q1 adjustable version(1)	1.7	2.3	2.7	MHz
		3.0 V ≤ V_{IN} ≤ 6 V; TPS62400-Q1, TPS62402-Q1, TPS62404-Q1(1)	2	2.3	2.7	
		3.6 V ≤ V_{IN} ≤ 5.1 V; TPS62405-Q1 fixed output voltage version(1)	2.06	2.2	2.49	
OUTPUT						
$t_{Start\ up}$	Start-up time	Activation time to start switching(2)		170		µs
t_{Ramp}	V_{OUTx} ramp-up time	Time to ramp from 5% to 95% of V_{OUTx}		750		µs

(1) For V_{OUTx} > 2 V, V_{IN} min = V_{OUTx} + 0.5 V
(2) This time is valid if one converter turns from shutdown mode (EN2 = 0) to active mode (EN2 = 1) with the other converter already enabled (for example, EN1 = 1). In case both converters are turned from shutdown mode (EN1 and EN2 = 0) to active mode (EN1 and/or EN2 = 1), a typical value of typ 80 µs for ramp up of internal circuits must be added. After t_{Start}, the converter starts switching and ramps V_{OUTx}.

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7.8 Typical Characteristics

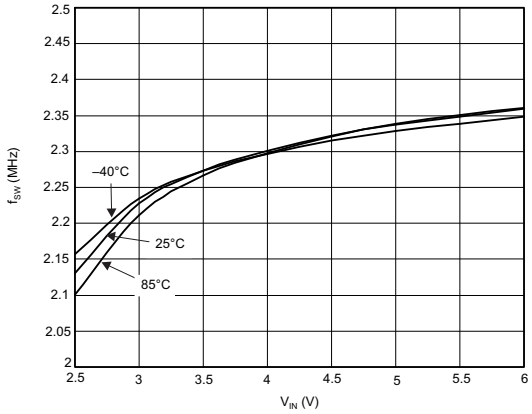

Figure 1. f_{SW} versus V_{IN}

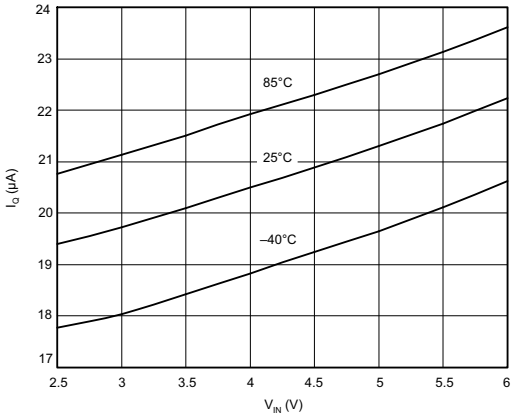

Figure 2. I_Q for One Converter, Not Switching

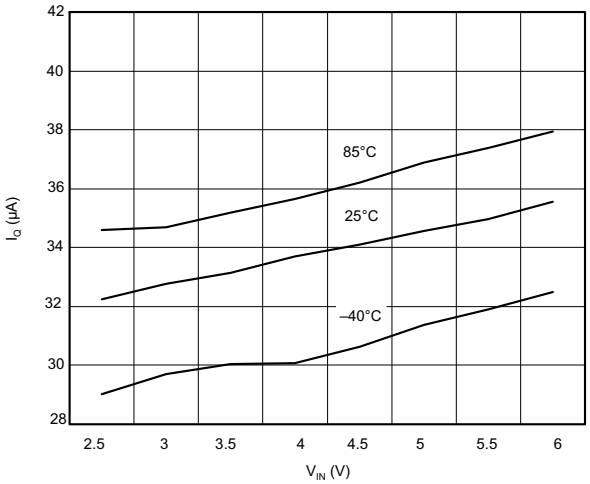

Figure 3. I_Q for Both Converters, Not Switching

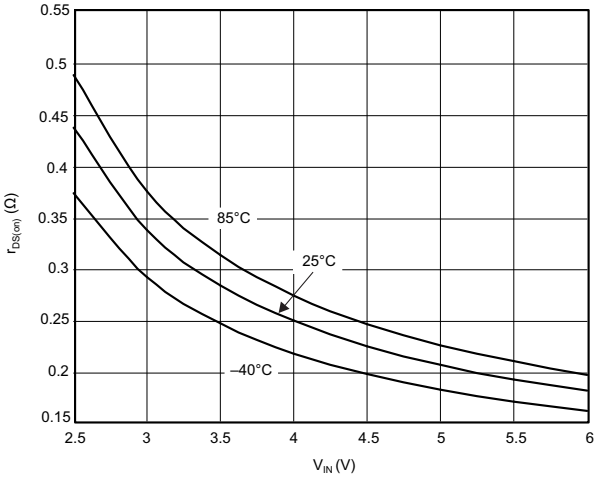

Figure 4. $r_{DS(on)}$ PMOS versus V_{IN}

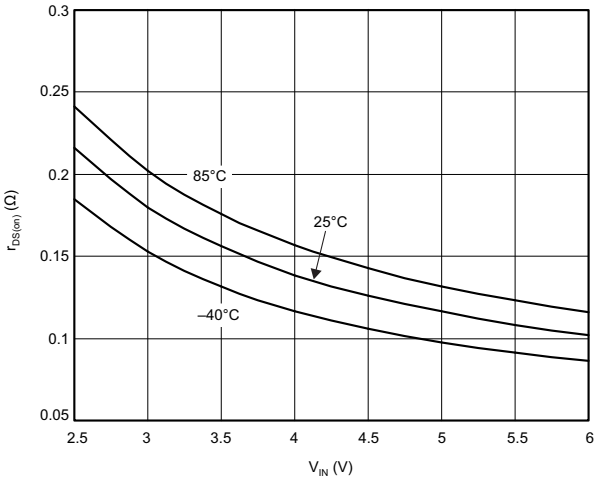

Figure 5. $r_{DS(on)}$ NMOS versus V_{IN}

8 Parameter Measurement Information

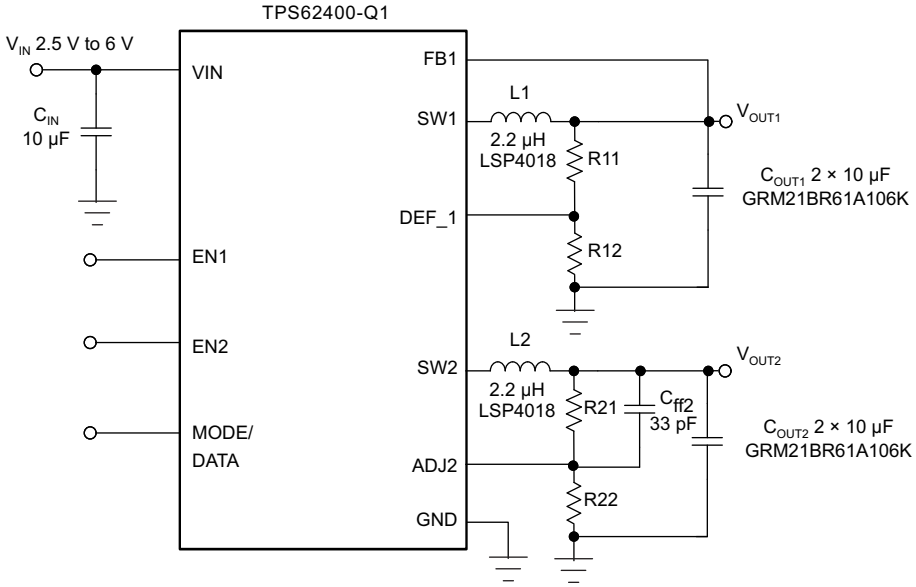

Figure 6. Measurement Circuit

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9 Detailed Description

9.1 Overview

The TPS62400-Q1 device includes two synchronous step-down converters. The converters operate with typically 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. With the power-safe mode enabled, the converters automatically enter power-save mode at light load currents and operate in PFM (pulse frequency modulation).

During PWM operation, the converters use a unique fast-response voltage-mode controller scheme with input-voltage feedforward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch turns on and the inductor current ramps up until the comparator trips and the control logic turns off the switch.

Each converter integrates two current limits, one in the P-channel MOSFET and another one in the N-channel MOSFET. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET turns off and the N-channel MOSFET turns on. If the current in the N-channel MOSFET is above the N-MOS current limit threshold, the N-channel MOSFET remains on until the current drops below its current limit.

The two DC-DC converters operate synchronized to each other. A 180° phase shift between converter 1 and converter 2 decreases the input rms current.

9.1.1 Converter 1

In the adjustable output-voltage version, TPS62400-Q1 device, one can set the converter 1 default output voltage with an external resistor network on the DEF_1 pin, which operates as an analog input. In this case, one can set the output voltage in the range of 0.6 V to VIN V. The FB1 pin must directly connect to the converter 1 output voltage V_{OUT1}. It feeds back the output voltage directly to the regulation loop.

One can also change the output voltage of converter 1 with the EasyScale serial Interface. This makes the device very flexible for output-voltage adjustment. In this case, the device uses an internal resistor network.

In the fixed default output voltage version, TPS62402-Q1 for example, the DEF_1 pin configuration is as a digital input. Converter 1 defaults to 1.2 V or 1.8 V, depending on the level of the DEF_1 pin. If DEF_1 is low, the default is 1.2 V; if high, the default is 1.8 V. With the EasyScale interface, one can change the output voltage for each DEF_1 pin condition (high or low).

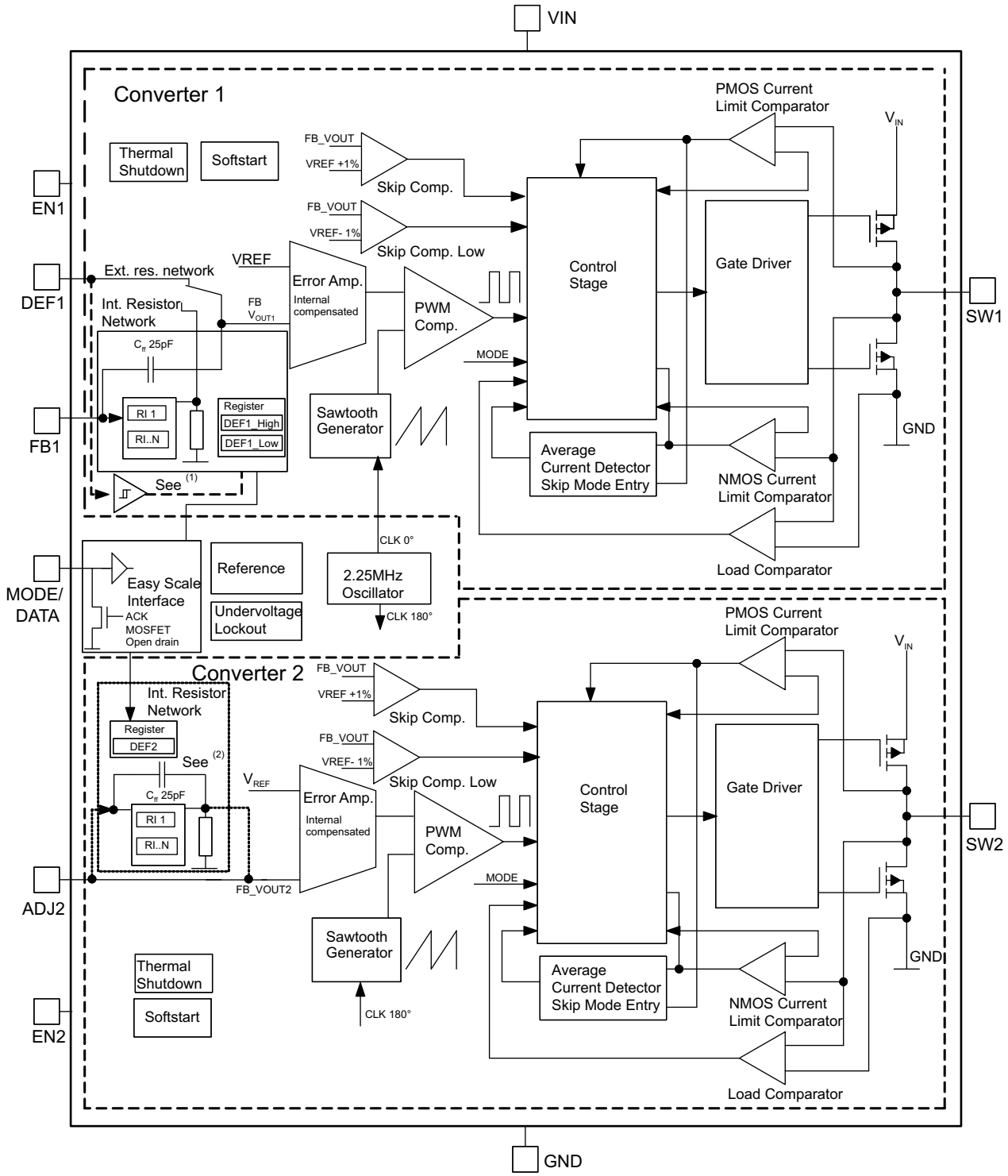
9.1.2 Converter 2

In the adjustable output-voltage version, TPS62400-Q1 device, an external resistor divider connected to ADJ2 pin sets the converter 2 output voltage. The converter uses an external feedforward capacitor of 33 pF.

For example, in the fixed output-voltage version TPS62402-Q1, the fixed default output voltage is fixed to 3.3 V. In this case, the ADJ2 pin must connect directly to the converter 2 output voltage, V_{OUT2}.

It is also possible to change the output voltage of converter 2 via the EasyScale interface. In this case, the ADJ2 pin must connect directly to converter 2 output voltage V_{OUT2}, with no connection of external resistors permitted.

9.2 Functional Block Diagram



(1) In the fixed output-voltage version, the DEF_1 pin connects to an internal digital input and disconnects from the error amplifier.

(2) To set the output voltage of converter 2 through the EasyScale™ interface, the ADJ2 pin must directly connect to V_{OUT2}.

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9.3 Feature Description

9.3.1 Enable

The device has a separate EN pin for each converter to start up each converter independently. If EN1 or EN2 is set to high, the corresponding converter starts up with soft start.

Pulling EN1 and EN2 pin low forces the device into shutdown, with a shutdown quiescent current of typically 1.2 µA. In this mode, the P- and N-channel MOSFETs turn off and the entire internal control circuitry switches off. For proper operation, terminate the EN1 and EN2 pins, do not leave them floating.

9.3.2 DEF_1 Pin Function

The DEF_1 pin, dedicated to converter 1, makes the output voltage selection very flexible to support dynamic voltage management.

Depending on the device version, this pin works either as:

1. Analog input for adjustable output voltage setting (TPS62400-Q1):
   – Connecting an external resistor network to this pin adjusts the default output voltage to any value starting from 0.6 V to V_{IN}.
2. Digital input for fixed default output voltage selection (TPS62402-Q1 for example):
   – Having this pin tied to a low level sets the output voltage according to the value in register REG_DEF_1_Low. The default voltage is 1.2 V. Having the pin tied to a high level sets the output voltage according to the value in register REG_DEF_1_High. The default value in this case is 1.8 V. The level of the DEF_1 pin selects between the two registers, REG_DEF_1_Low and REG_DEF_1_High, for the output-voltage setting. One can change the content of each register (and therefore output voltage) individually through the EasyScale interface. This makes the device very flexible in terms of output voltage setting; see Table 4.

9.3.3 180° Out-of-Phase Operation

In PWM mode, the converters operate with a 180° turnon phase shift of the PMOS (high side) transistors. This prevents the high-side switches of both converters from turning on simultaneously, and therefore smooths the input current. This feature reduces the surge current drawn from the supply.

9.3.4 Short-Circuit Protection

Both outputs are short-circuit protected with maximum output current = I_{LIMF}(P-MOS and N-MOS). Once the PMOS switch reaches its current limit, it turns off and the NMOS switch turns on. The PMOS only turns on again once the current in the NMOS decreases below the NMOS current limit.

9.3.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs turn off. The device continues its operation when the junction temperature falls below the thermal-shutdown hysteresis.

9.3.6 EasyScale Interface: One-Pin Serial Interface for Dynamic Output-Voltage Adjustment

9.3.6.1 General

The EasyScale interface is a simple but very flexible one-pin interface to configure the output voltage of both DC-DC converters. A master-slave structure is the basis of the interface, where the master is typically a microcontroller or application processor. Figure 9 and Table 3 give an overview of the protocol. The protocol consists of a device-specific address byte and a data byte. The device-specific address byte is fixed to 4E hex. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the request-for-acknowledge condition. The acknowledge condition only applies after correct reception of the protocol.

The advantage of the EasyScale interface compared to other one-pin interfaces is that its bit detection is to a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7 kb/s and up to 160 kb/s. Furthermore, the interface shares the MODE/DATA pin and requires no additional pin.

Feature Description (continued)

9.3.6.2 Protocol

Transmission of all bits is MSB first and LSB last. Figure 10 shows the protocol without the acknowledge request (bit RFA = 0) and Figure 11 shows the protocol with the acknowledge request (bit RFA = 1).

Prior to both bytes, device address byte and data byte, one must apply a start condition. For this, pull the MODE/DATA pin high for at least t_{Start} before the bit transmission starts with the falling edge. In case the MODE/DATA line was already at a high level (forced PWM mode selection), the device requires no application of a start condition prior to the device address byte.

Close the transmission of each byte with an end-of-stream condition for at least t_{EOS}.

9.4 Device Functional Modes

9.4.1 Power-Save Mode

Setting the MODE/DATA pin to low for both converters enables power-save mode. If the load current of a converter decreases, this converter enters power-save-mode operation automatically. The transition of a converter to power-save mode is independent from the operating condition of the other converter. During power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage in PFM mode to typically 1% above nominal V_{OUTx}. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

In order to optimize the converter efficiency at light load, the device monitors average inductor current. The device changes from PWM mode to power-save mode if in PWM mode the inductor current falls below a certain threshold. The typical output current threshold, which one can calculate using Equation 1 for each converter, depends on V_{IN}.

Equation 1: Average output current threshold to enter PFM mode

$$I_{OUTx_PFM_enter} = \frac{V_{IN}}{32\ \Omega} \tag{1}$$

Equation 2: Average output current threshold to leave PFM mode

$$I_{OUTx_PFM_leave} = \frac{V_{IN}}{24\ \Omega} \tag{2}$$

To keep the output-voltage ripple in power-save mode low, a single threshold comparator (skip comparator) monitors the output voltage. As the output voltage falls below the skip-comparator threshold (skip comp) of 1% above nominal V_{OUTx}, the corresponding converter starts switching for a minimum time period of typically 1 µs and provides current to the load and the output capacitor. Therefore, the output voltage increases and the device maintains switching until the output voltage trips the skip comparator threshold (skip comp) again. At this moment, all switching activity stops and the quiescent current reduces to minimum. The output capacitor supplies the load until the output voltage has dropped below the threshold again. Hereupon, the device starts switching again.

The converter leaves power-save mode and enters PWM mode if the output current exceeds the $I_{OUT_PFM_leave}$ current or if the output voltage falls below a second comparator threshold, called the skip-comparator-low (Skip Comp Low) threshold. This skip-comparator-low threshold is 2% below nominal V_{OUTx} and enables a fast transition from power-save mode to PWM mode during a load step.

Power-save mode typically reduces the quiescent current to 19 µA for one converter and 32 µA for both converters active. This single-skip comparator threshold method in power-save mode results in a very low output-voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing output capacitor values minimizes the output ripple. One can disable the power-save mode by setting the MODE/DATA pin to high. Both converters then operate in fixed PWM mode. Power-save mode enable or disable applies to both converters.

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Device Functional Modes (continued)

9.4.1.1 Dynamic Voltage Positioning

This feature reduces the voltage under- and overshoots at load steps from light to heavy load and from heavy to light. Power-save-mode operation activates dynamic voltage positioning and provides more headroom for both the voltage drop at a load step and the voltage increase when a load is switched off, which improves load-transient behavior.

At light loads, in which the converter operates in PFM mode, the output voltage regulation is typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage drops until it reaches the skip comparator low threshold set to 2% below the nominal value and enters PWM mode. During a load transition from heavy load to light load, the device also minimizes voltage overshoot because of active regulation turning on the N-channel switch.

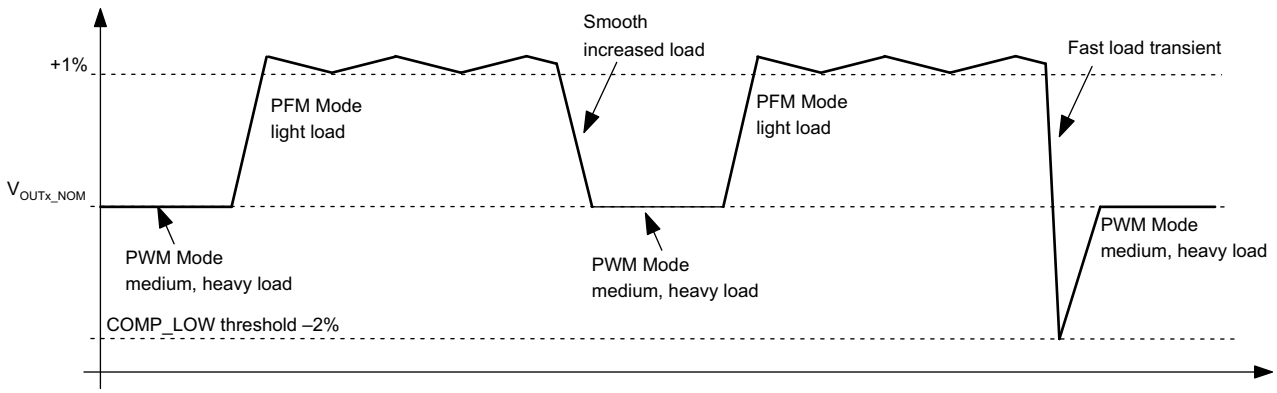

Figure 7. Dynamic Voltage Positioning

9.4.1.2 Soft Start

The two converters have an internal soft-start circuit that limits the inrush current during startup. Figure 8 shows control of the output-voltage ramp-up during soft start. The device is able to start into a pre-biased output capacitor.

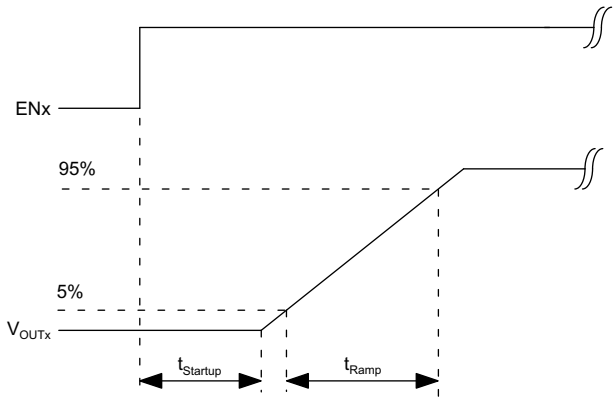

Figure 8. Soft Start

9.4.1.3 100% Duty-Cycle Low-Dropout Operation

The converters offer a low input-to-output voltage difference while still maintaining operation with the use of the 100% duty-cycle mode. In this mode, the P-channel switch is constantly on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery-voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, which one can calculate as:

$$V_{INmin} = V_{OUTxmax} + I_{OUTxmax} \times \left(r_{DS(on)max} + R_L\right)$$

Device Functional Modes (continued)

with

- $I_{OUTxmax}$ = maximum output current plus inductor ripple current
- $r_{DS(on)max}$ = maximum P-channel switch $r_{DS(on)}$
- R_L = dc resistance of the inductor
- $V_{OUTxmax}$ = nominal output voltage plus maximum output-voltage tolerance (3)

With decreasing load current, the device automatically switches into pulse-skipping operation, in which the power stage operates intermittently based on load demand. Running cycles periodically minimizes the switching losses, and the device runs with a minimum quiescent current, maintaining high efficiency.

9.4.1.4 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunction at low input voltages and from excessive discharge of the battery, and disables the converters. The undervoltage lockout threshold is typically 1.5 V and a maximum of 2.35 V. In case the interface overwrites the default register values, the new values in the registers REG_DEF_1_High, REG_DEF_1_Low and REG_DEF_2 remain valid as long the supply voltage does not fall below the undervoltage lockout threshold, independent of disabling of the converters.

9.4.2 Mode Selection

The MODE/DATA pin allows mode selection between forced PWM mode and power-save mode for both converters. Furthermore, this pin is a multipurpose pin and provides (besides mode selection) a one-pin interface to receive serial data from a host to set the output voltage, as described in the *EasyScale Interface* section.

Connecting this pin to GND enables the automatic PWM and power-save-mode operation. The converters operate in fixed-frequency PWM mode at moderate-to-heavy loads, and in the PFM mode during light loads, maintaining high efficiency over a wide load-current range.

Pulling the MODE/DATA pin high forces both converters to operate constantly in the PWM mode, even at light load currents. The advantage is that the converters operate with a fixed frequency, allowing simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

In the case of changing the operation mode from forced PWM mode (MODE/DATA = high) to power-save mode (MODE/DATA = 0), enabling the power-save mode occurs after a delay time of $t_{timeout}$, which is 520 µs maximum.

Setting the MODE/DATA to 1 enables forced-PWM-mode operation immediately.

9.5 Programming

9.5.1 Addressable Registers

Three registers with a data content of five bits are addressable. With 5-bit data content, 32 different values for each register are available. Table 1 shows the addressable registers to set the output voltage when the DEF_1 pin works as a digital input. In this case, converter 1 has a related register for each DEF_1 pin condition, and one register for converter 2. A high or low condition on pin DEF_1 (TPS62402-Q1, TPS62404-Q1, and TPS62405-Q1) selects either the content of register REG_DEF_1_High or REG_DEF_1_Low, thus setting the output voltage of converter 1 according to the values in Table 4.

Table 2 shows the addressable registers if the DEF_1 pin acts as an analog input with external resistors connected. In this case, one register is available for each converter. The values in Table 5 set the output voltage of converter 1. Table 6 shows the available voltages for converter 2. Use of a precise internal resistor divider network to generate these output voltages makes external resistors unnecessary (less board space) and provides higher output-voltage accuracy. Enabling at least one of the converters (EN1 or EN2 is high) activates the interface. After the start-up time t_{Start} (170 µs), the interface is ready for data reception.

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Programming (continued)

Table 1. Addressable Registers for Default Fixed-Output Voltage Options (PIN DEF_1 = Digital Input)

DEVICE	REGISTER	DESCRIPTION	DEF_1 PIN	A1	A0	D4	D3	D2	D1	D0
TPS62402-Q1, TPS62404-Q1, TPS62405-Q1	REG_DEF_1_High	Converter 1 output voltage setting for DEF_1 = High condition. The content of the register is active with the DEF_1 pin high.	High	0	1	Output voltage setting, see Table 4				
	REG_DEF_1_Low	Converter 1 output voltage setting for DEF_1 = Low condition.	Low	0	0	Output voltage setting, see Table 4				
	REG_DEF_2	Converter 2 output voltage	Not applicable	1	0	Output voltage setting, see Table 6				
		Do not use		1	1					

Table 2. Addressable Registers for Adjustable-Output Voltage Options (PIN DEF_1 = Analog Input)

DEVICE	REGISTER	DESCRIPTION	A1	A0	D4	D3	D2	D1	D0
TPS62400-Q1	REG_DEF_1_High	Not available							
	REG_DEF_1_ Low	Converter 1 output-voltage setting	0	0	See Table 5				
	REG_DEF_2	Converter 2 output voltage	1	0	See Table 6				
		Do not use	1	1					

9.5.1.1 Bit Decoding

The bit detection is based on a PWM scheme, where the criterion is the relation between the low time and high time of the low or high bit (t_{L_xB} and t_{H_xB}). Bit detection can be simplified to:

High bit: $t_{H_HB} > t_{L_HB}$, but with t_{H_HB} at least 2× t_{L_HB}, see Figure 9.

Low bit: $t_{L_LB} > t_{H_LB}$, but with t_{L_LB} at least 2× t_{H_LB}, see Figure 9.

The bit detection starts with a falling edge on the MODE/DATA pin and ends with the next falling edge. Detection of a 0 or 1 depends on the relation between t_{L_xB} and t_{H_xB}.

9.5.1.2 Acknowledge

The device only applies the acknowledge condition if all of the following occurs:

- A set RFA bit requests an acknowledge
- The transmitted device address matches with the device address of the device
- Correct reception of 16 bits occurred

In this case, the device turns on the internal ACKN-MOSFET and pulls the MODE/DATA pin low for the time t_{ACKN}, which is 520 µs maximum. The acknowledge condition is valid after an internal delay time t_{valACK}. This means the internal ACKN-MOSFET turns on after t_{valACK}, on detection of the last falling edge of the protocol. The master controller keeps the line low during this time.

The master device can detect the acknowledge condition with its input by releasing the MODE/DATA pin after t_{valACK} and reading back a 0.

In case of an invalid device address, or not-correctly-received protocol, application of a no-acknowledge condition does not occur; thus, the internal MOSFET does not turn on, and the external pullup resistor pulls the MODE/DATA pin high after t_{valACK}. One can use the MODE/DATA pin again after the acknowledge condition ends.

NOTE

The master device must have an open-drain output in order to request the acknowledge condition.

In case of a push-pull output stage, TI recommends using a series resistor in the MODE/DATA line to limit the current to 500 µA in case of an accidentally requested acknowledge, to protect the internal ACKN-MOSFET.

9.5.1.3 Mode Selection

Use of the MODE/DATA pin for two functions, interface and mode selection, necessitates a determination of when to decode the bit stream or to change the operation mode.

The device enters forced PWM mode operation immediately whenever the MODE/DATA pin turns to high level. The device also stays in forced PWM mode during the entire protocol reception time.

With a falling edge on the MODE/DATA pin, the device starts bit decoding. If the MODE/DATA pin stays low for at least $t_{timeout}$, the device gets an internal time-out and enables power-save-mode operation.

The device ignores a protocol sent within this time because the first interpretation of a falling edge for the mode change is at the start of the first bit. In this case, TI recommends sending the protocol first, and then changing to power-save mode at the end of the protocol.

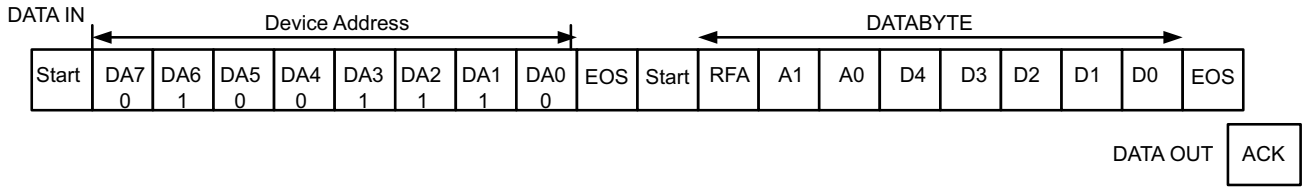

Figure 9. EasyScale Protocol Overview

Table 3. EasyScale Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device address byte	7	DA7	IN	0 MSB device address
	6	DA6	IN	1
	5	DA5	IN	0
	4	DA4	IN	0
4E hex	3	DA3	IN	1
	2	DA2	IN	1
	1	DA1	IN	1
	0	DA0	IN	0 LSB device address
Data byte	7 (MSB)	RFA	IN	Request for acknowledge; if high, the device applies an acknowledge condition.
	6	A1		Address bit 1
	5	A0		Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, the device applies this condition only in the case of a set RFA bit. Open-drain output, the host must pull the line high with a pullup resistor. One can only use this feature if the master has an open-drain output stage. In case of a push-pull output stage, do not request an acknowledge condition.

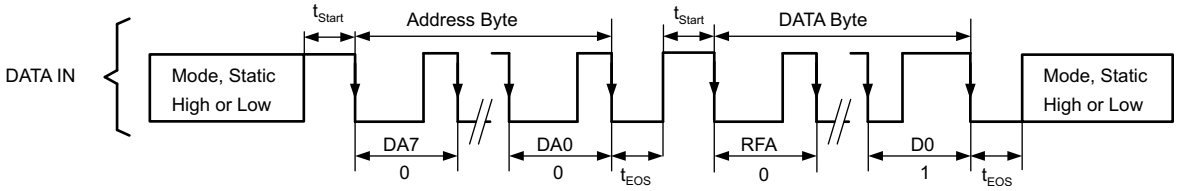

Figure 10. EasyScale Protocol Without Acknowledge

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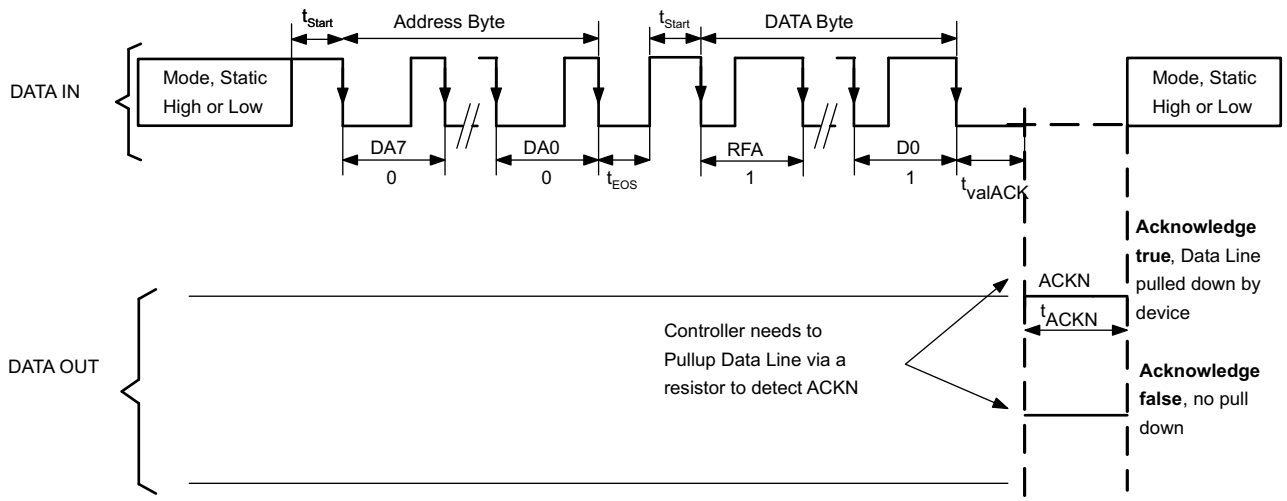

Figure 11. EasyScale Protocol Including Acknowledge

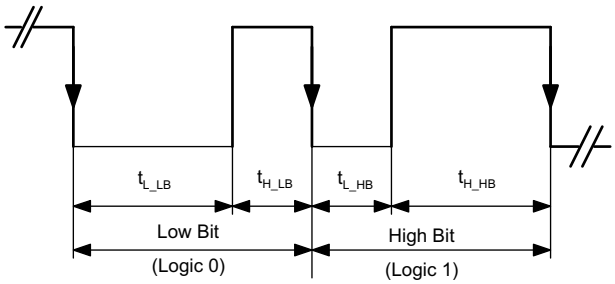

Figure 12. EasyScale – Bit Coding

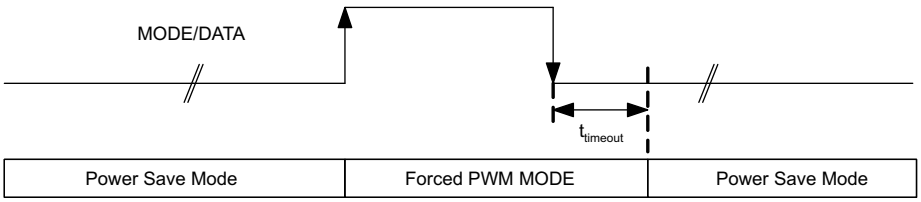

Figure 13. MODE/DATA PIN: Mode Selection

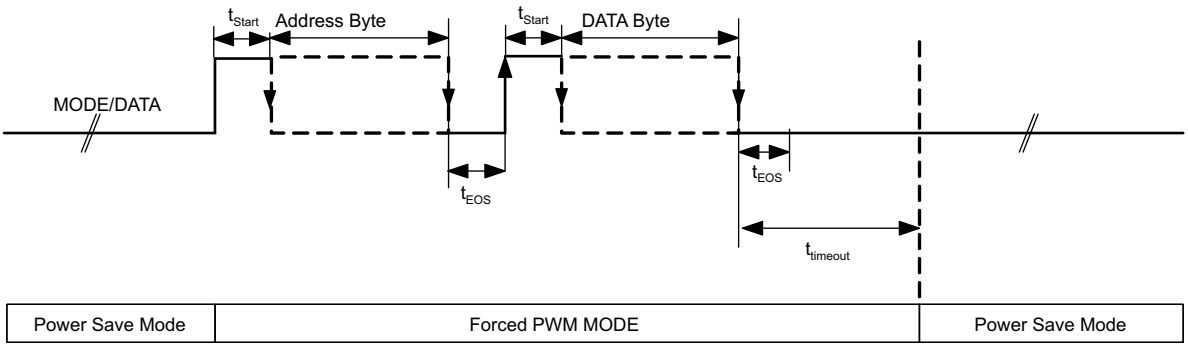

Figure 14. MODE/DATA Pin: Power-Save-Mode and Interface Communication

Table 4. Selectable Output Voltages for Converter 1, With Pin DEF_1 as Digital Input (TPS62402-Q1)

	TPS62402-Q1 OUTPUT VOLTAGE [V] REGISTER REG_DEF_1_LOW	TPS62402-Q1 OUTPUT VOLTAGE [V] REGISTER REG_DEF_1_HIGH	D4	D3	D2	D1	D0
0	0.8	0.9	0	0	0	0	0
1	0.825	0.925	0	0	0	0	1
2	0.85	0.95	0	0	0	1	0
3	0.875	0.975	0	0	0	1	1
4	0.9	1.0	0	0	1	0	0
5	0.925	1.025	0	0	1	0	1
6	0.95	1.050	0	0	1	1	0
7	0.975	1.075	0	0	1	1	1
8	1.0	1.1	0	1	0	0	**0**
9	1.025	1.125	0	1	0	0	1
10	1.050	1.150	0	1	0	1	0
11	1.075	1.175	0	1	0	1	1
12	1.1	1.2	0	1	1	0	0
13	1.125	1.225	0	1	1	0	1
14	1.150	1.25	0	1	1	1	0
15	1.175	1.275	0	1	1	1	1
16	1.2 **(default TPS62402-Q1)** 1.215 **(default TPS62405-Q1)**	1.3	1	0	0	0	0
17	1.225	1.325	1	0	0	0	1
18	1.25	1.350	1	0	0	1	0
19	1.275	1.375	1	0	0	1	1
20	1.3	1.4	1	0	1	0	0
21	1.325	1.425	1	0	1	0	1
22	1.350	1.450	1	0	1	1	0
23	1.375	1.475	1	0	1	1	1
24	1.4	1.5	1	1	0	0	0
25	1.425	1.525	1	1	0	0	1
26	1.450	1.55	1	1	0	1	0
27	1.475	1.575	1	1	0	1	1
28	1.5	1.6	1	1	1	0	0
29	1.525	1.7	1	1	1	0	1
30	1.55	1.8 **(default TPS62402-Q1)**	1	1	1	1	0
31	1.575 **(default TPS62404-Q1)**	1.9 **(default TPS62404-Q1)** 1.925 **(default TPS62405-Q1)**	**1**	**1**	**1**	**1**	**1**

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Table 5. Selectable Output Voltages for Converter 1, With DEF1 Pin as Analog Input (Adjustable, TPS62400-Q1)

	TPS62400-Q1 OUTPUT VOLTAGE [V] REGISTER REG_DEF_1_LOW	D4	D3	D2	D1	D0
0	V_{OUT1} Adjustable with Resistor Network on DEF_1 Pin (default TPS62400-Q1)	0	0	0	0	0
	0.6 V with DEF_1 connected to V_{OUT1} (default TPS62400-Q1)					
1	0.825	0	0	0	0	1
2	0.85	0	0	0	1	0
3	0.875	0	0	0	1	1
4	0.9	0	0	1	0	0
5	0.925	0	0	1	0	1
6	0.95	0	0	1	1	0
7	0.975	0	0	1	1	1
8	1	0	1	0	0	0
9	1.025	0	1	0	0	1
10	1.05	0	1	0	1	0
11	1.075	0	1	0	1	1
12	1.1	0	1	1	0	0
13	1.125	0	1	1	0	1
14	1.15	0	1	1	1	0
15	1.175	0	1	1	1	1
16	1.2	1	0	0	0	0
17	1.225	1	0	0	0	1
18	1.25	1	0	0	1	0
19	1.275	1	0	0	1	1
20	1.3	1	0	1	0	0
21	1.325	1	0	1	0	1
22	1.35	1	0	1	1	0
23	1.375	1	0	1	1	1
24	1.4	1	1	0	0	0
25	1.425	1	1	0	0	1
26	1.45	1	1	0	1	0
27	1.475	1	1	0	1	1
28	1.5	1	1	1	0	0
29	1.525	1	1	1	0	1
30	1.55	1	1	1	1	0
31	1.575	1	1	1	1	1

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Table 6. Selectable Output Voltages for Converter 2, (ADJ2 Connected to V_{OUT2})

	OUTPUT VOLTAGE [V] FOR REGISTER REG_DEF_2	D4	D3	D2	D1	D0
0	**V_{OUT2} Adjustable with resistor network and C_{ff} on ADJ2 pin (default TPS62400-Q1)**	**0**	**0**	**0**	**0**	**0**
	0.6 V with ADJ2 pin directly connected to V_{OUT2} (default TPS62400-Q1)					
1	0.85	0	0	0	0	1
2	0.9	0	0	0	1	0
3	0.95	0	0	0	1	1
4	1	0	0	1	0	0
5	1.05	0	0	1	0	1
6	1.1	0	0	1	1	0
7	1.15	0	0	1	1	1
8	1.2	0	1	0	0	0
9	1.25	0	1	0	0	1
10	1.3	0	1	0	1	0
11	1.35	0	1	0	1	1
12	1.4	0	1	1	0	0
13	1.45	0	1	1	0	1
14	1.5	0	1	1	1	0
15	1.55	0	1	1	1	1
16	1.6	1	0	0	0	0
17	1.7	1	0	0	0	1
18	1.8	1	0	0	1	0
19	1.85	1	0	0	1	1
20	2	1	0	1	0	0
21	2.1	1	0	1	0	1
22	2.2	1	0	1	1	0
23	2.3	1	0	1	1	1
24	2.4	1	1	0	0	0
25	2.5	1	1	0	0	1
26	2.6	1	1	0	1	0
27	2.7	1	1	0	1	1
28	2.8	1	1	1	0	0
29	2.85	1	1	1	0	1
30	3	1	1	1	1	0
31	3.3 **(default TPS62402-Q1, TPS62404-Q1)** 3.35 **(default TPS62405-Q1)**	1	1	1	1	1

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10 Application and Implementation

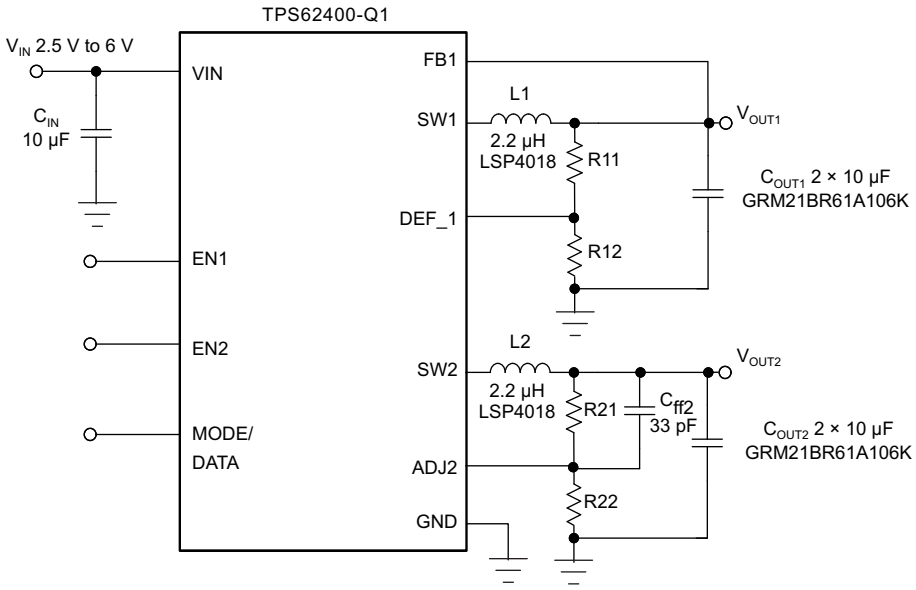
NOTE

Information in the following application sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6240x-Q1 family of devices are synchronous dual step-down DC-DC converters. The devices provide two independent output voltage rails. The following information provides guidance on selecting external components to complete the application design.

10.2 Typical Application



10.2.1 Design Requirements

The step-down converter design can be adapted to different output voltage and load current needs by choosing external components appropriate. The following design procedure is adequate for whole V_{IN}, V_{OUTx} and load current range of the TPS6240x-Q1 family of devices.

10.2.2 Detailed Design Procedure

10.2.2.1 Output Voltage Setting

10.2.2.1.1 Converter 1 Adjustable Default Output-Voltage Setting: TPS62400-Q1

Calculate the output voltage as:

$$V_{OUT1} = V_{REF} \times \left(1 + \frac{R11}{R12}\right)$$

where

- V_{REF} = 0.6-V (typical) internal reference voltage (4)

Typical Application (continued)

To keep the operating current to a minimum, TI recommends selecting R12 within a range of 180 kΩ to 360 kΩ. The sum of R12 and R11 must not exceed approximately 1 MΩ. For output voltages higher than 3.3 V, TI recommends choosing lower values than 180 kΩ for R12. Route the DEF_1 line away from noise sources, such as the inductor or the SW1 line. The FB1 line requires a direct connection to the output capacitor. A feedforward capacitor is not necessary.

10.2.2.1.2 Converter 1 Fixed Default Output-Voltage Setting (TPS62402-Q1, TPS62404-Q1, and TPS62405-Q1)

The DEF_1 pin selects output voltage $\mathbf{V_{OUT1}}$.

Pin DEF_1 = low:

- TPS62402-Q1 = 1.2 V
- TPS62404-Q1 = 1.575 V
- TPS62405-Q1 = 1.215 V

Pin DEF_1 = high:

- TPS62402-Q1 = 1.8 V
- TPS62404-Q1 = 1.9 V
- TPS62405-Q1 = 1.925 V

10.2.2.1.3 Converter 2 Adjustable Default Output-Voltage Setting (TPS62400-Q1):

One can set the output voltage of converter 2 by an external resistor network. For converter 2, the same recommendations apply as for converter 1. In addition to that, use a 33-pF feedforward capacitor C_{ff2} for good load transient response. Calculate the output voltage as:

$$V_{OUT2} = V_{REF} \times \left(1 + \frac{R21}{R22}\right)$$

where

- V_{REF} = 0.6-V (typical) internal reference voltage (5)

10.2.2.1.4 Converter 2 Fixed Default Output-Voltage Setting

ADJ2 pin must be directly connected with V_{OUT2}:

- TPS62402-Q1, V_{OUT2} default = 3.3 V
- TPS62404-Q1, V_{OUT2} default = 3.3 V
- TPS62405-Q1, V_{OUT2} default = 3.35 V

10.2.2.2 Output Filter Design (Inductor and Output Capacitor)

The converters operate with a minimum inductance of 1.75 µH and minimum capacitance of 6 µF. The device operation is optimum with inductors of 2.2 µH to 4.7 µH and output capacitors of 10 µF to 22 µF.

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Typical Application (continued)

10.2.2.2.1 Inductor Selection

Select the inductor based on its ratings for dc resistance and saturation current. The dc resistance of the inductor directly influences the efficiency of the converter. Therefore, select an inductor with lowest dc resistance for highest efficiency.

Equation 6 calculates the maximum inductor current under static load conditions. The saturation-current rating of the inductor must be higher than the maximum inductor current as calculated with Equation 7. TI makes this recommendation because during heavy load transients, the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUTx} \times \frac{1 - \frac{V_{OUTx}}{V_{IN}}}{L \times f_{SW}}$$

where

- ΔI_L = peak-to-peak inductor ripple current
- L = inductor value
- f_{SW} = switching frequency (2.25 MHz typical) (6)

$$I_{L\,max} = I_{OUTx\,max} + \frac{\Delta I_L}{2}$$

where

- I_{Lmax} = maximum inductor current and the highest inductor current occurs at maximum V_{IN} (7)

Open-core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Take into consideration that the core material from inductor to inductor differs, and this difference has an impact on the efficiency.

See Table 7 and the typical application circuit examples for possible inductors.

Table 7. List of Inductors

DIMENSIONS [mm]	INDUCTOR TYPE	SUPPLIER
3.2 × 2.6 × 1	MIPW3226	FDK
3 × 3 × 0.9	LPS3010	Coilcraft
2.8 × 2.6 × 1	VLF3010	TDK
2.8 x 2.6 × 1.4	VLF3014	TDK
3 × 3 × 1.4	LPS3015	Coilcraft
3.9 × 3.9 × 1.7	LPS4018	Coilcraft

10.2.2.2.2 Output-Capacitor Selection

The advanced fast-response voltage-mode control scheme of the converters allows the use of tiny ceramic capacitors with a typical value of 10 µF to 22 µF, without having large output-voltage under- and overshoots during heavy load transients. Ceramic capacitors with low ESR values result in lowest output-voltage ripple, and TI therefore recommends them. The output capacitor requires either X7R or X5R dielectric. TI does not recommend Y5V and Z5U dielectric capacitors because of their wide variation in capacitance.

If using ceramic output capacitors, the capacitor rms ripple-current rating always meets the application requirements. The rms ripple current can be calculated as:

$$I_{RMSCOUTx} = V_{OUTx} \times \frac{1 - \frac{V_{OUTx}}{V_{IN}}}{L \times f_{SW}} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

At nominal load current, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR, plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUTx} = V_{OUTx} \times \frac{1 - \frac{V_{OUTx}}{V_{IN}}}{L \times f_{SW}} \times \left(\frac{1}{8 \times C_{OUTx} \times f_{SW}} + ESR \right)$$

where the highest output-voltage ripple occurs at the highest input voltage, V_{IN}. (9)

At light load currents, the converters operate in power-save mode and the output-voltage ripple depends on the output-capacitor value. The internal comparator delay and the external capacitor set the output-voltage ripple. Higher output capacitors like 22 µF values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

10.2.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, the device requires a low-ESR input capacitor to prevent large voltage transients that can cause misbehavior of the device or interference with other circuits in the system. An input capacitor of 10 µF is sufficient.

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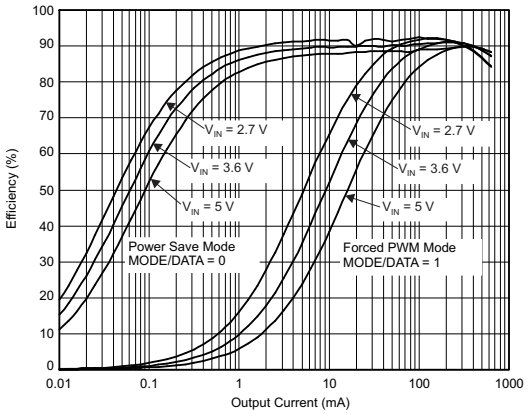
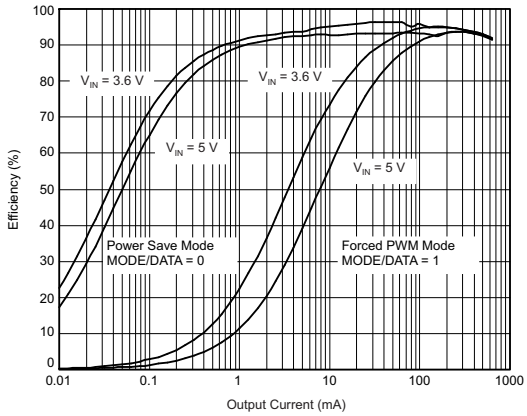
10.2.3 Application Curves



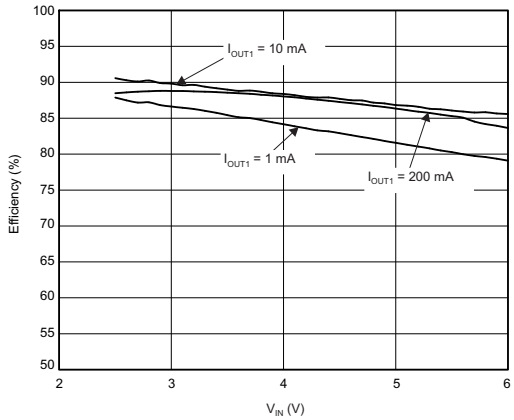
V_{OUT2} = 1.8 V

Figure 15. Efficiency



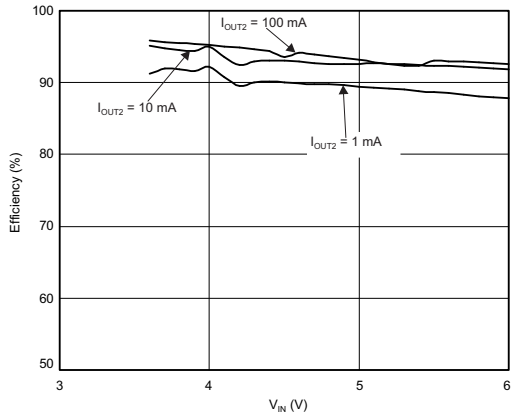
V_{OUT2} = 3.3 V

Figure 16. TPS62400-Q1 Efficiency



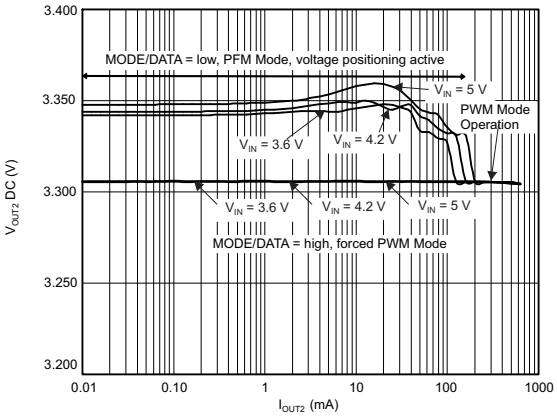
V_{OUT1} = 1.575 V MODE/DATA = 0

Figure 17. Efficiency versus V_{IN}



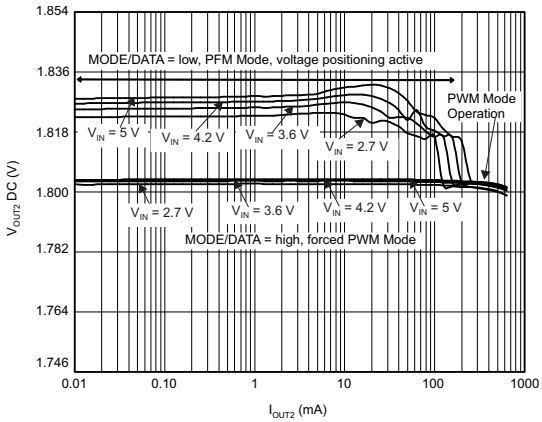
V_{OUT2} = 3.3 V MODE/DATA = 0

Figure 18. Efficiency versus V_{IN}



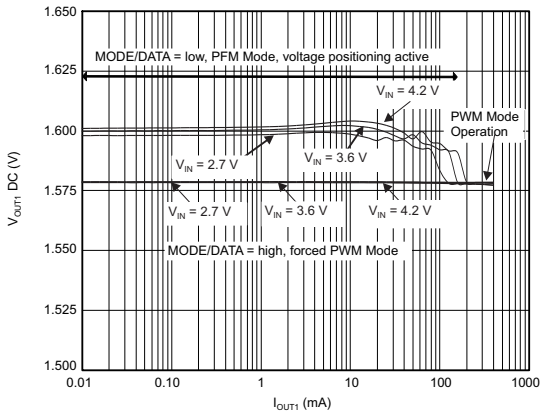
V_{OUT2} = 3.3 V

Figure 19. DC Output Accuracy



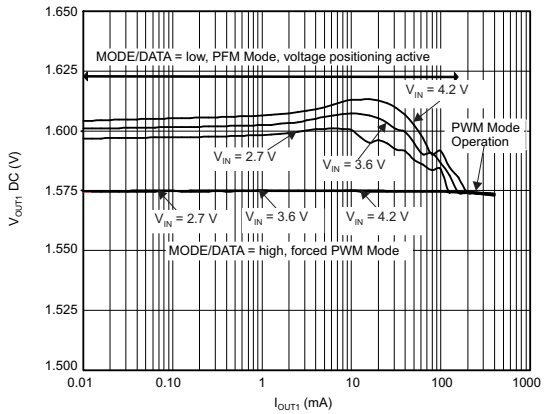
V_{OUT2} = 1.8 V

Figure 20. DC Output Accuracy



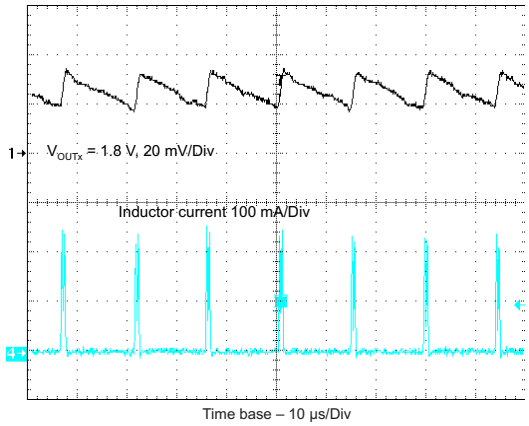
V_{OUT1} = 1.575 V L1 = 2.2 µH C_{OUT1} = 22 µF

Figure 21. DC Output Accuracy



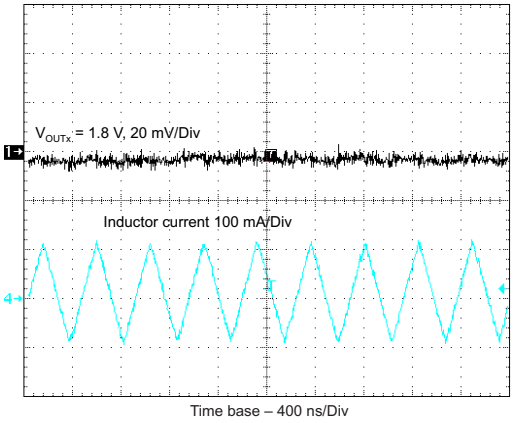
V_{OUT1} = 1.575 V L1 = 3.3 µH C_{OUT1} = 10 µF

Figure 22. DC Output Accuracy



Power save mode MODE/DATA = low I_{OUTx} = 10 mA

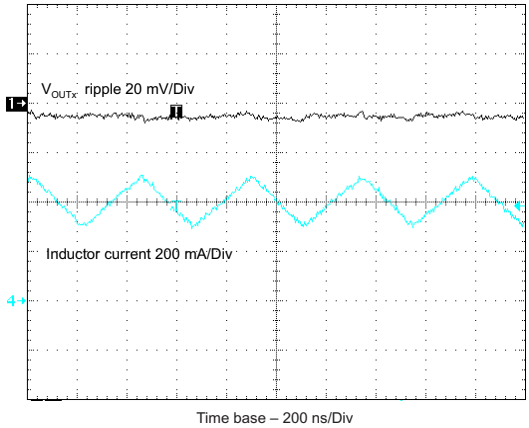
Figure 23. Light-Load Output-Voltage Ripple in Power-Save Mode



Forced PWM mode MODE/DATA = high

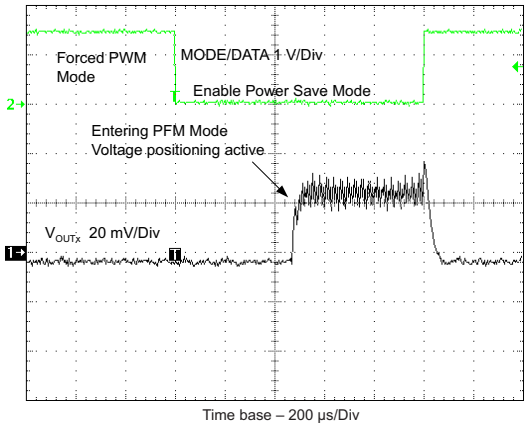
I_{OUTx} = 10 mA

Figure 24. Output-Voltage Ripple in Forced-PWM Mode



PWM mode V_{OUTx} = 1.8 V I_{OUTx} = 400 mA

Figure 25. Output-Voltage Ripple in PWM Mode



V_{OUTx} = 1.8 V I_{OUTx} = 20 mA

Figure 26. Forced PWM-to-PFM Mode Transition

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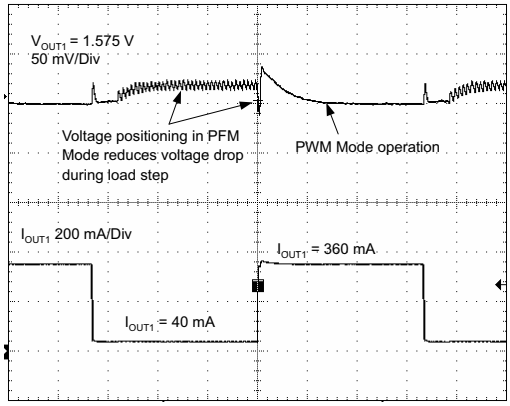
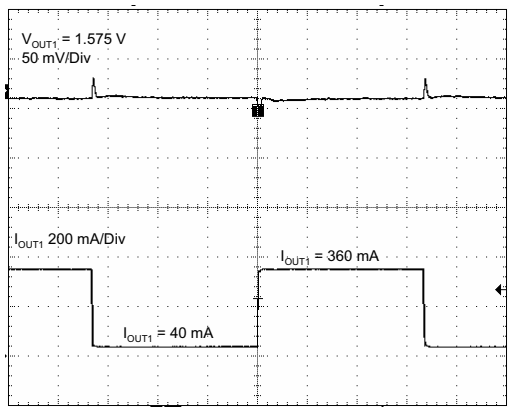


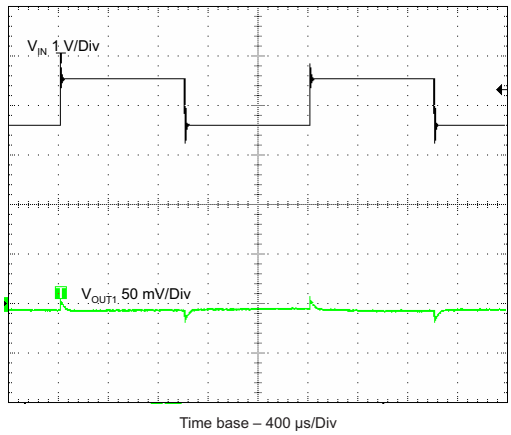
MODE/DATA = low

Figure 27. Load-Transient Response, PFM-to-PWM



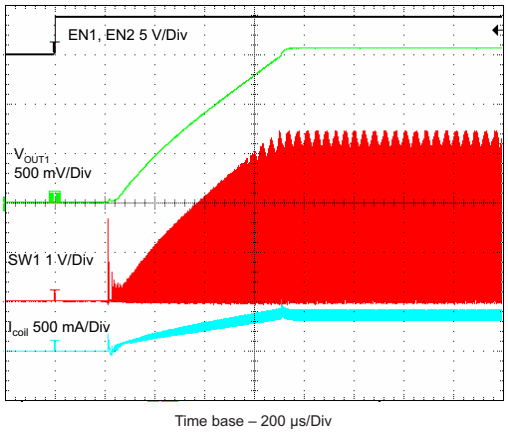
PWM mode MODE/DATA = high

Figure 28. Load-Transient Response, PWM Operation



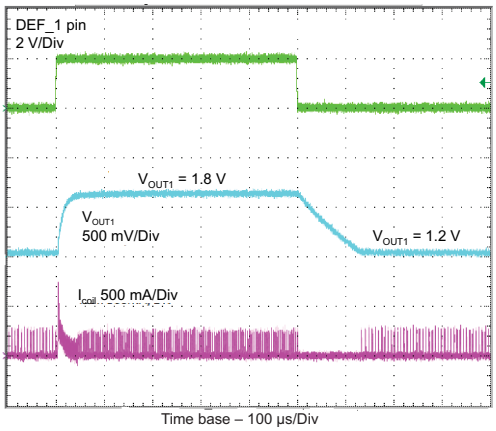
MODE/DATA = low V_{IN} = 3.6 to 4.6 V V_{OUT1} = 1.575 V
I_{OUT1} = 200 mA

Figure 29. Line-Transient Response



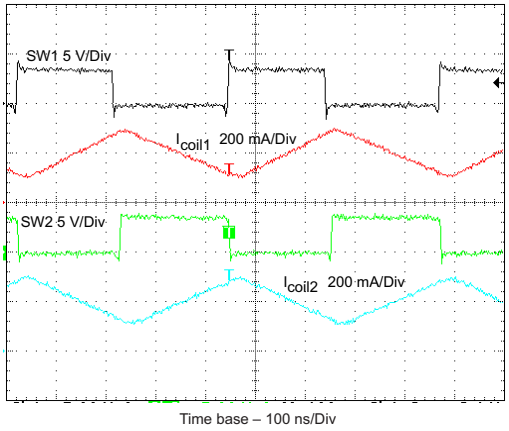
V_{IN} = 3.8 V $I_{OUT1max}$ = 400 mA

Figure 30. Start-up Timing, One Converter



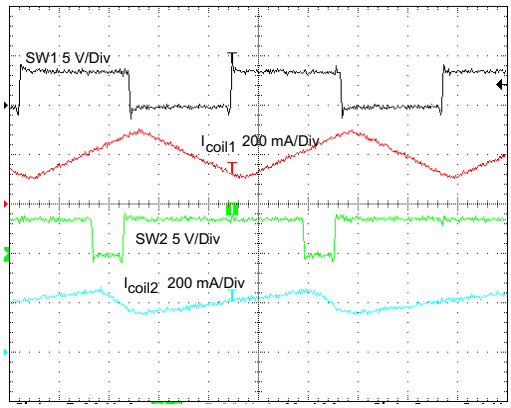
V_{IN} = 3.6 V MODE/DATA = low I_{OUT1} = 40 mA

Figure 31. TPS62402-Q1 DEF1_PIN Function for Output-Voltage Selection



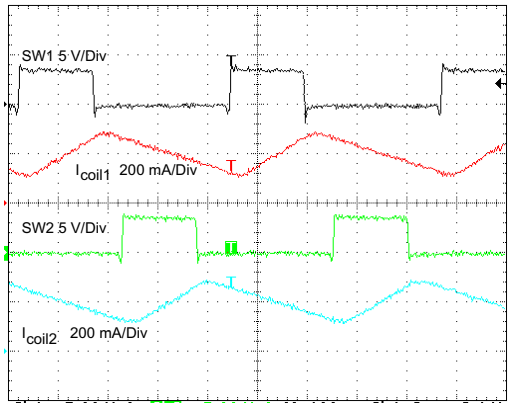
V_{IN} = 3.6 V V_{OUT1} = 1.575 V V_{OUT2} = 1.8 V
I_{OUT1} = I_{OUT2} = 200 mA

Figure 32. Typical Operation



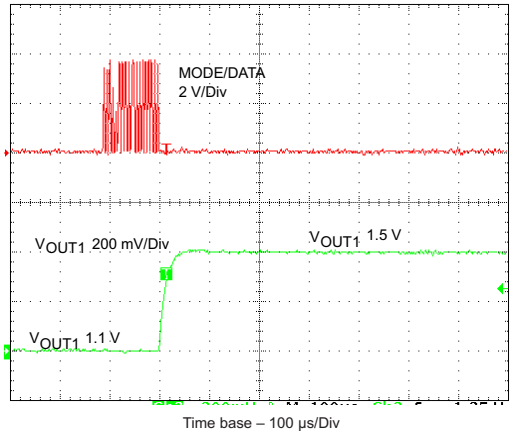
V_{IN} = 3.6 V V_{OUT1} = 1.8 V V_{OUT2} = 3 V
I_{OUT1} = I_{OUT2} = 200 mA

Figure 33. Typical Operation



V_{IN} = 3.6 V V_{OUT1} = 1.2 V V_{OUT2} = 1.2 V
I_{OUT1} = I_{OUT2} = 200 mA

Figure 34. Typical Operation



V_{IN} = 3.8 V ACKN = off I_{OUT1} = 150 mA
REG_DEF_1_Low

Figure 35. V_{OUT1} Change With EasyScale Interface

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10.3 System Examples

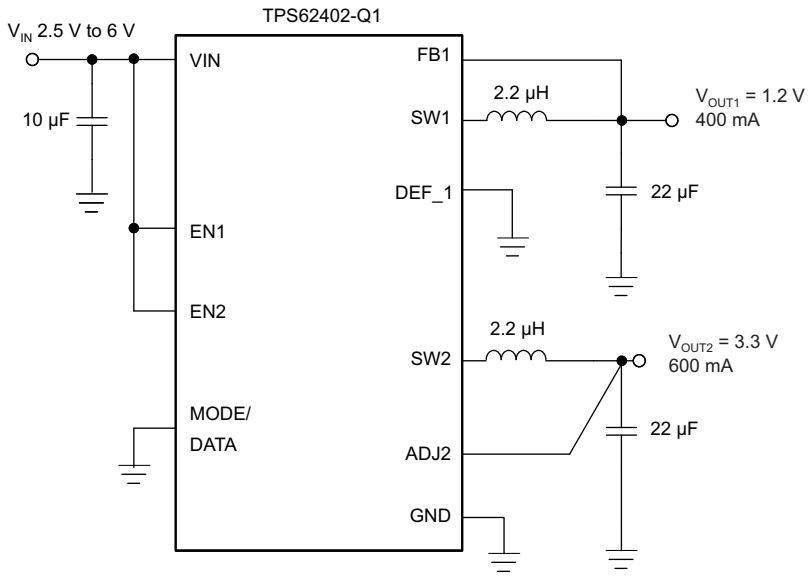

Figure 36. TPS62402-Q1 Fixed 1.2-V and 3.3-V Outputs, Low PFM Ripple Voltage Optimized

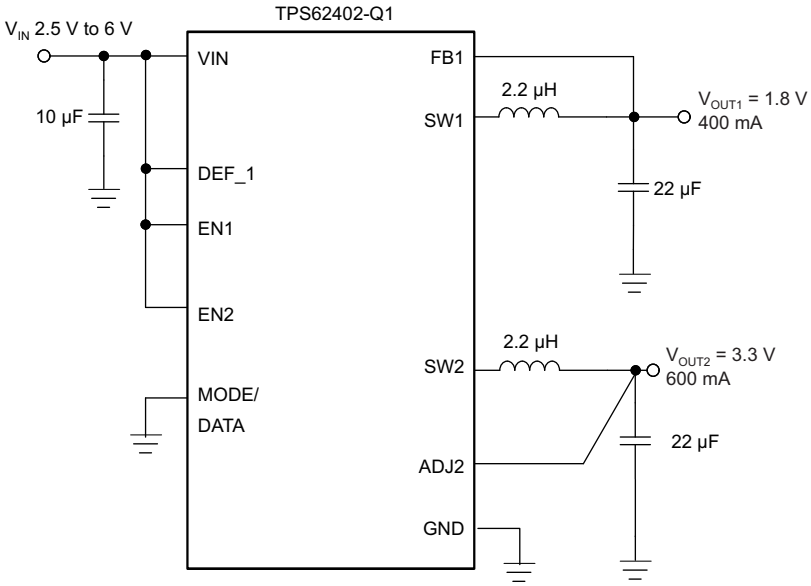

Figure 37. TPS62402-Q1 Fixed 1.8-V and 3.3-V Outputs, Low PFM Ripple Voltage Optimized

System Examples (continued)

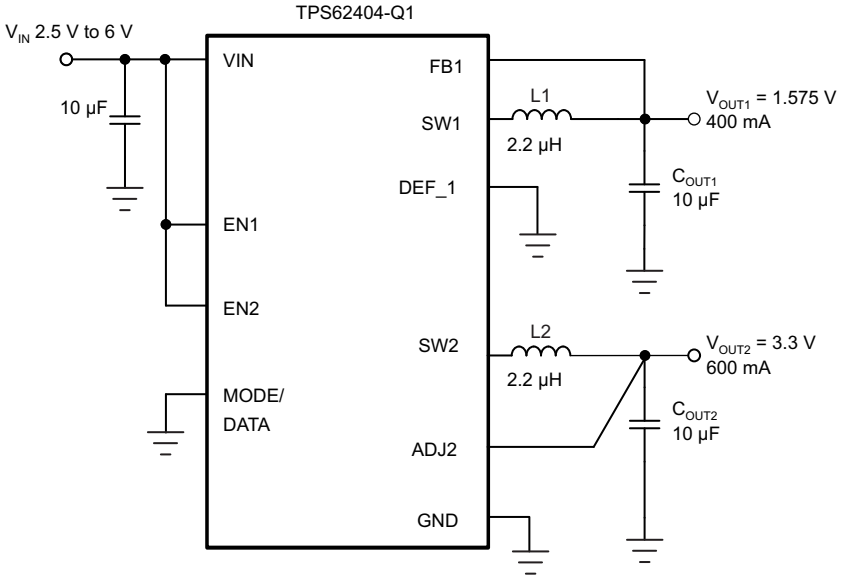

Figure 38. TPS62404-Q1 Fixed 1.575-V and 3.3-V Outputs

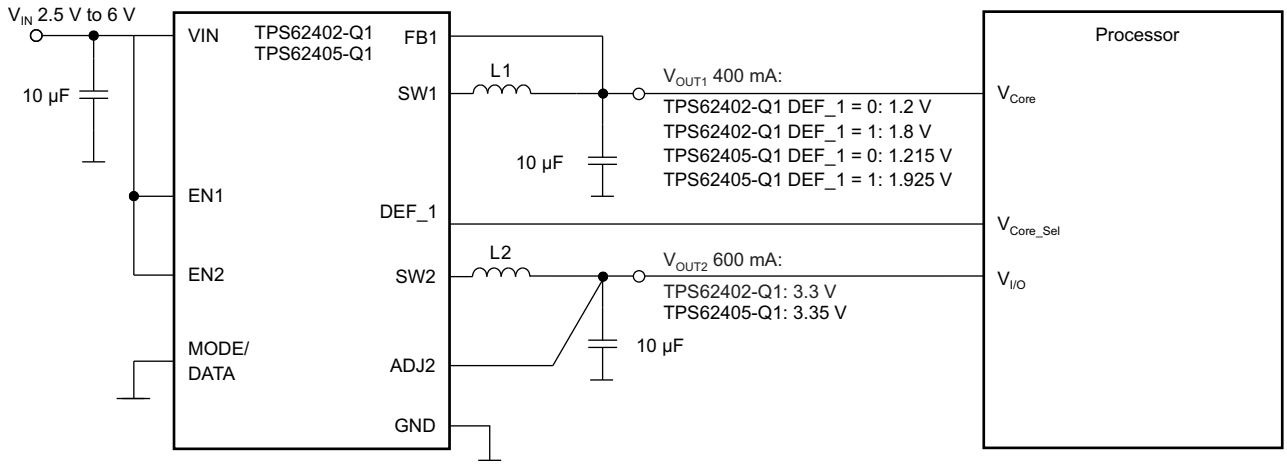

Figure 39. Dynamic Voltage Scaling on V_{OUT1} Controlled by DEF_1 Pin

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System Examples (continued)

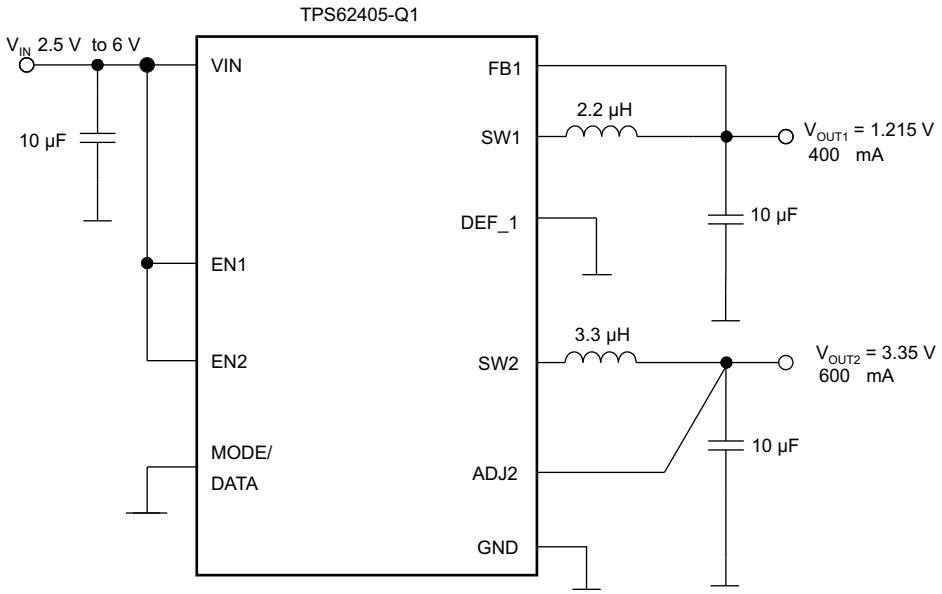

Figure 40. TPS62405-Q1 1.215-V and 3.35 Outputs

11 Power Supply Recommendations

This device has no special recommendation for the power supply. TI recommends to use the values listed in the *Recommended Operating Conditions*.

12 Layout

12.1 Layout Guidelines

- As for all switching power supplies, the layout is an important step in the design.
- Place the input capacitor as close as possible to the IC pins VIN and GND, then place the inductor and output capacitor as close as possible to the pins SW1 and GND.
- Connect the GND pin of the device to the PowerPAD of the PCB and use this pad as a star point. For each converter, use a common power GND node and a different node for the signal GND to minimize the effects of ground noise.
- Connect these ground nodes together to the PowerPAD (star point) underneath the IC. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors, as short as possible to avoid ground noise.
- Connect the output voltage-sense lines (FB 1, DEF_1, ADJ2) right to the output capacitor and route them away from noisy components and traces (for example, the SW1 and SW2 lines).
- If operating the EasyScale interface with high transmission rates, route the MODE/DATA trace away from the ADJ2 line to avoid capacitive coupling into the ADJ2 pin.
- A GND guard ring between the MODE/DATA pin and ADJ2 pin avoids potential noise coupling.

12.2 Layout Example

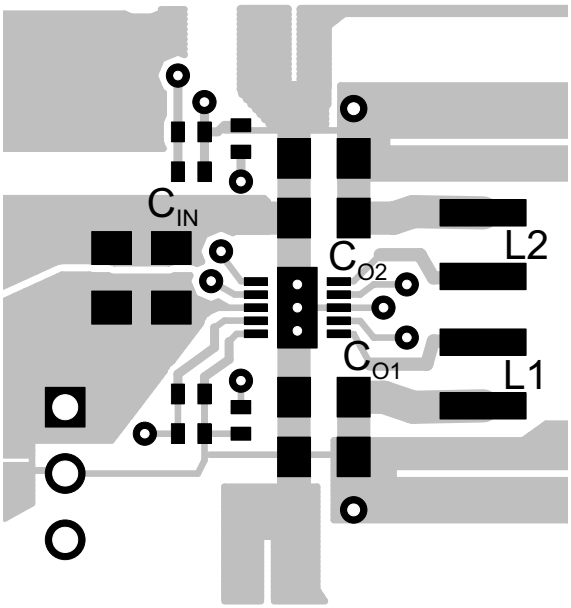

Figure 41. Layout Diagram

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62400-Q1	Click here	Click here	Click here	Click here	Click here
TPS62402-Q1	Click here	Click here	Click here	Click here	Click here
TPS62404-Q1	Click here	Click here	Click here	Click here	Click here
TPS62405-Q1	Click here	Click here	Click here	Click here	Click here

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

EasyScale, the EasyScale, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62400QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SHI
TPS62400QDRCRQ1.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SHI
TPS62402QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SJS
TPS62402QDRCRQ1.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SJS
TPS62404QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OET
TPS62404QDRCRQ1.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OET
TPS62405QDRCRQ1	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SJT
TPS62405QDRCRQ1.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SJT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62400-Q1, TPS62402-Q1, TPS62404-Q1 :

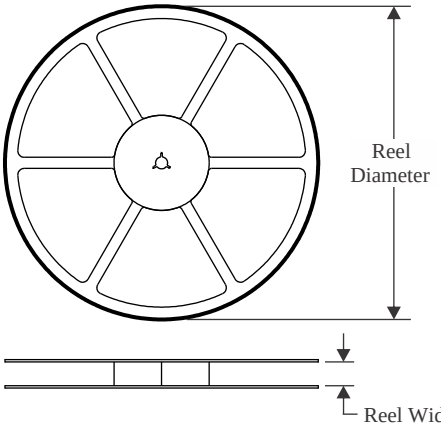
- Catalog : TPS62400, TPS62402, TPS62404

NOTE: Qualified Version Definitions:

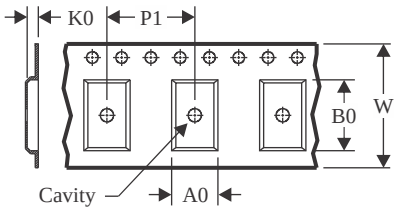
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

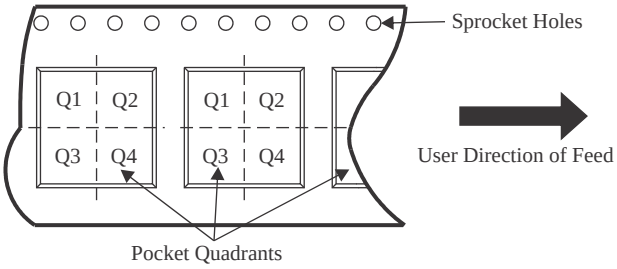


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

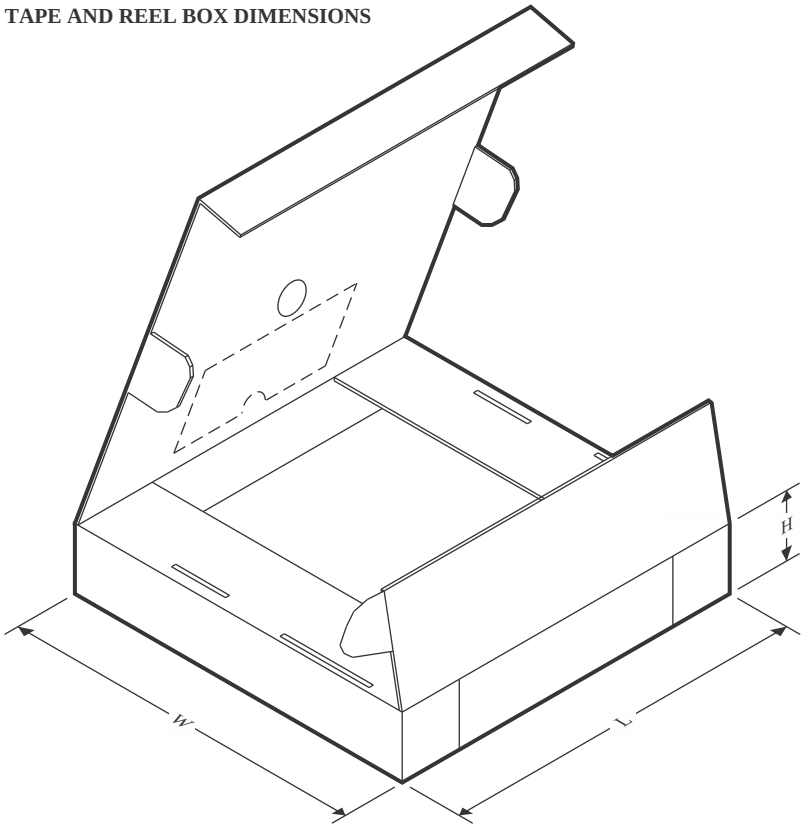
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62400QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62402QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62404QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62405QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62400QDRCRQ1	VSON	DRC	10	3000	353.0	353.0	32.0
TPS62402QDRCRQ1	VSON	DRC	10	3000	353.0	353.0	32.0
TPS62404QDRCRQ1	VSON	DRC	10	3000	353.0	353.0	32.0
TPS62405QDRCRQ1	VSON	DRC	10	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

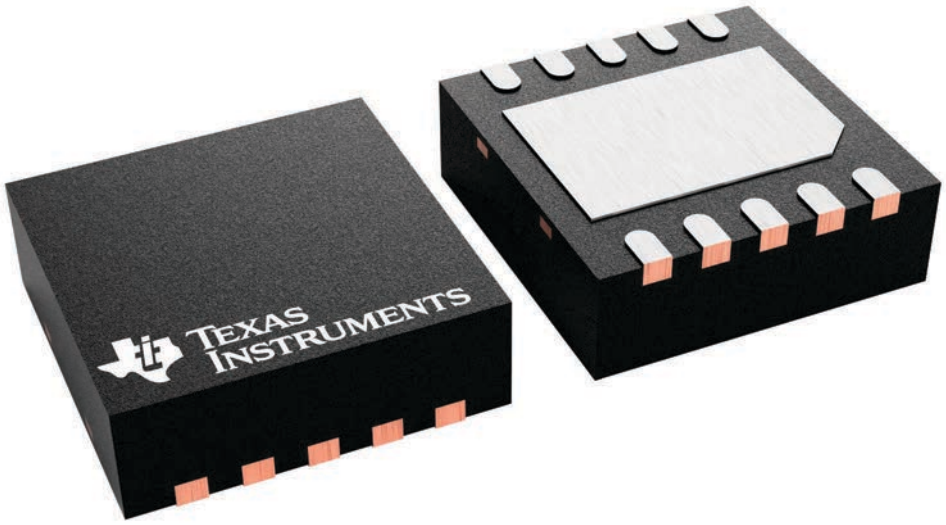
DRC 10

VSON - 1 mm max height

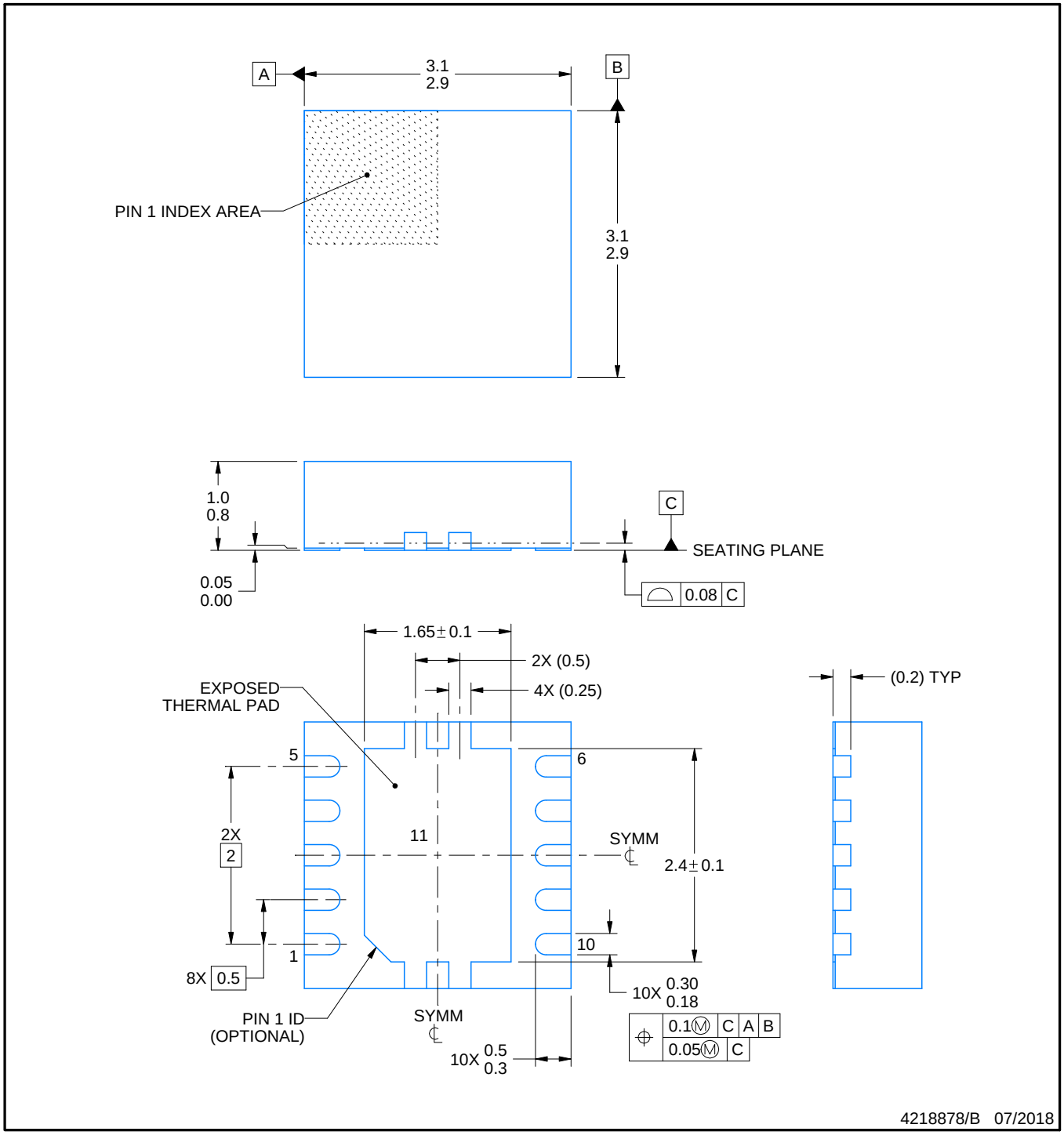
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

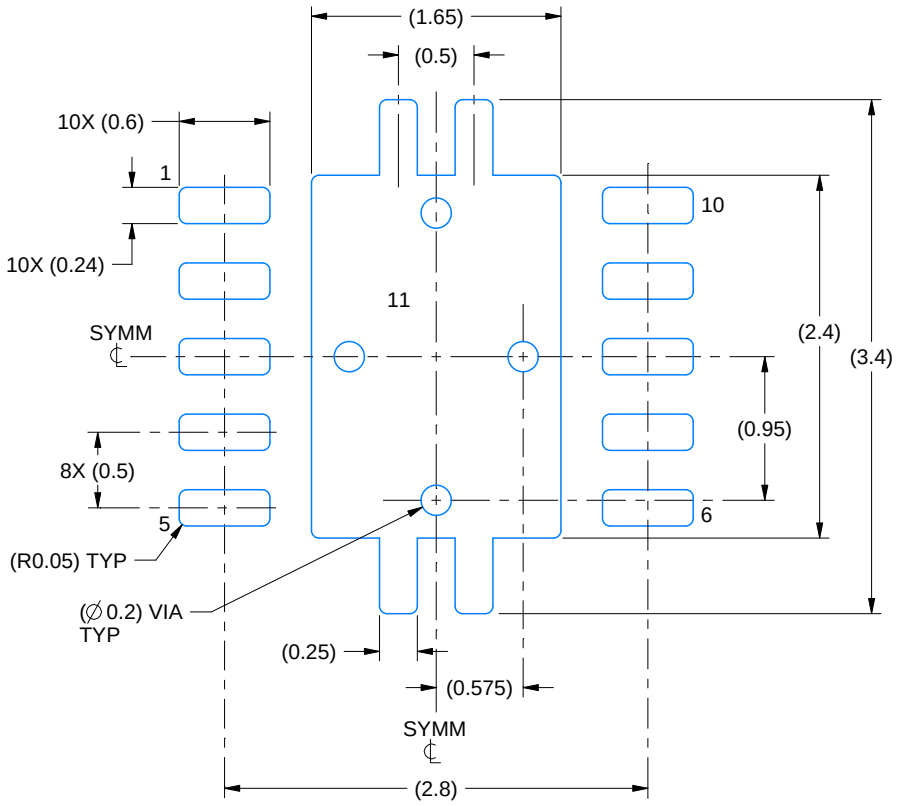


4226193/A

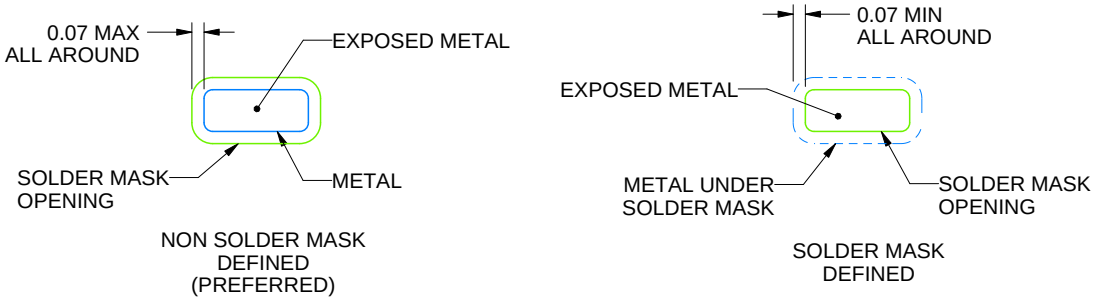


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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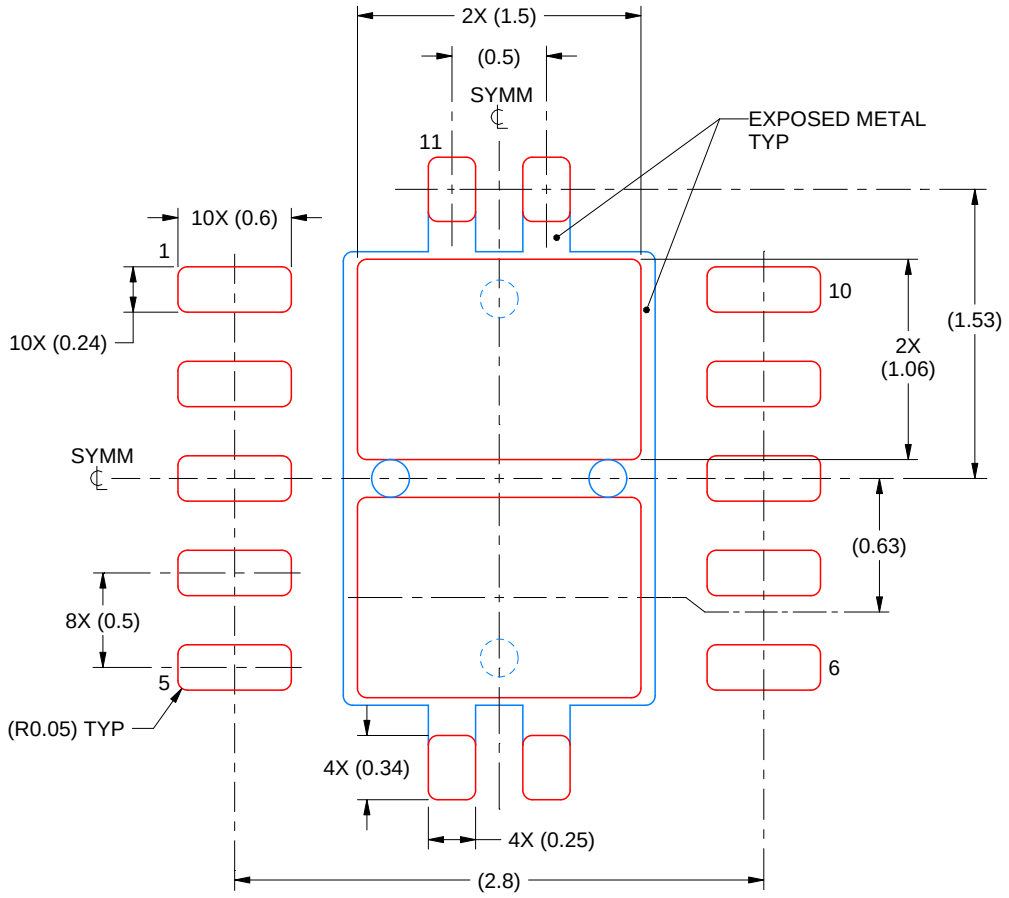
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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