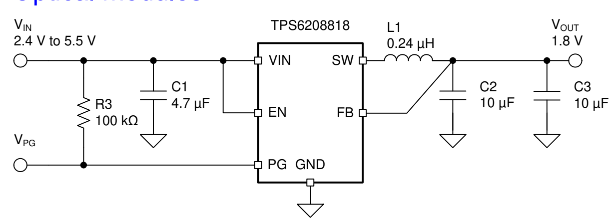
TPS62088 and TPS6208xA 2.4V to 5.5V Input, Tiny 6-Pin, 2A/3A Step-Down Converter in 1.2mm × 0.8mm Wafer Chip Scale Package Designed for Embedding

1 Features

- DCS-Control topology
- Up to 95% efficiency
- 26mΩ and 26mΩ internal power MOSFETs
- 2.4V to 5.5V input voltage range
- 4µA operating quiescent current
- 1% output voltage accuracy
- 4MHz switching frequency
- Power save mode for light-load efficiency
- A forced-PWM version for CCM operation
- 100% duty cycle for lowest dropout
- Active output discharge
- Power-good output
- Thermal shutdown protection
- Hiccup short-circuit protection
- Available in 6-pin WCSP and PowerWCSP with 0.4mm pitch
- 0.3mm tall YWC package supports embedded systems
- Supports 12mm^2 design size
- Supports < 0.6mm height design
- Create a custom design using the TPS62088 with the WEBENCH® Power Designer

2 Applications

- Solid-state drives
- Wearable products
- Smartphones
- Camera modules
- Optical modules



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Typical Application Schematic

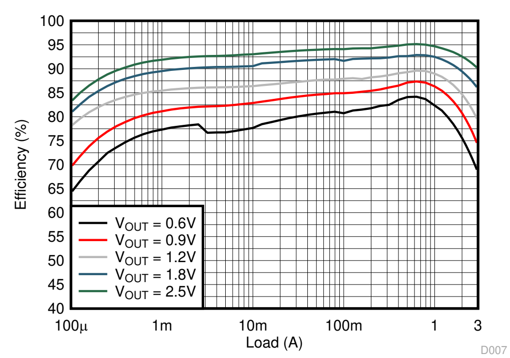
3 Description

The TPS6208xx device family is a high-frequency, synchronous step-down converter designed for small design size and high efficiency. With an input voltage range of 2.4V to 5.5V, common battery technologies are supported. At medium to heavy loads, the converter operates in PWM mode and automatically enters power save mode operation at light load to maintain high efficiency over the entire load current range. The forced PWM version of the device maintains a CCM operation across any load. The 4MHz switching frequency allows the device to use small external components. Together with DCS-control architecture, excellent load transient performance, and output voltage regulation accuracy are achieved. Other features like overcurrent protection, thermal shutdown protection, active output discharge, and power good are built in. The device is available in a 6-pin WCSP package.

Device Information

PART NUMBER(2)	PACKAGE(1)	BODY SIZE (NOM)
TPS62088	YFP (DSBGA, 6)	0.8mm × 1.2mm × 0.5mm
TPS62089A		
TPS62088A	YWC (DSBGA, 6)	0.8mm × 1.2mm × 0.3mm

(1) For more information, see Section 11.
(2) See the *Device Options* table.



3.3V Input Voltage Efficiency

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Table of Contents

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4 Device Options

PART NUMBER(1)	OPERATION MODE	OUTPUT VOLTAGE
TPS62088YFP	PFM/PWM	3-A adjustable
TPS62088YWC	PFM/PWM	3-A adjustable
TPS6208812YFP	PFM/PWM	3 A with 1.2 V
TPS6208818YFP	PFM/PWM	3 A with 1.8 V
TPS6208833YFP	PFM/PWM	3 A with 3.3 V
TPS62088AYFP	Forced-PWM	3-A adjustable
TPS62089AYFP	Forced-PWM	2-A adjustable

(1) For detailed ordering information, please check the package option addendum section at the end of this data sheet.

5 Pin Configuration and Functions

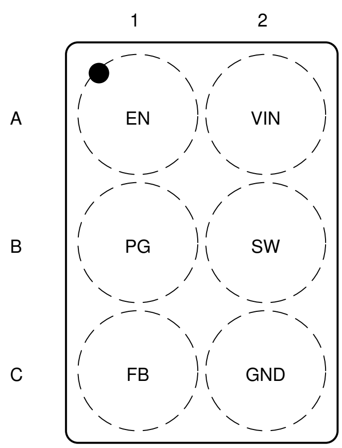

Figure 5-1. 6-Pin YFP Package, DSBGA (Top View)

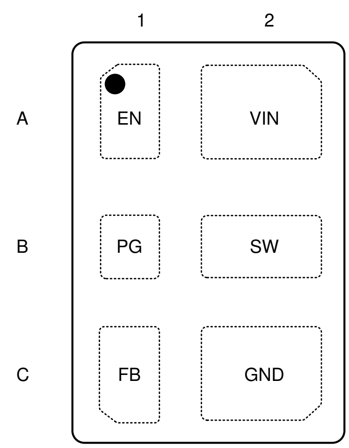

Figure 5-2. 6-Pin YWC Package, DSBGA (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	A1	I	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
PG	B1	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating.
FB	C1	I	Feedback pin. For the fixed output voltage versions, this pin must be connected to the output.
GND	C2	—	Ground pin
SW	B2	O	Switch pin of the power stage
VIN	A2	I	Input voltage pin

(1) I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage at pins (2)	VIN, FB, EN, PG	–0.3	6	V
	SW (DC)	–0.3	V_{IN} + 0.3	
	SW (DC, in current limit)	–1.0	V_{IN} + 0.3	
	SW (AC, less than 10 ns) (3)	–2.5	10	
Temperature	Operating junction temperature, T_J	–40	150	°C
	Storage temperature, T_{stg}	–65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.4		5.5	V
V_{OUT}	Output voltage range	0.6		4.0	V
I_{OUT}	Output current range, TPS62089A	0		2	A
I_{OUT}	Output current range, TPS62088, TPS62088A (1)	0		3	A
I_{SINK_PG}	Sink current at the PG pin			1	mA
V_{PG}	Pullup resistor voltage			5.5	V
T_J	Operating junction temperature	-40		125	°C

(1) For YFP package versions, lifetime is reduced when operating continuously at 3-A output current with the junction temperature higher than 85°C.

6.4 Thermal Information

THERMAL METRIC (1)		TPS62088/TPS6208xA				UNIT
		6 PINS				
		YFP (6 PINS)	YWC (6 PINS)	YFP EVM-814	YWC EVM-084	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.3	130.9	85.7	70.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	1.1	n/a (2)	n/a (2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.3	27.3	n/a (2)	n/a (2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	0.7	1.9	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.5	27.2	55.9	38.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM.

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6.5 Electrical Characteristics

T_J = –40°C to 125°C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = HIGH, no load, device not switching		4	10	µA
I_Q	Quiescent current	EN = HIGH, no load, TPS62088A and TPS62089A		8		mA
I_{SD}	Shutdown current	EN = LOW, T_J = –40℃ to 85℃		0.05	0.5	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lockout hysteresis	V_{IN} rising		160		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level input threshold voltage		1.0			V
V_{IL}	Low-level input threshold voltage				0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin			0.01	0.1	µA
SOFT START, POWER GOOD						
t_{SS}	Soft-start time	Time from EN high to 95% of V_{OUT} nominal		1.25		ms
V_{PG}	Power-good lower threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	94%	96%	98%	
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	90%	92%	94%	
	Power-good upper threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	103%	105%	107%	
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	108%	110%	112%	
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01	0.1	µA
OUTPUT						
V_{OUT}	Output voltage accuracy	TPS6208812, PWM mode	1.188	1.2	1.212	V
		TPS6208818, PWM mode	1.782	1.8	1.818	
		TPS6208833, PWM mode	3.267	3.3	3.333	
V_{FB}	Feedback regulation voltage	PWM mode	594	600	606	mV
$I_{FB,LKG}$	Feedback input leakage current	TPS62088, V_{FB} = 0.6 V		0.01	0.05	µA
R_{FB}	Internal resistor divider connected to FB pin	TPS6208812, TPS6208818, TPS6208833		7.5		MΩ
I_{DIS}	Output discharge current	V_{SW} = 0.4V; EN = LOW	75	400		mA
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			26		mΩ
I_{LIM}	High-side FET switch current limit	TPS62089A	2.7	3.3	3.9	A
I_{LIM}	High-side FET switch current limit	TPS62088 and TPS62088A	3.6	4.3	5.0	A
I_{LIM}	Low-side FET switch negative current limit	TPS62088A and TPS62089A		-1.6		A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 1.8 V		4		MHz

6.6 Typical Characteristics

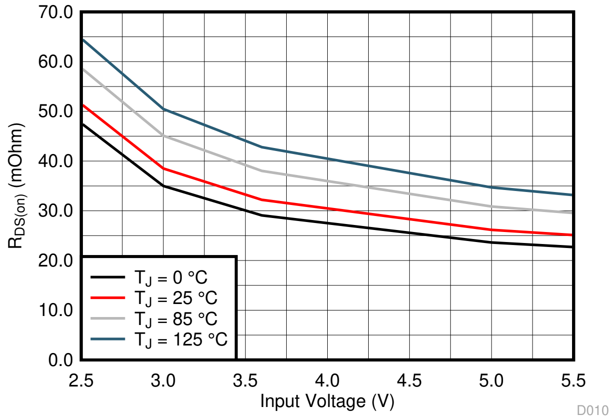

Figure 6-1. High-Side FET On-Resistance

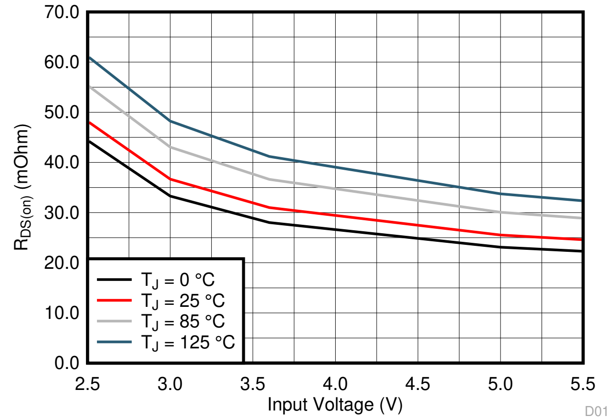

Figure 6-2. Low-Side FET On-Resistance

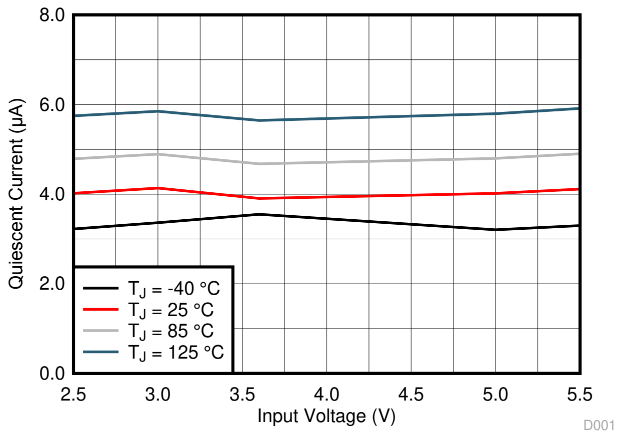

Figure 6-3. Quiescent Current

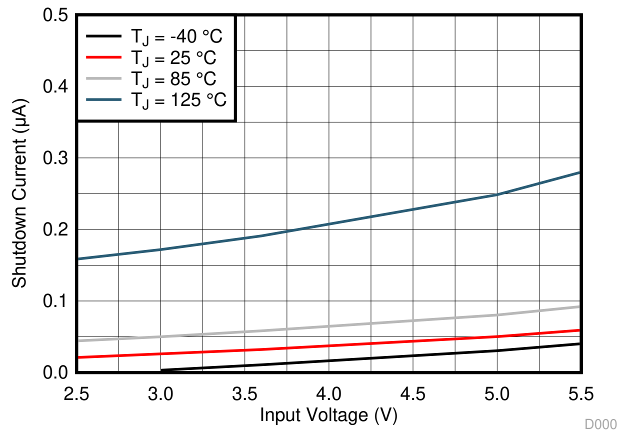

Figure 6-4. Shutdown Current

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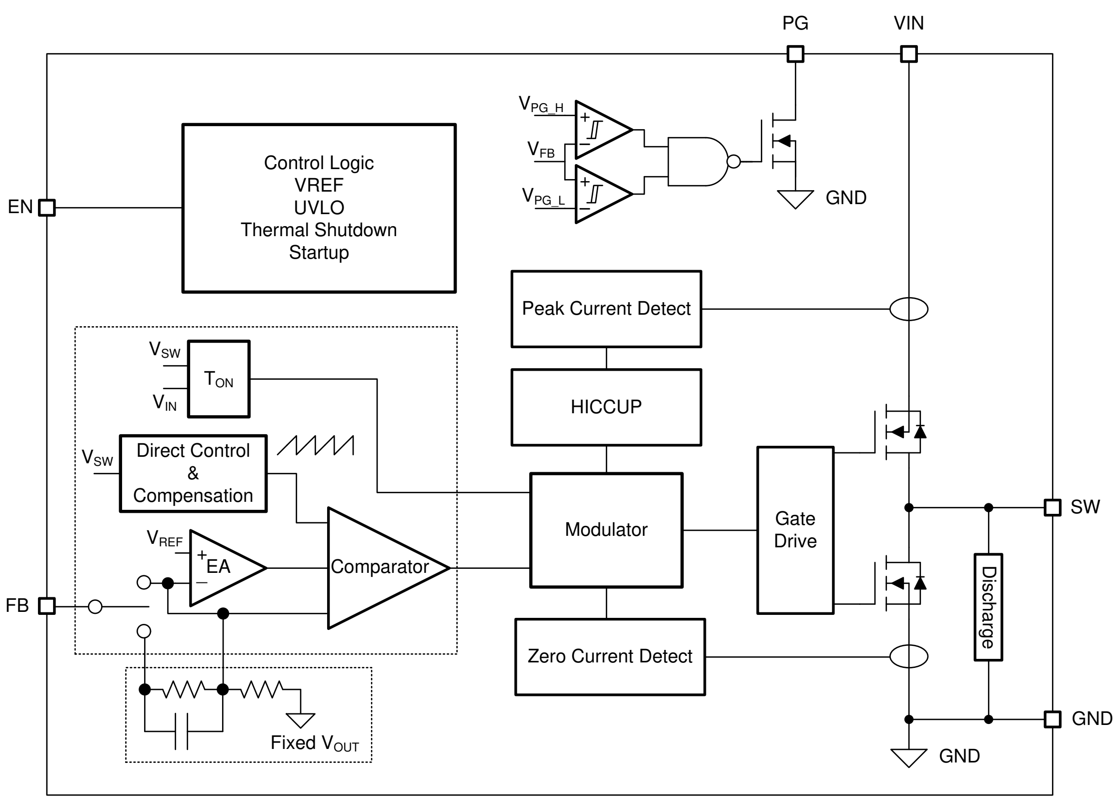
7 Detailed Description

7.1 Overview

The TPS62088xx family is a synchronous step-down converter that adopts a new generation DCS-Control (Direct Control with Seamless transition into power save mode) topology without the output voltage sense (VOS) pin. This topology is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control schemes.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in power save mode at light load currents. In PWM mode, the converter operates with the nominal switching frequency of 4 MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC current consumption to achieve high efficiency over the entire load current range. In forced PWM devices, the converter maintains a continuous conduction mode operation and keeps the output voltage ripple very low across the whole load range and at a nominal switching frequency of 4 MHz. Because DCS-Control supports both operation modes (PWM and PFM) within a single building block, the transition from PWM mode to power save mode is seamless and without effects on the output voltage. The devices offer both excellent DC voltage and excellent load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

As the load current decreases, the device enters power save mode operation. The power save mode occurs when the inductor current becomes discontinuous. Power save mode is based on a fixed on-time architecture, as related in Equation 1.

$$t_{ON} = 250ns \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

When the device operates close to 100% duty cycle mode, the device cannot enter power save mode regardless of the load current if the input voltage decreases to typically 10% above the output voltage. The device maintains output regulation in PWM mode.

7.3.2 Pulse Width Modulation (PWM) Operation

At load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM). The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency.

In forced-PWM devices, the device always operates in pulse width modulation in continuous conduction mode (CCM).

7.3.3 100% Duty Cycle Low Dropout Operation

The devices offer low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain output regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \quad (2)$$

where

- $V_{IN,MIN}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.4 Soft Start

After enabling the device, there is a 250-µs delay before switching starts. Then, an internal soft start-up circuitry ramps up the output voltage which reaches nominal output voltage during the start-up time of 1 ms. This action avoids excessive inrush current and creates a smooth output voltage rise slope. This action also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The device is able to start into a prebiased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.3.5 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET remains off, while the inductor current flows through the body diode and quickly ramps down.

When this switch current limits is triggered 32 times, the device stops switching. The device then automatically starts a new start-up after a typical delay time of 128 µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

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In forced PWM devices, a negative current limit (ILIMN) is enabled to prevent excessive current flowing backwards to the input. When the inductor current reaches ILIMN, the low-side MOSFET turns off and the highside MOSFET turns on and kept on until TON time expires.

7.3.6 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, undervoltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO}.

7.3.7 Thermal Shutdown

The device goes into thermal shutdown and stops the power stage switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically by switching the power stage again.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic HIGH. Accordingly, shutdown mode is forced if the EN pin is pulled LOW with a shutdown current of typically 50 nA. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal switch smoothly discharges the output through the SW pin in shutdown mode. Do not leave the EN pin floating.

The typical threshold value of the EN pin is 0.89 V for rising input signal, and 0.62 V for falling input signal.

7.4.2 Power Good

The device has a power-good output. The PG pin goes high impedance after the FB pin voltage is above 96% and less than 105% of the nominal voltage, and is driven low after the voltage falls below typically 92% or higher than 110% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5 V.

The PG signal can be used for sequencing of multiple rails by connecting the PG signal to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge has a 100-µs blanking time and the PG falling edge has a deglitch delay of 20 µs.

Table 7-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable	EN = HIGH, $V_{FB} \geq 0.576$ V	√	
	EN = HIGH, $V_{FB} \leq 0.552$ V		√
	EN = HIGH, $V_{FB} \leq 0.63$ V	√	
	EN = HIGH, $V_{FB} \geq 0.66$ V		√
Shutdown	EN = LOW		√
Thermal shutdown	$T_J > T_{JSD}$		√
UVLO	$0.7 V < V_{IN} < V_{UVLO}$		√
Power supply removal	$V_{IN} < 0.7$ V	undefined	

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

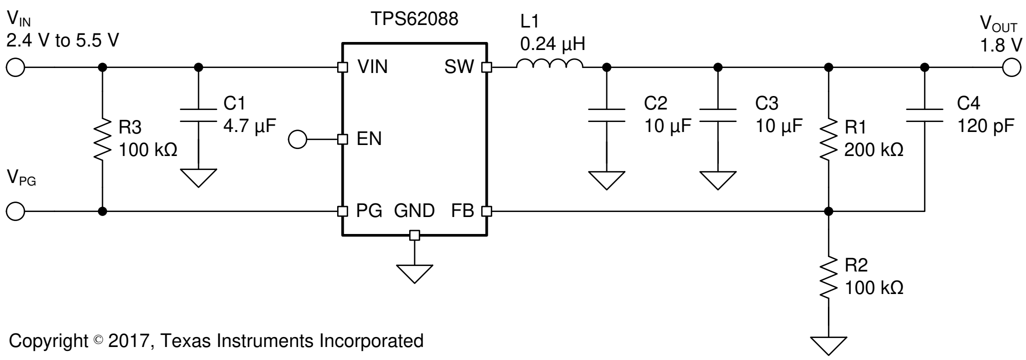

Figure 8-1. Typical Application of Adjustable Output

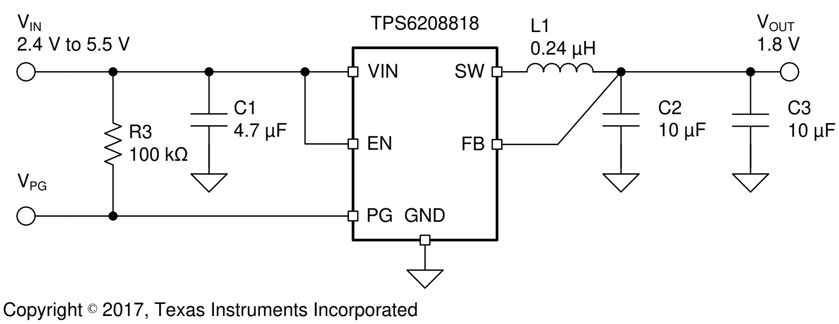

Figure 8-2. Typical Application of Fixed Output

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4 V to 5.5 V
Output voltage	1.8 V
Maximum peak output current	3 A

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Table 8-2 lists the components used for the example.

Table 8-2. List of Components of Figure 8-1

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	4.7 µF, Ceramic capacitor, 6.3 V, X7R, size 0603, JMK107BB7475MA	Taiyo Yuden
C2, C3	10 µF, Ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C4	120 pF, Ceramic capacitor, 50 V, size 0603, GRM1885C1H121JA01D	Murata
L1	0.24 µH, Power Inductor, size 0603, DFE160810S-R24M (DFE18SANR24MG0)	Murata
R1	Depending on the output voltage, 1%, size 0603	Std
R2	100 kΩ, Chip resistor, 1/16 W, 1%, size 0603	Std
R3	100 kΩ, Chip resistor, 1/16 W, 1%, size 0603	Std

(1) See the *Third-party Products* disclaimer.

Table 8-3. List of Components of Figure 8-2 , Smallest Solution

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1, C2, C3	10 µF, Ceramic capacitor, 6.3 V, X5R, size 0402, GRM155R60J106ME47	Murata
L1	0.24 µH, Power Inductor, size 0603, DFE160810S-R24M (DFE18SANR24MG0)	Murata
R3	100 kΩ, Chip resistor, 1/16 W, size 0402	Std

(1) See the *Third-party Products* disclaimer.

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62088 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting The Output Voltage

Choose resistors R1 and R2 to set the output voltage within a range of 0.6V to 4V, according to Equation 3. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100 kΩ to have at least 0.6 µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations For A Resistive Feedback Divider In A DC/DC Converter Analog Design Journal*.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (3)$$

For devices with a fixed output voltage, the FB pin must be connected to V_{OUT}. R1, R2, and C4 are not needed. The fixed output voltage devices have an internal feedforward capacitor.

8.2.2.3 Feedforward Capacitor

A feedforward capacitor (C4) is required in parallel with R1. Equation 4 calculates the capacitor value. For the recommended 100 k value for R2, a 120 pF feedforward capacitor is used. For forced PWM devices, a feedforward capacitor is not needed.

$$C4 = \frac{12\ \mu s}{R2} \tag{4}$$

8.2.2.4 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, Table 8-4 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Check further combinations for each individual application.

Table 8-4. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)			
	10	2 x 10 or 1 x 22	47	100
0.24	+	+(1)	+	
0.33	+	+	+	
0.47				

(1) This LC combination is the standard value and recommended for most applications. Other '+' marks indicate recommended filter combinations. Other values can be acceptable in some applications but must be fully tested by the user.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.

8.2.2.5 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 5 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \tag{5}$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

TI recommends to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. Table 8-5 lists recommended inductors.

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Table 8-5. List of Recommended Inductors

INDUCTANCE [μH] (1)	CURRENT RATING [A]	DIMENSIONS [L × W × H mm]	DC RESISTANCE [mΩ]	PART NUMBER
0.24	6.5	2.0 × 1.2 × 0.8	20	Murata, DFE21CCNR24MEL
0.24	6.5	2.0 × 1.2 × 1.0	25	Murata, DFE201210U-R24M
0.24	4.9	1.6 × 0.8 × 0.8	22	Cyntec, HTEH16080H-R24MSR
0.25	9.7	4.0 × 4.0 × 1.2	7.64	Coilcraft, XFL4012-251ME
0.24	3.5	2.0 × 1.6 × 0.6	35	Wurth Electronics, 74479977124
0.24	3.5	2.0 × 1.6 × 0.6	35	Sunlord, MPM201606SR24M

(1) See the *Third-party Products* disclaimer.

8.2.2.6 Capacitor Selection

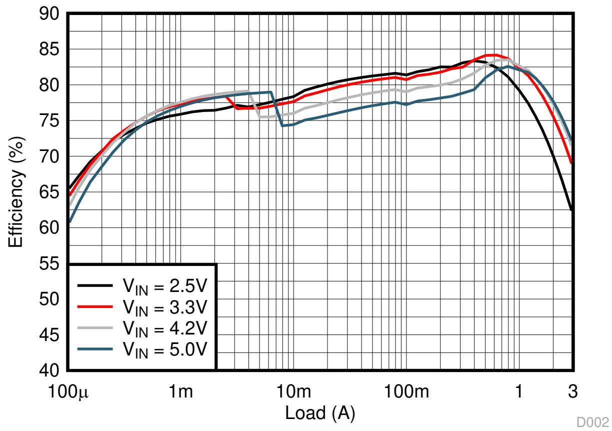
The input capacitor is the low-impedance energy source for the converters which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, 4.7 μF is sufficient, though a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep the low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. The recommended typical output capacitor value is 2 × 10 μF or 1 × 22 μF; this capacitance can vary over a wide range as outline in the output filter selection table.

A feedforward capacitor is required for the adjustable version, as described in Section 8.2.2.2. This capacitor is not required for the fixed output voltage versions.

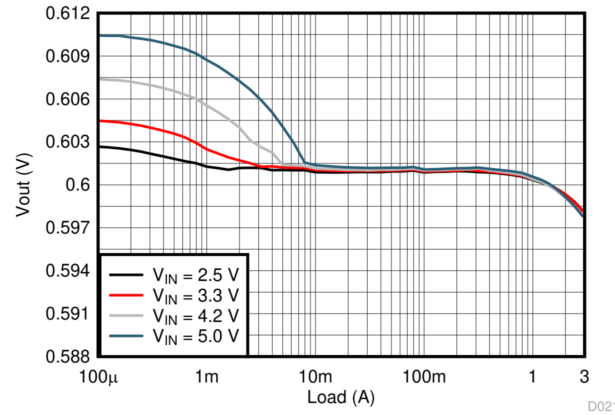
8.2.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 1.8 V, T_A = 25°C, BOM = Table 8-2, unless otherwise noted.



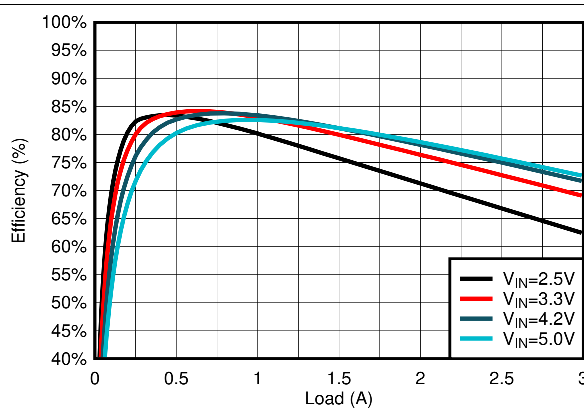
V_{OUT} = 0.6 V

Figure 8-3. Efficiency



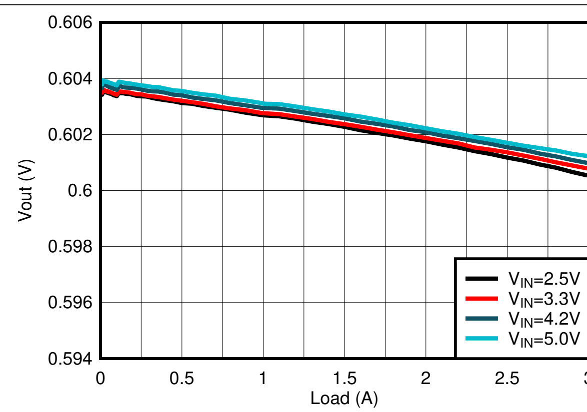
V_{OUT} = 0.6 V

Figure 8-4. Load Regulation



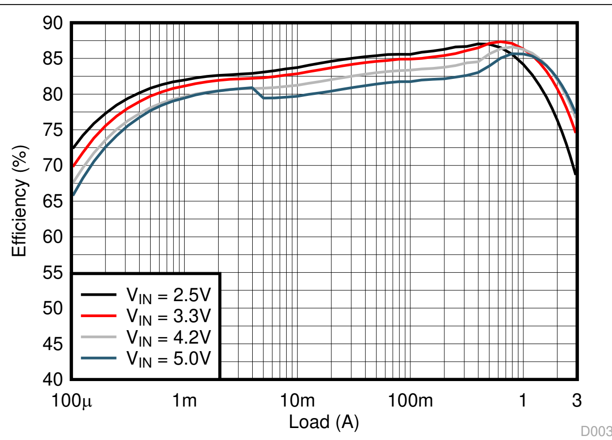
V_{OUT} = 0.6 V FPWM devices

Figure 8-5. Efficiency



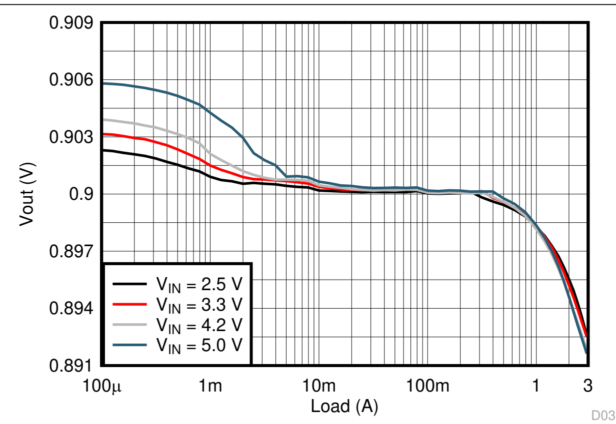
V_{OUT} = 0.6 V FPWM devices

Figure 8-6. Load Regulation



V_{OUT} = 0.9 V

Figure 8-7. Efficiency



V_{OUT} = 0.9 V

Figure 8-8. Load Regulation

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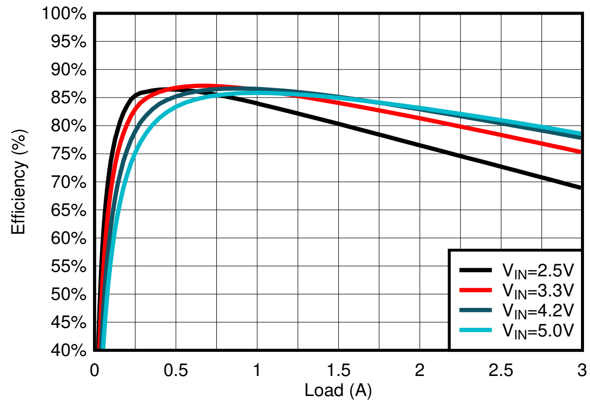
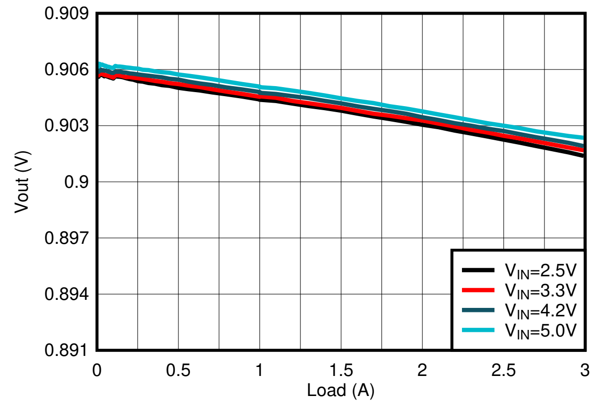


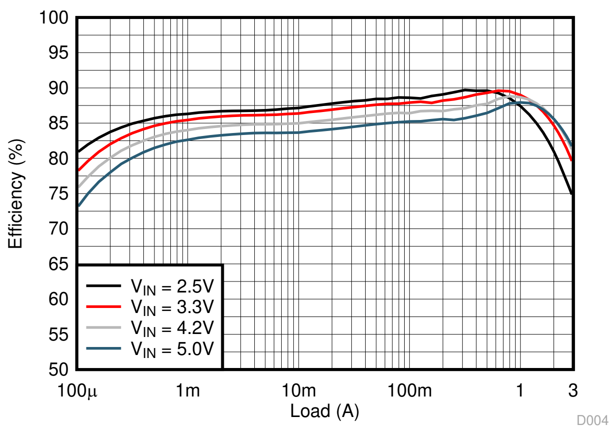
V_{OUT} = 0.9 V FPWM devices

Figure 8-9. Efficiency



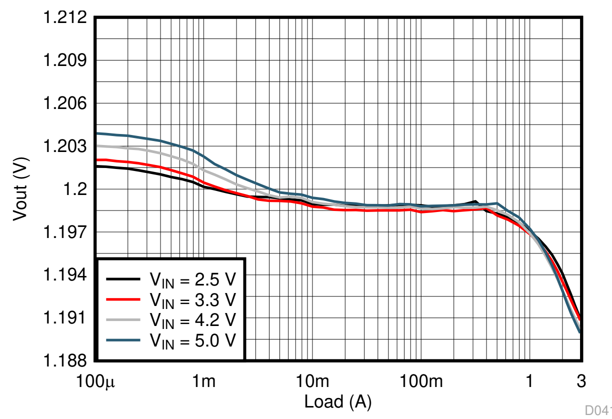
V_{OUT} = 0.9 V

Figure 8-10. Load Regulation



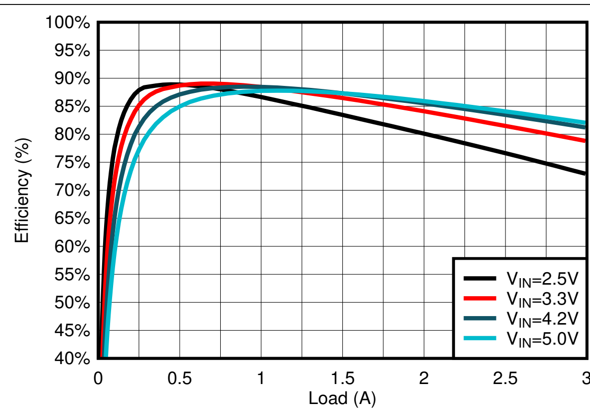
V_{OUT} = 1.2 V

Figure 8-11. Efficiency



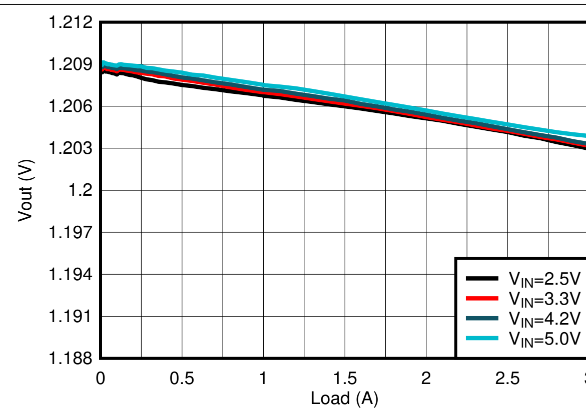
V_{OUT} = 1.2 V

Figure 8-12. Load Regulation



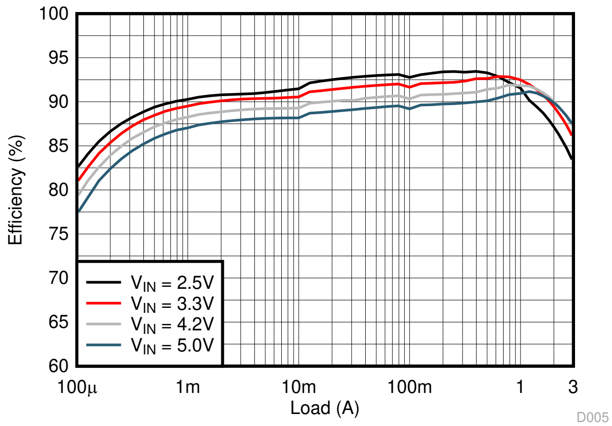
V_{OUT} = 1.2 V FPWM devices

Figure 8-13. Efficiency



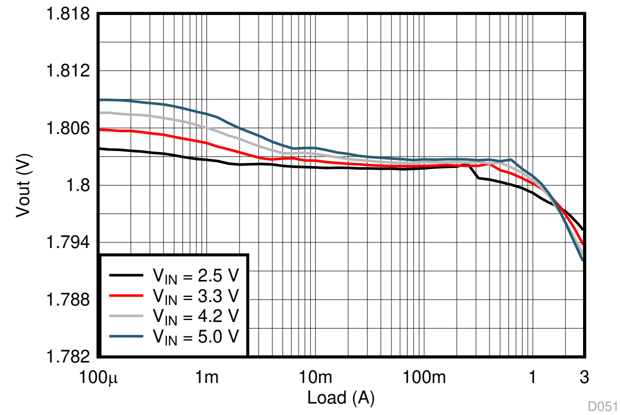
V_{OUT} = 1.2 V FPWM devices

Figure 8-14. Load Regulation



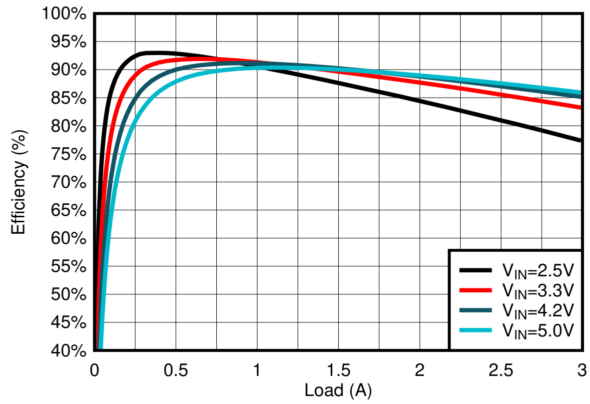
V_{OUT} = 1.8 V

Figure 8-15. Efficiency



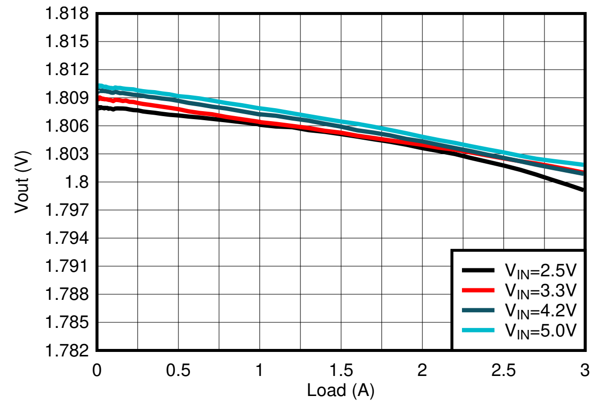
V_{OUT} = 1.8 V

Figure 8-16. Load Regulation



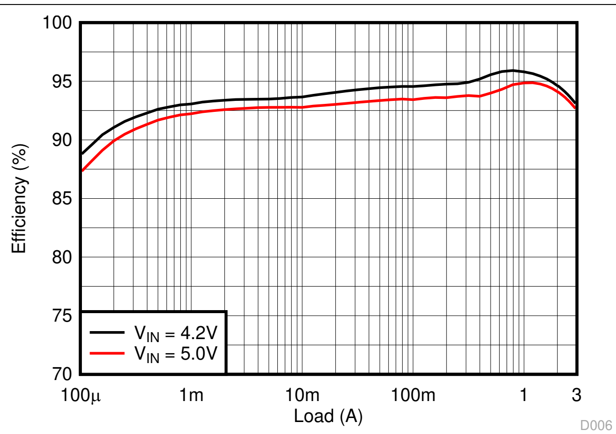
V_{OUT} = 1.8 V FPWM devices

Figure 8-17. Efficiency



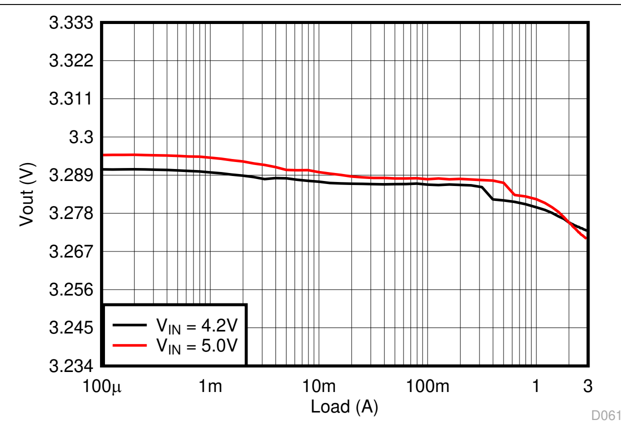
V_{OUT} = 1.8 V FPWM devices

Figure 8-18. Load Regulation



V_{OUT} = 3.3 V

Figure 8-19. Efficiency



V_{OUT} = 3.3 V

Figure 8-20. Load Regulation

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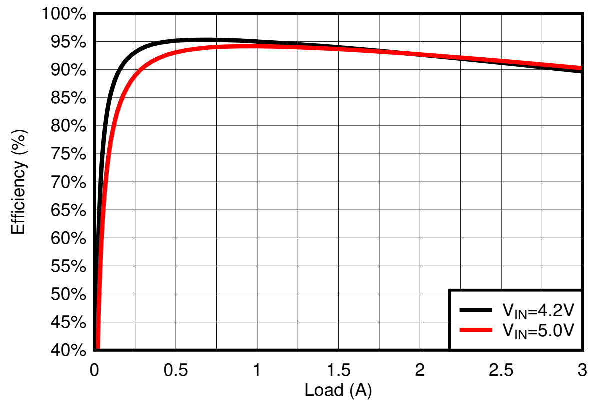
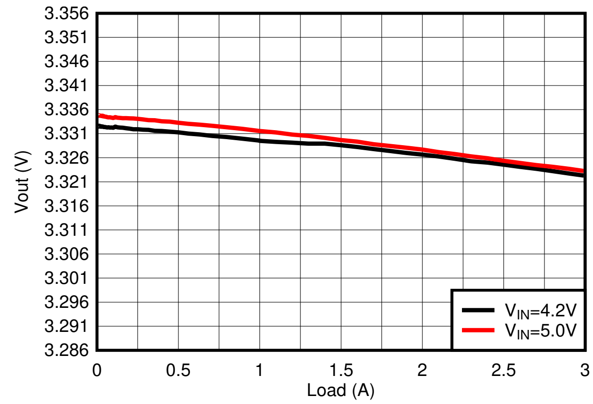


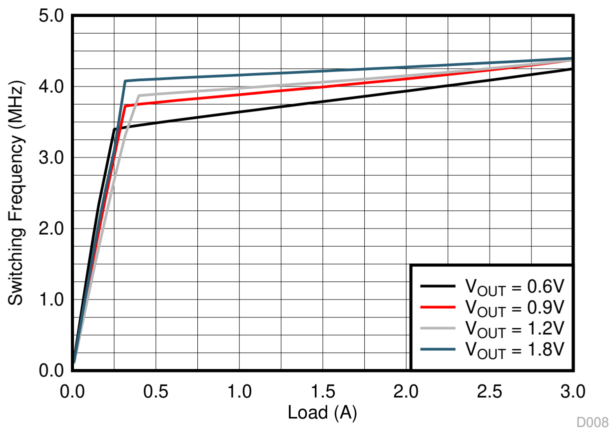
V_{OUT} = 3.32 V FPWM devices

Figure 8-21. Efficiency



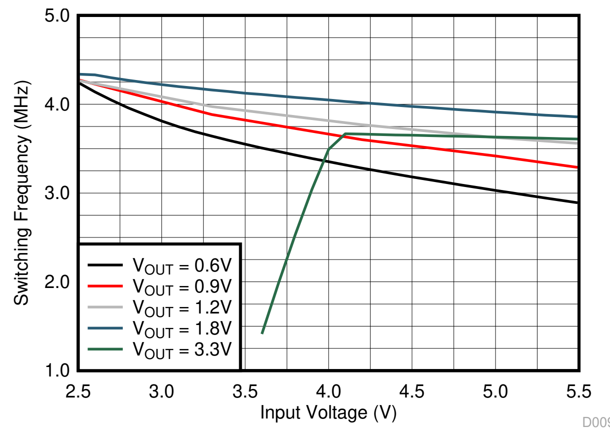
V_{OUT} = 3.32 V FPWM devices

Figure 8-22. Load Regulation



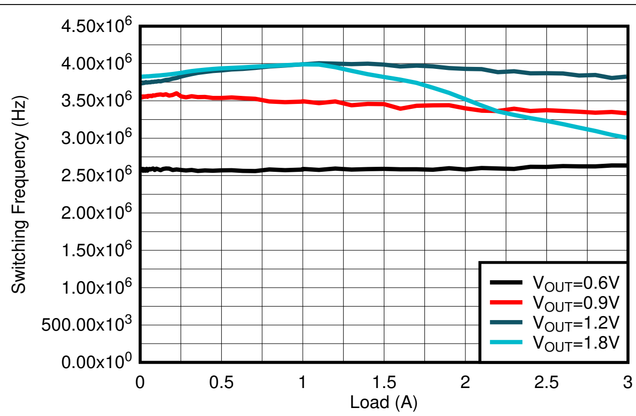
V_{IN} = 3.3 V

Figure 8-23. Switching Frequency



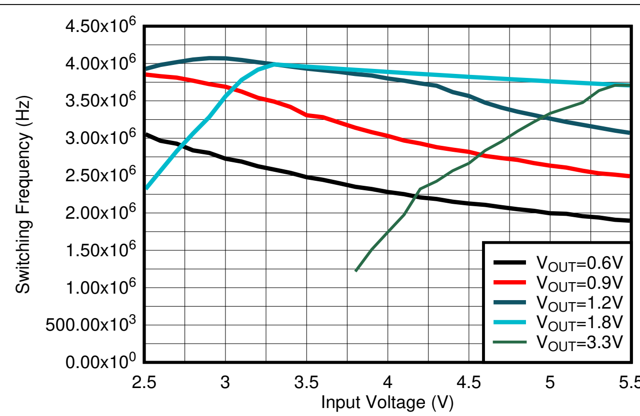
I_{OUT} = 1.0 A

Figure 8-24. Switching Frequency



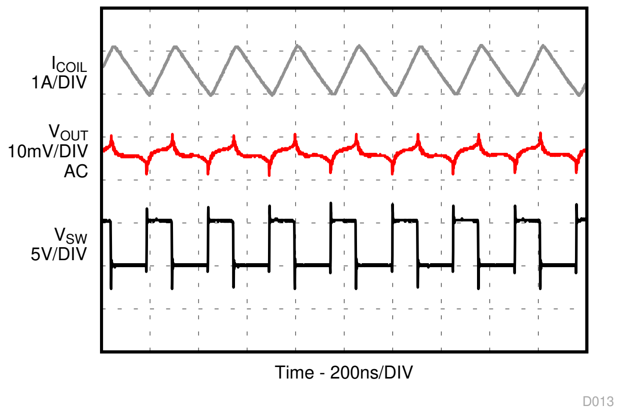
V_{IN} = 3.3 V FPWM devices

Figure 8-25. Switching Frequency



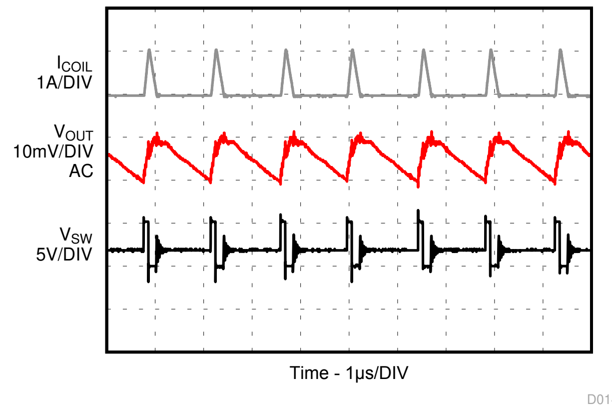
I_{OUT} = 1.0 A FPWM devices

Figure 8-26. Switching Frequency



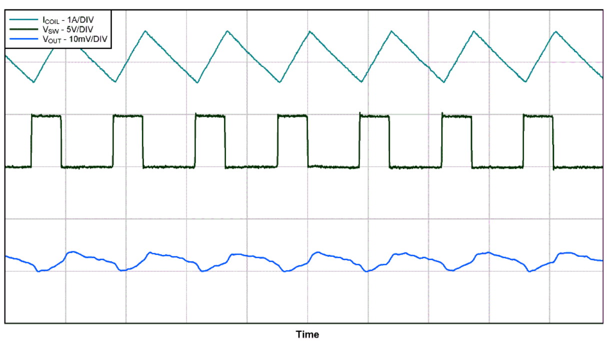
I_{OUT} = 3.0 A

Figure 8-27. PWM Operation



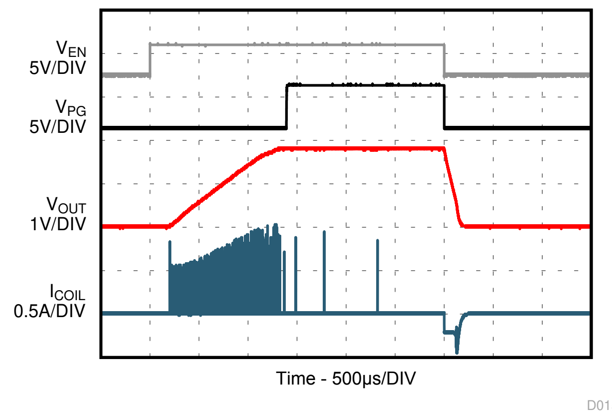
I_{OUT} = 0.1 A

Figure 8-28. PSM Operation



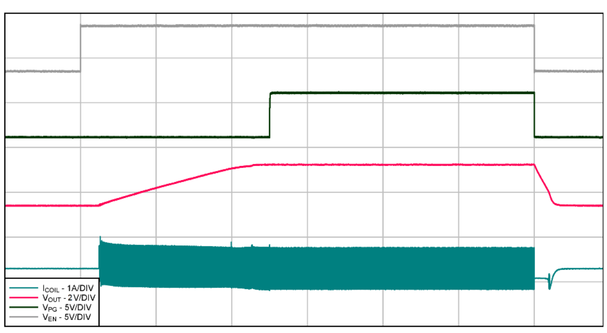
I_{OUT} = 0.1 A FPWM devices

Figure 8-29. FPWM Operation



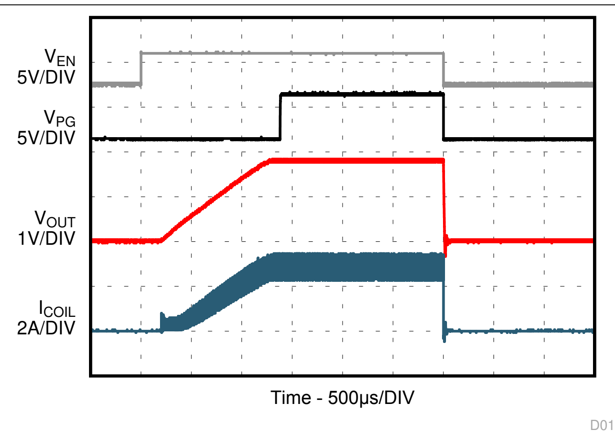
No load

Figure 8-30. Start-Up With No Load



No load FPWM devices

Figure 8-31. Start-Up With No Load



I_{OUT} = 3.0 A

Figure 8-32. Start-Up With Load

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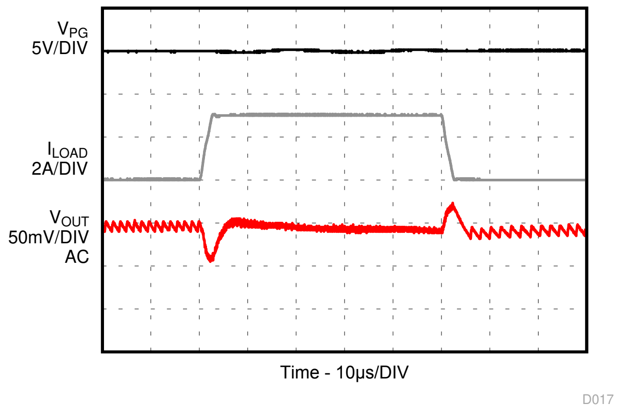
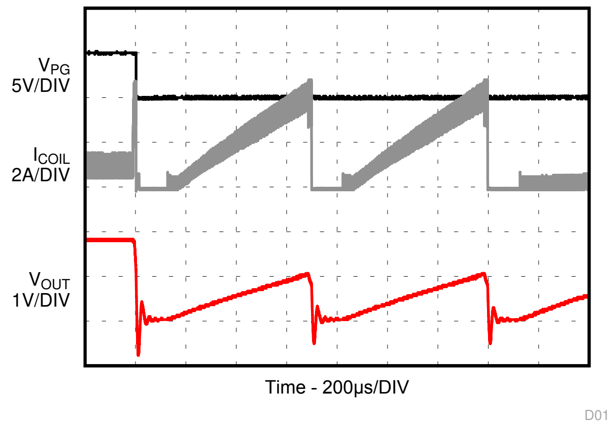


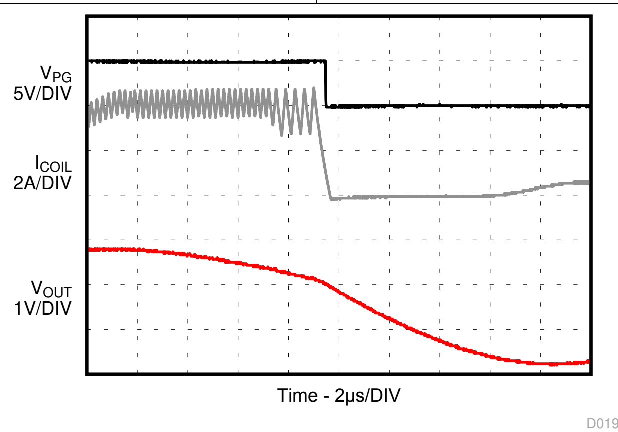
I_{OUT} = 0.1 A to 3 A

Figure 8-33. Load Transient



I_{OUT} = 1 A

Figure 8-34. HICCUP Short-Circuit Protection



I_{OUT} = 1 A

Figure 8-35. HICCUP Short-Circuit Protection (Zoom In)

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. Make sure that the input power supply has a sufficient current rating for the application.

8.4 Layout

8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See Figure 8-36 and Figure 8-37 for the recommended PCB layout.

- Place the input, output capacitors and the inductor as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB is a signal trace. Special care must be taken to avoid noise being induced. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors must be made at the output capacitor.
- Refer to Figure 8-36 and Figure 8-37 for an example of component placement, routing and thermal design.

8.4.2 Layout Example

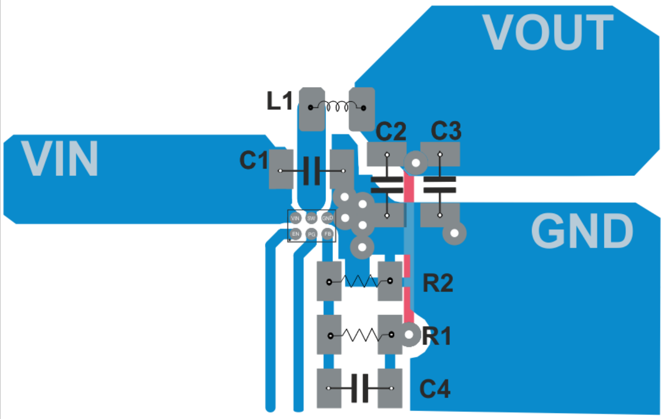


Figure 8-36. PCB Layout of Adjustable Output Voltage Application

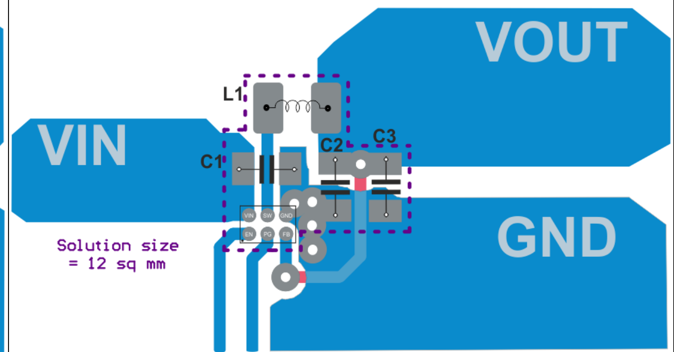


Figure 8-37. PCB Layout of Fixed Output Voltage Application

8.4.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report* and *Semiconductor and IC Package Thermal Metrics Application Report*.

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62088 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2021) to Revision F (November 2024) — **Page**

- Updated the inductor recommendation.......... 12

Changes from Revision D (September 2019) to Revision E (November 2021) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 1
- Added information for the FPWM devices.......... 3
- Added new curves for FPWM devices.......... 14

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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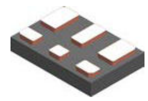
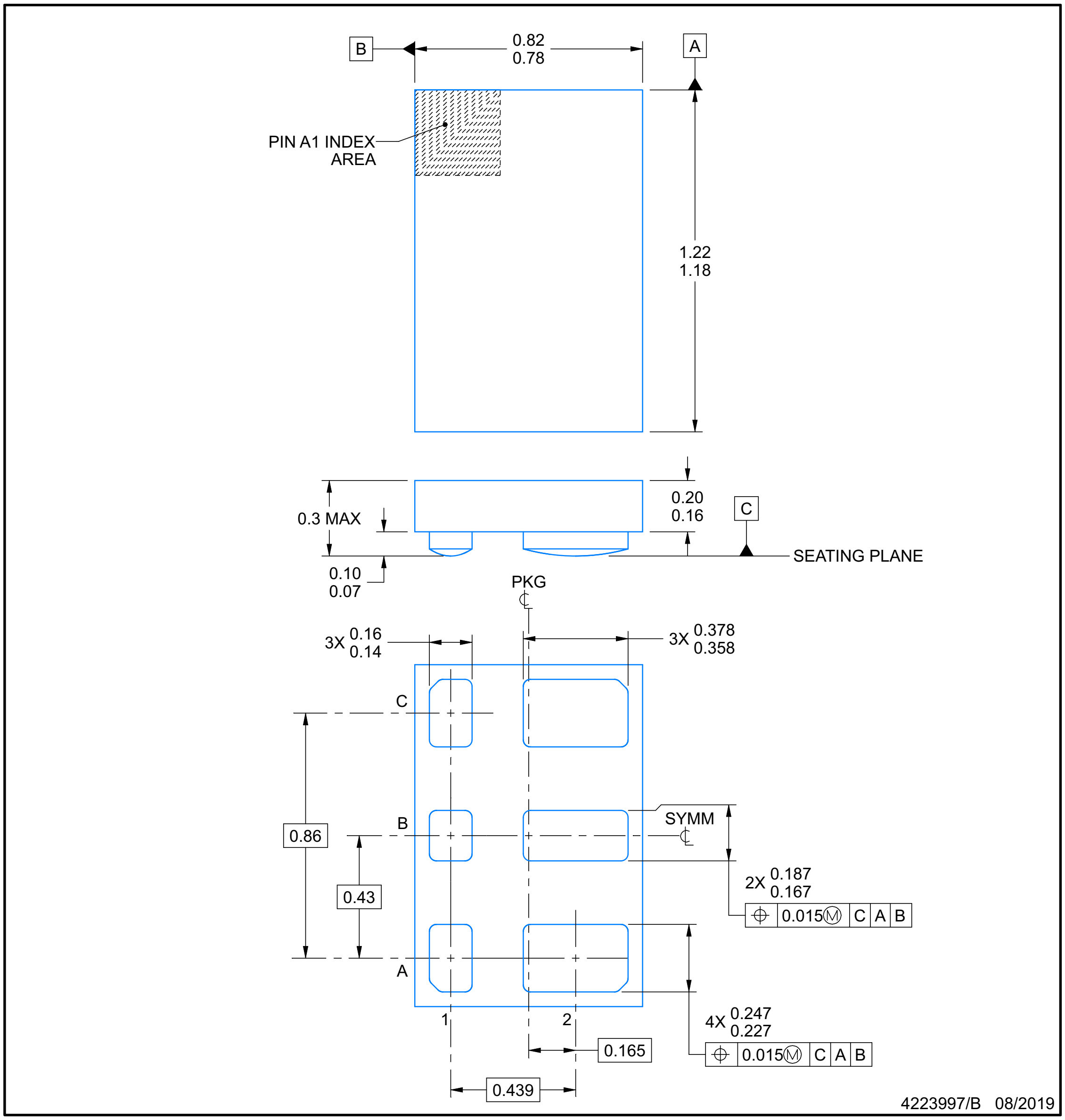


PACKAGE OUTLINE

YWC0006A

PowerWCSP - 0.3 mm max height

POWER CHIP SCALE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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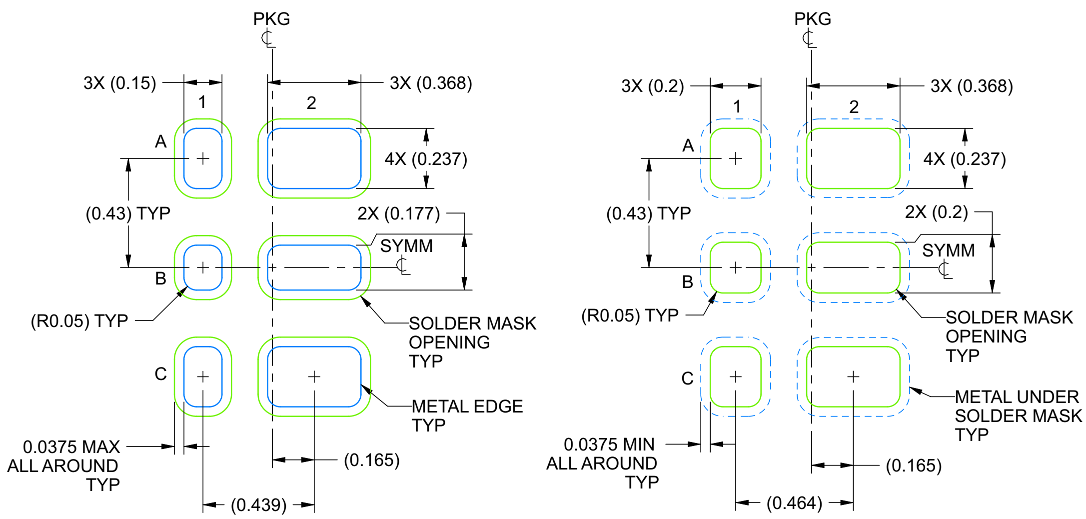
EXAMPLE BOARD LAYOUT

YWC0006A

PowerWCSP - 0.3 mm max height

POWER CHIP SCALE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 40X

LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 40X

4223997/B 08/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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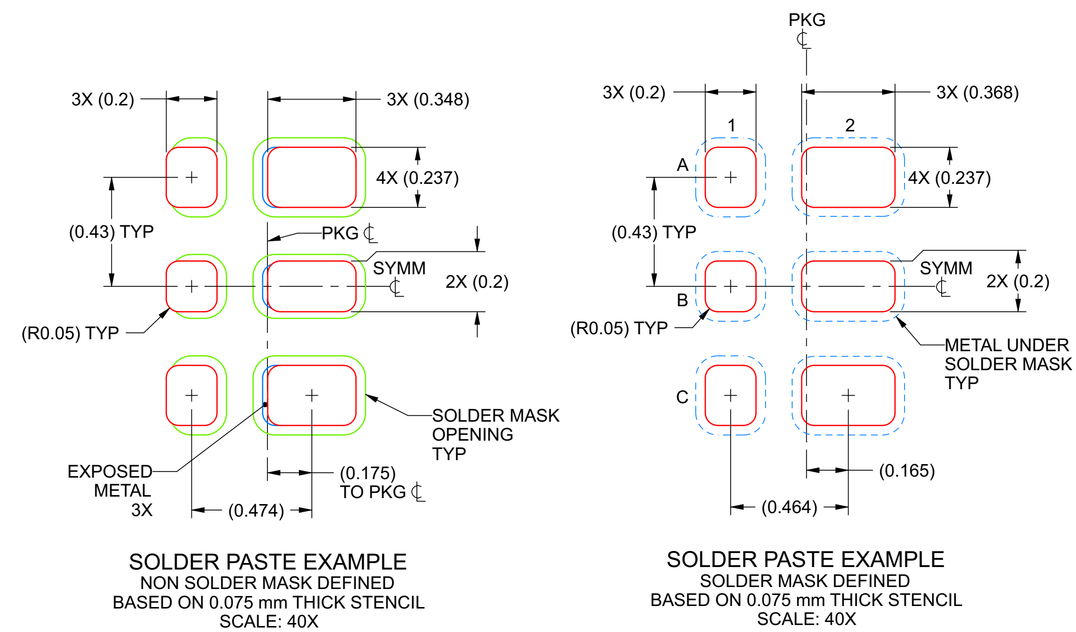
EXAMPLE STENCIL DESIGN

YWC0006A

PowerWCSP - 0.3 mm max height

POWER CHIP SCALE PACKAGE



4223997/B 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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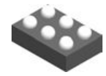
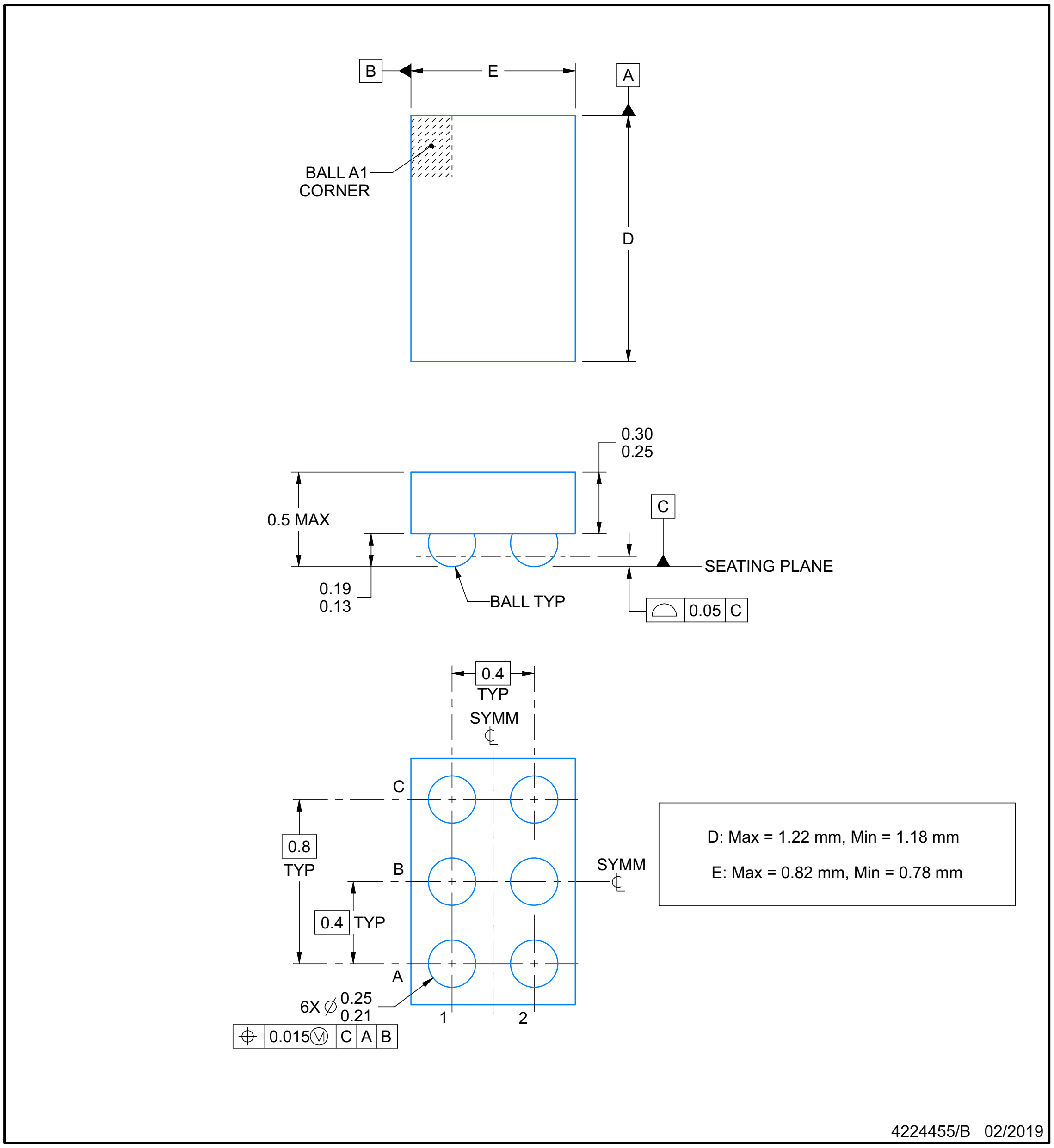


PACKAGE OUTLINE

YFP0006-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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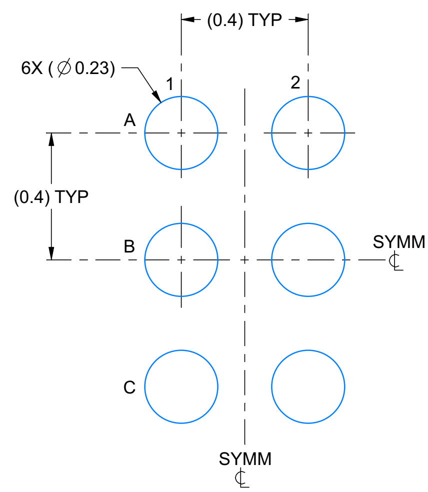
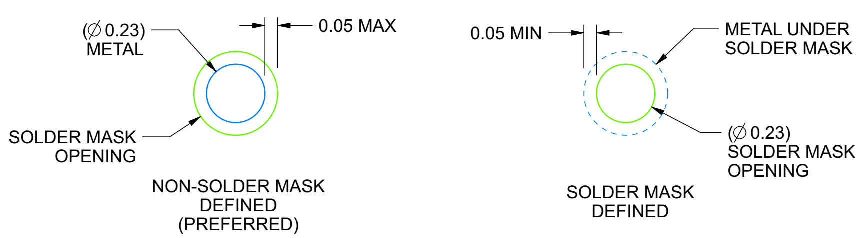
EXAMPLE BOARD LAYOUT

YFP0006-C01 DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4224455/B 02/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

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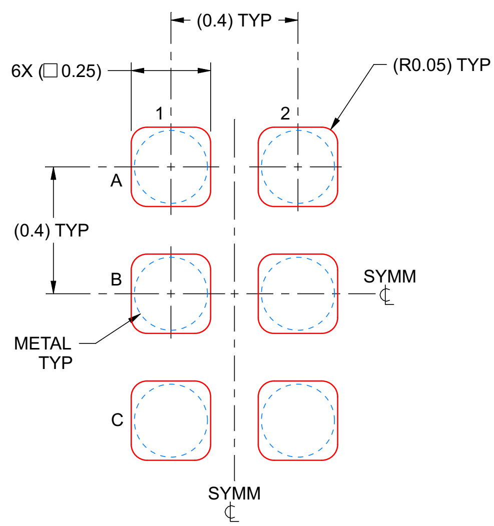
EXAMPLE STENCIL DESIGN

YFP0006-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4224455/B 02/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS6208812YFPR	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B5
TPS6208812YFPR.A	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B5
TPS6208812YFPT	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B5
TPS6208812YFPT.A	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B5
TPS6208818YFPR	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B6
TPS6208818YFPR.A	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B6
TPS6208818YFPT	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B6
TPS6208818YFPT.A	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B6
TPS6208833YFPR	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B7
TPS6208833YFPR.A	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B7
TPS6208833YFPT	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B7
TPS6208833YFPT.A	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1B7
TPS62088AYFPJ	Active	Production	DSBGA (YFP) | 6	6000 | JUMBO T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	W
TPS62088AYFPJ.A	Active	Production	DSBGA (YFP) | 6	6000 | JUMBO T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	W
TPS62088AYFPR	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	W
TPS62088AYFPR.A	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	W
TPS62088YFPR	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	15X
TPS62088YFPR.A	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	15X
TPS62088YFPT	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	15X
TPS62088YFPT.A	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	15X
TPS62088YWCR	Active	Production	DSBGA (YWC) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1GB
TPS62088YWCR.A	Active	Production	DSBGA (YWC) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1GB
TPS62089AYFPR	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X
TPS62089AYFPR.A	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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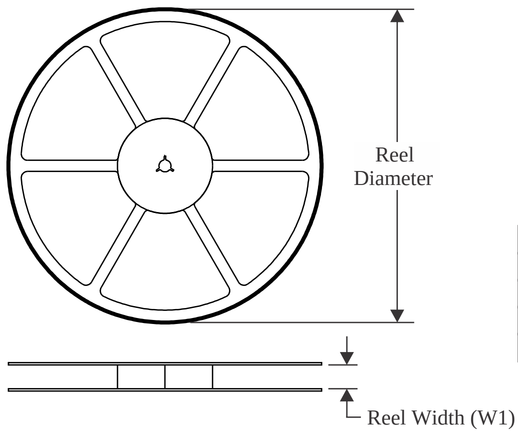
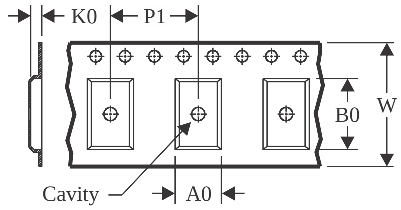
TAPE AND REEL INFORMATION

REEL DIMENSIONS

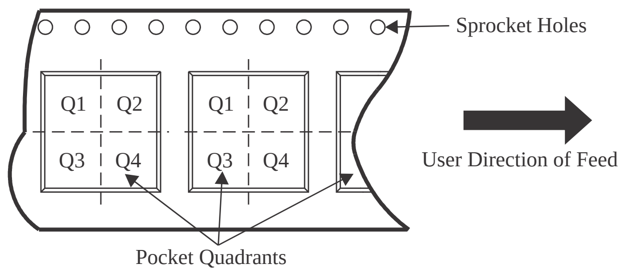


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

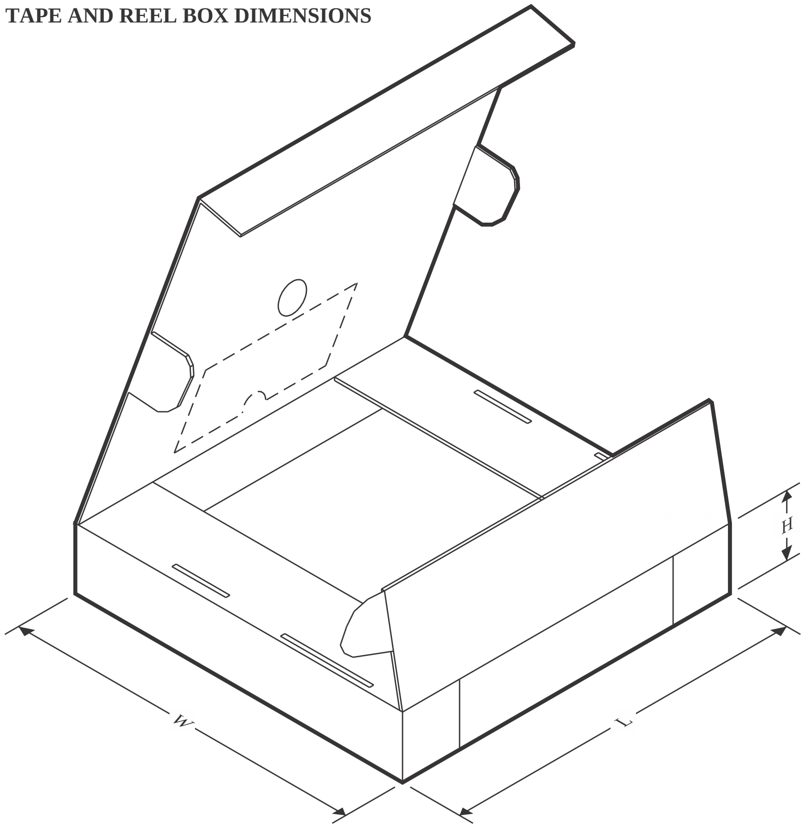
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6208812YFPR	DSBGA	YFP	6	3000	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1
TPS6208812YFPT	DSBGA	YFP	6	250	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1
TPS6208818YFPR	DSBGA	YFP	6	3000	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1
TPS6208818YFPT	DSBGA	YFP	6	250	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1
TPS6208833YFPR	DSBGA	YFP	6	3000	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1
TPS6208833YFPT	DSBGA	YFP	6	250	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1
TPS62088AYFPJ	DSBGA	YFP	6	6000	180.0	8.4	0.89	1.31	0.57	2.0	8.0	Q1
TPS62088AYFPR	DSBGA	YFP	6	3000	180.0	8.4	0.89	1.31	0.57	2.0	8.0	Q1
TPS62088YFPR	DSBGA	YFP	6	3000	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1
TPS62088YFPT	DSBGA	YFP	6	250	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1
TPS62088YWCR	DSBGA	YWC	6	3000	180.0	8.4	0.95	1.35	0.38	4.0	8.0	Q1
TPS62089AYFPR	DSBGA	YFP	6	3000	180.0	8.4	0.89	1.31	0.57	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6208812YFPR	DSBGA	YFP	6	3000	182.0	182.0	20.0
TPS6208812YFPT	DSBGA	YFP	6	250	182.0	182.0	20.0
TPS6208818YFPR	DSBGA	YFP	6	3000	182.0	182.0	20.0
TPS6208818YFPT	DSBGA	YFP	6	250	182.0	182.0	20.0
TPS6208833YFPR	DSBGA	YFP	6	3000	182.0	182.0	20.0
TPS6208833YFPT	DSBGA	YFP	6	250	182.0	182.0	20.0
TPS62088AYFPJ	DSBGA	YFP	6	6000	182.0	182.0	20.0
TPS62088AYFPR	DSBGA	YFP	6	3000	182.0	182.0	20.0
TPS62088YFPR	DSBGA	YFP	6	3000	182.0	182.0	20.0
TPS62088YFPT	DSBGA	YFP	6	250	182.0	182.0	20.0
TPS62088YWCR	DSBGA	YWC	6	3000	182.0	182.0	20.0
TPS62089AYFPR	DSBGA	YFP	6	3000	182.0	182.0	20.0

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