HIGH-EFFICIENCY STEP-DOWN LOW POWER DC-DC CONVERTER

FEATURES

- **High-Efficiency Synchronous Step-Down Converter With Greater Than 95% Efficiency**
- **2 V to 5.5 V Operating Input Voltage Range**
- **Adjustable Output Voltage Range From 0.8 V to V_I**
- **Synchronizable to External Clock Signal up to 1 MHz**
- **Up to 300 mA Output Current**
- **Pin-Programmable Current Limit**
- **High Efficiency Over a Wide Load Current Range in Power Save Mode**
- **100% Maximum Duty Cycle for Lowest Dropout**
- **Low-Noise Operation Antiringing Switch and PFM/PWM Operation Mode**
- **Internal Softstart**
- **50-μA Quiescent Current (TYP)**
- **Evaluation Module Available for Commercial Temperature Range**

APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

(1) Custom temperature ranges available

DESCRIPTION

The TPS62000 device is a low-noise synchronous step-down dc-dc converter that is ideally suited for systems powered from a 1-cell Li-ion battery or from a 2- to 3-cell NiCd, NiMH, or alkaline battery. The TPS62000 operates typically down to an input voltage of 1.8 V, with a specified minimum input voltage of 2 V.

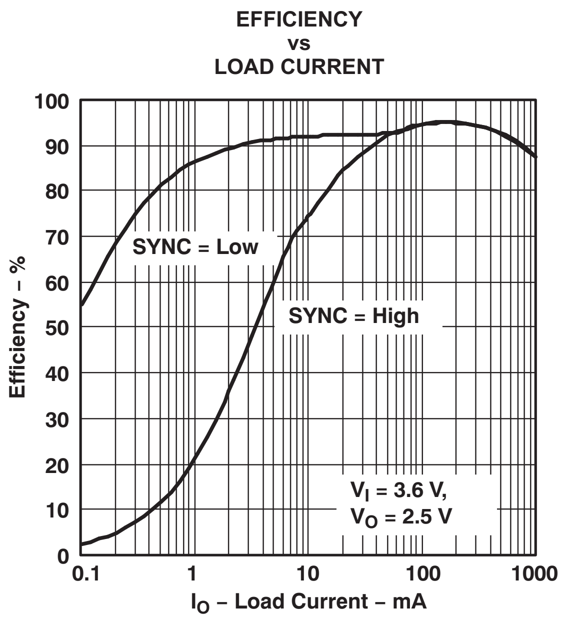


Figure 1.

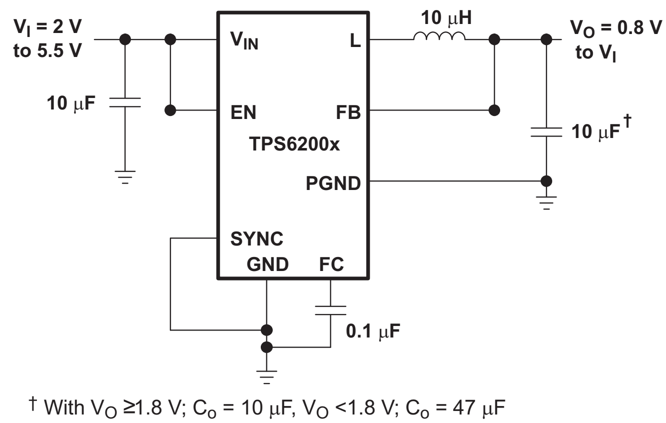
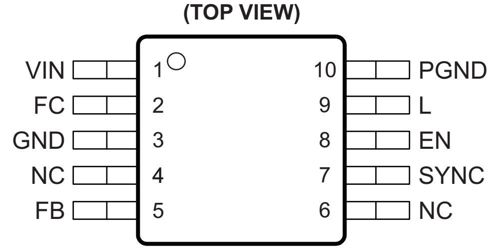


Figure 2. Typical Application Circuit for Fixed Output Voltage Option

DESCRIPTION (CONTINUED)

The TPS62000 is a synchronous current-mode PWM converter with integrated N- and P-channel power MOSFET switches. Synchronous rectification is used to increase efficiency and to reduce external component count. To achieve the highest efficiency over a wide load current range, the converter enters a power-saving pulse-frequency modulation (PFM) mode at light load currents. Operating frequency is typically 750 kHz, allowing the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500 kHz to 1 MHz. For low-noise operation, the converter can be operated in the PWM mode and the internal antiringing switch reduces noise and EMI. In the shutdown mode, the current consumption is reduced to less than 1 µA. The TPS62000-HT is available in the 10-pin (HKK). The dvice operates a free-air temperature range of –55Â°C to 210Â°C.

HKK PACKAGE
(TOP VIEW)

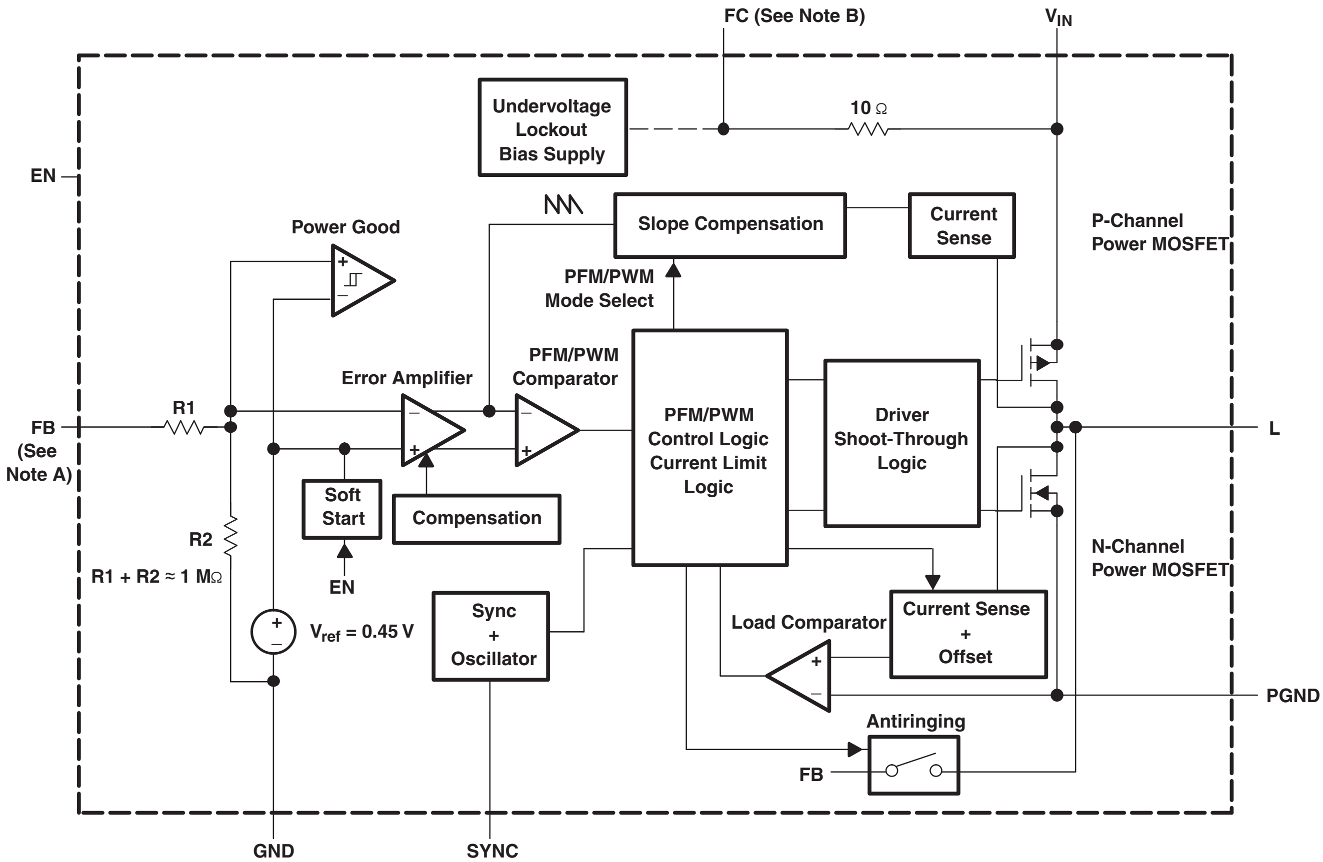


AVAILABLE OPTIONS(1)

T_A	VOLTAGE OPTIONS	PACKAGE(2)	ORDERING PART NUMBER
–55°C to 210°C	Adjustable	KGD	TPS62000SKGD1
		HKK	TPS62000SHKK

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM



A. The adjustable output voltage version does not use the internal feedback resistor divider. The FB pin is directly connected to the error amplifier.

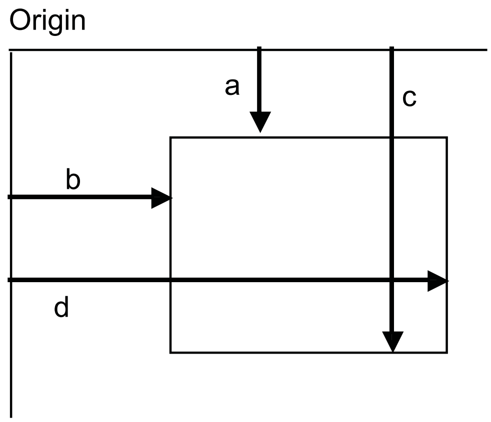
B. Do not connect the FC pin to an external power source

PIN FUNCTIONS

PIN NAME	I/O	DESCRIPTION
EN	I	Enable. A logic high enables the converter, logic low forces the device into shutdown mode reducing the supply current to less than 1 µA.
FB	I	An external resistive divider is connected to FB. The internal voltage divider is disabled.
FC		Supply bypass pin. A 0.1 µF coupling capacitor should be connected as close as possible to this pin for good high frequency input voltage supply filtering.
GND		Ground.
L	I/O	Connect the inductor to this pin. L is the switch pin connected to the drain of the internal power MOSFETS.
PGND		Power ground. Connect all power grounds to PGND.
SYNC	I	Input for synchronization to external clock signal. Synchronizes the converter switching frequency to an external clock signal with CMOS level: SYNC = HIGH: Low-noise mode enabled, fixed frequency PWM operation is forced. SYNC = LOW (GND): Power save mode enabled, PFM/PWM mode enabled.
V_{IN}	I	Supply voltage input.

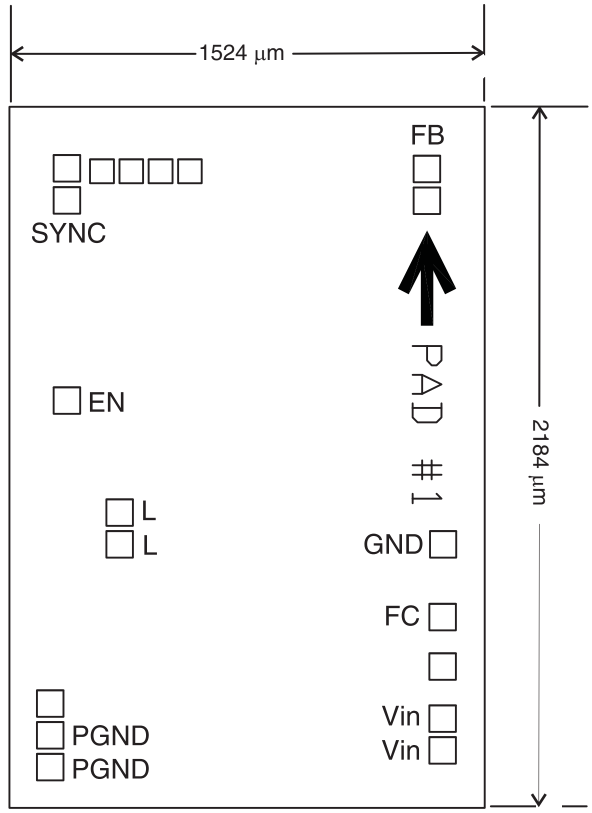
BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	GND	Al-Si-Cu (0.5%)



Bond Pad Coordinates in Microns - Rev A

DESCRIPTION	PAD NUMBER	a	b	c	d
FB	1	142.15	92.40	227.15	177.40
Do not use	2	142.15	194.40	227.15	279.40
Do not use	3	907.35	104.05	983.35	180.05
Do not use	4	1001.35	104.05	1077.35	180.05
Do not use	5	1095.35	104.05	1171.35	180.05
Do not use	6	1189.35	104.05	1265.35	180.05
Do not use	7	1296.85	90.60	1381.85	175.60
SYNC	8	1296.85	192.60	1381.85	277.60
EN	9	1296.85	835.10	1381.85	920.10
L	10	1128.20	1194.55	1213.20	1279.55
L	11	1128.20	1296.55	1213.20	1381.55
Do not use	12	1350.50	1806.50	1435.50	1891.50
PGND	13	1350.50	1908.50	1435.50	1993.50
PGND	14	1350.50	2010.50	1435.50	2095.50
Vin	15	92.40	1956.85	177.40	2041.85
Vin	16	92.40	1854.85	177.40	1939.85
Do not use	17	92.40	1687.70	177.40	1772.70
FC	18	92.40	1529.00	177.40	1614.00
GND	19	90.60	1295.70	175.60	1380.70


1524 µm
2184 µm
FB
SYNC
PAD #1
EN
L
L
GND
FC
Vin
Vin
PGND
PGND

DETAILED DESCRIPTION

Operation

The TPS62000 is a step down converter operating in a current mode PFM/PWM scheme with a typical switching frequency of 750 kHz.

At moderate to heavy loads, the converter operates in the pulse width modulation (PWM) and at light loads the converter enters a power save mode (pulse frequency modulation) to keep the efficiency high.

In the PWM mode operation, the part operates at a fixed frequency of 750 kHz. At the beginning of each clock cycle, the high side P-channel MOSFET is turned on. The current in the inductor ramps up and is sensed via an internal circuit. The high side switch is turned off when the sensed current causes the PFM/PWM comparator to trip when the output voltage is in regulation or when the inductor current reaches the current limit (set by ILIM). After a minimum dead time preventing shoot through current, the low side N-channel MOSFET is turned on and the current ramps down again. As the clock cycle is completed, the low side switch is turned off and the next clock cycle starts.

In discontinuous conduction mode (DCM), the inductor current ramps to zero before the end of each clock cycle. In order to increase the efficiency the load comparator turns off the low side MOSFET before the inductor current becomes negative. This prevents reverse current flowing from the output capacitor through the inductor and low side MOSFET to ground that would cause additional losses.

As the load current decreases and the peak inductor current does not reach the power save mode threshold of typically 120 mA for more than 15 clock cycles, the converter enters a pulse frequency modulation (PFM) mode.

In the PFM mode, the converter operates with:

- Variable frequency
- Constant peak current that reduces switching losses
- Quiescent current at a minimum

Thus maintaining the highest efficiency at light load currents. In this mode, the output voltage is monitored with the error amplifier. As soon as the output voltage falls below the nominal value, the high side switch is turned on and the inductor current ramps up. When the inductor current reaches the peak current of typical: 150 mA + 50 mA/V × (V_I – V_O), the high side switch turns off and the low side switch turns on. As the inductor current ramps down, the low side switch is turned off before the inductor current becomes negative which completes the cycle. When the output voltage falls below the nominal voltage again, the next cycle is started.

The converter enters the PWM mode again as soon as the output voltage can not be maintained with the typical peak inductor current in the PFM mode.

The control loop is internally compensated reducing the amount of external components.

The switch current is internally sensed and the maximum current limit can be set to typical 600 mA by connecting ILIM to ground; or, to typically 1.2 A by connecting ILIM to V_{IN}.

100% Duty Cycle Operation

As the input voltage approaches the output voltage and the duty cycle exceeds typical 95%, the converter turns the P-channel high side switch continuously on. In this mode, the output voltage is equal to the input voltage minus the voltage drop across the P-channel MOSFET.

Synchronization, Power Save Mode and Forced PWM Mode

If no clock signal is applied, the converter operates with a typical switching frequency of 750 kHz. It is possible to synchronize the converter to an external clock within a frequency range from 500 kHz to 1000 kHz. The device automatically detects the rising edge of the first clock and is synchronizes immediately to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation without interruption. The switch over is initiated if no rising edge on the SYNC pin is detected for a duration of four clock cycles. Therefore, the maximum delay time can be 8 µs in case the internal clock has a minimum frequency of 500 kHz.

In case the device is synchronized to an external clock, the power save mode is disabled and the device stays in forced PWM mode.

Connecting the SYNC pin to the GND pin enables the power save mode. The converter operates in the PWM mode at moderate to heavy loads and in the PFM mode during light loads maintaining high efficiency over a wide load current range.

Connecting the SYNC pin to the V_{IN} pin forces the converter to operate permanently in the PWM mode even at light or no load currents. The advantage is the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads (see Figure 1).

It is possible to switch from forced PWM mode to the power save mode during operation.

The flexible configuration of the SYNC pin during operation of the device allows efficient power management by adjusting the operation of the TPS62000 to the specific system requirements.

Low Noise Antiringing Switch

An *antiringing* switch is implemented in order to reduce the EMI radiated from the converter during discontinuous conduction mode (DCM). In DCM, the inductor current ramps to zero before the end of each switching period. The internal load comparator turns off the low side switch at that instant thus preventing the current flowing backward through the inductance which increases the efficiency. An antiringing switch across the inductor prevents parasitic oscillation caused by the residual energy stored in the inductance (see Figure 12).

NOTE:

The *antiringing* switch is only activated in the fixed output voltage versions. It is not enabled for the adjustable output voltage version TPS62000.

Soft Start

As the enable pin (EN) goes high, the soft-start function generates an internal voltage ramp. This causes the start-up current to slowly rise preventing output voltage overshoot and high inrush currents. The soft-start duration is typical 1 ms (see Figure 13). When the soft-start function is completed, the error amplifier is connected directly to the internal voltage reference.

Enable

Logic low on EN forces the TPS62000 into shutdown. In shutdown, the power switch, drivers, voltage reference, oscillator, and all other functions are turned off. The supply current is reduced to less than 1 µA in the shutdown mode.

Undervoltage Lockout

An undervoltage lockout circuit provides the save operation of the device. It prevents the converter from turning on when the voltage on V_{IN} is less than typically 1.6 V.

No Load Operation

In case the converter operates in the forced PWM mode and there is no load connected to the output, the converter will regulate the output voltage by allowing the inductor current to reverse for a short period of time.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[(1)]

	VALUE	UNIT
Supply voltages on pin VIN and FC[(2)]	–0.3 to 6	V
Voltages on pins EN, SYNC, FB, L[(2)]	–0.3 to V_{IN} + 0.3	V
Peak switch current	1.6	A

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		T_A = –55°C to 125°C			T_A = 210°C[(1)]			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_I	Supply voltage	2		5.5	2		5.5	V
V_O	Output voltage range for adjustable output voltage version	0.8		V_I	0.8		V_I	V
I_O	Output current for 3-cell operation (V_I ≥ 2.5 V; L = 10 µH, f = 750 kHz)			300			300	mA
I_O	Output current for 2-cell operation (V_I ≥ 2 V; L = 10 µH, f = 750 kHz)			200			200	mA
L	Inductor[(2)] (see Note 2)		10			10		µH
C_I	Input capacitor[(2)]	10			10			µF
C_o	Output capacitor[(2)] (V_O ≥ 1.8 V)	10			10			µF
C_o	Output capacitor[(2)] V_O < 1.8 V)	47			47			µF
T_A	Operating ambient temperature	–55		210	–55		210	°C

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Refer to application section for further information.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless oherwise noted), V_I = 3.6 V, V_O = 2.5 V, I_O = 300 mA (T_A = –55°C to 125°C), I_O = 50 mA (T_A = 210°C), EN = V_{IN}

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C MIN	TYP	MAX	T_A = 210°C(1) MIN	TYP	MAX	UNIT
SUPPLY CURRENT									
V_I	Input voltage range	I_O = 0 mA to 300 mA	2.5		5.5	2.5		5.5	V
		I_O = 0 mA to 200 mA	2		5.5	2		5.5	
$I_{(Q)}$	Operating quiescent current	I_O = 0 mA, SYNC = GND (PFM-mode enabled)		50	75		1400	4000	µA
$I_{(SD)}$	Shutdown current	EN = GND		0.1	1		90	200	µA
ENABLE									
V_{IH}	EN high-level input voltage		1.5			1.5			V
V_{IL}	EN low level input voltage				0.4			0.4	V
I_{lkg}	EN input leakage current	EN = GND or V_{IN}		0.1	1.1		0.1	1.1	µA
$V_{(UVLO)}$	Undervoltage lockout threshold		1.2	1.6	2	1.2	1.6	2	V
POWER SWITCH AND CURRENT LIMIT									
$r_{DS(on)}$	P-channel MOSFET on-resistance	V_I = V_{GS} = 3.6 V, I = 200 mA		580			670(2)		mΩ
		V_I = V_{GS} = 2 V, I = 200 mA		790			850(2)		
	N-channel MOSFET on-resistance	V_I = V_{GS} = 3.6 V, I_O = 200 mA		580			670(2)		mΩ
		V_I = V_{GS} = 2 V, I_O = 200 mA		790			800(2)		
OSCILLATOR									
f_s	Oscillator frequency		500	750	1000	200	320	600	kHz
$f_{(SYNC)}$	Synchronization range	CMOS-logic clock signal on SYNC pin	500		1000	500		1000	kHz
V_{IH}	SYNC high level input voltage		1.3			1.3			V
V_{IL}	SYNC low level input voltage				0.4			0.4	V
I_{lkg}	SYNC input leakage current	SYNC = GND or V_{IN}		0.1	1.1		0.1	1.1	µA
	Duty cycle of external clock signal		20%		60%	20%		60%	

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Measured at 50 mA.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted), V_I = 3.6 V, V_O = 2.5 V, I_O = 300 mA (T_A = –55°C to 125°C), I_O = 50 mA (T_A = 210°C), EN = V_{IN}, ILIM = V_{IN}

PARAMETER			TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C[(1)]			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Adjustable output voltage range	TPS62000		0.8		5.5	0.8		5.5	V
V_{ref}	Reference voltage	TPS62000			0.45			0.38		V
V_O	Fixed output voltage [(2)]	TPS62000 adjustable	V_I = 2.5 V to 5.5 V; 0 mA ≤ I_O ≤ 100 mA	–5.5		5				%V
			10 mA < I_O ≤ 300 mA	–5.5		5		15[(3)]		
	Line regulation		V_I = V_O + 0.5 V (min. 2 V) to 5.5 V, I_O = 10 mA		0.05			13[(4)]		%/V
	Load regulation		V_I = 5.5 V; I_O = 10 mA to 300 mA		0.6%			23%[(4)]		
η	Efficiency		V_I = 5 V; V_O = 3.3 V; I_O = 300 mA		85%			73%		
			VI = 3.6 V; V_O = 2.5 V; I_O = 200 mA							
	Start-up time		I_O = 0 mA, time from active EN to V_O	0.4		2		0.75		ms

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) The output voltage accuracy includes line and load regulation over the full temperature range, T_A = –55°C to 125°C.
(3) V_{IN} = 5.5 V
(4) V_{IN} = 3.3 V to 5.5 V, I_O = 100 mA to 300 mA

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
η	Efficiency	vs Load current	3, 4, 5
$V_{(drop)}$	Dropout voltage	vs Load current	6
I_Q	Operating quiescent current	vs Input voltage (power save mode)	7
		vs Input voltage (forced PWM)	8
f_{OSC}	Oscillator frequency	vs Free-air temperature	9
	Load transient response		10
	Line transient response		11
	Power save mode operation		12
	Start-up	vs Time	13
V_O	Output voltage	vs Load current	14

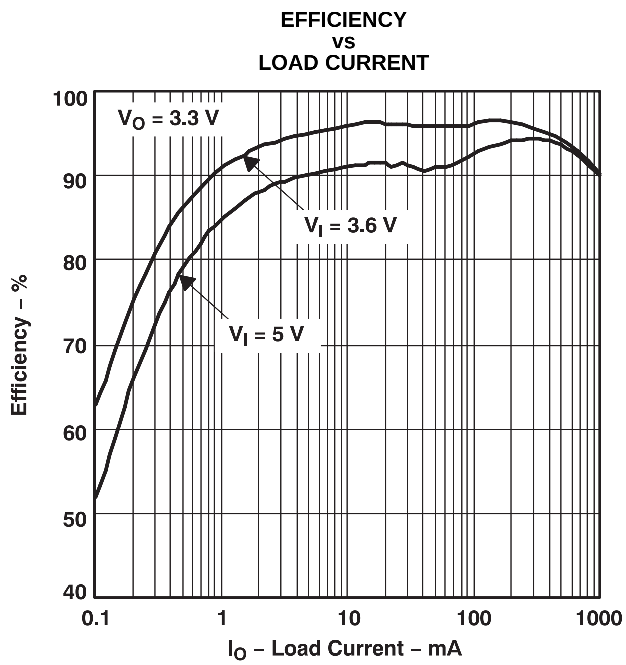


Figure 3.

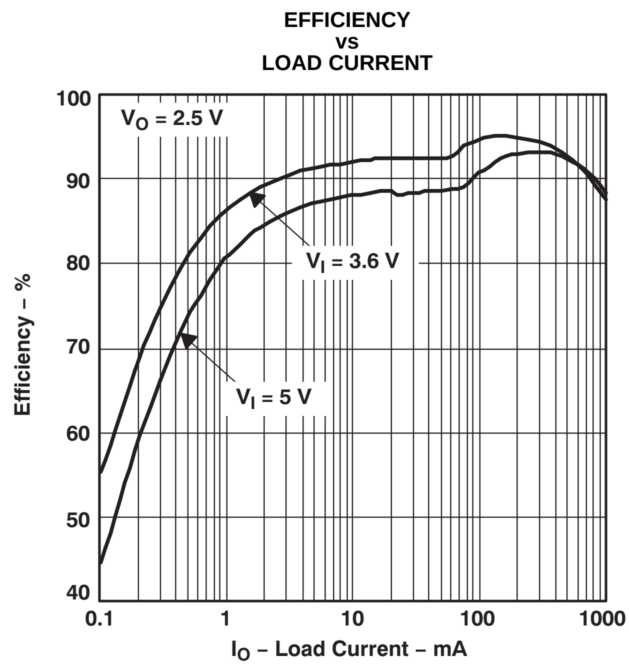


Figure 4.

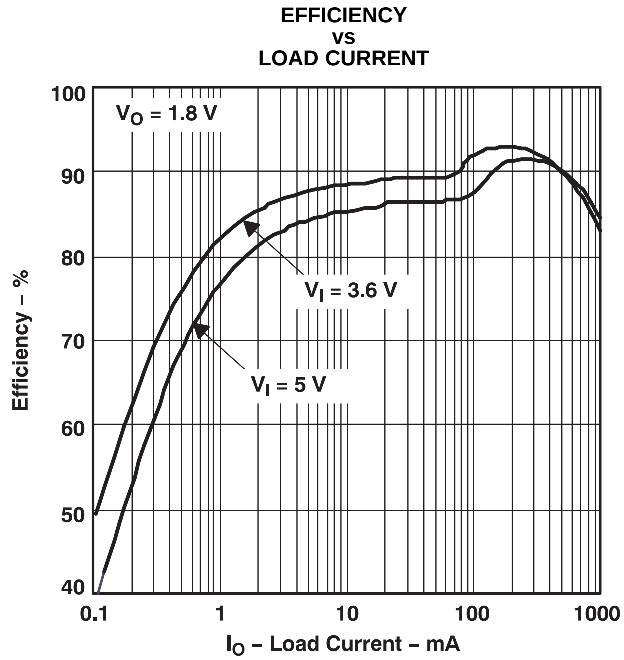


Figure 5.

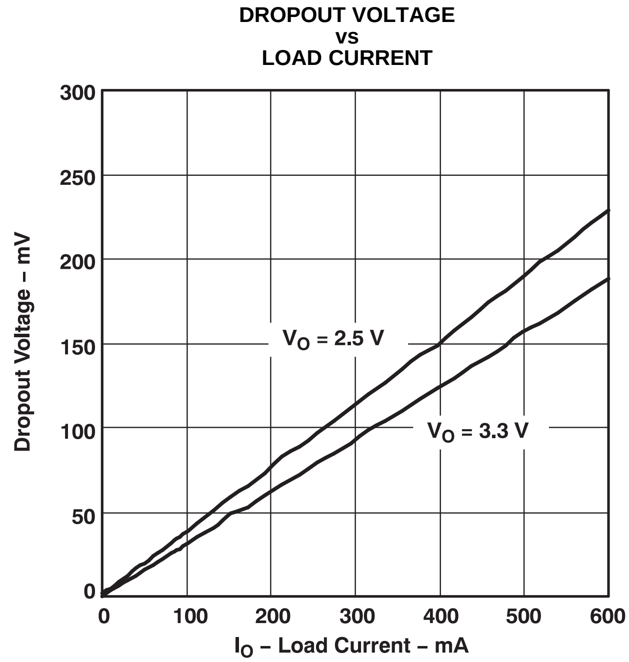


Figure 6.

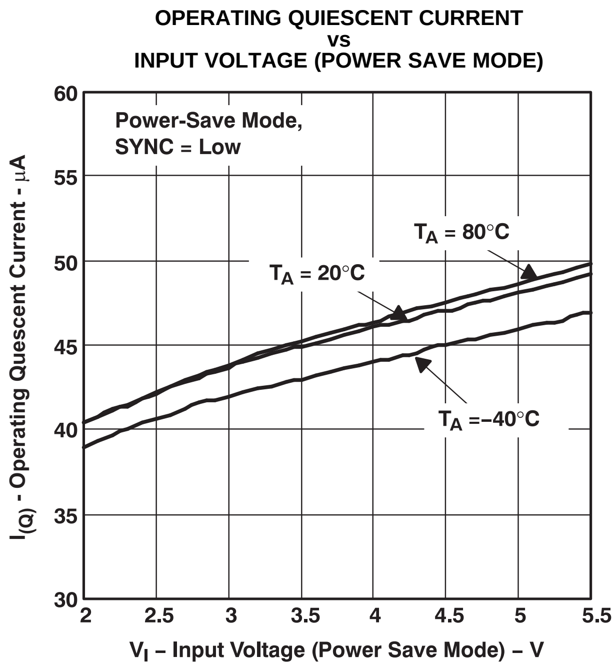


Figure 7.

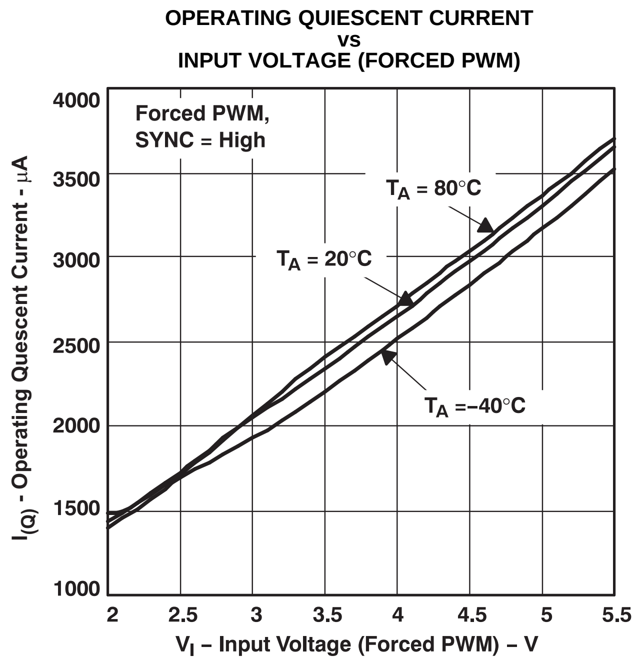


Figure 8.

OSCILLATOR FREQUENCY
vs
FREE-AIR TEMPERATURE

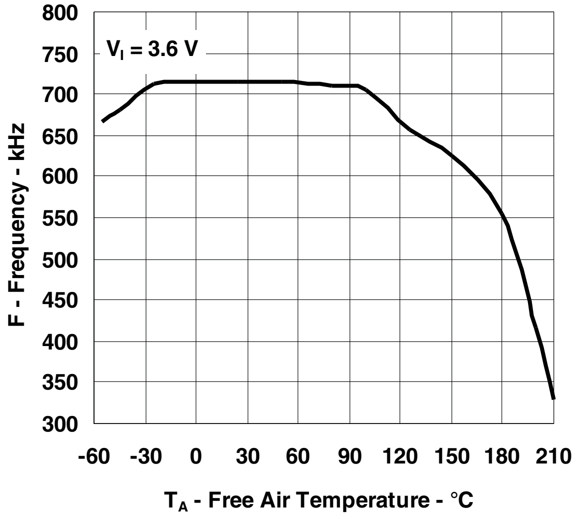


Figure 9.

LOAD TRANSIENT RESPONSE

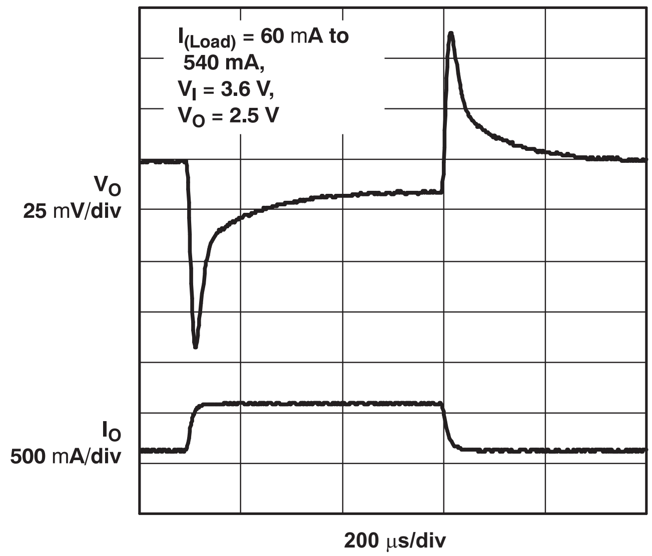


Figure 10.

LINE TRANSIENT RESPONSE

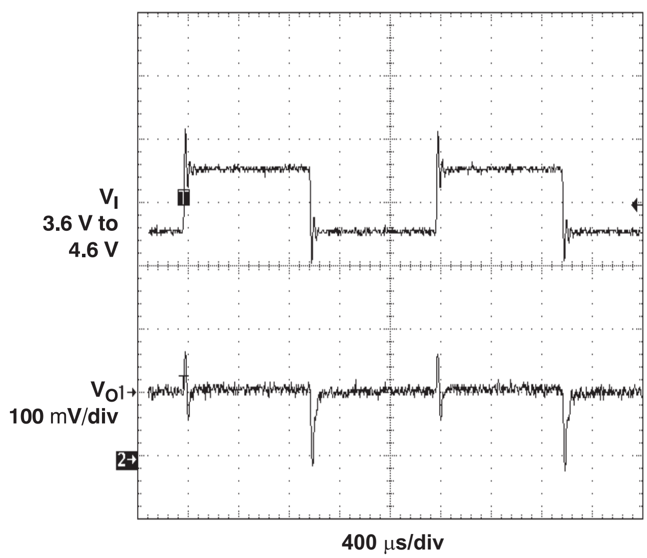


Figure 11.

POWER SAVE MODE OPERATION

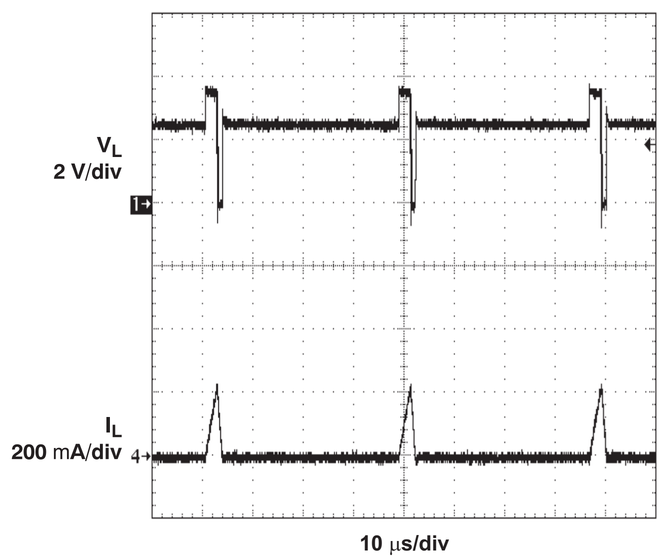


Figure 12.

START-UP
vs
TIME

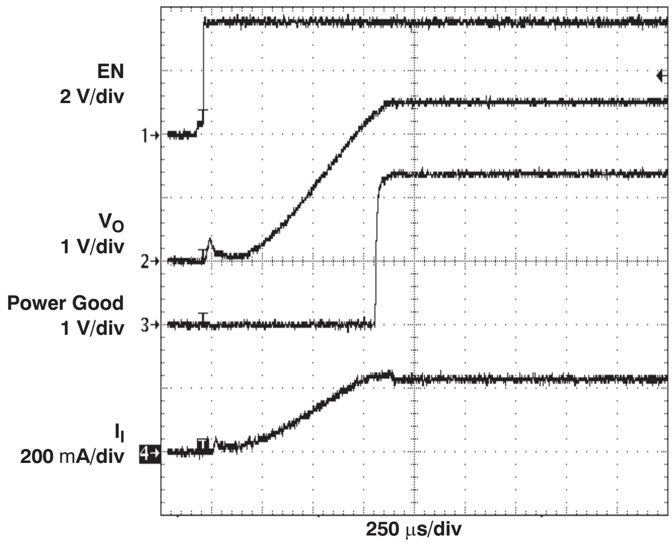


Figure 13.

OUTPUT VOLTAGE
vs
LOAD CURRENT

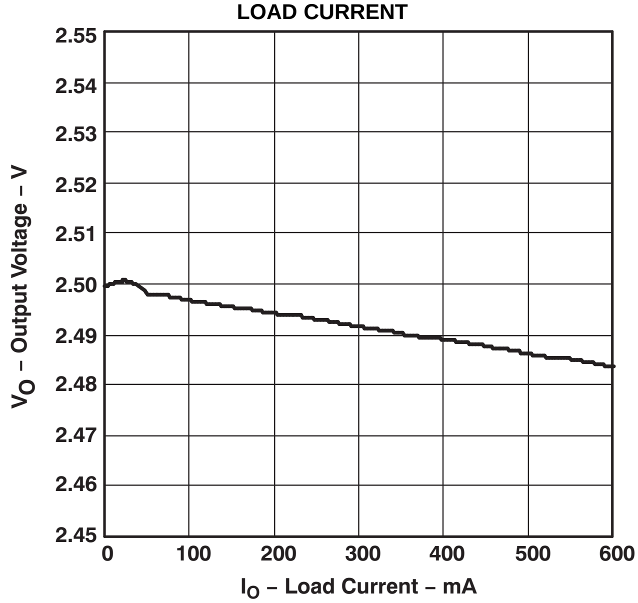


Figure 14.

APPLICATION INFORMATION(1)

ADJUSTABLE OUTPUT VOLTAGE VERSION

When the adjustable output voltage version (TPS62000DGS) is used, the output voltage is set by the external resistor divider (see Figure 15).

The output voltage is calculated as:

$$V_O = 0.45\ V \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

With R1 + R2 ≤ 1 MΩ

R1 + R2 should not be greater than 1 MW because of stability reasons.

For stability reasons, a small bypass capacitor ($C_{(ff)}$) is required in parallel to the upper feedback resistor, refer to Figure 15. The bypass capacitor value can be calculated as:

$$C_{(ff)} = \frac{1}{2\pi \times 30000 \times R1} \text{ for } C_o < 47\mu F \quad (2)$$

$$C_{(ff)} = \frac{1}{2\pi \times 5000 \times R1} \text{ for } C_o \geq 47\mu F \quad (3)$$

R1 is the upper resistor of the voltage divider. For $C_{(ff)}$, choose a value which comes closest to the computed result.

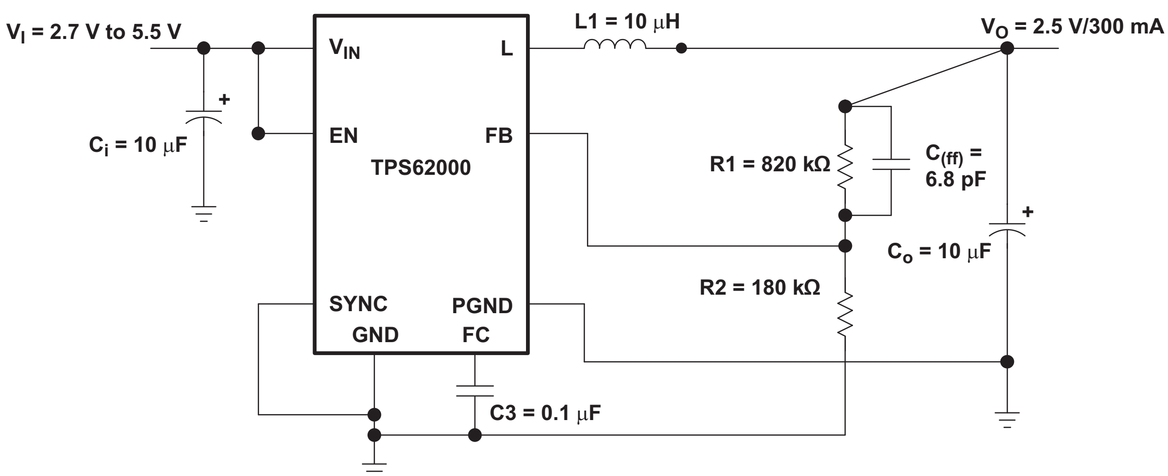


Figure 15. Typical Application Circuit for Adjustable Output Voltage Option

INDUCTOR SELECTION

A 10-µH minimum output inductor is used with the TPS62000. Values larger than 22 µH or smaller than 10 µH may cause stability problems because of the internal compensation of the regulator.

For output voltages greater than 1.8 V, a 22-µH inductance might be used in order to improve the efficiency of the converter.

After choosing the inductor value of typically 10 µH, two additional inductor parameters should be considered: first the current rating of the inductor and second the dc resistance.

The dc resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency.

In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus the inductor ripple current which is calculated as:

(1) Application information is provided for commercial temperature as a reference and not for high temperature.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_{L(max)} = I_{O(max)} + \frac{\Delta I_L}{2} \tag{4}$$

Where:

- f = Switching frequency (750 kHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_{L(max)}$ = Maximum inductor current

The highest inductor current occurs at maximum V_I.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS62000 which is 1.6 A with ILIM = V_{IN} and 900 mA with ILIM = GND. See Table 1 for recommended inductors.

Table 1. Tested Inductors(1)

OUTPUT CURRENT	INDUCTOR VALUE	COMPONENT SUPPLIER	COMMENTS
0 mA to 600 mA	10 µH	Coilcraft DO3316P-103 Coilcraft DT3316P-103 Sumida CDR63B-100 Sumida CDRH5D28-100	High efficiency
		Coilcraft DO1608C-103 Sumida CDRH4D28-100	Smallest solution
0 mA to 300 mA	10 µH	Coilcraft DO1608C-103	High efficiency
		Murata LQH4C100K04	Smallest solution

(1) Parts are valid for –40°C to 85°C.

OUTPUT CAPACITOR SELECTION

For best performance, a low ESR output capacitor is needed. At output voltages greater than 1.8 V, ceramic output capacitors can be used to show the best performance. Output voltages below 1.8 V require a larger output capacitor and ESR value to improve the performance and stability of the converter.

Table 2. Capacitor Selection

OUTPUT VOLTAGE RANGE	OUTPUT CAPACITOR	OUTPUT CAPACITOR ESR
1.8 V ≤ V_I ≤ 5.5 V	C_o ≥ 10 µF	ESR ≤ 120 mΩ
0.8 V ≤ V_I < 1.8 V	C_o ≥ 47 µF	ESR > 50 mΩ

See Table 3 for recommended capacitors.

If an output capacitor is selected with an ESR value ≤ 120 mΩ, its RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated as:

$$I_{RMS(C_O)} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{5}$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charge and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR\right) \tag{6}$$

Where the highest output voltage ripple occurs at the highest input voltage V_I.

Table 3. Tested Capacitors[(1)]

CAPACITOR VALUE	ESR/mΩ	COMPONENT SUPPLIER	COMMENTS
10 µF	50	Taiyo Yuden JMK316BJ106KL	Ceramic
47 µF	100	Sanyo 6TPA47M	POSCAP
68 µF	100	Sprague 594D686X0010C2T	Tantalum

(1) Parts are valid for –40°C to 85°C.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes.

The input capacitor should have a minimum value of 10 µF and can be increased without any limit for better input voltage filtering.

The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = I_{O(max)} \times \sqrt{\frac{V_O}{V_I} \times \left(1 - \frac{V_O}{V_I}\right)} \tag{7}$$

The worst case RMS ripple current occurs at D = 0.5 and is calculated as: $I_{RMS} = \frac{I_O}{2}$

Ceramic capacitor show a good performance because of their low ESR value, and they are less sensitive against voltage transients compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the IC for best performance.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems.

Therefore, use wide and short traces for the main current paths as indicted in bold in Figure 16. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Place the bypass capacitor, C3, as close as possible to the FC pin. The analog ground, GND, and the power ground, PGND, need to be separated. Use a common ground node as shown in Figure 16 to minimize the effects of ground noise.

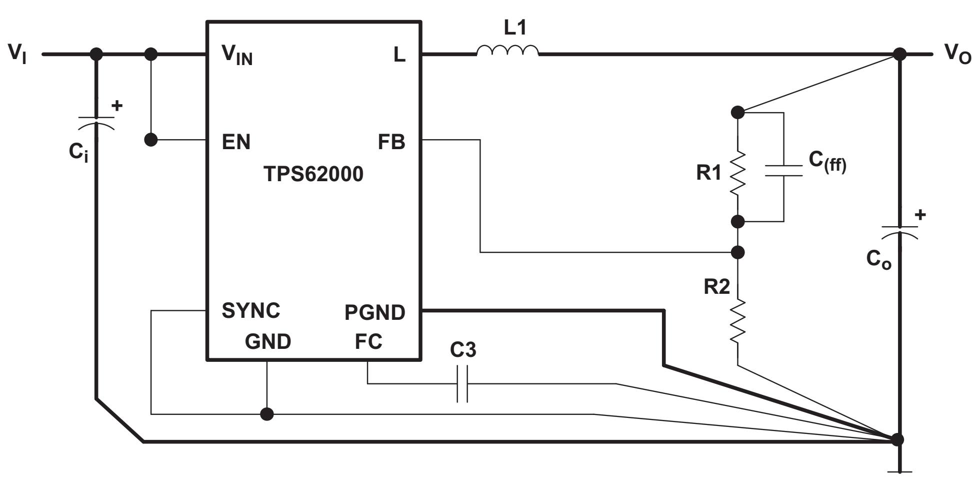
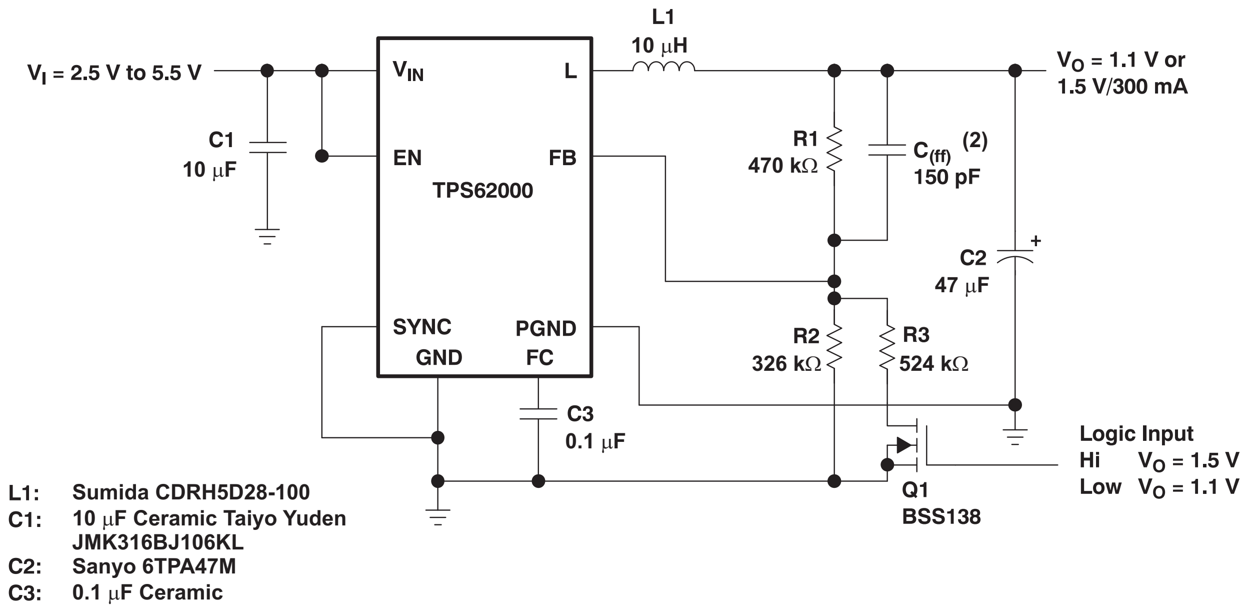


Figure 16. Layout Diagram

TYPICAL APPLICATION



(1) Use a small R-C filter to filter wrong reset signals during output voltage transitions.

(2) A large value is used for C(ff) to compensate for the parasitic capacitance introduced into the regulation loop by Q1.

Figure 17. Dynamic Output Voltage Programming As Used in Low Power DSP Applications

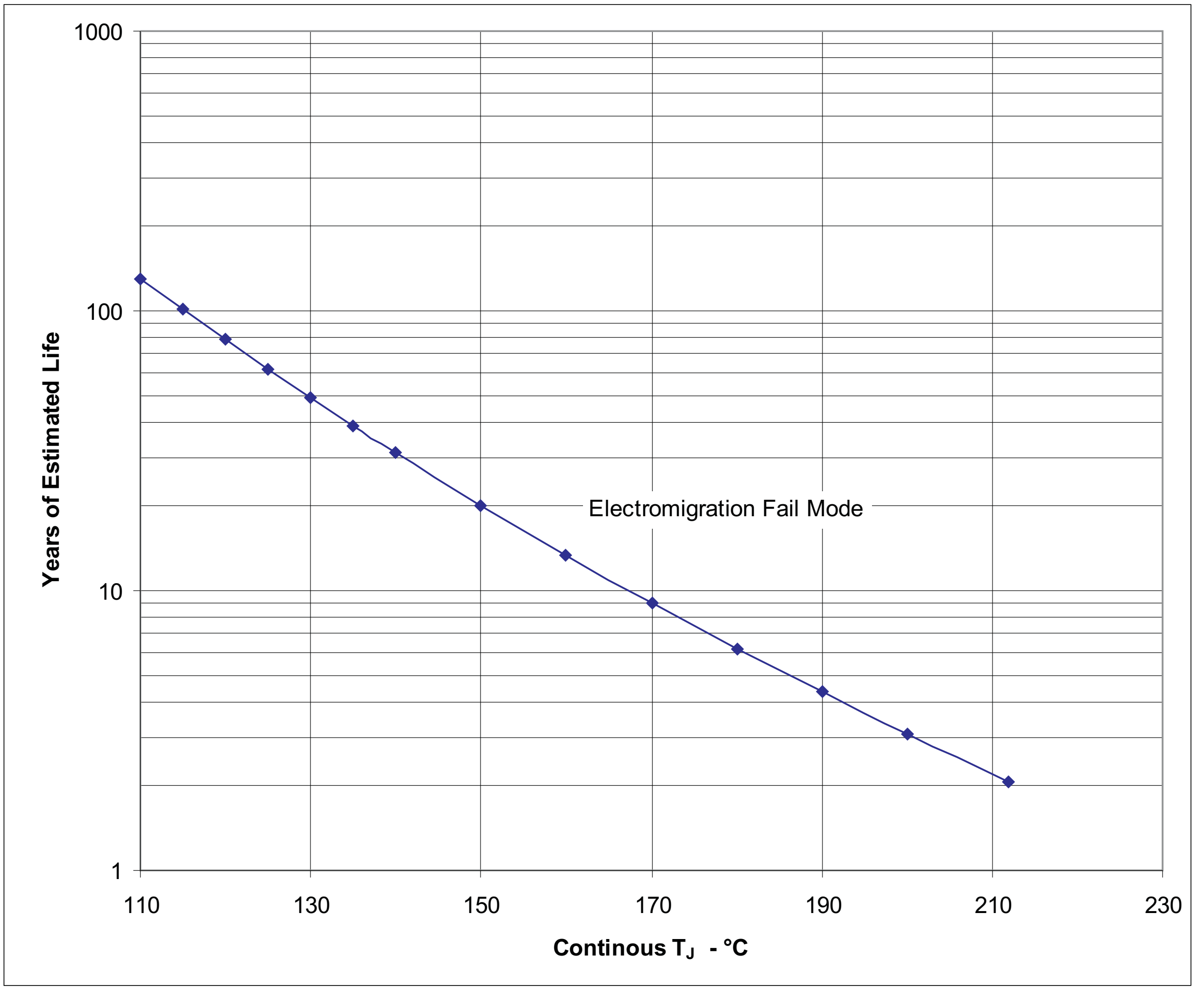


Figure 18. TPS62000SKGD1 Operating Life Derating Chart

Notes:

1. See data sheet for absolute maximum and minimum recommended operating conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62000SHKK	Active	Production	CFP (HKK) | 10	25 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 210	TPS62000S HKK
TPS62000SHKK.A	Active	Production	CFP (HKK) | 10	25 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 210	TPS62000S HKK
TPS62000SKGD1	Active	Production	XCEPT (KGD) | 0	100 | NOT REQUIRED	Yes	Call TI	N/A for Pkg Type	-55 to 210	
TPS62000SKGD1.A	Active	Production	XCEPT (KGD) | 0	100 | NOT REQUIRED	Yes	Call TI	N/A for Pkg Type	-55 to 210	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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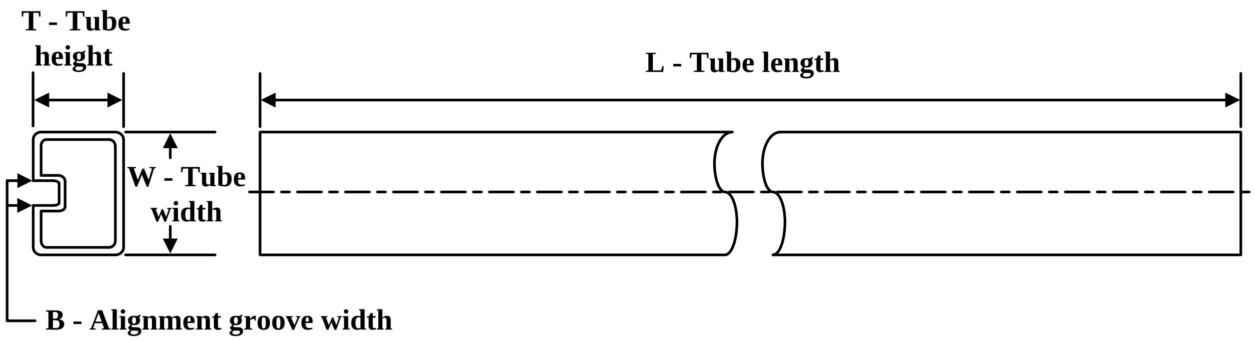
OTHER QUALIFIED VERSIONS OF TPS62000-HT :

- Catalog : TPS62000

NOTE: Qualified Version Definitions:

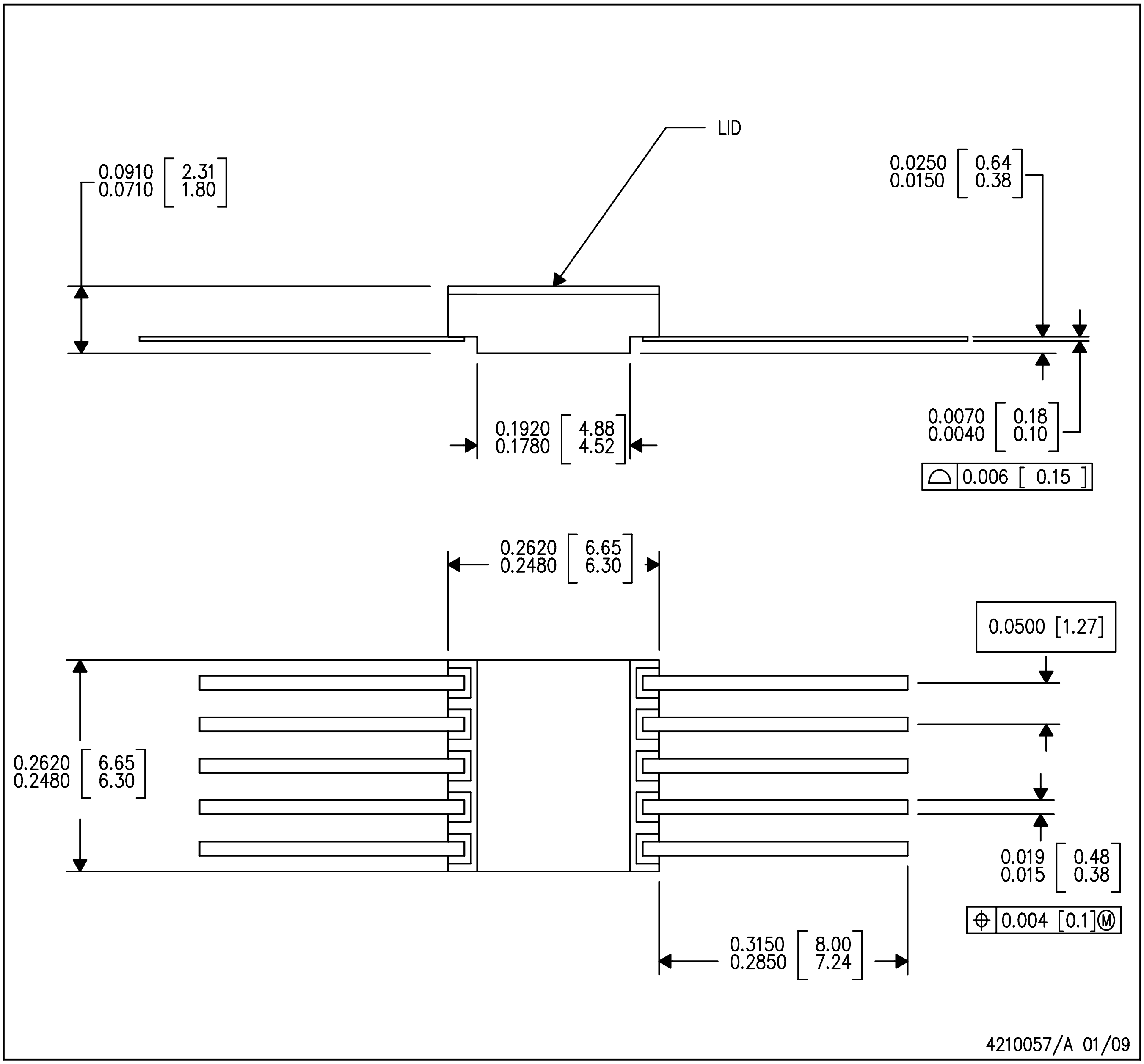
- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS62000SHKK	HKK	CFP	10	25	506.98	26.16	6220	NA
TPS62000SHKK.A	HKK	CFP	10	25	506.98	26.16	6220	NA



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This drawing does not comply with Mil Std 1835. Do not use this package for compliant product.
- D. The terminals will be gold plated.

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