TPS61256xC 3.5-MHz High Efficiency Step-Up Converter In Chip Scale Packaging

1 Features

- 93% Efficiency at 3.5-MHz Operation
- 37-µA Quiescent Current in Normal Operation
- Wide V_{IN} Range From 2.3 V to 5.5 V
- Support $V_{IN} \geq V_{OUT}$ Operation
- ±2% Total DC Voltage Accuracy
- Light-Load PFM Mode
- Pass-through Mode by Pulling EN Low
- Thermal Shutdown and Overload Protection
- Only Three Surface-Mount External Components Required
- Total Solution Size < 25 mm^2
- 9-Pin NanoFree™ (CSP) Packaging

2 Applications

- NFC PA Supply
- Cell Phones, Smart Phones
- Mono and Stereo APA Applications
- USB Charging Ports

3 Description

The TPS61256xC device provides a power supply solution for battery-powered portable applications. Intended for low-power applications, the TPS61256xC supports up to 800-mA load current from a battery discharged as low as 2.65 V and allows the use of low cost chip inductor and capacitors.

With a wide input voltage range of 2.3 V to 5.5 V, the device supports applications powered by Li-Ion batteries with extended voltage range. Different fixed voltage output versions are available from 3.15 V to 5.0 V.

The TPS61256xC operates at a regulated 3.5-MHz switching frequency and enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range. The PFM mode extends the battery life by reducing the quiescent current to 37 µA (typ) during light load operation.

In addition, the TPS61256xC device can also support the pass-through mode by pulling EN to low. In this mode, the output voltage follows the input voltage with a voltage drop by the resistance of the inductor and high-side FET.

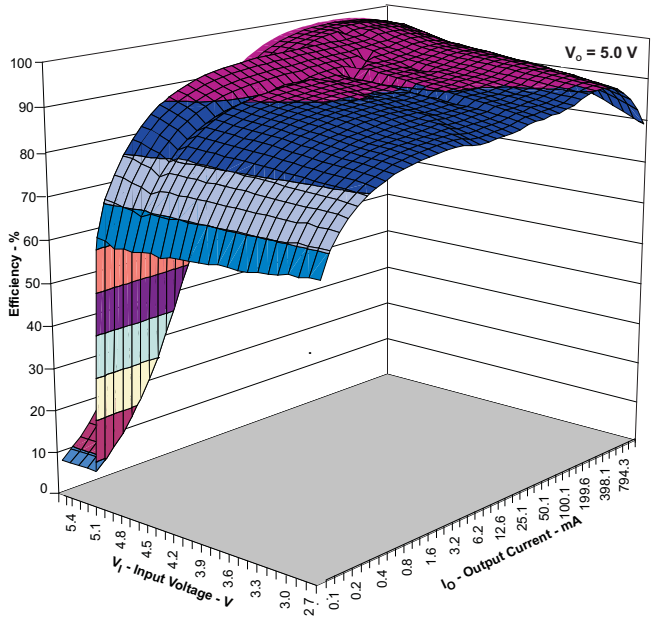
The TPS61256xC offers a very small solution size due to minimum amount of external components. It allows the use of small inductors and input capacitors to achieve a small solution size.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61256xC	DSBGA (9)	1.206 mm × 1.306 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Efficiency vs Load Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2017) to Revision A	Page
• Added device numbers TPS612562C and TPS612564C	3

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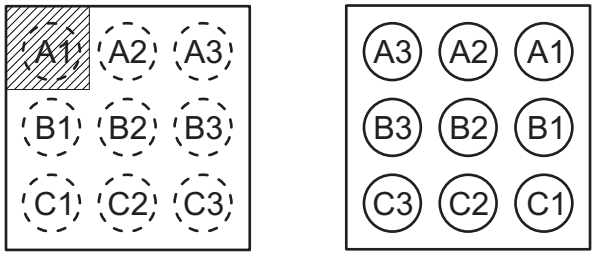
5 Device Options

T_A	PART NUMBER(1)	OUTPUT VOLTAGE	DEVICE SPECIFIC FEATURES
–40°C to 85°C	TPS61256C	5.0 V	Supports 5 V / 900 mA loading down to 3.3 V input voltage
–40°C to 85°C	TPS612562C	5.2 V	Supports 5.2 V / 900 mA loading down to 3.3 V input voltage
–40°C to 85°C	TPS612564C	5.4 V	Supports 5.4 V / 900 mA loading down to 3.3 V input voltage

(1) For all available packages, see the orderable addendum at the end of the datasheet.

6 Pin Configuration and Functions

YFF Package
9-Bump DSBGA
Top and Bottom Views



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	B3	I	EN = high, the device works in the boost mode. EN = low, the device is in pass-through mode. This pin must not be left floating and must be terminated.
GND	C1, C2, C3		Ground pin.
SW	B1, B2	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
VIN	A3	I	Power supply input.
VOUT	A1, A2	O	Boost converter output.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	Voltage at VIN(2), VOUT(2), SW(2), EN(2)	–0.3	7	V
Input current	Continuous average current into SW (3)		1.8	A
	Peak current into SW (4)		3.5	
Power dissipation		Internally limited		
Temperature	Operating, T_A (5)	–40	85	°C
	Operating virtual junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Limit the junction temperature to 105°C for continuous operation at maximum output power.
(4) Limit the junction temperature to 125°C for 5% duty cycle operation.
(5) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_I	Input voltage range	TPS61256xC	2.5		4.85	V
R_L	Minimum resistive load for start-up	TPS61256xC	10			Ω
L	Inductance		0.7	1.0	2.9	µH
C_O	Output capacitance		3.5	5	50	µF
T_A	Ambient temperature		–40		85	°C
T_J	Operating junction temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61256xC YFF 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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7.5 Electrical Characteristics

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, EN = 1.8V, T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, EN = 1.8V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Operating quiescent current into V_{IN} Operating quiescent current into V_{OUT} pass-through mode quiescent current into V_{IN} pass-through mode quiescent current into V_{OUT}	I_{OUT} = 0 mA, V_{IN} = 3.6 V EN = V_{IN} Device not switching		30	45	µA
				7	15	µA
		I_{OUT} = 0 mA, V_{IN} = V_{OUT} = 3.6 V EN = GND, Device not switching		11	20	µA
				9.5	15	µA
V_{UVLO}	Under-voltage lockout threshold	Falling		2.0	2.1	V
		Hysteresis		0.1		V
ENABLE						
V_{IL_EN}	Low-level input voltage				0.4	V
V_{IH_EN}	High-level input voltage		1.0			V
I_{lkg_EN}	Input leakage current	Input connected to GND or V_{IN}			0.5	µA
OUTPUT						
V_{OUT}	Regulated DC output voltage-TPS61256C	2.3 V ≤ V_{IN} ≤ 4.85 V, I_{OUT} = 0 mA PWM operation. Open Loop	4.92	5	5.08	V
V_{OUT}	Regulated DC output voltage-TPS612562C	2.3 V ≤ V_{IN} ≤ 4.85 V, I_{OUT} = 0 mA PWM operation. Open Loop	5.12	5.2	5.28	V
V_{OUT}	Regulated DC output voltage-TPS612564C	2.3 V ≤ V_{IN} ≤ 4.85 V, I_{OUT} = 0 mA PWM operation. Open Loop	5.31	5.4	5.49	V
ΔV_{OUT}	Power-save mode output ripple voltage	PFM operation, I_{OUT} = 1 mA		50		mVpk
POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET on resistance			170		mΩ
	Low-side MOSFET on resistance			100		
I_{LIM}	Switch valley current limit	EN = V_{IN}, Open Loop	1900	2150	2400	mA
	Pre-charge / pass-through mode current limit (linear mode)	TPS61256xC	500			
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C
OSCILLATOR						
f_{OSC}	Oscillator frequency	V_{IN} = 3.6 V, V_{OUT} = 4.5 V		3.5		MHz
TIMING						
	Start-up time	I_{OUT} = 0 mA. Time from active EN to start switching		70		µs
		I_{OUT} = 0 mA. Time from active EN to V_{OUT}		400		µs

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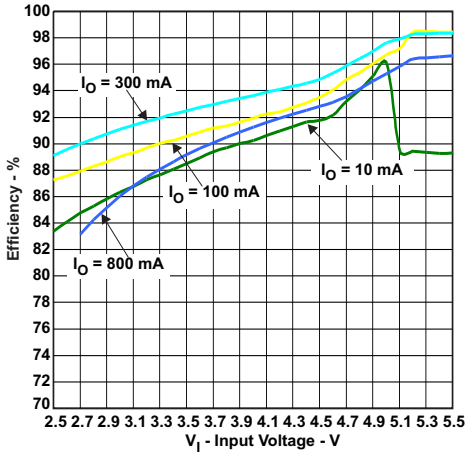
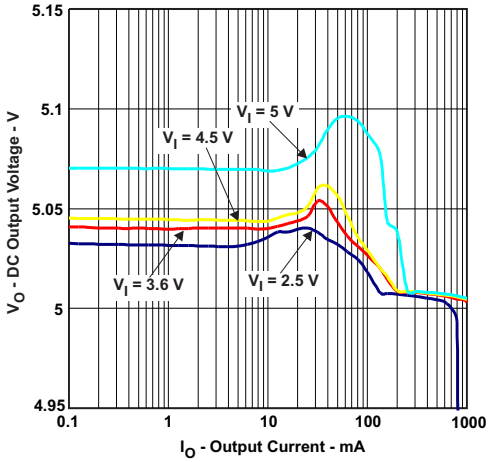
7.6 Typical Characteristics



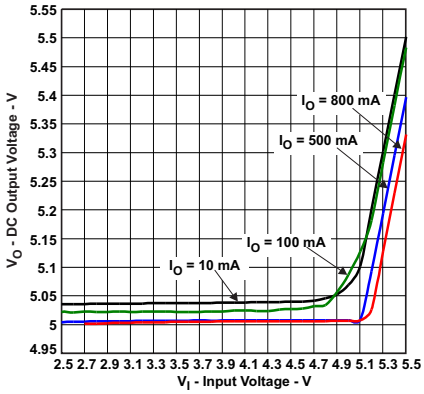
V_O = 5 V PFM/PWM Operation

Figure 1. Efficiency vs Input Voltage



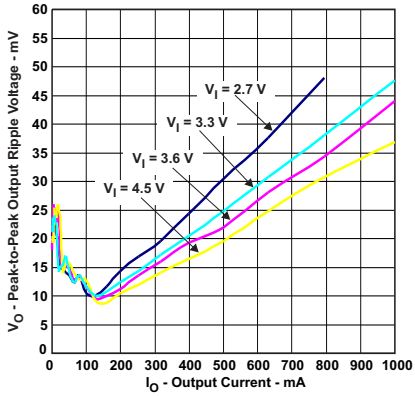
V_O = 5 V PFM/PWM Operation

Figure 2. DC Output Voltage vs Output Current



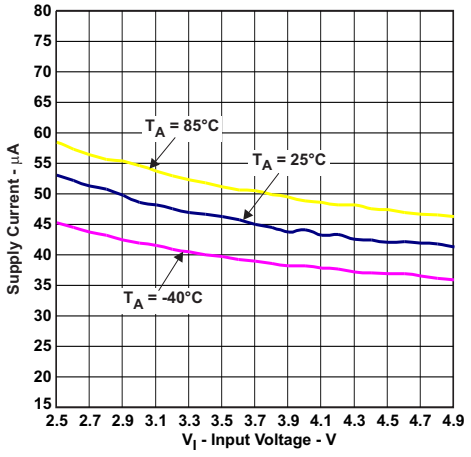
V_O = 5 V PFM/PWM Operation

Figure 3. DC Output Voltage vs Input Voltage



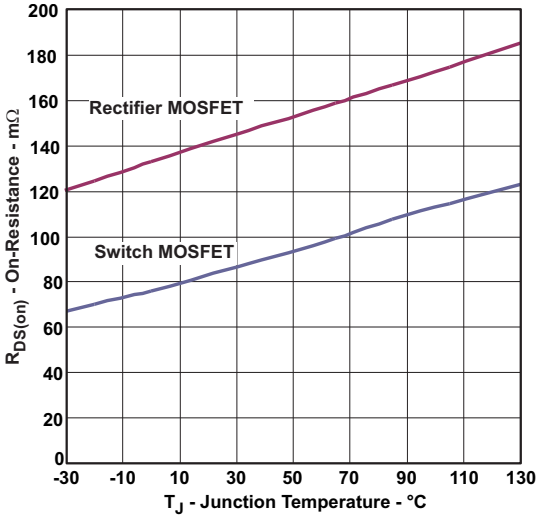
V_O = 5 V PFM/PWM Operation
C_O = 22 µF 10 V (1210) X5R, muRata GRM32ER71A226K

Figure 4. Peak-to-Peak Output Ripple Voltage vs Output Current



EN = High No Switching

Figure 5. Supply Current vs Input Voltage



V_O = 5 V

Figure 6. MOSFET $r_{DS(on)}$ vs Temperature

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8 Parameter Measurement Information

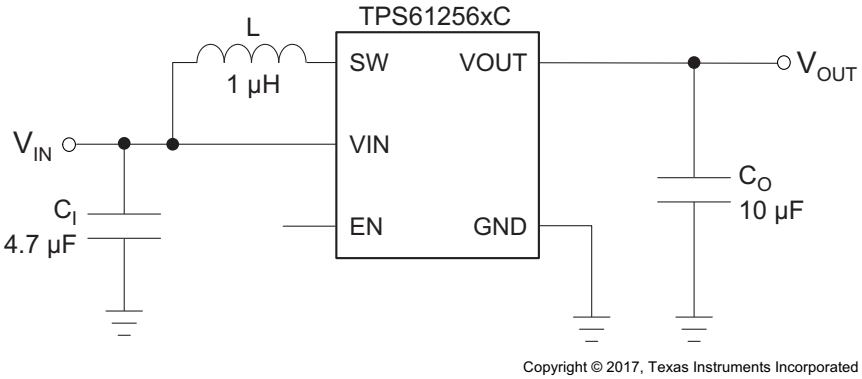

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Figure 7. Parameter Measurement Schematic

9 Detailed Description

9.1 Overview

The TPS61256xC synchronous step-up converter typically operates at a quasi-constant 3.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS61256xC converter operates in power-save mode with pulse frequency modulation (PFM).

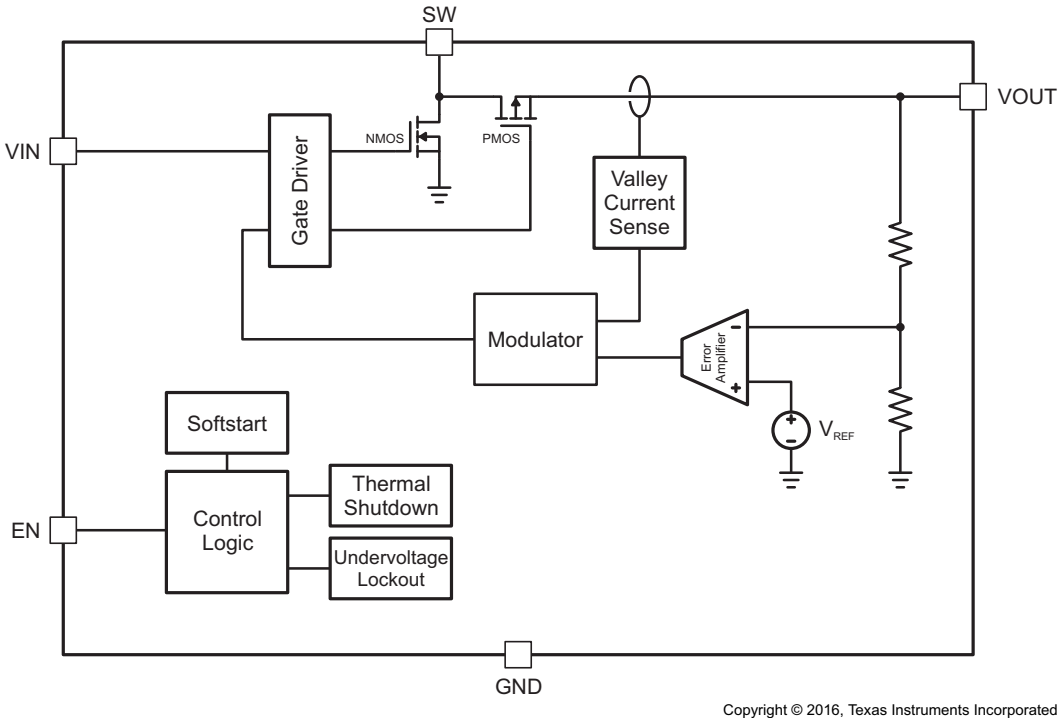
During PWM operation, the converter uses a novel quasi-constant on-time valley current mode control scheme to achieve excellent line/load regulation and allows the use of a small ceramic inductor and capacitors. Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time.

At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier is turned-on and the inductor current decays to a preset valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

In general, a dc/dc step-up converter can only operate in "true" boost mode, i.e. the output “boosted” by a certain amount above the input voltage. The TPS61256xC device operates differently as it can smoothly transition in and out of zero duty cycle operation. Therefore the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive. In this operation mode, the output current capability of the regulator is limited to 500 mA (min.). Refer to Figure 3 for further details.

The current mode architecture with adaptive slope compensation provides excellent transient load response, requiring minimal output filtering. Internal soft-start and loop compensation simplifies the design process while minimizing the number of external components.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Current Limit Operation

The TPS61256xC device employs a valley current limit sensing scheme. Current limit detection occurs during the off-time by sensing of the voltage drop across the synchronous rectifier.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit (CL) operation, can be defined by Equation 1.

$$I_{OUT(CL)} = (1 - D) \cdot \left(I_{VALLEY} + \frac{1}{2} \Delta I_L\right) \quad (1)$$

The duty cycle (D) can be estimated by Equation 2

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \quad (2)$$

and the peak-to-peak current ripple (ΔI_L) is calculated by Equation 3

$$\Delta I_L = \frac{V_{IN}}{L} \cdot \frac{D}{f} \quad (3)$$

The output current, $I_{OUT(DC)}$, is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off-time is increased to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism). When the current limit is reached the output voltage decreases during further load increase.

Figure 8 illustrates the inductor and rectifier current waveforms during current limit operation.

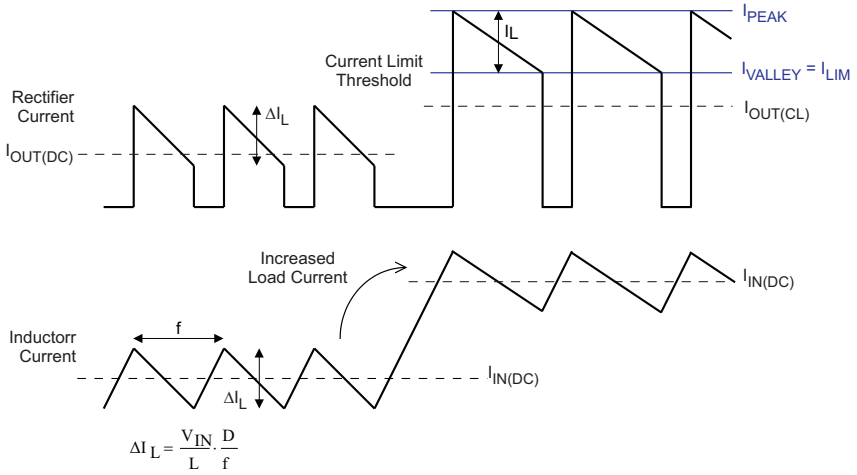

Figure 8. Inductor/Rectifier Currents in Current Limit Operation

9.3.2 Enable

The TPS61256xC device starts operation when EN is set high and starts up with the soft-start sequence. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN low and Vin above UVLO, the device is in the forced pass-through mode and the output voltage follows the input voltage (with a voltage drop of the inductor DCR and Rdson of HS FET).

9.3.3 Softstart

The TPS61256xC device has an internal softstart circuit that limits the inrush current during start-up. The first step in the start-up cycle is the pre-charge phase. During pre-charge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch is current limited (500 mA min.) during this phase. This mechanism is used to limit the output current under short-circuit condition.

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Feature Description (continued)

Once the output capacitor has been biased to the input voltage, the converter starts switching. The soft-start system progressively increases the on-time as a function of the input-to-output voltage ratio. As soon as the output voltage is reached, the regulation loop takes control and full current operation is permitted.

The TPS61256xC works in the pass-through mode when EN is low and Vin above UVLO, the device enters into the boost switching phase directly when EN becomes high.

9.3.4 Undervoltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling V_{IN} trips the under-voltage lockout threshold V_{UVLO} which is typically 2.0V. The device starts operation once the rising V_{IN} trips V_{UVLO} threshold plus its hysteresis of 100 mV at typically 2.1 V.

9.3.5 Thermal Regulation

The TPS61256xC device contains a thermal regulation loop that monitors the die temperature during the pre-charge phase. If the die temperature rises to high values of about 110 °C, the device automatically reduces the current to prevent the die temperature from increasing further. Once the die temperature drops about 10 °C below the threshold, the device automatically increases the current to the target value. This function also reduces the current during a short-circuit condition.

9.3.6 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typ.) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned-off. When the junction temperature falls below the thermal shutdown minus its hysteresis, the device continuous the operation.

9.4 Device Functional Modes

9.4.1 Power Save Mode

The TPS61256xC integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage.

The TPS61256xC ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage.

The PFM mode is exited and PWM mode entered when the output current can no longer be supported in PFM mode.

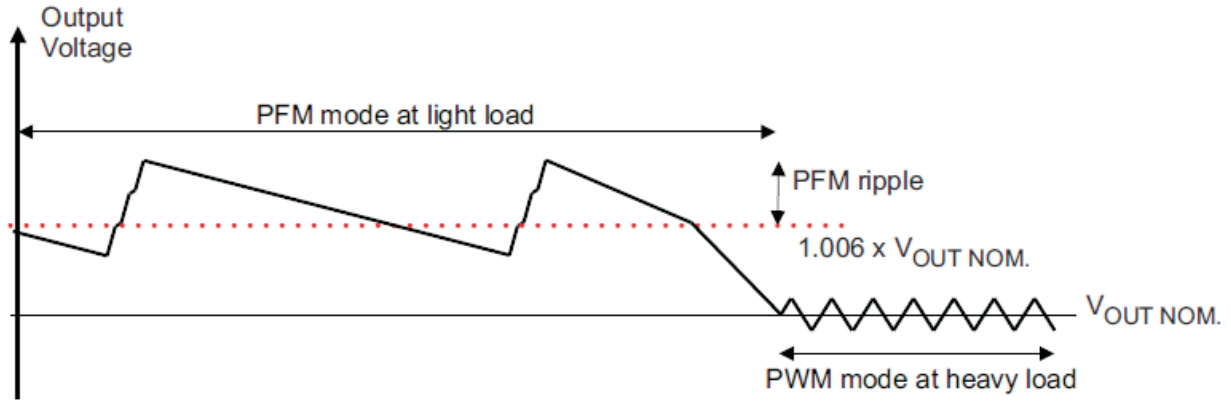

Figure 9. Power Save

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Device Functional Modes (continued)

9.4.2 Pass-Through Mode

When EN is pulled to low and Vin above UVLO, the device works in the pass-through mode and the output voltage of TPS61256xC follows the input voltage level. In so called pass-through mode, the synchronous rectifier is current limited to 500 mA (min.). The output voltage is slightly reduced due to voltage drop across the rectifier MOSFET and the inductor DC resistance.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

With a wide input voltage range of 2.3 V to 5.5 V, the TPS61256xC supports applications powered by Li-Ion batteries with extended voltage range. Intended for low-power applications, it supports up to 800-mA load current from a battery discharged as low as 2.65 V and allows the use of low cost chip inductor and capacitors. Different fixed voltage output versions are available from 3.15 V to 5.0 V. The TPS61256xC offers a very small solution size due to minimum amount of external components. The TPS6125xC allows the use of small inductors and input capacitors to achieve a small solution size. During the pass-through mode, the output voltage is biased to the input voltage.

10.2 Typical Application

This section details an application with TPS61256xC to output fixed 5.0 V.

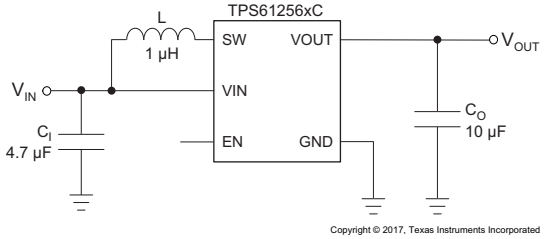

Figure 10. Smallest Solution Size Application

10.2.1 Design Requirements

In this example, TPS61256xC is used to design a 5-V power supply with up to 800-mA output current capability. The TPS61256xC can be powered by one-cell Li-ion battery, and in this example the input voltage range is from 2.65 V to 4.85 V.

10.2.2 Detailed Design Procedure

Table 1. List of Components

REFERENCE	DESCRIPTION	PART NUMBER, MANUFACTURER(1)
L(2)	1.0 µH, 1.8 A, 48 mΩ, 3.2 x 2.5 x 1.0mm max. height	LQM32PN1R0MG0, muRata
C_I	4.7 µF, 6.3 V, 0402, X5R ceramic	GRM155R60J475M, muRata
C_O	10 µF, 6.3 V, 0603, X5R ceramic	GRM188R60J106ME84, muRata

(1) See *Third-Party Products Discalimer*
(2) Inductor used to characterize TPS61256xCYFF device.

10.2.2.1 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion, an inductor and an output capacitor. TI advises selecting an inductor with a saturation current rating higher than the possible peak current flowing through the power switches.

The inductor peak current varies as a function of the load, the input and output voltages and can be estimated using Equation 4.

$$I_{L(PEAK)} = \frac{V_{IN} \cdot D}{2 \cdot f \cdot L} + \frac{I_{OUT}}{(1-D) \cdot \eta} \quad \text{with} \quad D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \tag{4}$$

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Selecting an inductor with insufficient saturation performance can lead to excessive peak current in the converter. This could eventually harm the device and reduce its reliability.

When selecting the inductor, as well as the inductance, parameters of importance are: maximum current rating, series resistance, and operating temperature. The inductor DC current rating should be greater (by some margin) than the maximum input average current, refer to Equation 5 and *Current Limit Operation* section for more details.

$$I_{L(DC)} = \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{\eta} \cdot I_{OUT} \quad (5)$$

The TPS61256xC series of step-up converters have been optimized to operate with a effective inductance in the range of 0.7 µH to 2.9 µH and with output capacitors in the range of 10 µF to 47 µF. The internal compensation is optimized for an output filter of L = 1 µH and C_O = 10 µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operating conditions. For more details, see the *Checking Loop Stability* section.

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS61256xC converters.

Table 2. List of Inductors

MANUFACTURER(1)	SERIES	DIMENSIONS (in mm)
HITACHI METALS	KSLI-322512BL1-1R0	3.2 x 2.5 x 1.2 max. height
MURATA	LQM32PN1R0MG0	3.2 x 2.5 x 1.0 max. height
	LQM2HPN1R0MG0	2.5 x 2.0 x 1.0 max. height
	LQM21PN1R5MC0	2.0 x 1.2 x 0.55 max height
TOKO	DFE322512C-1R0	3.2 x 2.5 x 1.2 max. height
	MDT2012-CLR1R0AM	2.0 x 1.2 x 0.58 max height

(1) See *Third-Party Products Disclaimer*

10.2.2.2 Output Capacitor

For the output capacitor, TI recommends using small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the V_{OUT} and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 6 can be used.

$$C_{MIN} = \frac{I_{OUT} \cdot (V_{OUT} - V_{IN})}{f \cdot \Delta V \cdot V_{OUT}} \quad (6)$$

Where f is the switching frequency which is 3.5 MHz (typ.) and ΔV is the maximum allowed output ripple.

With a chosen ripple voltage of 20mV, a minimum effective capacitance of 9 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 7

$$V_{ESR} = I_{OUT} \cdot R_{ESR} \quad (7)$$

An MLCC capacitor with twice the value of the calculated minimum should be used due to DC bias effects. This is required to maintain control loop stability. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients but the total output capacitance value should not exceed ca. 50µF.

DC bias effect: high cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the device's effective capacitance. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and it's effective capacitance. For instance, a 10-µF X5R 6.3-V 0603 MLCC capacitor would typically show an effective capacitance of less than 4 µF (under 5 V bias condition, high temperature).

In applications featuring high pulsed load currents, it is recommended to run the converter with a reasonable amount of effective output capacitance, for instance x2 10-µF X5R 6.3-V 0603 MLCC capacitors connected in parallel.

10.2.2.3 Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 4.7-µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_I and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_I.

10.2.2.4 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

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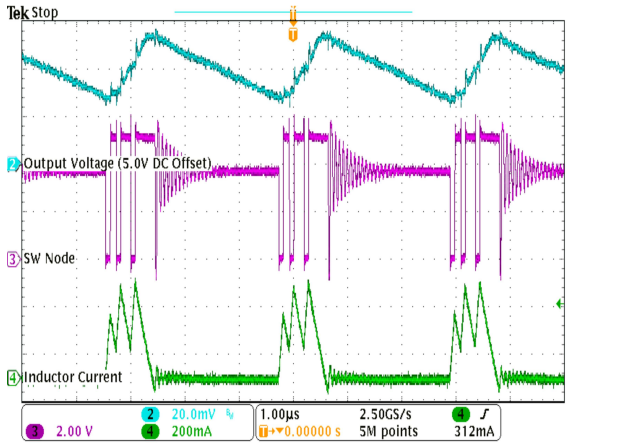
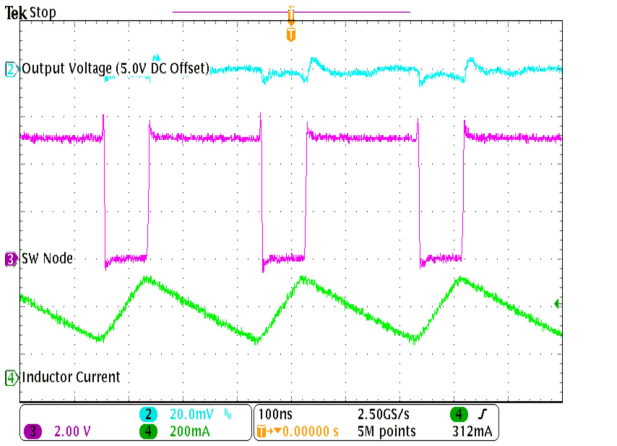
10.2.3 Application Curves

	FIGURE
PFM operation	Figure 11
PWM operation	Figure 12
Combined line/load transient response	Figure 13
Load transient response	Figure 14, Figure 16
AC load transient response	Figure 15, Figure 17
Start-up	Figure 18, Figure 19



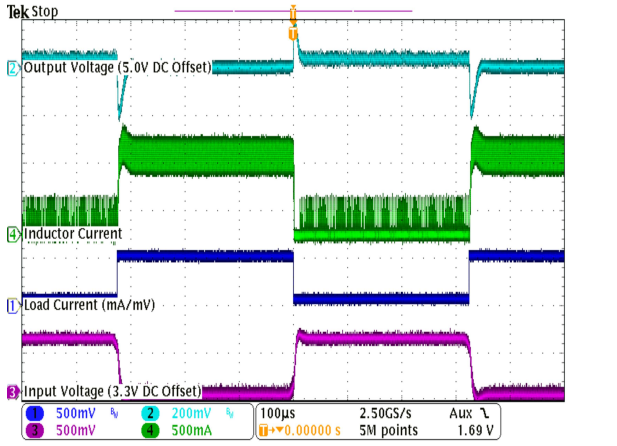
V_I = 3.6 V V_O = 5 V I_O = 40 mA

Figure 11. Power-Save Mode Operation



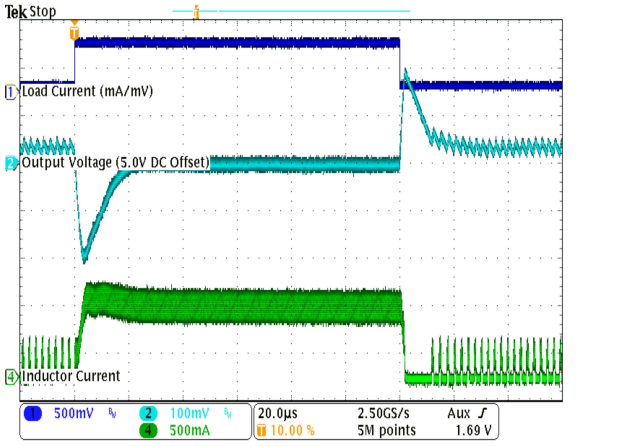
V_I = 3.6 V V_O = 5 V I_O = 200 mA

Figure 12. PWM Operation



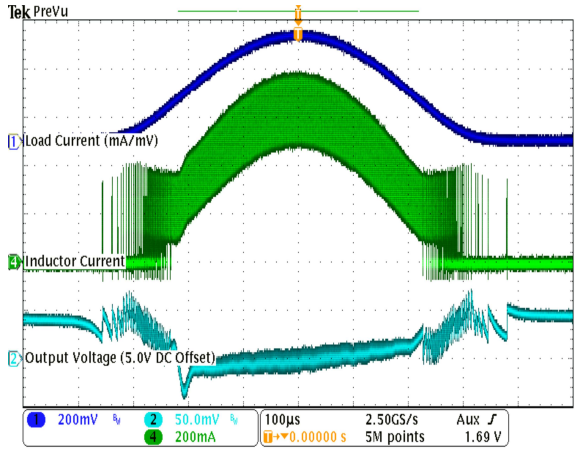
V_O = 5 V 50 to 500 mA Load Step 3.3 V to 3.9 V Line Step

Figure 13. Combined Line/Load Transient Response



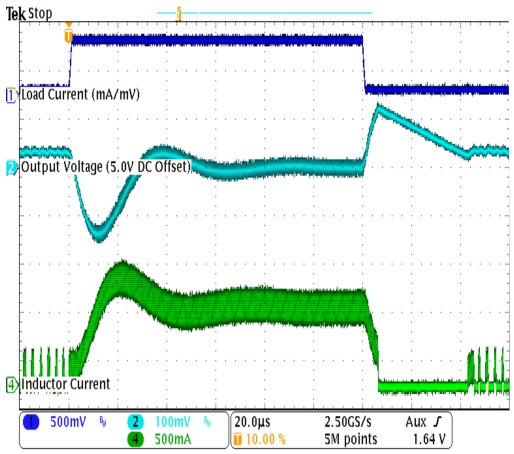
V_I = 3.6 V V_O = 5 V 50 to 500 mA Load Step
C_O = 10 µF 6.3 V (0603) X5R, muRata

Figure 14. Load Transient Response in PFM/PWM Operation



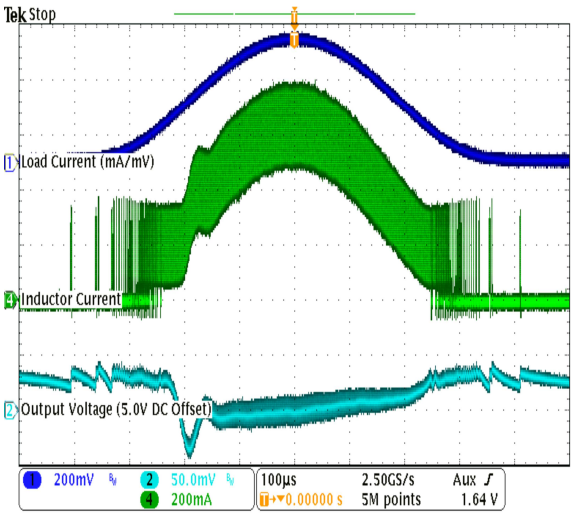
V_I = 3.6 V V_O = 5 V 0 to 400 mA Load
C_O = 10 µF 6.3 V (0603) X5R, muRata

Figure 15. AC Load Transient Response



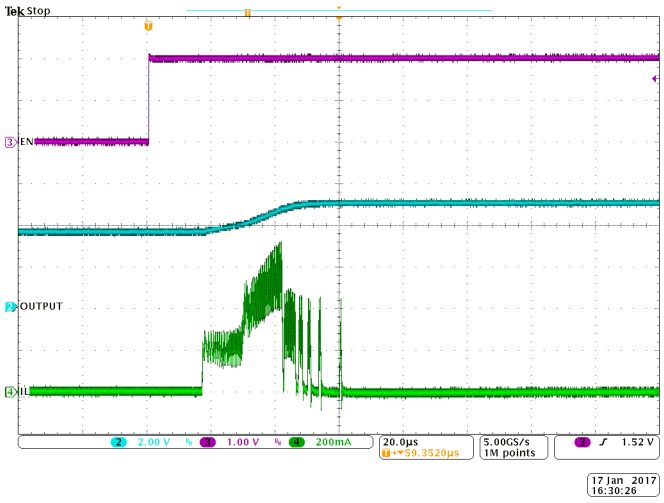
V_I = 3.6 V V_O = 5 V 50 to 500 mA Load Step
C_O = 22 µF 10 V (1210) X5R, muRata

Figure 16. Load Transient Response in PFM/PWM Operation



V_I = 3.6 V V_O = 5 V 0 to 400 mA Load
C_O = 22 µF 10 V (1210) X5R, muRata

Figure 17. AC Load Transient Response



V_I = 3.6 V V_O = 5 V I_O = 0 mA

Figure 18. Pass-through to Boost by EN toggling

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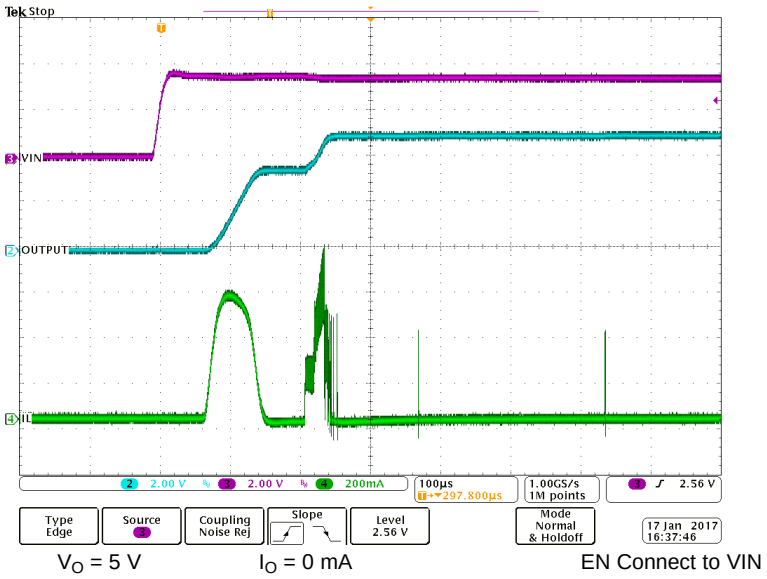

Figure 19. Start-Up by VIN

11 Power Supply Recommendations

The power supply can be three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. The input supply should be well regulated with the rating of TPS61256xC. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

12 Layout

12.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pins of the IC.

12.2 Layout Example

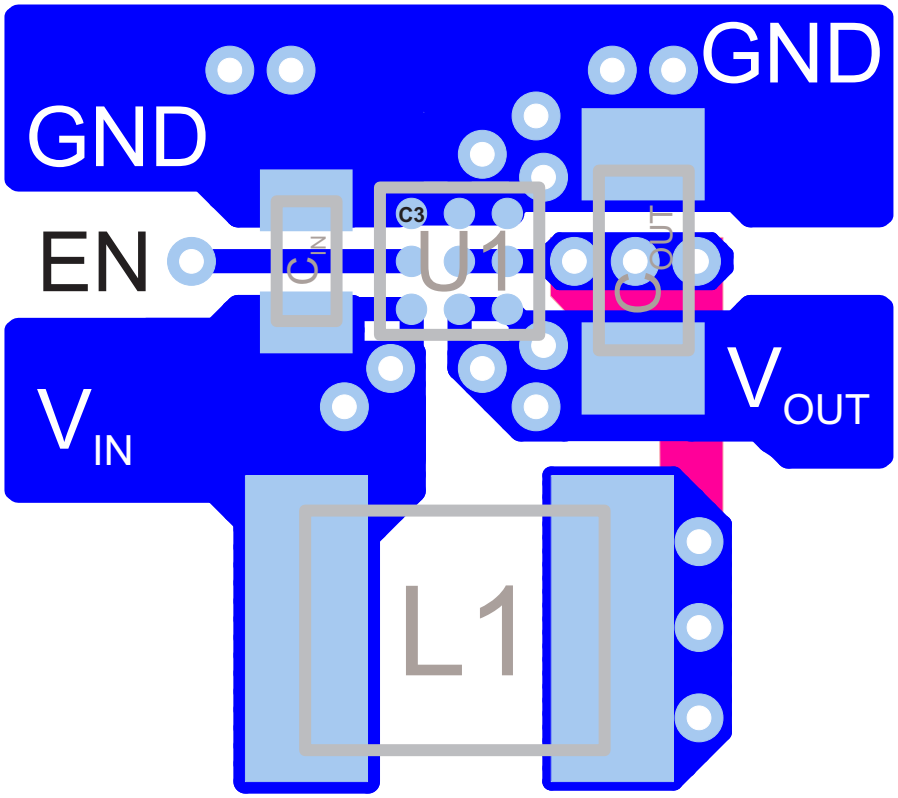

Figure 20. Suggested Layout (Top View)

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12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

As power demand in portable designs is more and more important, designers must figure the best trade-off between efficiency, power dissipation and solution size. Due to integration and miniaturization, junction temperature can increase significantly which could lead to bad application behaviors (i.e. premature thermal shutdown or worst case reduce device reliability).

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where the high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The device operating junction temperature (T_J) should be kept below 125°C.

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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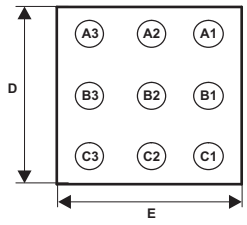
14 Mechanical, Packaging, and Orderable Information

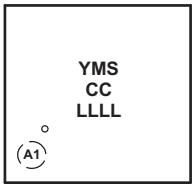
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 Package Summary

Chip Scale Package (Bottom View)



Chip Scale Package (Top View)



Code:

- YM - 2 digit date code
- S - assembly site code
- CC - chip code (see ordering table)
- LLLL - lot trace code

14.2 Package Option Addendum

14.2.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
TPS612562CYFFR	PREVIEW	DSBGA	YFF	9	3000	Green (RoHS and no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	–40 to 85	16H
TPS612562CYFFT	PREVIEW	DSBGA	YFF	9	250	Green (RoHS and no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	–40 to 85	16H
TPS612564CYFFR	PREVIEW	DSBGA	YFF	9	3000	Green (RoHS and no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	–40 to 85	16I
TPS612564CYFFT	PREVIEW	DSBGA	YFF	9	250	Green (RoHS and no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	–40 to 85	16I

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
TPS61256CYFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS and no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	–40 to 85	15U
TPS61256CYFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS and no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	–40 to 85	15U

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
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PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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(6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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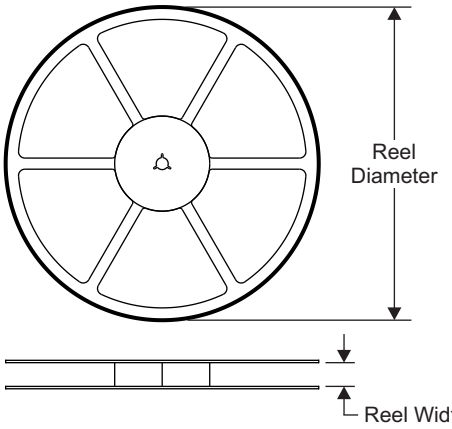
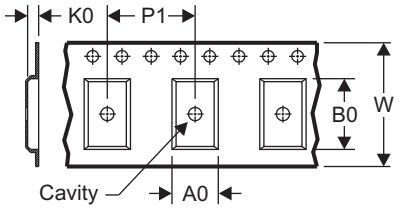
14.2.2 Tape and Reel Information

REEL DIMENSIONS

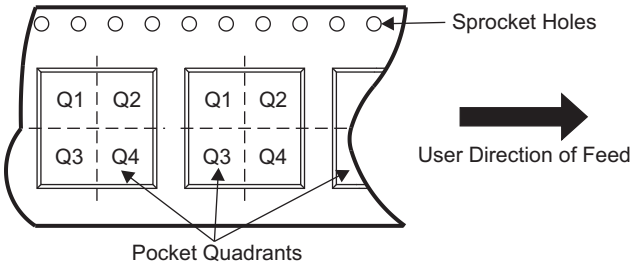


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS612562CYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS612562CYFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS612564CYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS612564CYFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61256CYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1
TPS61256CYFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	2.0	8.0	Q1

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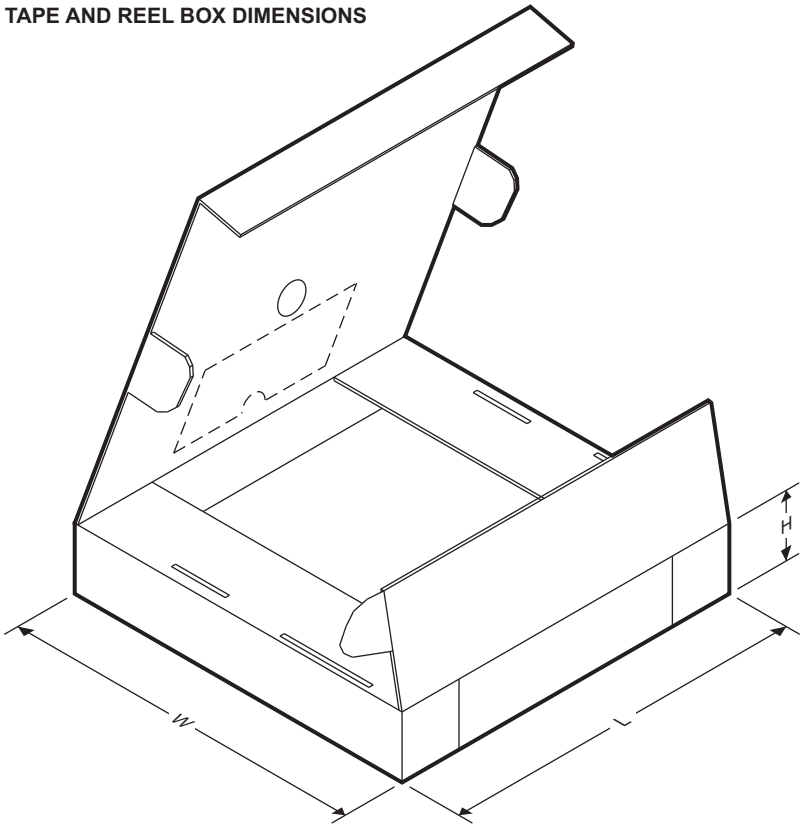
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS612562CYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS612562CYFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS612564CYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS612564CYFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS61256CYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61256CYFFT	DSBGA	YFF	9	250	182.0	182.0	20.0

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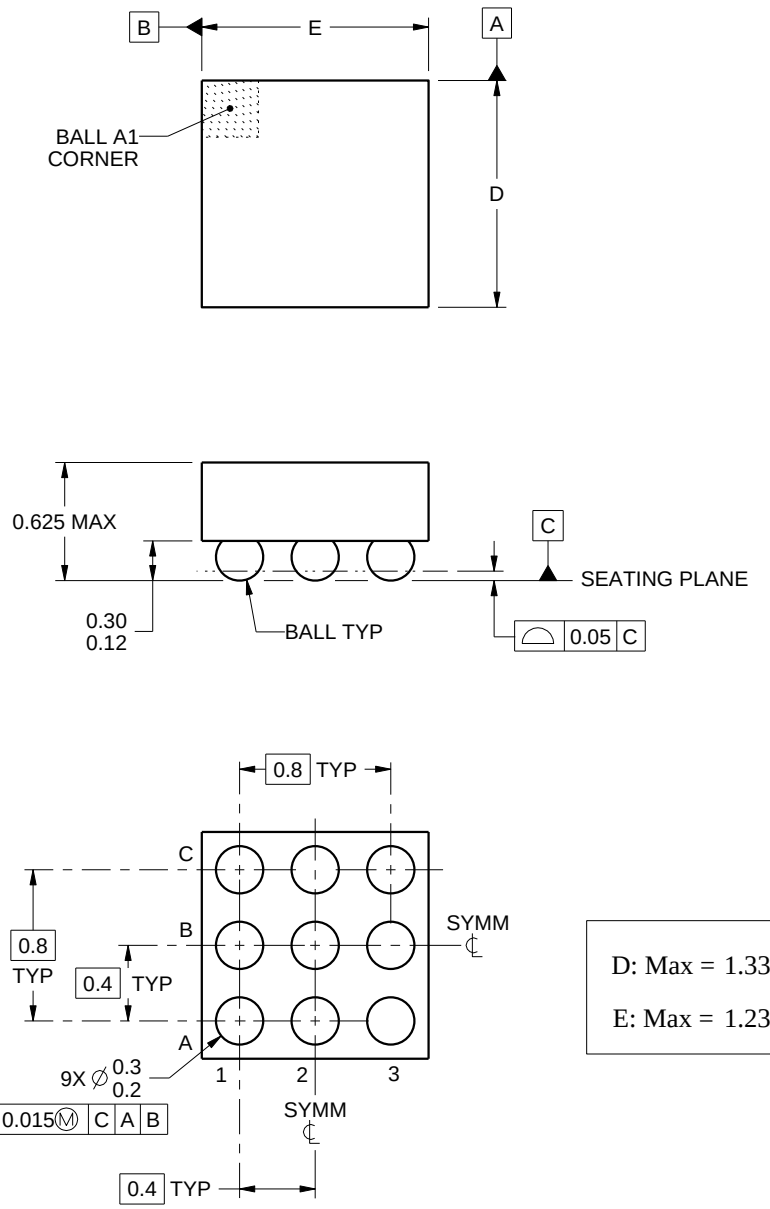
PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.336 mm, Min =1.276 mm

E: Max = 1.236 mm, Min =1.176 mm

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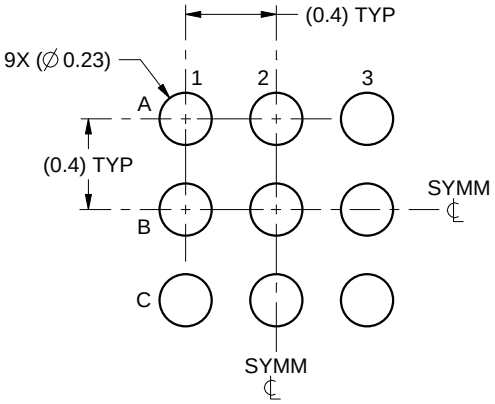
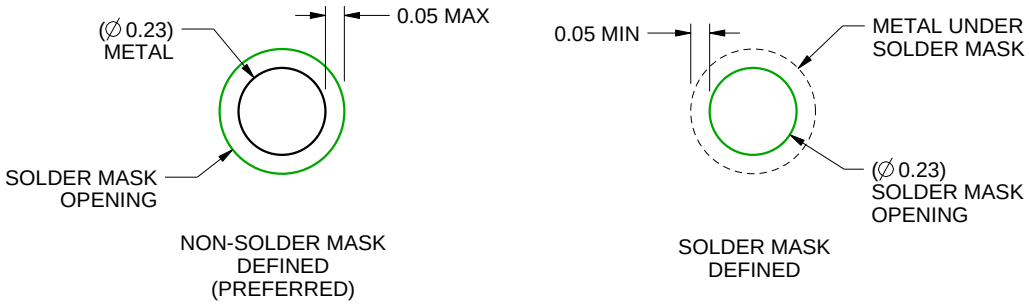
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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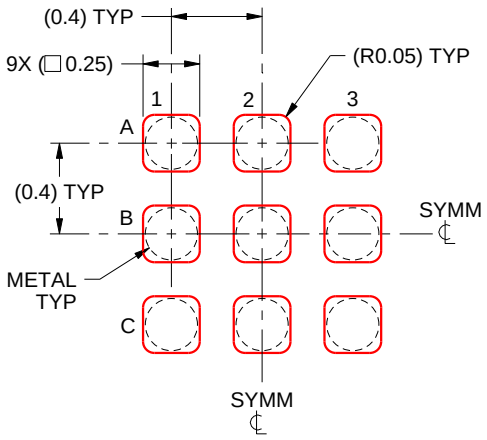
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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