TPS55285 22V, 8A Buck-Boost Converter with I²C Interface

1 Features

- Programmable power supply (PPS) support for USB power delivery (USB PD)
  - Wide input voltage range: 2.4V to 22V
  - 3.0V Minimum input voltage for start-up
  - Programmable output voltage range: 0.8V to 22V with 10mV step
  - ±1% reference voltage accuracy
  - Adjustable output voltage compensation for voltage drop over the cable
  - Programmable output current limit up to 6.35A with 50mA step
- High efficiency over entire load range
  - 92.0% efficiency at V_{IN} = 20V, V_{OUT} = 5V and I_{OUT} = 5A
  - 96.0% efficiency at V_{IN} = 12V, V_{OUT} = 20V and I_{OUT} = 3A
- I²C Programming
  - Output enable(OE) On/Off
  - Slew rate of output voltage change
  - Switching frequency: 400kHz, 800kHz, 1.6MHz, 2.2MHz
  - Programmable PFM and FPWM mode at light load
  - Spread spectrum enable/disable
  - Output discharge enable/disable
- Rich protection features
  - Input overvoltage protection
  - Output absolute overvoltage protection
  - Output relative overvoltage protection
  - Hiccup mode for output short-circuit protection
  - Thermal shutdown protection
  - 8A average inductor current limit
- Small solution size
  - Four low $R_{DS(ON)}$ internal MOSFETs
  - Maximum switching frequency up to 2.2MHz
  - 2.5mm × 3.5mm HotRod™ WQFN package

2 Applications

- USB PD
- Wireless charger
- Docking Station
- Notebook computer
- SSD

3 Description

The TPS55285 is a fully integrated synchronous buck-boost converter that is optimized for converting battery voltage, USB Power Delivery (USB PD) or adaptor voltage into power supply rails. The TPS55285 integrates four 15mΩ MOSFETs to provide a high efficiency and small size solution.

The TPS55285 has a wide input voltage range from 2.4V (3.0V rising) to 22V and is capable of outputting 0.8V to 22V voltage with 10mV step to support a variety of applications. It features 8A average inductor current limit and can supply up to 7A output current in buck mode. When working in boost mode, it can deliver 60W from 12V input or 30W from 5V input.

Through the I²C interface, the output voltage of the TPS55285 can be programmed dynamically. The default output voltage is 5V when the device is enabled. The I²C interface allows for configuration of slew rate of the output voltage change, switching frequency, forced PWM mode operation.

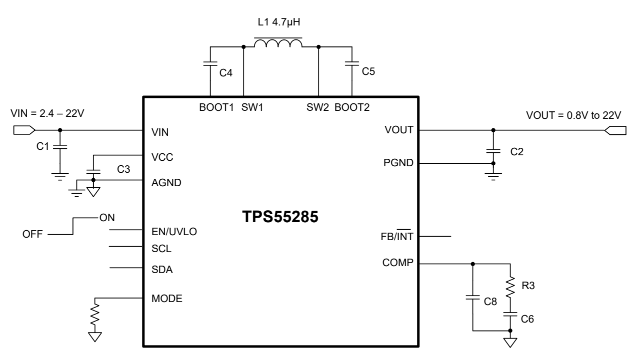
The TPS55285 offers input and output over-voltage protection, average inductor current limit, cycle-by-cycle peak current limit and output short circuit protection. The TPS55285 also ensures safe operating with output current limit without external output current sense resistor and hiccup mode protection in sustained overload conditions.

The TPS55285 allows the use of small inductor and capacitor with high switching frequency. It is available in 2.5mm × 3.5mm QFN package.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE
TPS55285	WQFN-HR	2.5mm × 3.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Circuit

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4 Pin Configuration and Functions

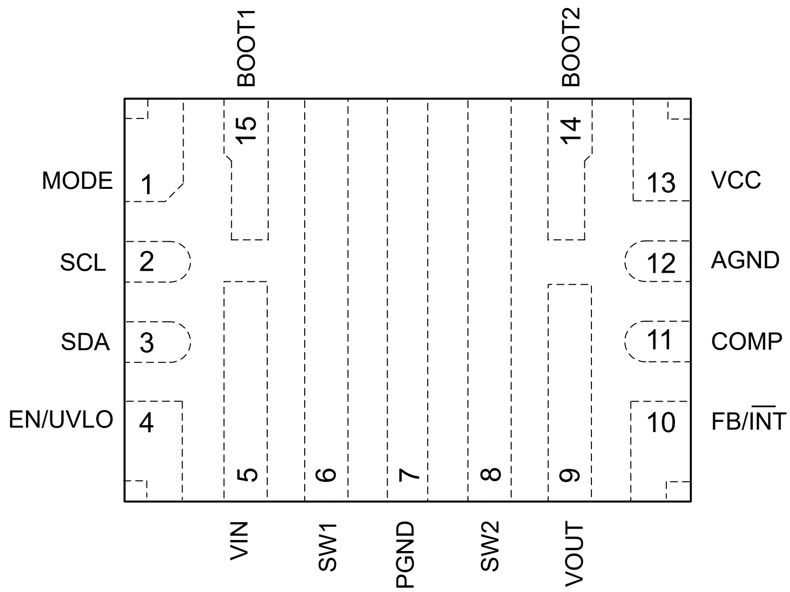

Figure 4-1. 15-pin WQFN-HR, VAL Package (Transparent Top View)

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	MODE	I	Select the TPS55285 default Output Enable (OE) bit by putting a resistor between this pin and AGND.
2	SCL	I	Clock of I^{2}C interface
3	SDA	I/O	Data of I^{2}C interface
4	EN/UVLO	I	Enable logic input and programmable input voltage under voltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode. After the voltage at EN/UVLO pin is above the logic high voltage of 1.125V, this pin acts as programmable UVLO input with 1.23V internal reference.
5	VIN	PWR	Input of the buck-boost conveter
6	SW1	PWR	The switching node pin of the buck side. It is connected to the drain of the internal buck low-side power MOSFET and the source of internal buck high-side power MOSFET.
7	PGND	PWR	Power ground of the device
8	SW2	PWR	The switching node pin of the boost side. It is connected to the drain of the internal boost low-side power MOSFET and the source of internal boost high-side power MOSFET.
9	VOUT	PWR	Output of the buck-boost converter
10	FB/$\overline{INT}$	I/O	When the device is set to use external output voltage feedback, connect to the center tap of a resistor divider to program the output voltage. When the device is set to use internal feedback, this pin is a fault indicator open-drain output. When there is an internal fault happening, this pin outputs logic low level.
11	COMP	O	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.
12	AGND	-	Signal ground of the device.
13	VCC	O	Output of the internal regulator. A ceramic capacitor of more than 4.7µF is required between this pin and the AGND pin.
14	BOOT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1µF must be connected between this pin and the SW2 pin.
15	BOOT1	O	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1µF must be connected between this pin and the SW1 pin.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, VOUT, SW1, SW2	–0.3	27	V
	BOOT1	SW1–0.3	SW1+6	V
	BOOT2	SW2–0.3	SW2+6	V
	EN/UVLO, VCC, SCL, SDA, COMP, FB/$\overline{INT}$, MODE	–0.3	6	V
	EN/UVLO, SCL, SDA, COMP, FB/$\overline{INT}$, MODE	–0.3	VCC+0.3	V
T_J	Operating Junction, T_J (3)	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.2 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range (Vout ≥ 3.0V)	2.4		22	V
	Input voltage range (Vout < 3.0V)	3		22	V
V_{OUT}	Output voltage range	0.8		22	V
L	Effective inductance range	1	4.7	10	µH
C_{IN}	Effective input capacitance range	4.7	22		µF
C_{OUT}	Effective output capacitance range	10	100	1000	µF
T_J	Operating junction temperature	–40		125	°C

5.3 Thermal Information

THERMAL METRIC(1)		VAL (WQFN) 15 PINS Standard	VAL (WQFN) 15 PINS EVM (2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.6	33	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	0.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	6.6	11.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured on TPS55285EVM, 4-layer, 2oz/1oz/1oz/2oz copper PCB.

5.4 Electrical Characteristics

T_J = -40°C to 125°C, V_{IN} = 12V and V_{OUT} = 20V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.4		22	V

T_J = -40°C to 125°C, V_{IN} = 12V and V_{OUT} = 20V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VIN_UVLO}	Under voltage lockout threshold	V_{IN} rising	2.8	2.9	3.0	V
		V_{IN} falling, V_{OUT} < 3V	2.6	2.7	2.8	V
		V_{IN} falling, V_{OUT} ≥ 3V	2.31	2.33	2.37	V
V_{VIN_OVP}	Input overvoltage protection threshold	Rising threshold	22	22.5	23	V
$V_{VIN\_OVP\_HYS}$	Input overvoltage protection hysteresis			0.9		V
I_Q	Quiescent current into VIN pin	IC enabled, no load, no switching. V_{IN} = 3.0V to 22V, V_{OUT} = 0.8V, V_{FB} = V_{REF} + 0.1V, Tj up to 125°C		770		µA
	Quiescent current into VOUT pin	IC enabled, no load, no switching, V_{IN} = 3.0V, V_{OUT} = 3V to 22V, V_{FB} = V_{REF} + 0.1V, Tj up to 125°C		770		µA
I_{SD}	Shutdown current into VIN pin	IC disabled, V_{IN} = 3.0V to 22V, Tj up to 125°C		1.3	3.8	µA
V_{CC}	Internal regulator output	V_{IN} = 8V, V_{OUT} = 20V, I_{VCC} = 20mA	5.0	5.2	5.4	V
EN/UVLO						
V_{EN_H}	EN Logic high threshold	V_{CC} = 3.0V to 5.5V			1.125	V
V_{EN_L}	EN Logic low threshold	V_{CC} = 3.0V to 5.5V	0.4			V
V_{EN_HYS}	Enable threshold hysteresis	V_{CC} = 3.0V to 5.5V	0.04			V
V_{UVLO}	UVLO rising threshold at the EN/UVLO pin	V_{CC} = 3.0V to 5.5V	1.20	1.23	1.26	V
V_{UVLO_HYS}	UVLO threshold hysteresis	V_{CC} = 3.0V to 5.5V		13		mV
I_{UVLO}	Sourcing current at the EN/UVLO pin	$V_{EN/UVLO}$ = 1.3V	4.5	5	5.5	µA
OUTPUT						
V_{OUT}	Output voltage range		0.8		22	V
V_{VOUT_OVP}	Output overvoltage protection threshold	Rising threshold	22	22.5	23	V
$V_{VOUT\_OVP\_HYS}$	Output overvoltage protection hysteresis			1		V
$V_{VOUT\_OVP\_FB}$	Detected with respect to FB rising		110.5	115	119.5	%
$V_{VOUT\_OVP\_FB\_HYS}$	hysteresis			2.3		%
I_{FB_LKG}	Leakage current at FB pin	Tj up to 125°C			100	nA
I_{VOUT_LKG}	Leakage current into VOUT pin	IC disabled, V_{OUT} = 20V, V_{SW2} = 0V, Tj up to 125°C		1	20	µA
I_{DISCHG}	Output discharge current, OE shutdown	V_{OUT} = 20V, V_{CC} = 5.2V	40	100	170	mA
	Output discharge current, EN and V_{IN} shutdown	V_{OUT} = 20V, V_{CC} = 5.2V	30	60	105	mA
INTERNAL REFERENCE DAC						
	Resolution of reference voltage DAC			11		bits
V_{OUT_FULL}	Output voltage when V_{REF} is set to 1.129V	VOUT_FS=03h, REF=0780h, V_{REF}=1.129V	19.7	20	20.3	V
		VOUT_FS=02h, REF=0780h, V_{REF}=1.129V	14.78	15	15.22	V
		VOUT_FS=01h, REF=0780h, V_{REF}=1.129V	9.85	10	10.15	V
		VOUT_FS=00h, REF=0780h, V_{REF}=1.129V	4.93	5	5.07	V

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T_J = -40°C to 125°C, V_{IN} = 12V and V_{OUT} = 20V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT_ZERO}	Output voltage when V_{REF} is set to 45mV	VOUT_FS=03h, REF=0000h, V_{REF}=45mV	0.74	0.8	0.86	V
		VOUT_FS=02h, REF=0000h, V_{REF}=45mV	0.55	0.6	0.65	V
		VOUT_FS=01h, REF=0000h, V_{REF}=45mV	0.36	0.4	0.44	V
		VOUT_FS=00h, REF=0000h, V_{REF}=45mV	0.18	0.2	0.22	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage at the FB/$\overline{INT}$ pin when using external feedback	External feedback with REF=0780H	1.117	1.129	1.141	V
		External feedback with REF=058CH	0.837	0.846	0.855	V
		External feedback with REF=0334H	0.502	0.508	0.514	V
		External feedback with REF=01A4H	0.276	0.282	0.288	V
POWER SWITCH						
$R_{DS(on)}$	Low-side MOSFET on resistance on buck side	V_{OUT} = 20V, V_{CC}=5.2V		15.5		mΩ
	High-side MOSFET on resistance on buck side	V_{OUT} = 20V, V_{CC}=5.2V		14.5		mΩ
	Low-side MOSFET on resistance on boost side	V_{OUT} = 20V, V_{CC}=5.2V		15.5		mΩ
	High-side MOSFET on resistance on boost side	V_{OUT} = 20V, V_{CC}=5.2V		14.5		mΩ
INTERNAL CLOCK						
f_{SW}	Switching frequency	FSW = 00b		400		kHz
f_{SW}	Switching frequency	FSW = 11b		2200		kHz
t_{OFF_min}	Min. off time	Boost mode		90	145	ns
t_{ON_min}	Min. on time	Buck mode		90	130	ns
CURRENT LIMIT						
I_{LIM_AVG}	Average inductor current limit	V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz, FPWM	7	8		A
		V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz, PFM	7	8		A
I_{LIM_PK}	Peak inductor current limit at boost high side	V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz, FPWM		13		A
		V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz, PFM		13		A
OUTPUT CURRENT LIMIT						
I_{OUT_LIMIT}	Output current limit	I_{OUT_LIMIT} Register = 1011 1100b		3		A
		I_{OUT_LIMIT} Register = 1110 0100b		5		A
CABLE VOLTAGE DROP COMPENSATION						
V_{OUT_CDC}	VOUT increase for cable drop compensation	CDC[2:0]=111, INTFB = 11b, I_{OUT} = 5A	610	700	790	mV
		CDC[2:0]=111, INTFB = 11b, I_{OUT} = 1A, FPWM	40	140	230	mV
		CDC[2:0]=001, INTFB = 11b, I_{OUT} = 5A	70	100	115	mV
		CDC[2:0]=001, INTFB = 11b, I_{OUT} = 1A, FPWM		15	40	mV
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 400mV, V_{COMP}=1.1V, V_{CC}=5V		20		µA

T_J = -40°C to 125°C, V_{IN} = 12V and V_{OUT} = 20V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} - 400mV, V_{COMP}=1.1V, V_{CC}=5V		60		µA
V_{CCLPH}	High clamp voltage at the COMP pin			1.2		V
V_{CCLPL}	Low clamp voltage at the COMP pin			0.7		V
G_{EA}	Error amplifier transconductance			190		µA/V
SOFT START						
t_{SS}	Soft-start time		2.5	3.6	5.2	ms
SPREAD SPECTRUM						
HICCUP						
t_{HICCUP}	Hiccup off time			76		ms
MODE						
I_{MODE}	Sourcing current from MODE pin		9	10	11	µA
V_{MODE_DT3}	Detection threshold voltage at MODE pin		0.169	0.189	0.209	V
LOGIC INTERFACE						
V_{I2C_IO}	IO voltage range for I^2C		1.7		5.5	V
V_{I2C_H}	I^2C input high threshold	V_{CC} = 3.0V to 5.5V			1.2	V
V_{I2C_L}	I^2C input low threshold	V_{CC} = 3.0V to 5.5V	0.4			V
$I_{FB/\overline{INT}\_H}$	Leakage current into FB/$\overline{INT}$ pin when outputting high impedance	$V_{FB/\overline{INT}}$ = 5V			100	nA
$V_{FB/\overline{INT}\_L}$	Output low voltage range of the FB/$\overline{INT}$ pin	Sinking 4mA current		0.03	0.1	V
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below Tsd		20		°C

5.5 I2C Timing Characteristics

T_J = -40°C to 125°C, V_{IN} = 12V and V_{OUT} = 20V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C TIMING						
f_{SCL}	SCL clock frequency		100		1000	kHz
t_{BUF}	Bus free time between a STOP and START condition	Fast mode plus	0.5			µs
$t_{HD(STA)}$	Hold time (repeated) START condition		260			ns
t_{LOW}	Low period of the SCL clock		0.5			µs
t_{HIGH}	High period of the SCL clock		260			ns
$t_{SU(STA)}$	Setup time for a repeated START condition		260			ns
$t_{SU(DAT)}$	Data setup time		50			ns
$t_{HD(DAT)}$	Data hold time		0			µs
t_{RCL}	Rise time of SCL signal				120	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an ACK bit				120	ns
t_{FCL}	Fall time of SCL signal				120	ns
t_{RDA}	Rise time of SDA signal				120	ns
t_{FDA}	Fall time of SDA signal				120	ns

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T_J = -40°C to 125°C, V_{IN} = 12V and V_{OUT} = 20V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU(STO)}$	Setup time of STOP condition		260			ns
C_B	Capacitive load for SDA and SCL				200	pF

5.6 Typical Characteristics

V_{IN} = 12V, T_A = 25°C, f_{SW} = 400kHz, unless otherwise noted.

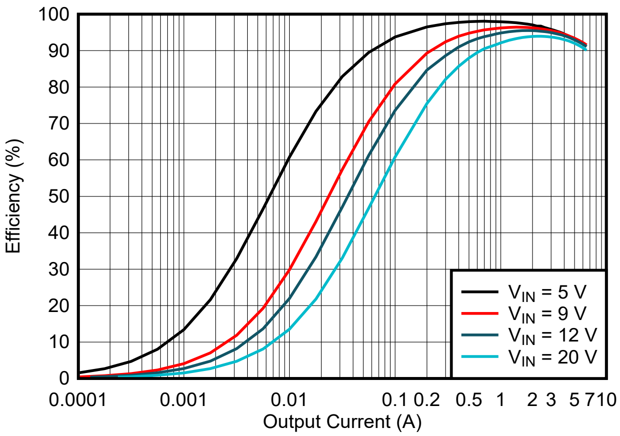

Figure 5-1. Efficiency vs Output Current, V_{OUT} = 5V, FPWM

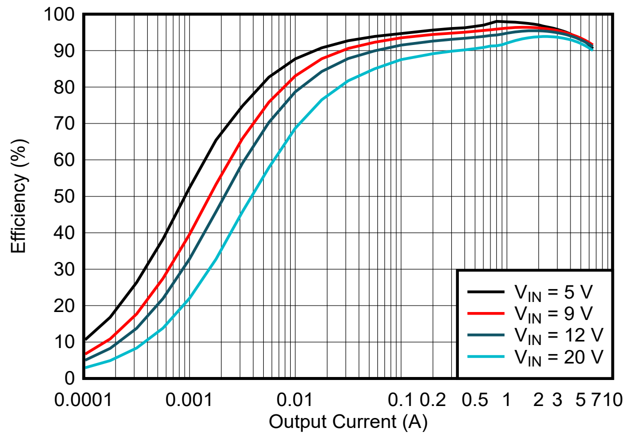

Figure 5-2. Efficiency vs Output Current, V_{OUT} = 5V, PFM

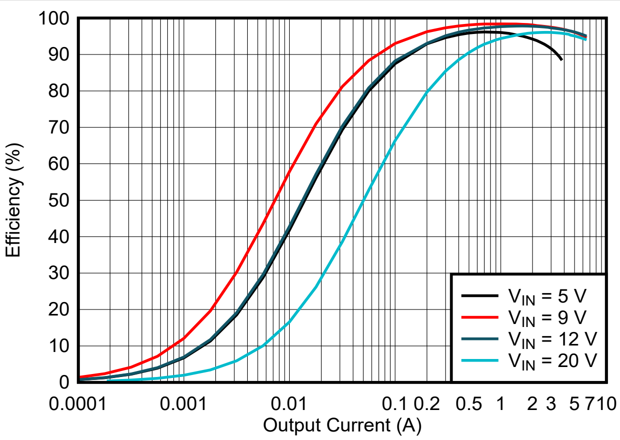

Figure 5-3. Efficiency vs Output Current, V_{OUT} = 9V, FPWM

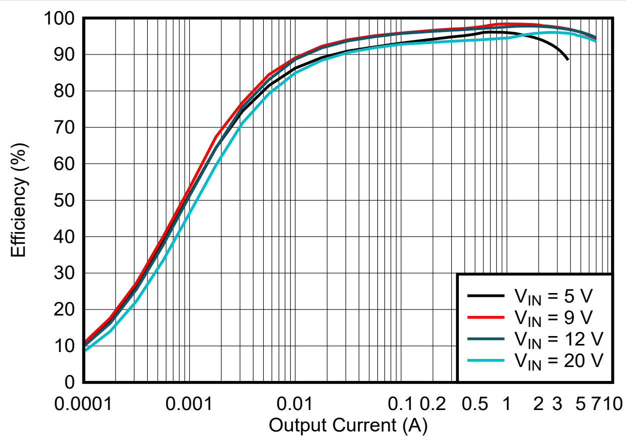

Figure 5-4. Efficiency vs Output Current, V_{OUT} = 9V, PFM

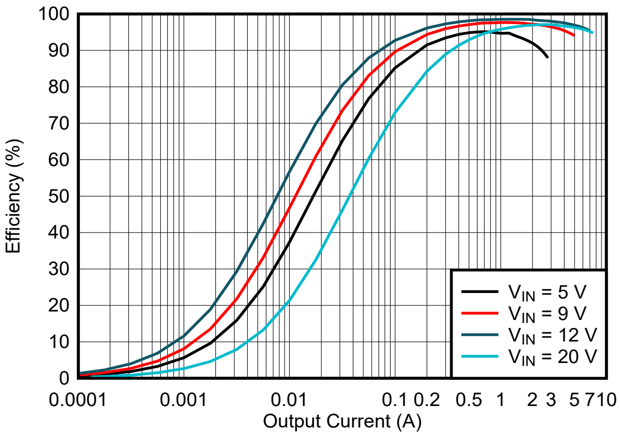

Figure 5-5. Efficiency vs Output Current, V_{OUT} = 12V, FPWM

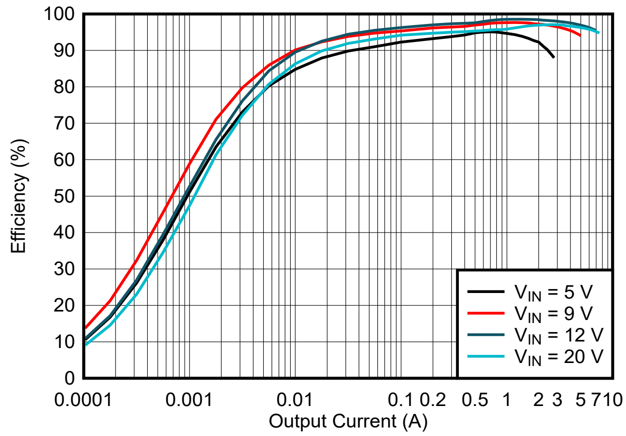

Figure 5-6. Efficiency vs Output Current, V_{OUT} = 12V, PFM

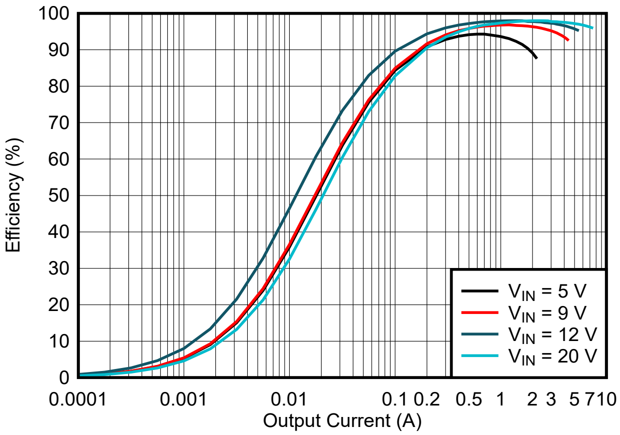

Figure 5-7. Efficiency vs Output Current, V_{OUT} = 15V, FPWM

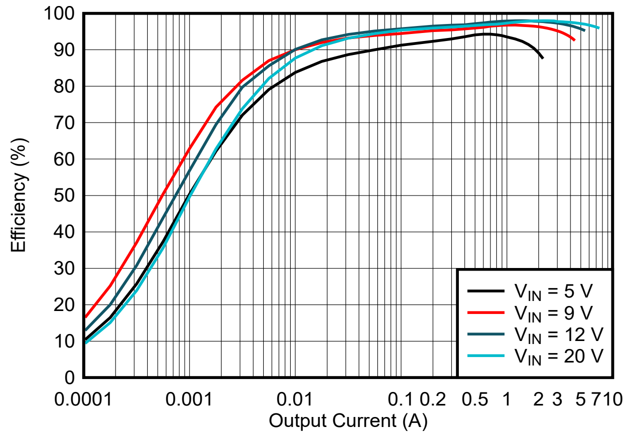

Figure 5-8. Efficiency vs Output Current, V_{OUT} = 15V, PFM

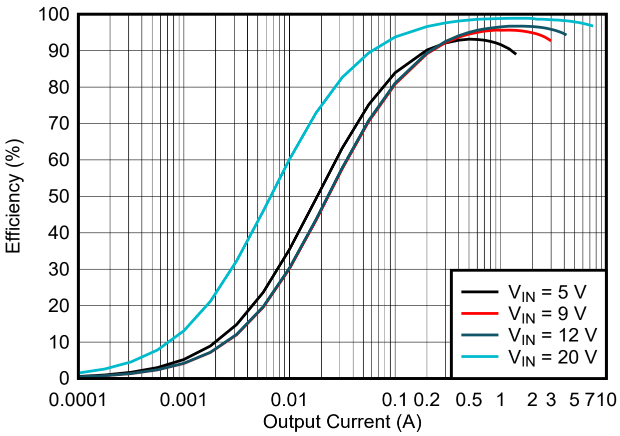

Figure 5-9. Efficiency vs Output Current, V_{OUT} = 20V, FPWM

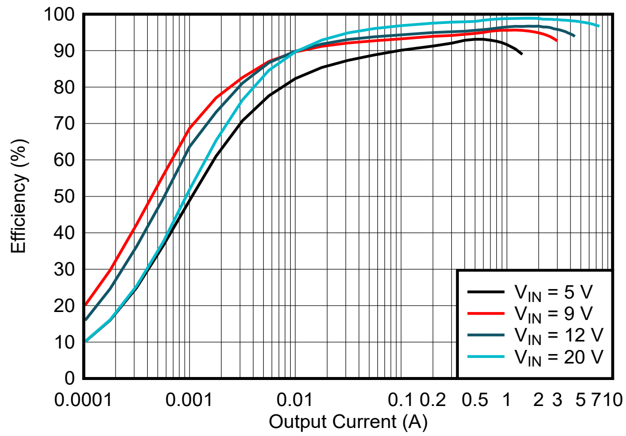

Figure 5-10. Efficiency vs Output Current, V_{OUT} = 20V, PFM

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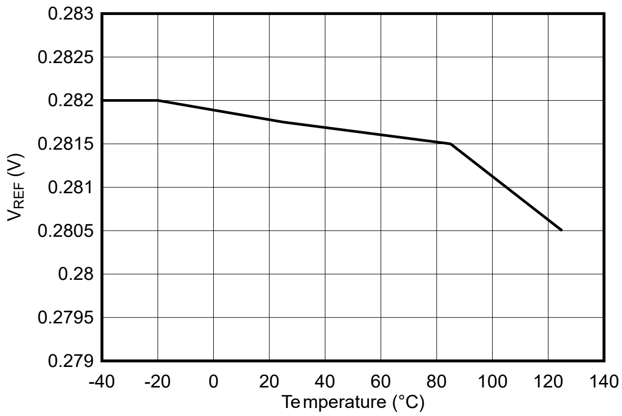

Figure 5-11. Reference Voltage vs Temperature (V_{REF} = 0.282V)

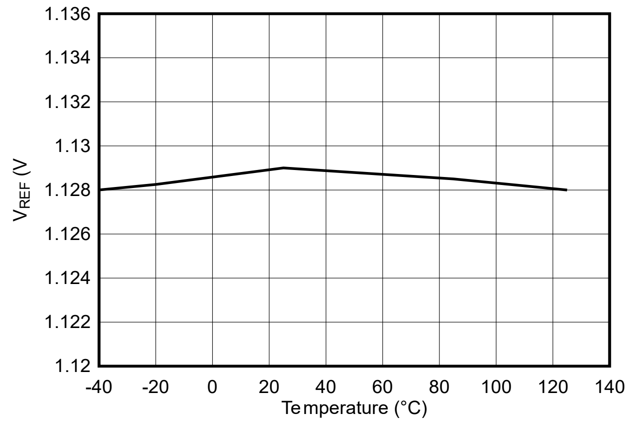

Figure 5-12. Reference Voltage vs Temperature (V_{REF} = 1.129V)

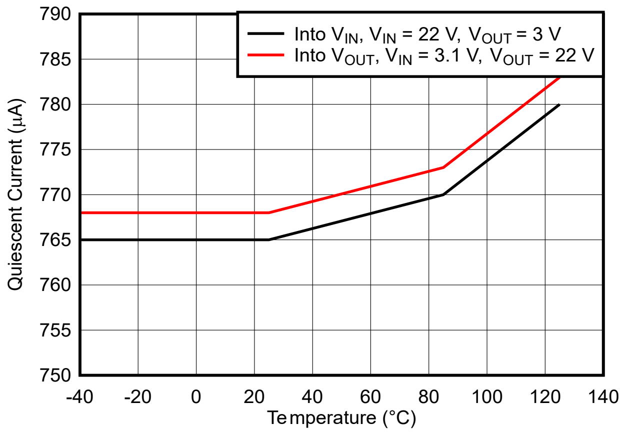

Figure 5-13. Quiescent Current vs Temperature

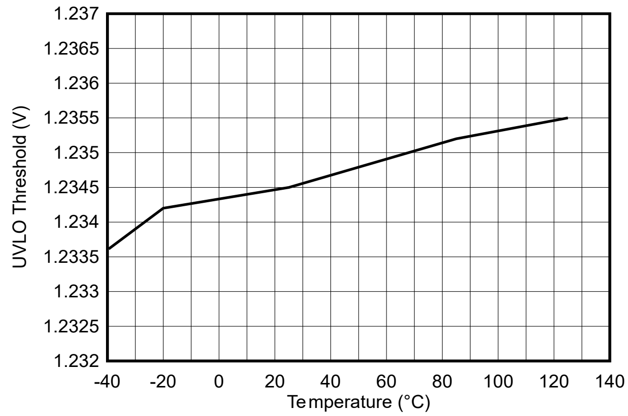

Figure 5-14. ENABLE/UVLO Rising Threshold vs Temperature

6 Detailed Description

6.1 Overview

The TPS55285 is a 8A buck-boost DC to DC converter with integrated four MOSFETs. The TPS55285 can operate over a wide range of 2.4V to 22V input voltage and output 0.8V to 22V. It can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPS55285 operates in the buck mode when the input voltage is greater than the output voltage and in the boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS55285 operates in one-cycle buck and one-cycle boost mode alternately.

The TPS55285 utilizes an average current mode control scheme. Current mode control provides simplified loop compensation, rapid response to the load transients and inherent line voltage rejection. An error amplifier compares the feedback voltage of the output voltage with the internal reference voltage. The output of the error amplifier determines the average inductor current.

The TPS55285 works in fixed-frequency PWM mode at moderate to heavy load currents. In the light load condition, the TPS55285 can be configured to automatically transition to PFM mode or be forced in PWM mode by setting the corresponding bit in an internal register.

The TPS55285 can adjust the output voltage by setting the internal register through I^2C interface. An internal 11 bit DAC adjusts the reference voltage related to the value writing into the DAC register. The device also can limit the output current without external current sense resistor, the output current limit can be set by internal register.

The TPS55285 provides typical 8A average inductor current limit. In addition, it provides cycle-by-cycle peak inductor current limit as well when the inductor peak current is above peak current limit.

A precision voltage threshold of 1.23V with 5µA sourcing current at the EN/UVLO pin supports programmable input under-voltage lockout (UVLO) with hysteresis. When input voltage is higher than 22.5V, the input over-voltage protection (OVP) feature turns off the device to prevent damage.

The output over-voltage protection (OVP) feature turns off the high side FETs to prevent damage to the devices powered by the TPS55285.

The TPS55285 provides a hiccup mode option to reduce the heating in the power components when the output short circuit happens. When the hiccup mode is enabled, the TPS55285 turns off for 76ms and restarts soft startup.

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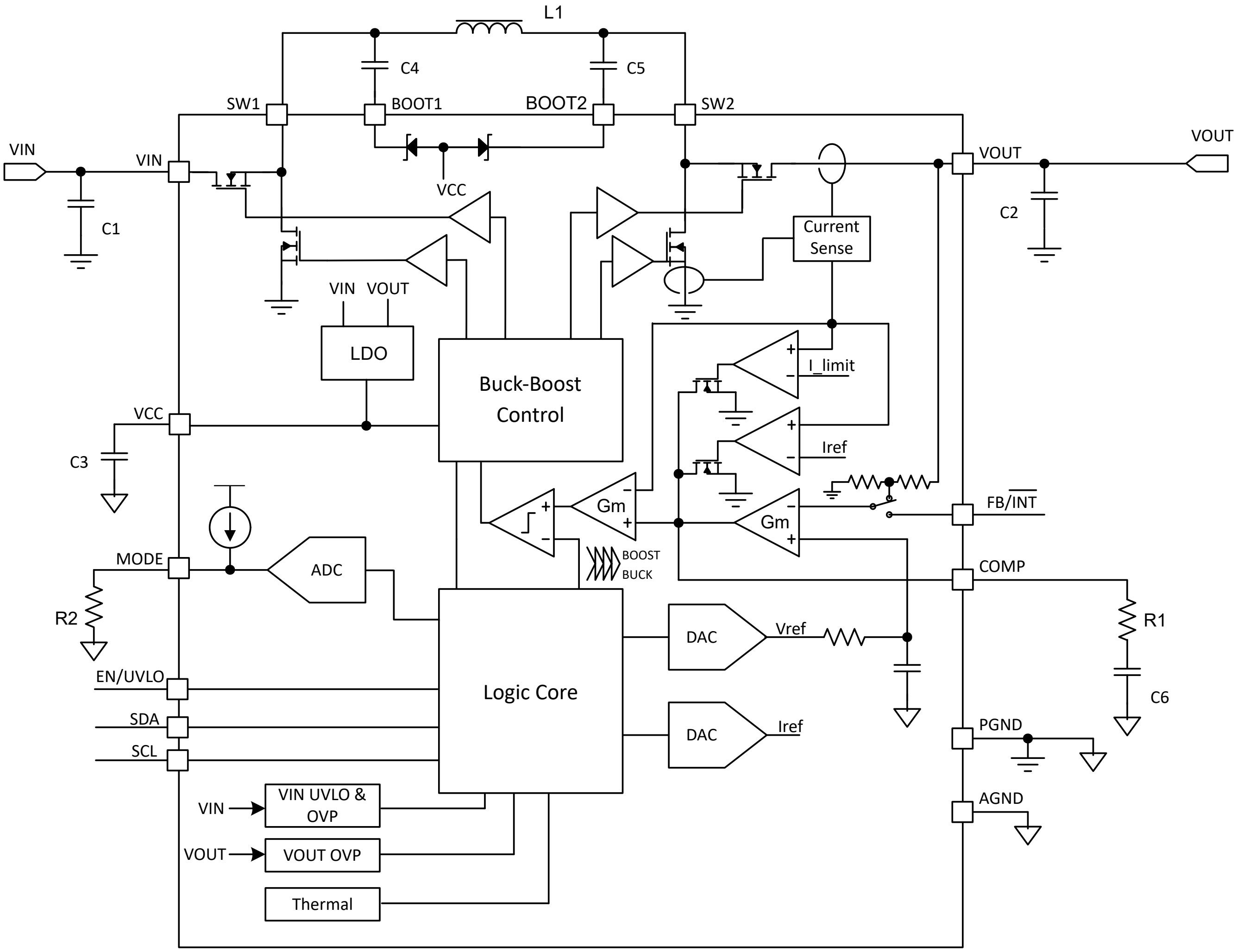
6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 VCC Power Supply

An internal LDO to supply the TPS55285 outputs regulated 5.2V voltage at the VCC pin. When V_{IN} is less than V_{OUT}, the internal LDO selects the power supply source by comparing V_{IN} to a rising threshold of 6.2V with 0.3V hysteresis. When V_{IN} is higher than 6.2V, the supply for LDO is V_{IN}. When V_{IN} is lower than 5.9V, the supply for LDO is V_{OUT}. When V_{OUT} is less than V_{IN}, the internal LDO selects the power supply source by comparing V_{OUT} to a rising threshold of 6.2V with 0.3V hysteresis. When V_{OUT} is higher than 6.2V, the supply for LDO is V_{OUT}. When V_{OUT} is lower than 5.9V, the supply for LDO is V_{IN}. Table 6-1 shows the supply source selection for the internal LDO.

Table 6-1. V_{CC} Power Supply Logic

V_{IN}	V_{OUT}	INPUT for V_{CC} LDO
V_{IN} > 6.2V	V_{OUT} > V_{IN}	V_{IN}
V_{IN} < 5.9V	V_{OUT} > V_{IN}	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT} > 6.2V	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT} < 5.9V	V_{IN}

6.3.2 Default Output Enable(OE) bit Status

By placing different resistors between the MODE pin and the AGND pin, the TPS55285 selects default Output Enable (OE) bit value. Output Enable (OE) bit is logic bit to control device output in 06H register.

If default Output Enable (OE) bit is set to 0, when V_{IN} and EN/UVLO pins exceed UVLO threshold, the device doesn't switch until Output Enable (OE) bit is set to 1 in 06H register.

If default Output Enable (OE) bit is set to 1, the FB bit in 04H register is also set to 1 automatically to select external feedback network. Once V_{IN} and EN/UVLO pins exceed UVLO threshold, the device starts switching with 282mV V_{REF}. External feedback resistors is needed in this case.

Table 6-2. I^2C Target Address and Default OE bit

Resistor Value (kΩ)	I^2C TARGET ADDRESS	DEFAULT OUTPUT ENABLE (OE) BIT
0	75H	0
24.9	75H	1

6.3.3 Input Undervoltage Lockout

When the input voltage is below 2.4V, the TPS55285 is disabled. When the input voltage is above 3V, the TPS55285 can be enabled by pulling the EN pin to a high voltage above 1.3V.

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6.3.4 Enable and Programmable UVLO

The TPS55285 has a dual function enable and undervoltage lockout (UVLO) circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 3V and the EN/UVLO pin is pulled above 1.125V but less than the enable UVLO threshold of 1.23V, the TPS55285 is enabled but still in standby mode. The TPS55285 starts to detect the resistance between MODE pin and ground. After that, the TPS55285 selects the I^2C target address and default OE bit status accordingly.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.23V, the TPS55285 is enabled for I^2C communication and switching operation. A hysteresis current I_{UVLO_HYS} is sourced out of the EN/UVLO pin to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

By using resistor divider as shown in Figure 6-1, the turn-on threshold is calculated using Equation 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times (1 + \frac{R1}{R2}) \quad (1)$$

where

- V_{UVLO} is the UVLO threshold of 1.23V at the EN/UVLO pin

The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by the Equation 2.

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

where

- I_{UVLO_HYS} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}

The EN/UVLO pin voltage needs to be less than 5.5V when using resistor divider to program the VIN UVLO threshold.

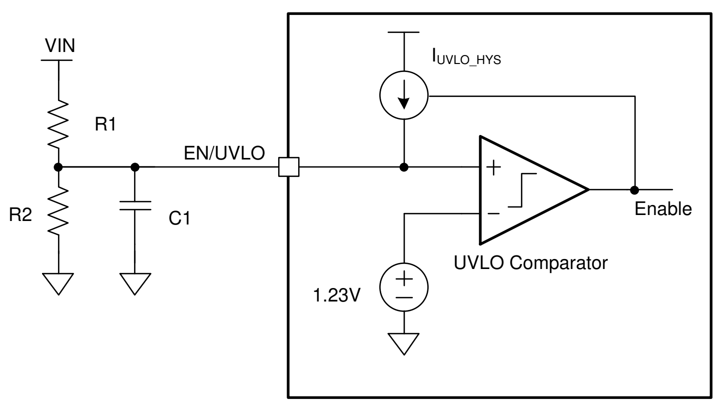

Figure 6-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin

Using an NMOSFET together with a resistor divider can implement both logic enable and programmable UVLO as shown in Figure 6-2. The EN logic high level must be greater than enable threshold plus the V_{th} of the NMOSFET Q1. The Q1 also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.

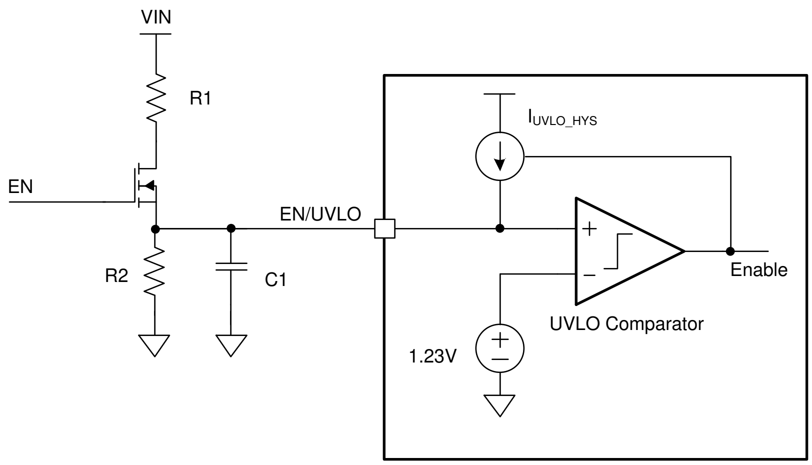

Figure 6-2. Logic Enable and Programmable UVLO

6.3.5 Soft Start

When the input voltage is above the UVLO threshold and the voltage at the EN/UVLO pin is above the enable UVLO threshold, the TPS55285 is ready to accept the command from I^2C controller device. An I^2C controller device can configure the internal registers of the TPS55285.

Once an I^2C controller device sets the OE bit to 1 or device detects the default OE bit is 1, the TPS55285 starts to ramp up the output voltage by ramping an internal reference voltage from 0V to a voltage set in the internal registers 00h and 01h within typical 3.6ms.

6.3.6 Shutdown and Load Discharge

When the EN/UVLO pin voltage is pulled below 0.4V, the TPS55285 is in shutdown mode, and all functions are disabled. All internal registers are reset to default values. When the EN/UVLO pin is at high logic level and the OE bit is cleared to 0, the TPS55285 turns off the switching operation but keeps the I^2C interface active.

If the DISCHG bit in the register 06h is set to 1, the TPS55285 discharges the output voltage below 0.8V by an internal constant current I_{DISCHG} when the OE bit is cleared to 0. If input voltage UVLO is triggered or EN/UVLO pin is pulled to low logic level, the TPS55285 output voltage is discharged until VCC is below V_{CC_UVLO}.

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6.3.7 Switching Frequency

The TPS55285 uses a fixed frequency average current control scheme. The switching frequency is set by FSW bit in register 06H with four options: 400kHz, 800kH, 1.6MHz, 2.2MHz.

To reduce the switching power loss in high power applications, it is recommended to set the swtiching frequency at 400kHz or 800kHz. If a system requires higher switching frequency at 1.6MHz or 2.2MHz for smaller solution size, it is recommended to operate at lower switch current for better thermal performance.

It is recommended to set the switching frequency first before enabling the OE bit.

6.3.8 Switching Frequency Dithering

The TPS55285 provides an optional switching frequency dithering that is enabled by SPREADSPECTRUM bit in 06H register at FPWM mode to minimize EMI interference. The device uses a triangle jitter to spread the switching freequency with ±7% of normal frequency set by FSW bit. The frequency of the triangle jitter is 1.5kHz when normal swtiching frequency is 400kHz. The frequency of the triangle jitter is 9kHz when normal switching frequency is 2.2MHz.

6.3.9 Inductor Current Limit

The TPS55285 implements both peak current and average inductor current limit. The average current mode control loop uses the current sense information at the high-side MOSFET of the boost leg to clamp the maximum average inductor current to 8A (typical).

Besides the average current limit, a peak current limit protection is implemented during transient to protect the device against over current condition beyond the capability of the device.

6.3.10 Internal Charge Path

Each of the two high-side MOSFET drivers is biased from its floating bootstrap capacitor, which is normally re-charged by V_{CC} through both the external and internal bootstrap diodes when the low-side MOSFET is turned on. When the TPS55285 operates exclusively in the buck or boost regions, one of the high-side MOSFETs is constantly on. An internal charge path, from VOUT and BOOT2 to BOOT1 or from VIN and BOOT1 to BOOT2, charges the bootstrap capacitor to V_{CC} so that the high-side MOSFET remains on.

6.3.11 Output Voltage Setting

There are two ways to set the output voltage: changing the feedback ratio and changing the reference voltage. The TPS55285 has a 11-bit DAC to program the reference voltage from 45mV to 1.2V. The TPS55285 can also select an internal feedback resistor divider or an external resistor divider by setting the FB bit in register 04h. When the FB bit is set to 0, the output voltage feedback ratio is set in internal register 04h. When the FB bit is set to 1, the output voltage feedback ratio is set by an external resistor divider.

When using internal output voltage feedback settings, there are four feedback ratios programmable by writing the INTFB[1:0] bits of register 04H. With this function, the TPS55285 can limit the maximum output voltage to different values. In addition, the minimum step of the output voltage change is also programmed to 10mV, 7.5mV, 5mV, and 2.5mV, accordingly.

When using an external output voltage feedback resistor divider as shown in Figure 6-3, use Equation 3 to calculate the output voltage with the reference voltage at the FB/$\overline{\text{INT}}$ pin.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB\_UP}}{R_{FB\_BT}}\right) \quad (3)$$

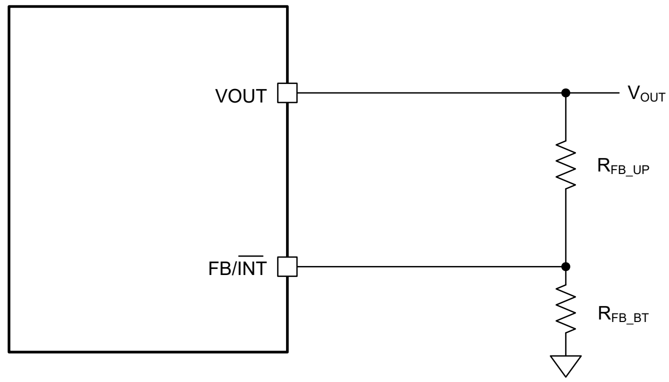

Figure 6-3. Output Voltage Setting by External Resistor Divider

TI recommends using 100kΩ for the up resistor R_{FB_UP}. The reference voltage V_{REF} at the FB/$\overline{INT}$ pin is programmable from 45mV to 1.2V by writing a 11-bit data into register 00H and 01H.

6.3.12 Output Current Limit

The TPS55285 supports output current limit function in buck, buck-boost and boost mode without external current sense resistor. The output current limit is programmable from 500mA to 6.35A by Current_Limit_Setting bit in 02H register. The programmable output current limit step is 50mA.

The output current limit can be disabled by reset the Current_Limit_EN bit in the Current_Limit register to 0.

6.3.13 Output Cable Voltage Drop Compensation

To compensate the voltage drop across a cable from the output of the USB port to its powered device, the TPS55285 can lift its output voltage in proportion to the load current.

By default, the cable voltage drop compensation function is disabled. Set the CDC_OPTION bit to 1 to enable cable voltage drop compensation function. Write the value into the bit CDC [2:0] in register 05H to get the desired voltage compensation.

The output voltage rise versus the sensed output current is shown in Figure 6-4.

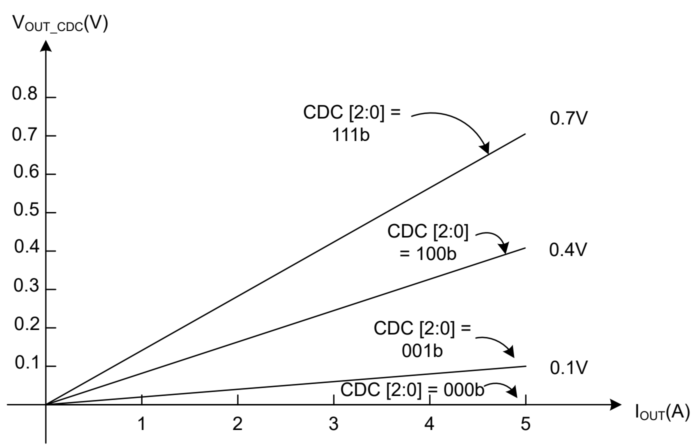

Figure 6-4. Output Voltage Rise versus Output Current

6.3.14 Input Overvoltage Protection

The TPS55285 has input overvoltage protection which avoids any damage to the device in case the current flows from the output to the input and the input source cannot sink current in FPWM mode. When the input voltage at the VIN pin is detected above 22.5V typically, the internal soft-start circuit is reset but all internal

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registers values remain unchanged when VIN OVP is triggered. The converter automatically restarts when the input voltage drops the hysteresis value lower than the input overvoltage protection threshold.

6.3.15 Output Overvoltage Protection

The TPS55285 has an absolute output overvoltage protection. When the output voltage at the VOUT pin is detected above 22.5V typically, the TPS55285 turns off two high-side FETs and turns on two low-side FETs until its output voltage drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the VOUT pin to protect the device.

The TPS55285 monitors a resistor-divided feedback voltage to detect output over-voltage condition. When the feedback voltage is over 115% of the target voltage, the device stops switching until output voltage drops the 2.3% hysteresis value, this function secures the circuits connected to the output from excessive overvoltage. When selecting internal feedback resistor, the TPS55285 detects the internal feedback voltage for overvoltage protection.

6.3.16 Output Short Circuit Protection

In addition to the average inductor current limit, the TPS55285 implements the output short-circuit protection by entering hiccup mode. To enable hiccup mode, the HICCUP bit in register 06h must be set. After soft start-up time of 3.6ms, the TPS55285 monitors the average inductor current and output voltage. Whenever the output short circuit happens, causing the average inductor current hitting the set limit and the output voltage below 0.8V, the TPS55285 shuts down the switching for 76ms (typical) and then repeats the soft start for 3.6ms. The hiccup mode helps reduce the total power dissipation on the TPS55285 in the output short-circuit or overcurrent condition.

6.3.17 Thermal Shutdown

The TPS55285 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 175°C (typical). The internal soft-start circuit is reset but all internal registers values remain unchanged when thermal shutdown is triggered. The converter automatically restarts when the junction temperature drops below the thermal shutdown hysteresis of 20°C (typical) below the thermal shutdown threshold.

6.4 Device Functional Modes

In light load condition, the TPS55285 can work in PFM or forced PWM mode to meet different application requirements. PFM mode decreases switching frequency to reduce the switching loss thus it gets high efficiency at light load condition. The FPWM mode keeps the switching frequency unchanged to avoid undesired low switching frequency but the efficiency becomes lower than that of PFM mode.

By default, the TPS55285 works in PFM mode. To set the device works in forced PWM mode, set the 01 bit of the register 06h to 1.

6.4.1 PWM Mode

In FPWM mode, the TPS55285 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to reduce the average inductor current down to deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this condition. However, with the fixed switching frequency, there is no audible noise or other problems that might be caused by low switching frequency in light load condition.

6.4.2 Power Save Mode

The TPS55285 improves the efficiency at light load condition with PFM mode. By enabling the PFM function in the internal register, the TPS55285 can work in PFM mode at light load condition. When the TPS55285 operates at light load condition, the output of the internal error amplifier decreases to make the inductor peak current down to deliver less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the switch-off time. When the TPS55285 works in buck mode, once the inductor current becomes zero, the low-side switch of the buck side is turned off to prevent the reverse current from output to ground. When the TPS55285 works in boost mode, once the inductor current becomes zero, the high side-switch of the boost side is turned off to prevent the reverse current from output to input. The TPS55285 resumes switching until the output voltage drops. Thus PFM mode reduces switching cycles and eliminates the power loss by the reverse inductor current to get high efficiency in light load condition.

6.5 Programming

The TPS55285 uses I^2C interface for flexible converter parameter programming. I^2C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). I^2C devices can be considered as controllers or targets when performing data transfers. A controller is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The TPS55285 operates as a target device with address 75h. Receiving control inputs from the controller device like a microcontroller or a digital signal processor reads and writes the internal registers 00h through 07h. The I^2C interface of the TPS55285 supports both standard mode (up to 100 kbit/s) and fast mode plus (up to 1000 kbit/s). Both SDA and SCL must be connected to the positive supply voltage through current sources or pullup resistors. When the bus is free, both lines are in high voltage.

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6.5.1 Data Validity

The data on the SDA line must be stable during the high level period of the clock. The high level or low level state of the data line can only change when the clock signal on the SCL line is low level. One clock pulse is generated for each data bit transferred.

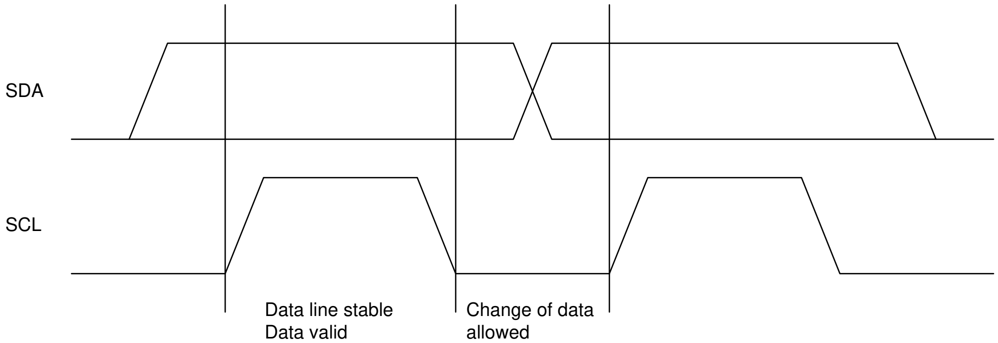

Figure 6-5. I²C Data Validity

6.5.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A high level to low level transition on the SDA line while SCL is at high level defines a START condition. A low level to high level transition on the SDA line when the SCL is at high level defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition.

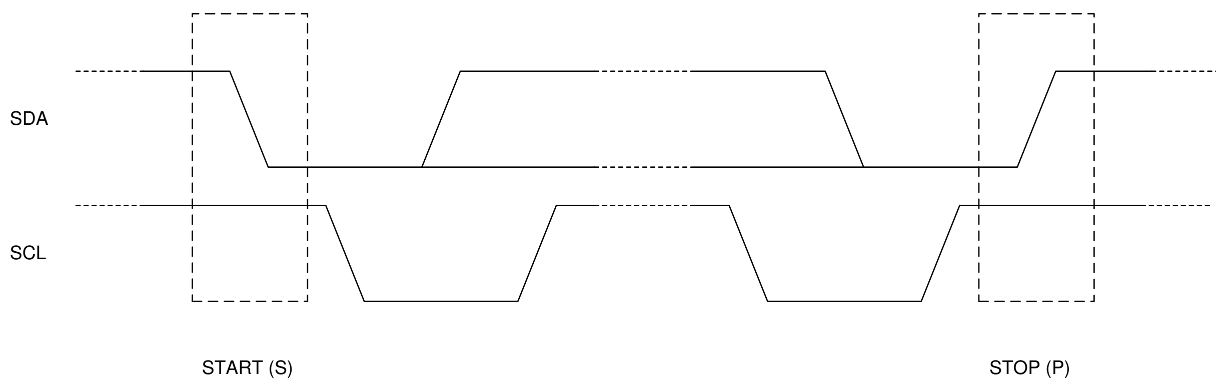

Figure 6-6. I²C START and STOP Conditions

6.5.3 Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the controller into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and release the clock line SCL.

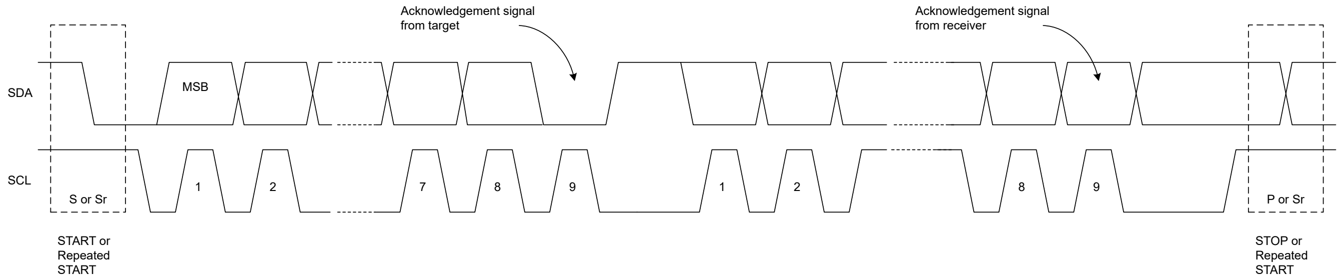

Figure 6-7. Byte Format

6.5.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9^{th} clock pulse, are generated by the controller.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line to low level and it remains stable low level during the high level period of this clock pulse.

The Not Acknowledge signal is when SDA remains high level during the 9^{th} clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

6.5.5 Target Address and Data Direction Bit

After the START, a target address is sent. This address is seven bits long followed by the eighth bit as a data direction bit (bit R/$\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

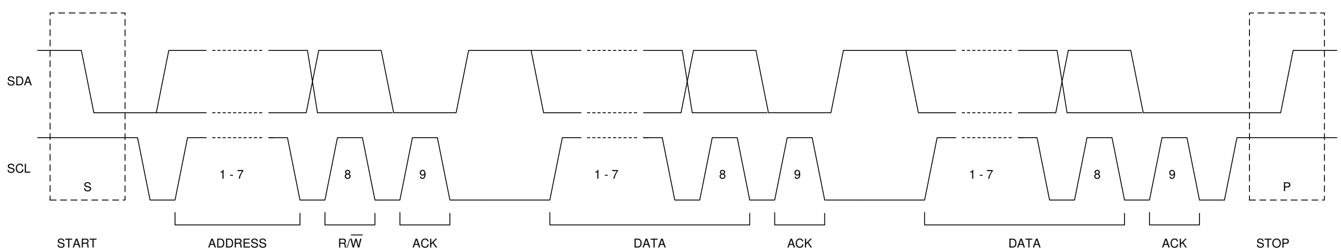

Figure 6-8. Target Address and Data Direction

6.5.6 Single Read and Write

Figure 6-9 and Figure 6-10 show the single-byte write and single-byte read format of the I²C communication.

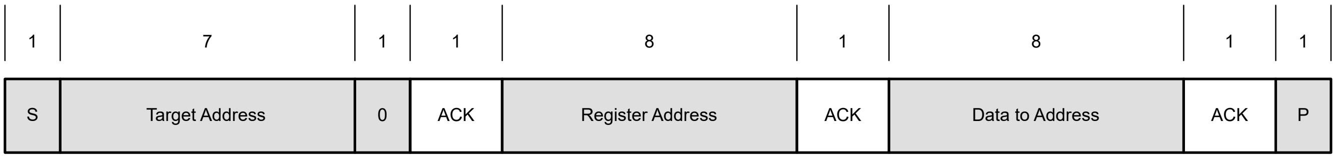

Figure 6-9. Single-byte Write

Figure 6-10. Single-byte Read

If the register address is not defined, the TPS55285 sends back NACK and goes back to the idle state.

6.5.7 Multi-Read and Multi-Write

The TPS55285 supports multi-read and multi-write.

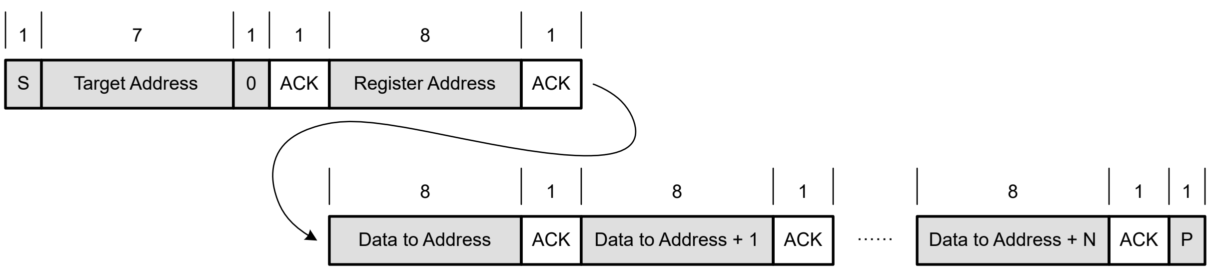

Figure 6-11. Multi-byte Write

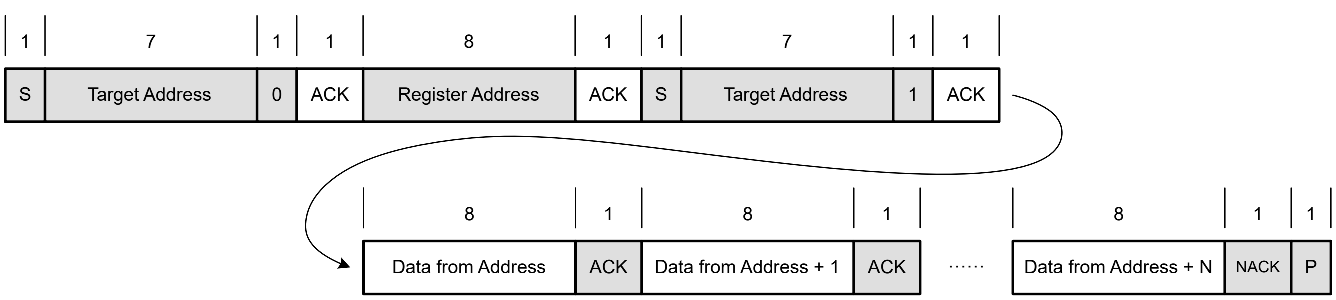

Figure 6-12. Multi-byte Read

7 Register Maps

Table 7-1 lists the memory-mapped registers for the device registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations, and the register contents should not be modified.

Table 7-1. Device Registers

Address	Acronym	Register Name	Section
0h, 1h	REF	Reference Voltage	Go
2h	IOUT_LIMIT	Current Limit Setting	Go
3h	VOUT_SR	Slew Rate	Go
4h	VOUT_FS	Feedback Selection	Go
5h	CDC	Cable Compensation	Go
6h	MODE	Mode Control	Go
7h	STATUS	Operating Status	Go

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7.1 REF Register (Address = 0h, 1h) [reset = 10100100b, 00000001b]

REF is shown in Figure 7-1 and Figure 7-2 described in Table 7-2.

Return to Summary Table.

REF sets the internal reference voltage of the TPS55285. The 01h register is the high byte and the 00h register is the low byte. One LSB of register 00h stands for 0.5645mV of the internal reference voltage. The default register value is 00000001 10100100b of 282mV. When the register value is 00000000 00000000b, the reference voltage is 45mV. When the register value is 00000111 10000000b, the reference voltage is 1.129V. The output voltage of the TPS55285 also depends on the output feedback ratio, which is either set in register 04h or set by an external resistor divider.

When using internal output voltage feedbcak divider, the output voltage V_{OUT} is calculated by Equation 4

$$V_{OUT} = \frac{V_{REF}}{INTFB} \tag{4}$$

The REF register can be configured by an I^2C controller before setting the OE bit in register 06h. For 5V output voltage, set the REF register value to 00000001 10100100b. To set the internal reference voltage, write the register 00h first, then write the register 01h.

Figure 7-1. REF_LSB

7	6	5	4	3	2	1	0
VREF							
R/W-10100100b							

Figure 7-2. REF_MSB

15	14	13	12	11	10	9	8
Reserved					VREF		
R-00000b					R/W-001b		

Table 7-2. REF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	Reserved	R	00000b	Reserved
10-0	VREF	R/W	001 10100100b	Sets the internal reference voltage 000 00000000b = 45mV reference voltage 000 00000001b = 45.5645mV reference voltage 000 00000010b = 46.129mV reference voltage ...... = ... 001 10100100b = 282mV reference voltage (Default) ...... = ... 011 00110100b = 508mV reference voltage ...... = ... 101 10001100b = 846mV reference voltage ...... = ... 111 10000000b = 1129mV reference voltage ...... = ... 111 11111110b = 1200mV reference voltage

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7.2 IOUT_LIMIT Register (Address = 2h) [reset = 11100100b]

IOUT_LIMIT is shown in Figure 7-3 and described in Table 7-3.

Return to Summary Table.

IOUT_LIMIT sets the target output current limit from 500mA to 6.35A. One LSB stands for 50mA output current limit step. The bit7 enables the current limit or disables the current limit.

Figure 7-3. IOUT_LIMIT Register

7	6	5	4	3	2	1	0
Current_Limit_EN	Current_Limit_Setting						
R/W-1b	R/W-1100100b						

Table 7-3. IOUT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Current_Limit_EN	R/W	1b	Enable or disable output current limit. 0b = Output current limit disabled 1b = Output current limit enabled (Default)
6-0	Current_Limit_Setting	R/W	1100100b	Sets the output current limit target 0000000b = 500mA output current limit 0000001b = 500mA output current limit 0000010b = 500mA output current limit …... = …... 0001010b = 500mA output current limit 0001011b = 550mA output current limit 0001100b = 600mA output current limit 0001101b = 650mA output current limit …... = …... 0010100b = 1A output current limit …... = …... 0101000b = 2A output current limit …... = …... 0111100b = 3A output current limit …... = …... 1100100b = 5A output current limit (Default) …... = …... 1111111b =6.35A output current limit

7.3 VOUT_SR Register (Address = 3h) [reset = 00000001b]

VOUT_SR is shown in Figure 7-4 and described in Table 7-4.

Return to Summary Table.

Register 03h sets the slew rate of the output voltage change and the response delay time after the output current exceeds the setting output current limit.

The OCP_DELAY [1:0] bits set the response time of the TPS55285 when the output overcurrent limit is hit. This allows the TPS55285 to output high current in a relative short duration time. The default setting is 128µs so that the TPS55285 immediately limits the output current.

The SR [1:0] bits set 1.25mV/µs, 2.5mV/µs, 5mV/µs, and 10mV/µs slew rate for output voltage change.

Figure 7-4. VOUT_SR Register

7	6	5	4	3	2	1	0
RESERVED		OCP_DELAY		RESERVED		SR	
R-0b		R/W-00b		R-00b		R/W-01b	

Table 7-4. VOUT_SR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-4	OCP_DELAY	R/W	00b	Sets the response time of the device when the output overcurrent limit is reached. 00b = 128µs (Default) 01b = Delay 1.024 x 3ms 10b = Delay 1.024 x 6ms 11b = Delay 1.024 x 12ms
3-2	RESERVED	R	00b	Reserved
1-0	SR	R/W	01b	Sets slew rate for output voltage change. 00b = 1.25mV/µs output change slew rate 01b = 2.5mV/µs output change slew rate (Default) 10b = 5mV/µs output change slew rate 11b = 10mV/µs output change slew rate

7.4 VOUT_FS Register (Address = 4h) [reset = 00000011b]

VOUT_FS is shown in Figure 7-5 and described in Table 7-5.

Return to Summary Table.

Register 04h sets the selection for the output voltage feedback divider, either by an internal resistor divider or external resistor divider, and sets the internal feedback ratio when using internal feedback resistor divider.

Figure 7-5. VOUT_FS Register

7	6	5	4	3	2	1	0
FB	FB_OVP	RESERVED				INTFB	
R/W-0b	R/W-0b	R-0000b				R/W-11b	

Table 7-5. VOUT_FS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FB	R/W	0b	Output voltage feedback divider 0b = Use internal output voltage feedback. The FB/$\overline{INT}$ pin is the indicator for output short circuit protection, overcurrent status, and overvoltage status (Default). 1b = Use external output voltage feedback. The FB/$\overline{INT}$ pin is the feedback input of the output voltage.
6	FB_OVP	R/W	0b	0b = Enable FB 115% OVP (Default) 1b = Disable FB 115% OVP
5-2	RESERVED	R	0000b	Reserved
1-0	INTFB	R/W	11b	Internal feedback ratio 00b = Set internal feedback ratio to 0.2256 01b = Set internal feedback ratio to 0.1128 10b = Set internal feedback ratio to 0.0752 11b = Set internal feedback ratio to 0.0564(Default)

Table 7-6. Output Voltage vs Internal Reference

INTFB1	INTFB0	REF=0000h	REF=001Ah	REF=0050h	REF=00F0h	REF=0780h	Output Voltage Step
0	0				0.8V	5V	2.5mV
0	1			0.8V		10V	5mV
1	0		0.8V			15V	7.5mV
1	1	0.8V				20V	10mV

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7.5 CDC Register (Address = 5h) [reset = 11110000b]

CDC is shown in Figure 7-6 and described in Table 7-7.

Return to Summary Table.

Register 05h sets masks for SC bit, OCP bit, OVP bit and TSD bit in register 07h. When the mask bit is set and corresponding fault happens, the device will mask the fault indication on FB/$\overline{INT}$ pin

In addition, register 05h sets the voltage rise added to the setting output voltage with respect to the sensed output current.

Figure 7-6. CDC Register

7	6	5	4	3	2	1	0
SC_MASK	OCP_MASK	OVP_MASK	TSD_MASK	CDC_OPTION	CDC		
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-0b	R/W-000b		

Table 7-7. CDC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SC_MASK	R/W	1b	Short circuit mask 0b = Disabled SC indication 1b = Enable SC indication (Default)
6	OCP_MASK	R/W	1b	Over current mask 0b = Disabled OCP indication 1b = Enable OCP indication (Default)
5	OVP_MASK	R/W	1b	Over voltage mask 0b = Disabled OVP indication 1b = Enable OVP indication (Default)
4	TSD_MASK	R/W	1b	Thermal shutdown mask 0b = Disabled TSD indication 1b = Enable TSD indication (Default)
3	CDC_OPTION	R/W	0b	Disable or enable cable voltage drop compensation function 0b = Disable CDC compensation (Default) 1b = Enable CDC compensation
2-0	CDC	R/W	000b	Compensation for voltage drop over the cable 000b = 0V output voltage rise with 5A output current (Default) 001b = 0.1V output voltage rise with 5A output current 010b = 0.2V output voltage rise with 5A output current 011b = 0.3V output voltage rise with 5A output current 100b = 0.4V output voltage rise with 5A output current 101b = 0.5V output voltage rise with 5A output current 110b = 0.6V output voltage rise with 5A output current 111b = 0.7V output voltage rise with 5A output current

7.6 MODE Register (Address = 6h) [reset = 00100000b]

MODE is shown in Figure 7-7 and described in Table 7-8.

Return to Summary Table.

MODE controls the operating mode of the TPS55285.

DISCHG_2 bit controls the discharge FET enabled or disabled when Vout steps down. When DISCHG_2 is set to 1, the discharge FET current helps reducing the reverse current in FPWM mode when Vout steps down.

Figure 7-7. MODE Register

7	6	5	4	3	2	1	0
OE	SPREAD SPECTRUM	HICCUP	DISCHG	FSW		FPWM	DISCHG_2
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-00b		R/W-0b	R/W-0b

Table 7-8. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0b	Output enable 0b = Output disabled (Default) 1b = Output enable
6	SPREADSPECTRUM	R/W	0b	Spread spectrum function 0b = Disable spread spectrum function (Default) 1b = Enable spread spectrum function
5	HICCUP	R/W	1b	Hiccup mode 0b = Disable the hiccup during output short circuit protection. 1b = Enable the hiccup during output short circuit protection (Default)
4	DISCHG	R/W	0b	Output discharge 0b = Disabled VOUT discharge when the device is in shutdown mode (Default) 1b = Enable VOUT discharge. VOUT is discharged to ground by an internal 100mA current sink in shutdown mode
3-2	FSW	R/W	00b	Switching frequency 00b = 400kHz (Default) 01b = 800kHz 11b = 1.6MHz 11b = 2.2MHz
1	FPWM	R/W	0b	Select operating mode at light load condition 0b = PFM operating mode at light load condition (Default) 1b = FPWM operating mode at light load condition
0	DISCHG_2	R/W	0b	0b = Output discharge function is enabled when VREF voltage decreases. (Default) 1b = Output discharge function is disabled when VREF voltage decreases.

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7.7 STATUS Register (Address = 7h) [reset = 00000001b]

STATUS is shown in Figure 7-8 and described in Table 7-9.

Return to Summary Table.

The STATUS register stores the operating status of the TPS55285. When any of the SCP bit, the OCP bit, the OVP bit or the TSD bit are set, and the corresponding mask bit in register 05h is set as well, the FB/$\overline{INT}$ pin outputs low logic level to indicate the situation. Reading register 07h clears the SCP bit, OCP bit, OVP bit and TSD bit. The FB/$\overline{INT}$ pin status and SCP bit, OCP bit, OVP bit or TSD bit are reset until the register 07h is read. If the fault situation still exists, the corresponding bit and FB/$\overline{INT}$ pin is set again.

Figure 7-8. STATUS Register

7	6	5	4	3	2	1	0
SCP	OCP	OVP	TSD	Reserved	Reserved	STATUS	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-11b	

Table 7-9. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SCP	R	0b	Short circuit protection 0b = No short circuit 1b = Short circuit happens. Does not reset until it is read.
6	OCP	R	0b	Overcurrent protection 0b = No output overcurrent 1b = Output current hits the current limit. Does not reset until it is read.
5	OVP	R	0b	Overvoltage protection 0b = No OVP 1b = Output voltage exceeds the OVP threshold. Does not reset until it is read.
4	TSD	R	0b	Thermal shutdown protection 0b = No TSD 1b = Thermal shutdown happens. Does not reset until it is read
3	RESERVED	R	0b	Reserved
2	RESERVED	R	0b	Reserved
1-0	STATUS	R	01b	Operating status 00b = Boost 01b = Buck 10b = Buck-Boost 11b = Reserved

7.8 Register Summary

The Table 7-10 summarizes the default settings of the registers in the TPS55285.

Table 7-10. Default Settings of Registers

Register Address	Register Name	R/W	Default Values
00h	VREF_LSB	R/W	10100100
01h	VREF_MSB	R/W	00000001
02h	IOUT_LIMIT	R/W	11100100
03h	VOUT_SR	R/W	00000001
04h	VOUT_FS	R/W	00000011
05h	CDC	R/W	11110000
06h	MODE	R/W	00100000
07h	STATUS	R	00000001

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS55285 can operate over a wide range of 2.4V to 22V input voltage and output 0.8V to 22V. It can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPS55285 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS55285 operates in one-cycle buck and one-cycle boost mode alternately. To reduce the switching power loss in high power conditions, it is recommended to set the switching frequency below 500kHz. If a system requires higher switching frequency above 500kHz, it is recommended to operate at lower switch current for better thermal performance.

8.2 Typical Application

The TPS55285 provides a small size solution for USB PD power supply application with the input voltage ranging from 5V to 22V.

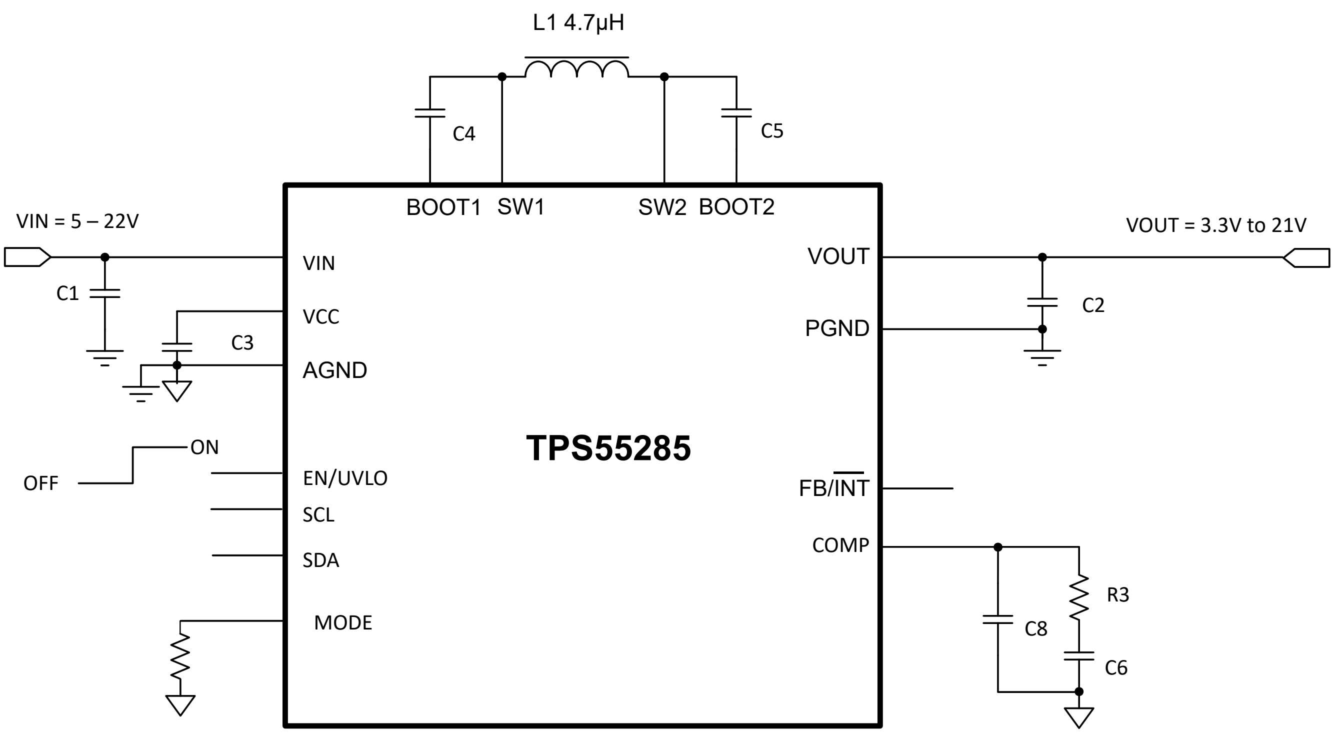

Figure 8-1. USB PD Power Supply With 5V to 22V Input Voltage

8.2.1 Design Requirements

The design parameters are listed in Table 8-1:

Table 8-1. Design Parameters

PARAMETERS	VALUES
Input voltage	5V to 22V
Output voltage	3.3V to 21V
Output current limit	3A
Output voltage ripple	±50mV
Operating mode at light load	FPWM

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

The switching frequency of the TPS55285 is set by FSW bit in 06H register. To reduce the switching power loss with such a high current application, 400kHz switching frequency is selected for this application.

8.2.2.2 Output Voltage Setting

The TPS55285 has I^2C interface to set the internal reference voltage. A microcontroller can easily set the desired output voltage by writing the proper data into the reference voltage registers through I^2C bus.

8.2.2.3 Inductor Selection

Since the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications: inductance, saturation current, and DC resistance.

The TPS55285 is designed to work with inductor values between 1µH and 10µH. The inductor selection is based on consideration of both buck and boost modes of operation.

The inner current loop uses internal compensationand requires the inductor value must be larger than 1.2/fSW.

For buck mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum input voltage. In CCM, Equation 5 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \times V_{OUT}}{\Delta I_{L(P-P)} \times f_{SW} \times V_{IN(MAX)}} \tag{5}$$

where

- $V_{IN(MAX)}$ is the maximum input voltage
- V_{OUT} is the output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when VOUT equals half of the maximum input voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For boost mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum output voltage. In CCM, Equation 6 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{V_{IN} \times \left(V_{OUT(MAX)} - V_{IN}\right)}{\Delta I_{L(P-P)} \times f_{SW} \times V_{OUT(MAX)}} \tag{6}$$

where

- V_{IN} is the input voltage
- $V_{OUT(MAX)}$ is the maximum output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when V_{IN} equals to the half of the maximum output voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For this application example, a 4.7µH inductor is selected, which produces approximate maximum inductor current ripple of 50% of the highest average inductor current in buck mode and 50% of the highest average inductor current in boost mode.

In buck mode, the inductor DC current equals to the output current. In boost mode, the inductor DC current can be calculated with Equation 7.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (7)$$

where

- V_{OUT} is the output voltage
- I_{OUT} is the output current
- V_{IN} is the input voltage
- η is the power conversion efficiency

For a given maximum output current of the buck-boost converter TPS55285, the maximum inductor DC current happens at the minimum input voltage and maximum output voltage. Set the inductor current limit of the TPS55285 higher than the calculated maximum inductor DC current to make sure the TPS55285 has the desired output current capability.

In boost mode, the inductor ripple current is calculated with Equation 8.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}} \quad (8)$$

where

- $\Delta I_{L(P-P)}$ is the inductor ripple current
- L is the inductor value
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the inductor peak current is calculated with Equation 9.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (9)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI, but in the same way, load transient response time is increased. The selected inductor must have higher saturation current than the calculated peak current.

The conversion efficiency is dependent on the resistance of its current path. The switching loss associated with the switching MOSFETs, and the inductor core loss. Therefore, the overall efficiency is affected by the inductor DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. Table 8-2 lists recommended inductors for the TPS55285. In this application example, the Coilcraft inductor XAL7070-472 is selected for its small size, high saturation current, and small DCR.

Table 8-2. Recommended Inductors

PART NUMBER	L (µH)	DCR (MAXIMUM) (mΩ)	SATURATION CURRENT / HEAT RATING CURRENT (A)	SIZE (L x W x H mm)	VENDOR[(1)]
XAL7070-472ME	4.7	14.3	15.2/10.5	7.5 × 7.2 × 7.0	Coilcraft
VCHA085D-4R7MS6	4.7	15.6	16.0/8.8	8.7 × 8.2 × 5.2	Cyntec
IHLP4040DZER4R7M01	4.7	16.5	17/9.5	10.2 × 10.2 × 4.0	Vishay

(1) See the *Third-party Products* disclaimer.

8.2.2.4 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitors is given by Equation 10.

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} \quad (10)$$

where

- $I_{CIN(RMS)}$ is the RMS current through the input capacitor
- I_{OUT} is the output current

The maximum RMS current occurs at the output voltage is half of the input voltage, which gives $I_{CIN(RMS)} = I_{OUT}$ / 2. Ceramic capacitors are recommended for their low ESR and high ripple current capability. A total of 20µF effective capacitance is a good starting point for this application.

8.2.2.5 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by Equation 11, where the minimum input voltage and the maximum output voltage correspond to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (11)$$

where

- $I_{COUT(RMS)}$ is the RMS current through the output capacitor
- I_{OUT} is the output current

In this example, the maximum output ripple RMS current is 2.8A.

The ESR of the output capacitor causes an output voltage ripple given by Equation 12 in boost mode.

$$V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times R_{COUT} \quad (12)$$

where

- R_{COUT} is the ESR of the output capacitance

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The capacitance also causes a capacitive output voltage ripple given by Equation 13 in boost mode. When input voltage reaches the minimum value and the output voltage reaches the maximum value, there is the largest output voltage ripple caused by the capacitance.

$$V_{RIPPLE(CAP)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \quad (13)$$

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple. From the required output voltage ripple, use Equation 12 and Equation 13 to calculate the minimum required effective capacitance of the C_{OUT}.

8.2.2.6 Output Current Limit

The output current limit is set through register 02h with 50mA step. The maximum value of the output current limit is 6.35A and minimum value of the output current limit is 500mA. The default limit voltage is 5A.

8.2.2.7 Loop Stability

The TPS55285 uses average current control scheme. The inner current loop uses internal compensation and requires the inductor value must be larger than $1.2/f_{SW}$. The outer voltage loop requires an external compensation. The COMP pin is the output of the internal voltage error amplifier. An external compensation network comprised of resistor and ceramic capacitors is connected to the COMP pin.

The TPS55285 operates in buck mode or boost mode. Therefore, both buck and boost operating modes require loop compensations. The restrictive one of both compensations is selected as the overall compensation from a loop stability point of view. Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to the presence of a right half plane zero (RHPZ).

The power stage in boost mode can be modeled by Equation 14.

$$G_{PS}(s) = \frac{R_{LOAD} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{s}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2\pi \times f_P}} \quad (14)$$

where

- R_{LOAD} is the output load resistance
- D is the switching duty cycle in boost mode
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.055Ω

The power stage has two zeros and one pole generated by the output capacitor and load resistance. Use Equation 15 to Equation 17 to calculate them.

$$f_P = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}} \quad (15)$$

$$f_{ESRZ} = \frac{1}{2\pi \times R_{COUT} \times C_{OUT}} \quad (16)$$

$$f_{RHPZ} = \frac{R_{LOAD} \times (1-D)^2}{2\pi \times L} \quad (17)$$

The internal transconductance amplifier together with the compensation network at the COMP pin constitutes the control portion of the loop. The transfer function of the control portion is shown by Equation 18.

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$$G_C(s) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{s}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{COMP2}}\right)} \quad (18)$$

where

- G_{EA} is the transconductance of the error amplifier
- R_{EA} is the output resistance of the error amplifier
- V_{REF} is the reference voltage input to the error amplifier
- V_{OUT} is the output voltage
- f_{COMP1} and f_{COMP2} are the pole's frequency of the compensation network
- f_{COMZ} is the zero's frequency of the compensation network

The total open-loop gain is the product of $G_{PS}(s)$ and $G_C(s)$. The next step is to choose the loop crossover frequency, f_C, at which the total open-loop gain is 1, namely 0dB. The higher in frequency that the loop gain stays above 0dB before crossing over, the faster the loop response. It is generally accepted that the loop gain cross over 0dB at the frequency no higher than the lower of either 1/10 of the switching frequency, f_{SW} or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then, set the value of R_C, C_C, and C_P by Equation 19 to Equation 21.

$$R_C = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times C_{OUT} \times f_C}{(1-D) \times V_{REF} \times G_{EA}} \quad (19)$$

where

- f_C is the selected crossover frequency

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{2 \times R_C} \quad (20)$$

$$C_P = \frac{R_{COUT} \times C_{OUT}}{R_C} \quad (21)$$

If the calculated C_P is less than 10pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10dB gain margin eliminates output voltage ringing during the line and load transient.

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8.2.3 Application Curves

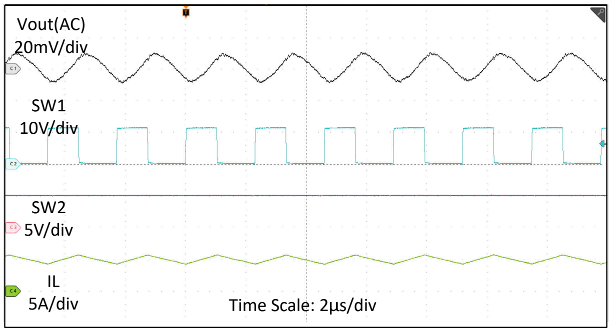

Figure 8-2. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 5V, I_O = 5A, FPWM

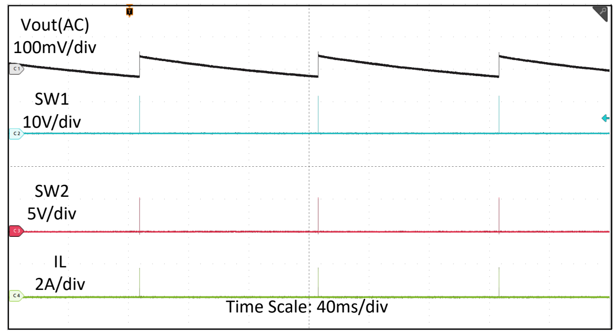

Figure 8-3. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 5V, I_O = 0A, PFM

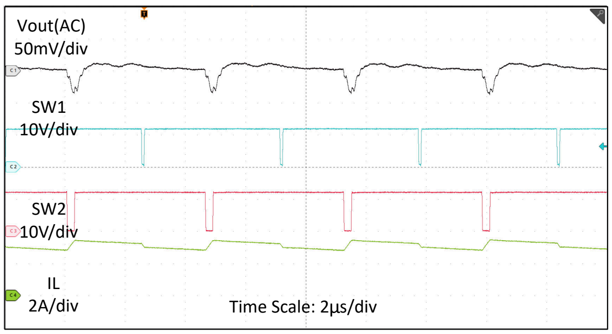

Figure 8-4. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 12V, I_O = 3A, FPWM

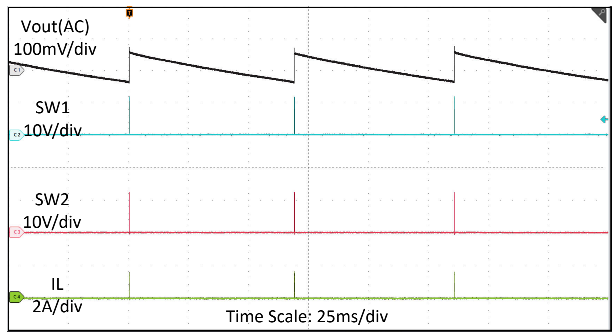

Figure 8-5. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 12V, I_O = 0A, PFM

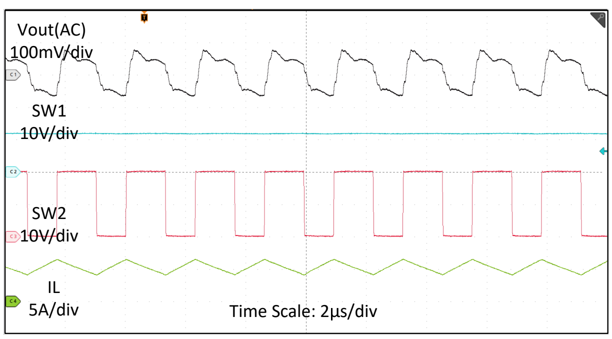

Figure 8-6. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 20V, I_O = 2A, FPWM

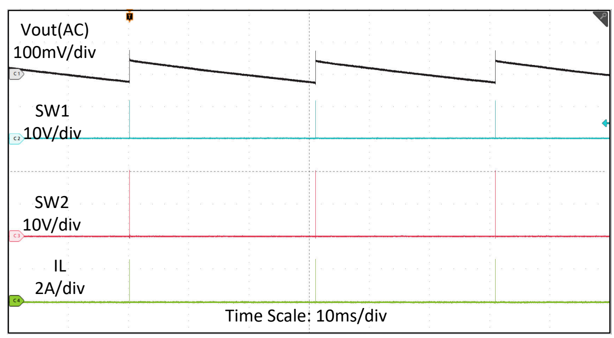

Figure 8-7. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 20V, I_O = 0A, PFM

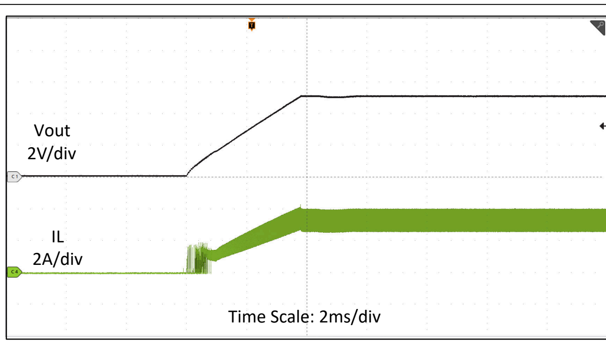

Figure 8-8. Start-up Waveforms in V_{IN} = 12V, V_{OUT} = 5V, R_{LOAD} = 1.5Ω, FPWM

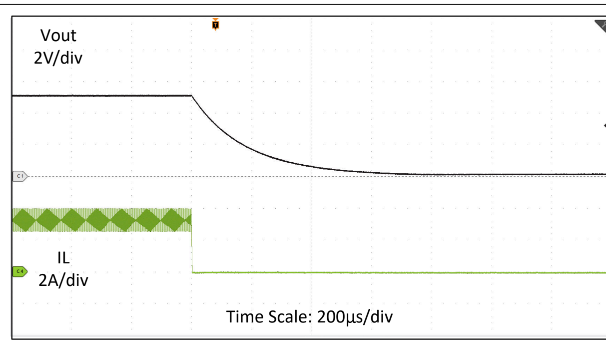

Figure 8-9. Shutdown Waveforms in V_{IN} = 12V, V_{OUT} = 5V, R_{LOAD} = 1.5Ω, FPWM

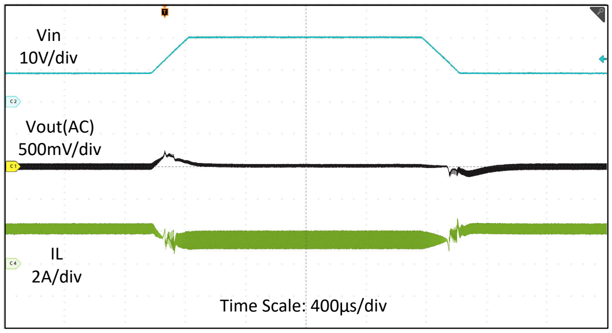

Figure 8-10. Line Transient Waveforms in V_{IN} = 9V to 20V, V_{OUT} = 12V, I_O = 3A with 200µs Slew Rate, FPWM

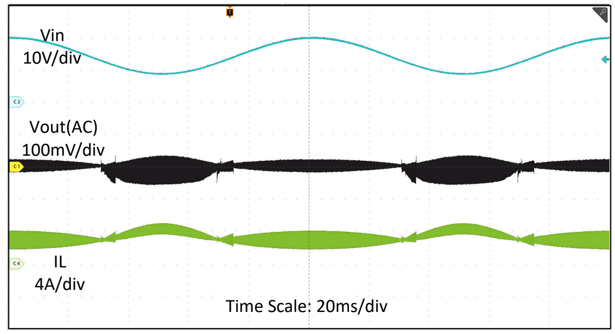

Figure 8-11. Line Sweep Waveforms in V_{IN} = 9V to 20V, V_{OUT} = 12V, I_O = 3A , FPWM

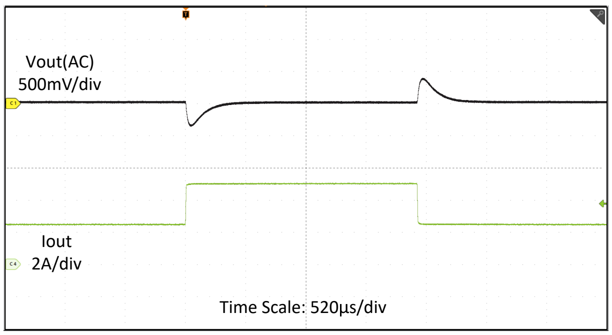

Figure 8-12. Load Transient Waveforms in V_{IN} = 12V, V_{OUT} = 5V, I_O = 2.5A to 5A with 2.5A/µs Slew Rate, FPWM

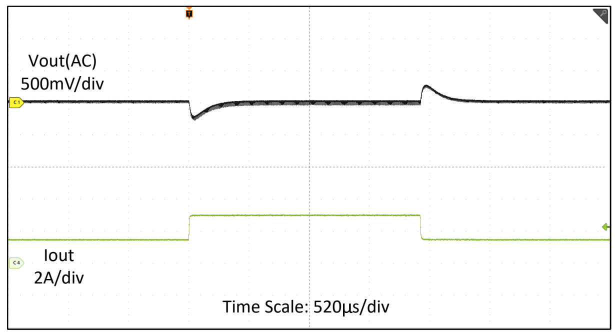

Figure 8-13. Load Transient Waveforms in V_{IN} = 12V, V_{OUT} = 12V, I_O = 1.5A to 3A with 2.5A/µs Slew Rate, FPWM

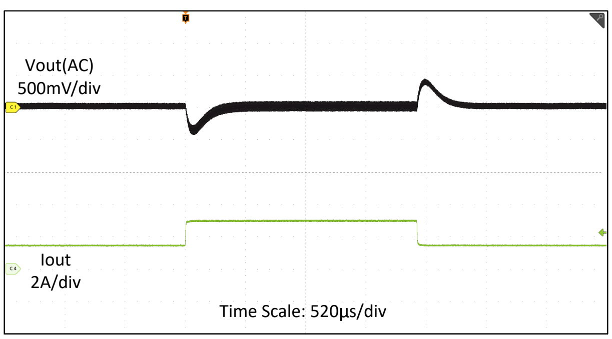

Figure 8-14. Load Transient Waveforms in V_{IN} = 12V, V_{OUT} = 20V, I_O = 1.5A to 3A with 2.5A/µs Slew Rate, FPWM

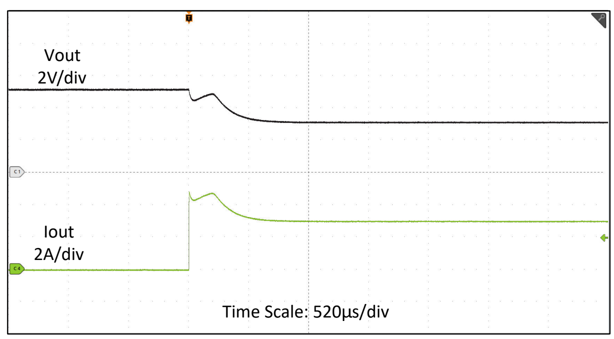

Figure 8-15. 3A Output Current Limit Waveforms in V_{IN} = 12V, V_{OUT} = 5V, R_{LOAD} = 1Ω

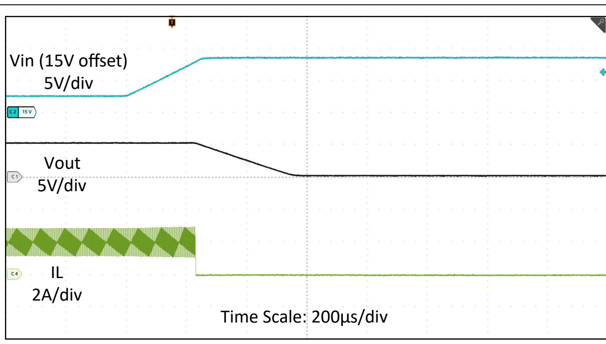

Figure 8-16. VIN OVP Waveforms in V_{IN} = 18V to 24V, V_{OUT} = 5V, I_{OUT} = 2A

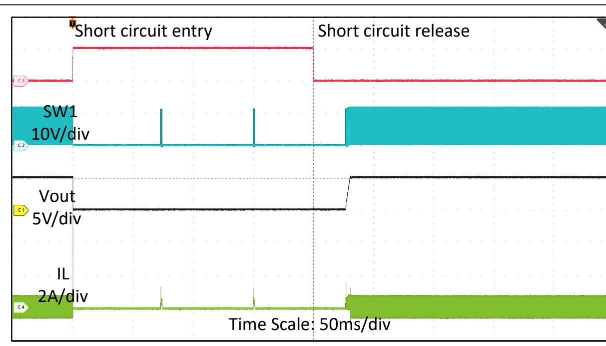

Figure 8-17. Short Circuit Protection in V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0.1A

ADVANCE INFORMATION

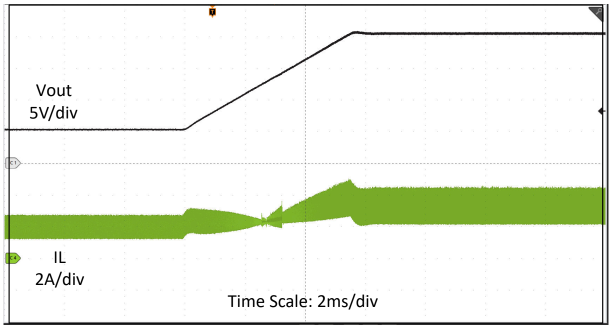

Figure 8-18. Vout Change Rising in V_{IN} = 12V, V_{OUT} = 5V to 20V with 2.5mV/µS, I_{OUT} = 2A, FPWM

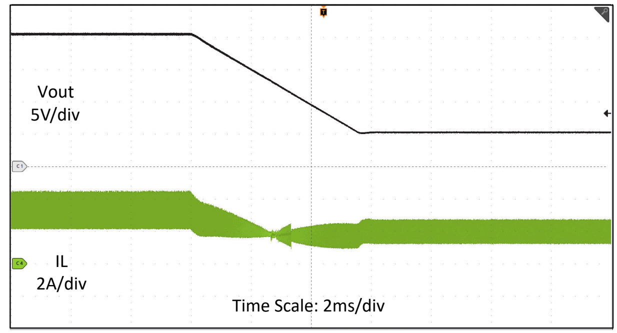

Figure 8-19. Vout Change Falling in V_{IN} = 12V, V_{OUT} = 20V to 5V with 2.5mV/µS, I_{OUT} = 2A, FPWM

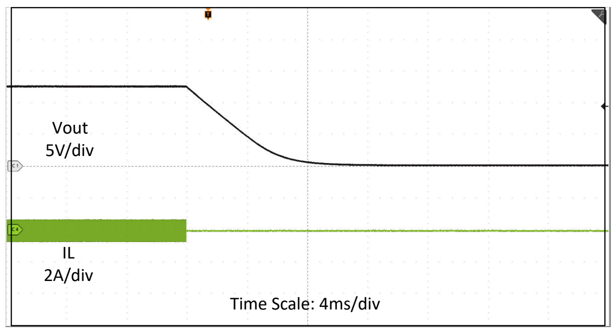

Figure 8-20. Output Discharge in V_{IN} = 12V, V_{OUT} = 5, I_{OUT} = 0A

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3.0V to 22V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an aluminum electrolytic capacitor with a value of 100µF.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems.

1. Place the 0.1-µF small package (0402) ceramic capacitors close to the VIN/VOUT pins to minimize high frequency current loops. This improves the radiation of high-frequency noise (EMI) and efficiency.
2. Use multiple GND vias near PGND pin to connect the PGND to the internal ground plane. This also improves thermal performance.
3. Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes. Use a ground plane under the switching regulator to minimize interplane coupling.
4. Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins. Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 and SW2 pins.
5. Place the VCC capacitor close to the IC with wide and short trace. The GND terminal of the VCC capacitor should be directly connected with PGND plane through three to four vias.
6. Isolate the power ground from the analog ground. The PGND plane and AGND plane are connected at the terminal of the VCC capacitor. Thus the noise caused by the MOSFET driver and parasitic inductance does not interface with the AGND and internal control circuit.
7. Place the compensation components as close to the COMP pin as possible. Keep the compensation components, feedback components, and other sensitive analog circuitry far away from the power components, switching nodes SW1 and SW2, and high-current trace to prevent noise coupling into the analog signals.
8. To improve thermal performance, it is recommended to use thermal vias close to the VIN pin to a large VIN area, and the VOUT pin to a large VOUT area separately.

ADVANCE INFORMATION

8.4.2 Layout Example

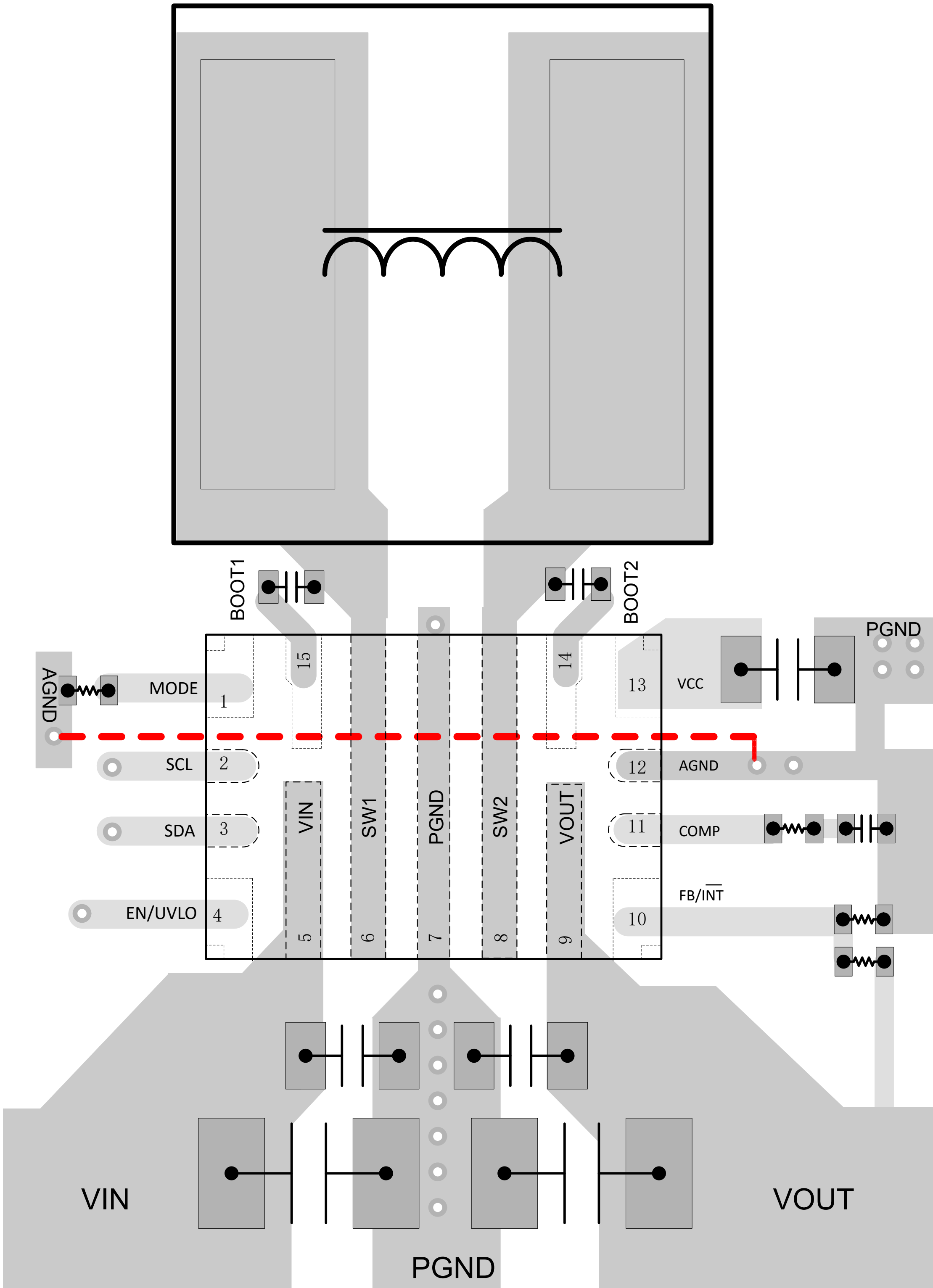

Figure 8-21. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.1.2 Development Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

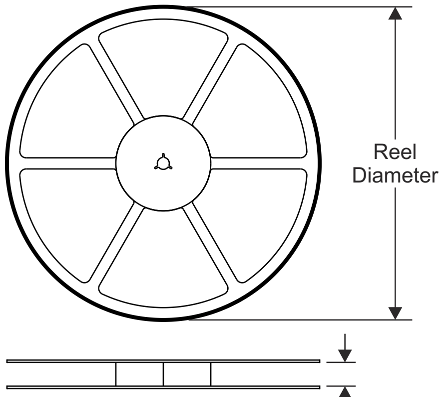
DATE	REVISION	NOTES
April 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

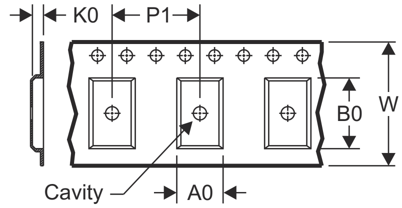
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

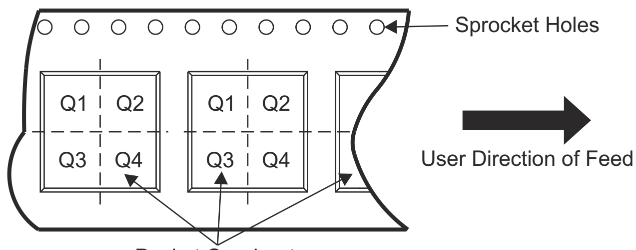


TAPE DIMENSIONS



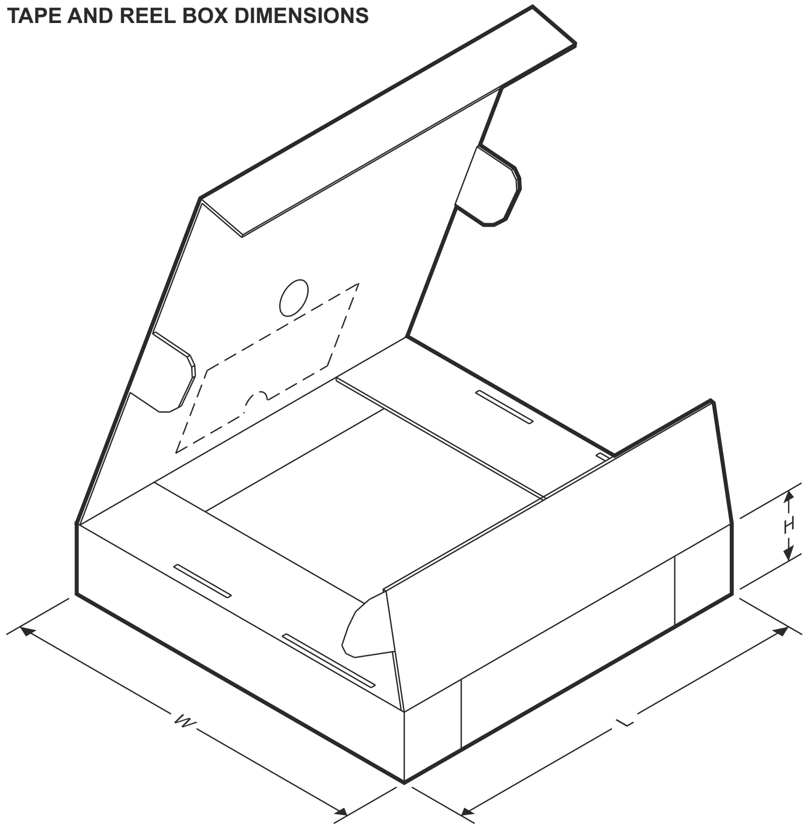
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55285VALR	WQFN-HR	VAL	15	3000	180	12.4	2.8	3.8	1.2	4	12	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55285VALR	WQFN-HR	VAL	15	3000	210.0	185.0	35.0

ADVANCE INFORMATION

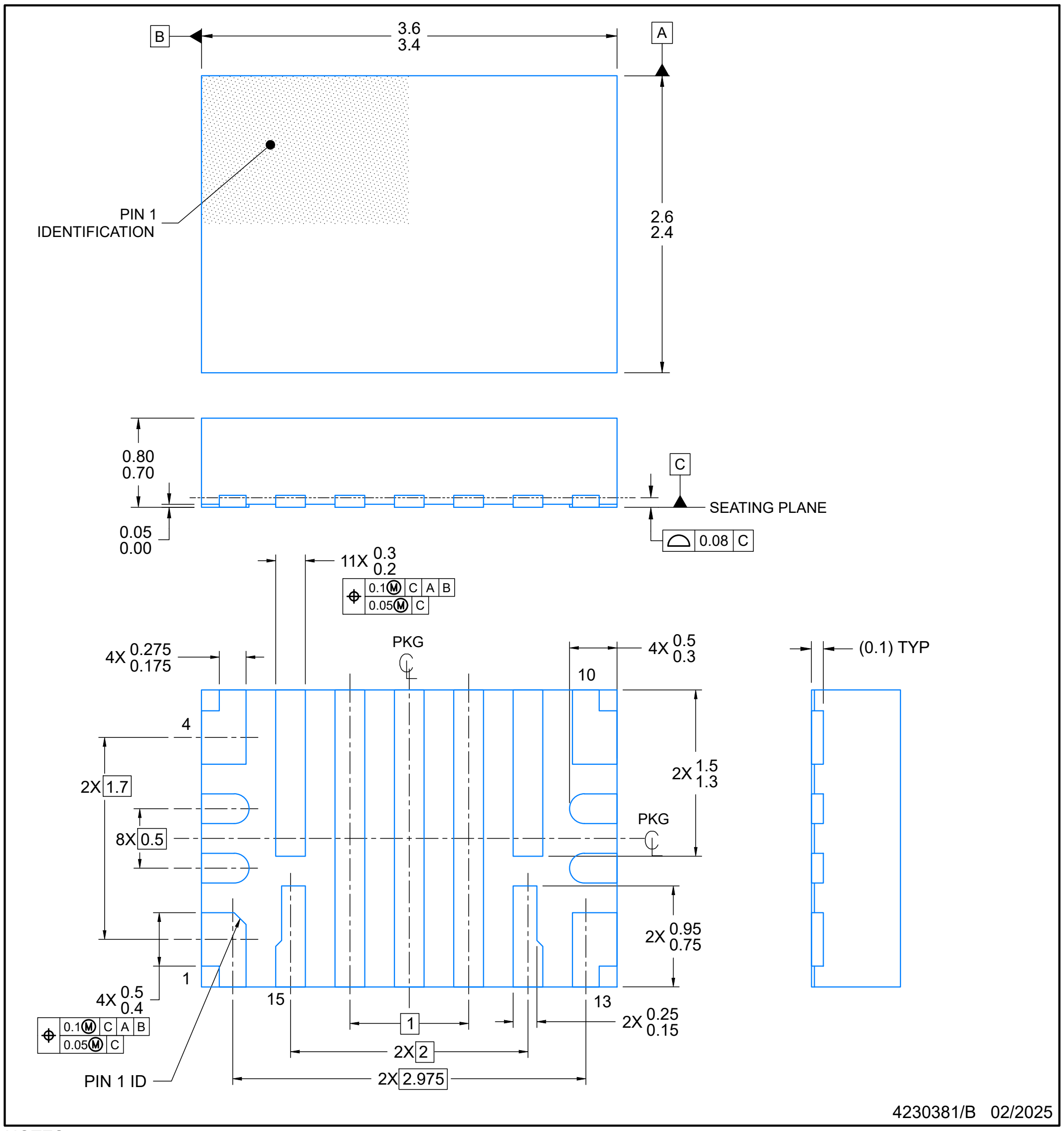
ADVANCE INFORMATION

PACKAGE OUTLINE

VAL0015A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

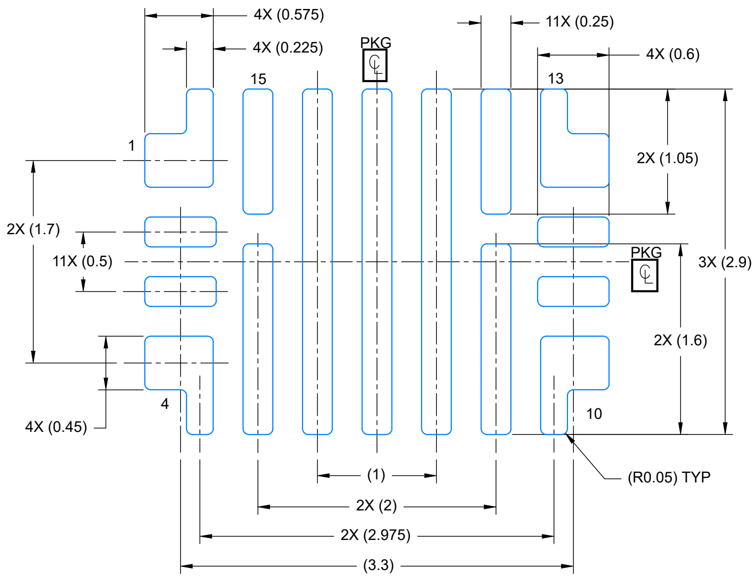
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

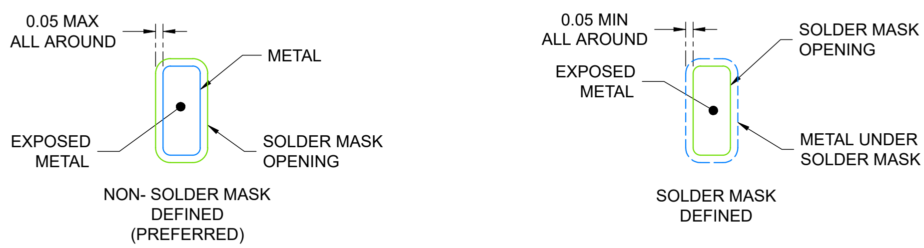
VAL0015A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS
NOT TO SCALE

4230381/B 02/2025

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

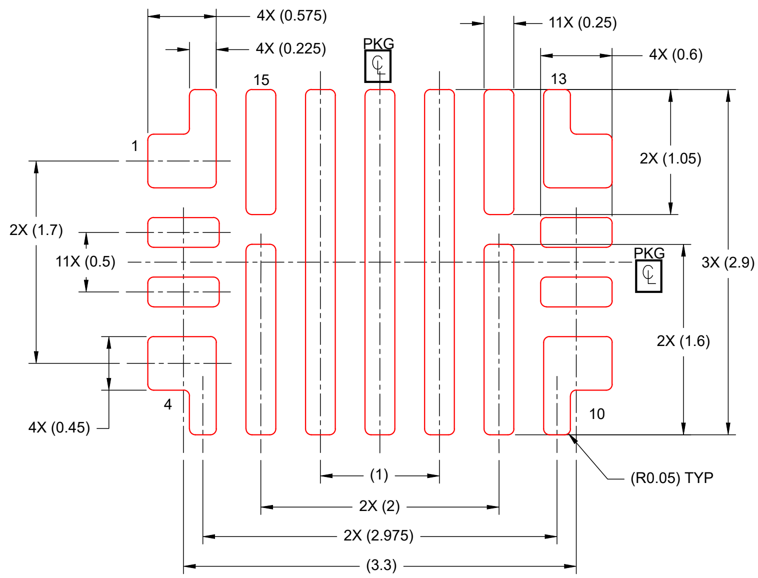
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

VAL0015A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

4230381/B 02/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XTPS55285VALR	Active	Preproduction	WQFN-HR (VAL) | 15	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XTPS55285VALR.A	Active	Preproduction	WQFN-HR (VAL) | 15	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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