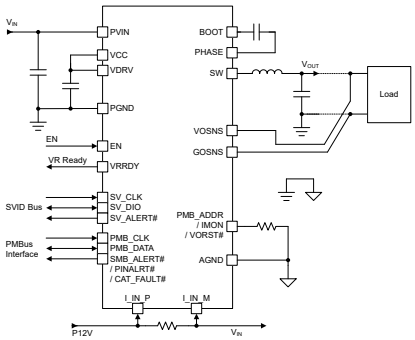
TPS544C27 4V to 18V Input, 35A, Buck Converter With SVID and PMBus®

1 Features

- Single chip power supply for SVID rails
- Intel® VR14 and VR13 compliant
- VR14.Cloud compliant with telemetry level 2 and security level 2
- PMBus® 1.5 interface with NVM for configuration, telemetry (V/I/T) and fault reporting
- Input voltage: 4V to 18V
- Output voltage: 0.25V to 5.5V
- Supports external 5V bias improving efficiency and enabling 2.7V minimum input voltage
- Output current: 35A continuous and 40A peak
- Cycle-by-cycle valley I_{OUT} OCF limit programmable up to 40A
- Input power monitoring (PIN sense)
- Programmable DCM or FCCM operation
- Switching frequency: 400kHz to 2MHz
- Programmable internal loop compensation including droop (DC Load Line)
- Programmable soft-start time from 0.5ms to 16ms
- Programmable soft-stop time from 0.5ms to 4ms
- Programmable output voltage slew rate: 0.625mV/µs to 25mV/µs
- Programmable V_{IN} UVLO, V_{OUT} OVF/UVF, and OTF
- Safe start-up into prebiased outputs
- Precision voltage reference and differential remote sense for high output accuracy
  - ±0.5% tolerance from 0°C to 85°C junction
  - ±1% tolerance from –40°C to 125°C junction
- Analog output current output pin (IMON)
- D-CAP+™ control topology with fast transient response
- Open-drain power-good output (VRRDY)



Simplified Schematic

2 Applications

- Server and cloud-computing POLs
- Hardware accelerator
- Network interface card
- Broadband, networking, and optical
- Wireless infrastructure

3 Description

The TPS544C27 device is highly integrated buck converter with D-CAP+ control topology for fast transient response. All programmable parameters can be configured by the PMBus interface and stored in non-volatile memory (NVM) as the new default values to minimize the external component count. These features make the device well-designed for space-constrained applications.

The TPS544C27 device is designed to work with Intel CPUs and fits well for single-phase, low-to-mid current SVID rails in the Intel server and SoC platforms requiring VR13, VR14, or VR14.Cloud compliance.

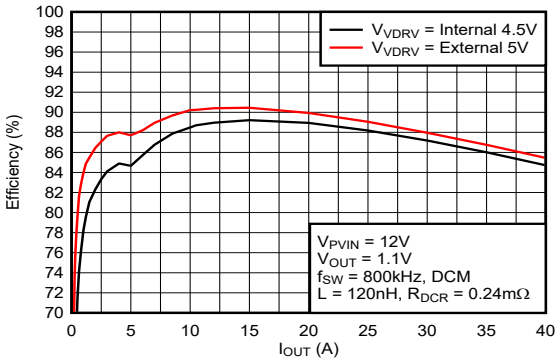
Fault management and status reports for the overcurrent fault (OCF), V_{OUT} overvoltage fault (OVF), undervoltage fault (UVF), and overtemperature fault are provided on the device. The TPS544C27 device provides a full set of telemetry, including output voltage, output current, and device temperature.

TPS544C27 is a lead-free device and is RoHS compliant without exemption.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS544C27	VBD (WQFN-FCRLF, 33)	5.00mm × 4.00mm

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Efficiency

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4 Pin Configuration and Functions

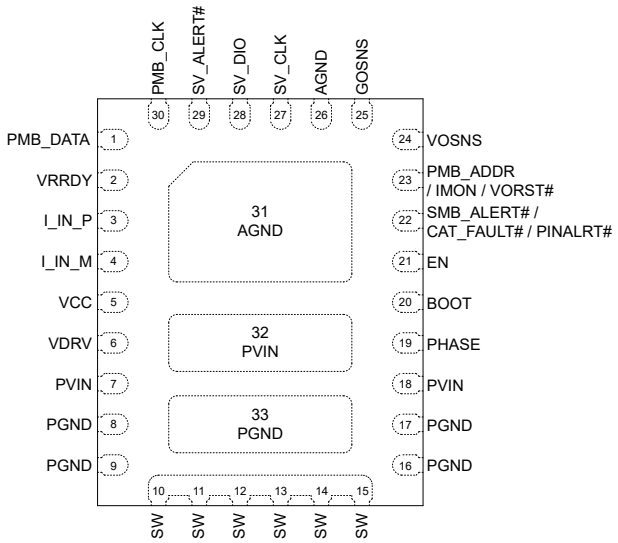

Figure 4-1. 33-Pin VBD, WQFN-FCRLF Package (Top View)

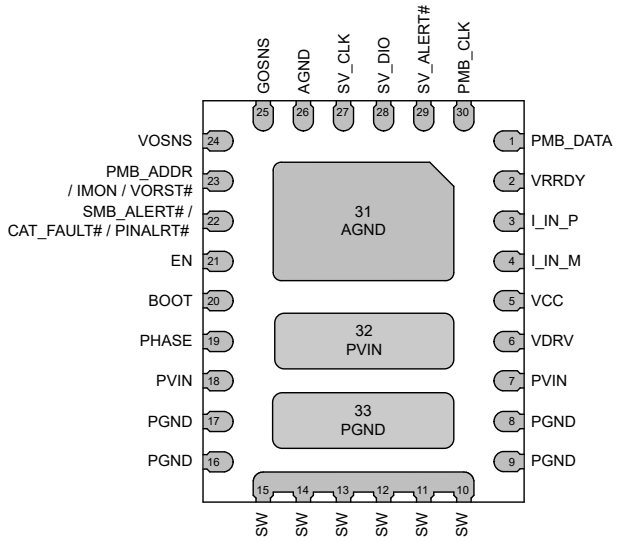

Figure 4-2. 33-Pin VBD, WQFN-FCRLF Package (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	26	G	Ground pin, reference point for internal control circuitry
AGND	31	G	Thermal pad internally tied to AGND. Connect this pad to board ground on PCB layout to enhance the thermal performance.
BOOT	20	P	Supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to the PHASE pin. A high temperature (X7R) 0.1µF or greater value ceramic capacitor is recommended.
EN	21	I	Enable pin, an active-high input pin that, when asserted high, causes the VR to begin soft-start sequence for the output voltage rail. When de-asserted low, the VR de-asserts VRRDY and begins the shutdown sequence of the output voltage rail and continue to completion.
GOSNS	25	I	Negative input of the differential remote sense circuit, connect to the ground sense point on the load side
I_IN_M	4	I	Negative input of the differential input current sense. Connect to PVIN side of input current sense resistor. If input current sense not used, connect directly to I_IN_P and PVIN.
I_IN_P	3	I	Positive Input of the differential input current sense. Connect to the input side of input current sense resistor. If input current sense not used, connect directly to I_IN_M and PVIN.
PGND	8-9, 16-17	G	Power ground for the internal power stage
PGND	33	G	Thermal pad internally tied to PGND. Connect this pad to board ground on PCB layout to enhance the thermal performance.
PHASE	19	O	Return for high-side MOSFET driver. Shorted to SW internally. Connect the BOOT pin bypass capacitor to this pin.
PMB_ADDR / IMON / VORST#	23	I/O	Multi-purpose pin. During the device initialization, the PMBus address of the controller is set by tying an external resistor between this pin and AGND. For proper resistor detection, do not load this pin with more than 20pF during the device initialization at VCC power-up. DC_LL, VBOOT, and OFFSET source 0 or 1 are selected as well. After device initialization, this pin can be used as an analog current monitor output. This pin is a current sense of low-side MOSFET. The analog IMON feature is enabled via the EN_AIMON bit. When using the IMON feature, do not load this pin with more than 50pF. This pin also performs a V_{OUT} reset function that can be enabled via the EN_VORST bit. If the EN_VORST bit is set, the analog IMON output is disabled.

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Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
PMB_CLK	30	I	PMBus serial clock pin
PMB_DATA	1	I/O	PMBus bi-directional serial data pin
PVIN	7, 18	P	Power input for both the power stage and the analog circuit. PVIN is the input of the internal VCC LDO.
PVIN	32	P	Pad internally tied to PVIN. Connect this pad to the power input voltage in the PCB layout and use vias to connect to internal layers to reduce AC and DC parasitics in the PCB layout.
SMB_ALERT# / CAT_FAULT# / PINALRT#	22	O	Multi-purpose open-drain pin. 1. SMB_ALERT# is PMBus serial active low alert line. 2. PINALRT# function (active low) 3. CAT_FAULT# active low Catastrophic Fault indicator. The functionality can be selected via the SEL_ALRT_FN field in the PMBus (D0h) SYS_CFG_USER1 command..
SV_ALERT#	29	O	SVID active low ALERT# signal. This output is asserted to indicate the status of the VR has changed.
SV_CLK	27	I	SVID clock pin
SV_DIO	28	I/O	SVID bi-directional data pin
SW	10-15	O	Output switching terminal of the power converter. Connect these pins to the output inductor.
VCC	5	I	5V bias for internal circuitry. Connect to VDRV or power from same external 5V bias. Bypass to AGND with minimum 1.0µF, 10V ceramic capacitor
VDRV	6	P	Internal LDO output and also input for gate driver circuit. An external 5V bias can be connected to this pin to save the power losses on the internal LDO.
VOSNS	24	I	Positive input of the differential remote sense circuit, connect to the Vout sense point on the load side
VRRDY	2	O	Voltage regulator “Ready” output signal. The VRRDY indicator is asserted when the controller is ready to accept SVID commands after EN is asserted. VRRDY is also be de-asserted low when a shutdown fault occurs. This open-drain output requires an external pullup resistor.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

ADVANCE INFORMATION

5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2024	*	Initial Release

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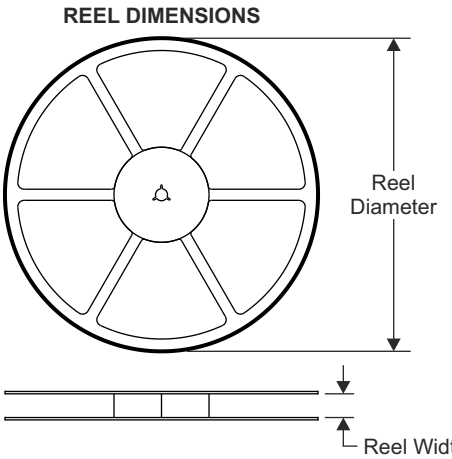
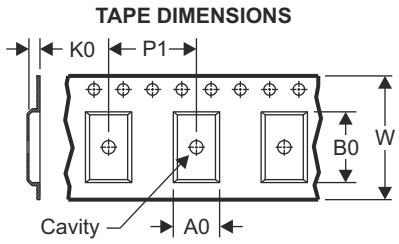
ADVANCE INFORMATION

7 Mechanical, Packaging, and Orderable Information

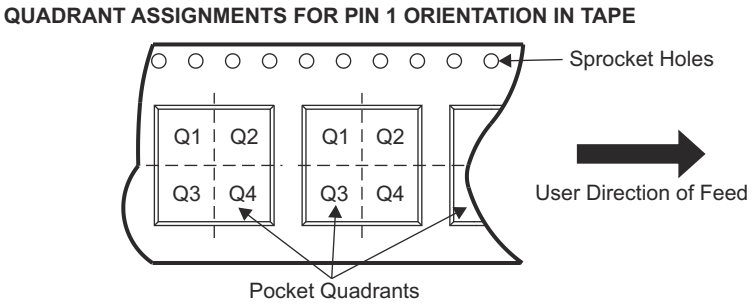
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information



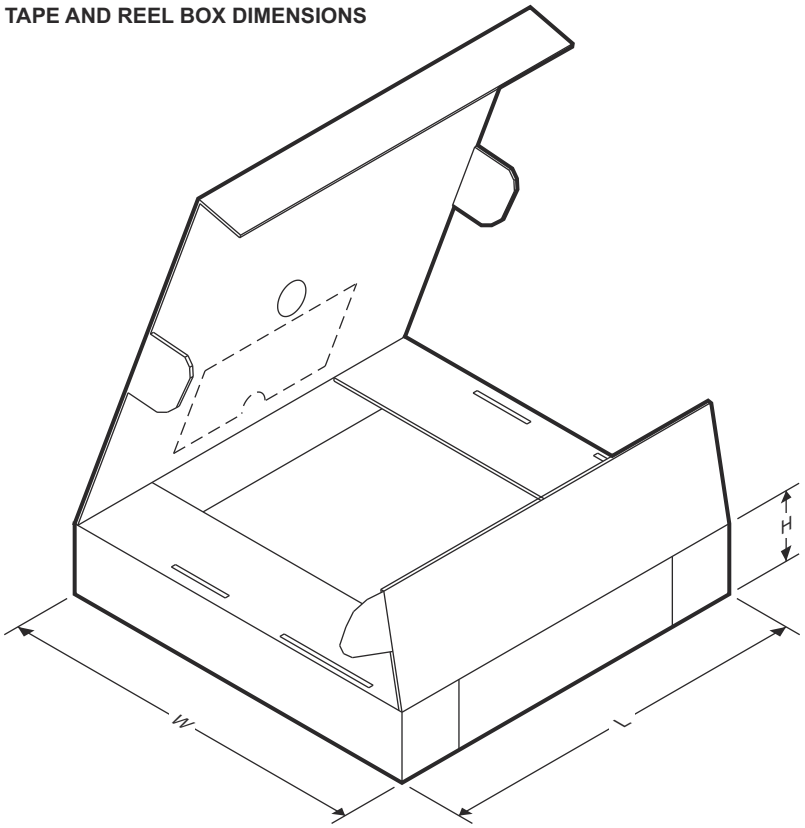


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS544C27VBDR	WQFN-FCRLF	VBD	33	3000	330	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS544C27VBDR	WQFN-FCRLF	VBD	33	3000	338	355	50

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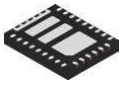
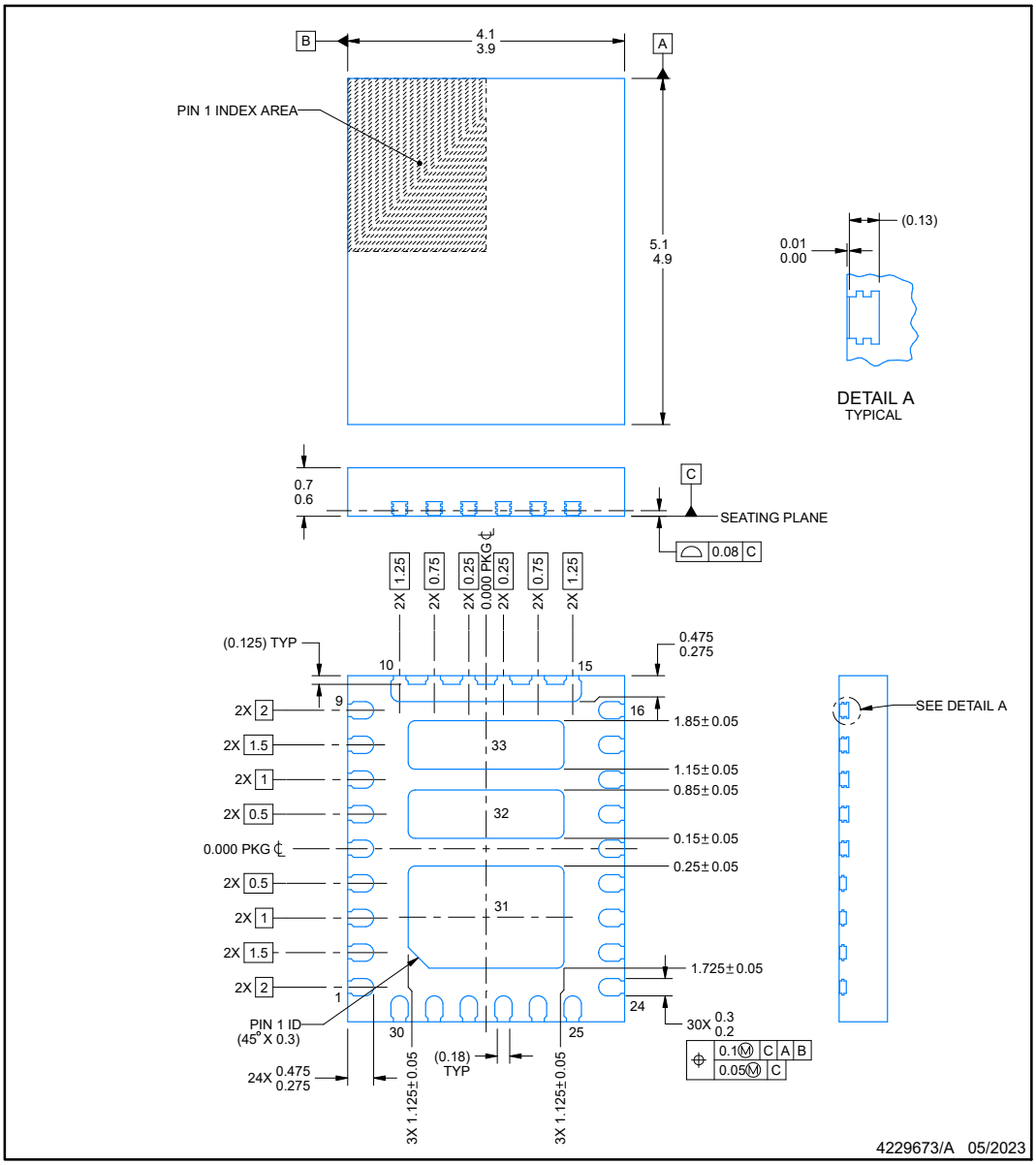
PACKAGE OUTLINE

VBD0033A



WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



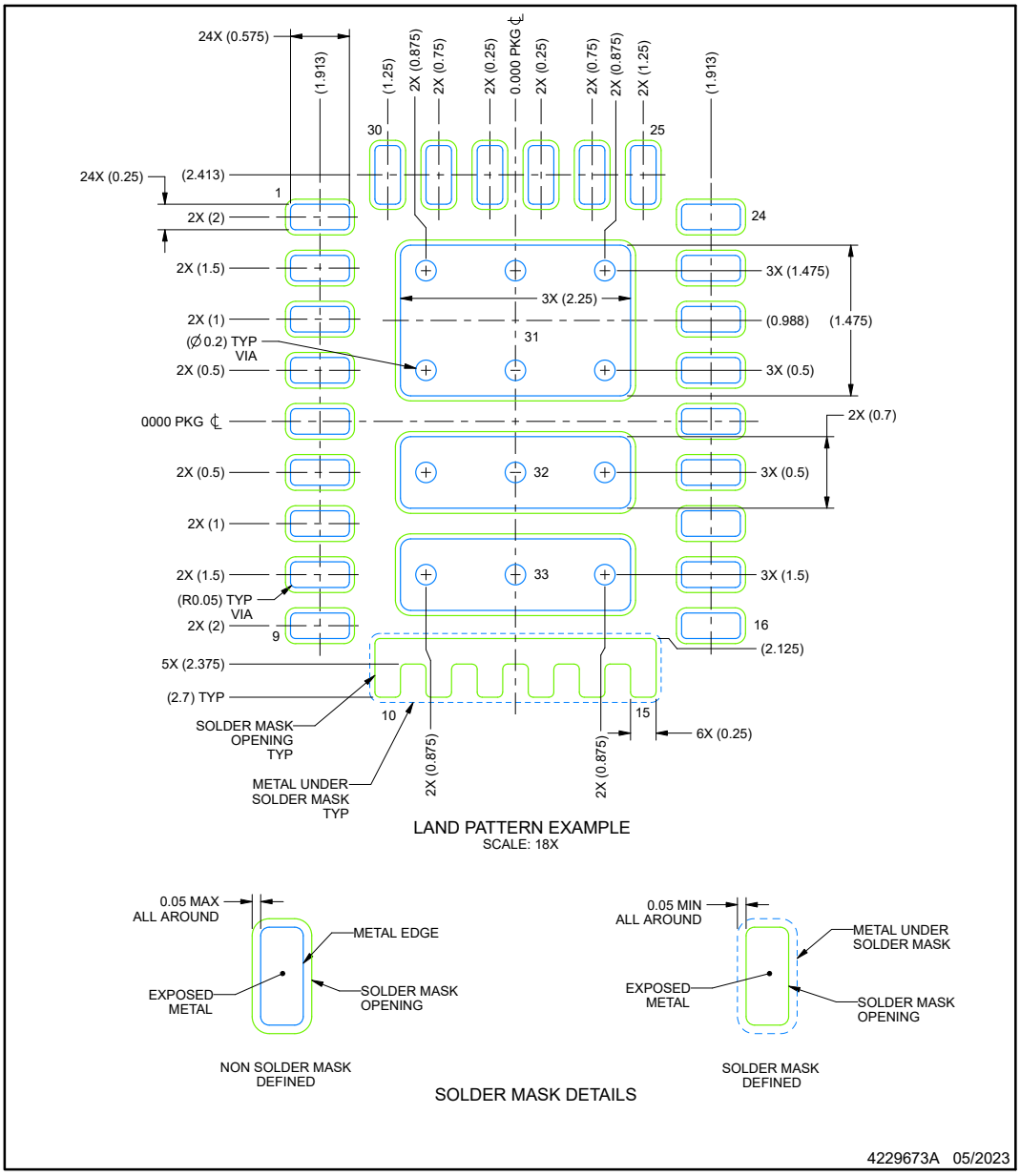
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VBD0033A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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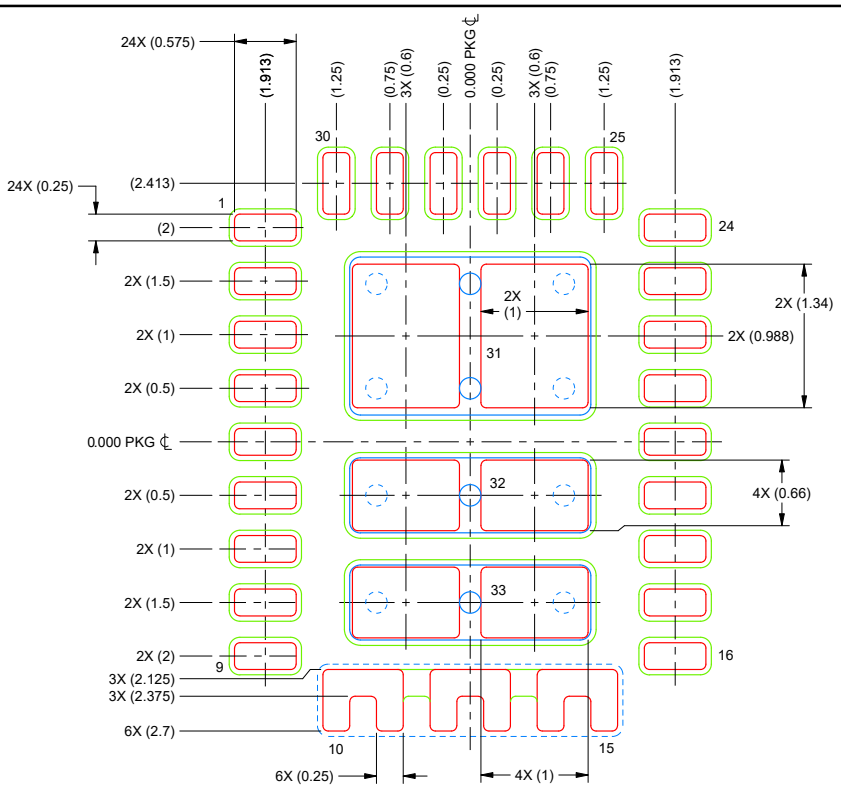
EXAMPLE STENCIL DESIGN

VBD0033A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 18X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD NUMBERED 10-15: 89%
PAD 31: 81%
PADS 32 & 33: 84%

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS544C27VBDR	Active	Preproduction	WQFN-FCRLF (VBD) | 33	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS544C27VBDR.A	Active	Preproduction	WQFN-FCRLF (VBD) | 33	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS544C27VBDR.B	Active	Preproduction	WQFN-FCRLF (VBD) | 33	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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