# TPS3760 High Voltage Supervisor with Programmable Sense and Reset Delay Function

## 1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Wide supply voltage range: 2.7 V to 65 V
- SENSE and RESET pins are 65 V graded
- Low quiescent current: 1 µA (typical)
- Flexible and wide voltage threshold options Table 12-1
  - 2.7 V to 36 V (1.5% maximum accuracy)
  - 800 mV option (1% maximum accuracy)
- Built-in hysteresis ($V_{HYS}$)
  - Percentage options: 2% to 13% (1% steps)
  - Fixed options: $V_{TH}$ < 8 V = 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V
- Programmable reset time delay
  - 10 nF = 12.8 ms, 10 µF = 12.8 s
- Programmable sense time delay
  - 10 nF = 1.28 ms, 10 µF = 1.28 s
- Manual Reset ($\overline{MR}$) feature
- Output reset latching feature
- Output topology: Open-Drain or Push-Pull

## 2 Applications

- Analog input module
- CPU (PLC controller)
- Servo drive control module
- Servo drive power stage module
- Servo drive functional safety module
- HVAL valve and actuator control

## 3 Description

The TPS3760 is a family of wide input range and low quiescent current window supervisors for fast detection of overvoltage (OV) or undervoltage (UV) conditions. The TPS3760 can be connected directly to and monitor 12 V / 24 V supply rails in a variety of industrial applications including factory automation, motor drives, building automation and others. Built-in hysteresis on the SENSE pins prevents false reset signals when monitoring a supply voltage rail.

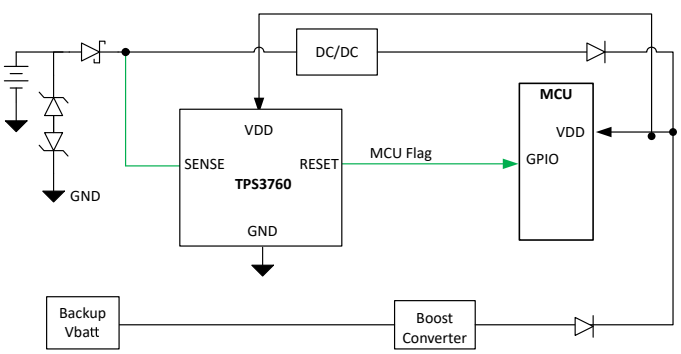
The separate VDD and SENSE pins allow redundancy sought by high-reliability systems. SENSE is decoupled from VDD and can monitor higher and lower voltages than VDD. Optional use of external resistors are supported by the high impedance input of the SENSE pins. CTSx and CTRx pins allow delay adjustability on the rising and falling edges of the RESET signals. Also, CTSx functions as a debouncer by ignoring voltage glitches on the monitored voltage rails; CTRx operates as a manual reset ($\overline{MR}$) that can be used to force a system reset.

The TPS3760 is available in a 4.1-mm×1.9-mm SOT 14-pin package. TPS3760 operates over –40°C to +125°C $T_A$.

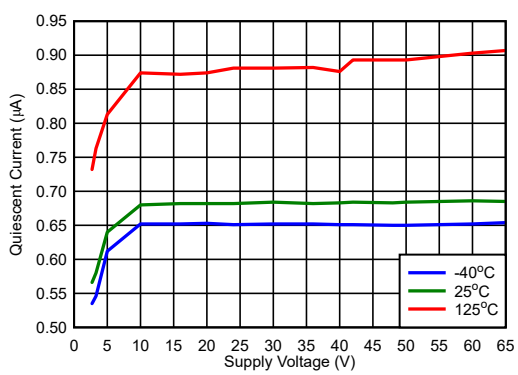
**Device Information**

| PART NUMBER | PACKAGE (1) | BODY SIZE (NOM) |
|---|---|---|
| TPS3760 | SOT-23 (14) (DYY) | 4.1 mm × 1.9 mm |

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.




**Typical Application Circuit**




**Typical $I_{DD}$ vs $V_{DD}$**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (March 2022) to Revision A (September 2023) | Page |
|---|---|
| • Added Latch nomenclature | 3 |
| • Removed DSK pinout description | 4 |
| • Added CTS and CTR timing plots | 13 |
| • Added Reset latch mode information | 26 |
| • Fixed nomenclature 08 to 01 | 35 |


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## 5 Device Comparison

**Voltage Threshold** **Hysteresis**

**TPS3760X X XX X DYY R**

**Topology**

| Suffix | CH1 |
|---|---|
| A | UV OD L |
| B | UV PP L |
| C | UV OD H |
| D | UV PP H |
| E | OV OD L |
| F | OV PP L |
| G | OV OD H |
| H | OV PP H |

**LATCH**

| Suffix | Name |
|---|---|
| L | LATCH |
| Blank | NO LATCH |

**Threshold Voltage**

| 100mV steps | | | | 400mV steps | | 500mV steps | | 1V steps | |
|---|---|---|---|---|---|---|---|---|---|
| Suffix | VIT | Suffix | VIT | Suffix | VIT | Suffix | VIT | Suffix | VIT |
| 01 | 800mV | 70 | 7.0V | A0 | 10.4V | D0 | 20.5V | F0 | 31.0V |
| 27 | 2.7V | 71 | 7.1V | A1 | 10.8V | D1 | 21.0V | F1 | 32.0V |
| 28 | 2.8V | 72 | 7.2V | A2 | 11.2V | D2 | 21.5V | F2 | 33.0V |
| 29 | 2.9V | 73 | 7.3V | A3 | 11.6V | D3 | 22.0V | F3 | 34.0V |
| 30 | 3.0V | 74 | 7.4V | A4 | 12.0V | D4 | 22.5V | F4 | 35.0V |
| 31 | 3.1V | 75 | 7.5V | A5 | 12.4V | D5 | 23.0V | F5 | 36.0V |
| 32 | 3.2V | 76 | 7.6V | A6 | 12.8V | D6 | 23.5V | | |
| 33 | 3.3V | 77 | 7.7V | A7 | 13.2V | D7 | 24.0V | | |
| 34 | 3.4V | 78 | 7.8V | A8 | 13.6V | D8 | 24.5V | | |
| 35 | 3.5V | 79 | 7.9V | A9 | 14.0V | D9 | 25.0V | | |
| 36 | 3.6V | 80 | 8.0V | B0 | 14.4V | E0 | 25.5V | | |
| 37 | 3.7V | 81 | 8.1V | B1 | 14.8V | E1 | 26.0V | | |
| 38 | 3.8V | 82 | 8.2V | B2 | 15.2V | E2 | 26.5V | | |
| 39 | 3.9V | 83 | 8.3V | B3 | 15.6V | E3 | 27.0V | | |
| 40 | 4.0V | 84 | 8.4V | B4 | 16.0V | E4 | 27.5V | | |
| 41 | 4.1V | 85 | 8.5V | B5 | 16.4V | E5 | 28.0V | | |
| 42 | 4.2V | 86 | 8.6V | B6 | 16.8V | E6 | 28.5V | | |
| 43 | 4.3V | 87 | 8.7V | B7 | 17.2V | E7 | 29.0V | | |
| 44 | 4.4V | 88 | 8.8V | B8 | 17.6V | E8 | 29.5V | | |
| 45 | 4.5V | 89 | 8.9V | B9 | 18.0V | E9 | 30.0V | | |
| 46 | 4.6V | 90 | 9.0V | C0 | 18.4V | | | | |
| 47 | 4.7V | 91 | 9.1V | C1 | 18.8V | | | | |
| 48 | 4.8V | 92 | 9.2V | C2 | 19.2V | | | | |
| 49 | 4.9V | 93 | 9.3V | C3 | 19.6V | | | | |
| 50 | 5.0V | 94 | 9.4V | C4 | 20.0V | | | | |
| 51 | 5.1V | 95 | 9.5V | | | | | | |
| 52 | 5.2V | 96 | 9.6V | | | | | | |
| 53 | 5.3V | 97 | 9.7V | | | | | | |
| 54 | 5.4V | 98 | 9.8V | | | | | | |
| 55 | 5.5V | 99 | 9.9V | | | | | | |
| 56 | 5.6V | 00 | 10.0V | | | | | | |
| 57 | 5.7V | | | | | | | | |
| 58 | 5.8V | | | | | | | | |
| 59 | 5.9V | | | | | | | | |
| 60 | 6.0V | | | | | | | | |
| 61 | 6.1V | | | | | | | | |
| 62 | 6.2V | | | | | | | | |
| 63 | 6.3V | | | | | | | | |
| 64 | 6.4V | | | | | | | | |
| 65 | 6.5V | | | | | | | | |
| 66 | 6.6V | | | | | | | | |
| 67 | 6.7V | | | | | | | | |
| 68 | 6.8V | | | | | | | | |
| 69 | 6.9V | | | | | | | | |

**Hysteresis**

| Suffix | CH1 |
|---|---|
| 2 | 2% |
| 3 | 3% |
| 4 | 4% |
| 5 | 5% |
| 6 | 6% |
| 7 | 7% |
| 8 | 8% |
| 9 | 9% |
| A | 10% |
| B | 11% |
| C | 12% |
| D | 13% |
| E | 0.5V |
| F | 1V |
| G | 1.5V |
| H | 2V |
| I | 2.5V |

**Package**

| Suffix | Name |
|---|---|
| DYY | SOT-23 |

**Reel**

| Suffix | Name |
|---|---|
| R | Large |

1. Sense logic: OV = overvoltage; UV = undervoltage
2. Reset topology: PP = Push-Pull; OD = Open-Drain
3. Reset logic: L = Active-Low; H = Active-High
4. A to I hysteresis options are only available for 2.9 V to 8V threshold options
5. Suffix 01 with VIT of 800mV corresponds to the adjustable variant, does not have internal voltage divider

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# 6 Pin Configuration and Functions

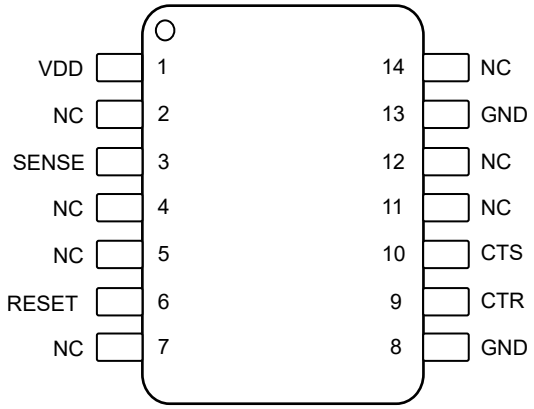


**Figure 6-1. DYY Package, 14-Pin SOT-23, TPS3760 (Top View)**

**Table 6-1. Pin Functions**

| PIN | SOT23 (DYY) | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VDD | 1 | I | **Input Supply Voltage:** Bypass with a 0.1 µF capacitor to GND. |
| SENSE | 3 | I | **Sense Voltage:** The voltage monitored by this pin is compared to the internal voltage threshold, $V_{th}$, that is determined by an internal voltage divider for fixed variants or an external voltage divider for adjustable variants. When the SENSE pin detects a fault, $\overline{\text{RESET}}$/RESET asserts after the sense time delay, set by CTS. When the voltage on the SENSE pin transitions back past $V_{th}$ and hysteresis, $V_{HYS}$, $\overline{\text{RESET}}$/RESET deasserts after the reset time delay, set by CTR. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance.<br>Sensing Topology: **Overvoltage (OV) or Undervoltage (UV)** |
| $\overline{\text{RESET}}$/RESET | 6 | O | **Output Reset Signal:** See Device Comparison for output topology options. $\overline{\text{RESET}}$/RESET asserts when SENSE crosses the voltage threshold after the sense time delay, set by CTS. $\overline{\text{RESET}}$/RESET remains asserted for the reset time delay period after SENSE transitions out of a fault condition. For active low open-drain reset output, an external pullup resistor is required. Do not place external pullup resistors on push-pull outputs.<br>Output topology: **Open Drain or Push Pull, Active Low or Active High** |
| CTS /$\overline{\text{LATCH}}$ | 10 | O | **SENSE Time Delay:** Capacitor programmable sense delay: CTS pin offers a user-adjustable sense delay time when asserting a reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$/RESET delay time to assert.<br>**$\overline{\text{LATCH}}$:** CTS functionality is disabled in latch capable devices. When latch mode is activated, $\overline{\text{RESET}}$/RESET will not de-assert even if the fault is cleared. To activate latch mode, the $\overline{\text{LATCH}}$ pin has to be driven low, to at least 1.4V. It is recommended to have a 10kΩ pull-down to ground. To deactivate latch mode, a 2.1V or greater for 3µs has to be applied to the $\overline{\text{LATCH}}$ pin while SENSE pin is not detecting a fault. $\overline{\text{RESET}}$/RESET will de-assert with delay $t_{ctr}$ starting on the rising edge of the deactivating signal. |
| CTR /$\overline{\text{MR}}$ | 9 | - | **RESET Time Delay:** User-programmable reset time delay for $\overline{\text{RESET}}$/RESET. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay.<br>**Manual Reset:** If this pin is driven low, the $\overline{\text{RESET}}$/RESET output will reset and become asserted. The pin can be left floating or be connected to a capacitor. This pin should not be driven high. |
| GND | 8, 13 | - | **Ground.** All GND pins must be electrically connected to the board ground. |


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**Table 6-1. Pin Functions (continued)**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | SOT23 (DYY) NO. | | |
| NC | 2, 4, 5, 7, 11,12, 14 | - | NC stands for “No Connect.” The pins are to be left floating. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted [1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | VDD, $V_{SENSE}$, $V_{RESET}$, $V_{\overline{RESET}}$ | –0.3 | 70 | V |
| Voltage | $V_{CTS}$, $V_{CTR}$ | –0.3 | 6 | V |
| Current | $I_{RESET}$, $I_{\overline{RESET}}$ | | 10 | mA |
| Temperature [2] | Operating junction temperature, $T_J$ | –40 | 150 | °C |
| Temperature [2] | Operating Ambient temperature, $T_A$ | –40 | 150 | °C |
| Temperature [2] | Storage, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-002 [1] | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101 [2] | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage | $V_{DD}$ | 2.7 | | 65 | V |
| Voltage | $V_{SENSE}$, $V_{RESET}$, $V_{\overline{RESET}}$ | 0 | | 65 | V |
| Voltage | $V_{CTS}$, $V_{CTR}$ | 0 | | 5.5 | V |
| Current | $I_{RESET}$, $I_{\overline{RESET}}$ | 0 | | ±5 | mA |
| $T_J$ | Junction temperature (free air temperature) | –40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC [1] | | TPS3760 DYY 14-PIN | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 131.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 61.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 56.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.


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## 7.5 Electrical Characteristics

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR/$\overline{MR}$ = CTS = open, output reset pull-up resistor $R_{PU}$ = 10 kΩ, voltage $V_{PU}$ = 5.5 V, and load $C_{LOAD}$ = 10 pF. The operating free-air temperature range $T_A$ = – 40°C to 125°C, unless otherwise noted. Typical values are at $T_A$ = 25°C and VDD = 16 V and $V_{IT}$ = 6.5 V ($V_{IT}$ refers to $V_{ITN}$ or $V_{ITP}$).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VDD** | | | | | | |
| $V_{DD}$ | Supply Voltage | | 2.7 | | 65 | V |
| UVLO [1] | Under Voltage Lockout | $V_{DD}$ Falling below $V_{DD\ (MIN)}$ | | | 2.7 | V |
| $V_{POR}$ | Power on Reset Voltage [2]<br>$\overline{RESET}$, Active Low<br>(Open-Drain, Push-Pull ) | $V_{OL(MAX)}$ = 300 mV<br>$I_{OUT\ (Sink)}$ = 15 µA | | | 1.4 | V |
| $V_{POR}$ | Power on Reset Voltage [2]<br>RESET, Active High<br>(Push-Pull ) | $V_{OH(MIN)}$ = 0.8 x $V_{DD}$<br>$I_{OUT\ (Source)}$ = 15 µA | | | 1.4 | V |
| $I_{DD}$ | Supply current into VDD pin | $V_{IT}$ = 800 mV<br>$V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$ | | 1 | 2.6 | µA |
| | | $V_{IT}$ = 2.7 V to 36 V<br>$V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$ | | 1 | 2 | µA |
| **SENSE (Input)** | | | | | | |
| $I_{SENSE}$ | Input current | $V_{IT}$ = 800 mV | | | 100 | nA |
| $I_{SENSE}$ | Input current | $V_{IT}$ < 10 V | | | 0.8 | µA |
| $I_{SENSE}$ | Input current | 10 V < $V_{IT}$ < 26 V | | | 1.2 | µA |
| $I_{SENSE}$ | Input current | $V_{IT}$ > 26 V | | | 2 | µA |
| $V_{ITN}$ | Input Threshold Negative (Undervoltage) | $V_{IT}$ = 2.7 V to 36 V | -1.5 | | 1.5 | % |
| | | $V_{IT}$ = 800 mV [3] | 0.792 | 0.800 | 0.808 | V |
| $V_{ITP}$ | Input Threshold Positive (Overvoltage) | $V_{IT}$ = 2.7 V to 36 V | -1.5 | | 1.5 | % |
| | | $V_{IT}$ = 800 mV [3] | 0.792 | 0.800 | 0.808 | V |
| $V_{HYS}$ | Hysteresis Accuracy [4] | $V_{IT}$ = 0.8 V and 2.7 V to 36 V<br>$V_{HYS}$ Range = 2% to 13%<br>(1% step) | -1.5 | | 1.5 | % |
| | | $V_{IT}$ = 2.7 V to 8 V<br>$V_{HYS}$ = 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V<br>($V_{ITP}$ - $V_{HYS}$) ≥ 2.4 V, OV Only | -1.5 | | 1.5 | % |
| **RESET (Output)** | | | | | | |
| $I_{lkg(OD)}$ | Open-Drain leakage | $V_{RESET}$ = 5.5 V<br>$V_{ITN}$ < $V_{SENSE}$ < $V_{ITP}$ | | | 300 | nA |
| | | $V_{RESET}$ = 65 V<br>$V_{ITN}$ < $V_{SENSE}$ < $V_{ITP}$ | | | 300 | nA |
| $V_{OL}$ [5] | Low level output voltage | 2.7 V ≤ VDD ≤ 65 V<br>$I_{RESET}$ = 5 mA | | | 300 | mV |
| $V_{OH_DO}$ | High level output voltage dropout<br>($V_{DD}$ - $V_{OH}$ = $V_{OH_DO}$)<br>(Push-Pull only) | 2.7 V ≤ VDD ≤ 65 V<br>$I_{RESET}$ = 500 uA | | | 100 | mV |
| $V_{OH}$ [5] | High level output voltage (Push-Pull only) | 2.7 V ≤ VDD ≤ 65 V<br>$I_{RESET}$ = 5 mA | 0.8$V_{DD}$ | | | V |

## 7.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR/$\overline{MR}$ = CTS = open, output reset pull-up resistor $R_{PU}$ = 10 kΩ, voltage $V_{PU}$ = 5.5 V, and load $C_{LOAD}$ = 10 pF. The operating free-air temperature range $T_A$ = – 40°C to 125°C, unless otherwise noted. Typical values are at $T_A$ = 25°C and VDD = 16 V and $V_{IT}$ = 6.5 V ($V_{IT}$ refers to $V_{ITN}$ or $V_{ITP}$).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Capacitor Timing (CTS, CTR)** | | | | | | |
| $R_{CTR}$ | Internal resistance (CTR / $\overline{MR}$) | | 877 | 1000 | 1147 | Kohms |
| $R_{CTS}$ | Internal resistance ($C_{TS}$) | | 88 | 100 | 122 | Kohms |
| **Manual Reset ($\overline{MR}$)** | | | | | | |
| $V_{\overline{MR}_IH}$ | CTR / $\overline{MR}$ pin logic high input | VDD = 2.7 V | 2200 | | | mV |
| $V_{\overline{MR}_IH}$ | CTR / $\overline{MR}$ pin logic high input | VDD = 65 V | 2500 | | | mV |
| $V_{\overline{MR}_IL}$ | CTR / $\overline{MR}$ pin logic low input | VDD = 2.7 V | | | 1300 | mV |
| $V_{\overline{MR}_IL}$ | CTR / $\overline{MR}$ pin logic low input | VDD = 65 V | | | 1300 | mV |

(1) When $V_{DD}$ voltage falls below UVLO, reset is asserted for Output. $V_{DD}$ slew rate ≤ 100 mV / µs
(2) $V_{POR}$ is the minimum $V_{DD}$ voltage for a controlled output state. Below VPOR, the output cannot be determined. $V_{DD}$ dv/dt ≤ 100mV/µs
(3) For adjustable voltage guidelines and resistor selection refer to **Adjustable Voltage Thresholds** in **Application and Implementation section**
(4) Hysteresis is with respect to $V_{ITP}$ and $V_{ITN}$ voltage threshold. $V_{ITP}$ has negative hysteresis and $V_{ITN}$ has positive hysteresis.
(5) For $V_{OH}$ and $V_{OL}$ relation to output variants refer to **Timing Figures after the Timing Requirement Table**


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## 7.6 Timing Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR/$\overline{MR}$ = CTS = open [(1)], output reset pull-up resistor $R_{PU}$ = 10 kΩ, voltage $V_{PU}$ = 5.5V, and $C_{LOAD}$ = 10 pF. VDD and SENSE slew rate = 1V / µs. The operating free-air temperature range $T_A$ = – 40°C to 125°C, unless otherwise noted. Typical values are at $T_A$ = 25°C and VDD = 16 V and $V_{IT}$ = 6.5 V ($V_{IT}$ refers to either $V_{ITN}$ or $V_{ITP}$).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Common timing parameters** | | | | | | |
| $t_{CTR}$ | Reset release time delay (CTR/$\overline{MR}$) [(2)] | VIT = 2.7 V to 36 V<br>$C_{CTR}$ = Open<br>20% Overdrive from Hysteresis | | | 100 | µs |
| | | VIT = 800 mV<br>$C_{CTR}$ = Open<br>20% Overdrive from Hysteresis | | | 40 | µs |
| $t_{CTS}$ | Sense detect time delay (CTS) [(3)] | VIT = 2.7 V to 36 V<br>$C_{CTS}$ = Open<br>20% Overdrive from $V_{IT}$ | | 34 | 90 | µs |
| | | VIT = 800 mV<br>$C_{CTS}$ = Open<br>20% Overdrive from $V_{IT}$ | | 8 | 17 | µs |
| $t_{SD}$ | Startup Delay [(4)] | $C_{CTR/\overline{MR}}$ = Open | | | 2 | ms |

(1) $C_{CTR}$ = Reset delay channel
$C_{CTS}$ = Sense delay channel

(2) **CTR Reset detect time delay:**
Overvoltage active-LOW output is measure from $V_{ITP\ -\ HYS}$ to $V_{OH}$
Undervoltage active-LOW output is measure from $V_{ITN\ +\ HYS}$ to $V_{OH}$
Overvoltage active-HIGH output is measure from $V_{ITP\ -\ HYS}$ to $V_{OL}$
Undervoltage active-HIGH output is measure from $V_{ITN\ +\ HYS}$ to $V_{OL}$

(3) **CTS Sense detect time delay:**
Active-low output is measure from $V_{IT}$ to $V_{OL}$ (or $V_{Pullup}$)
Active-high output is measured from $V_{IT}$ to $V_{OH}$
$V_{IT}$ refers to either $V_{ITN}$ or $V_{ITP}$

(4) During the power-on sequence, VDD must be at or above $V_{DD\ (MIN)}$ for at least $t_{SD}$ before the output is in the correct state based on $V_{SENSE}$.
$t_{SD}$ time includes the propagation delay ($C_{CTR}$ = Open). Capaicitor on $C_{CTR}$ will add time to $t_{SD}$.

## 7.7 Timing Diagrams

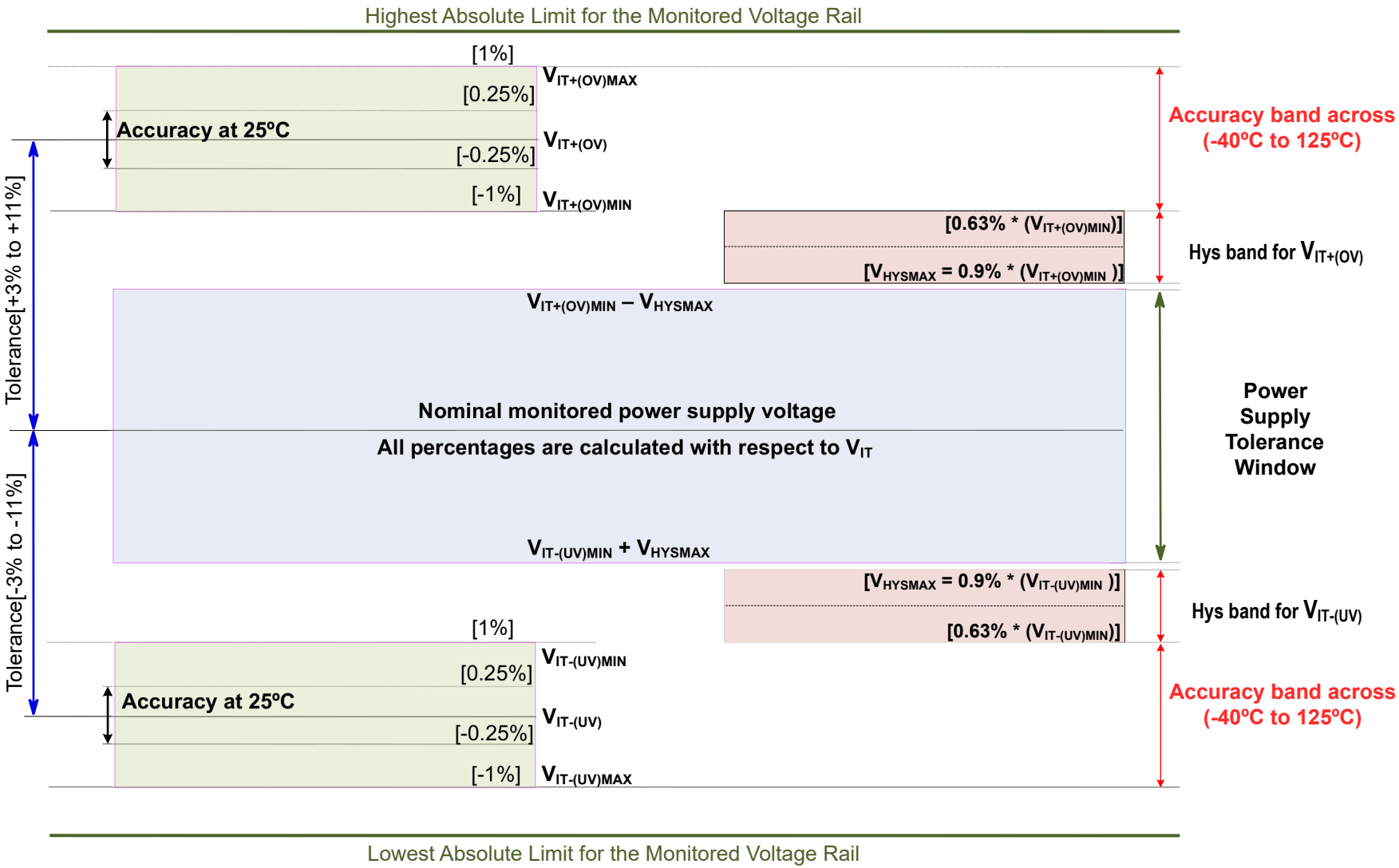


**Figure 7-1. Voltage Threshold and Hysteresis Accuracy**


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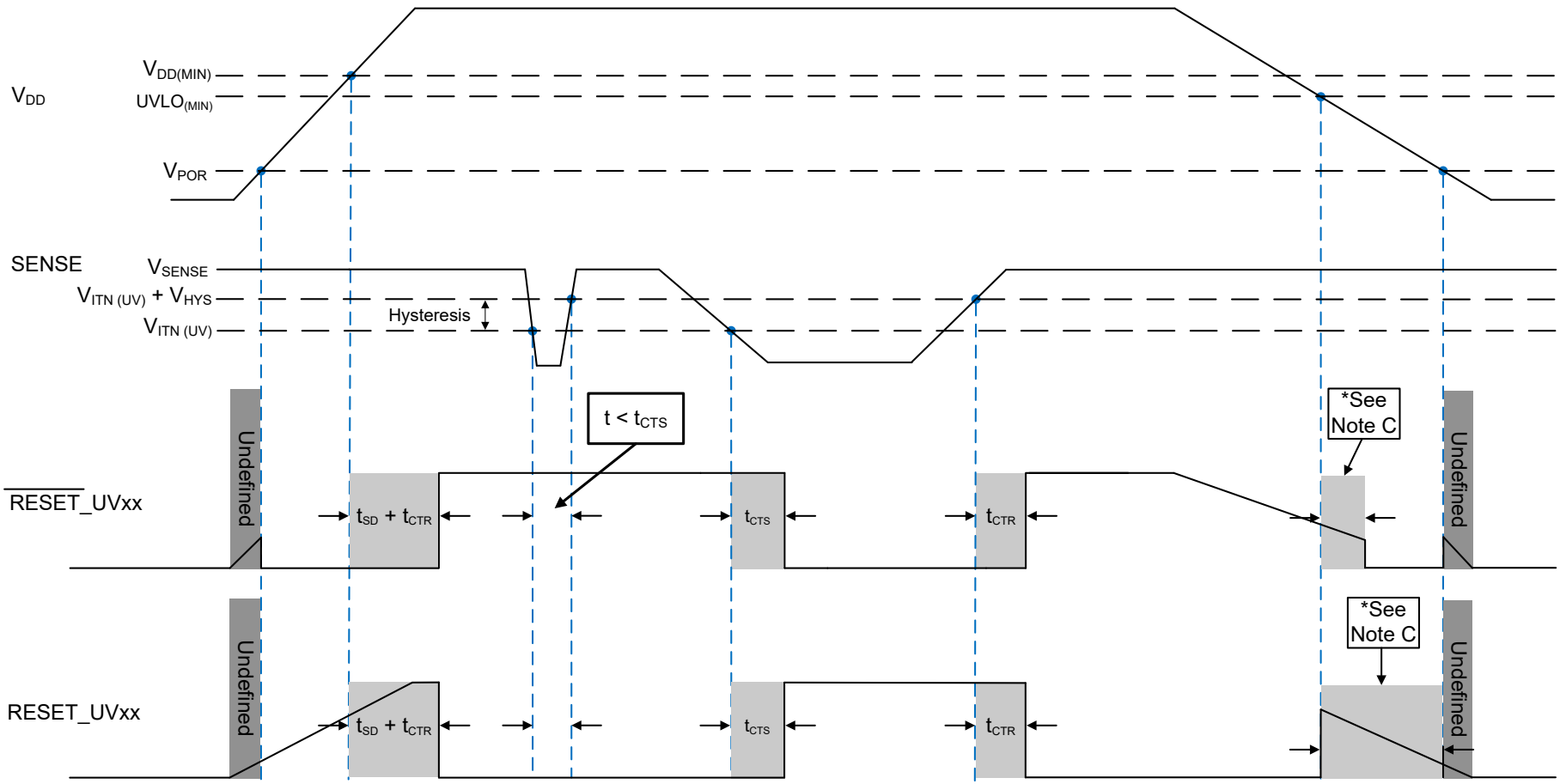
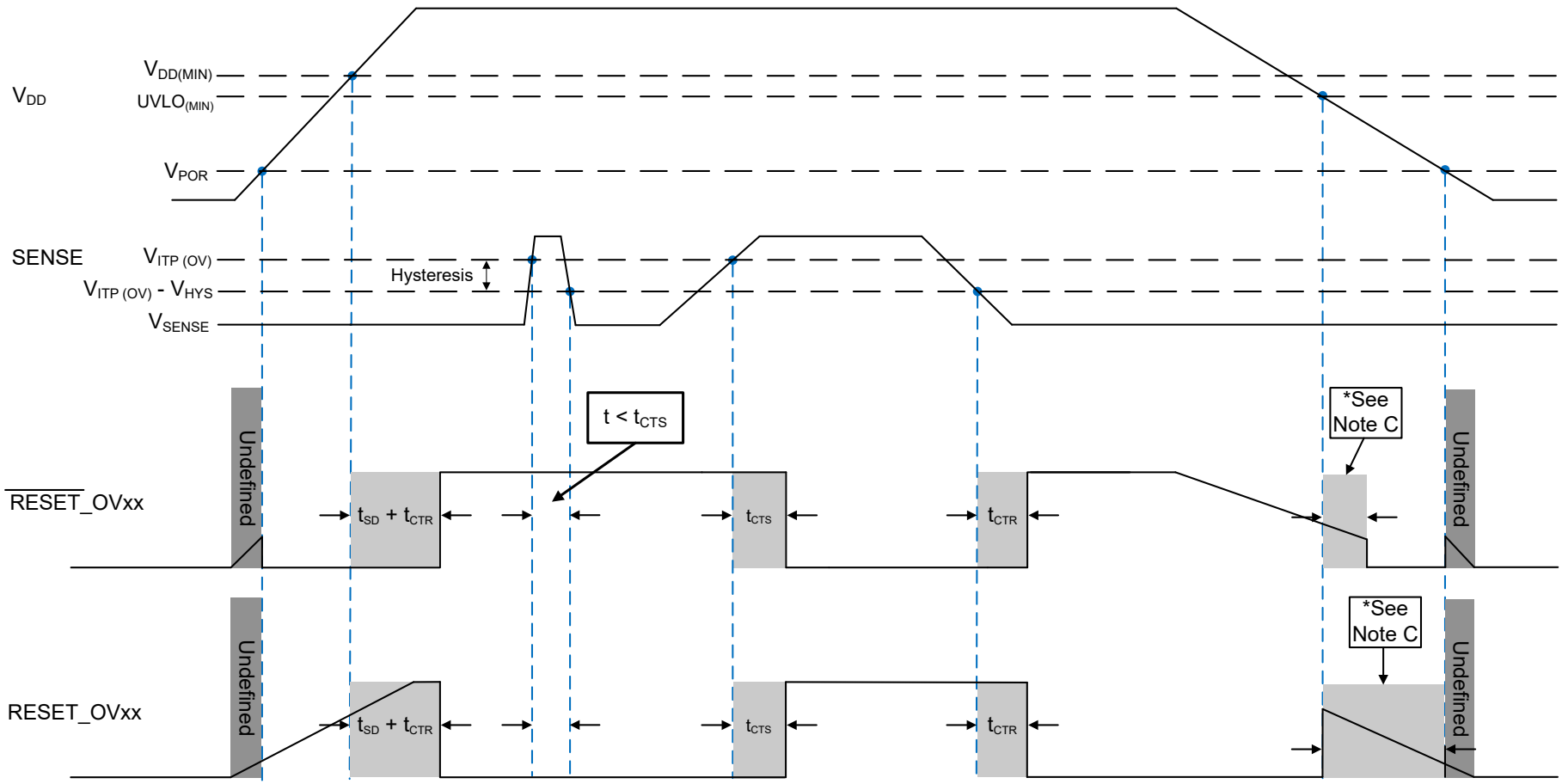



A. For open-drain output option, the timing diagram assumes the $\overline{\text{RESET}}$_UVOD / RESET_UVOD pin is connected via an external pull-up resistor to VDD.

B. Be advised that Figure 7-2 shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay ($t_{CTR}$) time.

C. $\overline{\text{RESET}}$_UVxx / RESET_UVxx is asserted when VDD goes below the $UVLO_{(MIN)}$ threshold after the time delay, $t_{CTR}$, is reached.

**Figure 7-2. SENSE Undervoltage (UV) Timing Diagram**




A. For open-drain output option, the timing diagram assumes the $\overline{\text{RESET}}$_OVOD / RESET_OVOD pin is connected via an external pull-up resistor to VDD.
B. Be advised that Figure 7-3 shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay ($t_{CTR}$) time.
C. $\overline{\text{RESET}}$_OVxx / RESET_OVxx is asserted when VDD goes below the $UVLO_{(MIN)}$ threshold after the time delay, $t_{CTR}$, is reached.

**Figure 7-3. SENSE Overvoltage (OV) Timing Diagram**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## 7.8 Typical Characteristics

Typical characteristics show the typical performance of the device. Test conditions are $T_A$ = 25°C, $R_{PU}$ = 100 kΩ, $C_{Load}$ = 50 pF, unless otherwise noted.

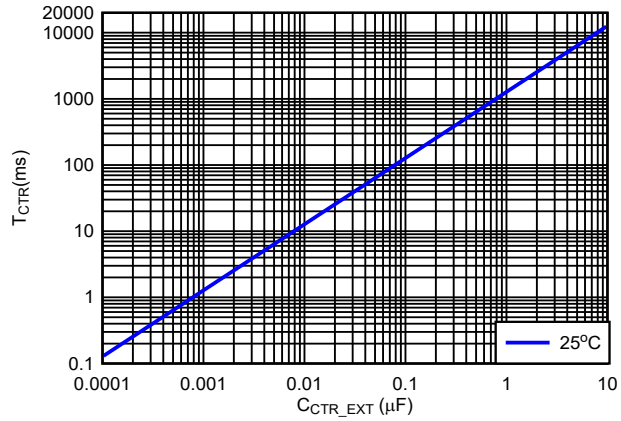



**Figure 7-4. $T_{CTR}$ vs $C_{CTR}$**

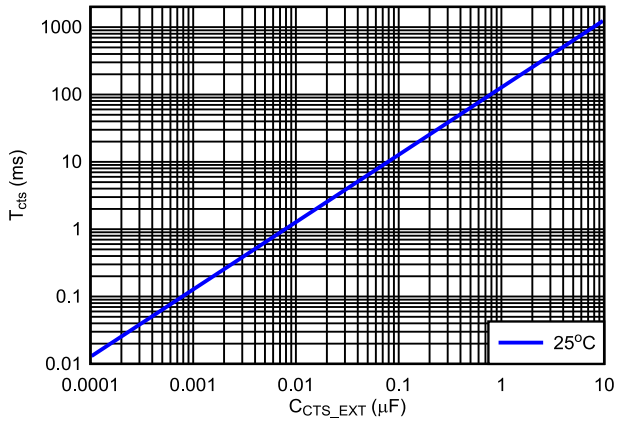
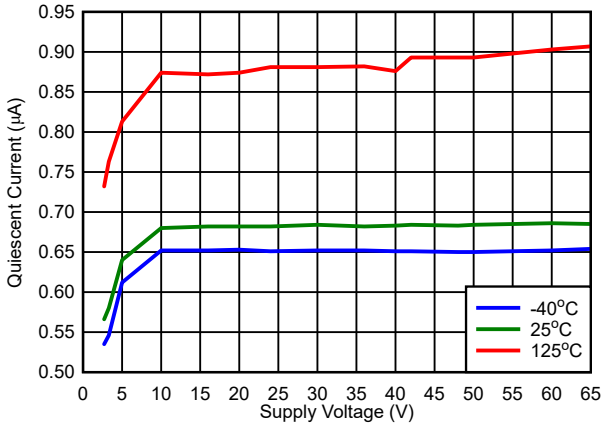
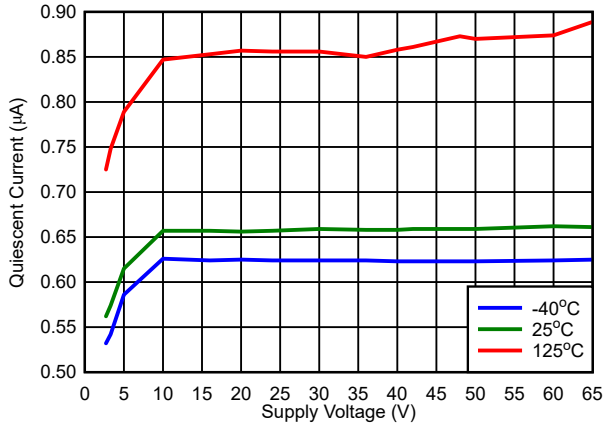



**Figure 7-5. $T_{CTS}$ vs $C_{CTS}$**



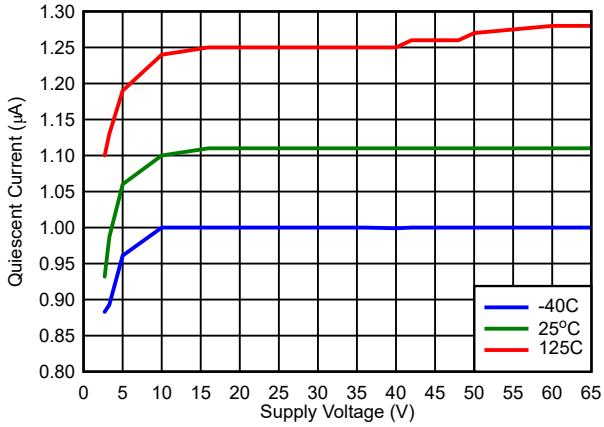

$\overline{RESET}$ = High, $V_{IT}$ = 2.7 V

**Figure 7-6. $V_{DD}$ vs $I_{DD}$ ($\overline{RESET}$ = High, $V_{IT}$ = 2.7 V)**



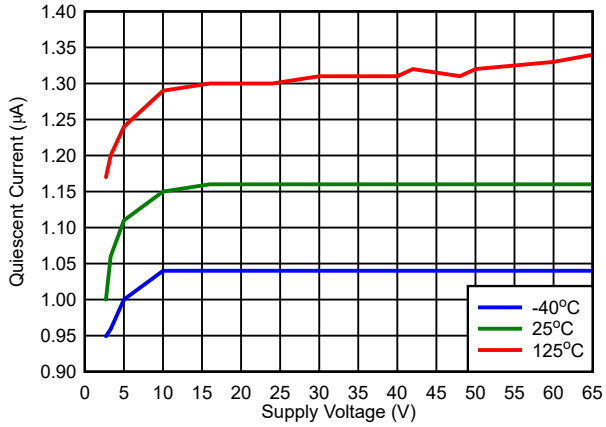

$\overline{RESET}$ = Low, $V_{IT}$ = 2.7 V

**Figure 7-7. $V_{DD}$ vs $I_{DD}$ ($\overline{RESET}$ = Low, $V_{IT}$ = 2.7 V)**




$\overline{RESET}$ = High, $V_{IT}$ = 0.8 V

**Figure 7-8. $V_{DD}$ vs $I_{DD}$ ($\overline{RESET}$ = High, $V_{IT}$ = 0.8 V)**




$\overline{RESET}$ = Low, $V_{IT}$ = 0.8 V

**Figure 7-9. $V_{DD}$ vs $I_{DD}$ ($\overline{RESET}$ = Low, $V_{IT}$ = 0.8 V)**

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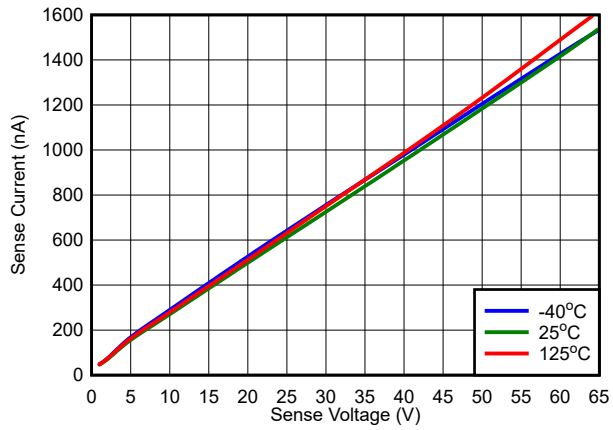
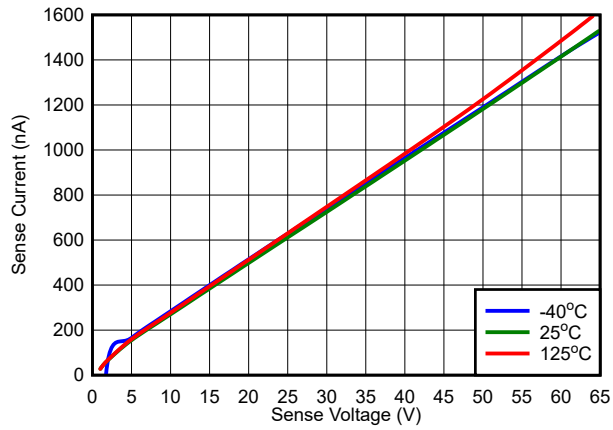
## 7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the device. Test conditions are $T_A$ = 25°C, $R_{PU}$ = 100 kΩ, $C_{Load}$ = 50 pF, unless otherwise noted.



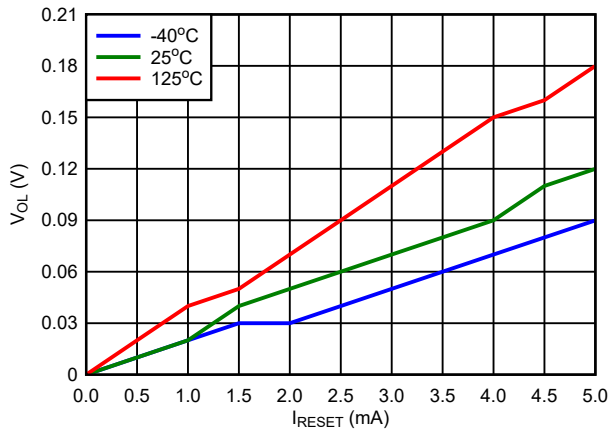

$V_{DD}$ = 2.7 V

**Figure 7-10. $V_{SENSE}$ vs $I_{SENSE}$**



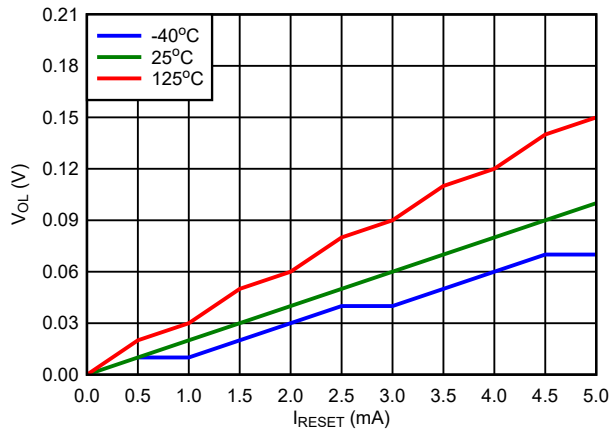

$V_{DD}$ = 65 V

**Figure 7-11. $V_{SENSE}$ vs $I_{SENSE}$**



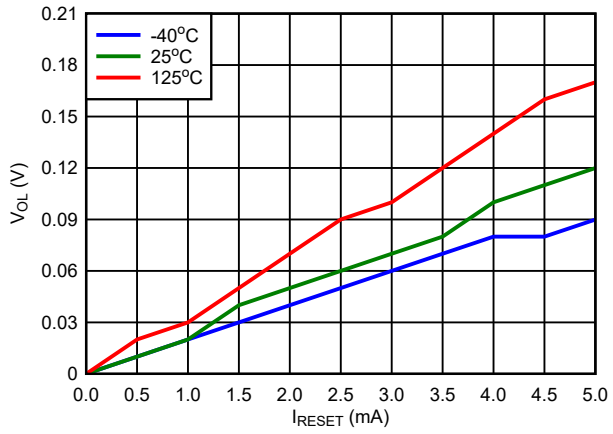

$V_{DD}$ = 2.7 V

**Figure 7-12. Open-Drain Active Low $V_{OL}$ vs $I_{RESET}$**



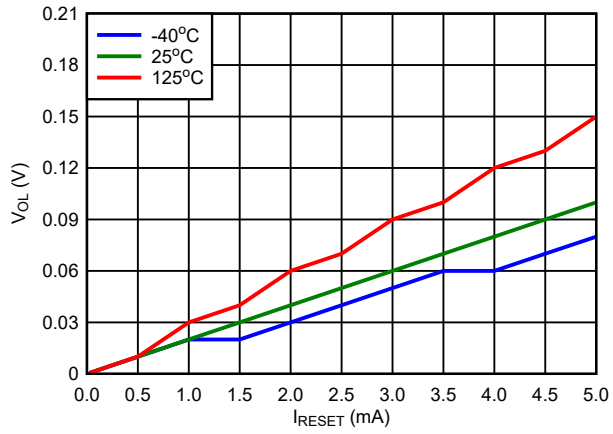

$V_{DD}$ = 65 V

**Figure 7-13. Open-Drain Active Low $V_{OL}$ vs $I_{RESET}$**




$V_{DD}$ = 2.7 V

**Figure 7-14. Open-Drain Active High $V_{OL}$ vs $I_{RESET}$**




$V_{DD}$ = 65 V

**Figure 7-15. Open-Drain Active High $V_{OL}$ vs $I_{RESET}$**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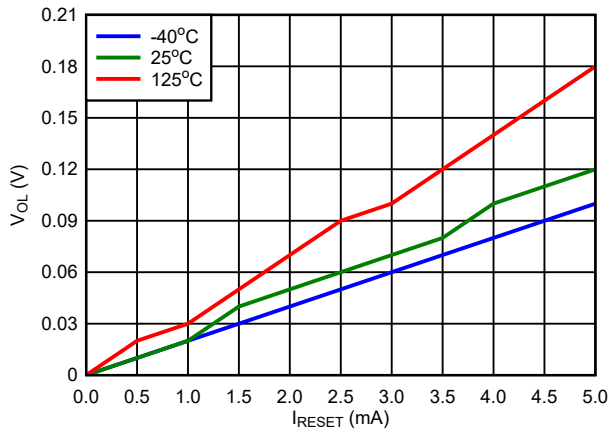
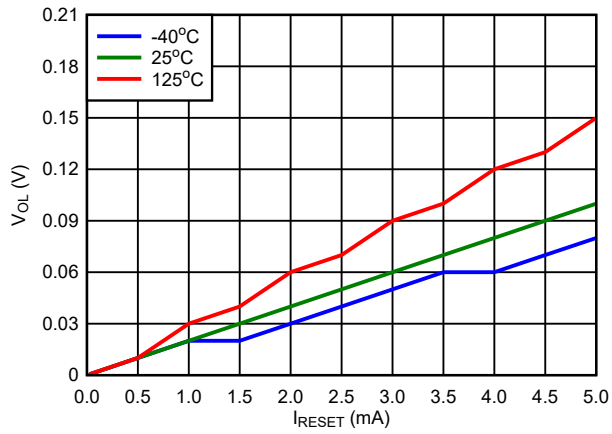
## 7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the device. Test conditions are $T_A$ = 25°C, $R_{PU}$ = 100 kΩ, $C_{Load}$ = 50 pF, unless otherwise noted.




$V_{DD}$ = 2.7 V

**Figure 7-16. Push-Pull Active High $V_{OL}$ vs $I_{RESET}$**




$V_{DD}$ = 65 V

**Figure 7-17. Push-Pull Active High $V_{OL}$ vs $I_{RESET}$**

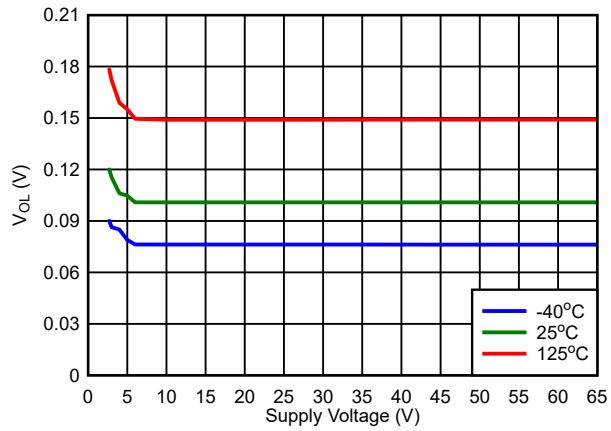



**Figure 7-18. Open-Drain Active Low $V_{OL}$ vs $V_{DD}$**

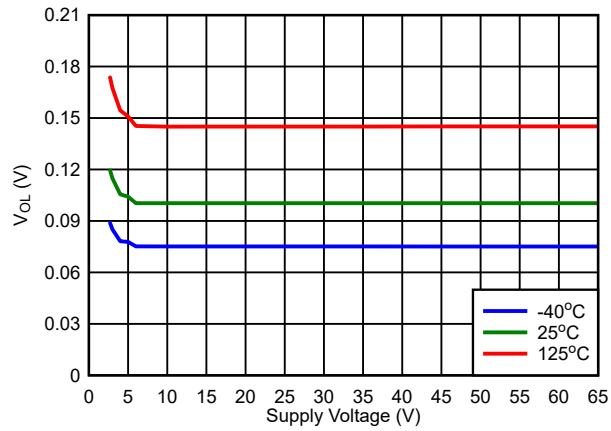



**Figure 7-19. Open-Drain Active High $V_{OL}$ vs $V_{DD}$**

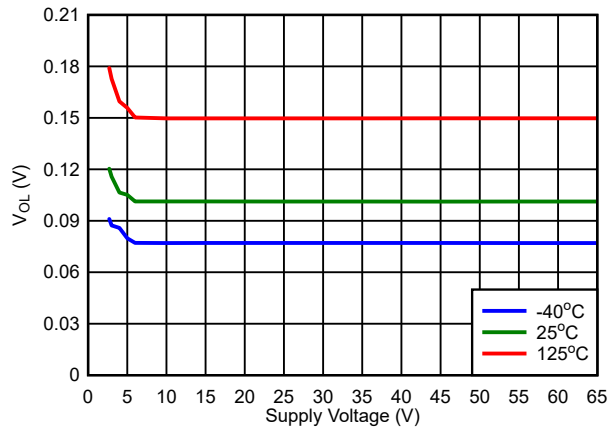



**Figure 7-20. Push-Pull Active Low $V_{OL}$ vs $V_{DD}$**

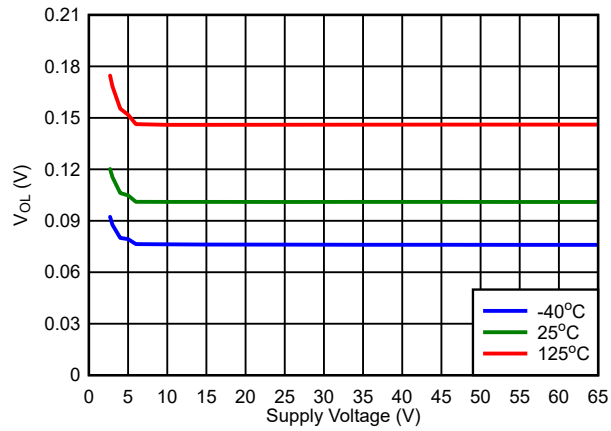



**Figure 7-21. Push-Pull Active High $V_{OL}$ vs $V_{DD}$**

## 7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the device. Test conditions are $T_A$ = 25°C, $R_{PU}$ = 100 kΩ, $C_{Load}$ = 50 pF, unless otherwise noted.

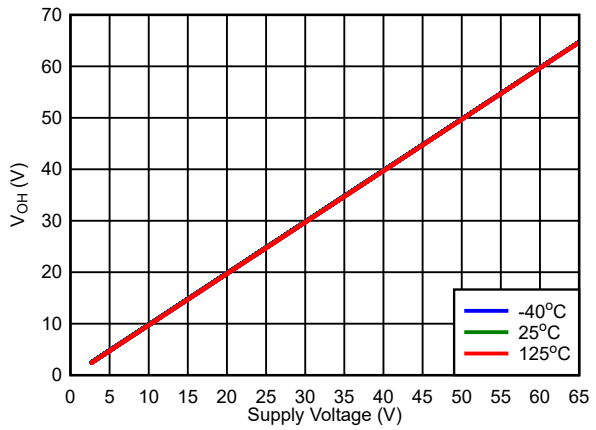



**Figure 7-22. Push-Pull Active Low $V_{OH}$ vs $V_{DD}$**

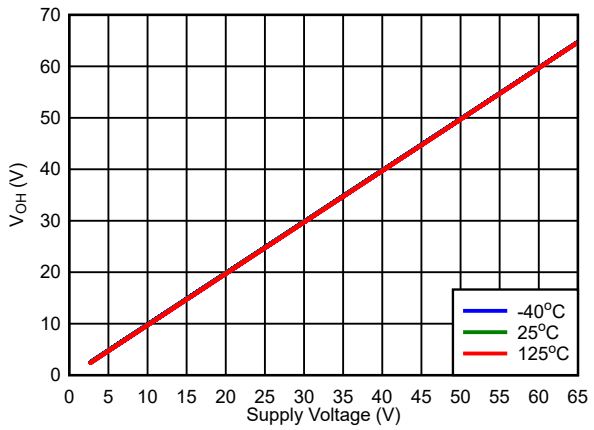



**Figure 7-23. Push-Pull Active High $V_{OH}$ vs $V_{DD}$**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# 8 Detailed Description

## 8.1 Overview

The TPS3760 is a family of high voltage and low quiescent current reset ICs with fixed threshold voltage. A voltage divider is integrated to eliminate the need for external resistors and eliminate leakage current that comes with resistor dividers. However, it can also support an external resistor if required by the application. The lowest threshold 800 mV (bypass internal resistor ladder) is recommenced for external resistors use case to take advantage of faster detection time and lower $I_{SENSE}$ current.

VDD, SENSE and RESET pins can support 65 V continuous operation; both VDD and SENSE voltage levels can be independent of each other, meaning VDD pin can be connected at 2.7 V while SENSE pins are connected to a higher voltage. Note, the TPS3760 does not have clamps within the device so external circuits or devices must be added to limit the voltages to the absolute maximum limit.

Additional features include programmable sense time delay (CTS) and reset delay time and manual reset (CTR / $\overline{MR}$).

## 8.2 Functional Block Diagram

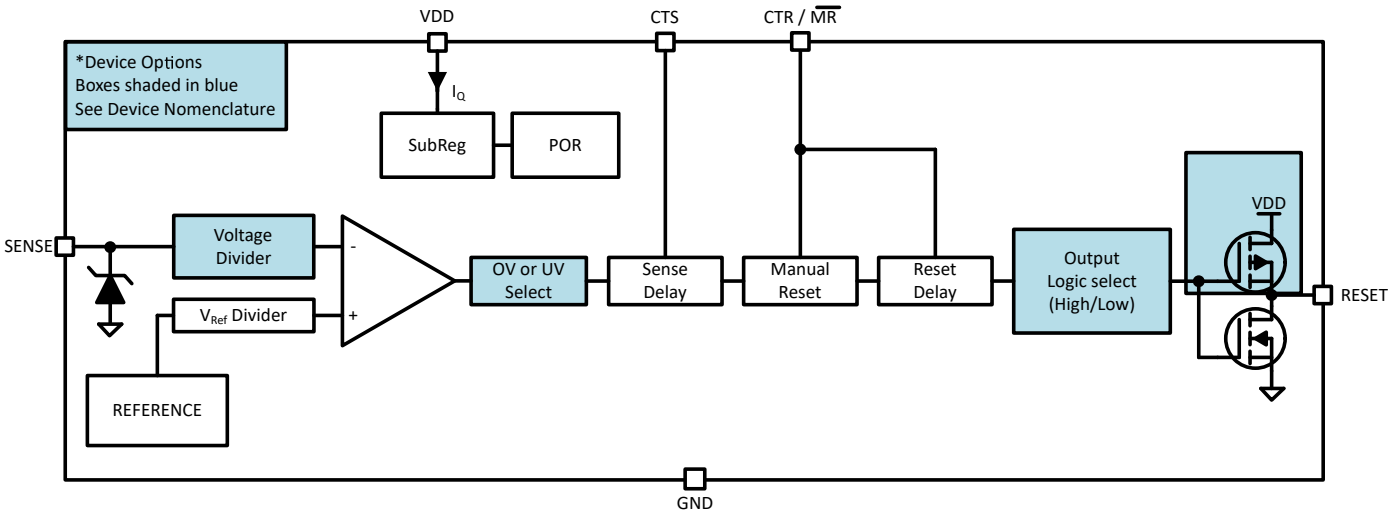


**Figure 8-1. Functional Block Diagram [1]**

[1] Refer to Section 5 for complete list of topologies and output logic combination

## 8.3 Feature Description

### 8.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7 V to 65 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1 µF capacitor between the VDD and GND.

VDD needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay ($t_{SD}$) for the device to be fully functional.

VDD voltage is independent of $V_{SENSE}$ and $V_{RESET}$, meaning that VDD can be higher or lower than the other pins.

#### *8.3.1.1 Undervoltage Lockout ($V_{POR}$ < $V_{DD}$ < UVLO)*

When the voltage on VDD is less than the UVLO voltage, but greater than the power-on reset voltage ($V_{POR}$), the output pins will be in reset, regardless of the voltage at SENSE pins.

#### *8.3.1.2 Power-On Reset ($V_{DD}$ < $V_{POR}$ )*

When the voltage on VDD is lower than the power on reset voltage ($V_{POR}$), the output signal is undefined and is not to be relied upon for proper device function.

Note: Figure 8-2 and Figure 8-3 assume an external pull-up resistor is connected to the reset pin via VDD.

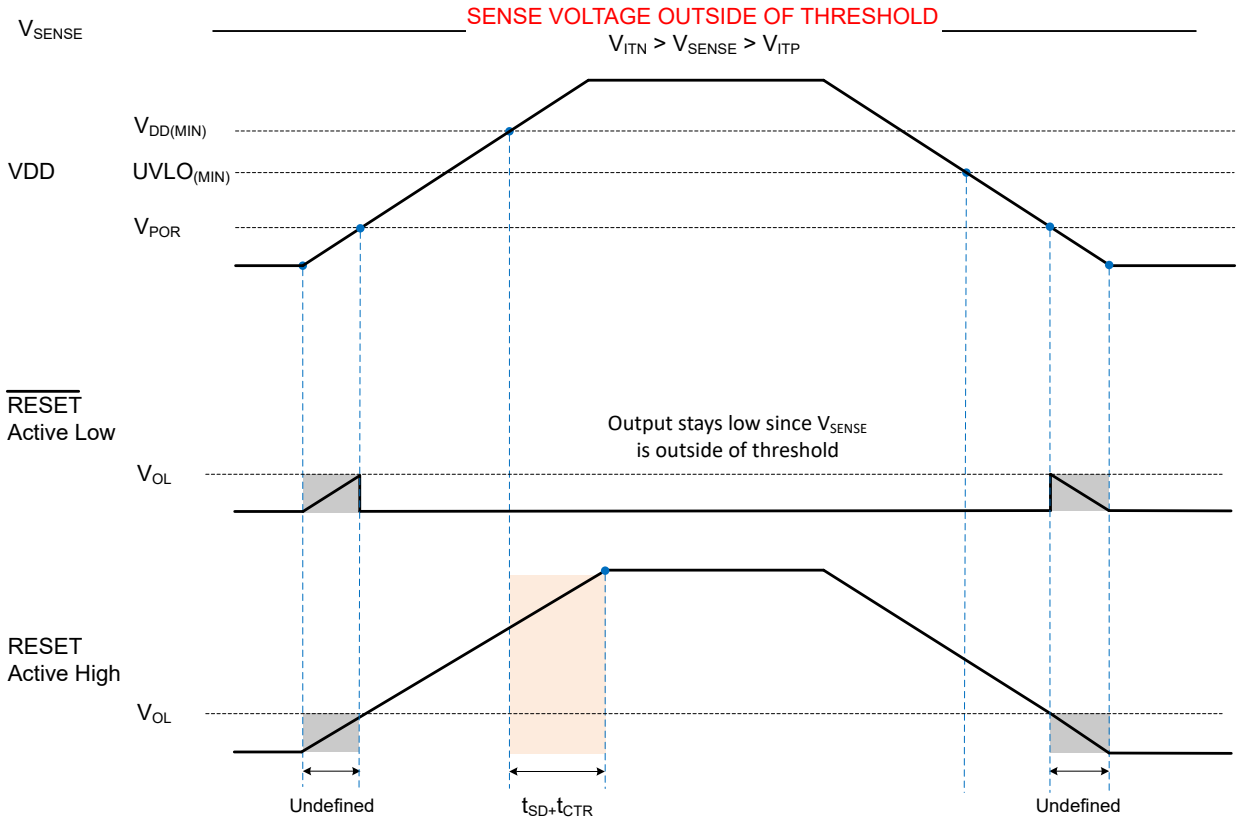


**Figure 8-2. Power Cycle (SENSE Outside of Nominal Voltage)**


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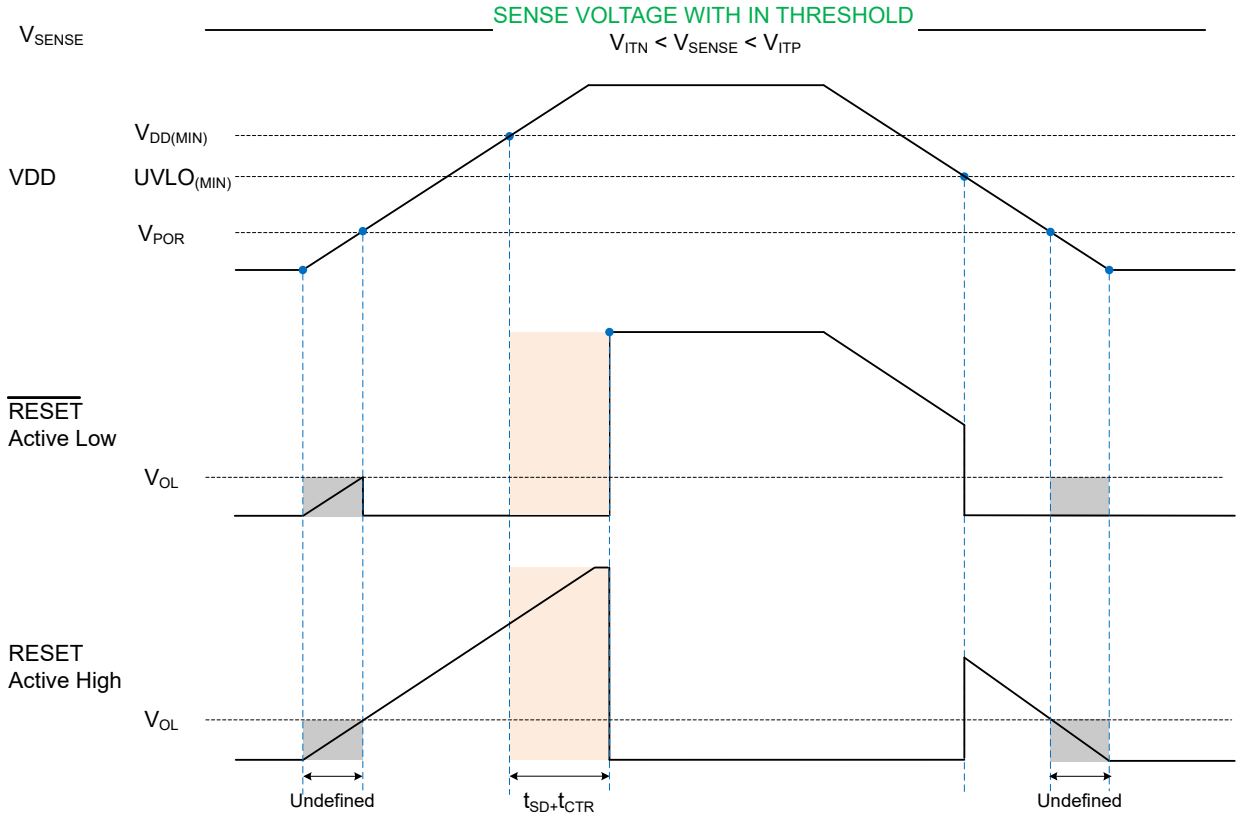


**Figure 8-3. Power Cycle (SENSE Within Nominal Voltage)**

### 8.3.2 SENSE

The TPS3760 high voltage family integrates a voltage comparator, a precision reference voltage and a trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Device also has built-in hysteresis that provides noise immunity and ensures stable operation.

Although not required in most cases, for noisy applications good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSE inputs in order to reduce sensitivity to transient voltages on the monitored signal. SENSE can be connected directly to VDD pin.

#### *8.3.2.1 SENSE Hysteresis*

Built-in hysteresis to avoid erroneous output reset release. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold ($V_{ITP}$), for undervoltage options hysteresis is added to the negative threshold ($V_{ITN}$).

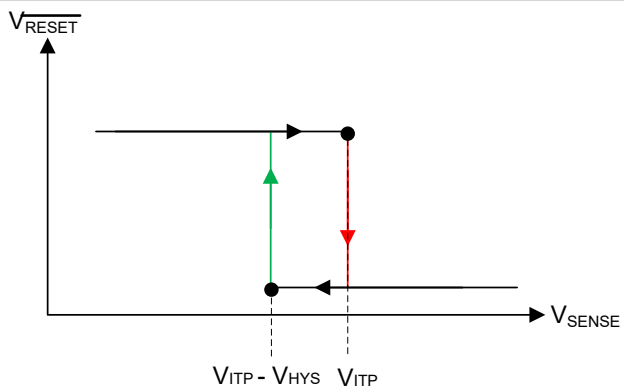


**Figure 8-4. Hysteresis (Overvoltage Active-Low)**

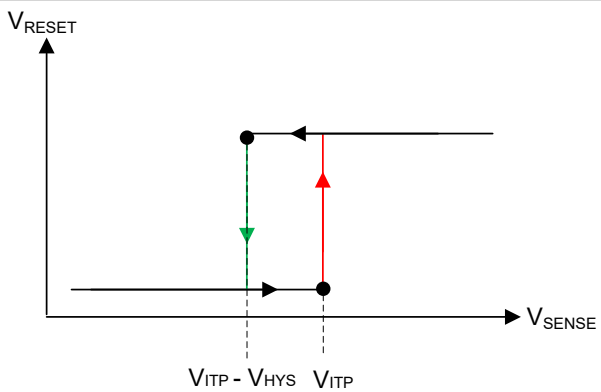


**Figure 8-5. Hysteresis (Overvoltage Active-High)**

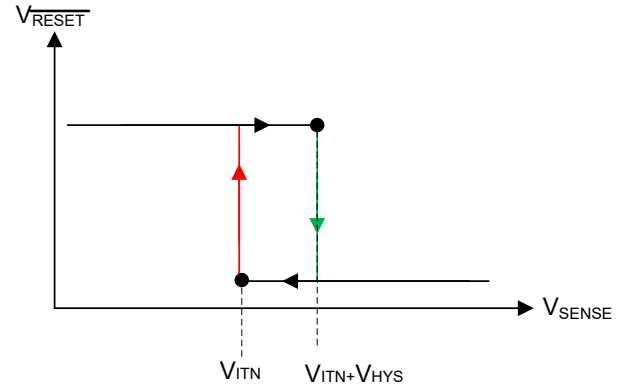


**Figure 8-6. Hysteresis (Undervoltage Active-High)**

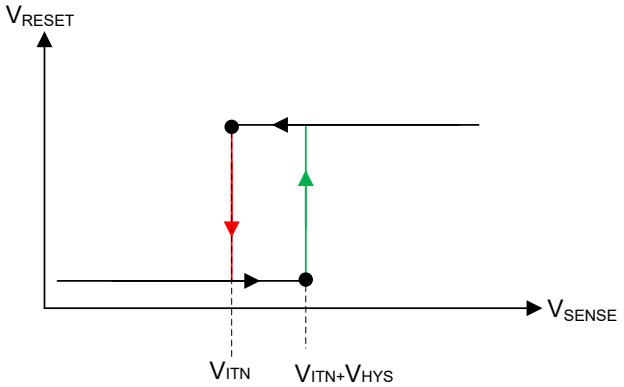


**Figure 8-7. Hysteresis (Undervoltage Active-Low)**


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**Table 8-1. Common Hysteresis Lookup Table**

| TARGET | | | DEVICE ACTUAL HYSTERESIS OPTION |
|---|---|---|---|
| DETECT THRESHOLD | TOPOLOGY | RELEASE VOLTAGE (V) | |
| 18.0 V | Overvoltage | 17.5 V | -3% |
| 18.0 V | Overvoltage | 16.0 V | -11% |
| 17.0 V | Overvoltage | 16.5 V | -3% |
| 16.0 V | Overvoltage | 15.0 V | -6% |
| 15.0 V | Overvoltage | 14.0 V | -7% |
| 6.0 V | Undervoltage | 6.5 V | 0.5 V |
| 5.5 V | Undervoltage | 6 V | 0.5 V |
| 8 V | Undervoltage | 9 V | 1 V |
| 5 V | Undervoltage | 7.5 V | 2.5 V |

Table 8-1 shows a sample of hysteresis and voltage options for the TPS3760. For threshold voltages ranging from 2.7 V to 8 V, one option is to select a fixed hysteresis value ranging from 0.5 V to 2.5 V in increments of 0.5 V. Additionally, a second option can be selected where the hysteresis value is a percentage of the threshold voltage. The percentage of voltage hysteresis ranges from 2% to 13%.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is ($V_{ITN\ (UV)}$ + $V_{HYS}$) and for the overvoltage (OV) channel is ($V_{ITP\ (OV)}$ - $V_{HYS}$). The accuracy of the release voltage, or stated in the Electrical Characteristics as *Hysteresis Accuracy* is ±1.5%. Expanding what is shown in Table 8-1, below are a few voltage hysteresis examples that include the hysteresis accuracy:

<u>Undervoltage (UV) Channel</u>

$V_{ITN}$ = 0.8 V

Voltage Hysteresis ($V_{HYS}$) = 5% = 40 mV

Hysteresis Accuracy = ±1.5% = 39.4 mV or 40.6 mV

Release Voltage = $V_{ITN}$ + $V_{HYS}$ = 839.4 mV to 840.6 mV

<u>Overvoltage (OV) Channel</u>

$V_{ITP}$ = 8 V

Voltage Hysteresis ($V_{HYS}$) = 2 V

Hysteresis Accuracy = ±1.5% = 1.97 V or 2.03 V

Release Voltage = $V_{ITN}$ - $V_{HYS}$ = 5.97 V to 6.03 V

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### 8.3.3 Output Logic Configurations

TPS3760 is a single channel device that has a single input sense pin and a single reset pin. The single channel is available as Open-Drain and Push-Pull.

The available output logic configuration combinations are shown in Table 8-2.

**Table 8-2. TPS3760 Output Logic**

| DESCRIPTION | NOMENCLATURE | VALUE |
|---|---|---|
| **GPN** | **TPS3760 (+ topology)** | **CHANNEL CONFIGURATION** |
| Topology (OV and UV only)<br>• UV = Undervoltage<br>• OV = Overvoltage<br>• PP = Push-Pull<br>• OD = Open-Drain<br>• L = Active low<br>• H = Active high | TPS3760A | UV OD L |
| | TPS3760B | UV PP L |
| | TPS3760C | UV OD H |
| | TPS3760D | UV PP H |
| | TPS3760E | OV OD L |
| | TPS3760F | OV PP L |
| | TPS3760G | OV OD H |
| | TPS3760H | OV PP H |

#### *8.3.3.1 Open-Drain*

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor consider system $V_{OH}$ and the ($I_{lkg}$) current provided in the electrical characteristics, high resistors values will have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS3760 open-drain output pin.

#### *8.3.3.2 Push-Pull*

Push-Pull output does not require an external resistor since is the output is internally pulled-up to VDD during $V_{OH}$ condition and output will be connected to GND during $V_{OH}$ condition.

#### *8.3.3.3 Active-High (RESET)*

RESET (active-high), denoted with no bar above the pin label. RESET remains low ($V_{OL}$, deasserted) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary ($V_{ITN}$).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary ($V_{ITP}$).

#### *8.3.3.4 Active-Low ($\overline{RESET}$)*

$\overline{RESET}$ (active low) denoted with a bar above the pin label. $\overline{RESET}$ remains high voltage ($V_{OH}$, deasserted) (open-drain variant $V_{OH}$ is measured against the pullup voltage) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary ($V_{ITN}$).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary ($V_{ITP}$).


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### 8.3.4 User-Programmable Reset Time Delay

TPS3760 has adjustable reset release time delay with external capacitors.

- A capacitor in CTR / $\overline{MR}$ programs the reset time delay of the output.
- No capacitor on this pin gives the fastest reset delay time indicated in the Section 7.6.

#### *8.3.4.1 Reset Time Delay Configuration*

The time delay ($t_{CTR}$) can be programmed by connecting a capacitor between CTR pin and GND.

The relationship between external capacitor $C_{CTR_EXT\ (typ)}$ and the time delay $t_{CTR\ (typ)}$ is given by Equation 1.

$$t_{CTR\ (typ)} = -\ln(0.28) \times R_{CTR\ (typ)} \times C_{CTR_EXT\ (typ)} + t_{CTR\ (no\ cap)} \quad (1)$$

$R_{CTR\ (typ)}$ = is in kilo ohms (kOhms)

$C_{CTR_EXT\ (typ)}$ = is given in microfarads (µF)

$t_{CTR\ (typ)}$ = is the reset time delay (ms)

The reset delay varies according to three variables: the external capacitor ($C_{CTR_EXT}$), CTR pin internal resistance ($R_{CTR}$) provided in Section 7, and a constant. The minimum and maximum variance due to the constant is show in Equation 2 and Equation 3:

$$t_{CTR\ (min)} = -\ln(0.31) \times R_{CTR\ (min)} \times C_{CTR_EXT\ (min)} + t_{CTR\ (no\ cap\ (min))} \quad (2)$$

$$t_{CTR\ (max)} = -\ln(0.25) \times R_{CTR\ (max)} \times C_{CTR_EXT\ (max)} + t_{CTR\ (no\ cap\ (max))} \quad (3)$$

The recommended maximum reset delay capacitor for the TPS3760 is limited to 10 µF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 5% of the programmed reset time delay.

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### 8.3.5 User-Programmable Sense Delay

TPS3760 has adjustable sense release time delay with external capacitors.

- A capacitor in CTS programs the excursion detection on SENSE.
- No capacitor on these pins gives the fastest detection time indicated in the Section 7.6.

#### *8.3.5.1 Sense Time Delay Configuration*

The time delay ($t_{CTS}$) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS_EXT\ (typ)}$ and the time delay $t_{CTS\ (typ)}$ is given by Equation 4.

$$t_{CTS\ (typ)} = -\ln(0.28) \times R_{CTS\ (typ)} \times C_{CTS_EXT\ (typ)} + t_{CTS\ (no\ cap)} \quad (4)$$

$R_{CTS}$ = is in kilo ohms (kOhms)

$C_{CTS_EXT}$ = is given in microfarads (µF)

$t_{CTS}$ = is the sense time delay (ms)

The sense delay varies according to three variables: the external capacitor ($C_{CTS_EXT}$), CTS pin internal resistance ($R_{CTS}$) provided in Electrical Characteristics, and a constant. The minimum and maximum variance due to the constant is show in Equation 5 and Equation 6:

$$t_{CTS\ (min)} = -\ln(0.31) \times R_{CTS\ (min)} \times C_{CTS_EXT\ (min)} + t_{CTS\ (no\ cap\ (min))} \quad (5)$$

$$t_{CTS\ (max)} = -\ln(0.25) \times R_{CTS\ (max)} \times C_{CTS_EXT\ (max)} + t_{CTSx\ (no\ cap\ (max))} \quad (6)$$

The recommended maximum sense delay capacitor for the is limited to 10 µF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time between fault events to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or time duration between fault events needs to be greater than 10% of the programmed sense time delay.


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### 8.3.6 Manual RESET (CTR / $\overline{MR}$) Input

The manual reset input allows a processor or other logic circuits to initiate a reset. In this section $\overline{MR}$ is a generic reference to (CTR / $\overline{MR}$). A logic low on $\overline{MR}$ causes $\overline{RESET}$ to assert on reset output. After $\overline{MR}$ is left floating, $\overline{RESET}$ will release the reset if the voltage at SENSE pin is at nominal voltage. $\overline{MR}$ should not be driven high, this pin should be left floating or connected to a capacitor to GND, this pin can be left unconnected if is not used.

If the logic driving the $\overline{MR}$ cannot tri-state (floating and GND) then a logic-level FET should be used as illustrated in Figure 8-8.

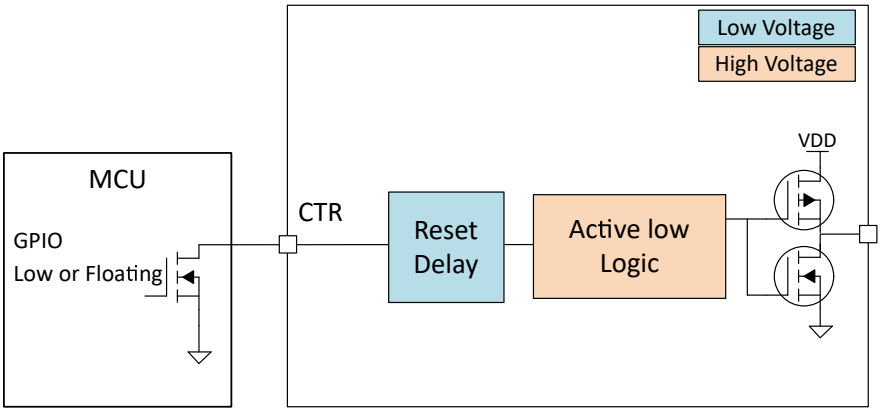


**Figure 8-8. Manual Reset Implementation**

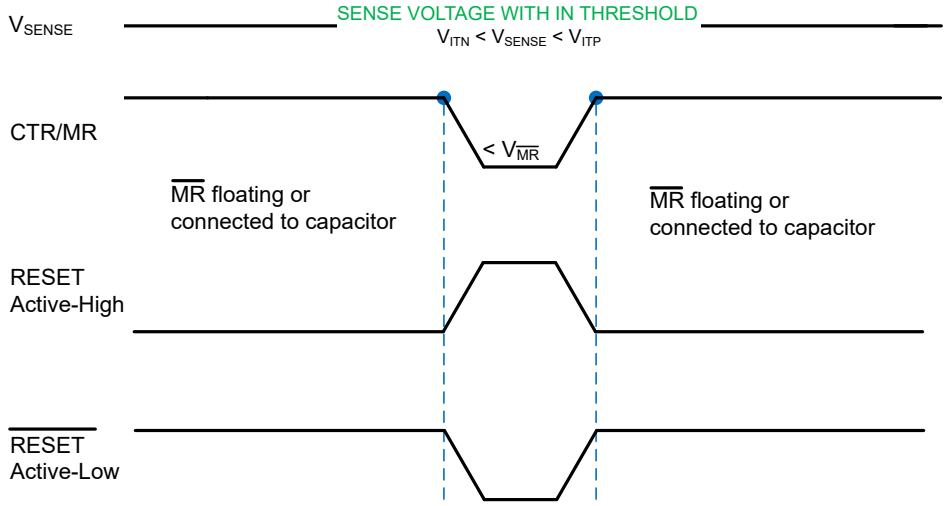


**Figure 8-9. Manual Reset Timing Diagram**

**Table 8-3. $\overline{MR}$ Functional Table**

| $\overline{MR}$ | SENSE ON NOMINAL VOLTAGE | RESET STATUS |
|---|---|---|
| Low | Yes | Reset asserted |
| Floating | Yes | Fast reset release when SENSE voltage goes back to nominal voltage |
| Capacitor | Yes | Programmable reset time delay |
| High | Yes | NOT Recommended |

### 8.3.7 $\overline{\text{RESET}}$ Latch Mode

The TPS3760 features a output latch mode on the RESET/$\overline{\text{RESET}}$ pin when connecting the $\overline{\text{LATCH}}$ pin to common ground. A pull-down resistor, 10 kΩ, is recommended to limit current consumption of the system. In latch mode, if the RESET/$\overline{\text{RESET}}$ pin is low or triggers low and less than 1.4V is applied to the $\overline{\text{LATCH}}$ pin, the RESET/$\overline{\text{RESET}}$ pin stays asserted regardless if VSENSE goes within the acceptable voltage boundaries (VSENSE > VITP + $V_{hyst}$ for UV or VSENSE < VITN - $V_{hyst}$ for OV). To unlatch the device a voltage greater than 2.1 V for greater than 3 µs is applied to the $\overline{\text{LATCH}}$ pin. This is recommended to maintain a proper unlatch. The RESET/$\overline{\text{RESET}}$ pin triggers high after the duration of $t_{ctr}$. TI recommends using a series resistance to limit current when an unlatch voltage is applied.

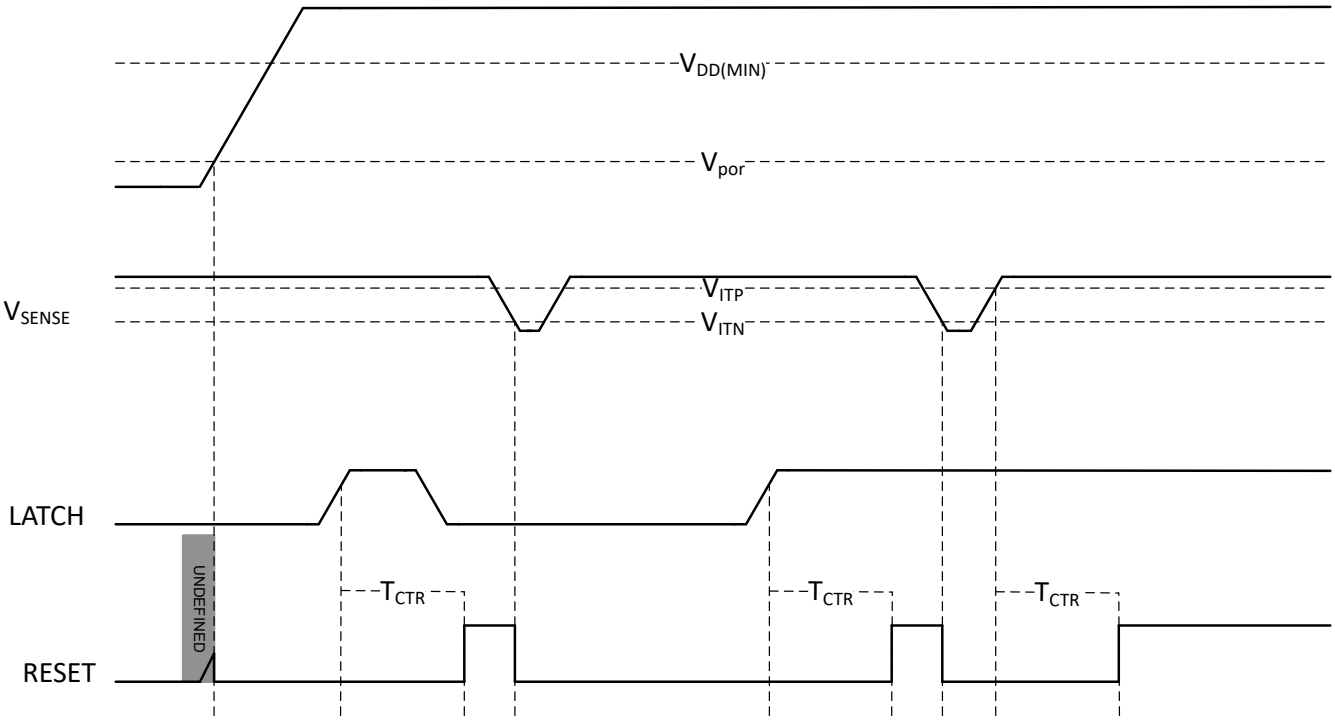


**Figure 8-10. Latch Timing Diagram**


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## 8.4 Device Functional Modes

**Table 8-4. Undervoltage Detect Functional Mode Truth Table**

| DESCRIPTION | SENSE | | CTR [1] / $\overline{MR}$ PIN | VDD PIN | OUTPUT [2] ($\overline{RESET}$ PIN) |
|---|---|---|---|---|---|
| | PREVIOUS CONDITION | CURRENT CONDITION | | | |
| Normal Operation | SENSE > $V_{ITN(UV)}$ | SENSE > $V_{ITN(UV)}$ | Open or capacitor connected | $V_{DD} > V_{DD(MIN)}$ | High |
| Undervoltage Detection | SENSE > $V_{ITN(UV)}$ | SENSE < $V_{ITN(UV)}$ | Open or capacitor connected | $V_{DD} > V_{DD(MIN)}$ | Low |
| Undervoltage Detection | SENSE < $V_{ITN(UV)}$ | SENSE > $V_{ITN(UV)}$ | Open or capacitor connected | $V_{DD} > V_{DD(MIN)}$ | Low |
| Normal Operation | SENSE < $V_{ITN(UV)}$ | SENSE > $V_{ITN(UV)}$ + HYS | Open or capacitor connected | $V_{DD} > V_{DD(MIN)}$ | High |
| Manual Reset | SENSE > $V_{ITN(UV)}$ | SENSE > $V_{ITN(UV)}$ | Low | $V_{DD} > V_{DD(MIN)}$ | Low |
| UVLO Engaged | SENSE > $V_{ITN(UV)}$ | SENSE > $V_{ITN(UV)}$ | Open or capacitor connected | $V_{POR} < V_{DD} < V_{DD(MIN)}$ | Low |
| Below $V_{POR}$, Undefined Output | SENSE > $V_{ITN(UV)}$ | SENSE > $V_{ITN(UV)}$ | Open or capacitor connected | $V_{DD} < V_{POR}$ | Undefined |

(1) Reset time delay is ignored in the truth table.
(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

**Table 8-5. Overvoltage Detect Functional Mode Truth Table**

| DESCRIPTION | SENSE | | CTR [1] / $\overline{MR}$ PIN | VDD PIN | OUTPUT [2] ($\overline{RESET}$ PIN) |
|---|---|---|---|---|---|
| | PREVIOUS CONDITION | CURRENT CONDITION | | | |
| Normal Operation | SENSE < $V_{ITN(OV)}$ | SENSE < $V_{ITN(OV)}$ | Open or capacitor connected | $V_{DD} > V_{DD(MIN)}$ | High |
| Overvoltage Detection | SENSE < $V_{ITN(OV)}$ | SENSE > $V_{ITN(OV)}$ | Open or capacitor connected | $V_{DD} > V_{DD(MIN)}$ | Low |
| Overvoltage Detection | SENSE > $V_{ITN(OV)}$ | SENSE < $V_{ITN(OV)}$ | Open or capacitor connected | $V_{DD} > V_{DD(MIN)}$ | Low |
| Normal Operation | SENSE > $V_{ITN(OV)}$ | SENSE < $V_{ITN(OV)}$ - HYS | Open or capacitor connected | $V_{DD} > V_{DD(MIN)}$ | High |
| Manual Reset | SENSE < $V_{ITN(OV)}$ | SENSE < $V_{ITN(OV)}$ | Low | $V_{DD} > V_{DD(MIN)}$ | Low |
| UVLO Engaged | SENSE < $V_{ITN(OV)}$ | SENSE < $V_{ITN(OV)}$ | Open or capacitor connected | $V_{POR} < V_{DD}$ < UVLO | Low |
| Below $V_{POR}$, Undefined Output | SENSE < $V_{ITN(OV)}$ | SENSE < $V_{ITN(OV)}$ | Open or capacitor connected | $V_{DD} < V_{POR}$ | Undefined |

(1) Reset time delay is ignored in the truth table.
(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The following sections describe in detail how to properly use this device. As this device has many applications and setups, there are many situations that this datasheet can not characterize in detail and will vary from these applications depending on the requirements of the final application

## 9.2 Adjustable Voltage Thresholds

Equation 7 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8 V voltage threshold device when using an adjustable voltage variant. This variant bypasses the internal resistor ladder.

For example, consider a 12 V rail being monitored $V_{MON}$ for undervoltage (UV) using of the TPS3760A012DYYR variant. Using Equation 7 and shown in Equation 8, $R_1$ is the top resistor of the resistor divider that is between $V_{MON}$ and $V_{SENSE}$, $R_2$ is the bottom resistor that is between $V_{SENSE}$ and GND, $V_{MON}$ is the voltage rail that is being monitored and $V_{SENSE}$ is the input threshold voltage. The monitored UV threshold, denoted as $V_{MON-}$, where the device will assert a reset signal occurs when $V_{SENSE} = V_{IT-(UV)}$ or, for this example, $V_{MON-} = 10.8V$ which is 90% from 12 V. Using Equation 7 and assuming $R_2 = 10k\Omega$ , $R_1$ can be calculated shown in Equation 8 where $I_{R1}$ is represented in Equation 9:

$$V_{SENSE} = V_{MON-} \times (R_2 \div (R_1 + R_2)) \tag{7}$$

$$R_1 = (V_{MON-} - V_{SENSE}) \div I_{R1} \tag{8}$$

$$I_{R1} = I_{R2} = V_{SENSE} \div R_2 \tag{9}$$

Substituting Equation 9 into Equation 8 and solving for $R_1$ in Equation 7, $R_1 = 125k\Omega$. The TPS3760A012DYYR is typically meant to monitor a 0.8 V rail with ±2% voltage threshold hysteresis. For the reset signal to become deasserted, $V_{MON}$ would need to go above $V_{IT-} + V_{HYS}$. For this example,
$V_{MON} = 11.016$ V when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that may affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance $R_{SENSE}$ can be calculated by the SENSE voltage $V_{SENSE}$ divided by the SENSE current $I_{SENSE}$ as shown in Equation 11. $V_{SENSE}$ can be calculated using Equation 7 depending on the resistor divider and monitored voltage. $I_{SENSE}$ can be calculated using Equation 10.

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \tag{10}$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \tag{11}$$


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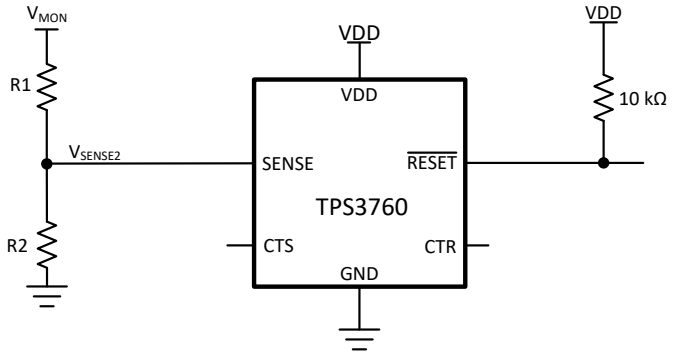


**Figure 9-1. Adjustable Voltage Threshold with External Resistor Dividers**

## 9.3 Typical Application

### 9.3.1 Design 1: Off-Battery Monitoring

This application is intended for the initial power stage in applications with the 12 V batteries. Variation of the battery voltage is common between 9 V and 16 V. Furthermore, if cold-cranking and load dump conditions are considered, voltage transients can occur as low as 3 V and as high as 42 V. In this design example, we are highlighting the ability for low power, direct off-battery voltage supervision.

Figure 11-1 illustrates an example of how the TPS3760 is monitoring the battery voltage while being powered by it, as well.

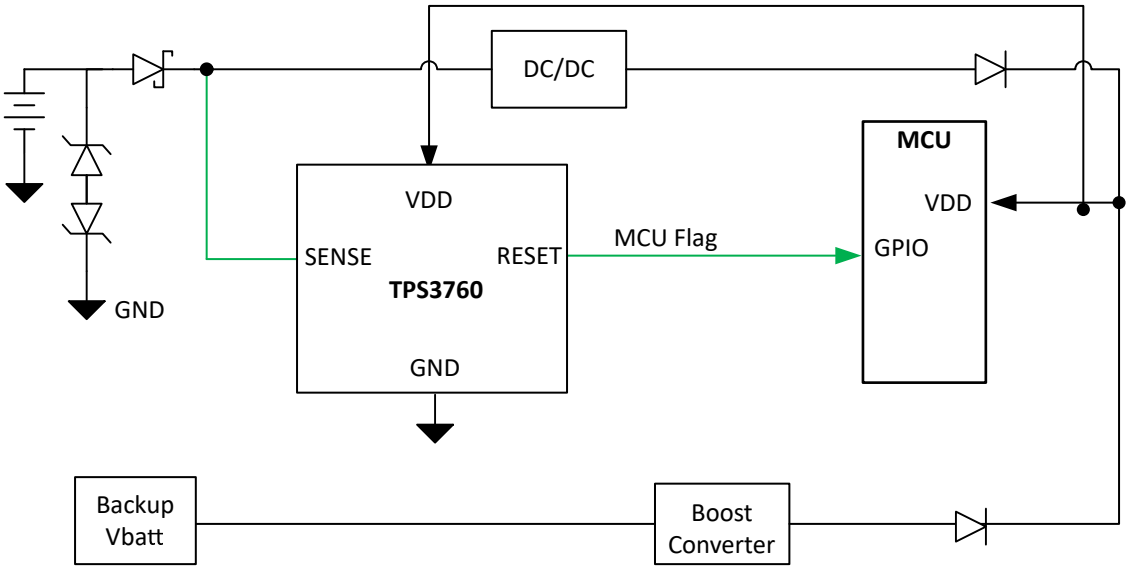


**Figure 9-2. TPS3760 Overvoltage Supervisor with Direct Off-Battery Monitoring**

#### 9.3.1.1 Design Requirements

This design requires voltage supervision on a 12 V power supply voltage rail with possibility of the 12 V rail rising up as high as 42 V. The undervoltage fault occurs when the power supply voltage drops below 7.7 V.

| PARAMETER | DESIGN REQUIREMENT | DESIGN RESULT |
|---|---|---|
| Power Rail Voltage Supervision | Monitor 12-V power supply for undervoltage condition, trigger a undervoltage fault at 7.7 V. | TPS3760 provides voltage monitoring with 1.5% max accuracy with adjustable/non-adjustable variations. |
| Maximum Input Power | Operate with power supply input up to 42 V. | The TPS3760 can support a VDD of up to 65 V. |
| Output logic voltage | Open-Drain Output Topology | An open-drain output is recommended to provide the correct reset signal, but a push-pull can also be used. |
| Maximum system current consumption | 2 µA max when power supply is at 12 V typical | TPS3760 allows for $I_Q$ to remain low with support of up to 65 V. This allows for no external resistor divider to be required. |
| Voltage Monitor Accuracy | Maximum voltage monitor accuracy of 1.5%. | The TPS3760 has 1.5% maximum voltage monitor accuracy. |
| Delay when returning from fault condition | $\overline{\text{RESET}}$ delay of at least 12.8 ms when returning from a undervoltage fault. | $C_{CTR}$ = 10 nF sets 12.8 ms delay |

#### 9.3.1.2 Detailed Design Procedure

The primary advantage of this application is being able to directly monitor a voltage on an automotive battery without needing external an resistor dividers on the SENSE input. This keeps the overall $I_Q$ of the design low while still achieving the desired rail monitoring.

Voltage rail monitoring is done by connecting the SENSE input directly to the battery rail after the TVS protection diodes. The TPS3760 that is being used in this example is a fixed voltage variant where theSENSE threshold voltage has been set internally. Word of caution, the TVS protection diodes must be chosen such that the transient voltages on the monitored rails do not exceed the absolute max limit listed in Section 7.1.

To use this configuration, the specific voltage threshold variation of the device must be chosen according to the application. In this configuration, the '77' variation must be chosen for 7.7 V as shown in Section 5.

The device being able to handle 65 V on VDD means the monitored voltage rail can go as high as 42 V for the application transients and not violate the recommended maximum for the supervisor as it usually would. This is useful when monitoring a voltage rail that has a wide range that may go much higher than the nominal rail voltage such as in this case. Good design practice recommends using a 0.1 µF capacitor on the VDD pin and this capacitance may need to increase if using an adjustable version with a resistor divider.


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### 9.3.1.3 Application Curves

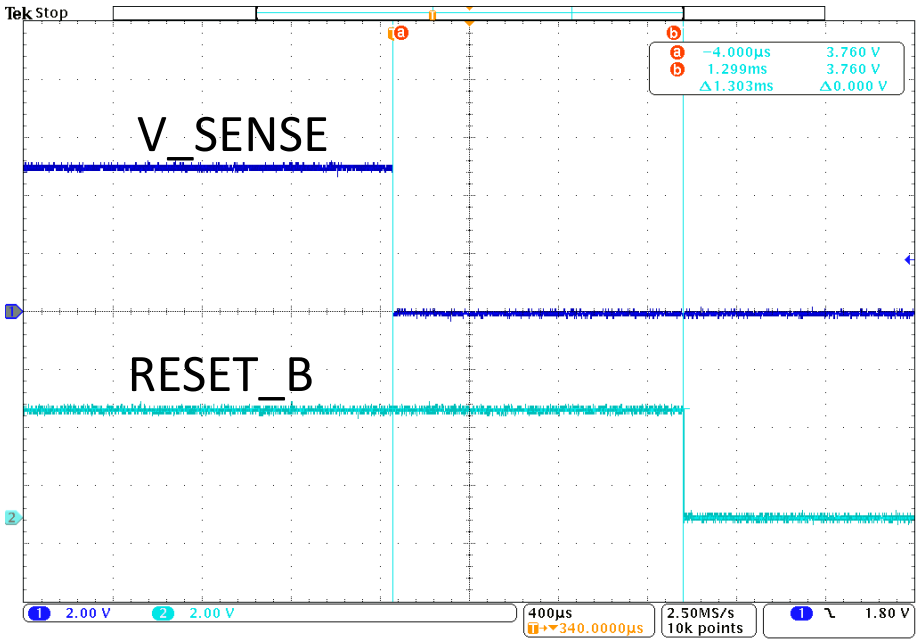


**Figure 9-3. Undervoltage Reset Waveform**

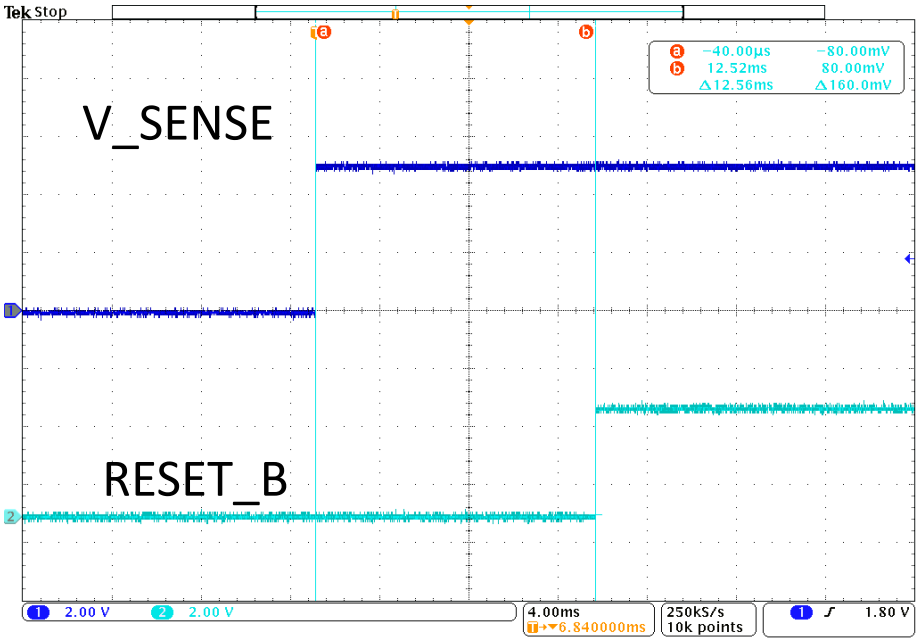


**Figure 9-4. Undervoltage Recovery Waveform**

# 10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.4 V ($V_{POR}$) to 65 V (maximum operation). Good analog design practice recommends placing a minimum 0.1 µF ceramic capacitor as near as possible to the VDD pin.

## 10.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using Equation 12:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} – T_A) / R_{\theta JA}) \quad (12)$$

The actual power being dissipated in the device can be represented by Equation 13:

$$P_D = V_{DD} \times I_{DD} + p_{RESET} \quad (13)$$

$p_{RESET}$ is calculated by Equation 14 or Equation 15

$$p_{RESET\ (PUSHPULL)} = VDD - V_{RESET} \times I_{RESET} \quad (14)$$

$$p_{RESET\ (OPEN\text{-}DRAIN)} = V_{RESET} \times I_{RESET} \quad (15)$$

Equation 12 and Equation 13 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation ($P_D$) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be de-rated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 16:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (16)$$


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# 11 Layout

## 11.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1 µF ceramic capacitor as near as possible to the VDD pin.
- To further improve the noise immunity on the SENSE pins, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5 pF.
- For open-drain variants, place the pull-up resistors on $\overline{\text{RESET}}$ as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces should be greater than 20 mils (0.5 mm).
- Do not have high voltage metal pads or traces closer than 20 mils (0.5 mm) to the low voltage metal pads or traces.

## 11.2 Layout Example

The layout example in Figure 11-1 shows how the TPS3760 is laid out on a printed circuit board (PCB) with user-defined delays.

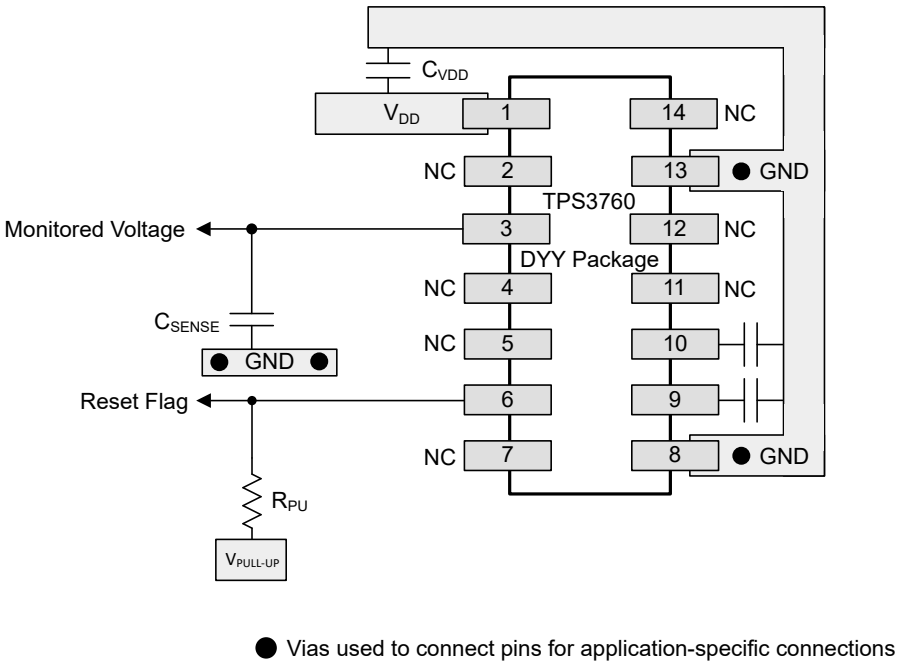


**Figure 11-1. TPS3760 Recommended Layout**

## 11.3 Creepage Distance

Per IEC 60664 Creepage is the shortest distance between two conductive parts or as shown in Figure 11-2 the distance between high voltage conductive parts and grounded parts, the floating conductive part is ignored and subtracted from the total distance.

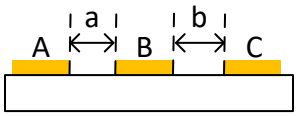


**Figure 11-2. Creepage Distance**

Figure 11-2 details

- A = Left pins (high voltage)
- B = Central pad (conductive not internally connected, can be left floating or connected to GND)
- C = Right pins (low voltages)
- Creepage distance = a + b


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# 12 Device and Documentation Support

## 12.1 Device Nomenclature

Section 5 shows how to decode the function of the device based on its part number

Table 12-1 shows possible voltage options per channel. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

**Table 12-1. Voltage Options**

| 100 mV STEPS | | | | 400 mV STEPS | | 500 mV STEPS | | 1 V STEPS | |
|---|---|---|---|---|---|---|---|---|---|
| NOMEN-CLATURE | VOLTAGE OPTIONS | NOMEN-CLATURE | VOLTAGE OPTIONS | NOMEN-CLATURE | VOLTAGE OPTIONS | NOMEN-CLATURE | VOLTAGE OPTIONS | NOMEN-CLATURE | VOLTAGE OPTIONS |
| **01** | 800 mV (divider bypass) | **70** | 7.0 V | **A0** | 10.4 V | **D0** | 20.5 V | **F0** | 31.0 V |
| **27** | 2.7 V | **71** | 7.1 V | **A1** | 10.8 V | **D1** | 21.0 V | **F1** | 32.0 V |
| **28** | 2.8 V | **72** | 7.2 V | **A2** | 11.2 V | **D2** | 21.5 V | **F2** | 33.0 V |
| **29** | 2.9 V | **73** | 7.3 V | **A3** | 11.6 V | **D3** | 22.0 V | **F3** | 34.0 V |
| **30** | 3.0 V | **74** | 7.4 V | **A4** | 12.0 V | **D4** | 22.5 V | **F4** | 35.0 V |
| **31** | 3.1 V | **75** | 7.5 V | **A5** | 12.4 V | **D5** | 23.0 V | **F5** | 36.0 V |
| **32** | 3.2 V | **76** | 7.6 V | **A6** | 12.8 V | **D6** | 23.5 V | | |
| **33** | 3.3 V | **77** | 7.7 V | **A7** | 13.2 V | **D7** | 24.0 V | | |
| **34** | 3.4 V | **78** | 7.8 V | **A8** | 13.6 V | **D8** | 24.5 V | | |
| **35** | 3.5 V | **79** | 7.9 V | **A9** | 14.0 V | **D9** | 25.0 V | | |
| **36** | 3.6 V | **80** | 8.0 V | **B0** | 14.4 V | **E0** | 25.5 V | | |
| **37** | 3.7 V | **81** | 8.1 V | **B1** | 14.8 V | **E1** | 26.0 V | | |
| **38** | 3.8 V | **82** | 8.2 V | **B2** | 15.2 V | **E2** | 26.5 V | | |
| **39** | 3.9 V | **83** | 8.3 V | **B3** | 15.6 V | **E3** | 27.0 V | | |
| **40** | 4.0 V | **84** | 8.4 V | **B4** | 16.0 V | **E4** | 27.5 V | | |
| **41** | 4.1 V | **85** | 8.5 V | **B5** | 16.4 V | **E5** | 28.0 V | | |
| **42** | 4.2 V | **86** | 8.6 V | **B6** | 16.8 V | **E6** | 28.5 V | | |
| **43** | 4.3 V | **87** | 8.7 V | **B7** | 17.2 V | **E7** | 29.0 V | | |
| **44** | 4.4 V | **88** | 8.8 V | **B8** | 17.6 V | **E8** | 29.5 V | | |
| **45** | 4.5 V | **89** | 8.9 V | **B9** | 18.0 V | **E9** | 30.0 V | | |
| **46** | 4.6 V | **90** | 9.0 V | **C0** | 18.4 V | | | | |
| **47** | 4.7 V | **91** | 9.1 V | **C1** | 18.8 V | | | | |
| **48** | 4.8 V | **92** | 9.2 V | **C2** | 19.2 V | | | | |
| **49** | 4.9 V | **93** | 9.3 V | **C3** | 19.6 V | | | | |
| **50** | 5.0 V | **94** | 9.4 V | **C4** | 20.0 V | | | | |
| **51** | 5.1 V | **95** | 9.5 V | | | | | | |
| **52** | 5.2 V | **96** | 9.6 V | | | | | | |
| **53** | 5.3 V | **97** | 9.7 V | | | | | | |
| **54** | 5.4 V | **98** | 9.8 V | | | | | | |
| **55** | 5.5 V | **99** | 9.9 V | | | | | | |
| **56** | 5.6 V | **00** | 10.0 V | | | | | | |
| **57** | 5.7 V | | | | | | | | |
| **58** | 5.8 V | | | | | | | | |
| **59** | 5.9 V | | | | | | | | |
| **60** | 6.0 V | | | | | | | | |
| **61** | 6.1 V | | | | | | | | |

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**Table 12-1. Voltage Options (continued)**

| 100 mV STEPS | | | | 400 mV STEPS | | 500 mV STEPS | | 1 V STEPS | |
|---|---|---|---|---|---|---|---|---|---|
| NOMEN-CLATURE | VOLTAGE OPTIONS | NOMEN-CLATURE | VOLTAGE OPTIONS | NOMEN-CLATURE | VOLTAGE OPTIONS | NOMEN-CLATURE | VOLTAGE OPTIONS | NOMEN-CLATURE | VOLTAGE OPTIONS |
| **62** | 6.2 V | | | | | | | | |
| **63** | 6.3 V | | | | | | | | |
| **64** | 6.4 V | | | | | | | | |
| **65** | 6.5 V | | | | | | | | |
| **66** | 6.6 V | | | | | | | | |
| **67** | 6.7 V | | | | | | | | |
| **68** | 6.8 V | | | | | | | | |
| **69** | 6.9 V | | | | | | | | |

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.4 Trademarks

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### 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS3760A012DYYR | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A012 |
| TPS3760A012DYYR.A | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A012 |
| TPS3760A015DYYR | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A015 |
| TPS3760A015DYYR.A | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A015 |
| TPS3760E012DYYR | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | E012 |
| TPS3760E012DYYR.A | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | E012 |
| TPS3760E565DYYR | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | E565 |
| TPS3760E565DYYR.A | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | E565 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TPS3760 :**

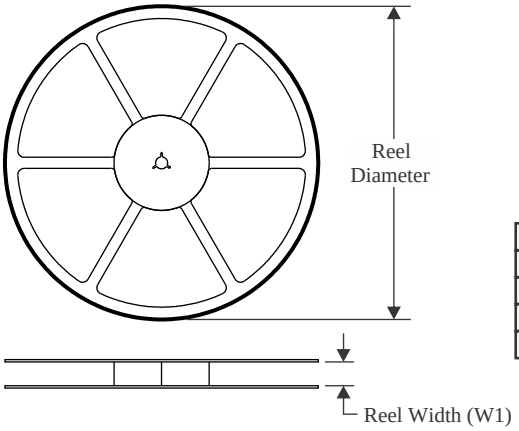
- Automotive : TPS3760-Q1

NOTE: Qualified Version Definitions:

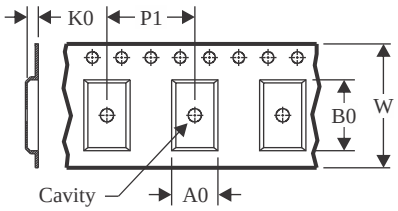
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

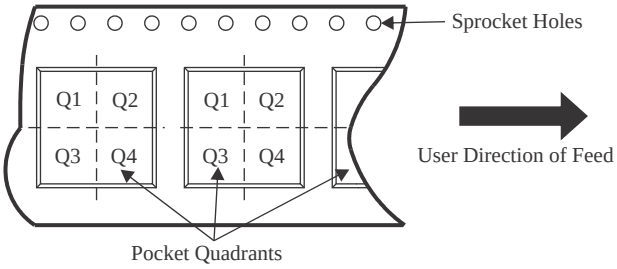



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

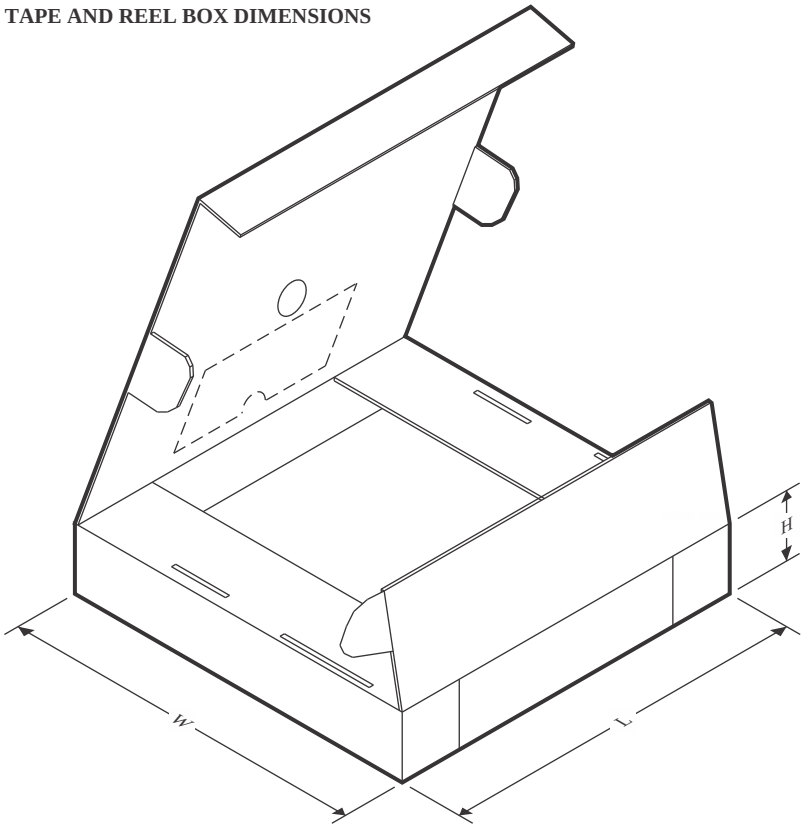
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

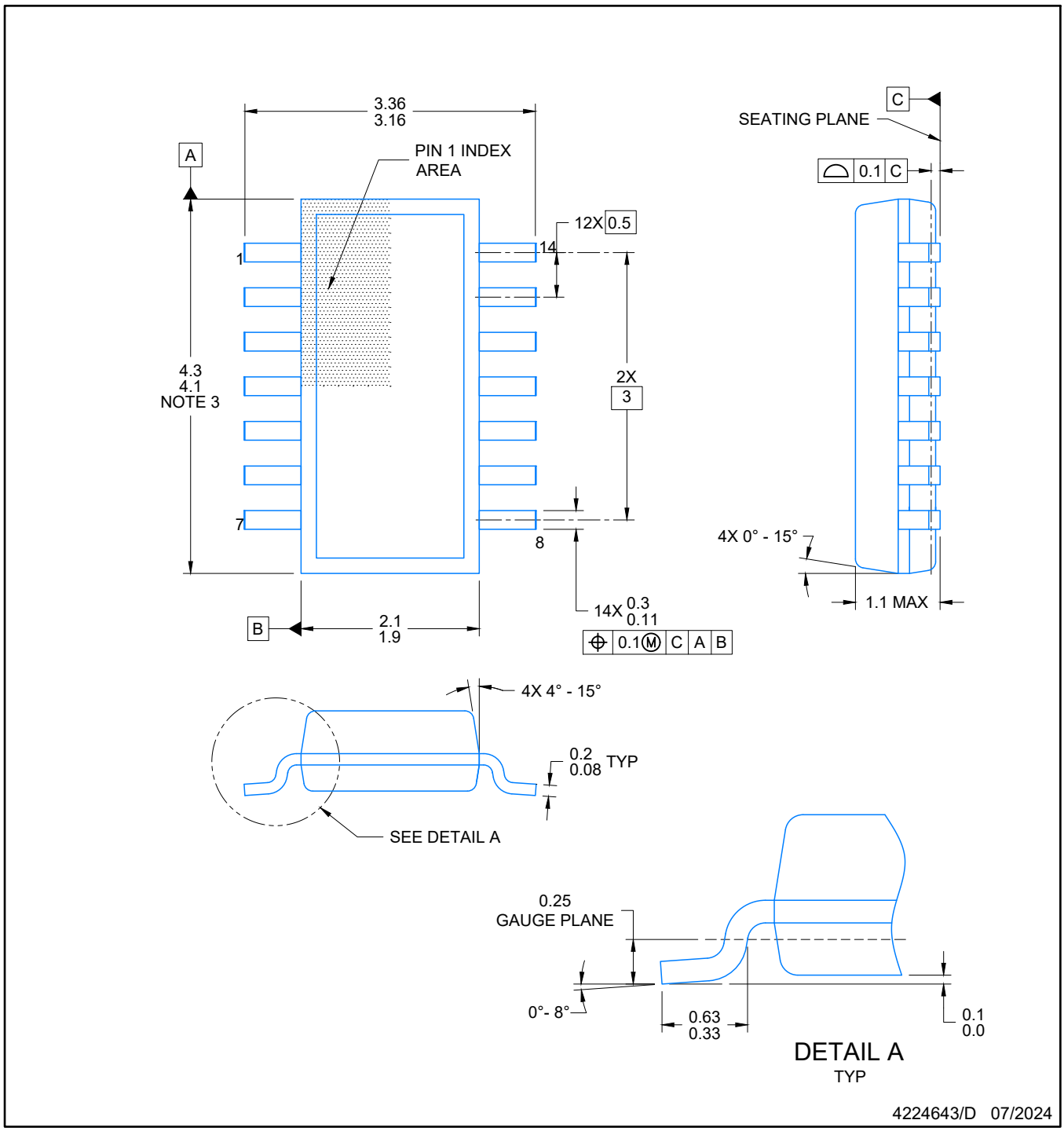
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3760A012DYYR | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| TPS3760A015DYYR | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| TPS3760E012DYYR | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| TPS3760E565DYYR | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS



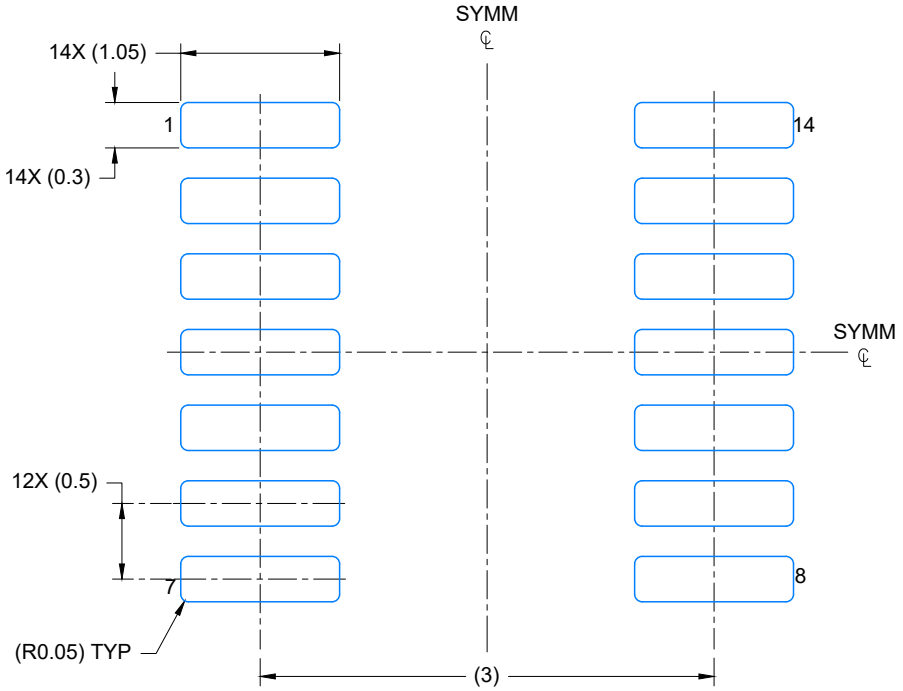

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS3760A012DYYR | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |
| TPS3760A015DYYR | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |
| TPS3760E012DYYR | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |
| TPS3760E565DYYR | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |

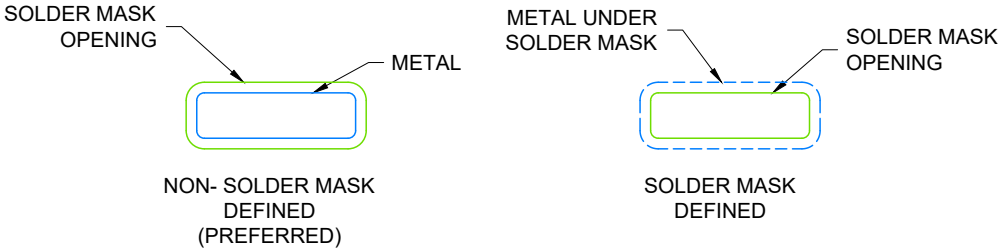



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




SOLDER MASK DETAILS

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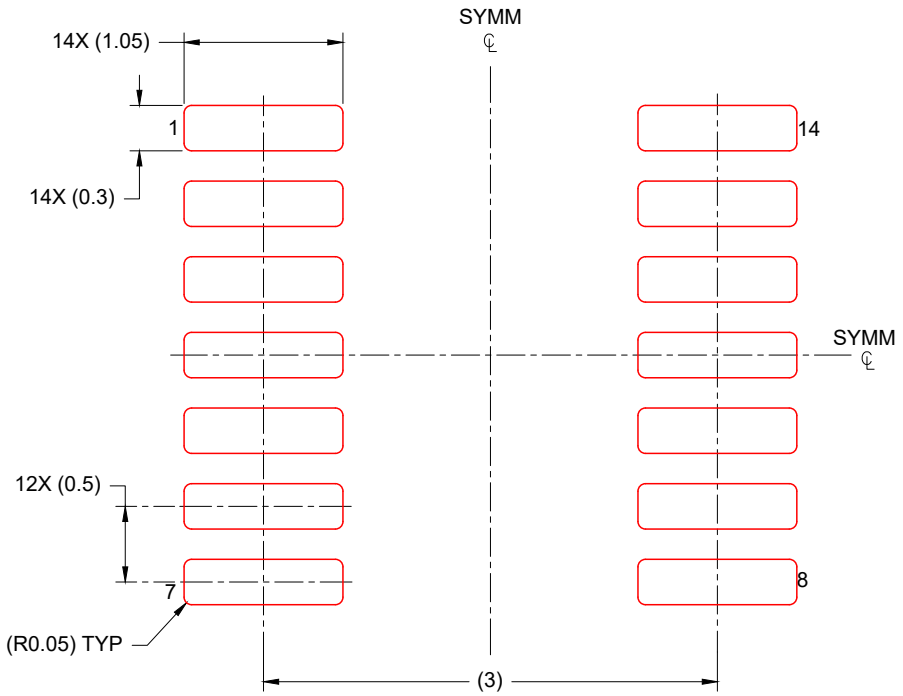
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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