

# TPS3700-Q1 Automotive High Voltage (18V) Window Voltage Detector With Internal Reference for Over and Undervoltage Monitoring

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
  - Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C6
- **Functional Safety-Capable**
  - [Documentation available to aid functional safety system design](#)
- Wide Supply Voltage Range: 1.8 V to 18 V
- Adjustable Threshold: Down to 400 mV
- Open-Drain Outputs for Overvoltage and Undervoltage Detection
- Low Quiescent Current: 5.5  $\mu\text{A}$  (typ)
- High Threshold Accuracy:
  - 1% Over Temperature
  - 0.25% (typ)
- Internal Hysteresis: 5.5 mV (typ)
- Available in ThinSOT23-6 and WSON Packages

## 2 Applications

- [Advanced Driver Assistance System \(ADAS\)](#)
- [ADAS Domain Controller](#)
- [Digital cockpit](#)
- [Automotive Infotainment & Cluster](#)
- [HEV/EV OBC and wireless charger](#)
- [Industrial Robot](#)

## 3 Description

The TPS3700-Q1 wide-supply window voltage detector operates over a 1.8 V to 18 V range. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The TPS3700-Q1 device can be used as a window voltage detector or as two independent voltage monitors; the monitored voltage can be set with the use of external resistors. For even wider input voltage capability up to 65 V, see the [TPS37A-Q1](#) or the [TPS38A-Q1](#) devices.

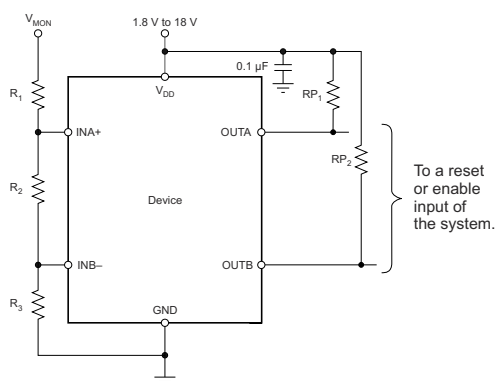
The OUTA terminal is driven low when the voltage at the INA+ terminal drops below  $(V_{IT+} - V_{hys})$ , and goes high when the voltage returns above the respective threshold  $(V_{IT+})$ . The OUTB terminal is driven low when the voltage at the INB– terminal rises above  $V_{IT+}$ , and goes high when the voltage drops below the respective threshold  $(V_{IT+} - V_{hys})$ . Both comparators in the TPS3700-Q1 device include built-in hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering.

The TPS3700-Q1 device is available in a Thin SOT-6 and a 1.5-mm x 1.5-mm WSON-6 package and is specified over the junction temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

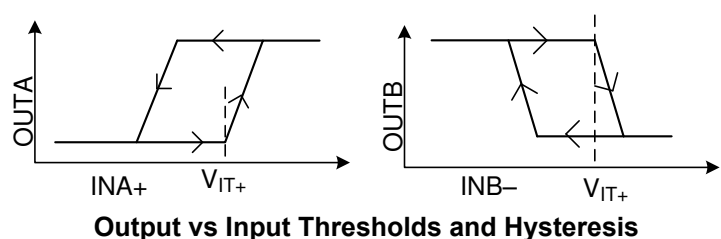
### Device Information

ORDER NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE
TPS3700-Q1	SOT23 (6)	2.90 mm x 1.60 mm
	WSON (6)	1.50 mm x 1.50 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Schematic**



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.2 Functional Block Diagram.....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	7.3 Feature Description.....	<b>9</b>
<b>3 Description</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>11</b>
<b>4 Revision History</b> .....	<b>2</b>	<b>8 Application and Implementation</b> .....	<b>12</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.1 Application Information.....	<b>12</b>
<b>6 Specifications</b> .....	<b>4</b>	8.2 Typical Application.....	<b>15</b>
6.1 Absolute Maximum Ratings.....	<b>4</b>	<b>9 Power Supply Recommendations</b> .....	<b>16</b>
6.2 ESD Ratings.....	<b>4</b>	<b>10 Layout</b> .....	<b>17</b>
6.3 Recommended Operating Conditions.....	<b>4</b>	10.1 Layout Guidelines.....	<b>17</b>
6.4 Thermal Information.....	<b>4</b>	10.2 Layout Example.....	<b>17</b>
6.5 Electrical Characteristics.....	<b>5</b>	<b>11 Device and Documentation Support</b> .....	<b>18</b>
6.6 Timing Requirements.....	<b>6</b>	11.1 Documentation Support.....	<b>18</b>
6.7 Timing Diagram .....	<b>6</b>	11.3 Electrostatic Discharge Caution.....	<b>18</b>
6.8 Switching Characteristics.....	<b>6</b>	11.4 Glossary.....	<b>18</b>
6.9 Typical Characteristics.....	<b>7</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>18</b>
<b>7 Detailed Description</b> .....	<b>9</b>		
7.1 Overview.....	<b>9</b>		

## 4 Revision History

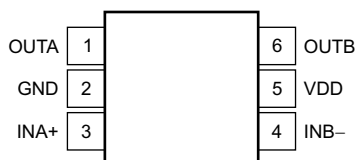
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (July 2017) to Revision C (March 2021)</b>	<b>Page</b>
• Added bullet for Functional Safety-Capable device.....	<b>1</b>
• Added links to TI.com applications pages.....	<b>1</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document, corrected part# to GPN in device information.....	<b>1</b>
• Moved Storage temperature range here in the Absolute Maximum Ratings from the section previously called handling ratings (which also included ESD ratings) when the ESD ratings section was updated per the latest format.....	<b>4</b>
• Corrected table formatting, descriptions and the notes in ESD Ratings section per the latest standards.....	<b>4</b>
• Corrected Input Voltage Max on INA+, INB- from 6 V to 6.5 V to match the device capability.....	<b>4</b>
• Added missing Thermal Information for the DSE package.....	<b>4</b>
• Added the missing max start-up delay spec and corrected corresponding note 2.....	<b>5</b>

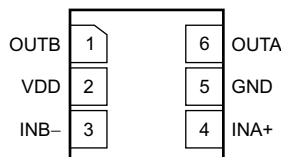
<b>Changes from Revision A (April 2014) to Revision B (July 2017)</b>	<b>Page</b>
• Added WSON Package to Device Information Table.....	<b>1</b>
• Added WSON Package to Pin Configuration and Function table .....	<b>3</b>

<b>Changes from Revision * (March 2014) to Revision A (April 2014)</b>	<b>Page</b>
• Changed device status from <i>Product Preview</i> to <i>Production Data</i> . .....	<b>1</b>

## 5 Pin Configuration and Functions



**Figure 5-1. DDC Package  
SOT-6  
Top View**



**Figure 5-2. DSE Package  
WSON-6  
Top View**

**Table 5-1. Pin Functions**

PIN			I/O	DESCRIPTION
NAME	DDC	DSE		
GND	2	5	—	Ground
INA+	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage ( $V_{IT+} - V_{HYS}$ ), OUTA is driven low.
INB-	4	3	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage ( $V_{IT+}$ ), OUTB is driven low.
OUTA	1	6	O	INA+ comparator open-drain output. OUTA is driven low when the voltage at this comparator is below ( $V_{IT+} - V_{HYS}$ ). The output goes high when the sense voltage returns above the respective threshold ( $V_{IT+}$ ).
OUTB	6	1	O	INB- comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds $V_{IT+}$ . The output goes high when the sense voltage returns below the respective threshold ( $V_{IT+} - V_{HYS}$ ).
VDD	5	2	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1- $\mu$ F ceramic capacitor close to this pin.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	V <sub>DD</sub>	−0.3	20	V
	OUTA, OUTB	−0.3	20	V
	INA+, INB−	−0.3	7	V
Current	Output terminal current		40	mA
Operating junction temperature, T <sub>J</sub>		−40	125	°C
Storage temperature range, T <sub>stg</sub>		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>ESD</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2500	V
		Charge device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage		1.8	18	V
V <sub>I</sub>	Input voltage	INA+, INB−	0	6.5	V
V <sub>O</sub>	Output voltage	OUTA, OUTB	0	18	V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS3700-Q1		UNIT
		DDC (SOT)	DSE (WSO)	
		6 pins	6 pins	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	174.0	160.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	81.5	101.9	
R <sub>θJB</sub>	Junction-to-board thermal resistance	47.2	68.8	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	22.0	5.4	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	46.9	68.6	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Over the operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , and  $1.8\text{ V} < V_{DD} < 18\text{ V}$ , unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$  and  $V_{DD} = 5\text{ V}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DD}$ Supply voltage range		1.8		18	V
$V_{(POR)}$ Power-on reset voltage <sup>(1)</sup>	$V_{OLmax} = 0.2\text{ V}$ , $I_{(OUTA/B)} = 15\text{ }\mu\text{A}$			0.8	V
$V_{IT+}$ Positive-going input threshold voltage	$V_{DD} = 1.8\text{ V}$	396	400	404	mV
	$V_{DD} = 18\text{ V}$	396	400	404	mV
$V_{IT-}$ Negative-going input threshold voltage	$V_{DD} = 1.8\text{ V}$	387	394.5	400	mV
	$V_{DD} = 18\text{ V}$	387	394.5	400	mV
$V_{hys}$ Hysteresis voltage ( $hys = V_{IT+} - V_{IT-}$ )			5.5	12	mV
$I_{(INA+)}$ Input current (at the INA+ or INB– terminal) $I_{(INB-)}$	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_I = 6.5\text{ V}$	–25	1	25	nA
	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_I = 0.1\text{ V}$	–15	1	15	nA
$V_{OL}$ Low-level output voltage	$V_{DD} = 1.3\text{ V}$ , $I_O = 0.4\text{ mA}$			250	mV
	$V_{DD} = 1.8\text{ V}$ , $I_O = 3\text{ mA}$			250	mV
	$V_{DD} = 5\text{ V}$ , $I_O = 5\text{ mA}$			250	mV
$I_{lk(OD)}$ Open-drain output leakage-current	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_O = V_{DD}$			300	nA
	$V_{DD} = 1.8\text{ V}$ , $V_O = 18\text{ V}$			300	nA
$I_{DD}$ Supply current	$V_{DD} = 1.8\text{ V}$ , no load		5.5	11	$\mu\text{A}$
	$V_{DD} = 5\text{ V}$		6	13	$\mu\text{A}$
	$V_{DD} = 12\text{ V}$		6	13	$\mu\text{A}$
	$V_{DD} = 18\text{ V}$		7	13	$\mu\text{A}$
Startup delay <sup>(2)</sup>			150	450	$\mu\text{s}$
UVLO Undervoltage lockout <sup>(4)</sup>	$V_{DD}$ falling	1.3		1.7	V

(1) The lowest supply voltage ( $V_{DD}$ ) at which output is active;  $t_{r(VDD)} > 15\text{ }\mu\text{s/V}$ . Below  $V_{(POR)}$ , the output cannot be determined.

(2) During power on,  $V_{DD}$  must exceed  $1.8\text{ V}$  for  $450\text{ }\mu\text{s}$  (max) before the output is in a correct state.

(3) High-to-low and low-to-high refers to the transition at the input terminals (INA+ and INB–).

(4) When  $V_{DD}$  falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined below  $V_{(POR)}$ .

## 6.6 Timing Requirements

Over operating temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
$t_{PHL}$	High-to-low propagation delay <sup>(3)</sup>	$V_{DD} = 5\text{ V}$ , 10-mV input overdrive, $R_P = 10\text{ k}\Omega$ , $V_{OH} = 0.9 \times V_{DD}$ , $V_{OL} = 400\text{ mV}$ See Figure 6-1		18		$\mu\text{s}$
$t_{PLH}$	Low-to-high propagation delay <sup>(3)</sup>	$V_{DD} = 5\text{ V}$ , 10-mV input overdrive, $R_P = 10\text{ k}\Omega$ , $V_{OH} = 0.9 \times V_{DD}$ , $V_{OL} = 400\text{ mV}$ See Figure 6-1		29		$\mu\text{s}$

## 6.7 Timing Diagram

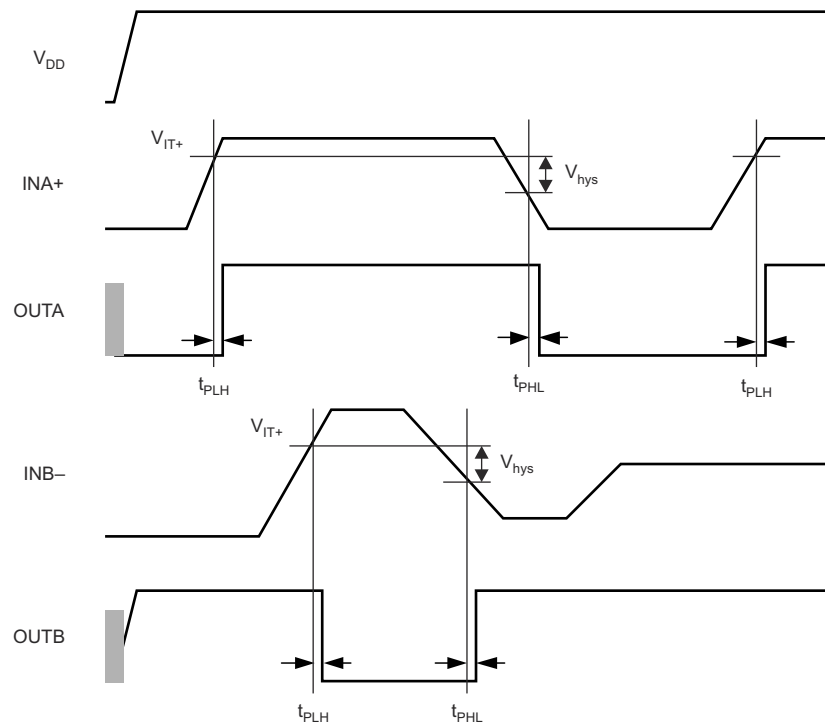


Figure 6-1. Timing Diagram

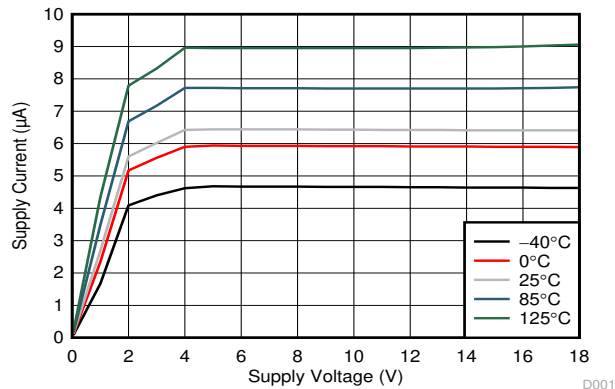
## 6.8 Switching Characteristics

Over operating temperature range (unless otherwise noted)

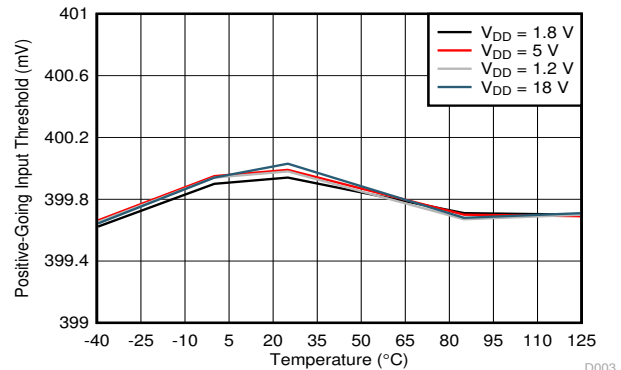
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output rise time $V_{DD} = 5\text{ V}$ , 10-mV input overdrive, $R_P = 10\text{ k}\Omega$ , $V_O = (0.1\text{ to }0.9) \times V_{DD}$		2.2		$\mu\text{s}$
$t_f$	Output fall time $V_{DD} = 5\text{ V}$ , 10-mV input overdrive, $R_P = 10\text{ k}\Omega$ , $V_O = (0.1\text{ to }0.9) \times V_{DD}$		0.22		$\mu\text{s}$

## 6.9 Typical Characteristics

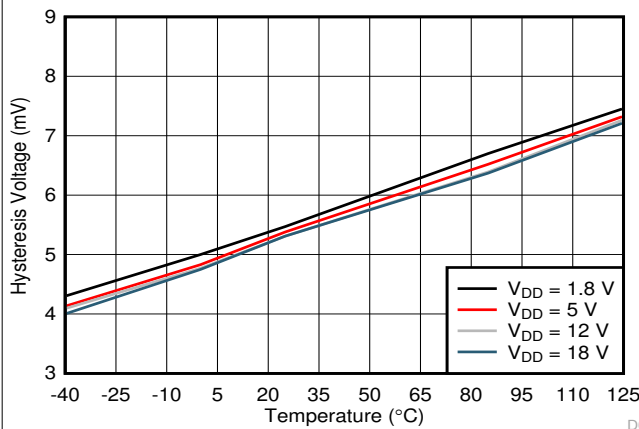
At  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$ , unless otherwise noted.



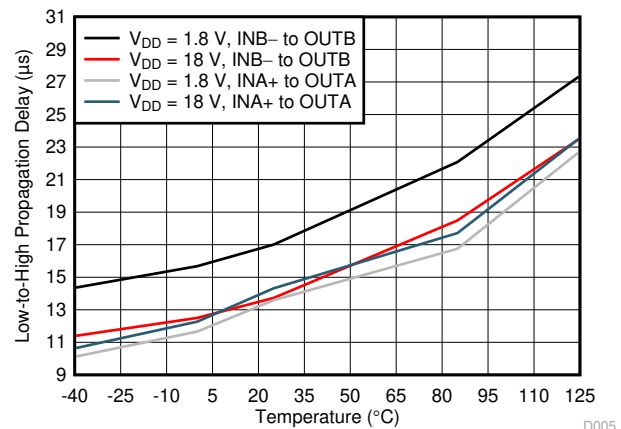
**Figure 6-2. Supply Current ( $I_{DD}$ ) vs Supply Voltage ( $V_{DD}$ )**



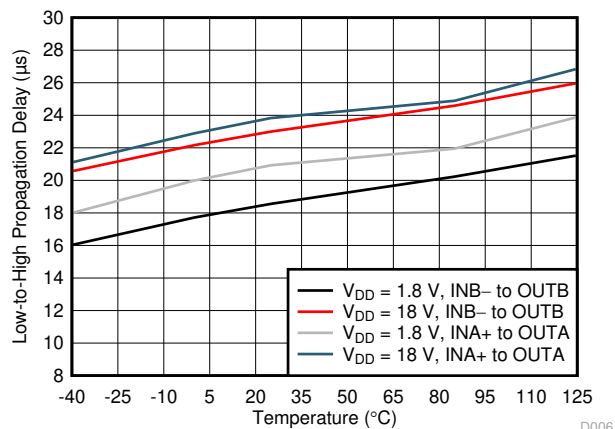
**Figure 6-3. Rising Input Threshold Voltage ( $V_{IT+}$ ) vs Temperature**



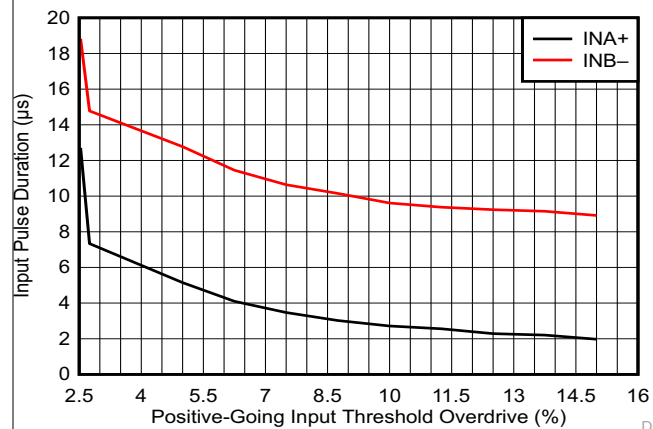
**Figure 6-4. Hysteresis ( $V_{hys}$ ) vs Temperature**



**Figure 6-5. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)**



**Figure 6-6. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)**



INA+ = negative spike below  $V_{IT-}$   
INB- = positive spike above  $V_{IT+}$

**Figure 6-7. Minimum Pulse Width vs Threshold Overdrive Voltage**

## 6.9 Typical Characteristics (continued)

At  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$ , unless otherwise noted.

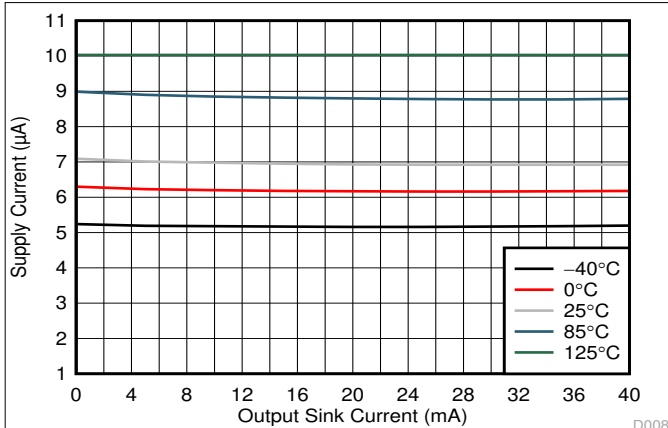


Figure 6-8. Supply Current ( $I_{DD}$ ) vs Output Sink Current

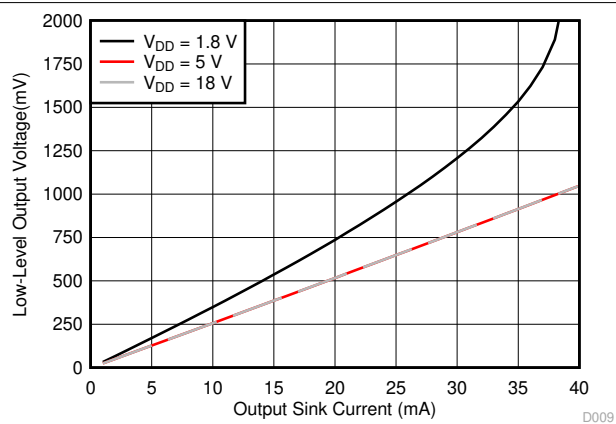


Figure 6-9. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $-40^\circ\text{C}$ )

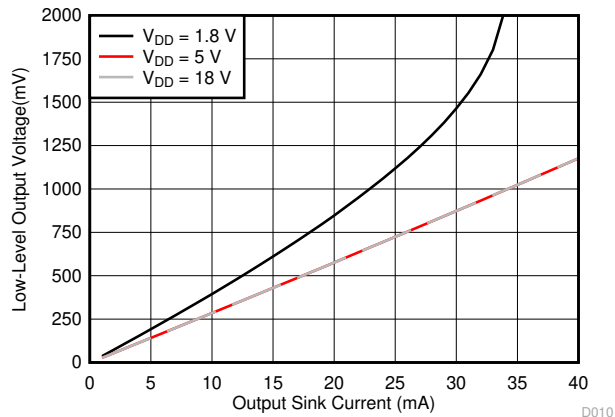


Figure 6-10. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $0^\circ\text{C}$ )

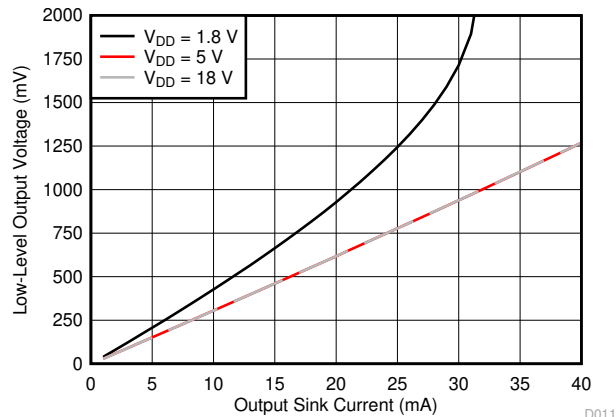


Figure 6-11. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $25^\circ\text{C}$ )

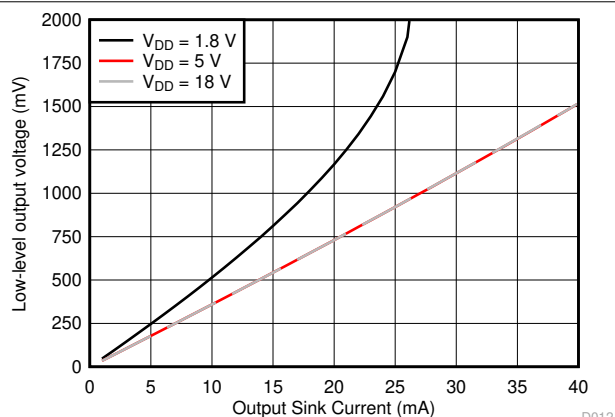


Figure 6-12. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $85^\circ\text{C}$ )

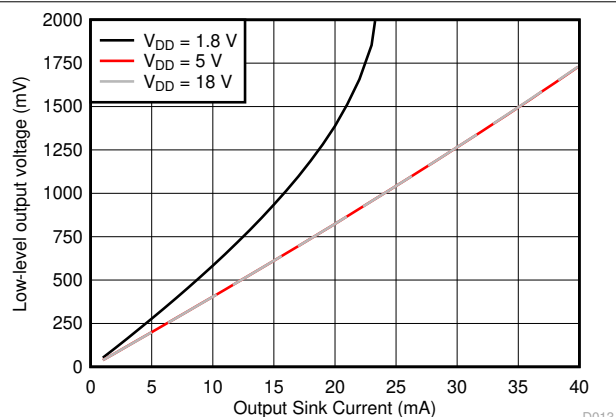


Figure 6-13. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $125^\circ\text{C}$ )

## 7 Detailed Description

### 7.1 Overview

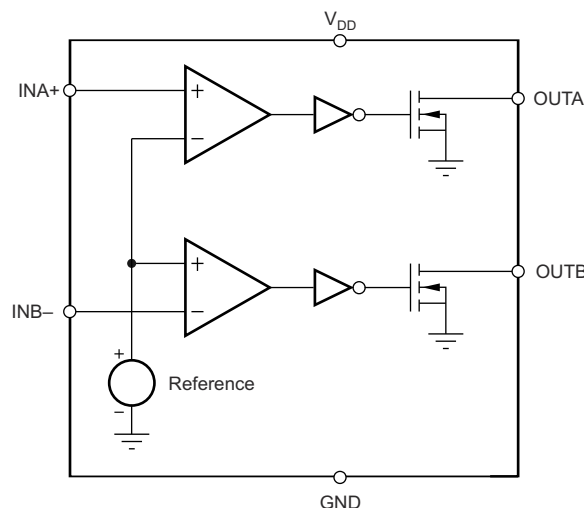
The TPS3700-Q1 device combines two comparators for overvoltage and undervoltage detection. The TPS3700-Q1 device is a wide-supply voltage range (1.8 to 18 V) device with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The outputs are also rated to 18 V and can sink up to 40 mA.

The TPS3700-Q1 device is designed to assert the output signals, as shown in Table 7-1. Each input terminal can be set to monitor any voltage above 0.4 V using an external resistor divider network. With the use of two input terminals of different polarities, the TPS3700-Q1 device forms a window voltage detector. Broad voltage thresholds can be supported that allow the device to be used in a wide array of applications.

**Table 7-1. TPS3700-Q1 Truth Table**

CONDITION	OUTPUT	STATUS
$INA+ > V_{IT+}$	OUTA high	Output A not asserted
$INA+ < V_{IT-}$	OUTA low	Output A asserted
$INB- > V_{IT+}$	OUTB low	Output B asserted
$INB- < V_{IT-}$	OUTB high	Output B not asserted

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Inputs (INA+, INB-)

The TPS3700-Q1 device combines two comparators. Each comparator has one external input (inverting and noninverting); the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to the reference voltage (400 mV). Both comparators also have a built-in falling hysteresis that makes the device less sensitive to supply rail noise and ensures stable operation.

The INA+ and INB- inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications in order to reduce sensitivity to transients and layout parasitics.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA+ voltage drops below  $(V_{IT+} - V_{hys})$ . When the voltage exceeds  $V_{IT+}$ , the output (OUTA) goes to a high-impedance state; see Figure 6-1.

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB- exceeds  $V_{IT+}$ . When the voltage drops below  $V_{IT+} - V_{hys}$  the output (OUTB) goes to a high-impedance state;

see [Figure 6-1](#). Together, these comparators form a window-detection function as discussed in the [Section 7.3.3](#) section.

### 7.3.2 Outputs (OUTA, OUTB)

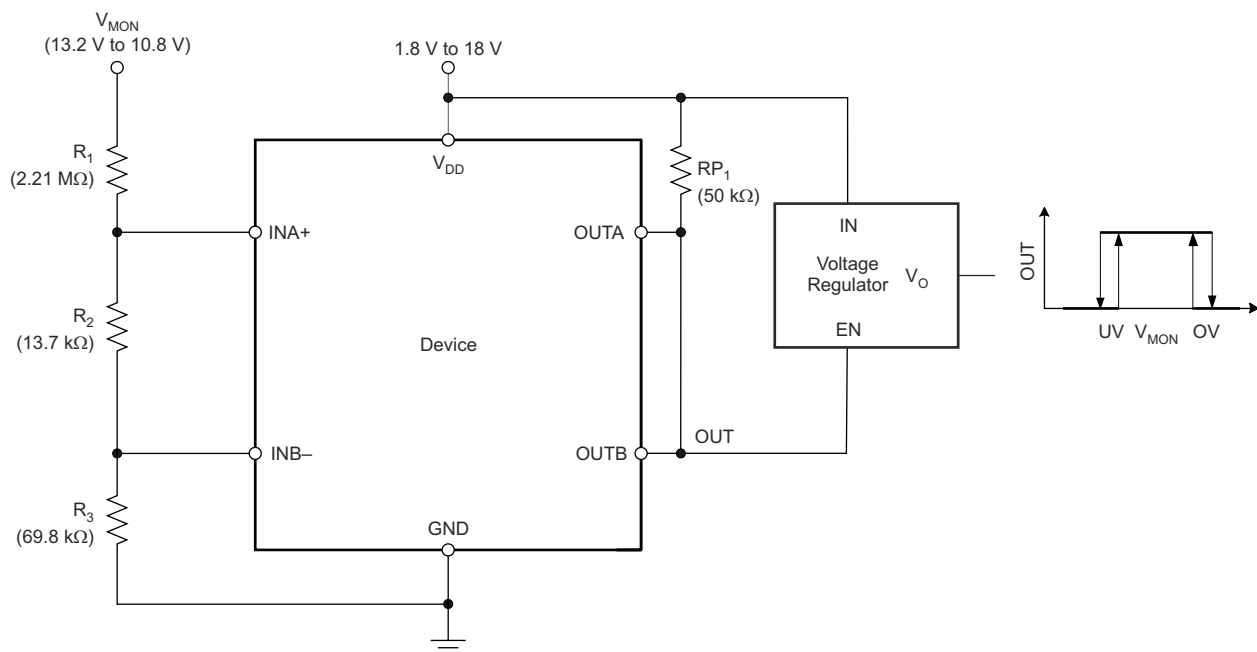
In a typical TPS3700-Q1 application, the outputs are connected to a reset or enable input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]) or the outputs are connected to the enable input of a voltage regulator (such as a DC-DC or low-dropout regulator [LDO]).

The TPS3700-Q1 device provides two open-drain outputs (OUTA and OUTB). Pullup resistors must be used to hold these lines high when the output goes to high impedance (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at the correct interface-voltage levels. The TPS3700-Q1 outputs can be pulled up to 18 V, independent of the device supply voltage. To ensure proper voltage levels, some thought should be given while choosing the pullup resistor values. The pullup resistor value is determined by  $V_{OL}$ , sink-current capability, and output-leakage current ( $I_{lk(OD)}$ ). These values are specified in the [Section 6.5](#) table. By using wired-AND logic, OUTA and OUTB can merge into one logic signal.

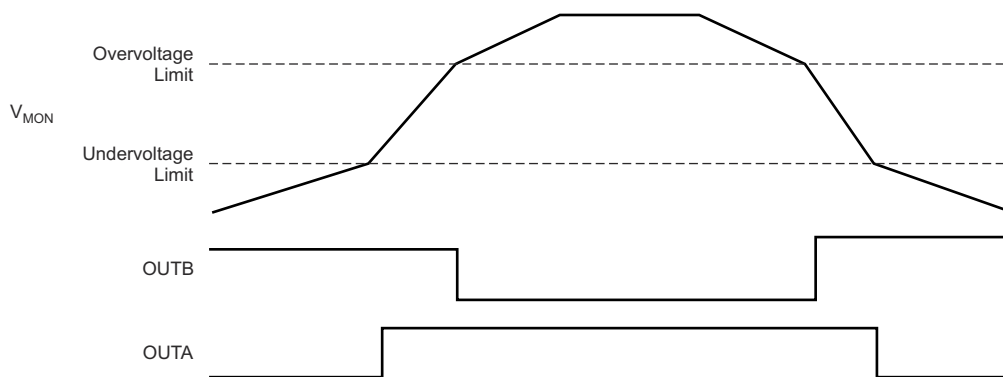
[Table 7-1](#) and the [Section 7.3.1](#) section describe how the outputs are asserted or de-asserted. See [Figure 6-1](#) for a timing diagram that describes the relationship between threshold voltages and the respective output.

### 7.3.3 Window Voltage Detector

The inverting and noninverting configuration of the comparators forms a window voltage detector circuit using a resistor divider network, as shown in [Figure 7-1](#) and [Figure 7-2](#). The input terminals can monitor any system voltage above 400 mV with the use of a resistor divider network. The INA+ and INB– terminals monitor for undervoltage and overvoltage conditions, respectively.



**Figure 7-1. Window Voltage Detector Block Diagram**



**Figure 7-2. Window Voltage Detector Timing Diagram**

### 7.3.4 Immunity to Input Terminal Voltage Transients

The TPS3700-Q1 device is relatively immune to short voltage transient spikes on the input terminals. Sensitivity to transients is dependent on both transient duration and amplitude; see the *Minimum Pulse Width vs Threshold Overdrive Voltage* curve (Figure 6-7) in the Section 6.9 section.

### 7.4 Device Functional Modes

The TPS3700-Q1 has a single functional mode, which is on when  $V_{DD}$  is greater than 1.8 V.

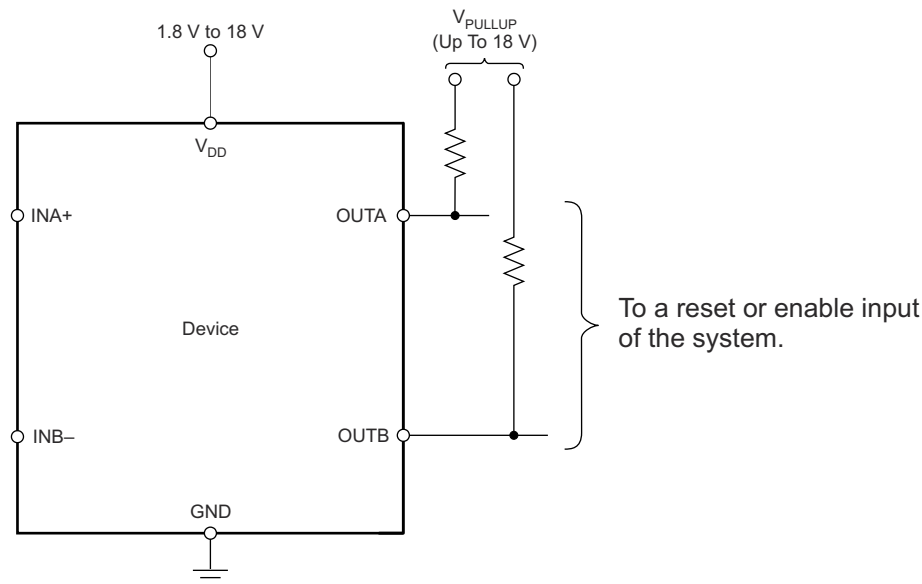
## 8 Application and Implementation

### 8.1 Application Information

The TPS3700-Q1 device is a wide-supply voltage window voltage detector that operates over a  $V_{DD}$  range of 1.8-V to 18-V. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The device can be used either as a window voltage detector or as two independent voltage monitors. The monitored voltages are set with the use of external resistors.

#### 8.1.1 $V_{PULLUP}$ to a Voltage Other Than $V_{DD}$

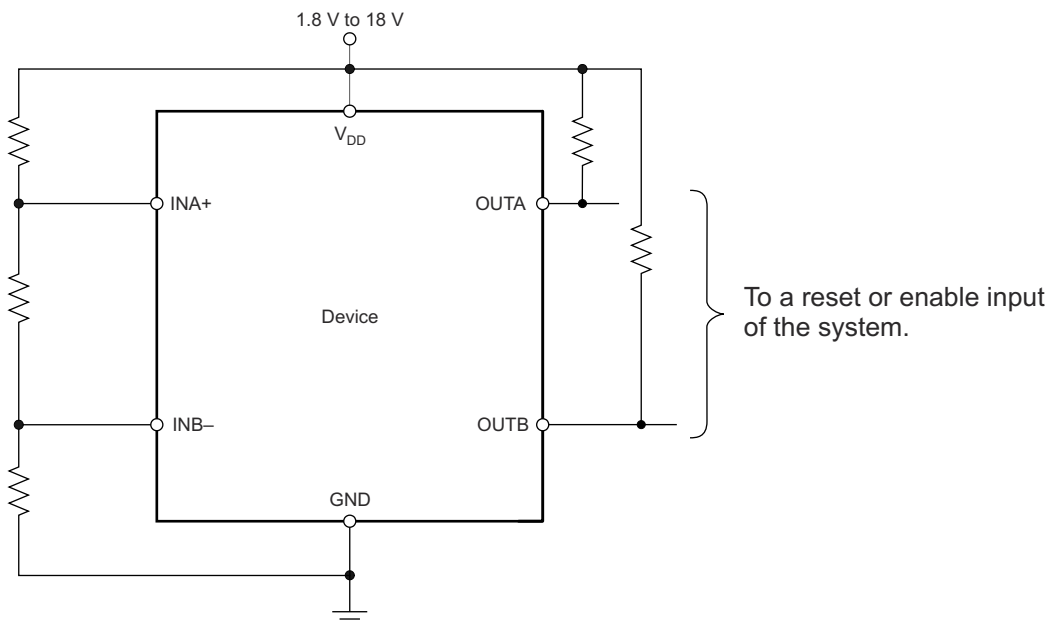
The outputs are often tied to  $V_{DD}$  through a resistor. However some applications may require the outputs to be pulled up to a higher or lower voltage than  $V_{DD}$  in order to correctly interface with the reset and enable the terminal of other devices.



**Figure 8-1. Interfacing to Voltages Other Than  $V_{DD}$**

### 8.1.2 Monitoring $V_{DD}$

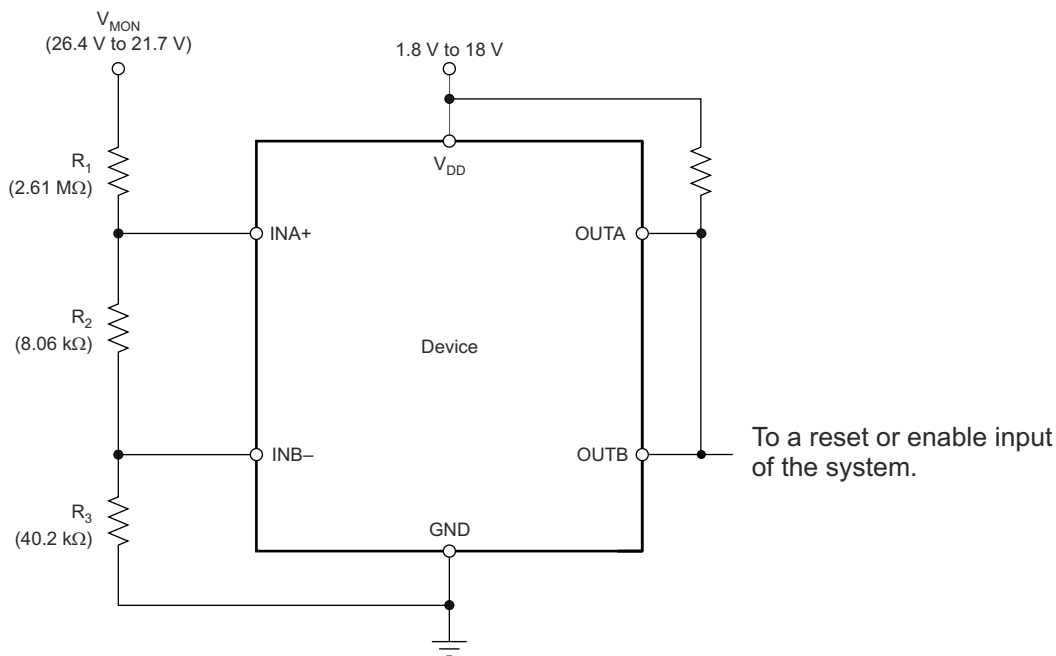
Many applications monitor the same rail that is powering  $V_{DD}$ . In these applications the resistor divider is simply connected to the  $V_{DD}$  rail.



**Figure 8-2. Monitoring the Same Voltage as  $V_{DD}$**

### 8.1.3 Monitoring a Voltage Other Than $V_{DD}$

Some applications monitor rails other than the one that is powering  $V_{DD}$ . In these types of applications the resistor divider used to set the desired thresholds is connected to the rail that is being monitored.

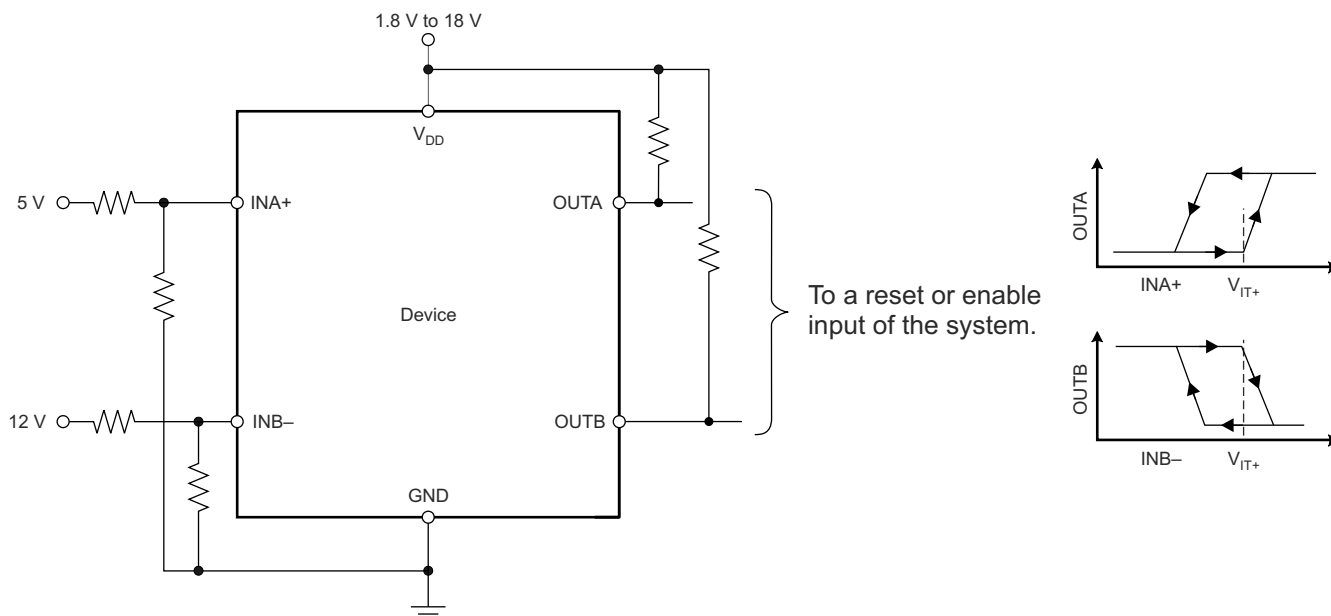


**NOTE:** The inputs can monitor a voltage higher than  $V_{DDmax}$  with the use of an external resistor divider network.

**Figure 8-3. Monitoring a Voltage Other Than  $V_{DD}$**

### 8.1.4 Monitoring Overvoltage and Undervoltage for Separate Rails

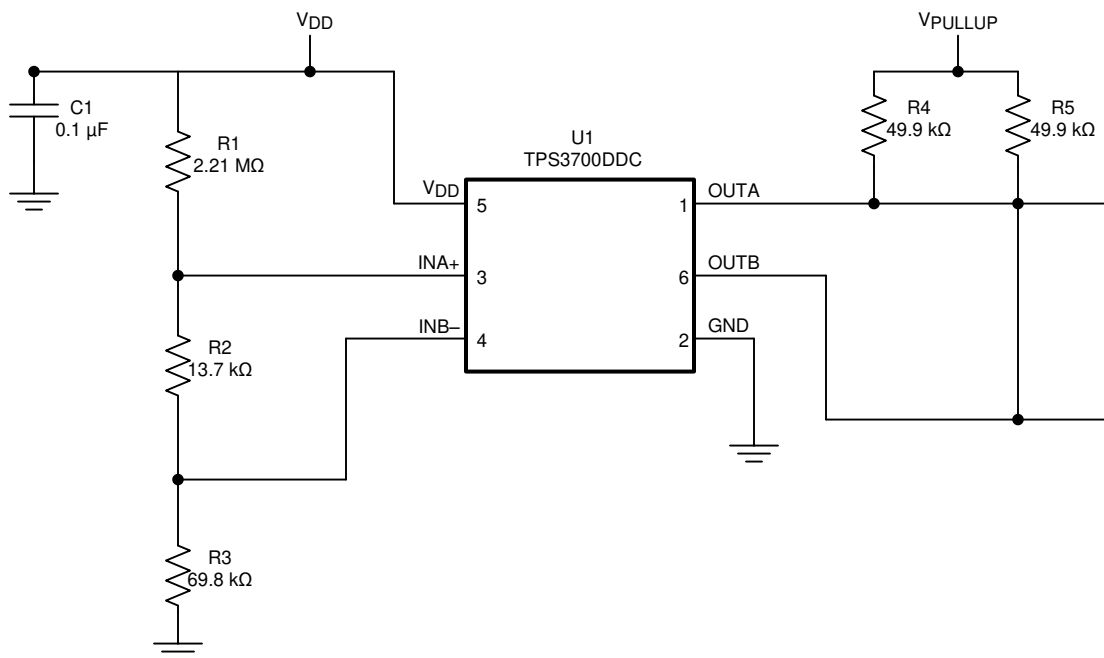
Some applications may want to monitor for overvoltage conditions on one rail while also monitoring for undervoltage conditions on a different rail. In those applications two independent resistor dividers will need to be used.



**NOTE:** In this case,  $OUTA$  is driven low when an undervoltage condition is detected at the 5-V rail and  $OUTB$  is driven low when an overvoltage condition is detected at the 12-V rail.

**Figure 8-4. Monitoring Overvoltage for One Rail and Undervoltage for a Different Rail**

## 8.2 Typical Application



**Figure 8-5. Typical Application Schematic**

### 8.2.1 Design Requirements

#### 8.2.1.1 Input Supply Capacitor

Although an input capacitor is not required for stability, connecting a 0.1-μF low equivalent series resistance (ESR) capacitor across the V<sub>DD</sub> terminal and GND terminal is good analog design practice. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

#### 8.2.1.2 Input Capacitors

Although not required in most cases, for extremely noisy applications, placing a 1-nF to 10-nF bypass capacitor from the comparator inputs (INA+, INB-) to the GND terminal is good analog design practice. This capacitor placement reduces device sensitivity to transients.

### 8.2.2 Detailed Design Procedure

Use [Equation 1](#) through [Equation 4](#) to calculate the resistor divider values and target threshold voltage.

$$R_T = R_1 + R_2 + R_3 \quad (1)$$

Select a value for R<sub>T</sub> such that the current through the divider is approximately 100-times higher than the input current at the INA+ and INB- terminals. The resistors can have high values to minimize current consumption as a result of low-input bias current without adding significant error to the resistive divider. See the application note *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for details on sizing input resistors.

Use [Equation 2](#) to calculate the value of R<sub>3</sub>.

$$R_3 = \frac{R_T}{V_{MON(OV)}} \times V_{IT+} \quad (2)$$

where

- V<sub>MON(OV)</sub> is the target voltage at which an overvoltage condition is detected

Use Equation 3 or Equation 4 to calculate the value of  $R_2$ .

$$R_2 = \left[ \frac{R_T}{V_{MON(\text{no UV})}} \times V_{IT+} \right] - R_3 \quad (3)$$

where

- $V_{MON(\text{no UV})}$  is the target voltage at which an undervoltage condition is removed as  $V_{MON}$  rises

$$R_2 = \left[ \frac{R_T}{V_{MON(\text{UV})}} \times (V_{IT+} - V_{hys}) \right] - R_3 \quad (4)$$

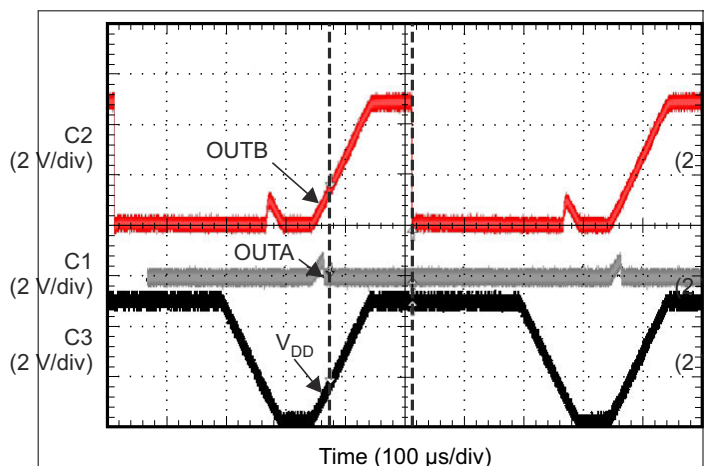
where:

$V_{MON(\text{UV})}$  is the target voltage at which an undervoltage condition is detected

•

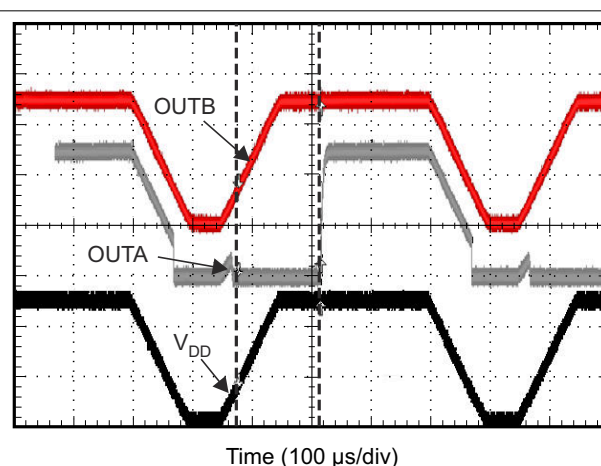
### 8.2.3 Application Curves

$T_J = 25^\circ\text{C}$



$V_{DD} = 5\text{ V}$     $V_{(INA+)} = 390\text{ mV}$     $V_{(INB-)} = 410\text{ mV}$

**Figure 8-6. Startup Delay (Outputs Pulled Up to  $V_{DD}$ )**



$V_{DD} = 5\text{ V}$     $V_{(INA+)} = 410\text{ mV}$     $V_{(INB-)} = 390\text{ mV}$

**Figure 8-7. Startup Delay (Outputs Pulled Up to  $V_{DD}$ )**

## 9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.8 V and 18 V.

## 10 Layout

### 10.1 Layout Guidelines

Placing a 0.1- $\mu$ F capacitor close to the  $V_{DD}$  terminal to reduce the input impedance to the device is good analog design practice. The pullup resistors can be separated if separate logic functions are needed (see [Figure 10-1](#)) or both resistors can be tied to a single pullup resistor if a logical AND function is desired.

### 10.2 Layout Example

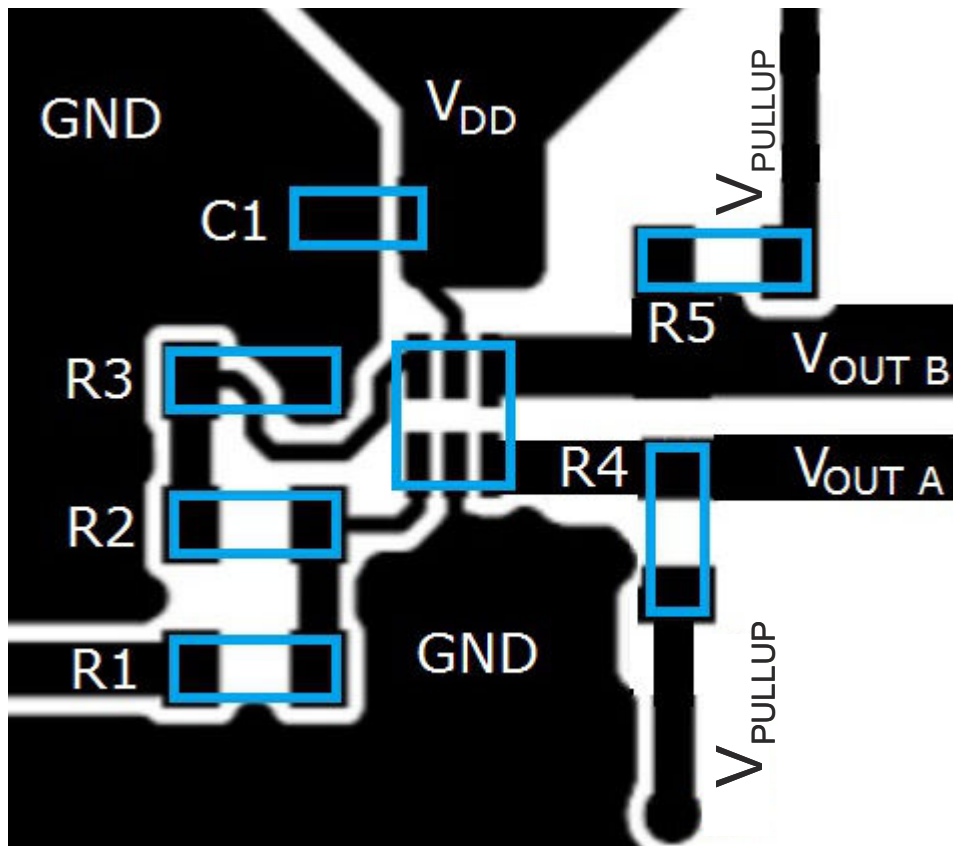


Figure 10-1. TPS3700-Q1 Layout Example

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- *Using the TPS3700 as a Negative Rail Over- and Undervoltage Detector*, [SLVA600](#)
- *Optimizing Resistor Dividers at a Comparator Input*, [SLVA450](#)
- *TPS3700EVM-114 Evaluation Module*, [SLVU683](#)

### 11.2 Trademarks

All trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS3700QDDCRQ1</a>	Active	Production	SOT-23-THIN (DDC)   6	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PD7Q
TPS3700QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC)   6	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PD7Q
<a href="#">TPS3700QDSERQ1</a>	Active	Production	WSON (DSE)   6	3000   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	5O
TPS3700QDSERQ1.A	Active	Production	WSON (DSE)   6	3000   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	5O
TPS3700QDSERQ1.B	Active	Production	WSON (DSE)   6	3000   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	5O

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

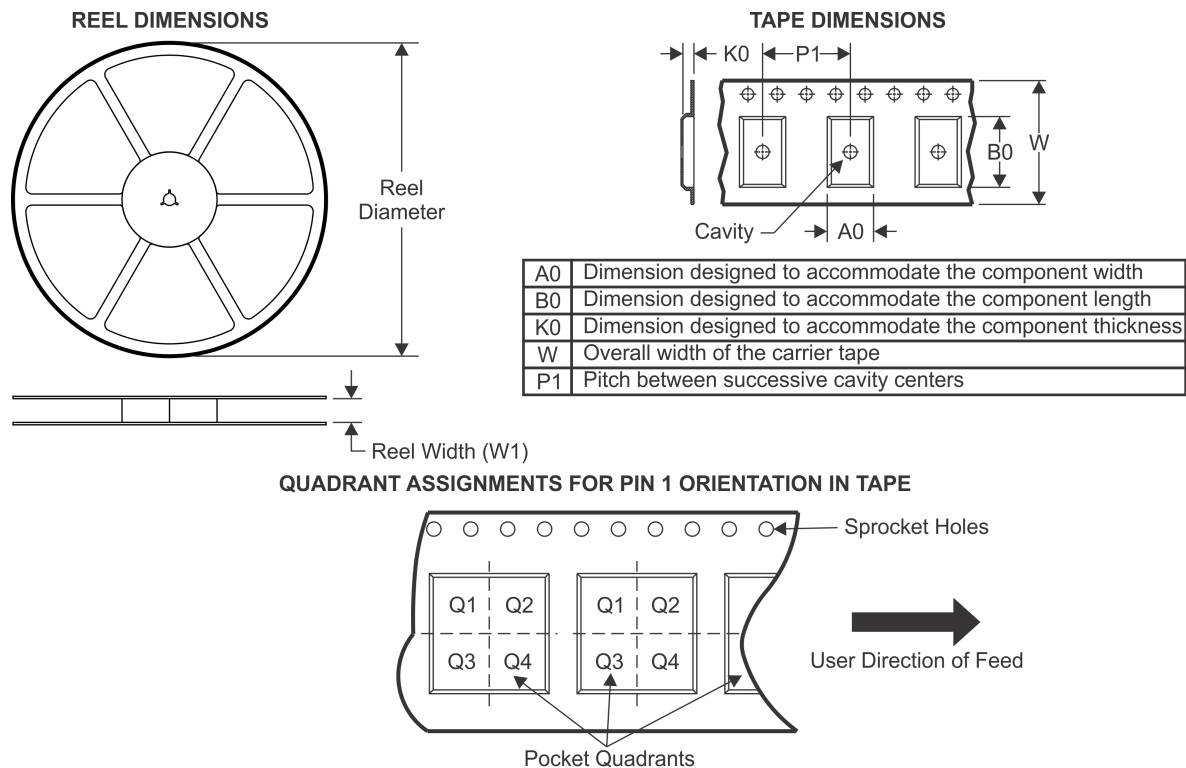
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS3700-Q1 :**

- Catalog : [TPS3700](#)

NOTE: Qualified Version Definitions:

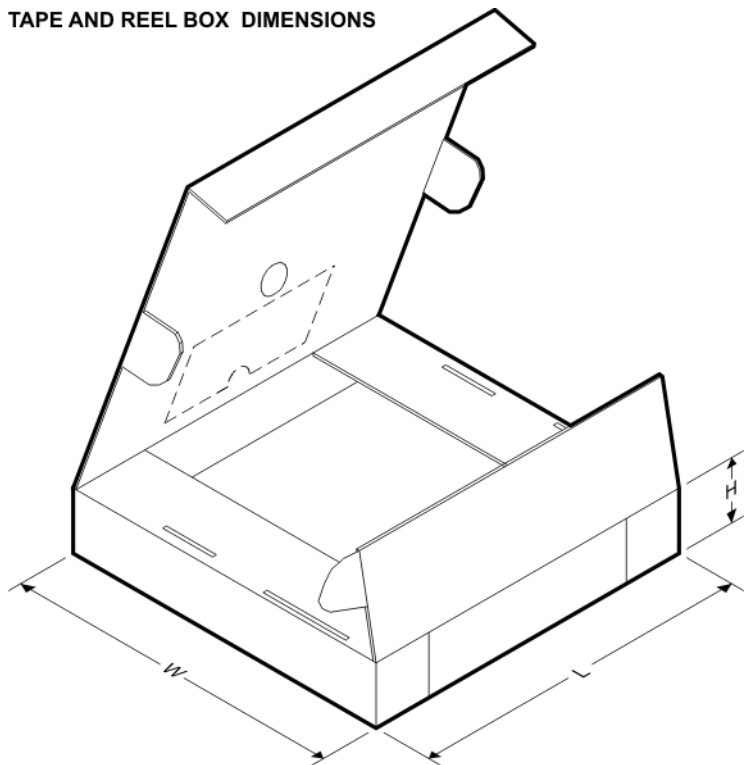
- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3700QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700QDSERQ1	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



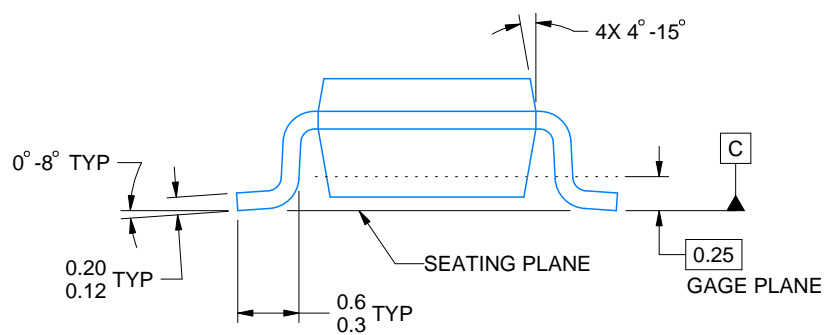
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3700QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3700QDSERQ1	WSON	DSE	6	3000	213.0	191.0	35.0



## SOT-23 - 1.1 max height

## SMALL OUTLINE TRANSISTOR



4214841/E 08/2024

NOTES:

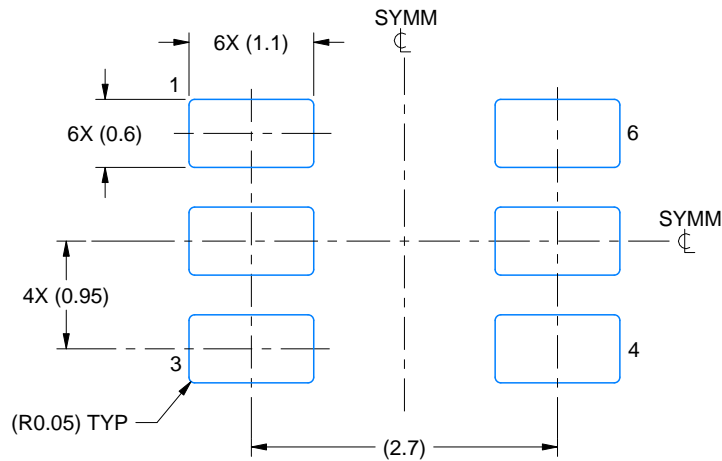
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

# EXAMPLE BOARD LAYOUT

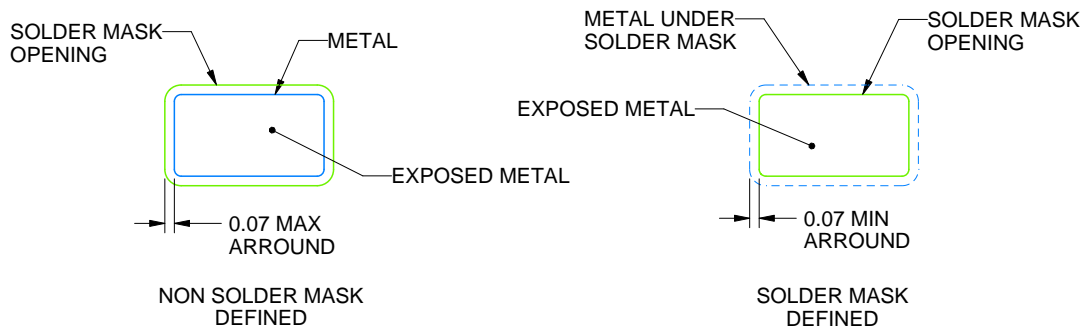
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X

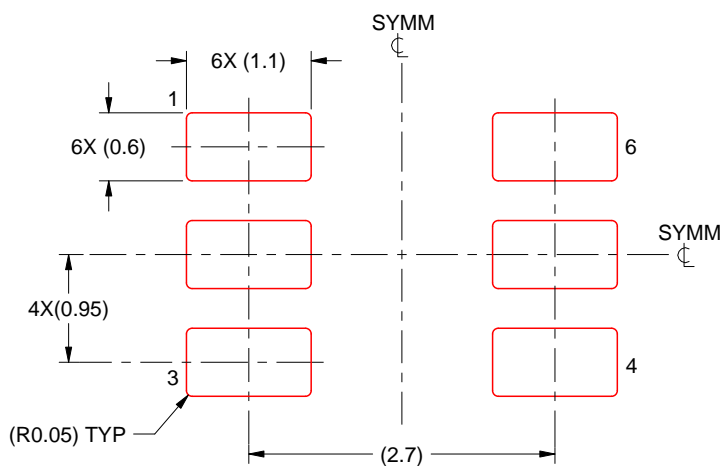


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



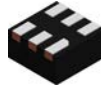
SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

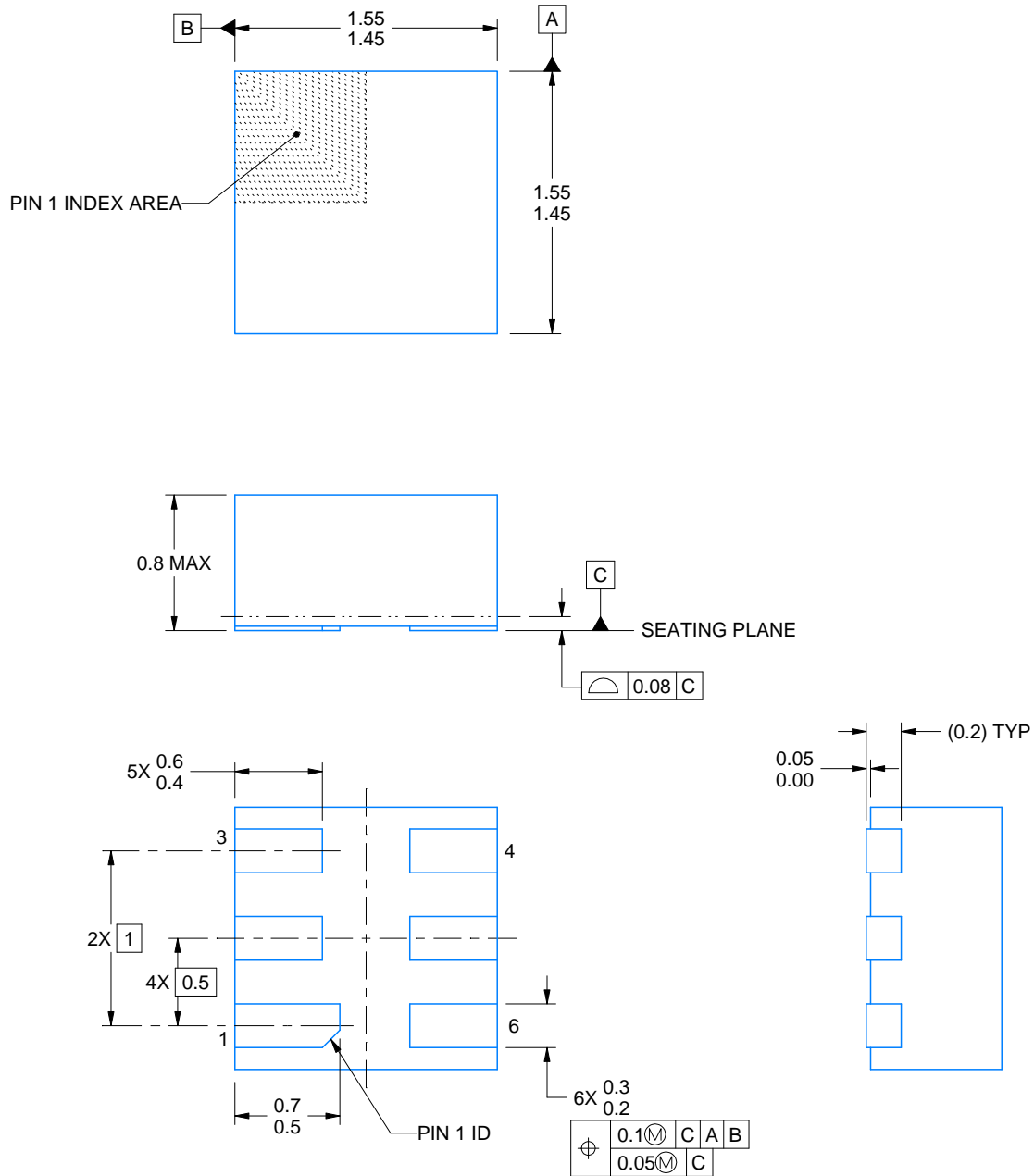
DSE0006A



# PACKAGE OUTLINE

## WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220552/B 01/2024

### NOTES:

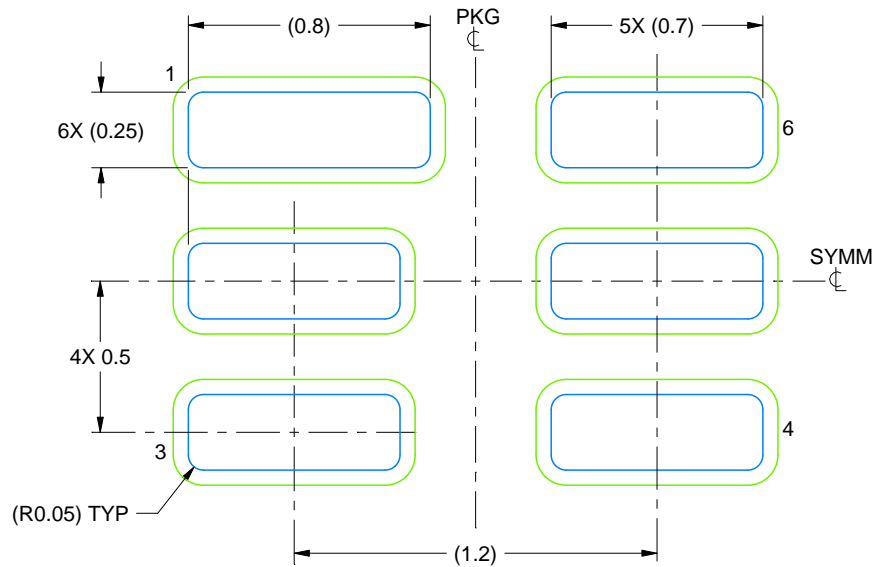
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

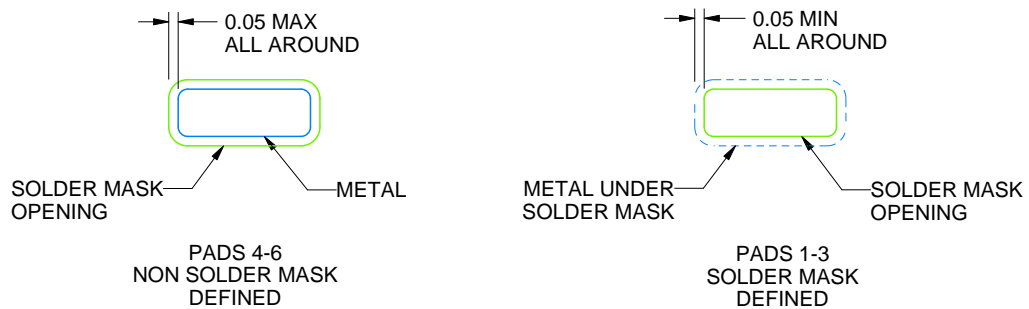
DSE0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

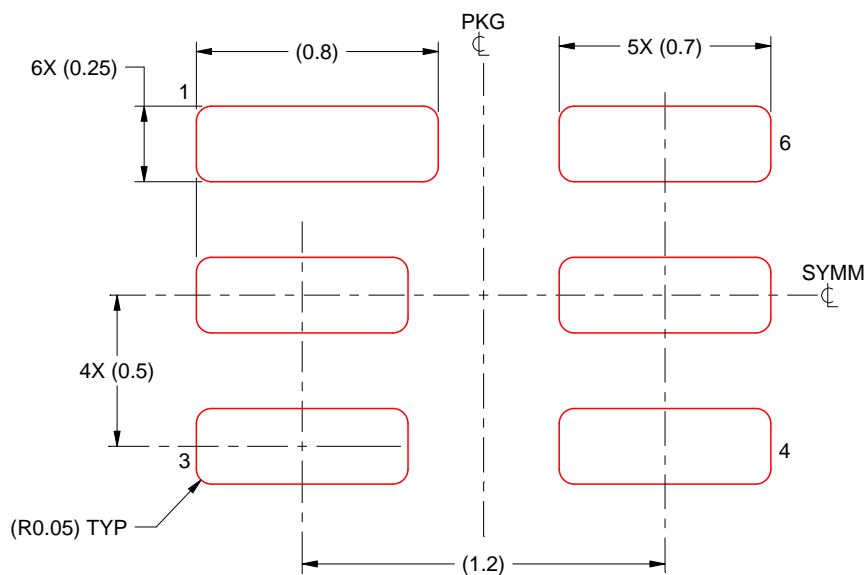
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

## EXAMPLE STENCIL DESIGN

DSE0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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