SLVS335C - DECEMBER 2000 - REVISED JANUARY 2007

### features

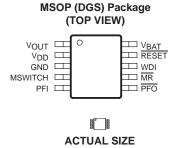
- Supply Current of 40 μA (Max)
- Precision 3.3-V Supply Voltage Monitor Other Voltage Options on Request
- Watchdog Timer With 800-ms Time-Out
- Backup-Battery Voltage Can Exceed V<sub>DD</sub>
- Power-On Reset Generator With Fixed
   100-ms Reset Delay Time
- Voltage Monitor for Power-Fail or Low-Battery Monitoring
- Manual Switchover to Battery-Backup Mode
- Manual Reset
- Battery Freshness Seal
- 10-Pin MSOP Package
- Temperature Range . . . −40°C to 85°C

# description

The TPS3606-33 supervisory circuit monitors and controls the processor activity. In case of powerfail or brownout conditions, the backup-battery switchover function of the TPS3606-33 allows a low-power processor and its peripherals to run from the installed backup battery without asserting a reset beforehand.

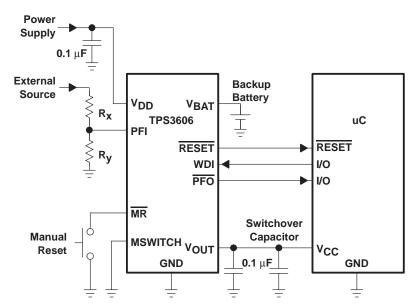
# typical applications

- Fax Machines
- Set-Top Boxes
- Advanced Voice Mail Systems
- Portable Battery Powered Equipment
- Computer Equipment
- Advanced Modems
- Automotive Systems
- Portable Long-Time Monitoring Equipment
- Point-of-Sale Equipment



3,05 mm x 4,98 mm

# typical operating circuit





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SLVS335C - DECEMBER 2000 - REVISED JANUARY 2007

# description (continued)

During power on,  $\overline{\text{RESET}}$  is asserted when the supply voltage (V<sub>DD</sub> or V<sub>BAT</sub>) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V<sub>OUT</sub> and keeps the  $\overline{\text{RESET}}$  output active as long as V<sub>OUT</sub> remains below the threshold voltage (V<sub>IT</sub>). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V<sub>OUT</sub> has risen above V<sub>IT</sub>. When the supply voltage drops below V<sub>IT</sub>, the output becomes active (low) again.

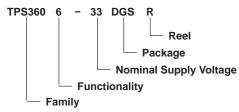
The TPS3606-33 is available in a 10-pin MSOP package and is characterized for operation over a temperature range of –40°C to 85°C.

### **PACKAGE INFORMATION**

TA	DEVICE NAME	MARKING
-40°C to 85°C	TPS3606-33DGSR <sup>†</sup>	AKE

<sup>&</sup>lt;sup>†</sup> The DGSR passive indicates tape and reel of 2500 parts.

# ordering information application specific versions (see Note)



DEVICE NAME	NOMINAL VOLTAGE <sup>‡</sup> , V <sub>NOM</sub>
TPS3606-33 DGS	3.3 V

For other threshold voltages, contact the local TI sales office for availability and lead-time.

# **FUNCTION TABLES TPS3606**

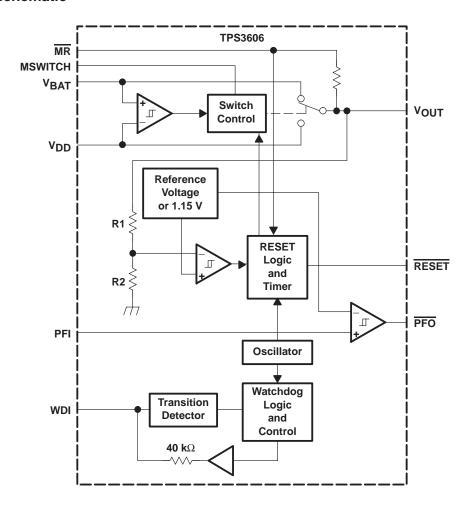
V <sub>DD</sub> > V <sub>SW</sub>	V <sub>OUT</sub> > V <sub>IT</sub>	V <sub>DD</sub> > V <sub>BAT</sub>	V <sub>OUT</sub>	RESET
0	0	0	VBAT	0
0	0	1	$V_{DD}$	0
0	1	0	$V_{BAT}$	1
0	1	1	$V_{DD}$	1
1	1	0	$V_{DD}$	1
1	1	1	$V_{DD}$	1

PFI > V <sub>PFI</sub>	PFO
0	0
1	1

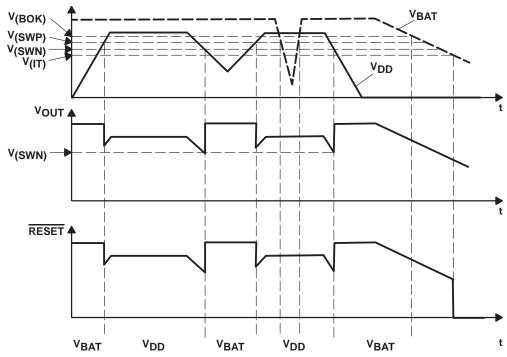
CONDITION .: VOUT > VDD(min)



# functional schematic



# timing diagram



NOTES: A. MSWITCH = 0,  $\overline{MR} = 1$ 

# **Terminal Functions**

TERMINAL			DECORPTION		
NAME	NO.	I/O	DESCRIPTION		
GND	3	I	Ground		
MR	7	I	Manual reset input		
MSWITCH	4	I	Manual switch to force device into battery-backup mode		
PFI	5	ı	Power-fail comparator input		
PFO	6	0	Power-fail comparator output		
RESET	9	0	Active-low reset output		
VBAT	10	- 1	Backup-battery input		
$V_{DD}$	2	- 1	Input supply voltage		
VOUT	1	0	Supply output		
WDI	8	I	Watchdog timer input		



SLVS335C - DECEMBER 2000 - REVISED JANUARY 2007

# detailed description

# battery freshness seal

The battery freshness seal of the TPS3606 family disconnects the backup battery from the internal circuitry until it is needed. This ensures that the backup battery connected to V<sub>BAT</sub> is fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

- Connect V<sub>BAT</sub> (V<sub>BAT</sub> > V<sub>BAT(min)</sub>)
- 2. Ground PFO
- 3. Connect PFI to V<sub>DD</sub> or PFI > V<sub>(PFI)</sub>
- 4. Connect V<sub>DD</sub> to power supply (V<sub>DD</sub> > V<sub>IT</sub>)
- 5. Ground MR
- 6. Power down V<sub>DD</sub>
- 7. The freshness seal mode is entered and pins  $\overline{PFO}$  and  $\overline{MR}$  can be disconnected.

The battery freshness seal mode is disabled by the positive-going edge of RESET when V<sub>DD</sub> is applied.

# power-fail comparator (PFI and PFO)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail input (PFI) is compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold ( $V_{(PFI)}$ ) of 1.15 V typical, the power-fail output (PFO) goes low. If it goes above  $V_{(PFI)}$  plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above  $V_{(PFI)}$ . The sum of both resistors should be about 1 M $\Omega$ , to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage.

If the power-fail comparator is unused, connect PFI to ground and leave PFO unconnected.

# backup-battery switchover

In the event of a brownout or power failure, it may be necessary to keep a processor running. If a backup battery is installed at  $V_{BAT}$ , the devices automatically connect the processor to backup power when  $V_{DD}$  fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than  $V_{DD}$ , this family of supervisors does not connect  $V_{BAT}$  to  $V_{OUT}$  when  $V_{BAT}$  is greater than  $V_{DD}$ .  $V_{BAT}$  only connects to  $V_{OUT}$  (through a 2- $\Omega$  switch) when  $V_{OUT}$  falls below  $V_{(SWN)}$  and  $V_{BAT}$  is greater than  $V_{DD}$ . When  $V_{DD}$  recovers, switchover is deferred either until  $V_{DD}$  crosses  $V_{BAT}$ , or when  $V_{DD}$  rises above the threshold ( $V_{(SWP)}$ ).

V <sub>DD</sub> > V <sub>BAT</sub>	V <sub>DD</sub> > V <sub>(SWN)</sub>	V <sub>OUT</sub>
1	1	$V_{DD}$
1	0	$V_{DD}$
0	1	$V_{DD}$
0	0	V <sub>BAT</sub>



# detailed description (continued)

# manual switchover (MSWITCH)

While operating in the normal mode from  $V_{DD}$ , the device can be manually forced to operate in the battery-backup mode by connecting MSWITCH to  $V_{DD}$ . The table below shows the different switchover modes.

	MSWITCH	Status
Vde	GND	V <sub>DD</sub> mode
V <sub>DD</sub> mode	$V_{DD}$	Switch to battery-backup mode
Dattemy backup made	GND	Battery-backup mode
Battery-backup mode	$V_{DD}$	Battery-backup mode

If the manual switchover feature is not used, MSWITCH must be connected to ground.

# watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure the correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or the DSP has to toggle the watchdog input within typically 0.8 s to avoid a time-out from occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected, the watchdog is disabled and is retriggered internally.

# saving current while using the watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead, WDI is externally driven high for the majority of the time-out period, a current of e.g. 5 V/40  $k\Omega \approx 125 \,\mu\text{A}$  can flow into WDI.

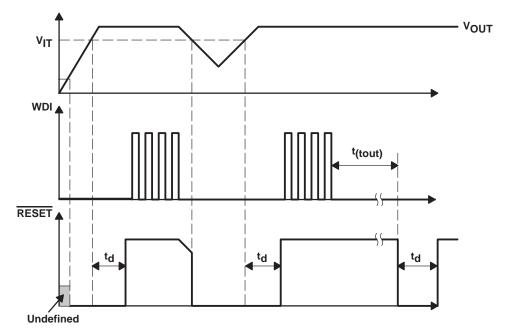


Figure 1. Watchdog Timing



# TPS3606-33 BATTERY-BACKUP SUPERVISOR FOR LOW-POWER PROCESSORS

SLVS335C - DECEMBER 2000 - REVISED JANUARY 2007

# absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V <sub>DD</sub> (see Note1)	7 V
MR, WDI, and PFI pins (see Note 1)	$-0.3 \text{ V to } (V_{DD} + 0.3 \text{ V})$
Continuous output current at V <sub>OUT</sub> : I <sub>O</sub>	300 mA
All other pins, IO	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T <sub>A</sub>	–40°C to 85°C
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### **DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> < 25°C	DERATING FACTOR	T <sub>A</sub> = 70°C	T <sub>A</sub> = 85°C
	POWER RATING	ABOVE T <sub>A</sub> = 25°C	POWER RATING	POWER RATING
DGS	424 mW	3.4 mW/°C	271 mW	220 mW

# recommended operating conditions at specified temperature range

	I	MIN	MAX	UNIT
Supply voltage, V <sub>DD</sub>		1.65	5.5	V
Battery supply voltage, VBAT		1.5	5.5	V
Input voltage, V <sub>I</sub>		0	V <sub>O</sub> + 0.3	V
High-level input voltage, VIH		0.7 x V <sub>O</sub>		V
Low-level input voltage, all other pins, V <sub>IL</sub>			0.3 x V <sub>O</sub>	V
Continuous output current at V <sub>OUT</sub> , I <sub>O</sub>			200	mA
Input transition rise and fall rate at WDI, MSWITCH, $\Delta t/\Delta V$			100	ns/V
Slew rate at V <sub>DD</sub> or V <sub>BAT</sub>			34	mV/μs
Operating free-air temperature range, TA		-40	85	°C



NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000h continuously.

# TPS3606-33 BATTERY-BACKUP SUPERVISOR FOR LOW-POWER PROCESSORS

SLVS335C - DECEMBER 2000 - REVISED JANUARY 2007

# electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER			NDITIONS	MIN	TYP	MAX	UNIT	
				V <sub>OUT</sub> = 2 V,	$I_{OH} = -400  \mu A$	V <sub>OUT</sub> – 0.2 V			
,,		RESET	V <sub>OUT</sub> = 3.3 V V <sub>OUT</sub> = 5 V,		V <sub>OUT</sub> – 0.4 V			V	
VOH	High-level output voltage		$V_{OUT} = 1.8 V,$	$I_{OH} = -20  \mu A$	V <sub>OUT</sub> – 0.3 V			V	
		PFO		$I_{OH} = -80 \mu\text{A}$ $I_{OH} = -120 \mu\text{A}$	V <sub>OUT</sub> – 0.4 V				
		RESET	$V_{OUT} = 2 V$ ,	$I_{OL} = 400  \mu A$			0.2		
VOL	Low-level output voltage	PFO	V <sub>OUT</sub> = 3.3 V, V <sub>OUT</sub> = 5 V,				0.4	V	
V <sub>res</sub>	Power-up reset voltage (see Note 2)		V <sub>BAT</sub> > 1.1 V V <sub>DD</sub> > 1.4 V,				0.4	V	
	Normal mode		$I_O = 5 \text{ mA},$	V <sub>DD</sub> = 1.8 V	V <sub>DD</sub> – 50 mV				
			$I_O = 75 \text{ mA},$	$V_{DD} = 3.3 \text{ V}$	V <sub>DD</sub> – 150 mV				
Vout			$I_O = 150 \text{ mA},$	$V_{DD} = 5 V$	V <sub>DD</sub> – 250 mV			V	
	Battery-backup mode		$I_O = 4 \text{ mA},$	$V_{BAT} = 1.5 V$	V <sub>BAT</sub> – 50 mV				
			$I_0 = 75 \text{ mA},$	$V_{BAT} = 3.3 V$	V <sub>BAT</sub> – 150 mV				
T-1- ()	V <sub>DD</sub> to V <sub>OUT</sub> on-resistant	e	$V_{DD} = 3.3 \text{ V}$			1	2	Ω	
<sup>r</sup> ds(on)	V <sub>BAT</sub> to V <sub>OUT</sub> on-resistar	ice	$V_{BAT} = 3.3 V$			1	2	32	
VIT	Negative-going input threshold voltage (see Notes 3 and 4)	TPS3606x33			2.87	2.93	2.99	V	
V <sub>(PFI)</sub>	Power-fail input threshold voltage	PFI			1.13	1.15	1.17		
V <sub>(SWN)</sub>	Battery switch threshold vonegative-going VOUT	ltage			V <sub>IT</sub> + 1%	V <sub>IT</sub> + 2%	V <sub>IT</sub> + 3.2%	V	

NOTES: 2. The lowest supply voltage at which  $\overline{\text{RESET}}$  becomes active.  $t_{\Gamma(VDD)} \ge 15 \,\mu\text{s/V}$ .

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1  $\mu$ F) should be placed near the supply terminal.

4. Voltage is sensed at VOUT

5. For details on how to optimize current consumption when using WDI refer to section detailed description.



# TPS3606-33 BATTERY-BACKUP SUPERVISOR FOR LOW-POWER PROCESSORS

SLVS335C - DECEMBER 2000 - REVISED JANUARY 2007

# electrical characteristics over recommended operating conditions (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS	MIN TYP	MAX	UNIT	
			1.65 V < V <sub>IT</sub> < 2.5 V	20	1		
		∨ <sub>IT</sub>	2.5 V < V <sub>IT</sub> < 3.5 V	40	1		
			3.5 V < V <sub>IT</sub> < 5.5 V	50	1		
V <sub>hys</sub>	Hysteresis	VPFI		12		mV	
			1.65 V < V <sub>(SWN)</sub> < 2.5 V	85			
		V(SWN)	2.5 V < V <sub>(SWN)</sub> < 3.5 V	100	l		
		,	3.5 V < V <sub>(SWN)</sub> < 5.5 V	110	l		
1	LPak Lava Parast assument	WDI	$WDI = V_{DD} = 5.5 V$		150	μΑ	
ΊΗ	High-level input current	MR	$\overline{MR} = 0.7 \times V_{DD}, V_{DD} = 5 \text{ V}$	-33	-76		
		WDI	$WDI = 0 V$ , $V_{DD} = 5 V$		-150		
IIL	Low-level input current	MR	$\overline{MR} = 0 \text{ V}, \qquad V_{DD} = 5 \text{ V}$	-110	-255		
II	Input current	PFI, MSWITCH	V <sub>I</sub> < V <sub>DD</sub>	-25	25	nA	
			PFO = 0 V, V <sub>DD</sub> = 1.8 V		-0.3		
los	Short-circuit current	PFO	PFO = 0 V, V <sub>DD</sub> = 3.3 V		-1.1	mA	
			PFO = 0 V, V <sub>DD</sub> = 5 V		-2.4		
I	V cumply ourront		$V_{OUT} = V_{DD}$		40	^	
l <sub>DD</sub>	V <sub>DD</sub> supply current		V <sub>OUT</sub> = V <sub>BAT</sub>		8	μΑ	
	M. sometiment		V <sub>OUT</sub> = V <sub>DD</sub>	-0.1	0.1		
I(BAT)	V <sub>BAT</sub> supply current		V <sub>OUT</sub> = V <sub>BAT</sub>		40	μΑ	
Ci	Input capacitance		V <sub>I</sub> = 0 V to 5 V		5	pF	

# timing requirements at RL = 1 M $\Omega$ , CL = 50 pF, TA = -40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
		$V_{DD}$	$V_{IH} = V_{IT} + 0.2 \text{ V},  V_{IL} = V_{IT} - 0.2 \text{ V}$	5			μs
t <sub>w</sub>	Pulse width	MR	V V 00VV 00 V V 07 V	400			
		WDI	$V_{DD} > V_{IT} + 0.2 \text{ V}, V_{IL} = 0.3 \text{ x } V_{DD}, V_{IH} = 0.7 \text{ x } V_{DD}$	100	100		ns

# switching characteristics at R<sub>L</sub>= 1 M $\Omega$ , C<sub>L</sub> = 50 pF, T<sub>A</sub> = -40°C to 85°C

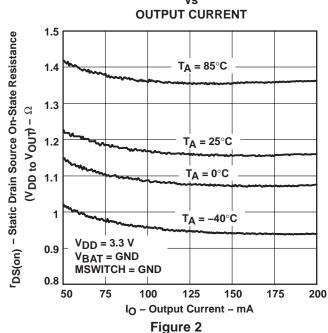
	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
td	Delay time		$V_{DD} \ge V_{IT} + 0.2 \text{ V},$ $\overline{\text{MR}} \ge 0.7 \text{ x V}_{DD},$ See timing diagram	60	100	140	ms
t(tout)	Watchdog time-out		V <sub>DD</sub> > V <sub>IT</sub> + 0.2 V, See timing diagram	0.48	0.8	1.12	S
		V <sub>DD</sub> to RESET	$V_{IL} = V_{IT} - 0.2 \text{ V}, \qquad V_{IH} = V_{IT} + 0.2 \text{ V}$		2	5	μs
	Propagation (delay) time,	PFI to PFO	$V_{IL} = V_{(PFI)} - 0.2 \text{ V},  V_{IH} = V_{(PFI)} + 0.2 \text{ V}$		3	5	μs
PHL	high-to-low-level output	MR to RESET	$V_{DD} \ge V_{IT} + 0.2 \text{ V}, \qquad V_{IL} = 0.3 \text{ x } V_{DD},$ $V_{IH} = 0.7 \text{ x } V_{DD}$		0.1	1	μs
	Transition time	V <sub>DD</sub> to V <sub>BAT</sub>	$V_{IL} = V_{(BAT)} - 0.2 \text{ V}, \ V_{IH} = V_{(BAT)} + 0.2 \text{ V}$ $V_{(BAT)} < V_{IT}$	,		3	μs



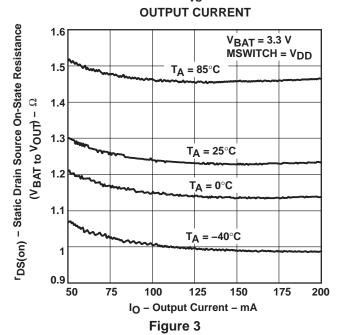
# **Table of Graphs**

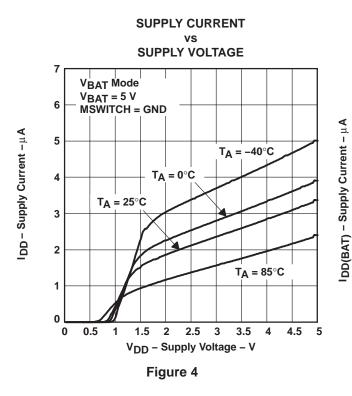
			FIGURE
	Static drain-source on-state resistance (V <sub>DD</sub> to V <sub>OUT</sub> )	vs Output current	2
rDS(on)	Static drain-source on-state resistance (VBAT to VOUT)	vs Output current	3
	Complex company	vs Supply voltage	4
IDD	Supply current	vs Battery supply	5
VIT	Input threshold voltage at RESET	vs Free-air temperature	6
V	High-level output voltage at RESET	and Park Land and and annual	7, 8
VOH	High-level output voltage at PFO	vs High-level output current	9, 10
VOL	Low-level output voltage at RESET	vs Low-level output current	11, 12
	Minimum pulse duration at V <sub>DD</sub>	vs Threshold voltage overdrive at V <sub>DD</sub>	13
	Minimum pulse duration at PFI	vs Threshold voltage overdrive at PFI	14

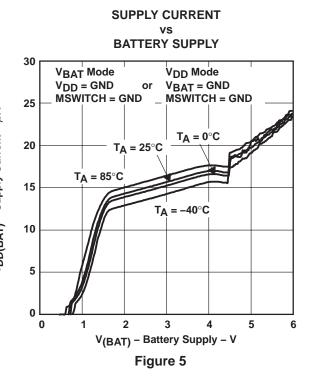
# STATIC DRAIN SOURCE ON-STATE RESISTANCE (V<sub>DD</sub> TO V<sub>OUT</sub>) vs



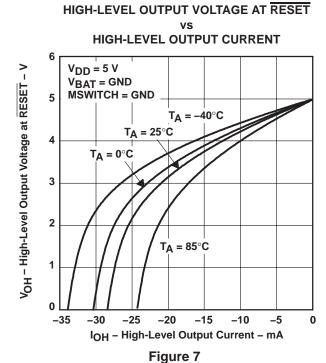
# STATIC DRAIN SOURCE ON-STATE RESISTANCE $(V_{BAT} TO V_{OUT})$



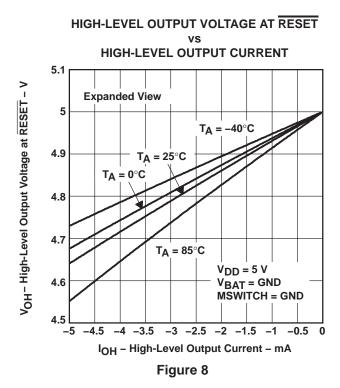


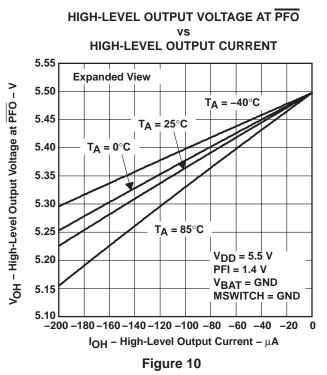


# INPUT THRESHOLD VOLTAGE AT RESET VS FREE-AIR TEMPERATURE 1.001 0.999 0.999 0.998 0.995 -40 -30 -20 -10 0 10 20 30 40 50 60 70 80 TA - Free-Air Temperature - °C Figure 6

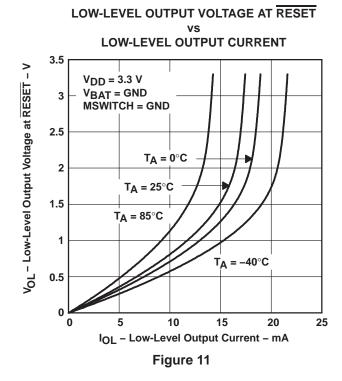


TEXAS

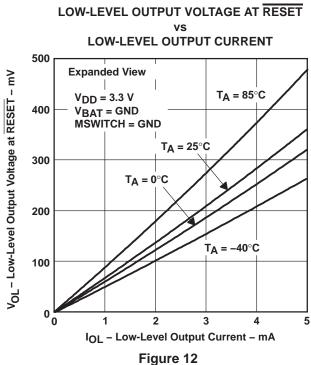


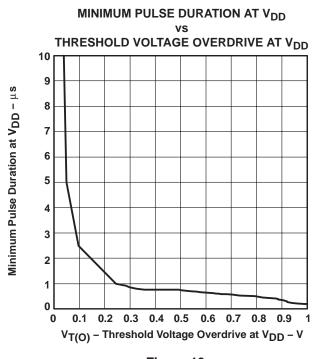


# HIGH-LEVEL OUTPUT VOLTAGE AT PFO **HIGH-LEVEL OUTPUT CURRENT** V<sub>OH</sub> - High-Level Output Voltage at PFO - V 5 $T_A = -40^{\circ}C$ T<sub>A</sub> = 25°C $T_A = 0^{\circ}C$ 3 T<sub>A</sub> = 85°C 2 V<sub>DD</sub> = 5.5 V PFI = 1.4 V V<sub>BAT</sub> = GND MSWITCH = GND -2.5 -2 -1.5-1 -0.5 IOH - High-Level Output Current - mA Figure 9









# Figure 13

# MINIMUM PULSE DURATION AT PFI THRESHOLD VOLTAGE OVERDRIVE AT PFI 5 $V_{DD} = 1.65 \text{ V}$ 4.6 Minimum Pulse Duration at PFI – $\mu$ s 4.2 3.8 3.4 3 2.6 2.2 1.8 1.4 1 0.6 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 V<sub>T(O)</sub> - Threshold Voltage Overdrive at PFI - V Figure 14



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# PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
TPS3606-33DGS	Active	Production	VSSOP (DGS)   10	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKE
TPS3606-33DGS.A	Active	Production	VSSOP (DGS)   10	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKE
TPS3606-33DGSR	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKE
TPS3606-33DGSR.A	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKE

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# PACKAGE MATERIALS INFORMATION

www.ti.com 3-Aug-2017

# TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



# \*All dimensions are nominal

Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3606-33DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 3-Aug-2017



### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3606-33DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0



SMALL OUTLINE PACKAGE



# NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187, variation BA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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