TPS2HCS08-Q1 8.9mΩ, Automotive Dual-Channel, SPI Controlled High-Side Switch With Integrated I2T Wire Protection and Low Power Mode

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C5
  - Withstands 36V load dump
- Dual-channel SPI controlled smart high-side switch with integrated nFETs.
- Integrated wire-harness protection without MCU involvement and a SPI programmable fuse curve
  - Protection against persistent overload condition
- Improve system level reliability through SPI programmable adjustable overcurrent protection
- SPI configurable capacitive charging mode to drive a wide range of capacitive input ECUs load current needs.
- Low quiescent current, low power ON-state to supply always-ON loads with automatic wake on load current increase with wake signal to MCU
- Robust integrated output protection:
  - Integrated thermal protection
  - Protection against short-to-ground
  - Protection against reverse battery events including automatic switch on of FET with reverse supply voltage
  - Automatic shut off on loss of battery and ground
  - Integrated output clamp to demagnetize inductive loads
- Digital sense output via SPI can be configured to measure:
  - Load current accurately with integrated ADC
  - Output or supply voltage, FET temperature
- Provides full fault diagnostics through SPI interface and indication through FLT pin
  - Detection of open load and short-to-battery

2 Applications

- Automotive zone ECU
- Power distribution modules
- Body control modules

3 Description

The TPS2HCS08-Q1 device is a dual channel, smart high-side switch controlled through a serial peripheral interface (SPI) and is intended for power distribution and actuator drive applications. The device integrates robust protection to ensure output wire and load protection against short circuit or overload conditions. The device features overcurrent protection configurable via SPI with sufficient flexibility to support loads that require large inrush currents and provide improved protection. The device also integrates a programmable fuse profile (current versus time) that turns off the switch under persistent overload condition. The two features together allow optimization of the wire harness for any load profile with full protection.

The device supports a SPI-configurable capacitive charging mode for ECU loads in power distribution switch applications. The device also includes two low power mode (LPM) states, an auto entry mode or a manual entry mode, that enables the device to provide current to the load ECU while only consuming about 10–20µA of current.

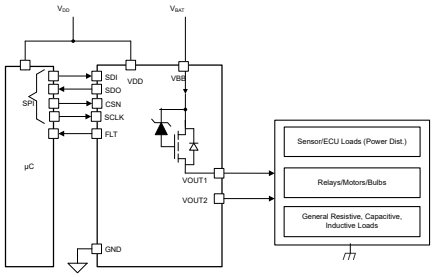
The TPS2HCS08-Q1 device also provides a high accuracy digital current sense over SPI that allows for improved load diagnostics. By reporting load current and the channel output voltage and output FET temperature to a system MCU, the device enables diagnosis of switch and load failures.

The TPS2HCS08-Q1 is available in a HTSSOP package which allows for reduced PCB footprint.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS2HCS08-Q1	PWP (HTSSOP, 16)	5mm x 6.4mm

(1) For all available packages, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Device Comparison Table

Table 4-1. Device Options

Device Version	Part Number	Output Control in ACTIVE State	I2T Range Based on R_{SNS} = 700Ω	Overcurrent Protection (I_{OCP}) Range	Limp Home State
A	TPS2HCS08A-Q1	Set through SPI	8.8A^2s to 350A^2s	10A to 55A	Yes
B	TPS2HCS08B-Q1	Set through DIx pins only			No

5 Pin Configuration and Functions

5.1 A Version Package

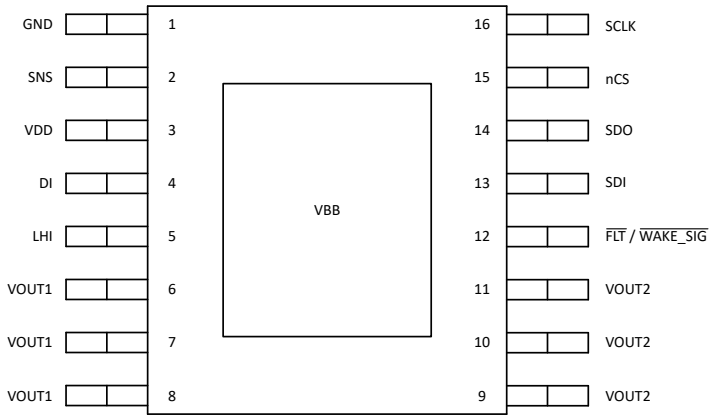


Figure 5-1. TPS2HCS08A-Q1 PWP Package,16-Pin HTSSOP (Top View)

5.2 Pinout - Version A

Pin Number	Pin Name	Type	Description
1	GND	GND	Device ground
2	SNS	O	SNS current output – use a parallel RC network to the GND pin of the IC.
3	VDD	Power	Logic Supply Input – closely decouple to GND pin of the IC with a ceramic capacitor.
4	DI	I	Sets the output behavior in the LIMP HOME mode, if configured as such.The pin needs to be connected to MCU or other HI/LO source through a 10K resistor tor protection and enabling the reverse polarity FET turn-on function.
5	LHI	I	External input (active High) to enable LIMP HOME mode.
6,7,8	VOUT1	O	Output of channel 1
9,10,11	VOUT2	O	Output of channel 2
12	$\overline{\text{FLT}}$ / $\overline{\text{WAKE\_SIG}}$	O	Fault output – on any (one or more) channel - open drain, pull up with a 4.7K resistor to VDD pin. Also functions as a wake signal to the MCU upon load current demand in key-off mode.
13	SDI	I	SPI device (secondary) data input
14	SDO	O	SPI Data Output from the device. Internally pulled up to VDD.
15	CSN	I	Chip select. Internally pulled up to VDD
16	SCLK	I	SPI Clock input
Thermal Pad	VBB	Power	Power Supply

5.3 Version B Package

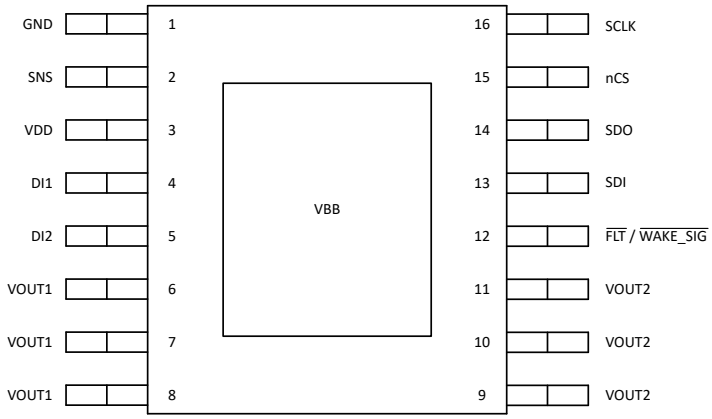


Figure 5-2. PWP Package, 16-Pin HTSSOP (Top View) - TPS2HCS08B-Q1

5.4 Pinout - Version B

Pin Number	Pin Name	Type	Description
1	GND	GND	Device ground
2	SNS	O	SNS current output – *use a resistor to GND.*
3	VDD	Power	Logic Supply Input – closely decouple to GND pin of the IC with a ceramic 1uF capacitor.
4	DI1	I	Enables channel 1 output to turn ON. The pin needs to be connected to MCU or other HI/LO source through a 10K resistor tor protection and enabling the reverse polarity FET turn-on function.
5	DI2	I	Enables channel 2 output to turn ON
6,7,8	VOUT1	O	Output of channel 1
9,10,11	VOUT2	O	Output of channel 2
12	$\overline{\text{FLT}}$ / $\overline{\text{WAKE\_SIG}}$	O	Fault output – on any (one or more) channel - open drain, pull up with a 4.7K resistor to VDD pin. Also functions as a wake signal to the MCU upon load current demand in key-off mode.
13	SDI	I	SPI device (secondary) data input
14	SDO	O	SPI Data Output from the device. Internally pulled up to VDD.
15	CSN	I	Chip select. Internally pulled up to VDD
16	SCLK	I	SPI Clock input
Thermal Pad	VBB	Power	Power Supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum continuous supply voltage, V_{VBB}			28	V
Load dump voltage	ISO16750-2:2010(E)		36	V
Maximum transient voltage on VBB pin, (example during ISO 7637 pulse 2a transient) V_{BBt}			54	V
Short circuit supply voltage capability	I_{OCP} = 55A, L_{OUT} = 5µH, t_{SHORT} = 300ms, T_A = 125°C		24	V
Short circuit supply voltage capability, parallel mode	PARALLEL_12 = 1, I_{OCP} = 40A, L_{OUT} = 5µH, t_{SHORT} = 300ms, T_A = 125°C		24	V
VOUT voltage		–30	V_{VS}+0.3	V
Reverse polarity voltage, continuous on VBB pin		–18		V
Low voltage supply pin voltage, V_{DD}		–0.3	7	V
Digital input pin voltages, V_{DIG}	SDI, SDO, SCLK, $\overline{CS}$	–0.3	7	V
Sense pin voltage, V_{SNS}		–0.3	7	V
$\overline{FLT}$ pin voltage, $V_{\overline{FLT}}$		–0.3	7	V
Limp home activation pin voltage, V_{LHI}			V_{BB}	V
Limp home direct input pin voltages, V_{DI}		–0.3	7	V
Reverse ground current, I_{GND}	V_{BB} < 0 V		–50	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per AEC Q100-002 Classification Level H2	All pins including VBB and VOUTx	±2000	V
		Human-body model (HBM), per AEC Q100-002 Classification Level H3A(2)	VBB and VOUTx	±4000	
		Charged-device model (CDM), per AEC Q100-011 Classification Level C5	All pins	±750	

(1) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.
(2) ESD strikes are with reference from the pin mentioned to GND

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BB_NOM}	Nominal supply voltage		6	18	V
V_{BB_EXT}	Extended supply voltage	See the conditions in section 9.2, power supply recommendations, operating voltage range	3	28	V
V_{DD}	Low voltage supply voltage		3.0	5.5	V
V_{DIG}	All digital input pin voltage		–0.3	5.5	V
$V_{\overline{FLT}}$	$\overline{FLT}$ pin voltage		–0.3	5.5	V

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{LHI}	Limp home activation pin voltage, LHI		V_{BB}	V
V_{DI}	Limp home direct pin input voltage, DI	–0.3	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS2HCS08-Q1 PWP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the https://www.ti.com/lit/an/spra953c/spra953c.pdf application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
V_{Clamp}	VDS clamp voltage	I_{OUT} = 10mA VBB > 28V	T_J = 25°C to 150°C	35	40	45	V
		I_{OUT} = 10mA 12V < VBB < 28V	T_J = –40°C to 150°C	30	34	38	V
		I_{OUT} = 10mA VBB = 3V	T_J = –40°C to 150°C	27.5		36.5	V
V_{BB_UVLOR}	V_{BB} undervoltage lockout rising	Measured with respect to the GND pin of the device.		3.0	3.5	4.0	V
V_{BB_UVLOF}	V_{BB} undervoltage lockout falling			2.6	2.8	3.0	V
$V_{BB\_UV\_WRN\_R}$	VBB voltage UV_WRN rising threshold	Measured with respect to the GND pin of the device.			4.9		V
$V_{BB\_UV\_WRN\_F}$	VBB voltage UV_WRN falling threshold threshold				4.5		V
V_{VDD_UVLOR}	V_{VDD} undervoltage lockout rising	Measured with respect to the GND pin of the device		1.94		2.2	V
V_{VDD_UVLOF}	V_{VDD} undervoltage lockout falling			1.86		2.07	V
$I_{SLEEP,VBB}$	Sleep current (total device leakage including all MOSFET channels)	V_{BB} ≤ 18V, device in SLEEP mode, V_{OUT} = 0V	T_J = 25°C			0.5	µA
			T_J = 85°C			2.2	µA
$I_{SLEEP,VDD}$	Sleep current from VDD pin	V_{VDD} ≤ 5.5V, device in SLEEP mode, V_{OUT} = 0V	T_J = 25°C			0.3	µA
			T_J = 85°C			0.5	µA
$I_{OUT(OFF)}$	Output leakage current (per channel)	V_{OUT} = 0V, Channel disabled, ACTIVE/CONFIG state	T_J = –40 to 125°C		1	14	µA

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q,VDD}$	VDD quiescent current	ACTIVE state, SCLK off	V_{DD} = 5.5V		1.4	1.6	mA
		ACTIVE state, SCLK ON				2.2	mA
$I_{Q,VBB}$	V_{BB} quiescent current	All channels enabled, I_{OUTx} = 0A, SCLK off, Diagnostics disabled	V_{DD} = 5.5V		3.8	4.3	mA
			V_{DD} = 3.0V		4.25	5.2	mA
		All channels enabled, I_{OUTx} = 0A, SCLK off, Diagnostics enabled (ISNS, ADC)	V_{DD} = 5.5V		3.9	4.5	mA
			V_{DD} = 0V		4.4	5.5	mA
$I_{L,CONT}$	Continuous load current, per channel	All channels enabled, T_{AMB} = 85°C			8		A
		One channel enabled, T_{AMB} = 85°C			13		A
RON CHARACTERISTICS							
R_{ON}	On-resistance	6V ≤ V_{BB} ≤ 28V, I_{OUTx} = 1A, OL_ON_EN_CH1 = 0	T_J = 25°C		8.9		mΩ
			T_J = 150°C			17.8	mΩ
R_{ON_OL}	On-resistance, OL_ON mode	6V ≤ V_{BB} ≤ 28V, I_{OUTx} = 0.3A, OL_ON_EN_CHx = 1	T_J = 25°C		27		mΩ
			T_J = 150°C			54	mΩ
$R_{ON(REV)}$	On-resistance during reverse polarity	–18V ≤ V_{BB} ≤ –7V, Version A & B	T_J = 25°C		9.5		mΩ
			T_J = 150°C			20	mΩ
ΔR_{ON}	Percentage difference in on-resistance between channels ($R_{ON,CHx}$ - $R_{ON,CHy}$)	V_{BB} ≥ 6V, T_J = 25°C			0.5	7	%
CURRENT SENSE CHARACTERISTICS							
K_{SNS1}	Current sense ratio I_{OUTx} / I_{SNS}	I_{OUT} = 1.0A, OL_ON_EN_CHx = 0			5000		
K_{SNS2}	Current sense ratio I_{OUTx} / I_{SNS}	I_{OUT} = 50mA, OL_ON_EN_CHx = 1			1400		
I_{SNS_SAT}	Saturated sense current	VBB > 6V, RSNS = 374Ω OL_ON_EN_CHx =0	I_{OUT} = > 30A	6			mA
K_{SNS1}	K_{SNS1} ratio I_{OUT} / I_{SNS1} across I_{OUT}	RSNS = 374Ω, OL_ON_EN_CHx = 0	I_{OUT} = 20A		5000		
				-3		3	%
		RSNS = 698Ω OL_ON_EN_CHx = 0	I_{OUT} = 10A		5000		
				-4		4	%
			I_{OUT} = 5A		5000		
				-5		5	%
			I_{OUT} = 2.5A		5000		
				-5		5	%
			I_{OUT} = 1A		5000		
				-5		5	%
			I_{OUT} = 500mA		5000		
				-7		7	%
			I_{OUT} = 250mA		5000		
				-10		10	%
			I_{OUT} = 100mA		5000		
				-18		18	%

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
K_{SNS2}	K_{SNS2} ratio I_{OUT} / I_{SNS2} across I_{OUT}	RSNS = 698Ω OL_ON_EN_CHx = 1	I_{OUT} = 250mA		1400		
				-10		10	%
			I_{OUT} = 100mA		1400		
				-10		10	%
			I_{OUT} = 50mA		1400		
				-12		12	%
			I_{OUT} = 25mA		1400		
				-20		20	%
			I_{OUT} = 10mA		1400		
				40		40	%
$I_{ENTRY\_OL\_ON}$	I_{OUT} current to enter OL_ON mode (OL_ON_EN_CHx = 1)			0.5			A
$I_{EXIT\_OL\_ON}$	I_{OUT} current to exit OL_ON mode (OL_ON_EN_CHx = 1)					1.7	A
ADC CHARACTERISTICS							
$V_{ADCREFHI}$	ADC reference voltage			2.76	2.81	2.9	V
Isample	Current sense sampling time	Including mux timing and ADC conversion time		50			µs
I_{ADC}	ADC current consumption					0.5	mA
SNS CHARACTERISTICS							
$ISNS_{ADC,ACC}$	ISNS ADC accuracy	OL_ON_EN_CHx =1, ISNS_SCALE_CHx = 1	SNS pin voltage = 2.7V	-3		3	%
			SNS pin voltage = 1.4V	-3.25		3.25	%
			SNS pin voltage = 0.7V	-4		4	%
			SNS pin voltage = 0.1V	-15		15	%
		OL_ON_EN_CHx =1, ISNS_SCALE_CHx = 8	SNS pin voltage = 0.04V	-10.5		10.5	%
			SNS pin voltage = 0.01V	-37.5		37.5	%
ADC_{TSNS}	T_{SNS} ADC output code	T_J = 25°C	Includes buffer gain		474		
$TSNS_{ACC}$	T_{SNS} measurement accuracy			-17		17	°C
ADC_{VSNS}	ADC code of output voltage measurement	VOUTx = 13.5V, referenced to device GND	Includes buffer gain		459		
$VSNS_{ACC}$	VOUT SNS (VSNS) measurement accuracy			-5		5	%
ADC_{VBBSNS}	ADC code of VBB voltage measurement	VBB = 13.5V, referenced to device GND	Includes buffer gain		452		
$VBBSNS_{ACC}$	VBB SNS (VBBSNS) measurement accuracy			-5		5	%
OVERCURRENT PROTECTION CHARACTERISTICS							
I_{OCP_RANGE}	Overcurrent protection threshold, immediate shutdown - range	di/dt = 2A/µs		10		55	A

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OCP}	Overcurrent protection threshold, immediate shutdown	di/dt = 2A/µs T_J = –40°C to 150°C	ILIMIT_SET_CHx = 0x0		10		A
			ILIMIT_SET_CHx = 0x1		12.5		A
			ILIMIT_SET_CHx = 0x2		15		A
			ILIMIT_SET_CHx = 0x3		17.5		A
			ILIMIT_SET_CHx = 0x4		20		A
			ILIMIT_SET_CHx = 0x5		22.5		A
			ILIMIT_SET_CHx = 0x6		25		A
			ILIMIT_SET_CHx = 0x7		32.5		A
			ILIMIT_SET_CHx = 0x8		40		A
			ILIMIT_SET_CHx = 0x9		47.5		A
			ILIMIT_SET_CHx = 0xA		55		A
$I_{OCP\_RANGE,PARALLEL}$	Overcurrent protection threshold, immediate shutdown - range in parallel mode	di/dt = 2A/µs PARALLEL_12 = 1		10		40	A
$I_{OCP\_RETRY\_FLBK}$	Overcurrent protection foldback threshold, immediate shutdown mode	Only applicable for CAP_CHRG_CHx = 00 and I_{OCP} > 47.5A, n_{RETRY} > 7, di/dt = 2A/µs, T_J = –40°C to 150°C			47.5		A
t_{OCP_DETECT}	Immediate shutdown detection time	T_J = -40°C to 150°C	From I_{OUT} = I_{OCP} to I_{OCP} detection R_{OUT} = 150% of I_{OCP} , L_{IN} = L_{OUT}= 0nH	0.3		1.5	us
t_{OCP_TOFF}	Immediate shutdown turn off time	T_J = -40°C to 150°C	From I_{OCP} detection to 10% of V_{OUTx} R_{OUT} = 150% of I_{OCP} , L_{IN} = L_{OUT} = 0nH			7.5	us
$I_{OCP\_TEMP\_COMP}$	I_{OCP} high temperature compensation	T_J ≥ 85°C, I_{OCP} ≥ 47.5A			-0.375		%/°C
CAP CHRG CURRENT LIMITATION							
I_{CL_Reg}	Current regulation mode current in inrush period	T_J = –40°C to 150°C dI/dt < 0.01A/ms	INRUSH_LIMIT_CHx = 0	0.81	1.67	2.485	A
			INRUSH_LIMIT_CHx = 1		2		A
			INRUSH_LIMIT_CHx = 2		2.4		A
			INRUSH_LIMIT_CHx = 3		2.8		A
			INRUSH_LIMIT_CHx = 4	1.7	3.3	5	A
			INRUSH_LIMIT_CHx = 5		3.6		A
			INRUSH_LIMIT_CHx = 6		4.2		A
			INRUSH_LIMIT_CHx = 7		5.5		A
			INRUSH_LIMIT_CHx = 8		6.8		A
			INRUSH_LIMIT_CHx = 9		8.1		A
			INRUSH_LIMIT_CHx = A		9.5		A
			INRUSH_LIMIT_CHx = B		11		A
			INRUSH_LIMIT_CHx = C		12		A
CAPACITIVE CHARGING							
t_{INRUSH_RANGE}	Inrush duration settings range	INRUSH_DURATION_CHx range		0		100	ms
FAULT CHARACTERISTICS							

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OL_OFF}	Off state open-load (OL) detection internal pull-up current	Switch disabled, OL_OFF_EN_CHx = enabled	OL_PULLUP_STR=00	20.1	26.5	100	µA
			OL_PULLUP_STR=01	48.1	60	126	µA
			OL_PULLUP_STR=10	103.2	127	208	µA
			OL_PULLUP_STR=11	213	260	348	µA
R_{SHRT_VBB}	Off state short to VBB detection pulldown resistance	Channel disabled, off-state short_VBB diagnostics enabled		5.5	6.8	8	kΩ
$V_{OL\_OFF\_TH}$	Off state Open-load (OL) detection voltage	Channel Disabled, off-state open load diagnostics enabled, V_{OUTx}		1.9	2.5	2.95	V
T_{ABS}	Thermal shutdown			155	180	205	°C
T_{OTW}	Thermal shutdown warning			130	150	170	°C
T_{REL}	Relative thermal shutdown temperature				60		°C
T_{HYS}	Thermal shutdown hysteresis			20	25	30	°C
$n_{RETRY,\ INT}$	Number of retry cycles before I_{OCP} = $I_{OCP\_RETRY\_FLBK}$	Only applicable for CAP_CHRG_CHx = 00 and I_{OCP} > 47.5A			7		
t_{RETRY}	Retry time	Time from fault shutdown until switch re-enable (thermal shutdown or overcurrent). PWM will wait until next cycle to come back on			2		ms
t_{WAKE_SIG}	WAKE_SIG / FLT pin indication for LPM exit				100		µs
TIMING CHARACTERISTICS							
OSC_{ACC}	Oscillator accuracy			-10		10	%
PWM_{FREQ}	PWM Frequency	PWM_EN = 1	PWM_FREQ_CHx = 101	372	425	478	Hz
LOW POWER MODE CHARACTERISTICS							
R_{ON,LPM_AUTO}	R_{ON} in AUTO_LPM mode		T_J = –40°C to 105°C		9	18	mΩ
R_{ON,LPM_MAN}	R_{ON} in MANUAL_LPM mode		T_J = –40°C to 105°C		28	58	mΩ
$I_{ENTRY\_LPM\_AUTO}$	I_{OUT} current to enter AUTO_LPM state		T_J = –40°C to 105°C		0.95		A
$I_{EXIT\_LPM\_AUTO}$	I_{OUT} current to exit AUTO_LPM state		T_J = –40°C to 105°C		1.05		A
$I_{SCP\_LPM\_AUTO}$	Short-circuit detection threshold for AUTO_LPM state		T_J = –40°C to 105°C		13.7		A
$I_{EXIT\_LPM\_MAN}$	IOUTx threshold for MANUAL_LPM exit	Current ramp at 1mA/µs T_J = –40°C to 85°C	MAN_LPM_EXIT_CURR_CHx = 00	365	530	690	mA
			MAN_LPM_EXIT_CURR_CHx = 01	500	700	915	mA
			MAN_LPM_EXIT_CURR_CHx = 10	114	165	236	mA
			MAN_LPM_EXIT_CURR_CHx = 11	240	350	460	mA
$I_{SCP\_LPM\_MAN}$	Load current when the channel detects a short circuit	di/dt = 5mA/µs	LPM exit test mode		4.0		A
t_{RETRY_LPM}	Retry time in LPM state				5		µs
$t_{STBY\_LPM\_AUTO}$	standby time before enter AUTO_LPM state	$I_{OUTx} \le I_{ENTRY\_LPM\_AUTO}$			20		ms

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{LPM_ENTRY}	Time to enter LPM state				200		µs
t_{WAKE}	$I_{EXIT\_LPM\_MAN}$ detection time				5		µs
t_{SLEW}	Time to slew on the main FET after $I_{EXIT\_LPM\_MAN}$				200		µs
I_{Q,VDD,LPM_MAN}	VDD quiescent current in MANUAL_LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C	both channels OFF		9	18	µA
			one channel ON		12.3	21.6	µA
			both channels ON		15.6	23	µA
I_{Q,VDD,LPM_AUTO}	VDD quiescent current in AUTO_LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C	both channels OFF		9	18	µA
			one channel ON		12.3	21.6	µA
			both channels ON		15.6	23	µA
I_{Q,VBB,LPM_MAN}	VBB quiescent current in MANUAL_LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C	both channels OFF		3.72	7	µA
			one channel ON		5.1	9.1	µA
			both channels ON		6.42	9.5	µA
I_{Q,VBB,LPM_AUTO}	VBB quiescent current in AUTO_LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C	both channels OFF		10.4	15.5	µA
			one channel ON		11	15.8	µA
			both channels ON		11.6	16.1	µA
DIGITAL INPUT PIN CHARACTERISTICS							
$V_{IH,SPI}$	Input voltage high-level (SCLK, SDI, CSN)	3.0V ≤ VDD ≤ 5.5V		0.7 × V_{VDD}			V
$V_{IL,SPI}$	Input voltage low-level (SCLK, SDI, CSN)	3.0V ≤ VDD ≤ 5.5V				0.3 × V_{VDD}	V
$R_{PD,SCLK}$	SCLK Internal pulldown resistor			1.90	2	2.16	MΩ
$I_{IH,SCLK}$	Input current high-level	SCLK V_{DI} = 5V	V_{SCLK} = 5V		2.5		µA
$R_{PD,SDI}$	SDI Internal pulldown resistor			1.90	2	2.16	MΩ
$I_{IH,SDI}$	Input current high-level	SDI	V_{SDI} = 5V		2.5		µA
$R_{PU,CSN}$	CSN Internal pullup resistor			85	90	96	kΩ
$V_{IH,DI}$	input voltage high-level	DI (version A)		1.65			V
$V_{IL,DI}$	Input voltage low-level					0.8	V
$R_{PD,DI}$	Internal pulldown resistor			772	850	915	kΩ
$I_{IH,DI}$	Input current high-level		V_{DI} = 5V		6		µA
$V_{IH,DI1}$	input voltage high-level	DI1 (version B)		1.65			V
$V_{IL,DI1}$	Input voltage low-level					0.8	V
$R_{PD,DI1}$	Internal pulldown resistor			772	850	915	kΩ
$I_{IH,DI1}$	Input current high-level		V_{DI1} = 5V		6		µA
$V_{IH,LHI}$	input voltage high-level	LHI (version A)		1.65			V
$V_{IL,LHI}$	Input voltage low-level					0.8	V
$R_{PD,LHI}$	Internal pulldown resistor			772	850	915	kΩ
$I_{IH,LHI}$	Input current high-level		V_{LHI} = 5V		6		µA
$V_{IH,DI2}$	input voltage high-level	DI2 (version B)		1.65			V
$V_{IL,DI2}$	Input voltage low-level					0.8	V
$R_{PD,DI2}$	Internal pulldown resistor			772	850	915	kΩ
$I_{IH,DI2}$	Input current high-level		V_{DI2} = 5V		6		µA
DIGITAL OUTPUT PIN CHARACTERISTICS							

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH,SDO}$	Output logic high voltage drop	SDO pin current = -2mA			0.2	V
$V_{OL,SDO}$	Output logic low voltage	SDO Pin current = 2mA			0.2	V
V_{OL_FLT}	Output logic low voltage drop	$\overline{FLT}$ pin current = 4mA			0.55	V

6.6 SPI Timing Requirements

Over operating junction temperature T_J = –40°C to 150°C, V_{DD} = 3.0V to 5.5V (measured with respect to the GND pin of the device)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SPI}	SPI clock (SCLK) frequency	C_{SDO} = 30 pF, IO protection resistor 0.22 kΩ			8	MHz
t_{high}	High time: SCLK logic high-time duration		45			ns
t_{low}	Low time: SCLK logic low-time duration		45			ns
t_{sucs}	$\overline{CS}$ setup time: time delay between falling edge of $\overline{CS}$ and rising edge of SCLK		45			ns
t_{su_SDI}	SDI setup time: setup time of SDI before the falling edge of SCLK		15			ns
t_{h_SDI}	SDI hold time: hold time of SDI before the falling edge of SCLK		30			ns
t_{d_SDO}	Delay time: time delay from rising edge of SCLK to data valid at SDO				30	ns
t_{hcs}	Hold time: time between the falling edge of SCLK and rising edge of $\overline{CS}$		45			ns
t_{dis_cs}	$\overline{CS}$ disable time, $\overline{CS}$ high to SDO high impedance			10		ns
t_{hics}	SPI transfer inactive time (time between two transfers) during which $\overline{CS}$ must remain high		500			ns

6.7 Switching Characteristics

V_{BB} = 13.5V, R_L = 2Ω, T_J = –40°C to 150°C (unless otherwise noted)

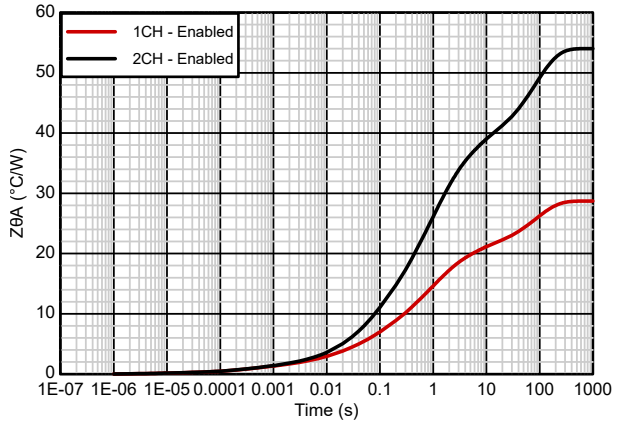
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR1}	Channel turnon delay time	50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 10 (default)	8	30	45	µs
t_{DF1}	Channel turnoff delay time	50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 10 (default)	10	20	30	µs
SR_R	VOUT rising slew rate	20% to 80% of V_{OUT}, SLRT_CHx = 11		0.55		V/µs
		20% to 80% of V_{OUT}, SLRT_CHx = 10 (default)		0.45		V/µs
		20% to 80% of V_{OUT}, SLRT_CHx = 01		0.34		V/µs
		20% to 80% of V_{OUT}, SLRT_CHx = 00		0.25		V/µs
SR_F	VOUT falling slew rate	80% to 20% of V_{OUT}, SLRT_CHx = 11		0.6		V/µs
		80% to 20% of V_{OUT}, SLRT_CHx = 10 (default)		0.42		V/µs
		80% to 20% of V_{OUT}, SLRT_CHx = 01		0.30		V/µs
		80% to 20% of V_{OUT}, SLRT_CHx = 00		0.21		V/µs
t_{ON}	Channel turnon time	50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx=10 (default)	40	53	70	µs
t_{OFF}	Channel turnoff time	50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx=10 (default)	30	36	50	µs

6.7 Switching Characteristics (continued)

V_{BB} = 13.5V, R_L = 2Ω, T_J = –40°C to 150°C (unless otherwise noted)

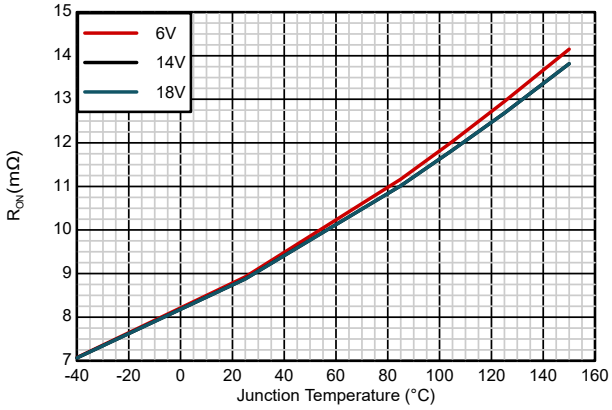
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON} - t_{OFF}	Turnon and off matching	1ms ON time switch enable pulse	–10		30	µs
		200µs OFF time switch enable pulse, frequency = 1kHz	–10		30	µs
		200µs ON time switch enable pulse, frequency = 1 kHz	–15	–4	5	µs
E_{ON}	Switching energy losses during turnon	VOUT from 10% to 90%, SLRT_CHx = 11		0.4		mJ
		VOUT from 10% to 90%, SLRT_CHx = 10 (default)		0.5		mJ
		VOUT from 10% to 90%, SLRT_CHx = 01		0.65		mJ
		VOUT from 10% to 90%, SLRT_CHx = 00		0.9		mJ
E_{OFF}	Switching energy losses during turnoff	VOUT from 90% to 10%, SLRT_CHx = 11		0.37		mJ
		VOUT from 90% to 10%, SLRT_CHx = 10 (default)		0.48		mJ
		VOUT from 90% to 10%, SLRT_CHx = 01		0.68		mJ
		VOUT from 90% to 10%, SLRT_CHx = 00		0.9		mJ

6.8 Typical Characteristics



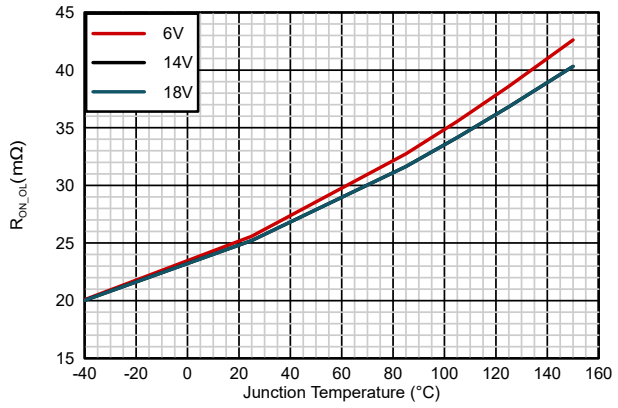
JEDEC 2s2p PCB
Board dimensions (W x L x H):
76.2mm x 114.3mm x 1.6mm

Figure 6-1. Transient Thermal Impedance



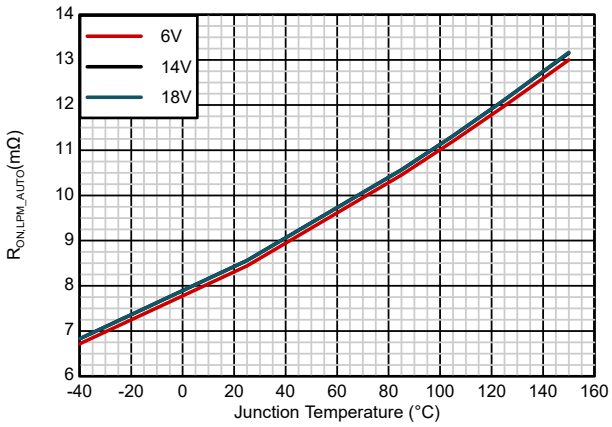
I_{OUT} = 500mA Active state
OL_ON_EN_CHx = 0

Figure 6-2. On resistance (R_{ON}) vs Temperature



I_{OUT} = 500mA Active state
OL_ON_EN_CHx = 1

Figure 6-3. On resistance, OL_ON mode (R_{ON_OL}) vs Temperature



I_{OUT} = 500mA AUTO_LPM state

Figure 6-4. On resistance in AUTO_LPM (R_{ON,LPM_AUTO}) vs Temperature

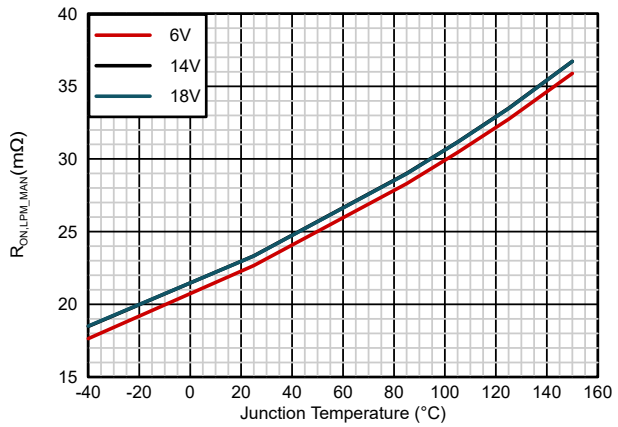
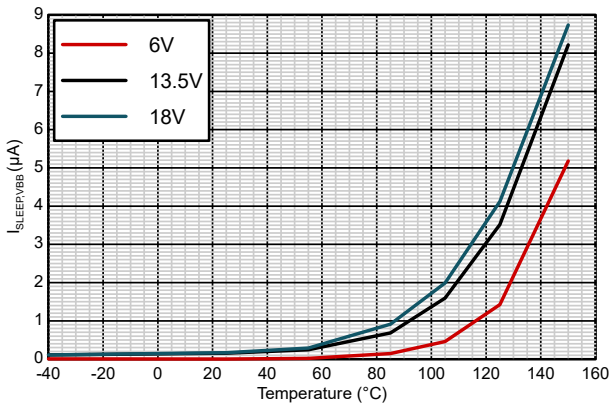


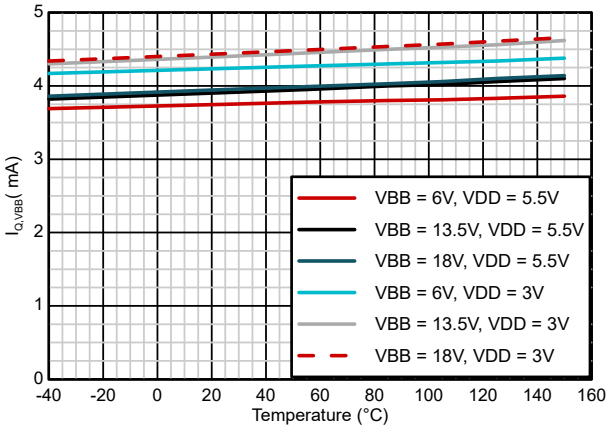
Figure 6-5. On resistance in MANUAL_LPM (R_{ON,LPM_MAN}) vs Temperature



VDD = 5.5V SLEEP state

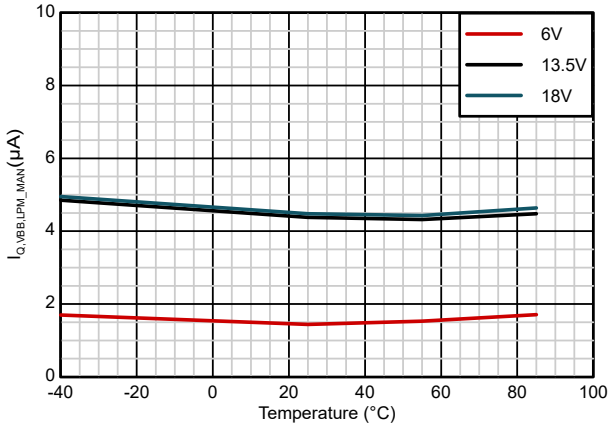
Figure 6-6. VBB sleep current ($I_{SLEEP,VBB}$) vs Temperature

6.8 Typical Characteristics (continued)



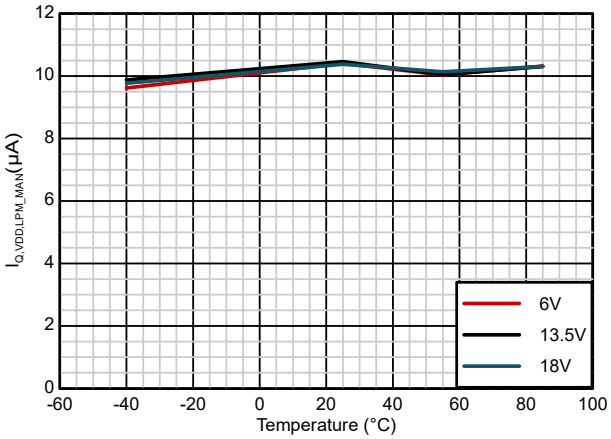
ACTIVE state
IOUT = 0A
Diagnostics enabled (ISNS, ADC)
SCLK off

Figure 6-7. VBB IQ current ($I_{Q,VBB}$) vs Temperature



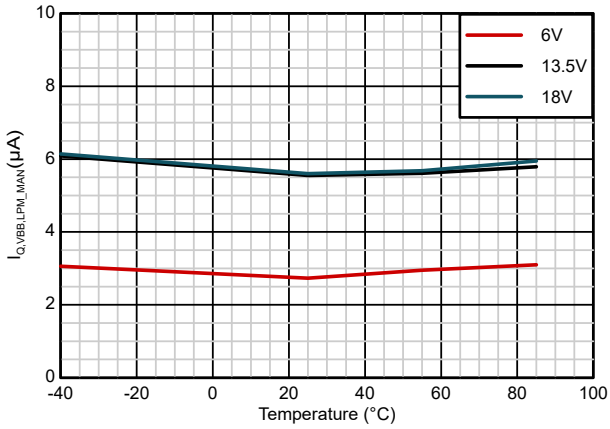
MANUAL_LPM state
Channels off
VDD = 5V

Figure 6-8. VBB IQ current in MANUAL_LPM (I_{Q,VBB,LPM_MAN}) - channels off vs. Temperature



MANUAL_LPM state
Channels off
VDD = 5V
IOUT = 0A

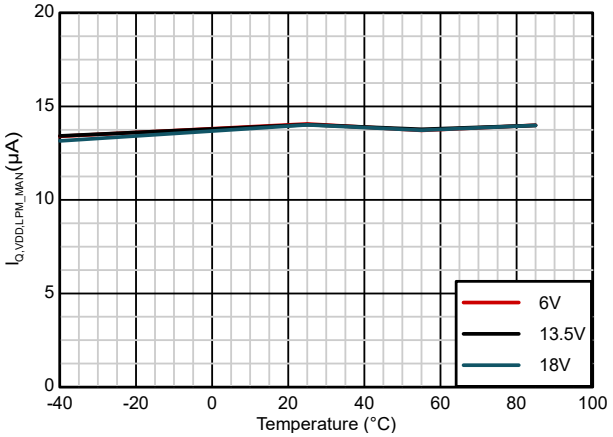
Figure 6-9. VDD IQ current in MANUAL_LPM (I_{Q,VDD,LPM_MAN}) - channels off vs. Temperature



MANUAL_LPM state
One channel enabled
VDD = 5V
IOUT = 0A

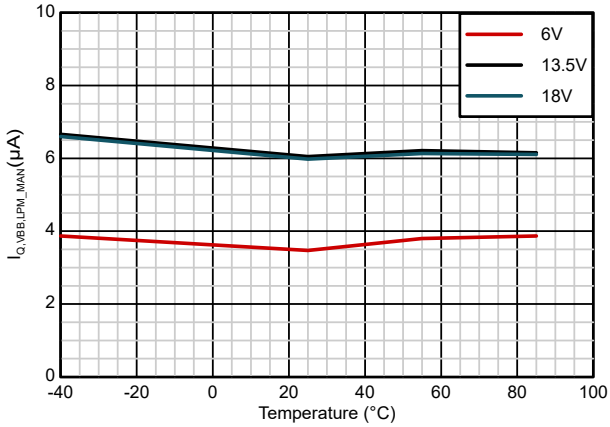
Figure 6-10. VBB IQ current in MANUAL_LPM (I_{Q,VBB,LPM_MAN}) - one channel enabled vs. Temperature

6.8 Typical Characteristics (continued)



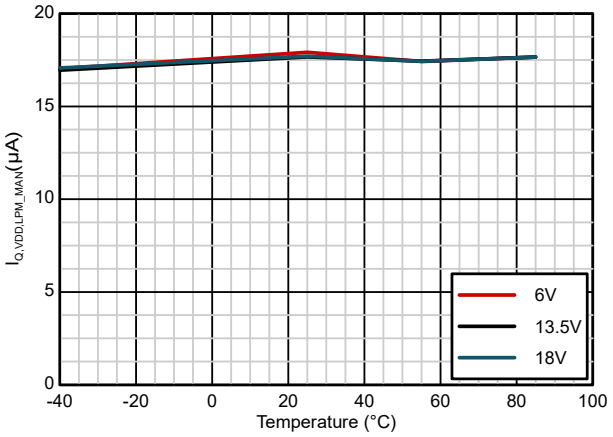
MANUAL_LPM state: VDD = 5V
One channel enabled: IOUT = 0A

Figure 6-11. VDD IQ current in MANUAL_LPM (I_{Q,VDD,LPM_MAN}) - one channel enabled vs. Temperature



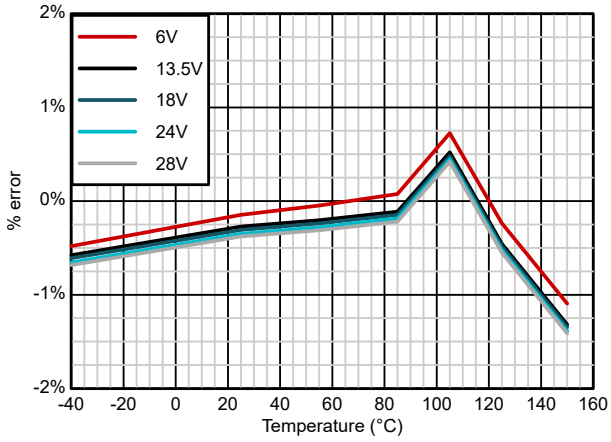
MANUAL_LPM state: VDD = 5V
Both channels enabled: IOUT = 0A

Figure 6-12. VBB IQ current in MANUAL_LPM (I_{Q,VBB,LPM_MAN}) - both channels enabled vs. Temperature



MANUAL_LPM state: VDD = 5V
Both channels enabled: IOUT = 0A

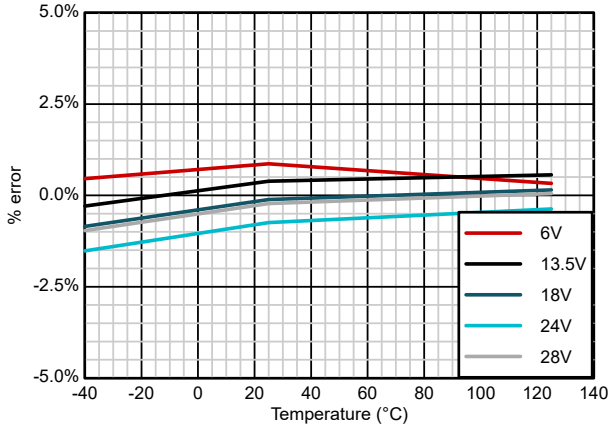
Figure 6-13. VDD IQ current in MANUAL_LPM (I_{Q,VDD,LPM_MAN}) - both channels enabled vs. Temperature



K_{SNS1} reference = 5000
OL_ON_EN_CHx = 0: IOUT = 2A

Figure 6-14. K_{SNS1} % error vs. Temperature

6.8 Typical Characteristics (continued)



K_{SNS2} reference = 1400
OL_ON_EN_CHx = 1
IOUT = 25mA

Figure 6-15. K_{SNS2} % error vs. Temperature

7 Parameter Measurement Information

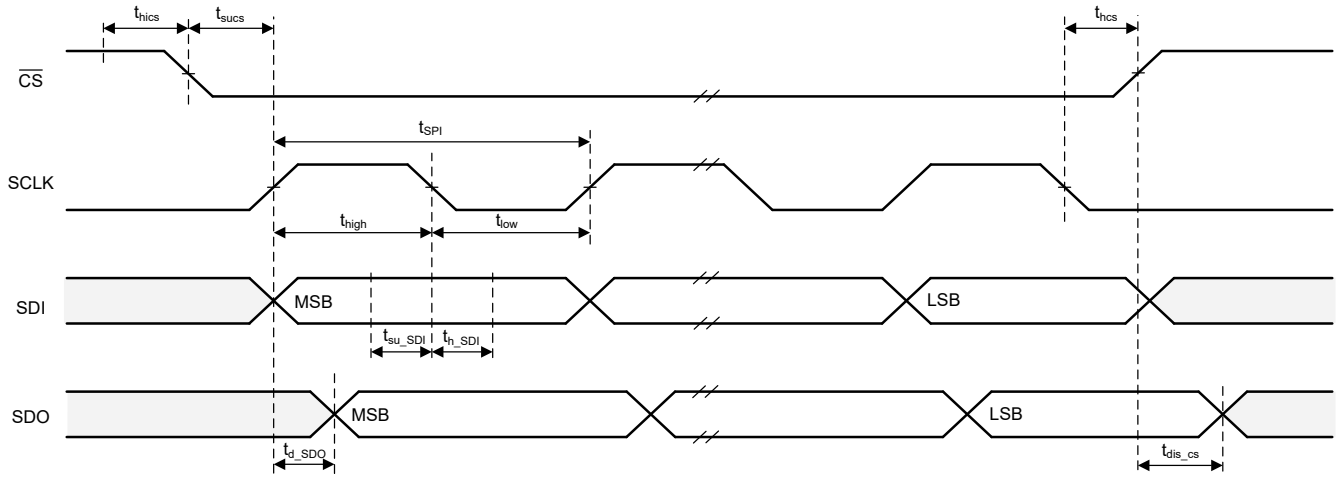


Figure 7-1. SPI Timing Characteristics Definitions

8 Detailed Description

8.1 Overview

The TPS2HCS08-Q1 device is a dual-channel smart high-side switch intended for use with 12V automotive batteries. The TPS2HCS08-Q1 device integrates SPI control and configuration as well digital readout with an ADC of key device and load diagnostics. The device incorporates all of the specific features needed for a power distribution switch as well as the traditional protective and diganostic functions seen in high side switches for actuator drive applications.

Diagnostics features include a digital current, output voltage and FET temperature sense output that can be read over the SPI serial interface. The high-accuracy load current sense allows for diagnostics of complex loads. The output voltage sense and FET temperature sense fearures in the device enables diagnosis of the switch and load failures.

This device includes protection through thermal shutdown, overcurrent protection, transient withstand, and reverse battery operation. In addition, the device also includes an SPI-configurable wire-harness protection function through a defined fuse or tme-current curve. The protection works in conjunction with an immediate switch-off overcurrent protection with an SPI-configurable threshold to fully protect against overload and short circuit faults.

The TPS2HCS08-Q1device also integrates a low quiescent current mode where the device can provide currents in the 100s of mA range while consuming only micro-amps of current. The device automatically switches to the high-current mode on an increase in load current and provide a wake signal to the MCU. Further, the device includes a capacitive charging mode that reduces the peak current load on the supply. Together, the two features support power distribution switch to off-board ECU applications.

For more details on the diagnosis, power distribution and protection features, refer to the *Feature Description* and *Application Information* sections of the document.

The TPS2HCS08-Q1 is one device in a family of TI high side switches. For each device, the part number indicates elements of the device behavior. Figure 8-1 gives an example of the device nomenclature.

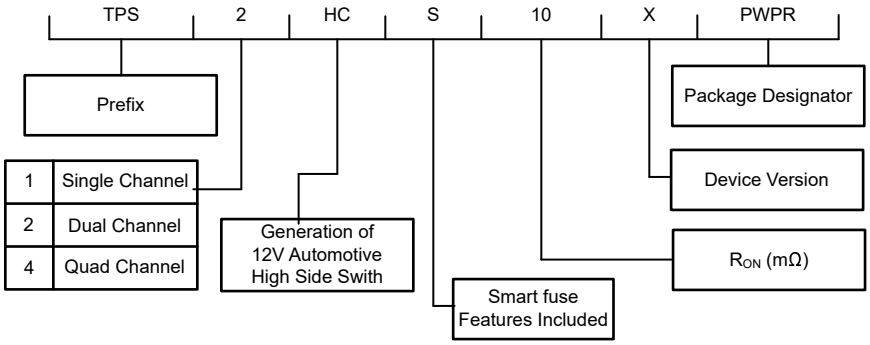


Figure 8-1. Naming Convention

8.2 Functional Block Diagram

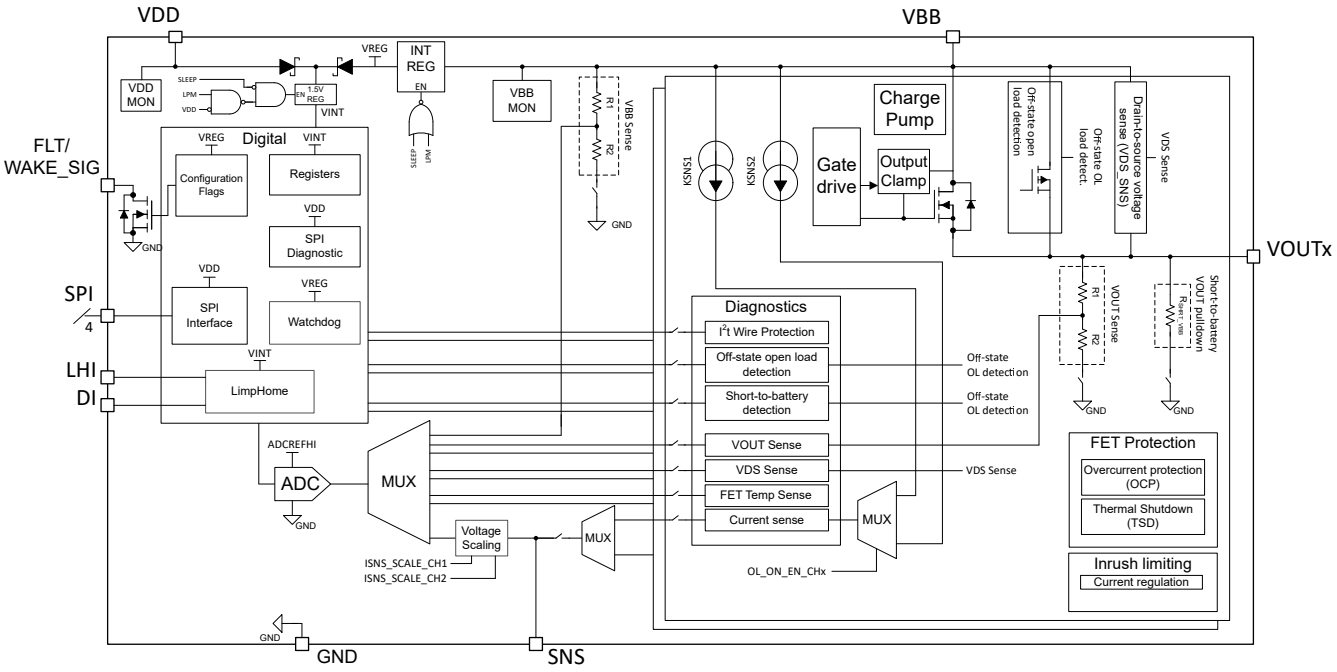


Figure 8-2. TPS2HCS08A-Q1 functional block diagram

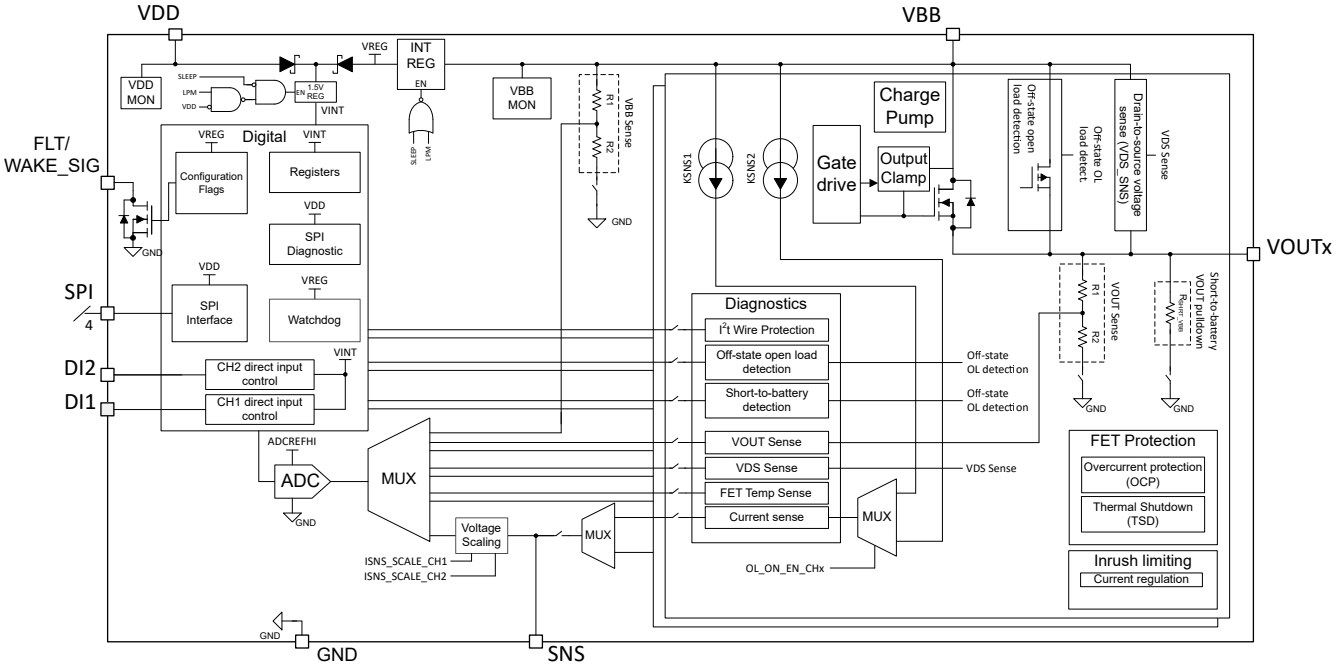


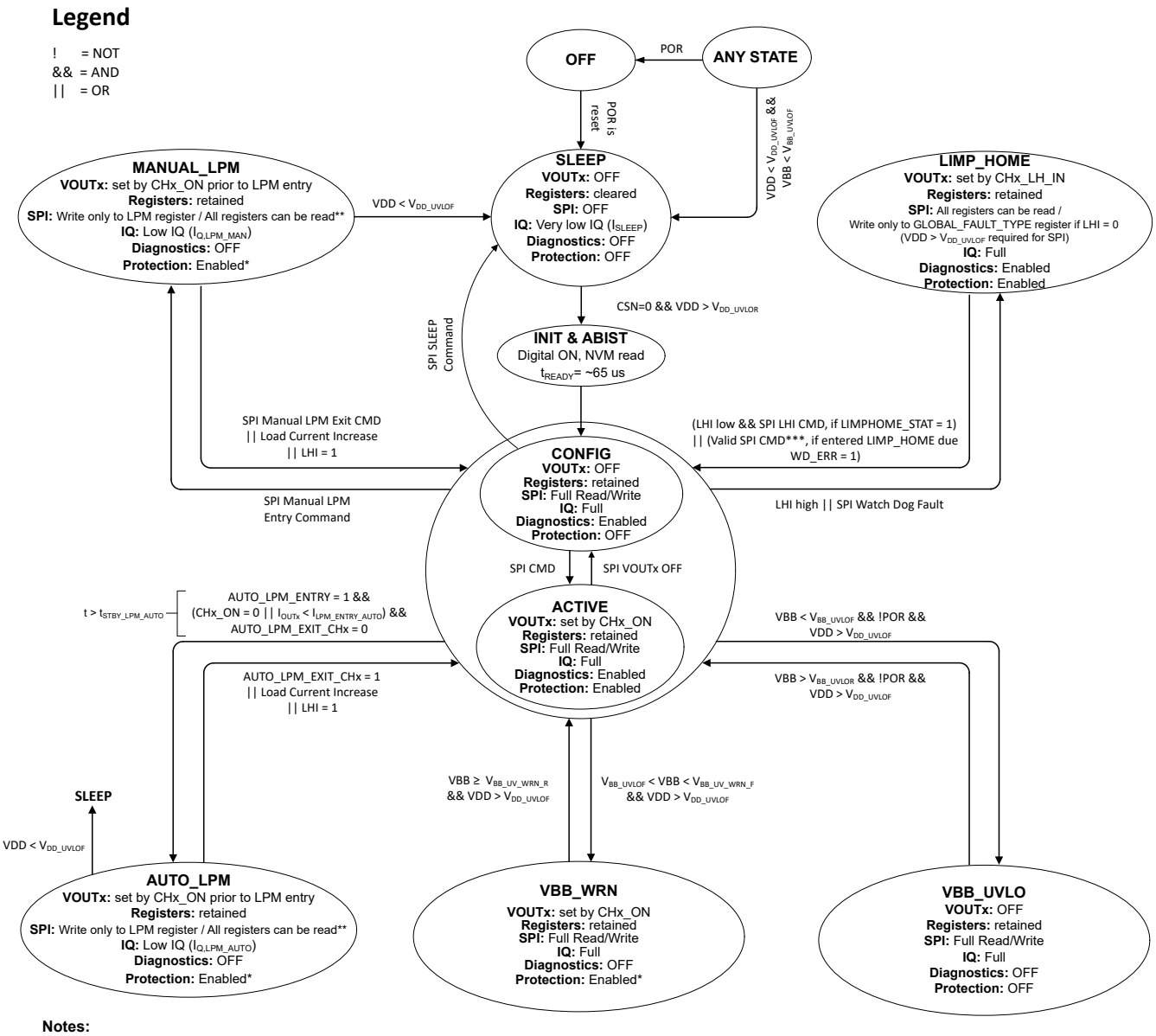
Figure 8-3. TPS2HCS08B-Q1 functional block diagram

8.3 Device Functional Modes

8.3.1 State Diagram

The device has three main categories of states it can transition into and out of low quiescent current, normal operation, and limp home. Inside of each of the categories are several states the device can be in. The state

diagram for the TPS2HCS08A-Q1 device is shown in Figure 8-4 and the state diagram for the TPS2HCS08B-Q1 device is shown in Figure 8-5.

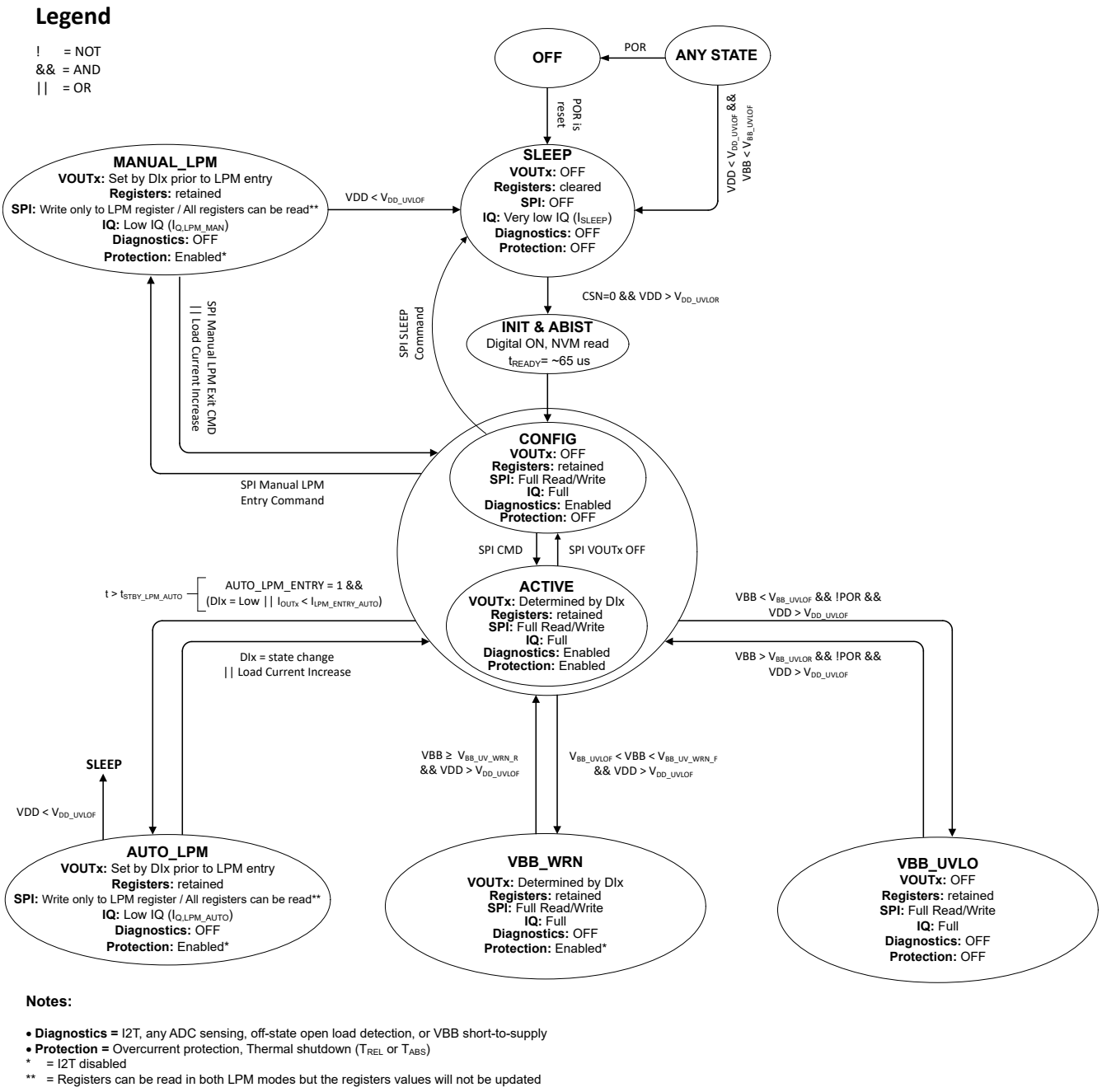


Notes:

- **Diagnostics =** I2T, any ADC sensing, off-state open load detection, or VBB short-to-supply
- **Protection =** Overcurrent protection (I_{OCP}), Thermal shutdown (T_{REL} or T_{ABS}), and I2T protection (if enabled) or LPM short-circuit ($I_{SCP,LPM}$) in LPM states

* = I2T disabled
** = Registers can be read in both LPM modes but the registers values will not be updated
*** = See “SPI watchdog function” section

Figure 8-4. State Diagram - Version A



Notes:

- **Diagnostics =** I2T, any ADC sensing, off-state open load detection, or VBB short-to-supply
- **Protection =** Overcurrent protection, Thermal shutdown (T_{REL} or T_{ABS})

* = I2T disabled

** = Registers can be read in both LPM modes but the registers values will not be updated

Figure 8-5. State Diagram - Version B

8.3.2 Output Control

Control of the eFuse channels varies depending on the device version. See the below sections for more details on the ouptut control method for each of the device versions.

Output Control - Version A

The state of the eFuse outputs for ACTIVE state for TPS2HCS08A-Q1 is controlled by the CHx_ON bits in the SW_STATE register. Table 8-1 below showcases the output control method in each state for the TPS2HCS08A-Q1 device.

Table 8-1. Output Control by State - TPS2HCS08A-Q1

State	Control Type	Output Control Description
SLEEP	N/A	Output OFF
CONFIG	SPI	Output OFF
ACTIVE	SPI	Set by CHx_ON
LIMP_HOME	SPI or DI pin	Set by SPI through CHx_LH_IN bit See Section 8.3.7 section for more details on output control settings
AUTO_LPM	SPI	Set by CHx_ON prior to AUTO_LPM entry
MANUAL_LPM	SPI	Set by CHx_ON prior to MANUAL_LPM entry
VBB_WRN	SPI	Set by CHx_ON
VBB_UVLO	N/A	Output OFF

Output Control - Version B

The state of the eFuse outputs for ACTIVE state for TPS2HCS08B-Q1 is controlled exclusively by the DI1 for channel 1 and DI2 for channel 2. The CHx_ON bits in the SW_STATE register have no effect on the output state of the TPS2HCS08B-Q1. Table 8-2 below showcases the output control method in each state for the TPS2HCS08B-Q1 device.

Table 8-2. Output Control by State - TPS2HCS08B-Q1

State	Control Type	Output Control Description
SLEEP	N/A	Output OFF
CONFIG	DIx	Output OFF
ACTIVE	DIx	Set by DIx pins
AUTO_LPM	DIx	Set by DIx pins prior to AUTO_LPM entry
MANUAL_LPM	DIx	Set by DIx pins prior to MANUAL_LPM entry
VBB_WRN	DIx	Set by DIx pins
VBB_UVLO	N/A	Output OFF

8.3.3 SPI Mode Operation

The TPS2HCS08-Q1 communicates with the host controller through a high-speed SPI serial interface. The interface has three logic inputs: clock (CLK), chip select ($\overline{CS}$), serial data in (SDI), and one data out (SDO). The SDO is tri-stated when the $\overline{CS}$ pin is high. The maximum SPI clock rate is 8 MHz, but is limited in practice by the series protection resistor.

The device supports simple daisy chain SPI. This mode can be used with or without CRC.

The communication between the TPS2HCS08-Q1 IC and the controller or MCU is through a SPI bus in a primary-secondary configuration. The external MCU is always an SPI primary device that sends command requests on the SDI pin of the TPS2HCS08-Q1 IC and receives device responses on the SDO pin of the IC. The TPS2HCS08-Q1 device is always an SPI secondary device that receives command requests over the SDI line and sends responses (such as status and measured values) to the external MCU over the SDO line.

The TPS2HCS08-Q1 device can be connected to the primary MCU in the following formats:

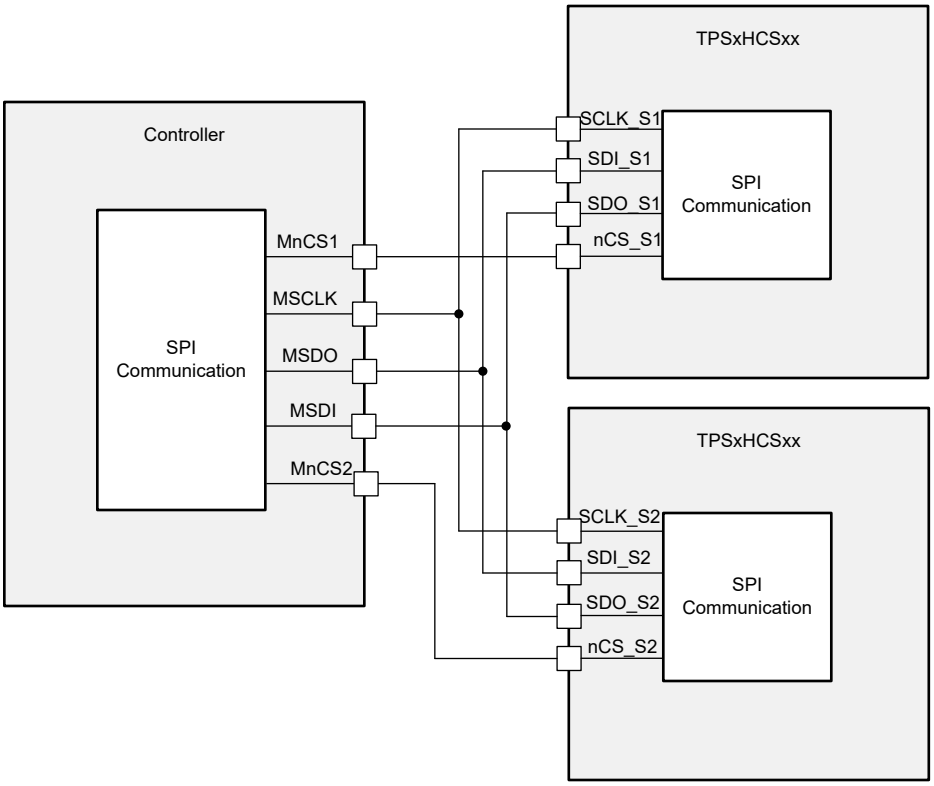


Figure 8-6. Independent Secondary Configuration (Separate nCS Signal)

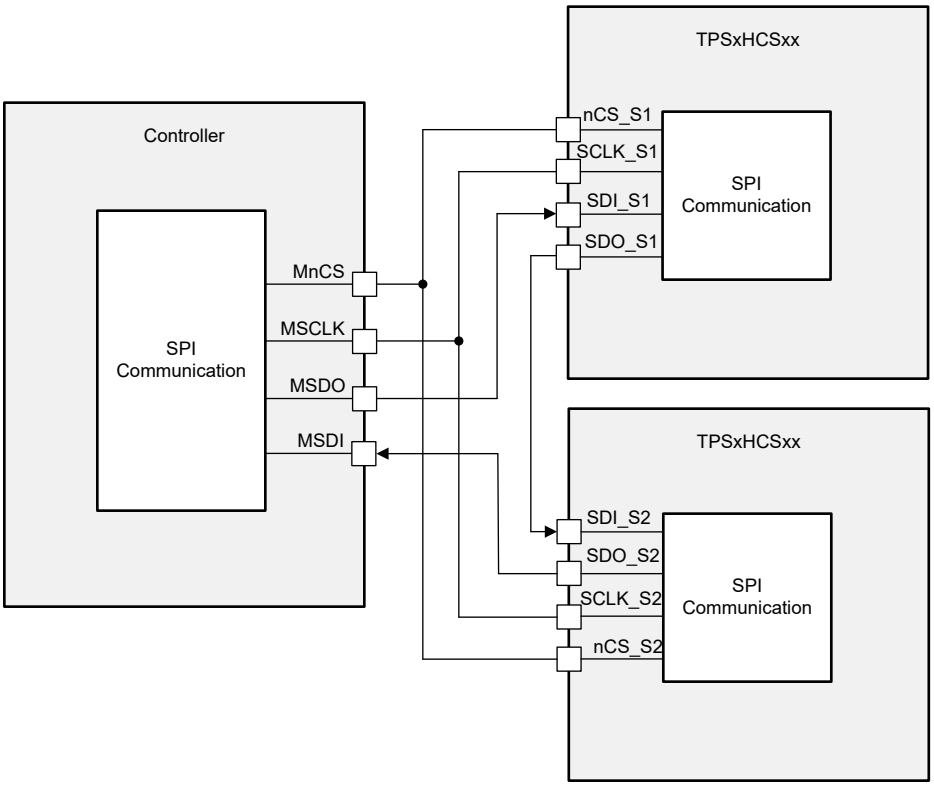


Figure 8-7. Daisy Chain Configuration

SPI Interface

The SPI interface pin behavior is described in this section

Chip Select ($\overline{CS}$ or nCS)

The system microcontroller selects the TPS2HCS08-Q1 to receive communication using the $\overline{CS}$ pin. With the $\overline{CS}$ pin in a logic LOW state, command/configuration words may be sent to the TPS2HCS08-Q1 via the serial input (SDI) pin, and the device information can be retrieved by the microcontroller via the serial output (SDO) pin. The falling edge of the $\overline{CS}$ enables the SDO output and latches the content of the GLOBAL_FAULT_TYPE register that will be sending out on SDO. The microcontroller may issue a READ command to retrieve information stored in the registers. The rising edge on the $\overline{CS}$ pin initiates the following actions:

1. Addressed registers are updated if there is no SPI communication error and if it is an SPI write command.
2. Read clear register is cleared if a READ command to this register was issued during CS = LOW.

To avoid any corrupted data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic LOW state. A clean $\overline{CS}$ signal is needed to ensure no incomplete SPI words are sent to the device. This pin is internally pulled up to the VDD rail.

System Clock

The system clock (SCLK) pin clocks the internal shift register of the TPS2HCS08-Q1. The SDI data is latched into the input shift register on the falling edge of the SCLK signal. The SDO pin shifts the device stored information out on the rising edge of SCLK. The SDO data is available for the microcontroller to read on the falling edge of SCLK.

False clocking of the shift register must be avoided to ensure validity of data and it is essential the SCLK pin be in a logic LOW state whenever $\overline{CS}$ pin makes any transition. Therefore, it is recommended that the SCLK pin gets pulled to a logic LOW state as long as the device is not accessed and the $\overline{CS}$ pin is at a logic HIGH state. When the $\overline{CS}$ is in a logic HIGH state, any signal on the SCLK and SDI pins will be ignored and the SDO pin remains as a high impedance output.

Serial Data In (SDI) and Serial Data Out (SDO)

The SDI pin is used for serial instruction data input. SDI information is latched into the input shift register on the falling edge of the SCLK when $\overline{CS}$ is low.

The SDO pin is the output from the internal shift register. This pin is internally pulled up to the VDD rail. SDO pin is high impedance when the $\overline{CS}$ pin is high. Each successive **rising** SCLK edge makes the next data bit available for the microcontroller to read on the **falling** edge of SCLK. SDO will go back to high-impedance when $\overline{CS}$ is high.

CRC Error Detection and Checking of Clocks

Setting the CRC_EN bit high enables CRC error detection. A CRC-4-ITU-Normal Check Sequence (FCS) is then sent along with each serial transaction. The 4-bit CRC is based on the normal generator polynomial X4+X+1 with CRC starting value = 1111. When CRC is enabled, the TPS2HCS08-Q1 expects a check byte appended to the SDI program/configure data that it receives.

To program a complete word, exact bits of information (shown in following table) must be enter into the device. When CRC is disabled, the IC enables register write only if exactly bits have been clocked in. When CRC is enabled, the IC enables register write only if exactly bits have been clocked in with no CRC errors. In case the word length exceeds or does not meet the required length or there is CRC errors, the SPI_ERR bit in the GLOBAL_FAULT_TYPE register is asserted to logic “1”,and the data received is considered invalid. Note the SPI_ERR bit is not flagged if SCLK is not present. The SPI_ERR will be sent back to SPI Main device on SDO during next chip access. **Note that clear on read applies only when there is no SPI error when the register is read.**

SPI Frame Format

The device uses a 24-bit frame width (when CRC is not used) with the format as shown in Figure 8-8. Please note that the 16-bit wide "Data Out" in the SDO output is always for the previous SPI command frame (Read or Write).

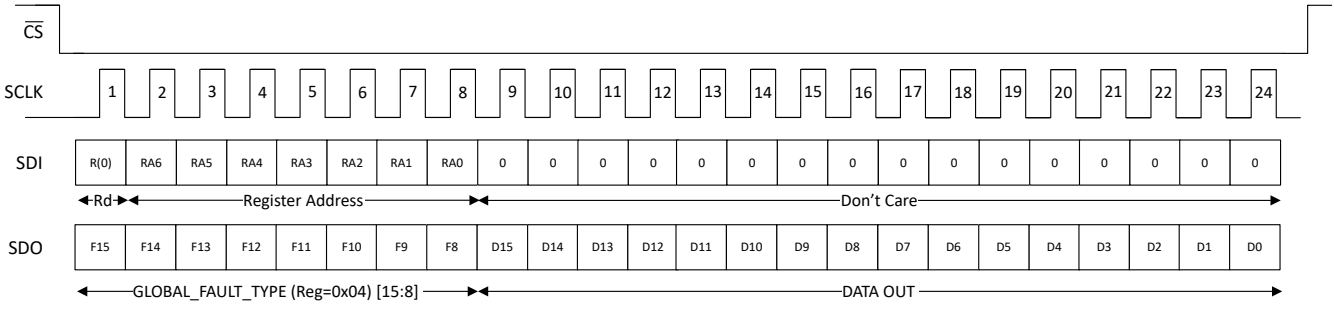


Figure 8-8. 24-bit Read, No CRC (CRC_EN=0)

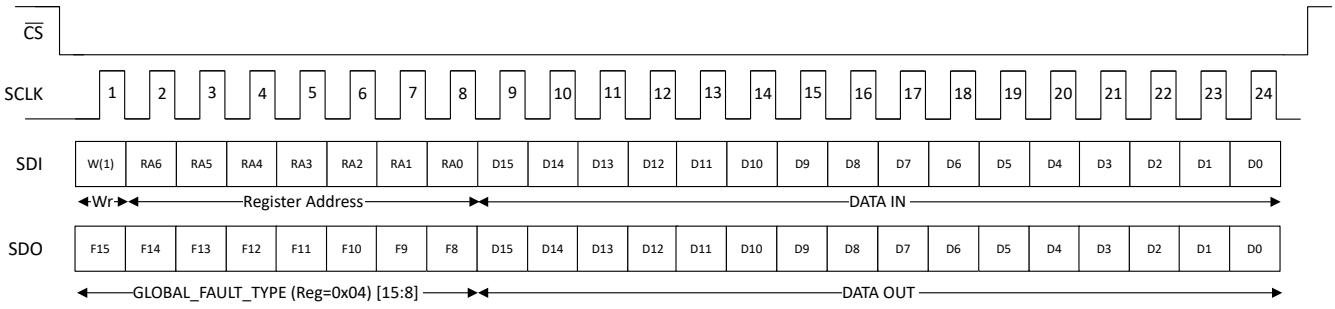


Figure 8-9. 24-bit Write, No CRC (CRC_EN=0)

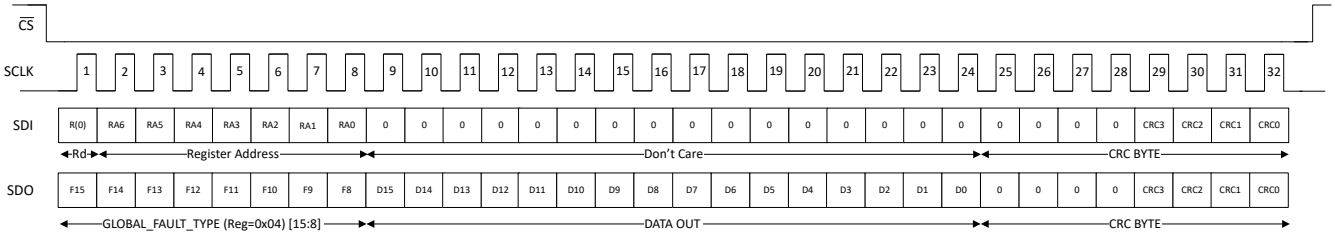


Figure 8-10. 32-bit Read, CRC Enabled (CRC_EN=1)

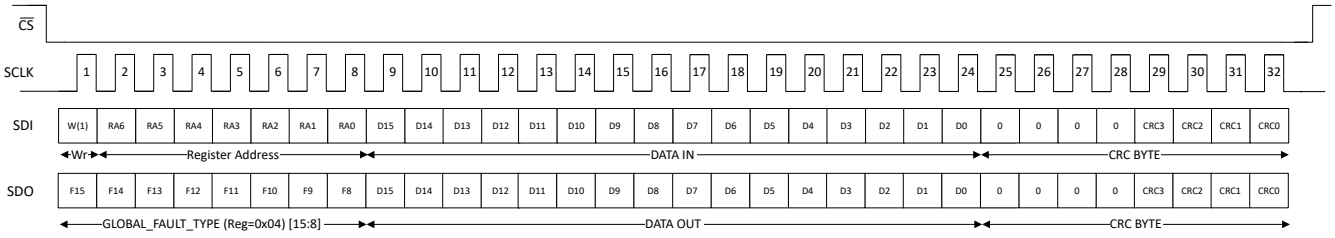


Figure 8-11. 32-bit Write, CRC Enabled (CRC_EN=1)

GLOBAL_FAULT_TYPE [15:8] Bits

The TPS2HCS08-Q1 device, outputs the GLOBAL_FAULT_TYPE [15:8] bits on the SDO header so these status bits can be continously read thr during each SPI transaction. The GLOBAL_FAULT_TYPE [15:8] bits can be configured as read clear or real-time status bits based on the FLT_LTCH_DIS bit setting in the DEV_CONFIG register. The FLT_LTCH_DIS bit however does not apply to the LPM_STATUS bit.

If FLT_LTCH_DIS = 0, then the fault bits are latched and are cleared only when the associated regsiter in the bit description is read and the fault no longer exists. Table 8-3 below highlights which registers need to be read in order to clear each of the different fault bits if the fault no longer exists. This is also detailed in each of the bit descriptions in the register map.

Table 8-3. GLOBAL_FAULT_TYPE [15:8] Bits Behavior when FLT_LTCH_DIS = 0

Bit #	Bit name	Register which needs to be read to clear the fault bit if the fault no longer exists
15	Reserved	N/A
14	Reserved	N/A
13	CH2_FLT	FLT_STAT_CH2
12	CH1_FLT	FLT_STAT_CH1
10	CHAN_OCP_I2T_TSD	FLT_STAT_CHx
9	OL_SHRT_VBB_OFF_FLT	FLT_STAT_CHx
8	GLOBAL_ERR_WRN	GLOBAL_FAULT_TYPE

If FLT_LTCH_DIS = 1, then the fault bits will not be latched and will clear when the fault no longer exists.

Figure 8-12 highlights the FLT_LTCH_DIS function of the device in regards to the GLOBAL_FAULT_TYPE [15:8] bits.

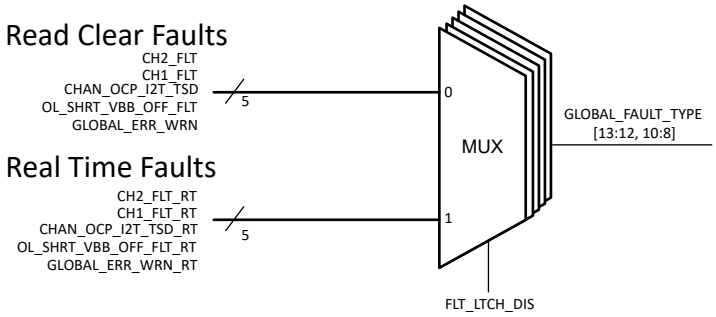


Figure 8-12. FLT_LTCH_DIS Implementation

SPI Watchdog Function

The TPS2HCS08-Q1 device offers an optional SPI watchdog function to monitor for valid SPI transactions from the host controller and loss of the VDD supply. If a valid SPI transaction does not occur in the configurable timeout period, WD_TO, then the FLT pin will go low and the WD_ERR bit in the GLOBAL_FAULT_TYPE register will be set to 1. A valid SPI transaction consists of a SPI transaction with no SPI errors and/or CRC errors (if enabled). If the VDD supply to the device drops below the VDD_UVLO threshold then SPI on the device is not operational. If the VDD supply remains below the VDD_UVLO for longer than the watchdog time period, then the device will issue a watchdog error where the WD_ERR bit will be set to 1 and the FLT pin will go low.

The watchdog function is enabled through WD_EN bit in the DEV_CONFIG register. Table 8-4 below showcases the different configurable watchdog timeout windows, WD_TO.

Table 8-4. Watchdog Timeout Settings

WD_TO Setting	Watchdog Timeout Period
00	400µs
01	400ms
10	800ms
11	1200ms

Depending on the version, the watchdog will work differently. See the below sections on how the watchdog works for TPS2HCS08A-Q1 and TPS2HCS08B-Q1.

SPI Watchdog Operation - TPS2HCS08A-Q1

If the watchdog function is enabled (WD_EN = 1) and a watchdog error occurs either do to no valid SPI transactions in the watchdog timeout window or due to a loss of VDD supply, WD_ERR = 1, FLT pin will go low, and the device will transition to the LIMP_HOME state where the output control of the channels will be set by the CHx_LH_IN bits in the DEV_CONFIG register. Note, the LIMPHOME_STAT bit will not be set to 1 as a result of watchdog error. Once a valid SPI transaction has been detected, the FLT pin will go high and the device will automatically exit the LIMP_HOME state and will revert the output control of the channel back to the CHx_ON bit. The WD_ERR bit in the GLOBAL_FAULT_TYPE register will be latched to 1 as a result of a SPI watchdog timeout error and will be cleared only after read and the error no longer exists.

SPI watchdog Operation - TPS2HCS08B-Q1

If the watchdog function is enabled (WD_EN = 1) and a watchdog error occurs either do to no valid SPI transactions in the watchdog timeout window or due to a loss of VDD supply, WD_ERR = 1 and the FLT pin will go low. The output state will not change as result of the watchdog error and the output control of the channels will continue to follow the DIx exclusively. Once a valid SPI transaction has been detected, the FLT pin will go high. The WD_ERR bit in the GLOBAL_FAULT_TYPE register will be latched to 1 as a result of a SPI watchdog timeout error and will be cleared only after read and the error no longer exists.

8.3.4 Fault Reporting

The device provides enhanced fault reporting through a $\overline{\text{FLT}}$ status pin and fault status bits through SPI.

The $\overline{\text{FLT}}$ status pin allows the device to interrupt the system when a fault has occurred on the device. The $\overline{\text{FLT}}$ status pin is an open drain output that asserts low when a fault occurs on the device. For faults which are read clear, the $\overline{\text{FLT}}$ pin will go high if the fault no longer exists and the specific register to clear the fault is read. Indication on the $\overline{\text{FLT}}$ pin can be masked for some faults through FAULT_MASK register. See the FAULT_MASK register for more details.

The device also provides fault information through SPI through a global fault register (GLOBAL_FAULT_TYPE) and channel specific fault registers (FLT_STAT_CHx) to enable the system to quickly diagnose what caused the fault in the device. The device outputs the GLOBAL_FAULT_TYPE [15:8] bits on the SDO header so these status bits can be continosly read for each SPI transaction.

For more details on each of the individual fault status bits see the GLOBAL_FAULT_TYPE and FLT_STAT_CHx registers in the register map.

Table 8-5 highlights how the device signals different events through the $\overline{\text{FLT}}$ pin and the fault status bits.

When the device is in low power mode no fault information is available through the $\overline{\text{FLT}}$ pin. If short circuit were to occur in LPM the device would protect itself then transition to ACTIVE state and then will signal fault on the $\overline{\text{FLT}}$ pin and in the fault status registers.

Table 8-5. Fault Reporting Table

Event / Fault		Detection	Protection	GLOBAL_FAULT_TYPE reporting	FLT_STAT_CHx reporting	$\overline{\text{FLT}}$ indication
FET - Overtemperature Warning		Y	N	CHx_FLT[1]	THERMAL_WRN_CHx[1]	N
FET - Temperature shutdown (TSD)		Y	Y	CHx_FLT[1] and CHAN_OCP_I2T_TSD[1]	THERMAL_WRN_CHx[1]	Y
I_{OCP} - Immediate shutdown		Y	Y	CHx_FLT[1] and CHAN_OCP_I2T_TSD[1]	ILIMIT_CHx[1]	Y
I_{CL_REG} - Current limit regulation		Y	Y	N/A	N/A	N
I_{CL_REG} - Current limit regulation - inrush period expiry		Y	Y	CHx_FLT[1] and CHAN_OCP_I2T_TSD[1]	ILIMIT_CHx[1]	Y
I_{CL_REG} - Current limit regulation - TSD		Y	Y	CHx_FLT[1] and CHAN_OCP_I2T_TSD[1]	ILIMIT_CHx[1] and THERMAL_SD_CHx[1]	Y
Channel in T_{RETRY} (LATCH_CHx = 0)		Y	N/A	N/A	FLT_CHx	Y
Channel is latched-off (LATCH_CHx = 1)		Y	N/A	N/A	LATCH_STAT_CHx and FLT_CHx	Y
Limp Home Entry (LHI = 1)		Y	N/A	GLOBAL_ERR_WRN[1] and LIMPHOME_STAT[2]	N/A	N
Active I2T Accumulation or Decrement		Y	N/A	N/A	I2T_MOD_CHx	N
I2T Shutdown		Y	Y	CHx_FLT[1] and CHAN_OCP_I2T_TSD[1]	I2T_FLT_CHx[1] and FLT_CHx	Y
VOUT shorted to VBB		Y	N	CHx_FLT[1] and OL_SHRT_VBB_OFF_FLT[1] (if OL_SVBB_EN_CHx = 01)	OL_OFF_CHx[1] (if OL_SVBB_EN_CHx = 01)	Y, unless masked
Open load	Off State	Y	N	CHx_FLT[1] and OL_SHRT_VBB_OFF_FLT[1] (if OL_SVBB_EN_CHx=10)	OL_OFF_CHx[1] (if OL_SVBB_EN_CHx=10)	Y, unless masked
	On State	Y	N	N/A	N/A	N
Reverse battery		Y	Y, with external components	N/A	N/A	N
VBB UV warning		Y	N	GLOBAL_ERR_WRN[1] and VBB_UV_WRN[1]	N/A	N
VBB_UVLO		Y	Y	GLOBAL_ERR_WRN[1] and VBB_UVLO[1]	N/A	Y
VDD_UVLO		Y	Y	GLOBAL_ERR_WRN[1] and VDD_UVLO[1]	N/A	N
Power on Reset (POR)		Y	Y	GLOBAL_ERR_WRN[1] and POR[1]	N/A	Y
Loss of GND		Y	Y, with R_{SDO} ≥ 768Ω	N/A	N/A	N
SPI Watchdog Error		Y	N/A	GLOBAL_ERR_WRN[1] and WD_ERR[1] (if WD_EN = 1)	N/A	Y, unless masked
SPI Frame Error		Y	N/A	GLOBAL_ERR_WRN[1] and SPI_ERR[1]	N/A	Y, unless masked
SPI CRC Error		Y	N/A	GLOBAL_ERR_WRN[1] and SPI_ERR[1] (if CRC_EN = 1)	N/A	Y, unless masked

1. Read-clear (RC) fault bits
2. Write 1 to clear (W1C) bits

8.3.5 SLEEP

The TPS2HCS08-Q1 device offers a SLEEP state where the device is placed into an ultra low current consumption state. When the device is in SLEEP state, both channels are OFF, registers are cleared, and all digital circuits are powered off. The device will transition to this state if VBB < VBB_UVLO and VDD < VDD_UVLO or if VDD drops below VDD_UVLO while in either MANUAL_LPM or AUTO_LPM state. The device can manually be put into SLEEP state by writing a 1 to the SLEEP bit in the SLEEP register.

The device can be woken from the SLEEP state through the CSN pin going low. There are two methods to wake the device up from SLEEP through the CSN pin:

1. Pulse the CSN pin low for t < t_{READY}
2. Hold the CSN pin low for at least t_{READY} and continue to hold CSN pin low through the first SPI transaction

Both methods above will result in the device waking up without a SPI_ERR fault. A dummy SPI transaction could be used to sastify method #1 if the dummy SPI transaction is completed in t < t_{READY}. Figure 8-13 below shows examples of the two proper wakeup scenarios which will result in no SPI_ERR fault and one improper wakeup scenario which will result in a SPI_ERR fault.

Upon wakeup from SLEEP state, the values in the registers will be set to their reset values detailed in the register map below. Additionally, the FLT pin will be asserted low and the POR, VDD_UVLO, and VBB_UVLO fault bits will be asserted and will be cleared when the GLOBAL_FAULT_TYPE register is read if none of these faults currently exist when read.

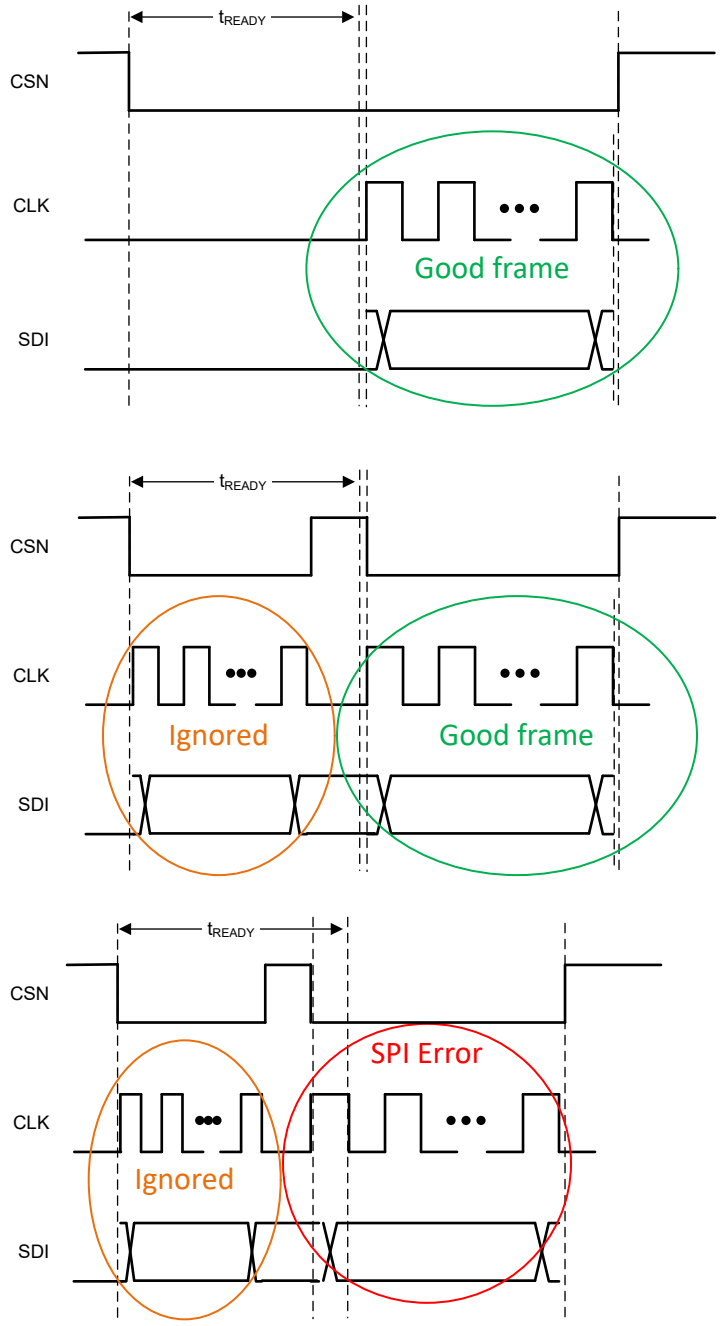


Figure 8-13. Startup Communication Timing

8.3.6 CONFIG/ACTIVE

The CONFIG/ACTIVE state is where the device stays during normal operation when the outputs are OFF (CONFIG) or ON (ACTIVE). The difference between the two is that in the CONFIG state (with the outputs OFF) all of the registers can be configured. In the ACTIVE state with the outputs ON, the parallel configuration of the channel cannot be changed (PARALLEL_12 bit in the DEV_CONFIG register). The configuration registers (especially ones needed to successfully enable the channel) are expected to be written to before the outputs can be turned ON, when transitioning from the SLEEP state (and all the registers are lost). However, the configuration registers are retained while in the LPM state and so the device does not need to be reconfigured while tranisitioning from the LPM state to the ACTIVE state. The quiescent current draw from VBB, ($I_{Q,VBB}$) and

VDD, ($I_{Q,VDD}$) is higher than in the other states to support the load and device diagnostics. SPI communication and diagnostics checks are fully supported in this state.

The device can be transitioned into the CONFIG state from the SLEEP state by the CSN pin going low (a dummy SPI command serves this purpose). The device completes the transition through all initializations and functional safety checks. The device transitions to and from the LIMP HOME state depending on the internal SPI watchdog monitor and the status of the LHI input pin. The device can transition into and out of the LPM state by a write to the LPM register.

In the CONFIG state, the device utilizes a gate to source pulldown to achieve the configured slew rate when the channel is enabled and disabled. As a result, when the channel is off there is a 1µA bias path to VOUT which creates a 1µA leakage current to VOUT. If there is no load on the output this can cause the output to float up. To reduce the open load VOUT voltage, the R_{SHRT_VBB} pulldown resistor can be enabled to reduce the output voltage to low levels. The R_{SHRT_VBB} pulldown resistor can be enabled through the OL_SVBB_EN_CHx [1:0] bits in the CHx_CONFIG registers. In SLEEP and LPM states, to achieve the lowest IQ the device instead utilizes a gate to ground pulldown so the 1µA bias path doesn't exist in these states.

8.3.7 LIMP_HOME State (Version A only)

The LIMP_HOME state is intended to place the outputs in the desired safe state when there is a failure of SPI communication (if WD_EN=1), loss of VDD supply (if WD_EN = 1), or another system-level fault which causes the LHI pin to go high. When the ECU detects a system-level fault, the system controller raises the LHI pin high to signal to the device to go to the LIMP_HOME state. If the device detects a SPI watch dog timeout error and thus a SPI communication error, the device goes to the LIMP HOME state. In both cases, the output state is as specified on a per channel basis through the CHx_LH_IN bits of the DEV_CONFIG register. The settings for the CHx_LH_IN bits are detailed in Table 8-6.

Table 8-6. CHx_LH_IN bit settings

Setting	Setting Description
00	Output state is set by the DI pin when in LIMP_HOME state • If DI = HI, then CHx = ON in LIMP_HOME state • If DI = LO, then CHx = OFF in LIMP_HOME state
01	Keeps the same output state from CHx_ON bit when entering LIMP_HOME state
10	Output will be OFF in LIMP_HOME state
11	Output will be ON in LIMP_HOME state

The register values are retained in the LIMP HOME state, which means that the appropriate overcurrent protection threshold values, duration and retry behavior are all set with the outputs corresponding to the state based on the CHx_LH_IN bits. If the device entered into the LIMP_HOME state as a result of the LHI pin going high, the LIMPHOME_STAT bit in the GLOBAL_FAULT_TYPE register is set to 1 which lets the MCU or controller know that the device is in the LIMP HOME state. The MCU cannot write to any of the registers until the device is out of the LIMP HOME state.

If the device entered the LIMP_HOME state as a result of LHI going high, the device transitions out of the LIMP_HOME state when the LHI pin is brought low and a is written to the LIMPHOME_STAT bit in the GLOBAL_FAULT_TYPE register. The register settings are reatined while in LIMP HOME state and the device transitions back into normal operation in the ACTIVE state.

If the device entered LIMP_HOME state as a result of a SPI watchdog timeout error, the outputs will be set according to the CHx_LH_IN bits but the LIMPHOME_STAT bit will not be set to 1. The device will automatically exit the LIMP_HOME state if a valid SPI transaction is detected. The WD_ERR bit in the GLOBAL_FAULT_TYPE register will be latched to 1 as a result of a SPI watchdog timeout error and can be cleared only after read and the error no longer exists.

LIMP HOME State Exceptions

The device can receive an LHI signal during cap charging or inrush duration. If the desired state is ON, the device continues cap charging per programmed register values. If the desired state is OFF, then the channel is turned off.

8.3.8 Battery Supply Input (VBB) Under-voltage

The device includes a battery supply (VBB) under-voltage monitoring and a VDD under-voltage monitoring. Some of the internal reference and regulators and the output FETs are turned OFF when the VBB supply falls below the V_{BB_UVLOF} threshold. When the input VBB supply is lost, the device relies on the VDD supply input to keep the digital functions and registers alive. The SPI communication is also available as long as the VDD input is greater than V_{DD_UVLOF}. The VBB_UVLO fault and the VDD_UVLO bits can be read over SPI from the GLOBAL_FAULT_TYPE register. The VBB_UVLO and VDD_UVLO fault bits are latched if there is a fault for either and are cleared on read if the UVLO condition no longer exists. The following table indicates the device operation under a loss of supply condition.

Table 8-7. Device Operation Under Supply Loss Condition

	VDD < VDD_UVLO	VDD > VDD_UVLO
VBB < VBB_UVLO	• Channels are OFF • Registers are reset and digital core OFF • SPI communication not possible	• Channels are OFF • Registers are maintained and digital core is ON • SPI communication possible
VBB > VBB_UVLO	• If WD_EN = 1, – Device is in LIMP_HOME state after watchdog timeout expires, channels output states are set by the CHx_LH_IN bits. • If WD_EN = 0 – Channels are based on CHx_ON setting • Registers are maintained and digital core is ON • SPI communication not possible	• Channel output states are set by the CHx_ON bits. • Registers are maintained and digital core is ON • SPI communication possible

The register information may be lost when both the VBB and VDD supplies are below the POR and UVLO conditions respectively. The device is able to indicate with a register read of the POR bit in the GLOBAL_FAULT_TYPE register that a reset of the digital has occurred. This will ensure that the SPI master can identify that the register contents are all lost and the configuration registers needs to be rewritten. It is recommended that the bit be read if any under-voltage fault is detected.

8.3.9 LOW POWER MODE (LPM) States

The device offers two low power mode (LPM) states where the device can remain on but the device operates in a low quiescent current (IQ) state to extend battery life. The device offers a manual LPM (MANUAL_LPM) state which can be entered through a SPI write to the LPM register and an automatic LPM (AUTO_LPM) state which can be entered automatically if the output current in the enabled channels is below a certain threshold for $t_{STBY\_LPM\_AUTO}$.

When the device is in either LPM state, SPI writes and reads are only available to the LPM register. In either LPM state, the device can continue to pass SPI data to successive devices in a daisy chain configuration and the status bits in the SDO frame can still be read. When the device transitions in and out of LPM, the fault bits in the SDO frame will update to alert the system the device has exited LPM mode.

A valid VDD voltage greater than V_{DD_UVLOF} is required for the device to remain in either of the LPM states. If the VDD voltage is removed in either LPM states the device will transition to the SLEEP state which in turn disables the outputs and clears the registers.

In MANUAL_LPM state, the device disables all diagnostics as well as the watchdog timer and I2T protection to help reduce the IQ of the device. Once the device exits MANUAL_LPM, the diagnostics which were enabled prior to LPM entry will automatically be re-enabled. I2T protection and the watchdog timer will also be re-enabled

after LPM exit. For AUTO_LPM state, the system must first disable the watchdog timer and all ADC diagnostics except ISNS before the device can transition into the AUTO_LPM state. The device will automatically disable the I2T protection and ISNS for AUTO_LPM state and will re-enable these functions when the device exits the AUTO_LPM state to the ACTIVE state. In terms of protection, short-circuit protection remains enabled in the both the LPM states. Different short circuit thresholds are used in the LPM states compared to the short circuit thresholds in ACTIVE state.

When in either of the LPM states, the device automatically responds to load current increases by transitioning to active state. If the current increase is too high the device will trip its short circuit protection. For MANUAL_LPM state, the device provides a wake signal to the microcontroller (which is in sleep mode) to wake the system up through the $\overline{\text{FLT}}$ / $\overline{\text{WAKE\_SIG}}$ pin for either load increase scenario. For the AUTO_LPM state, only a load increase above the LPM short-circuit threshold (I_{SCP_AUTO}) will trigger the $\overline{\text{FLT}}$ / $\overline{\text{WAKE\_SIG}}$ pin to be pulled low. If a load increase in AUTO_LPM is above the exit threshold ($I_{EXIT\_LPM\_AUTO}$) but below the $I_{SCP\_LPM\_AUTO}$ threshold, the device will not pull the $\overline{\text{FLT}}$ / $\overline{\text{WAKE\_SIG}}$ pin low. For both LPM states, the device will only signal an overcurrent protection fault if the overcurrent is confirmed in the ACTIVE state as well.

If needed, the system can manually wake up the device from the LPM states through different SPI writes depending on the LPM state that the device is in. If LHI goes high in either of the LPM states, the device will exit LPM and will transition to ACTIVE state and then to LIMP_HOME state.

Table 8-8 below highlights some of the major differences between the two low power modes. For more information on how each LPM state operates, see the below sections on the MANUAL_LPM and AUTO_LPM states.

Table 8-8. LPM Characteristics

Mode Type	Entry Method	Specification	Description	Typical	Unit
MANUAL_LPM	Write 1 to LPM bit in LPM register	I_{Q,VBB,LPM_MAN}	Both channels enabled	6.42	µA
		I_{Q,VDD,LPM_MAN}	Both channels enabled	15.6	µA
		R_{ON,LPM_MAN}	R_{ON} in MANUAL_LPM	25.4	mΩ
		$I_{EXIT\_LPM\_MAN}$	IEXIT_LPM_MAN_CHx = 00	0.53	A
			IEXIT_LPM_MAN_CHx = 01	0.7	
			IEXIT_LPM_MAN_CHx = 10	0.165	
			IEXIT_LPM_MAN_CHx = 11	0.35	
		$I_{SCP\_LPM\_MAN}$	short-circuit threshold in MANUAL_LPM	4	A
AUTO_LPM	Automatic entry if AUTO_LPM_ENTRY =1	I_{Q,VBB,LPM_AUTO}	Both channels enabled	11.6	µA
		I_{Q,VDD,LPM_AUTO}	Both channels enabled	15.6	µA
		R_{ON,LPM_AUTO}	R_{ON} in AUTO_LPM	8.8	mΩ
		$t_{STBY\_LPM\_AUTO}$	standby time before entry into AUTO_LPM if $I_{OUTx} < I_{ENTRY\_LPM\_AUTO}$	20	ms
		$I_{ENTRY\_LPM\_AUTO}$	I_{OUTx} current to enter AUTO_LPM	0.95	A
		$I_{EXIT\_LPM\_AUTO}$	I_{OUTx} current to exit AUTO_LPM	1.05	A
		$I_{SCP\_LPM\_AUTO}$	short-circuit threshold in AUTO_LPM	13.7	A

8.3.9.1 MANUAL_LPM State

The MANUAL_LPM state provides a mode where the system can manually put the device into a low IQ state while keeping the channels on, if desired, and protected through short-circuit protection. To enter the MANUAL_LPM state the LPM bit in the LPM register needs to be set to 1. Depending on the version, before the LPM command is written to enter MANUAL_LPM the device needs to meet the following conditons:

- Version A
  - In active or config state with no channel state changes through CHx_ON bits
  - Enabled channels are not in the inrush period
  - $I_{OUT} < I_{EXIT\_LPM\_MAN}$ for enabled channels

  - THERMAL_WRN_CHx = 0
- Version B
  - In active or config state with no channel state changes through DIx pins
  - Enabled channels are not in the inrush period
  - $I_{OUT} < I_{EXIT\_LPM\_MAN}$ for enabled channels
  - THERMAL_WRN_CHx = 0

If the above conditions are not met the device will not transition to the MANUAL_LPM state and the MANUAL_LPM_ENTRY bit will be set back to 0 and the LPM_STATUS bit in the SDO frame will remain 0. If all conditions are met and 1 is written to the LPM bit the device will update the LPM_STATUS bit in the SDO frame and then will transition to the MANUAL_LPM state in t_{LPM_ENTRY}.

In the MANUAL_LPM state, the smaller internal FET is used to provide the lowest IQ. The R_{ON} for the smaller FET is defined by the R_{ON,LPM_MAN} in the electrical characteristics section. Given the smaller FET is used in MANUAL_LPM, the exit thresholds and the short-circuit thresholds will be lower compared to the AUTO_LPM state where the larger internal FET is used.

System Wakeup from MANUAL_LPM

For TPS2HCS08A-Q1, the MCU or controller can write a 0 to the LPM bit in the LPM register to manually transition the device out of MANUAL_LPM state to the ACTIVE state. The device will evaluate the AUTO_LPM_EXIT_CHx bits when a 0 is written to the LPM bit to exit the MANUAL_LPM state. If either AUTO_LPM_EXIT_CHx are 1 then the corresponding channel will be enabled if not already enabled when the device is in ACTIVE state.

For TPS2HCS08B-Q1, the MCU or controller can also write a 0 to the LPM bit in the LPM register to manually transition the device out of MANUAL_LPM state to the ACTIVE state except the TPS2HCS08B-Q1 device will not evaluate the AUTO_LPM_EXIT_CHx bits. The AUTO_LPM_EXIT_CHx bits have no effect on the TPS2HCS08B-Q1. The TPS2HCS08B-Q1 will also transition out of the MANUAL_LPM state to ACTIVE state if DI1 or DI2 change states in MANUAL_LPM state.

Automatic Exit from MANUAL_LPM

When in MANUAL_LPM state, the device will wake itself up and the system through the FLT / WAKE_SIG pin when there is a load current increase beyond the programmed $I_{EXIT\_LPM\_MAN}$ threshold. The FLT / WAKE_SIG pin will pulse low for t_{WAKE_SIG} to alert the system that the device has exited MANUAL_LPM and transitioned to the ACTIVE state. The threshold to switchover for each channel can be programmed through the MAN_LPM_EXIT_CURR_CHx bits to the following wake up settings detailed in Table 8-9.

If there is a larger ECU load current demand increase or output short circuit above the $I_{SCP\_LPM\_MAN}$, the device will turn off the smaller internal FET for that channel and will retry with the larger MOSFET in t_{RETRY_LPM} with I_{OCP} set as the overcurrent protection threshold.

The additional load current demand and the transition to the active state is signaled to the MCU or the System Basis Chip (SBC) with a falling edge of the FLT or WAKE_SIG (active low pull-up resistor to VDD) that can be used as an interrupt by the MCU or the SBC to wake up the system. The device can then be polled over SPI to see if the FLT or WAKE_SIG pin transition was caused by the load ECU current demand or a short circuit. The device registers a fault as over-current protection fault only if the overcurrent is also confirmed in the ACTIVE state.

Depending on the load step magnitude, the device will transition to the ACTIVE state in different ways. Figure 8-14, Figure 8-15, and Figure 8-16 showcase how the device responds to different load step magnitudes.

Once the device transitions to ACTIVE because of a load current increase, the LPM bit in the LPM register remains set to 1. To go to LPM state again, the LPM bit in the LPM register needs to be set to 0 and then to 1 again.

Table 8-9. Load Wake Up Settings - MANUAL_LPM State

MAN_LPM_EXIT_CURR_CHx in LPM register	Typ	Unit
00 (default)	0.53	A
01	0.7	A
10	0.165	A
11	0.35	A

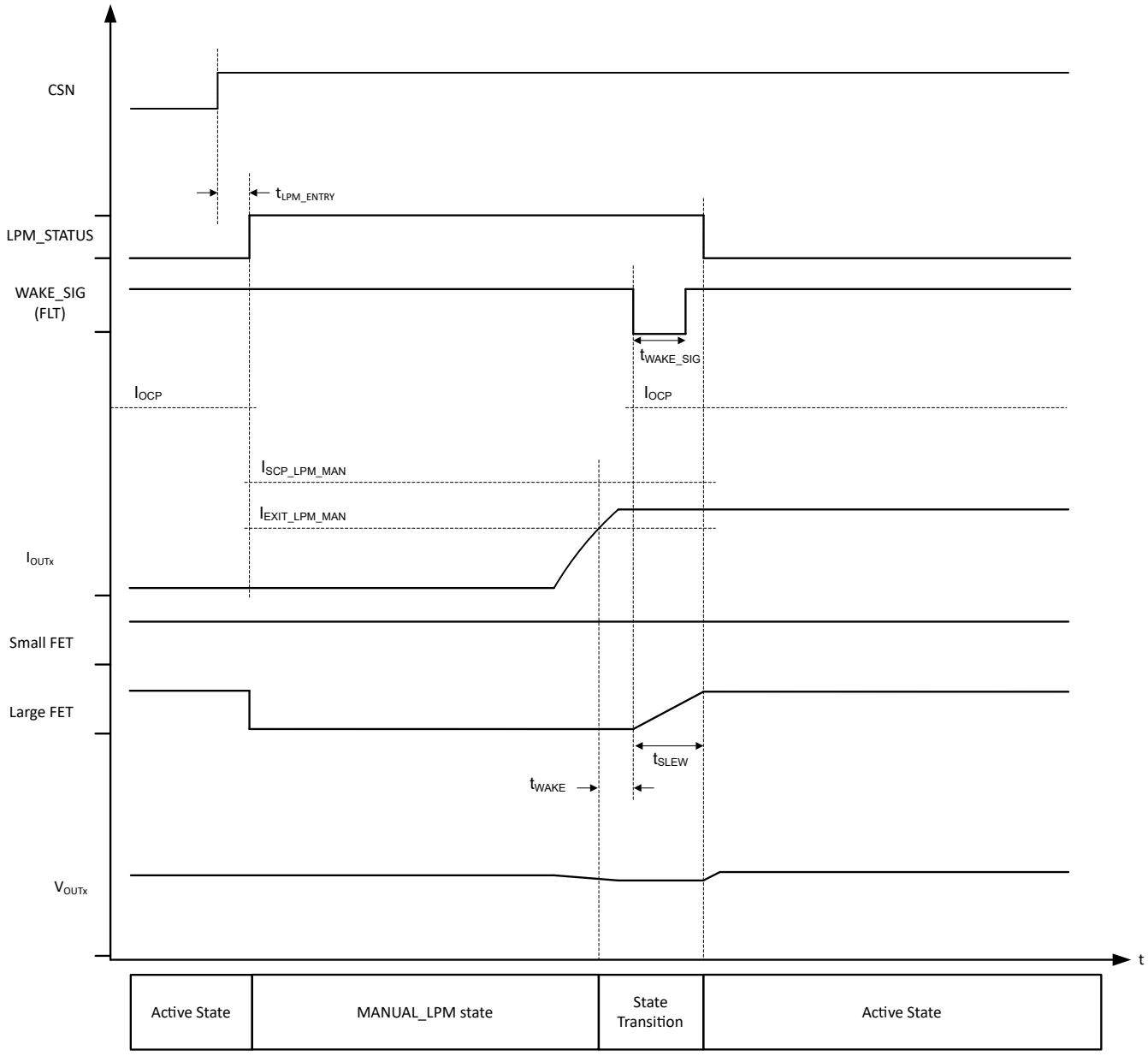


Figure 8-14. Load Increase Above $I_{EXIT\_LPM\_MAN}$ and Below $I_{SCP\_LPM\_MAN}$ in MANUAL_LPM state

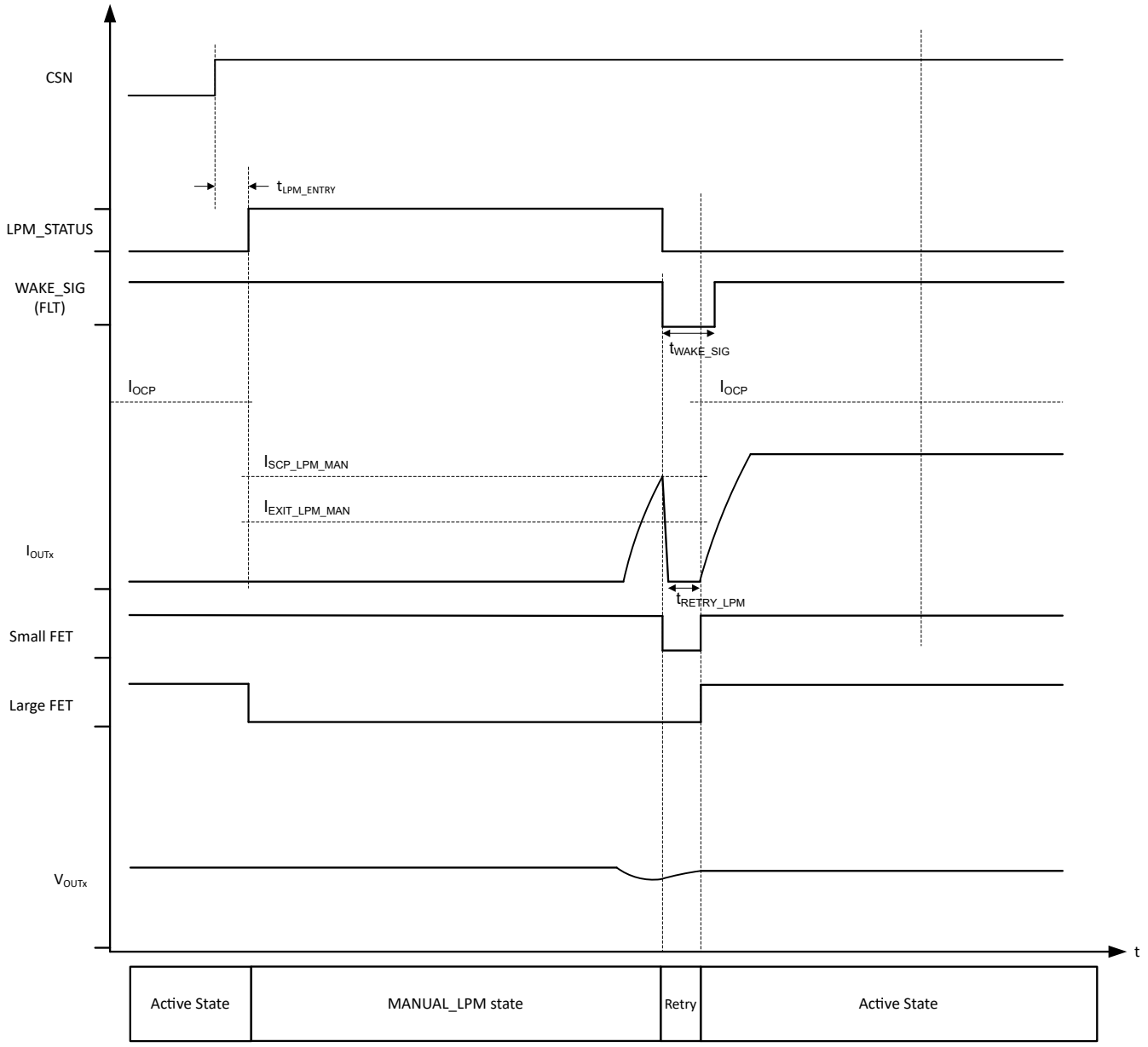


Figure 8-15. Load Increase Above $I_{SCP\_LPM\_MAN}$ and Below I_{OCP} in MANUAL_LPM State

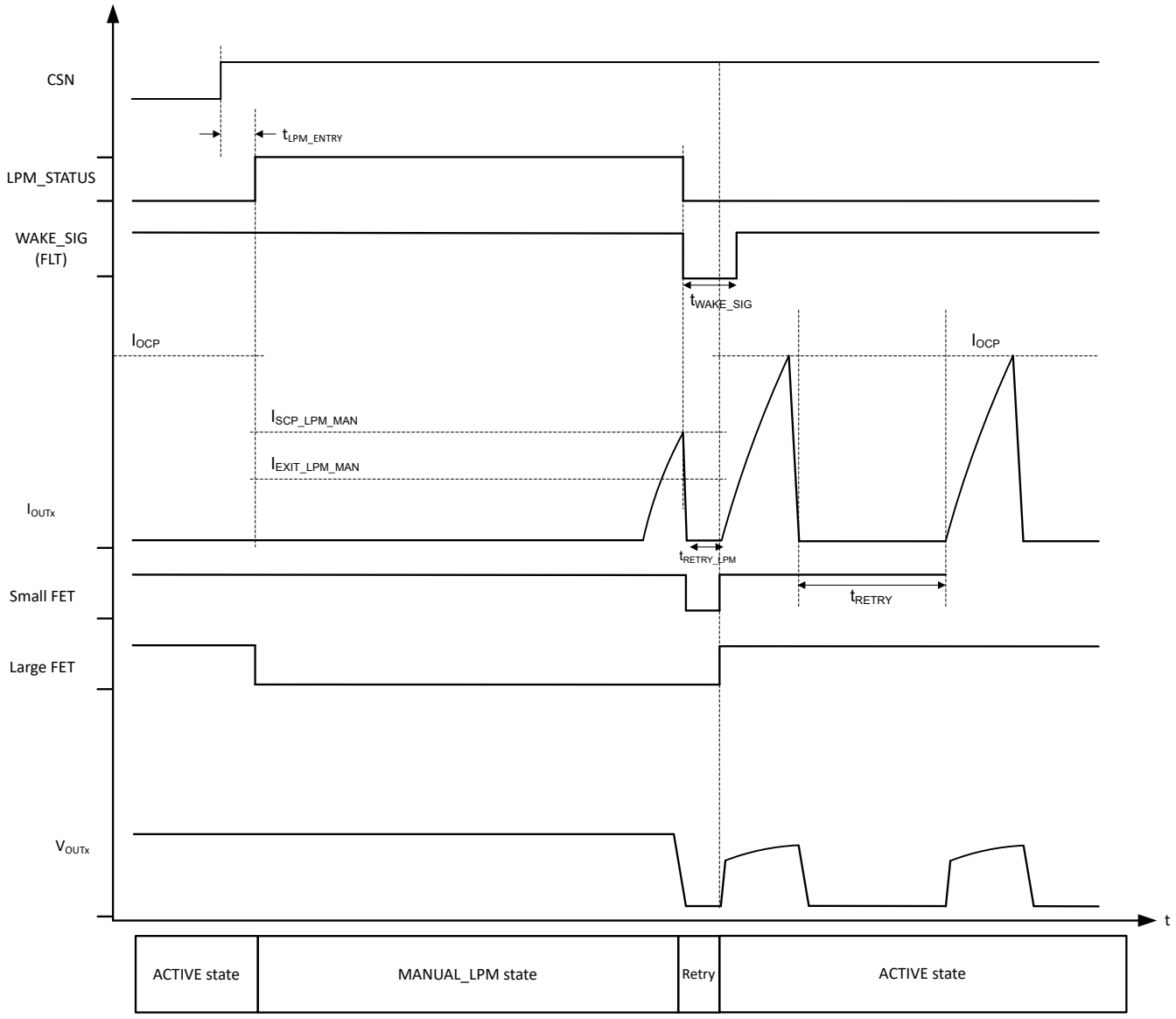


Figure 8-16. Load Increase Above I_{OCP} in MANUAL_LPM State

8.3.9.2 AUTO_LPM State

The AUTO_LPM state provides a mode where the device can automatically transition to a low IQ state while keeping the channels on, if desired, and protected through short-circuit protection. Depending on the device version used, to enter the AUTO_LPM state the AUTO_LPM_ENTRY bit in the DEV_CONFIG register needs to be set to 1 and the following conditions need to be met for at least $t_{STBY\_LPM\_AUTO}$:

- Version A
  - In active or config state with no channel state changes through CHx_ON bits
  - Enabled channels are not in the inrush period
  - All ADC diagnostics (VSNS, VBBSNS, TSNS, and VDS_SNS) are disabled except ISNS
  - $I_{OUT} < I_{ENTRY\_LPM\_AUTO}$ for enabled channels
  - AUTO_LPM_EXIT_CHx bits must both be set to 0
  - THERMAL_WRN_CHx = 0
  - Watchdog timer is disabled (WD_EN = 0)
  - No faults exist on the device

- Version B
  - In active or config state with no channel state changes through DIx pins
  - Enabled channels are not in the inrush period
  - All ADC diagnostics (VSNS, VBBSNS, TSNS, and VDS_SNS) are disabled except ISNS
  - $I_{OUT} < I_{ENTRY\_LPM\_AUTO}$ for enabled channels
  - AUTO_LPM_EXIT_CHx bits must both be set to 0
  - THERMAL_WRN_CHx = 0
  - Watchdog timer is disabled (WD_EN = 0)
  - No faults exist on the device

Once the conditions are met the device will update the LPM_STATUS bit in the SDO frame/ GLOBAL_FAULT_TYPE register and the LPM_STATUS_1 bit in the GLOBAL_FAULT_TYPE register before entering the AUTO_LPM state to alert the system that device has transitioned to AUTO_LPM. The device will enter AUTO_LPM state in t_{LPM_ENTRY}.

In the AUTO_LPM state, the larger internal FET is used to allow for larger load steps. The R_{ON} for the larger internal FET is defined by the R_{ON,LPM_AUTO} in the electrical characteristics section. The IQ in AUTO_LPM will be higher compared to the MANUAL_LPM state. In AUTO_LPM, the entry threshold is specified by $I_{ENTRY\_LPM\_AUTO}$ and the exit threshold is specified by $I_{EXIT\_LPM\_AUTO}$.

System Wakeup from AUTO_LPM

For TPS2HCS08A-Q1, the MCU or controller can write a 1 to the either or both AUTO_LPM_EXIT_CHx bits to manually transition the device out of the AUTO_LPM state to the ACTIVE state. If either AUTO_LPM_EXIT_CHx are 1 then the corresponding channel will be enabled if not already enabled when the device is in ACTIVE state. For TPS2HCS08A-Q1, both AUTO_LPM_EXIT_CHx bits have to be set back to 0 before the device is allowed to transition back to the AUTO_LPM state.

For TPS2HCS08B-Q1, the AUTO_LPM_EXIT_CHx bits have no effect on the TPS2HCS08B-Q1. The system can manually transition the TPS2HCS08B-Q1 device out of AUTO_LPM by changing the state of DI1 or DI2 or both in AUTO_LPM state.

Automatic Exit from AUTO_LPM

When in AUTO_LPM state, the device will wake itself up and will change the LPM_STATUS bit to 0 when there is a load current increase beyond the $I_{EXIT\_LPM\_AUTO}$ threshold. The LPM_STATUS_1 bit in the GLOBAL_FAULT_TYPE register is set to 1 when in AUTO_LPM state and is read clear which enables the system to tell if the device had transitioned to the AUTO_LPM state since the GLOBAL_FAULT_TYPE register was last read. An ECU load current demand increase above the $I_{EXIT\_LPM\_AUTO}$ threshold will activate the transition to the ACTIVE state. Note, in this load increase scenario the device will not pull the $\overline{FLT}$ / $\overline{WAKE\_SIG}$ low.

If there is a larger ECU load current demand increase or output short circuit above the $I_{SCP\_LPM\_AUTO}$, the device will turn off the internal FET for that channel and will retry in t_{RETRY} with I_{OCP} set as the overcurrent protection threshold. In this scenario, the device will pull the $\overline{FLT}$ / $\overline{WAKE\_SIG}$ pin low when there is a load current increase beyond the $I_{SCP\_LPM\_AUTO}$ threshold. The device registers a fault as over-current protection fault only if the overcurrent is also confirmed in the ACTIVE state.

Depending on the load step magnitude, the device will transition to the ACTIVE state in different ways. Figure 8-17, Figure 8-18, and Figure 8-19 showcase how the device responds to different load step magnitudes.

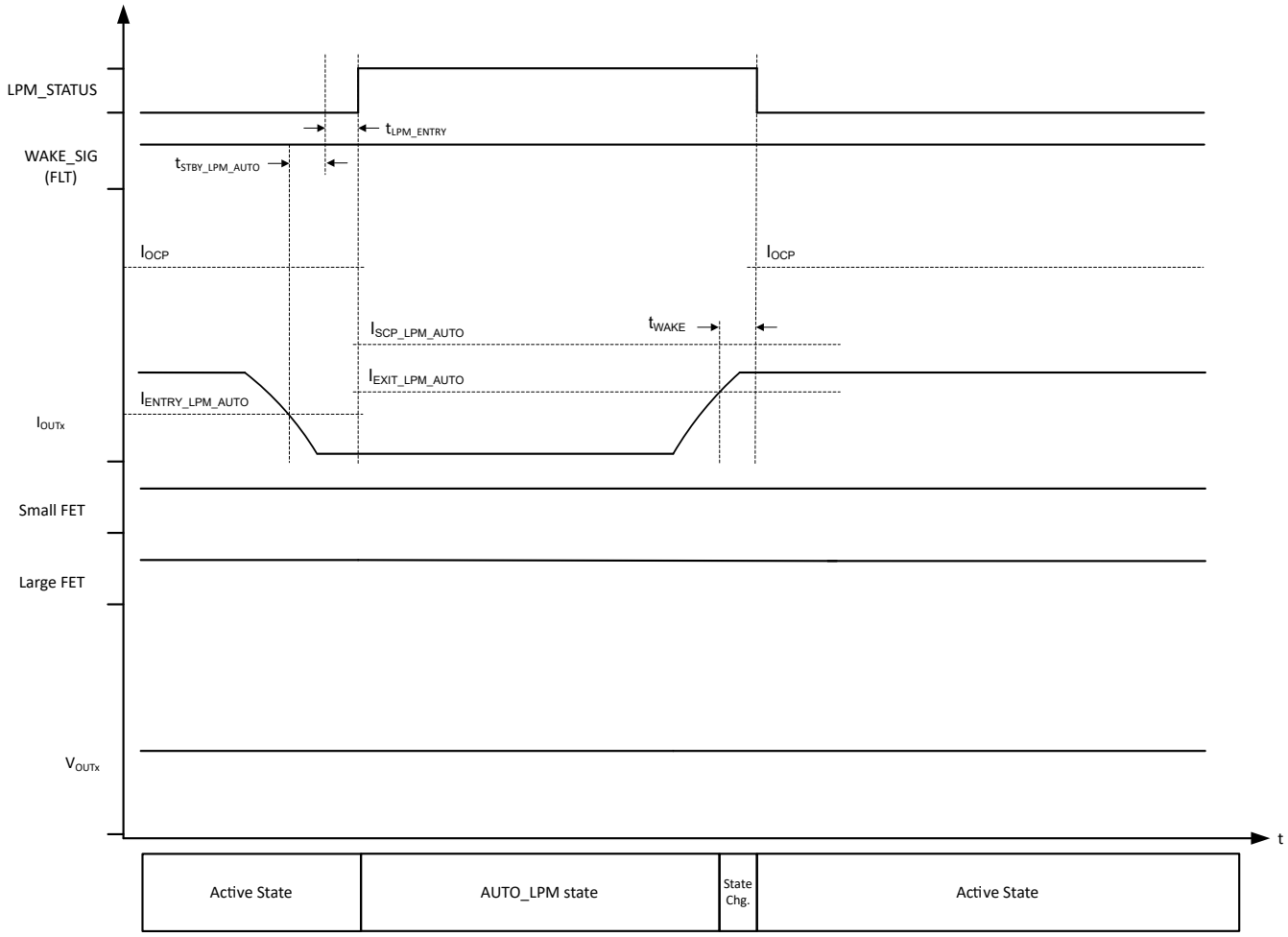


Figure 8-17. Load Increase Above $I_{EXIT\_LPM\_AUTO}$ and Below $I_{SCP\_LPM\_AUTO}$ in AUTO_LPM State

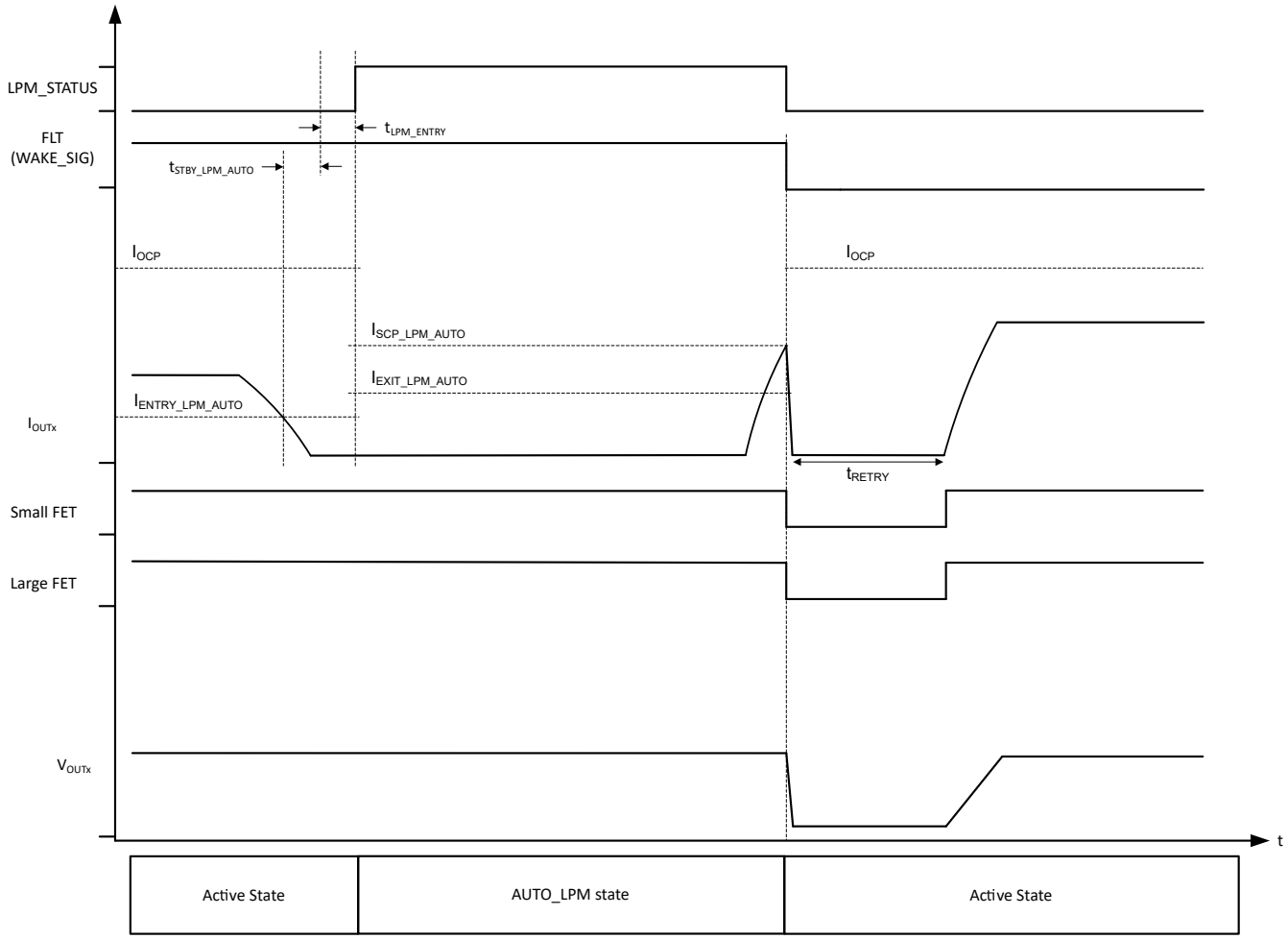


Figure 8-18. Load Increase Above $I_{SCP\_LPM\_AUTO}$ and Below I_{OCP} in AUTO_LPM State

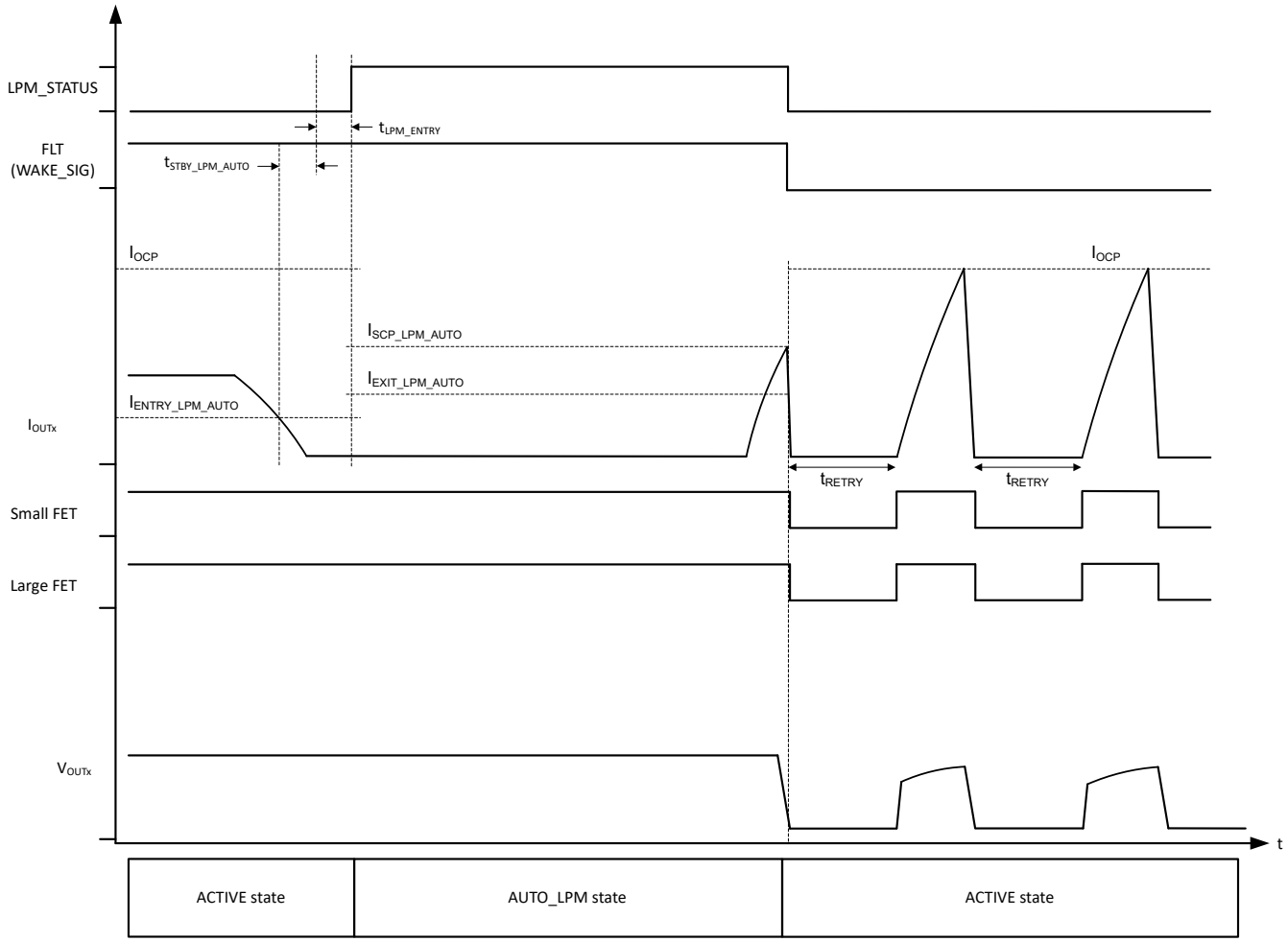


Figure 8-19. Load Increase Above I_{OCP} in AUTO_LPM State

8.4 Feature Description

8.4.1 Protection Mechanisms

8.4.1.1 Overcurrent Protection

The TPS2HCS08-Q1 device offers the following functions to protect the device from different overcurrent events:

- Capacitive load charging in inrush period
- Immediate shutdown overcurrent protection (I_{OCP})
- Programmable fuse protection (or I2T protection) in steady state (if enabled)
- Thermal shutdown (T_{REL} and T_{ABS})
- Short-circuit protection ($I_{SCP\_LPM\_MAN}$ or $I_{SCP\_LPM\_AUTO}$) in LPM states

In regards to overcurrent protection, the device has two operation modes, an optional inrush period at channel startup and during steady state operation. The optional inrush period can be configured to allow the device to handle different inrush currents such as bulbs, motor stall currents, or capacitive loads at the initial turn on of a channel. The CAP_CHRG_CHx, INRUSH_DURATION_CHx, and INRUSH_LIMIT_CHx bits in the ILIM_CONFIG_CHx registers control the operation of the device in the inrush period. Steady state operation takes over after the inrush period has completed. During steady state operation, overcurrent protection (I_{OCP}) is active and I2T protection is active (if enabled).

During the inrush period all voltage sensing (VBB, VOUT, and VDS) and FET temperature sensing can be used if enabled. Current sensing is only available after the inrush period has completed and the device is in steady

state operation. All voltage sensing, FET temperature sensing, and current sensing is available in the steady operation.

Figure 8-20 provides an overview of the overcurrent protection in the optional inrush period and steady state operation.

For more details on the different protections available in the inrush period and in steady state, see the following sections. Overcurrent protection in the LPM states is covered in the LPM section.

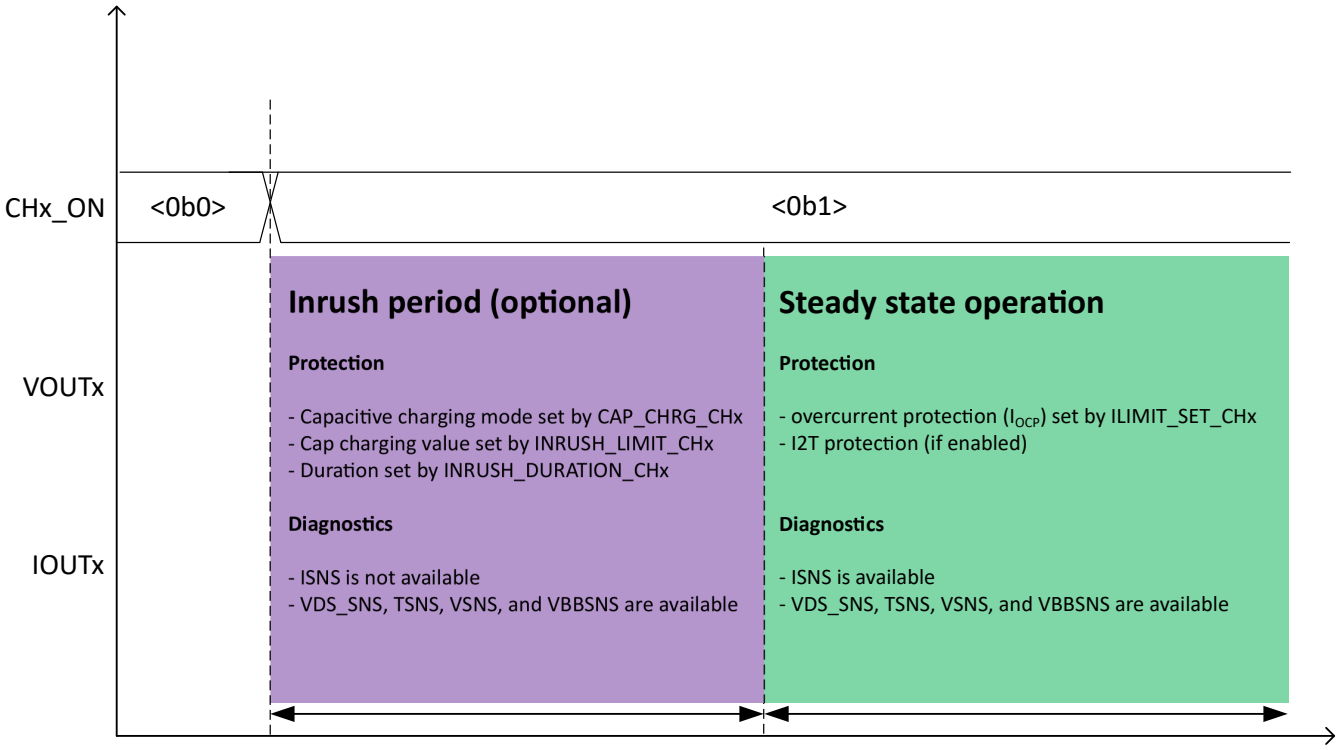


Figure 8-20. Overcurrent protection modes overview

8.4.1.1.1 Inrush Period - Overcurrent Protection

The inrush period is an optional mode of the device where it can be configured to allow the device to handle different inrush currents such as bulbs, motor stall currents, or capacitive loads at the initial turn on of a channel. The inrush period can be configured through the CAP_CHRG_CHx, INRUSH_DURATION_CHx, and INRUSH_LIMIT_CHx bits in the ILIM_CONFIG_CHx registers. If the inrush period is enabled, it will take effect in both the ACTIVE state and the LIMP_HOME state if a channel is enabled in either of these states.

The device offers two different ovecurrent protection settings in the inrush period which can be set through the CAP_CHRG_CHx bits:

- No capacitive charging - immediate shutdown overcurrent protection (I_{OCP}) only
- Current limit regulation (I_{CL_REG})

The no capacitive charging setting, enables the device to have a different overcurrent protection (I_{OCP}) value in the inrush period compared to steady state to allow for bulb current inrush or motor stall current. The current limit regulation mode, allows for the device to charge up large capacitances such as input capacitors on downstream ECUs. Depending on the CAP_CHRG_CHx bit settings, the values of the INRUSH_LIMIT_CHx will change. The overcurrent protection for each channel is independent and can be set on an per channel basis. Table 8-10 provides an overview of the two overcurrent protections in the inrush period.

Table 8-10. Overview of Capacitive Charging Mode in Inrush Period

Capacitive Charging Mode (CAP_CHRG_CHx)	Overcurrent Type	Range	Duration set by	Value set by
00	Immediate shutdown (I_{OCP})	10A to 55A	INRUSH_DURATION_CHx [2:0]	INRUSH_LIMIT_CHx [3:0]
01	Not supported			
10	Current limit regulation (I_{CL_REG})	1.6A to 12A	INRUSH_DURATION_CHx [2:0]	INRUSH_LIMIT_CHx [3:0]
11	Not supported			

The INRUSH_DURATION_CHx bits set the duration of the inrush period. It can be set from 0ms to 100ms. If the INRUSH_DURATION_CHx = 0, the inrush period duration will be set to 0ms and and the inrush period will not be entered when the channel is initially enabled. If a retry were to occur due to an overcurrent or thermal shutdown fault in the inrush period, the timer for exiting the inrush period will reset after each retry.

No Capacitive Charging - CAP_CHRG_CHx [1:0] = 00

The no capacitive charging setting, enables the device to have a different immediate shutdown overcurrent protection (I_{OCP}) value in the inrush period compared to steady state operation to allow for different inrush events at startup such as bulb current inrush or motor stall current.

If CAP_CHRG_CHx [1:0] = 00, the immediate shutdown overcurrent protection (I_{OCP}) value in the inrush period is set by the INRUSH_LIMIT_CHx [3:0] bits and the duration is set by the INRUSH_DURATION_CHx [2:0] bits. Once the inrush period duration timer expires the immediate shutdown overcurrent protection (I_{OCP}) value will be set by the ILIMIT_SET_CHx [3:0] bits in steady state operation.

An example of this is shown in Figure 8-21.

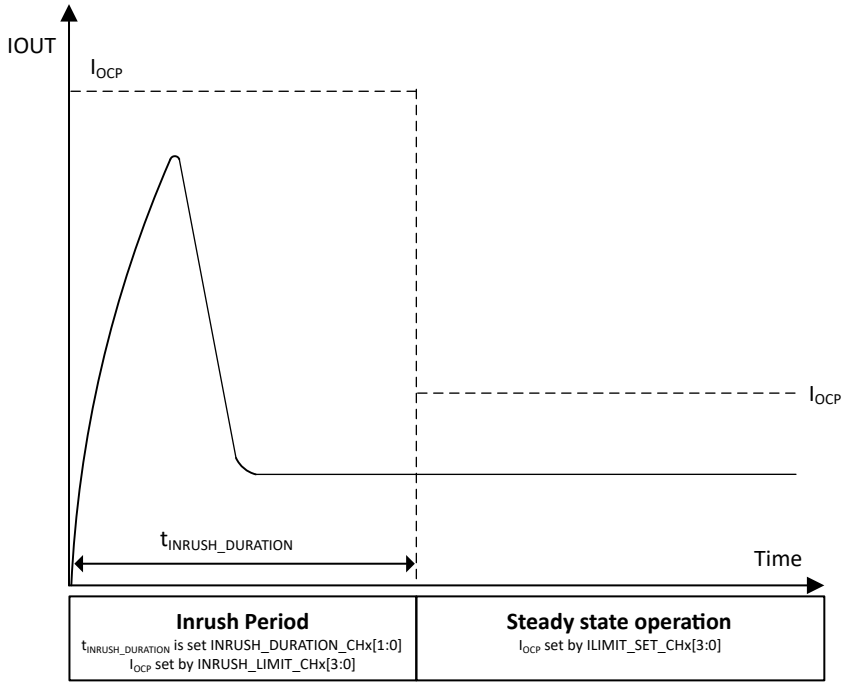


Figure 8-21. No Capacitive Charging (CAP_CHRG_CHx [1:0] = 00) - Bulb Driving Example

Current Limit Regulation Capacitive Charging Mode - CAP_CHRG_CHx [1:0] = 10

The device offers a current limit regulation capacitive charging mode to charge up large downstream capacitive loads such as bulk input capacitors on ECUs. If CAP_CHRG_CHx [1:0] = 10, the current limit regulation mode will clamp the output current when the channel is initially enabled at a value set by the INRUSH_LIMIT_CHx [3:0]. The device will limit the current continuously until the capacitive load has finished charging, the inrush period expires, or a thermal shutdown has occurred. The range of settings which can be programmed through the INRUSH_LIMIT_CHx [3:0] are from 1.6A to 12A and are specified in the electrical characteristic table as I_{CL_REG}. If the VOUT voltage is greater than VBB - 2V and the inrush period timer has not expired, the device is able to slowly exit the current limit regulation without a large spike. An example of the current limit regulation capacitive charging mode and the slow exit before the inrush period timer expiration is shown in Figure 8-22.

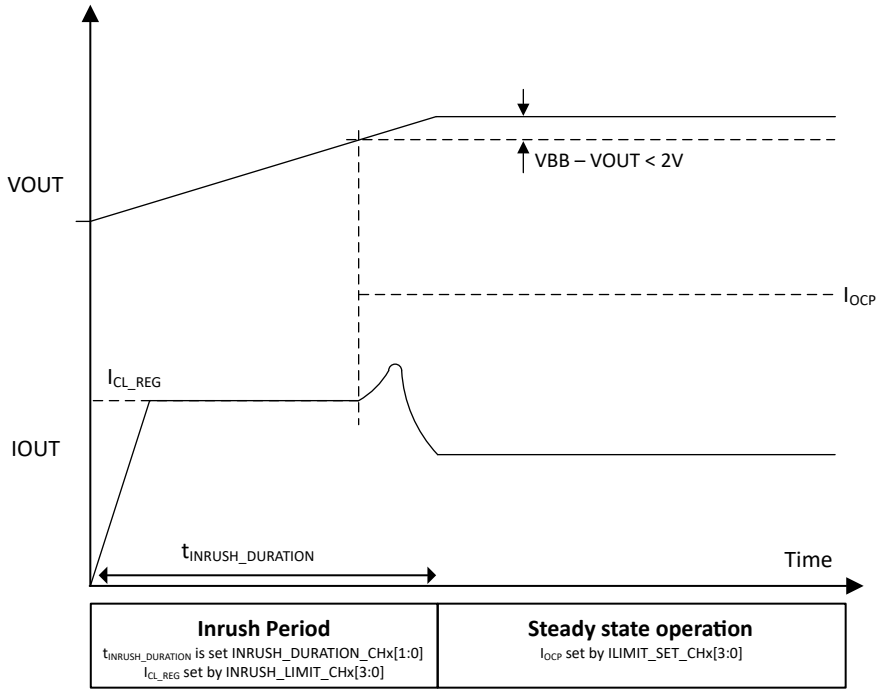


Figure 8-22. Current Limit Regulation Capacitive Charging (CAP_CHRG_CHx [1:0] = 10) - ECU Input Bulk Capacitance Driving Example

8.4.1.1.2 Overcurrent Protection - Steady State Operation

After the device has completed the optional inrush period (if enabled) the device will enter the steady operation. In this operation, the overcurrent protection is provided by the immediate shutdown overcurrent protection (I_{OCP}) and I2T protection (if enabled). The I_{OCP} is an overcurrent protection function that immediately turns off the channel if the output current exceeds I_{OCP} threshold that is set by the ILIMIT_SET_CHx [3:0] bits. The I_{OCP} function can not be disabled and is always active in the steady state operation while the device is enabled. The I2T protection provides a programmable fuse protection that is based on a defined time-current curve. The intent of the I2T protection is to match the behavior of a melting fuse. The time-current curve of the I2T protection can be set through the NOM_CUR_CHx [2:0] bits and I2T_TRIP_CHx [3:0] bits. The ISWCL_CHx [1:0] and I_{OCP} also help to define the time-current curve for the I2T protection. The I_{OCP} and I2T protection (if enabled) are active in the ACTIVE state and the LIMP_HOME state if the channel is in the steady state operation after the inrush period.

The next sections describes the I2T protection and the I_{OCP} protection.

8.4.1.1.3 Programmable Fuse Protection

The device includes a programmable fuse protection for each channel, that is based on a defined time-current curve and is commonly referred to as I2t protection in melting fuse data sheets. The intent is to match the switch turnoff behavior of a melting fuse. The NOM_CUR_CHx [2:0] bits and I2T_TRIP_CHx [3:0] bits set the

time-current curve but the device also uses a fixed delay shutdown (I_{SWCL}) and immediate shutdown protection (I_{OCP}) to create the full I2T protection for the device. The I2T protection of the TPS2HCS08-Q1 consists of four regions:

1. Nominal current
2. Fuse shutdown
3. Fixed delay shutdown
4. Immediate shutdown protection (I_{OCP})

The nominal current region (1) defines the region where the device can supply current indefinitely without turning off. This is roughly equivalent to the fuse current rating of a melting fuse. This region is set by the NOM_CUR_CHx [2:0] bits and if the output current is less than the NOM_CUR_CHx setting then the device can supply current indefinitely as previously stated and it will not start the I2T accumulation. If the output current is greater than or equal to the NOM_CUR_CHx setting then the device will enter the I2T accumulation loop and will start to accumulate until the I2T_TRIP_CHx [3:0] threshold is met. If the output current falls back below the NOM_CUR_CHx before the I2T_TRIP_CHx value is reached then the device will stop the I2T accumulation but will still keep track of the accumulated energy as long as power is provided to the device.

Above the nominal current region, is the fuse shutdown region (2) which is set by the I2T_TRIP_CHx [3:0] bits. This region defines the curvature of time-current curve and the region where the I2T accumulation of the device is active. Based on the output current level and the NOM_CUR_CHx setting the device will trip at different time intervals based on the I2T_TRIP value that is set. The time-current curve of the device is defined by Equation 1.

$$\mathrm{I2T\_TRIP} = \left({I_{OUT}}^2 - \mathrm{NOM\_CUR\_CHx}^2 \right) \times t \quad (1)$$

If the accumulation does not exceed the I2T_TRIP value and the current falls below NOM_CUR_CH then equation 1 is used to decrement the accumulated energy based on the ISNS value until the accumulated energy reaches zero. While the device continues to decrement down to zero, the I2T_MOD bit will remain 1 until accumulated energy returns back to zero and then the I2T_MOD bit will be set back to zero. If any conversions were disabled due to a channel entering the I2T loop then they will be re-enabled when I2T_MOD = 0.

Above the fuse shutdown region, is the fixed delay shutdown region (3) where the device provides a fixed delayed shutdown that is set by the ISWCL_CHx [1:0] and SWCL_DLY_TMR_CHx [1:0] bits. The ISWCL_CHx [1:0] sets the output current value and the SWCL_DLY_TMR_CHx sets the time. If the output current exceeds the ISWCL_CHx level continously for SWCL_DLY_TMR_CHx then the channel will immediately turn off.

If a shutdown occurs either due to the I2T_TRIP_CHx value being exceeded or due to the ISWCL_CHx function, the device will remain off for a period set by the TCLDN_CHx [1:0]. If the TCLDN_CHx [1:0] = 00 then the device will remain off and will not retry. To retry in this setting, the TCLDN_CHx [1:0] bits need to be changed to another setting. Once the setting has been changed, the device will retry after the defined cool down time of the new setting. Note, when the channel enters the I2T shutdown state the accumulator value will be reset to 0 so the retry time should be adjusted to make sure enough time has elasped for the wire harness to cool down. Also note, when the channel enters the I2T shutdown state, the values for NOM_CUR_CHx, I2T_TRIP_CHx, and ISWCL_CHx can not be changed.

Above the fixed delay shutdown region, is the immediate shutdown overcurrent protection (I_{OCP}) region (4). This region is set by the ILIMIT_SET_CHx [3:0] bits. If the output current exceeds the I_{OCP} level then the device will turn off immediately. The retry or latched off behavior for the I_{OCP} is set by the LATCH_CHx bit and discussed in the next section.

These operational regions for the I2T protection are show in Figure 8-23.

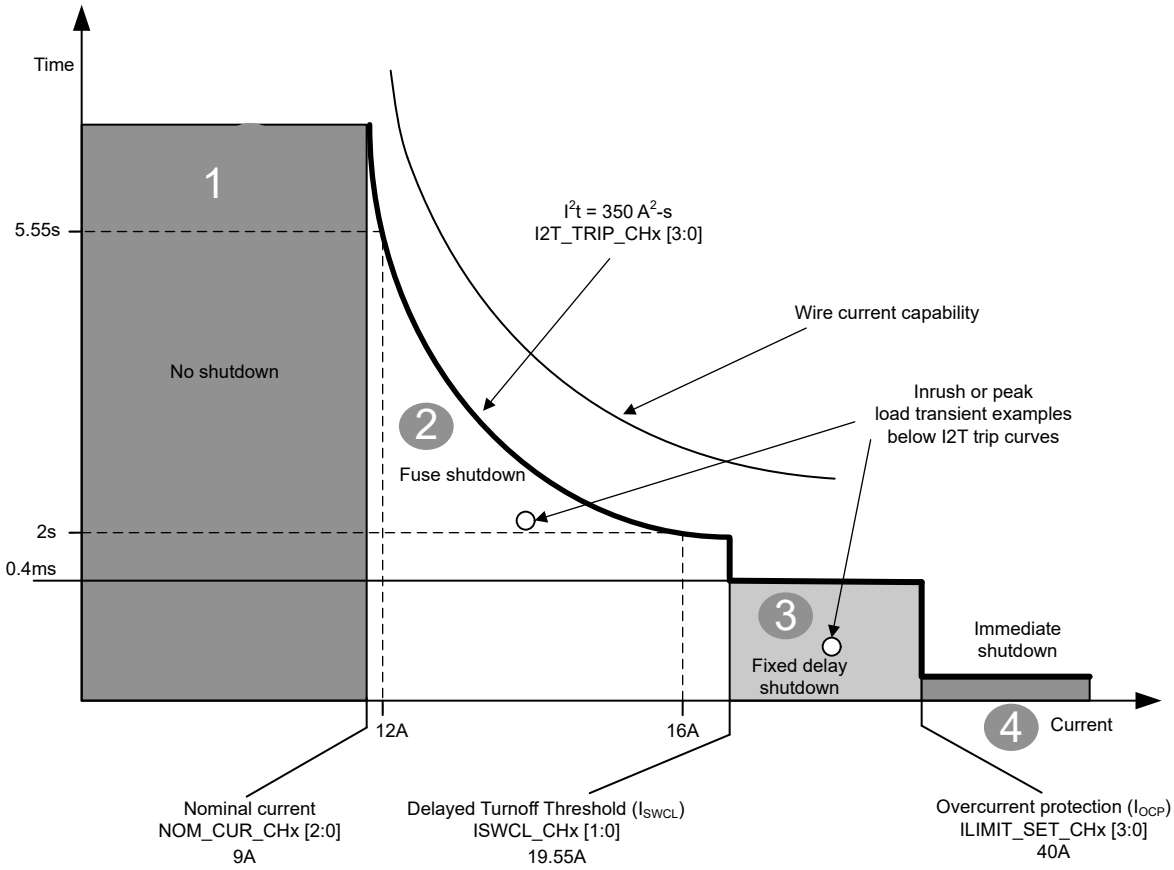


Figure 8-23. Operational Region of Fuse Based Shutdown

The values for the NOM_CUR_CHx, I2T_TRIP_CHx, and ISWCL_CHx in the register map are based on an R_{SNS} value of 700Ω. The device offers the flexibility for these values to be scaled based on different R_{SNS} values. The equations for scaling the NOM_CUR_CHx, I2T_TRIP_CHx, and the ISWCL_CHx are defined below.

$$NOM\_CUR_{ADJ,\,TYP} = \frac{NOM\_CUR_{700} \times 700}{R_{SNS,\,ADJ,\,TYP}} \quad (2)$$

$$I_{SWCL,\,ADJ,\,TYP} = \frac{I_{SWCL,\,700} \times 700}{R_{SNS,\,ADJ,\,TYP}} \quad (3)$$

$$I2T_{ADJ\,.\,TYP} = I2T_{700} \times \left(\frac{700}{R_{SNS,\,ADJ,\,TYP}}\right)^2 \quad (4)$$

where,

$$NOM\_CUR_{700} = \text{NOM\_CUR\_CHx value in the datasheet based on } R_{SNS} \text{ of } 700\Omega \quad (5)$$

$$I_{SWCL,\,700} = I_{SWCL} \text{ value in the datasheet based on } R_{SNS} \text{ of } 700\Omega \quad (6)$$

$$I2T_{700} = \text{I2T trip value in the datasheet based on } R_{SNS} \text{ of } 700\Omega \quad (7)$$

8.4.1.1.4 Immediate Shutdown Overcurrent Protection (I_{OCP})

In steady state operation, the device offers immediate shutdown overcurrent protection (I_{OCP}) which is an overcurrent protection function that immediately turns off the channel if the output current exceeds the I_{OCP} threshold that is set by the ILIMIT_SET_CHx [3:0] bits. The ILIMIT_SET_CHx [3:0] bits enable the I_{OCP} function to be set on a per channel basis. The I_{OCP} function can not be disabled and is always active in the steady state operation while the device is enabled.

If the I_{OCP} level is exceeded, the channel will turn off immediately and the channel will either retry or latch-off based on the setting of the LATCH_CHx bit. If LATCH_CHx = 0, the device will retry after t_{RETRY}. If After the retry time expires, the device will start up into the inrush period if configured. If LATCH_CHx = 1 and the I_{OCP} level is exceeded, the device will latch-off and will not retry until the CHx_ON bit (version A) is toggled or the DIx pin (version B) is toggled or the LATCH_CHx bit is toggled. For more details on how the retry and latch off works for different device settings, see the retry and latch-off behavior section below.

8.4.1.1.5 Auto Retry and Latch-off Behavior

When a thermal shutdown or an immediate shutdown overcurrent protection fault occurs, the channel with the fault will either auto-retry or latch off based on the LATCH_CHx bit setting in the CHx_CONFIG registers. Depending on the CAP_CHRG_CHx settings and the I_{OCP} level, the auto retry response will behave differently.

Auto Retry Behavior - No Capacitive Charging Mode (CAP_CHRG_CHx = 00)

If CAP_CHRG_CHx = 00 and LATCH_CHx = 0 and a short circuit event occurs, after the channel turns off and t_{RETRY} expires the device will retry in the inrush period with the I_{OCP} level set through the INRUSH_LIMIT_CHx [3:0] bits. The INRUSH_DURATION_CHx [2:0] still sets the duration of the inrush period. If the I_{OCP} level is greater than the $I_{OCP\_RETRY\_FLBK}$ and the number of retries is greater than n_{RETRY} then the device will foldback to the $I_{OCP\_RETRY\_FLBK}$ level and will continue to retry at this level until the short is removed or the channel is toggled. Figure 8-24 and Figure 8-25 showcases these hot short cases that occur in steady state operation with I_{OCP} below $I_{OCP\_RETRY\_FLBK}$ and I_{OCP} above $I_{OCP\_RETRY\_FLBK}$, respectively. Starting into a short in the inrush period results in the same retry behavior as a hot short in steady state except the first initial overcurrent shutdown level will be determined by the INRUSH_LIMIT_CHx [3:0].

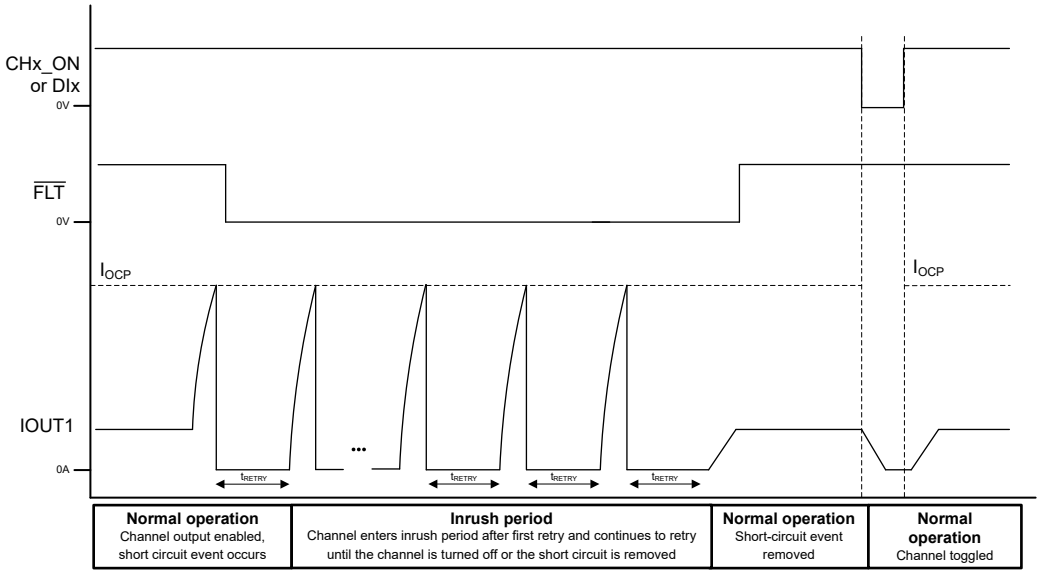


Figure 8-24. Hot Short during Steady State Operation with CAP_CHRG_CHx = 00, Auto-retry (LATCH_CHx = 0), and $I_{OCP} < I_{OCP\_RETRY\_FLBK}$

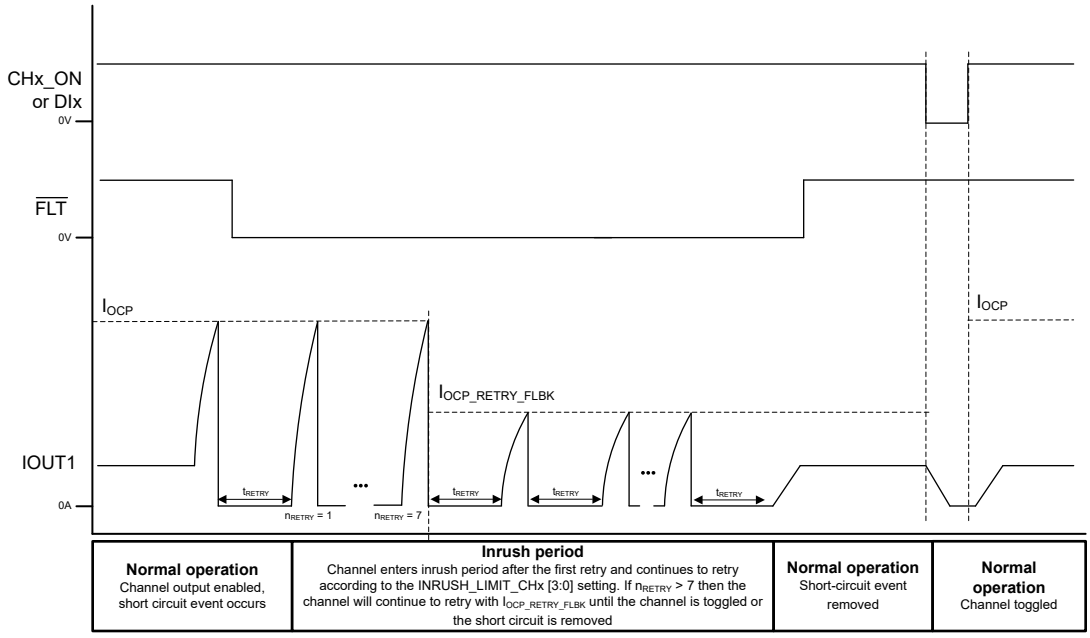


Figure 8-25. Hot Short during Steady State Operation with CAP_CHRG_CHx = 00, Auto-retry (LATCH_CHx = 0), and I_{OCP} > $I_{OCP\_RETRY\_FLBK}$

Latch-off Behavior - No Capacitive Charging Mode (CAP_CHRG_CHx = 00)

If LATCH_CHx = 1 and CAP_CHRG_CHx = 00 and the I_{OCP} level is exceeded, the device will latch-off and will not retry until the CHx_ON bit (version A) is toggled or the DIx pin (version B) is toggled or the LATCH_CHx bit is toggled. Upon resetting the latch either through an output toggle or through the LATCH_CHx bit toggle, the channel will start up into the inrush period if configured. Figure 8-26 below shows the latch behavior if a hot short circuit occurs during steady state operation with LATCH_CHx = 1. Figure 8-27 shows the latch behavior if the channel starts into a short circuit event in the inrush period.

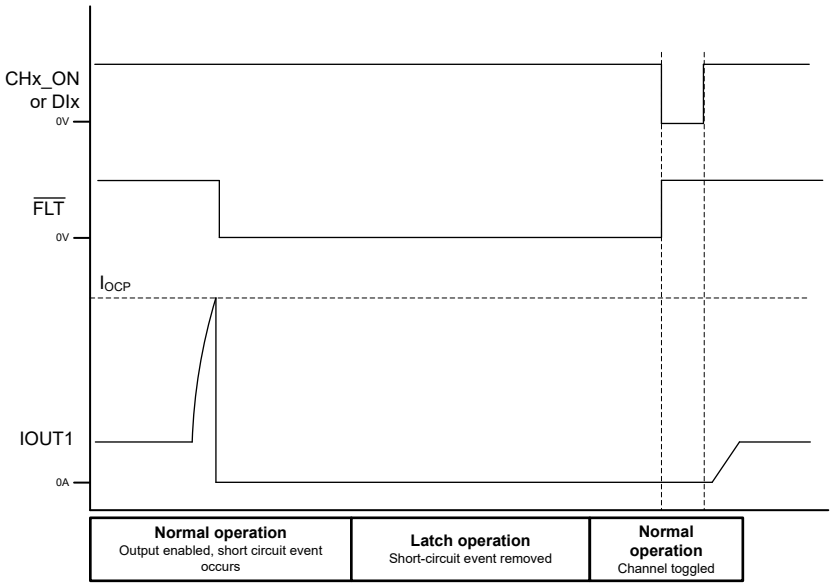


Figure 8-26. Hot Short during Steady State Operation with CAP_CHRG_CHx = 00, Latch-off (LATCH_CHx = 1)

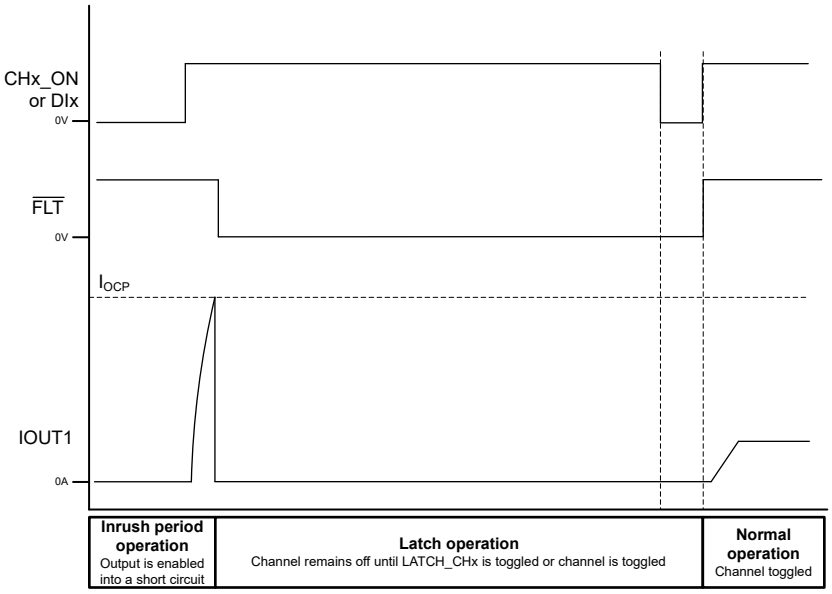


Figure 8-27. Start into a Short Circuit Event with CAP_CHRG_CHx = 00, Latch-off (LATCH_CHx = 1)

Auto Retry Behavior - Current Limit Regulation Charging Mode (CAP_CHRG_CHx = 10)

If a short circuit event occurs in steady state operation with CAP_CHRG_CHx = 10 and LATCH_CHx = 0, after the channel turns off and t_{RETRY} expires the device will retry into the inrush period with the current limit regulation (I_{CL_REG}) set through the INRUSH_LIMIT_CHx [3:0] bits. Figure 8-28 shows a hot short event that occurs in steady state operation with CAP_CHRG_CHx = 10 and LATCH_CHx = 0. Figure 8-29 shows the auto-retry behavior if the channel starts into a short circuit event in the inrush period.

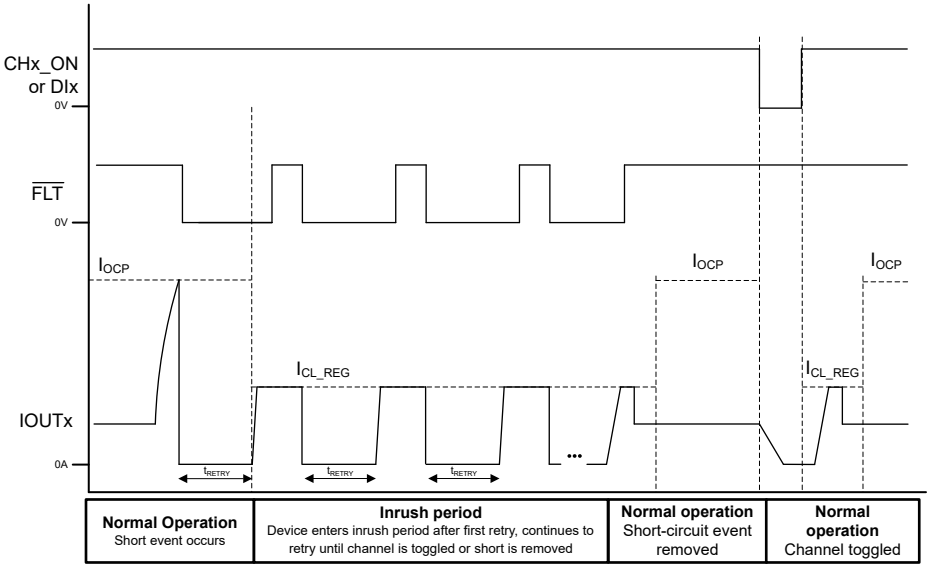


Figure 8-28. Hot Short during Steady State Operation with CAP_CHRG_CHx = 10 and Auto-retry (LATCH_CHx = 0)

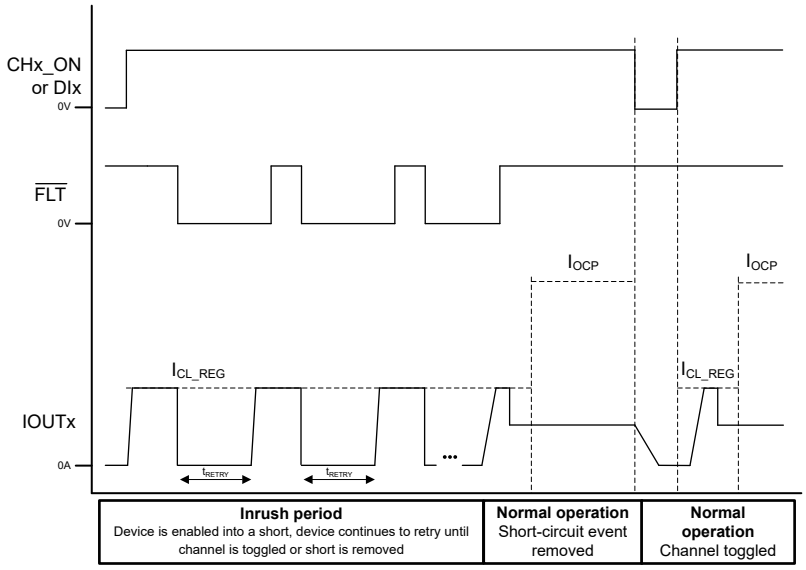


Figure 8-29. Start into a Short Circuit Event with CAP_CHRG_CHx = 10 and Auto-rety (LATCH_CHx = 0)

Latch-off Behavior - Current Limit Regulation Capactive Charging Mode (CAP_CHRG_CHx = 10)

If LATCH_CHx = 1 and CAP_CHRG_CHx = 10 and the I_{OCP} level is exceeded, the device will latch-off and will not retry until the CHx_ON bit (version A) is toggled or the DIx pin (version B) is toggled or the LATCH_CHx bit is toggled. Upon resetting the latch either through an output toggle or through the LATCH_CHx bit toggle, the channel will start up into the inrush period if configured. Figure 8-30 below shows the latch behavior if a hot short circuit occurs during steady state operation with LATCH_CHx = 1. Figure 8-31 shows the latch behavior if the channel starts into a short circuit event in the inrush period.

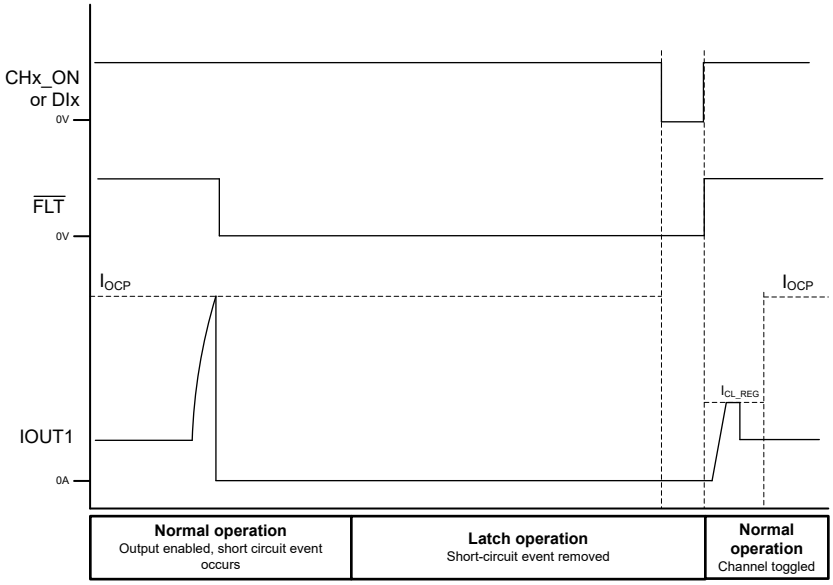


Figure 8-30. Hot Short during Steady State Operation with CAP_CHRG_CHx = 10, Latch-off (LATCH_CHx = 1)

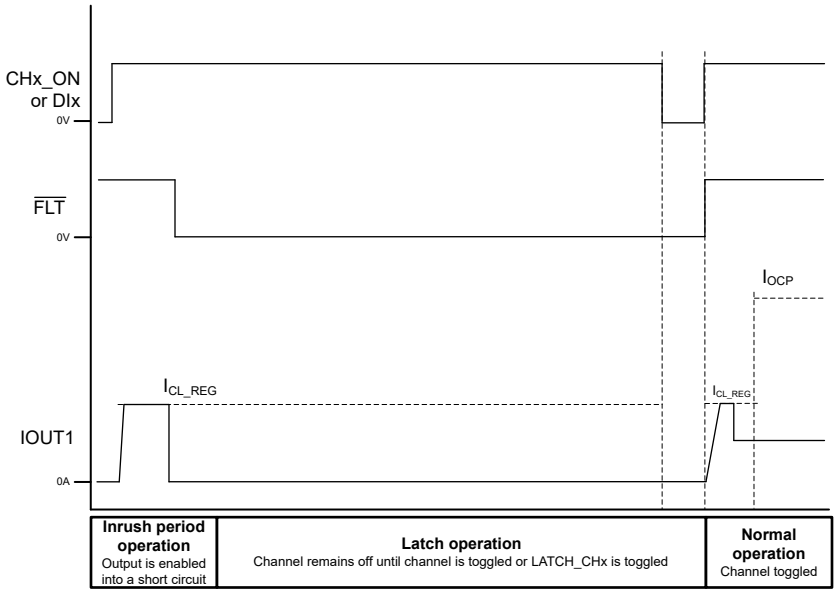


Figure 8-31. Start into a Short Circuit Event with CAP_CHRG_CHx = 10, Latch-off (LATCH_CHx = 1)

8.4.1.2 Thermal Shutdown

The device includes a temperature sensor on each power FET and within the controller portion of the device to monitor the temperature of each FET ($T_{J,FET}$) and the temperature of the controller ($T_{J,CONTROLLER}$). There are two cases that the device will consider to be a thermal shutdown fault:

- **Relative Thermal Shutdown (T_{REL}):** $T_{J,FET} - T_{J,CONTROLLER} > T_{REL}$
- **Absolute Thermal Shutdown (T_{ABS}):** $T_{J,FET} > T_{ABS}$

If either the above faults occur, the relevant switch will be turned off. Each channel is turned off based on the measurement of the temperature sensor for that channel. As result, if the thermal fault is detected on only one channel, the other channel continues operation.

Relative Thermal Shutdown (T_{REL})

A relative thermal shutdown event can occur when there is a large peak power event such as a short-to-ground event where the FET temperature ($T_{J,FET}$) quickly rises relative to the controller temperature ($T_{J,CONTROLLER}$). Once the relative temperature ($T_{J,FET} - T_{J,CONTROLLER}$) exceeds T_{REL} the relevant channel will be turned off.

Absolute Thermal Shutdown (T_{ABS})

An absolute thermal shutdown occurs when the FET temperature ($T_{J,FET}$) rises above T_{ABS}. This can occur when a channel is subjected to long durations of overcurrent such as a permanent short use case. Once the FET temperature ($T_{J,FET}$) exceeds T_{ABS} the relevant channel will be turned off.

8.4.1.3 Reverse Battery

In the reverse battery condition, the switch will automatically be enabled regardless of the state of the output (set by the SW_STATE register) to prevent excess power dissipation inside the MOSFET body diode. In many applications (for example, resistive loads), the full load current may be present during reverse battery. In order to activate the automatic switch on feature, the DI pin (version A) or DI1 (version B) must have a path to ground from either from the MCU or it needs to be tied to ground through R_{PROT} if unused.

There are two options for handling reverse battery in the system. The first option is to place a blocking device (FET or diode) in series with the battery supply, blocking all current paths. The second option is to place a blocking diode in parallel with a resistor on the GND node of the high-side switch. This method will protect the controller portion of the switch (path 2) by limiting the current through the internal circuits. Additionally in the

second option, the automatic switch on feature of the device will allow the device to be put into low R_{ON} state to allow current to flow through the switch efficiently and through the load (path 3). The diode used for the second option may be shared amongst multiple high-side switches.

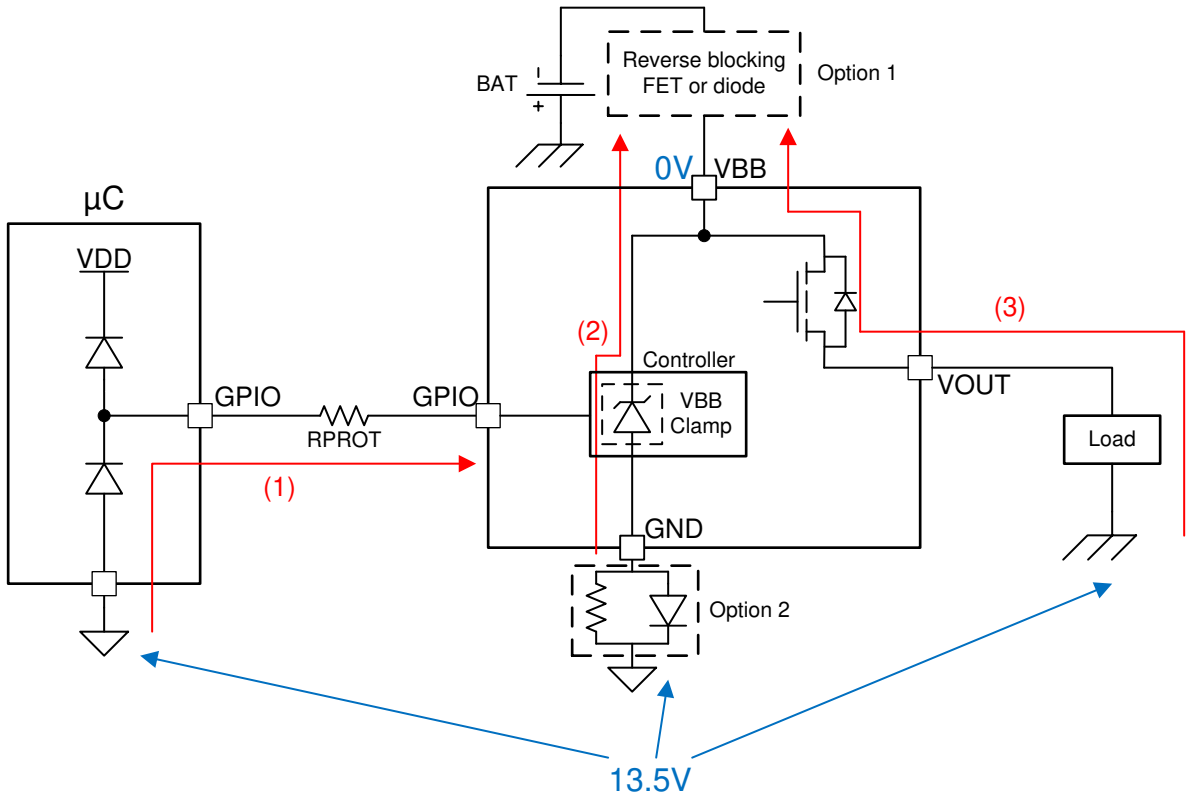


Figure 8-32. Current Path During Reverse Battery

For more information on reverse battery protection, refer to TI's *Reverse Battery Protection for High Side Switches* application note.

8.4.2 Diagnostic Mechanisms

8.4.2.1 Integrated ADC

The TPS2HCS08-Q1 provides an integrated successive approximation 10-bit ADC which can convert different analog signals to digital signals which can be read out through SPI. The ADC can convert the following analog signals:

- CH1 and CH2 current sense (ISNS1/2)
- CH1 and CH2 MOSFET temperature sense (TSNS1/2)
- VBB voltage sense (VBB_SNS)
- CH1 and CH2 VOUT voltage sense (VSNS1/2)
- CH1 and CH2 MOSFET drain-to-source voltage (VDS) sense (VDS_SNS1/2)

Figure 8-35 provides a functional block diagram of the integrated ADC along with the analog signal inputs to the ADC.

Conversion of any of the analog signals can either be disabled globally through the ADC_CONFIG register or on a per channel basis through CHx_CONFIG registers with the exception of temperature sensing. The temperature sensing can not be disabled on a per channel basis and can only be disabled globally through the ADC_TSNS_DIS bit.

To help reduce the quiescent current, the device only enables the current sense circuitry when the ADC is converting either of the ISNSx signals and disables it during all other signal conversions. The device also

provides a configurable delay which can also help to further reduce the quiescent current of the device by reducing the sampling rate of the ADC. The configurable delay is set by the ADC_ISNS_SAMPLE_CONFIG [1:0] bits in the ADC_CONFIG register.

If I2T protection is enabled (I2T_EN_CHx = 1) and either channel is not in I2T mode (I2T_MOD_CHx = 0), then the device will convert each of the analog signals in a round robin sequence with the configurable delay. Figure 8-33 below shows the ADC scheduling if no channel is in I2T mode (I2T_MOD_CHx = 0) and all analog signal conversions are enabled. If I2T protection is disabled then the round robin sequence below also applies.

	ISNS1	ISNS2	TSNS1	TSNS2	VBB_SNS	VSNS1	VSNS2	VDS_SNS1	VDS_SNS2	Configurable delay ADC_ISNS_SAMPLE_CONFIG [1:0]
ISNS_EN	1		0							
I2T_MOD_CHx	0									

Figure 8-33. ADC Sequence with I2T_MOD_CHx = 0

If I2T protection is enabled (I2T_EN_CHx = 1) and one or both of the channels are in I2T mode (I2T_MOD_CHx = 1), then the device disables all conversions except for the ISNSx conversions which are used for the internal I2T protection. The device also disables the configurable delay function as well. Figure 8-34 below shows the ADC scheduling if one or both of the channels are in I2T mode (I2T_MOD_CHx = 1).

	ISNS1	ISNS2	ISNS1	ISNS2	...	ISNS1	ISNS2
ISNS_EN	1						
I2T_MOD_CHx	1						

Figure 8-34. ADC Sequence with I2T_MOD_CHx = 1

The reference voltage for the ADC is fixed internally and is specified in the electrical characteristics table through the $V_{ADCREFHI}$ parameter. The ADC's ground reference is connected internally to the GND of the device. For accurate current sense results, the ground connection of the R_{SNS} resistor should be connected to the GND pin of the device. The conversion equation for each of the analog signals can be found in their respective sections below.

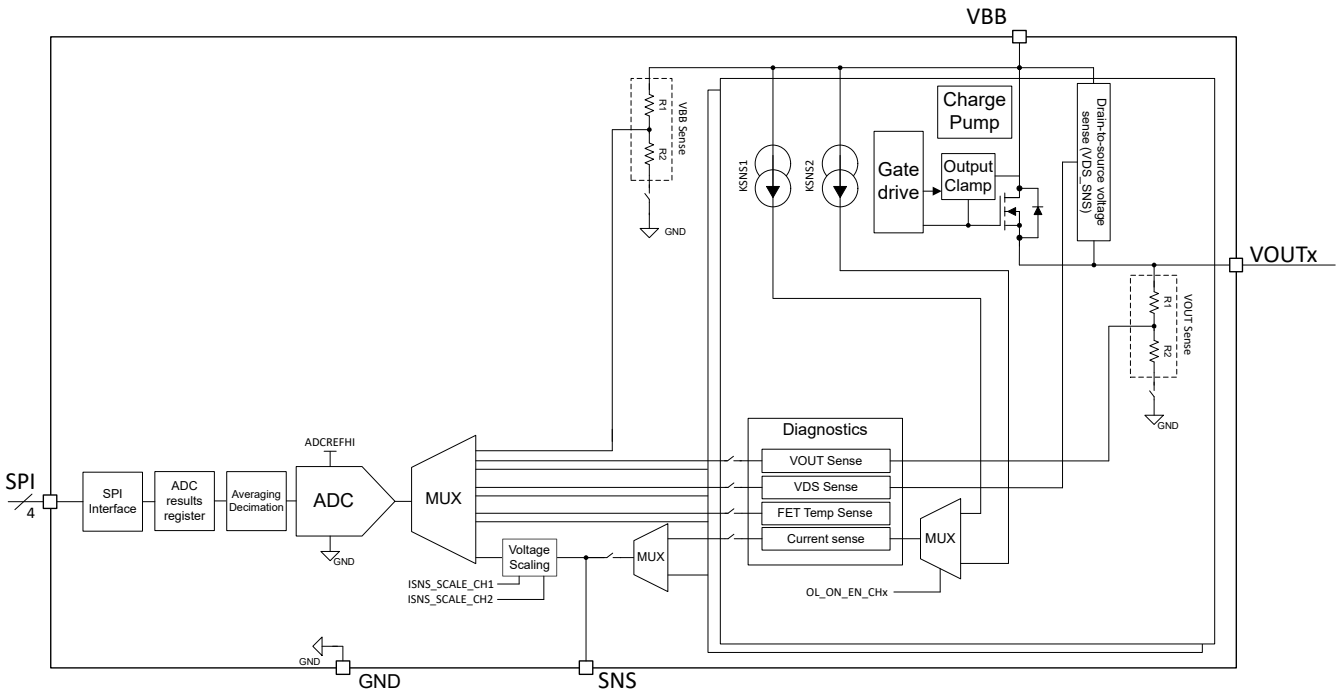


Figure 8-35. Integrated ADC Functional Block Diagram

8.4.2.2 Digital Current Sense Output

The integrated current sense circuit of the device provide a sense current (I_{SNS}) proportional to the load current (I_{OUTx}) of each channel through the SNS pin to an external sense resister (R_{SNS}) to create a voltage. The current sense of each channel is multiplexed internally and is outputted on the SNS pin by the ADC scheduler. The voltage created by the I_{SNS} and R_{SNS} is then sampled by the internal 10-bit ADC where the result of the ADC conversion is stored in ADC_RESULT_CHx_I for each channel. The ISNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register was last read.

To ensure an accurate sensing measurement by the internal ADC, the sensing resistor should be connected to the IC GND.

The device offers two current sense ratios (K_{SNS1}) and (K_{SNS2}) for each channel which can be set through the OL_ON_EN_CHx bit in the CHx_CONFIG registers. The higher K_{SNS1} ratio (OL_ON_EN_CHx = 0 mode) allows for the channel to accurately measure high output current levels where the lower K_{SNS2} ratio (OL_ON_EN_CHx = 1 mode) enables the channel to accurately measure low output current levels. The K_{SNS1} utilizes the full mosfet where K_{SNS2} utilizes a small mosfet with ON resistance, R_{ON_OL}, to provide the lower current sense ratio. To use the K_{SNS2} ratio, the output current level must be below $I_{ENTRY\_OL\_ON}$ before the OL_ON_EN_CHx bit is set to 1. If the current is not below $I_{ENTRY\_OL\_ON}$, the K_{SNS2} operation will not be entered and the K_{SNS1} operation will still be active. If the channel is operating with K_{SNS2} and the output current increases above $I_{EXIT\_OL\_ON}$, the device will automatically transition out of K_{SNS2} to K_{SNS1} where the OL_ON_EN_CHx bit will be reset to 0 and the full mosfet is active. If the current falls below $I_{ENTRY\_OL\_ON}$ again then the OL_ON_EN_CHx bit needs to be set back to 1 to transition to K_{SNS2} operation again. The system can manually exit K_{SNS2} operation by writing OL_ON_EN_CHx = 0. When measuring the output current through the integrated ADC in K_{SNS2} operation, the system should continue to monitor the OL_ON_EN_CHx = 1 bit to ensure the device is still in K_{SNS2} operation when the output current measurement is read.

The device also offers a voltage scaling option to amplify the current sense voltage at the ADC input. At low output current levels this helps to allow the current sense voltage to be at higher levels of the integrated ADC. The voltage scaling is set through the ISNS_SCALE_CHx bit. Table 8-11 below provides the different settings for the ISNS_SCALE_CHx. ISNS_SCALE_CHx = 1 operation is recommended only in OL_ON_EN_CHx = 1 mode.

It is recommended to only use OL_ON_EN_CHx = 1 mode and/or ISNS_SCALE_CHx = 1 with I2T disabled (I2T_EN = 0). If OL_ON_EN_CHx = 1 and/or ISNS_SCALE_CHx = 1 is used with I2T enabled (I2T_EN = 1) this could cause the channel to turn off at unintended lower I2T thresholds.

Table 8-11. ISNS_SCALE_CHx Settings

ISNS_SCALE_CHx	Value
0	x1
1	x8

The ISNS_SCALE_EFF_CHx bit in the ADC_RESULT_CHx_I register, will provide an indication if the channel is operating with 1x or 8x voltage scaling so the system knows which voltage scaling factor to apply when converting the current sense measurement.

The ADC conversion equation for current sense for different OL_ON_EN_CHx settings are below:

with OL_ON_EN_CHx = 0,

$$\mathrm{IOUT}\left(\mathrm{A}\right) = \left(\frac{\mathrm{KSNS1} \times \mathrm{V_{ADCREFHI}}}{1023 \times \mathrm{R_{SNS}}}\right) \times \mathrm{ADC\_RESULT\_CHx\_I} \quad (8)$$

with OL_ON_EN_CHx = 1,

$$\mathrm{IOUT}\left(\mathrm{A}\right) = \left(\frac{\mathrm{KSNS2} \times \mathrm{V_{ADCREFHI}}}{1023 \times \mathrm{R_{SNS}} \times \mathrm{ISNS\_SCALE\_CHx}}\right) \times \mathrm{ADC\_RESULT\_CHx\_I} \quad (9)$$

The current sense function is enabled for each channel by default. The current sense function can be enabled or disabled globally through the ADC_ISNS_DIS bit in the ADC_CONFIG register. When the global ADC_ISNS_DIS bit is 0 the device will enable or disable the current sense function on each channel according to the ISNS_DIS_CHx bit in the respective CHx_CONFIG registers.

If I2T protection is used, the current sense function has to be enabled before the I2T protection can be used. The current sense function is only available when the channel is enabled and in the steady state operation. The current sense function is not available in the inrush period.

8.4.2.3 Output Voltage Measurement

The TPS2HCS08-Q1 provides an output voltage measurement per channel through the integrated 10-bit ADC.

The output voltage measurement function is disabled by default. To enable the output voltage sense function it needs to be globally enabled in the ADC_CONFIG register through the ADC_VSNS_DIS bit. If the global bit is enabled then the device will enable the output voltage measurement on each channel according to the VSNS_DIS_CHx bit in the respective CHx_CONFIG register.

The conversion equation for the output voltage measurement is detailed in Equation 10. The ADC measurement result will be available in the ADC_RESULT_CHx_V register. The VSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register was last read. If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the output voltage measurement, if enabled, will be disabled for all the channels and the VSNS_RDY_CHx bit will be 0. Once the channel(s) exit the I2T loop (I2T_MOD_CHx = 0), then the output voltage measurement will be automatically re-enabled if previously enabled before the I2T event.

$$\mathrm{VOUT}\left(\mathrm{V}\right) = \left(\frac{17.89 \times \mathrm{V_{ADCREFHI}}}{1023 \times 1.667}\right) \times \mathrm{ADC\_RESULT\_CHx\_V} \quad (10)$$

The output voltage measurement is referenced to the device ground so if there is a ground network used for reverse battery then there can be an offset in the voltage measurement.

8.4.2.4 MOSFET Temperature Measurement

The TPS2HCS08-Q1 provides a temperature measurement for each of the power MOSFETs through the 10-bit ADC.

The FET temperature sense function is disabled by default. To enable the FET temperature sense function for each channel it needs to be globally enabled in the ADC_CONFIG register through the ADC_TSNS_DIS bit.

The conversion equation for the FET temperature measurement is detailed in Equation 11. The ADC measurement result will be available in the ADC_RESULT_CHx_T register. The TSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register was last read. If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the FET temperature measurement, if enabled, will be disabled for all the channels and the TSNS_RDY_CHx bit will be 0. Once the channel(s) exit the I2T loop (I2T_MOD_CHx = 0), then the FET temperature measurement will be automatically re-enabled if previously enabled before the I2T event.

$$T_{J,FET}\left(°C\right) = 381.367 - \left(0.75157 \times \text{ADC\_RESULT\_CHx\_T}\right) \quad (11)$$

8.4.2.5 Drain-to-Source Voltage (V_{DS}) Measurement

The TPS2HCS08-Q1 provides a drain-to-source voltage (V_{DS}) measurement per channel through the integrated 10-bit ADC.

The V_{DS} voltage measurement function is disabled by default. To enable the V_{DS} voltage sense function it needs to be globally enabled in the ADC_CONFIG register through the ADC_VDS_DIS bit. If the global bit is enabled, then the device will enable the V_{DS} voltage measurement on each channel according to the VDS_SNS_DIS_CHx bit in the respective CHx_CONFIG register.

The conversion equation for the V_{DS} voltage measurement is detailed in Equation 12. The V_{DS} conversion equation is only valid for V_{DS} voltages up to 1.5V. The ADC measurement result will be available in the ADC_RESULT_CHx_VDS register. The VDSSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register was last read. If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the V_{DS} voltage measurement, if enabled, will be disabled for all the channels and the VDSSNS_RDY_CHx bit will be 0. Once the channel(s) exit the I2T loop (I2T_MOD_CHx = 0), then the V_{DS} voltage measurement will be automatically re-enabled if previously enabled before the I2T event.

$$\text{VDS}\left(\text{V}\right) = \frac{\text{ADC\_RESULT\_CHx\_VDS} - 24}{288.267} \quad (12)$$

8.4.2.6 VBB Voltage Measurement

The TPS2HCS08-Q1 provides a VBB voltage measurement through the 10-bit ADC.

The VBB voltage measurement is disabled by default. The VBB voltage sense function can be enabled through the ADC_VBB_DIS bit in the ADC_CONFIG register.

The conversion equation for the VBB voltage measurement is detailed in Equation 13. The ADC measurement result will be available in the ADC_RESULT_VBB register. The VBB_RDY bit is set to 1 if a new ADC conversion result exists since the register was last read. If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the VBB voltage measurement, if enabled, will be disabled and the VBB_RDY bit will be 0. Once the channel(s) exit the I2T loop (I2T_MOD_CHx = 0), then the VBB voltage measurement will be automatically re-enabled if previously enabled before the I2T event.

$$\text{VBB}\left(\text{V}\right) = \left(\frac{18.18 \times V_{ADCREFHI}}{1023 \times 1.667}\right) \times \text{ADC\_RESULT\_VBB} \quad (13)$$

The VBB voltage measurement is referenced to the device ground so if there is a ground network used for reverse battery then there can be an offset in the voltage measurement.

8.4.2.7 VOUT Short-to-Battery and Open-Load

The TPS2HCS08-Q1 is capable of detecting short-to-battery and open-load events regardless of whether the channel output is turned on or off, however the two conditions use different methods.

8.4.2.7.1 Measurement With Channel Output (FET) Enabled

When the channel output is enabled and the FET is on, the VOUT short-to-battery and open-load conditions can be measured with the current sense feature. In both cases, the load current is measured using the current sense circuit and the ADC (available in the ADC_RESULT_CHx_I registers). The current sense accuracy can be increased at low current levels by changing the current sense ratio from a nominal value of 5000 to a nominal lower value of 1400. This is accomplished by setting the OL_ON_EN_CHx bit to 1 in the individual CHx_CONFIG register. However, the load current must be below $I_{ENTRY\_OL\_ON}$ for this bit to take effect. In addition, the voltage input to the ADC can be scaled by 8x by setting the ISNS_SCALE_CHx bit in the same CHx_CONFIG register. This enables the ADC to measure the low load current with higher accuracy.

It is recommended to only use OL_ON_EN_CHx = 1 mode and/or ISNS_SCALE_CHx = 1 with I2T disabled (I2T_EN = 0). If OL_ON_EN_CHx = 1 and/or ISNS_SCALE_CHx = 1 is used with I2T enabled (I2T_EN = 1) this could cause the channel to turn off at unintended lower I2T thresholds.

8.4.2.7.2 Detection With Channel Output Disabled

The device is able to detect an open load or a short-to-battery event when the channel output is disabled (FET is off). These will be referred to below as off state open load detection and off state short-to-battery detection. Whhen the channel output is disabled, the device is able to distinguish between an open load event and a short-to-battery event through a defined sequence that will be discussed below. A block diagram for the off-state open load and off-state short-to-battery detection is shown in Figure 8-36.

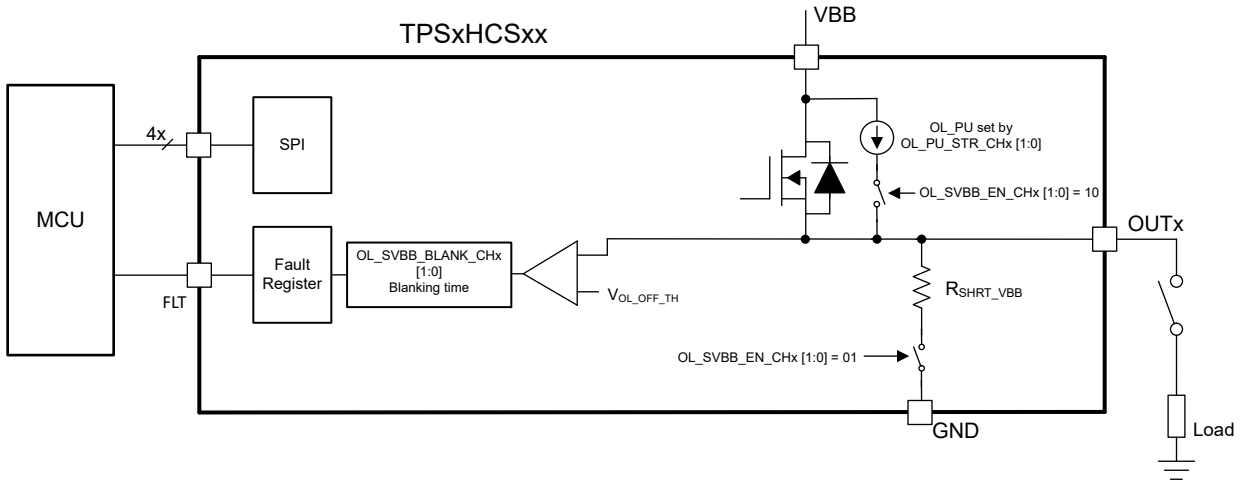


Figure 8-36. Open Load and Short-to-battery Detection

Note

This figure assumes that the device ground and the load ground are at the same potential. In a real system, there may be a ground shift voltage of the order of 1 V.

Off-state Open Load Detection

The device integrates a pull-up current source, OL_PU, for each channel which can be used to pull-up the output to determine if there is an open load or short-to-battery event. The pull-up current source is enabled when OL_SVBB_EN_CHx [1:0] = 10 along with an internal comparator which is used to detect when the output voltage rises above the $V_{OL\_OFF\_TH}$. The strength of the internal pull-up can be programmed through the OL_PU_STR_CHx bits for each channel in the CHx_CONFIG registers. The device also offers a programmable blanking timer per channel to allow the output to settle before determining if there is an open load or a

short-to-battery event. The blanking time can be programmed through the OL_SVBB_BLANK_CHx bits in the CHx_CONFIG registers.

When OL_SVBB_EN_CHx [1:0] = 10, the device is only able to report if there is either an open load or a short-to-battery event, it is not able to distinguish between the two with this setting alone. If either an open load or a short-to-battery fault has occurred, then the OL_OFF_CHx bit in the FLT_STAT_CHx register for the corresponding channel will be set to 1. The OL_OFF_CHx bit is a read clear bit which will clear when the FLT_STAT_CHx register is read and the fault no longer exists, either from the removal of the fault or from the open load circuitry being disabled. To distinguish between an open load and short-to-battery faults, a certain procedure needs to be followed. This is detailed below in the Distinguishing Between Open Load and Short-to-battery Faults section.

If OL_SVBB_EN_CHx [1:0] = 10 and the output is enabled, the device will disable the pull-up current source and internal comparator before turning on the output. If OL_SVBB_EN_CHx [1:0] = 10 and the channel is enabled and then is disabled, the device will automatically enable the pull-up source and internal comparator.

Off-state Short-to-battery Detection

The device also integrates a pull-down resistor for each channel which can be used to help distinguish between an open load and a short-to-battery fault when the channel is disabled. The pull-down resistor is enabled when OL_SVBB_EN_CHx [1:0] = 01 along with an internal comparator which is used to detect when the output voltage rises above the $V_{OL\_OFF\_TH}$. The pull-down resistor is specified by the R_{SHRT_VBB} parameter in the electrical characteristics. The device offers a programmable blanking timer per channel to allow the output to settle before determining if there is a short-to-battery event. The blanking time can be programmed through the OL_SVBB_BLANK_CHx bits in the CHx_CONFIG registers.

When OL_SVBB_EN_CHx [1:0] = 01, the device is only able to report if there is a short-to-battery event. The device is not able to detect if an open load fault has occurred. If a short-to-battery fault has occurred, then the SHRT_VBB_CHx bit in the FLT_STAT_CHx register for the corresponding channel will be set to 1. The SHRT_VBB_CHx bit is a read clear bit which will clear when the FLT_STAT_CHx register is read and the fault no longer exists, either from the removal of the fault or from the short-to-battery detection circuitry being disabled. To distinguish between an open load and short-to-battery faults, a certain procedure needs to be followed. This is detailed below in the Distinguishing Between Open Load and Short-to-battery Faults section.

If OL_SVBB_EN_CHx [1:0] = 01 and the output is enabled, the device will disable the pull-down resistor and internal comparator before turning on the output. If OL_SVBB_EN_CHx [1:0] = 01 and the channel is enabled and then is disabled the device will automatically enable the pull-down resistor and the internal comparator.

Distinguishing Between Open Load and Short-to-battery Faults

The TPS2HCS08-Q1 device is able to distinguish between an open load and a short-to-battery fault through a defined procedure. Figure 8-37 highlights the procedure that is recommended to distinguish between an open load and a short-to-battery fault.

When reading the OL_OFF_CHx bits and SHRT_VBB_CHx bits to determine if there is an open load fault or a short-to-battery fault, three read command should be used to determine which fault has occurred. The first read command is to set which register to read, the second read command is to see if a fault has occurred and a third read command is to see if the fault has persisted. After these three successive reads, then the determination of the fault can be done.

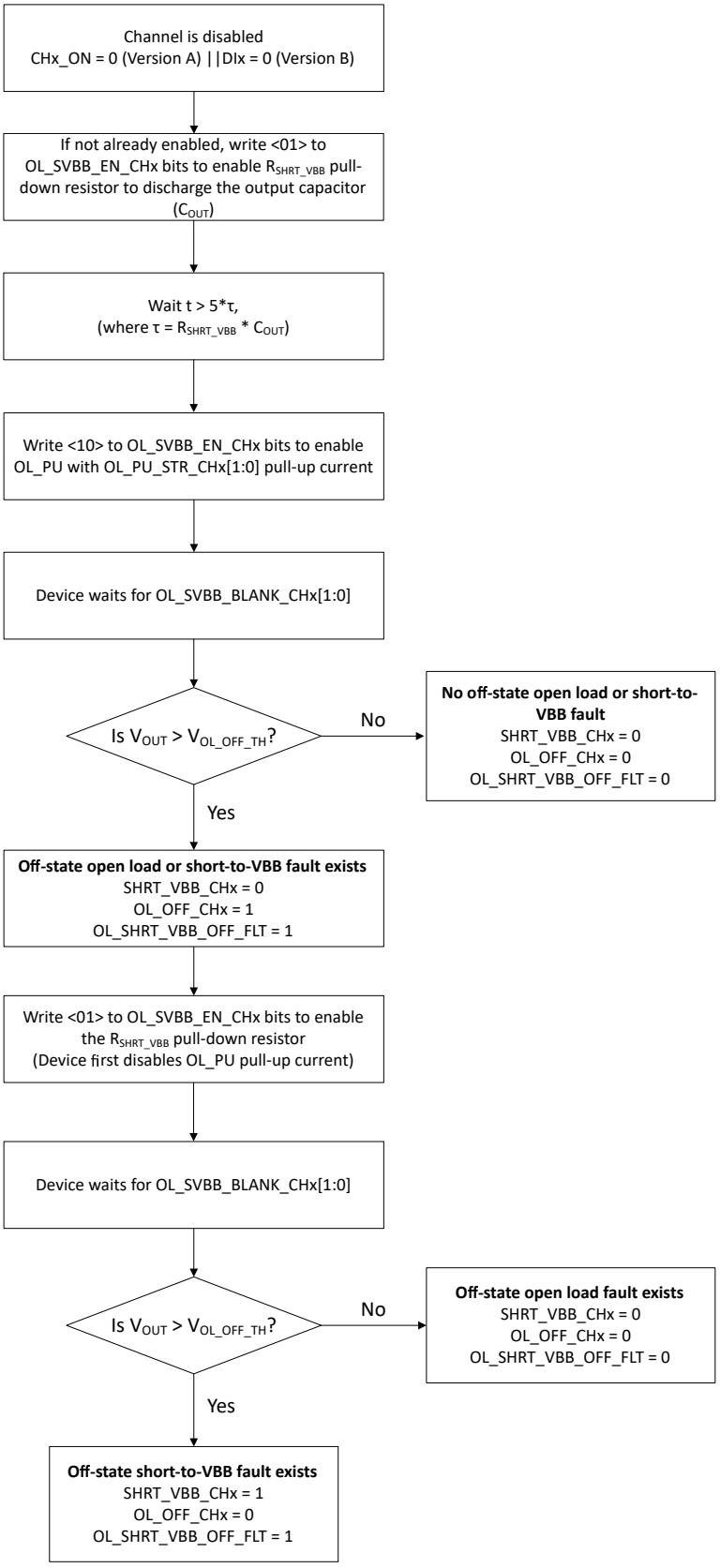


Figure 8-37. Logic Flow Chart to Distinguish Between Open Load and Short-to-battery Faults

8.5 Parallel Mode Operation

When the PARALLEL_12 bit is set to 1, the device supports a parallel mode where the outputs of the device can be connected together externally to operate the device as a single channel device. This reduces the RON approximately by half and increases the continuous output current by approximately 2x.

When setting the PARALLEL_12 bit, both channels must be off in order for it to take effect. To confirm if the PARALLEL_12 bit has taken effect, the DEV_CONFIG register can be read to verify the PARALLEL_12 bit is set to 1.

The following sections cover the different configurations and behaviors specific to the parallel mode of the device. If any function or feature is not described in the followings sections, the device will operate the same as in single channel operation for that function or feature.

Channel Control in Parallel Mode

In parallel mode, channel control in the ACTIVE state is set only through the CH1_ON bit in the SW_STATE register for TPS2HCS08A-Q1. For TPS2HCS08B-Q1, channel control in ACTIVE state is set only through the DI1 pin. For LIMP_HOME state, channel control is set only through CH1_LH_IN bits only in the DEV_CONFIG register.

Fault Reporting - Parallel Mode

In parallel mode, if a fault on either or both channels, the fault flags for both channels will assert for the respective fault.

Diagnostics - Parallel Mode

In parallel mode, the ADC diagnostics (ISNS, VSNS, VBBSNS, VDS_SNS, and TSNS) are available for both channels. These diagnostics can be enabled or disabled on a per channel basis through the respective CHx_CONFIG registers.

To enter KSNS2 operation (or also known as OL_ON_EN_CHx = 1 mode), the output current must be below 2x $I_{ENTRY\_OL\_ON}$ before the OL_ON_EN_CH1 bit is set to 1. If the current is not below 2x $I_{ENTRY\_OL\_ON}$, the K_{SNS2} operation will not be entered and the K_{SNS1} operation will still be active. If the channel is operating with K_{SNS2} and the output current increases above 2x $I_{EXIT\_OL\_ON}$, the device will automatically transition out of K_{SNS2} to K_{SNS1} where the OL_ON_EN_CH1 bit will be reset to 0 and the full MOSFET is active. If the current falls below 2x $I_{ENTRY\_OL\_ON}$ again then the OL_ON_EN_CH1 bit needs to be set back to 1 to transition to K_{SNS2} operation again. The system can manually exit K_{SNS2} operation by writing OL_ON_EN_CH1 = 0. When measuring the output current through the integrated ADC in K_{SNS2} operation, the system should continue to monitor the OL_ON_EN_CH1 = 1 bit to ensure the device is still in K_{SNS2} operation when the output current measurement is read.

Off state open load detection and off state short to battery detection settings are set by the CH1_CONFIG register only. The device will only enable the circuitry on channel 1 to detect off state open load and the off state short to battery.

Inrush Period - Overcurrent Protection in Parallel Mode

In parallel mode, the overcurrent protection in the optional inrush period is set by the ILIM_CONFIG_CH1 register only. Either of the two capacitive charging modes, no capacitive charging or current regulation, can be used in parallel mode and is set by the CAP_CHRG_CH1 bits. The duration for the inrush period is set by INRUSH_DURATION_CH1. The value for the capacitive charging is set by the INRUSH_LIMIT_CH1 bits and the effective value for the entire device for parallel operation will be approximately double the INRUSH_LIMIT_CH1 setting.

The overcurrent protection and thermal shutdown protection in both channels will be enabled for the two capacitive charging modes. For the no capacitive charging mode, if the output current through either channel

goes above the INRUSH_LIMIT_CH1 setting then both channels will be turned off. For both capacitive charging modes, if either channel has a thermal shutdown fault, both channels will be turned off.

See Table 8-12below for more details on how the device can be configured for the overcurrent protection in the optional inrush period.

Table 8-12. Inrush Period Overcurrent Protection Configuration Methods for Parallel Mode

Capacitive Charging Mode (CAP_CHRG_CH1)	Duration Set By	Value Set By	Effective Typical Value When PARALLEL_12 = 1
00	INRUSH_DURATION_CH1 [2:0]	INRUSH_LIMIT_CH1 [3:0]	2x INRUSH_LIMIT_CH1 [3:0]
10	INRUSH_DURATION_CH1 [2:0]	INRUSH_LIMIT_CH1 [3:0]	2x INRUSH_LIMIT_CH1 [3:0]

Steady State - Overcurrent Protection in Parallel Mode

In parallel mode, the immediate shutdown overcurrent protection (I_{OCP}) in the steady state operation is set by the ILIMIT_SET_CH1 bits in the ILIM_CONFIG_CH1 register only. The effective value for the entire device for parallel operation will be approximately double the ILIMIT_SET_CH1 setting.

The overcurrent protection and thermal shutdown protection in both channels will be enabled in steady state operation. If the output current through either channel goes above the ILIMIT_SET_CH1 setting then both channels will be turned off.

Note

The max ILIMIT_SET_CH1 value that is supported for parallel mode is 40A. If CAP_CHRG_CH1 = 00, the max INRUSH_LIMIT_CH1 value that is supported for parallel mode is 40A.

Steady State - I2T Protection in Parallel Mode

In parallel mode, the I2T protection is set by the I2T_CONFIG_CH1 register only. The value for INOM for the I2T is set by the NOM_CUR_CH1 bits and the effective value for the entire device for parallel operation will be approximately double the NOM_CUR_CH1 setting. The value for the I2T threshold is set by the I2T_TRIP_CH1 bits and the effective value for the entire device for the parallel operation is approximately quadruple the I2T_TRIP_CH1 setting. The value for the ISWCL is set by the ISWCL_CH1 bits and the effective value for the entire device for the parallel operation is approximately double the ISWCL_CH1 setting.

Enabling of I2T in parallel mode is done only through the I2T_EN_CH1 bit in the ILIM_CONFIG_CH1 register.

For I2T accumulation, only the current sense for channel 1 is used. If the I2T_TRIP_CH1 value is exceeded for channel 1 then both channels will be turned off.

MANUAL_LPM - Parallel Mode

In parallel mode, the MANUAL_LPM is entered through the MANUAL_LPM_ENTRY bit. The device operates the same as in single channel operation as described in the MANUAL_LPM section with the following exceptions:

- For TPS2HCS08A-Q1, the device only monitors the AUTO_LPM_EXIT_CH1 setting when coming out of MANUAL_LPM to determine if the channel needs to be turned on when in active state if not already enabled. AUTO_LPM_EXIT_CH2 setting will be ignored.
- The device monitors the output current for both channels to determine when the device will exit the MANUAL_LPM state. If either of the channels output current exceeds the $I_{EXIT\_LPM\_MAN}$ thresholds, the device will exit the MANUAL_LPM state. For the correct operation, MAN_LPM_EXIT_CURR_CH1 and MAN_LPM_EXIT_CURR_CH2 settings need to be set to the same value. The effective value for the entire device for the parallel operation is approximately double the MAN_LPM_EXIT_CURR_CHx settings.
- For TPS2HCS08B-Q1, the device only monitors changes in the DI1 pin to exit MANUAL_LPM.

AUTO_LPM - Parallel Mode

In parallel mode, the AUTO_LPM is entered AUTO_LPM_ENTRY bit is set to 1. The device operates the same as in single channel operation as described in the AUTO_LPM section with the following exceptions:

- For TPS2HCS08A-Q1, the device will only monitor AUTO_LPM_EXIT_CH1 to exit AUTO_LPM and turn on the channels if they are not already enabled. AUTO_LPM_EXIT_CH2 setting will be ignored.
- The device monitors the output current for both channels to determine when the device should exit the AUTO_LPM state. If either of the channels output current exceeds the $I_{EXIT\_LPM\_AUTO}$ threshold, the device will exit the AUTO_LPM state. The effective value for the entire device for the parallel operation is approximately double the $I_{EXIT\_LPM\_AUTO}$ value.
- For TPS2HCS08B-Q1, the device will only monitor changes in the DI1 pin to exit AUTO_LPM.

PWM - Parallel Mode

In parallel mode, the PWM settings will be set by the PWM_CH1 register only. The PWM_SHIFT_DIS bit will be ignored as both channels will turn on at the same time. Enabling of PWM for parallel mode is done through the PWM_EN_CH1 bit.

RON - Parallel Mode

The RON for each channel varies slightly from each other and can cause a small load mismatch. This is specified in the electrical characteristics through the ΔR_{ON} parameter.

Layout Recommendations - Parallel Mode

In parallel mode, the routing of the output channels is important to avoid any additional load mismatch. The output traces should be symmetrical to avoid any extra resistance which can cause uneven current draw through the output channels.

8.6 TPS2HCS08 Registers

Table 8-13 lists the memory-mapped registers for the TPS2HCS08 registers. All register offset addresses not listed in Table 8-13 should be considered as reserved locations and the register contents should not be modified.

Table 8-13. TPS2HCS08 Registers

Offset	Acronym	Register Name	Section
0h	DEV_ID	Read the device ID from NVM	Go
1h	CRC_CONFIG	CRC configuration register	Go
2h	SLEEP	Set to go to SLEEP state from ACTIVE or CONFIG state	Go
3h	LPM	Low power mode (LPM) settings register	Go
4h	GLOBAL_FAULT_TYPE	Channel Fault Status and Global Fault Type	Go
5h	FAULT_MASK	Mask the reporting of faults on the fault pin	Go
7h	SW_STATE	ON/OFF control for VOUT1 and VOUT2	Go
9h	DEV_CONFIG	Global device configuration register	Go
Ah	ADC_CONFIG	ADC configuration register	Go
Bh	ADC_RESULT_VBB	ADC conversion result - VBB	Go
Dh	FLT_STAT_CH1	Channel 1 fault status	Go
Eh	PWM_CH1	PWM configuration register for channel 1	Go
Fh	ILIM_CONFIG_CH1	Protection configuration register for channel 1	Go
10h	CH1_CONFIG	Configuration register for channel 1	Go
11h	ADC_RESULT_CH1_I	ADC conversion result - load current sense for channel 1	Go
12h	ADC_RESULT_CH1_T	ADC conversion result - TJ.FET temperature sense for channel 1	Go
13h	ADC_RESULT_CH1_V	ADC conversion result - VOUT sense for channel 1	Go
14h	ADC_RESULT_CH1_VDS	ADC conversion result - VDS sense for channel 1	Go
15h	I2T_CONFIG_CH1	I2T configuration register for channel 1	Go
16h	FLT_STAT_CH2	Fault status for channel 2	Go
17h	PWM_CH2	PWM configuration register for channel 2	Go
18h	ILIM_CONFIG_CH2	Protection configuration register for channel 2	Go
19h	CH2_CONFIG	Configuration register for channel 2	Go
1Ah	ADC_RESULT_CH2_I	ADC conversion result - load current sense for channel 2	Go
1Bh	ADC_RESULT_CH2_T	ADC conversion result - TJ.FET temperature sense for channel 2	Go
1Ch	ADC_RESULT_CH2_V	ADC conversion result - VOUT sense for channel 2	Go
1Dh	ADC_RESULT_CH2_VDS	ADC conversion result - VDS sense for channel 2	Go
1Eh	I2T_CONFIG_CH2	I2T configuration register for channel 2	Go

Complex bit access types are encoded to fit into small table cells. Table 8-14 shows the codes that are used for access types in this section.

Table 8-14. TPS2HCS08 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear

Table 8-14. TPS2HCS08 Access Type Codes (continued)

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 DEV_ID Register (Offset = 0h) [Reset = XXXXh]

DEV_ID is shown in Table 8-15.

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Table 8-15. DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEVICE_ID	R	X	X = Part Number FFF0h = TPS2HCS08A FFF1h = TPS2HCS08B

8.6.2 CRC_CONFIG Register (Offset = 1h) [Reset = FFFEh]

CRC_CONFIG is shown in Table 8-16.

Return to the Summary Table.

Table 8-16. CRC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	7FFFh	Reserved
0	CRC_EN	R/W	0h	Enables CRC check of SPI command frame. 0h = No CRC check of SPI command frame 1h = CRC check of SPI command frame enabled

8.6.3 SLEEP Register (Offset = 2h) [Reset = FFFEh]

SLEEP is shown in Table 8-17.

Return to the Summary Table.

Table 8-17. SLEEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	7FFFh	Reserved
0	SLEEP	R/W	0h	Set this bit to 1 to send the device to SLEEP state 0h = No change 1h = Sends the device to SLEEP state

8.6.4 LPM Register (Offset = 3h) [Reset = FF80h]

LPM is shown in Table 8-18.

Return to the Summary Table.

Table 8-18. LPM Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	1FFh	Reserved
6-5	MAN_LPM_EXIT_CURR_CH2	R/W	0h	Set the threshold to exit from MANUAL_LPM mode due to load current increase - CH2 0h = 530mA 1h = 700mA 2h = 165mA 3h = 350mA
4-3	MAN_LPM_EXIT_CURR_CH1	R/W	0h	Set the threshold to exit from MANUAL_LPM mode due to load current increase - CH1 0h = 530mA 1h = 700mA 2h = 165mA 3h = 350mA
2	AUTO_LPM_EXIT_CH2	R/W	0h	This bit forces the device out of AUTO_LPM mode to ACTIVE state and enables CH2 if not already enabled. To re-enable the device to enter AUTO_LPM mode this bit must be set back to 0. 0h = Re-enables device to enter AUTO_LPM mode if all conditions are met 1h = Forces an exit from AUTO_LPM state to ACTIVE state. Enable CH2 if not already enabled
1	AUTO_LPM_EXIT_CH1	R/W	0h	This bit forces the device out of AUTO_LPM mode to ACTIVE state and enables CH1 if not already enabled. To re-enable the device to enter AUTO_LPM mode this bit must be set back to 0. 0h = Re-enables device to enter AUTO_LPM mode if all conditions are met 1h = Forces an exit from AUTO_LPM state to ACTIVE state. Enable CH1 if not already enabled
0	MANUAL_LPM_ENTRY	R/W	0h	Setting this bit to 1 puts the device into MANUAL_LPM. Note: Both channels must be off or the current on any enabled channel(s) must be below MAN_LPM_EXIT_CURR_CHx to enter MANUAL_LPM mode. If the device is in MANUAL_LPM state and a 0 is written to the MANUAL_LPM_ENTRY bit the device will look at the contents of AUTO_LPM_EXIT_CHx bits and if any of the bits are set to 1 the device will exit MANUAL_LPM mode and will turn on the channel(s) if not already enabled. If the device exits MANUAL_LPM state to ACTIVE state due to a load current increase > MAN_LPM_EXIT_CURR_CHx, the MANUAL_LPM_ENTRY bit needs to be set 0 and then back to 1 to re-enter MANUAL_LPM state 0h = Sends the device to ACTIVE mode if device is in MANUAL_LPM 1h = Sends the device to MANUAL_LPM mode if all conditions are met

8.6.5 GLOBAL_FAULT_TYPE Register (Offset = 4h) [Reset = 0147h]

GLOBAL_FAULT_TYPE is shown in Table 8-19.

Return to the Summary Table.

Table 8-19. GLOBAL_FAULT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	CH2_FLT	R	0h	Fault status of channel 2. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CH2 register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No fault(s) have occurred on CH2 1h = Fault(s) have occurred on CH2
12	CH1_FLT	R	0h	Fault status of channel 1. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CH1 register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No fault(s) have occurred on CH1 1h = Fault(s) have occurred on CH1
11	LPM_STATUS	R	0h	This bit indicates if the device is in either MANUAL_LPM mode or AUTO_LPM mode and is cleared when the device is not in any LPM mode. 0h = Device is not in the AUTO_LPM or MANUAL_LPM state 1h = Device has entered either AUTO_LPM or MANUAL_LPM state
10	CHAN_OCP_I2T_TSD	R	0h	This bit indicates if there is an overcurrent protection or I2T protection or thermal shutdown fault in any one of the channels. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No overcurrent protection, I2T protection, or thermal shutdown fault in any of the channels 1h = Overcurrent protection, I2T protection, or thermal shutdown fault(s) in one or both of the channels
9	OL_SHRT_VBB_OFF_FLT	R	0h	This bit indicates if there is a short to VBB supply in the off-state fault in any one of the channels. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition(s) no longer exist 0h = No off-state short to VBB or open load fault in any of the channels 1h = Off-state short to VBB or open load fault(s) in one or both of the channels

Table 8-19. GLOBAL_FAULT_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	GLOBAL_ERR_WRN	R	1h	This bit indicates if there is a global fault reported in FLT_GLOBAL_TYPE[7:0] bits. The faults that are reported through this bit are LIMPHOME_STATE, POR, SPI_ERR, WD_ERR, VDD_UVLO, VBB_UV_WRN, or VBB_UVLO. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the GLOBAL_FAULT_TYPE register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No global fault has occurred 1h = One of the following event(s) have occurred: LIMPHOME_STATE, POR, SPI_ERR, WD_ERR, VDD_UVLO, VBB_UV_WRN, or VBB_UVLO
7	LIMPHOME_STAT	R/W1C	0h	This bit indicates if the device is in LIMP_HOME state as a result of the LHI pin going high. Write 1 to clear and exit LIMP_HOME state. The LHI pin must be LOW when the bit is set to 1 to exit LIMP_HOME state. 0h = Device is not in LIMP_HOME state 1h = Device is in LIMP_HOME state due to LHI pin going high
6	POR	RC	1h	The bit is indicates if a power on reset (POR) has occurred since the last read This bit is cleared on read, so if read again and the bit is 0, this means that no power-on reset has occurred since the read. 0h = No power on reset (POR) has occured since the last register read 1h = A power-on reset has occurred since the last register read.
5	LPM_STATUS_1	RC	0h	This bit indicates if the device is in either MANUAL_LPM or AUTO_LPM modes. This bit is latched and cleared only when read and the device is not in any LPM mode. Note: If the conditons are not met for MANUAL_LPM entry, this bit will be set to 1 and cleared when read. 0h = Device is not in the AUTO_LPM or MANUAL_LPM state 1h = Device has entered either AUTO_LPM or MANUAL_LPM state
4	SPI_ERR	RC	0h	This bit indicates if there is a SPI communication error either from format, clock or CRC. The fault bit is latched and cleared only after read and the error(s) no longer exist. 0h = No SPI communication error(s) fault have occurred 1h = SPI communication error either from format, clock or CRC has occurred
3	WD_ERR	RC	0h	If WD_EN = 1, this bit indicates if there has not been an acceptable SPI command in the watchdog timeout window. The fault bit is latched and cleared only after read and the error no longer exists 0h = No SPI interface watchdog error 1h = SPI watchdog timeout error has occurred
2	VDD_UVLO	RC	1h	This bit indicates if the VDD supply is below VDD_UVLOF at any time. The fault bit is cleared if the GLOBAL_FAULT_TYPE register is read and the UVLO condition is removed 0h = No VDD_UVLO fault has occurred 1h = VDD_UVLO fault has occurred

Table 8-19. GLOBAL_FAULT_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VBB_UV_WRN	RC	1h	This bit indicates if the VBB supply is below the $V_{BB\_UV\_WRN}$ at any time. If VBB is below $V_{BB\_UV\_WRN}$, the diagnostics in the device are turned off The fault bit is cleared if the GLOBAL_FAULT_TYPE register is read and the UV condition no longer exists 0h = No VBB_UV_WRN fault has occurred 1h = VBB_UV_WRN fault has occurred
0	VBB_UVLO	RC	1h	This bit indicates if the VBB supply is below the V_{BB_UVLOF} at any time. The fault bit is cleared if the GLOBAL_FAULT_TYPE register is read and the UVLO condition is removed 0h = No VBB_UVLO fault has occurred 1h = VBB_UVLO fault has occurred

8.6.6 FAULT_MASK Register (Offset = 5h) [Reset = FF80h]

FAULT_MASK is shown in Table 8-20.

Return to the Summary Table.

Table 8-20. FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	1FFh	Reserved
6	RESERVED	R/W	0h	Reserved
5	MASK_SHRT_VBB	R/W	0h	This bit determines if the device should mask the signaling of an off-state short-to-battery fault on the FLT pin 0h = Short to VBB fault is signaled on the FLT pin 1h = Short to VBB fault is not signaled (masked from) on the FLT pin
4	MASK_OL_OFF	R/W	0h	The bit determines if the device should mask the signaling of an off-state open load fault on the FLT pin 0h = Off-state wire-break fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = Off-state wire-break fault is not signaled (masked from) on the FLT pin
3	RESERVED	R	0h	Reserved
2	MASK_SPI_ERR	R/W	0h	The bit determines if the device should mask a SPI error (SPI_ERR) on the FLT pin and in the GLOBAL_FAULT_TYPE register 0h = SPI error is signaled on the FLT pin and in the GLOBAL_FAULT_TYPE register 1h = SPI error is not signaled on the FLT pin or in the GLOBAL_FAULT_TYPE register
1	MASK_WD_ERR	R/W	0h	The bit determines if the device should mask a SPI watchdog error (WD_ERR) on the FLT pin and in the GLOBAL_FAULT_TYPE register 0h = SPI watchdog error is signaled on the FLT pin and in the GLOBAL_FAULT_TYPE register 1h = SPI watchdog error is not signaled on the FLT pin or in the GLOBAL_FAULT_TYPE register
0	MASK_VBB_UVLO	R/W	0h	The bit determines if the device should mask the supply voltage VBB UVLO fault on the FLT pin 0h = VBB_UVLO fault is signaled on the FLT pin 1h = VBB_UVLO fault is not signaled (masked from) on the FLT pin

8.6.7 SW_STATE Register (Offset = 7h) [Reset = FFFCh]

SW_STATE is shown in Table 8-21.

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Table 8-21. SW_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	3FFFh	Reserved
1	CH2_ON	R/W	0h	This bit determines the output state of channel 2 for TPS2HCS08A-Q1 versions. 0h = CH2 Output set to OFF (FET is OFF) 1h = CH2 Output set to ON (FET is ON) Note: This bit has no effect on TPS2HCS08B-Q1. For TPS2HCS08B-Q1, control of channel 2 output is determined only through the DI2 pin.
0	CH1_ON	R/W	0h	This bit determines the output state of channel 1 for TPS2HCS08A-Q1 versions. 0h = CH1 Output set to OFF (FET is OFF) 1h = CH1 Output set to ON (FET is ON) Note: This bit has no effect on TPS2HCS08B-Q1 version. For TPS2HCS08B-Q1, control of channel 1 output is determined only through the DI1 pin

8.6.8 DEV_CONFIG Register (Offset = 9h) [Reset = F800h]

DEV_CONFIG is shown in Table 8-22.

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Table 8-22. DEV_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10-9	CH2_LH_IN	R/W	0h	These bits determine how the channel 2 output should respond in LIMP_HOME state for the TPS2HCS08A-Q1 versions. Note: These bits have no effect on TPS2HCS08B-Q1. There is no LIMP_HOME state in TPS2HCS08B-Q1. 0h = DI pin controls the output when in LIMP_HOME state 1h = Keeps the same output state from CH2_ON bit when entering LIMP_HOME state 2h = Output will be OFF in LIMP_HOME mode 3h = Output will be ON in LIMP_HOME mode
8-7	CH1_LH_IN	R/W	0h	These bits determine how the channel 1 output should respond in LIMP_HOME state for the TPS2HCS08A-Q1 versions. Note: These bits have no effect on TPS2HCS08B-Q1. There is no LIMP_HOME state in TPS2HCS08B-Q1. 0h = DI pin controls the output when in LIMP_HOME state 1h = Keeps the same output state from CH1_ON bit when entering LIMP_HOME state 2h = Output will be OFF in LIMP_HOME mode 3h = Output will be ON in LIMP_HOME mode
6	PWM_SHIFT_DIS	R/W	0h	This bit determines if there should be an offset in the start of the PWM between the channels. 0h = PWM rising edges delayed by 100µs on the first rising edge 1h = PWM delay (offset) is disabled so rising edges are aligned
5	AUTO_LPM_ENTRY	R/W	0h	This bit determines if the device should enter AUTO_LPM mode if all the conditions are met to enter AUTO_LPM mode. 0h = Entry into AUTO_LPM mode is disabled 1h = Entry into AUTO_LPM mode is enabled and the device enters if all the conditions are met to enter
4	PARALLEL_12	R/W	0h	This bit signals to the device that channel 1 (CH1) and channel 2 (CH2) are paralleled in the system. 0h = CH1 and CH2 are not paralleled together 1h = CH1 and CH2 are paralleled together Note: A write to this bit is only valid if CH1_ON and CH2_ON bits in the SW_STATE register are 0.
3	WD_EN	R/W	0h	The bit determines if the SPI watchdog function is enabled. If enabled, the watchdog timeout triggers if there is not a valid SPI command in the watchdog timeout window 0h = Watchdog is disabled 1h = Watchdog function is enabled
2-1	WD_TO	R/W	0h	This bit determines the timeout period for the SPI watchdog function (if enabled). The watchdog timeout triggers if there is not a valid SPI command in the watchdog timeout window. 0h = Watchdog timeout period is 400µs 1h = Watchdog timeout period is 400ms 2h = Watchdog timeout period is 800ms 3h = Watchdog timeout period is 1200ms

Table 8-22. DEV_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FLT_LTCH_DIS	R/W	0h	This bit determines if the fault bits in FAULT_GLOBAL_TYPE [13:8] should latch if a fault occurs. 0h = Fault bits [13:8] in FAULT_GLOBAL_TYPE register latched and cleared only on read of the associated register 1h = Fault bits [13:8] in FAULT_GLOBAL_TYPE register are not latched and are cleared when the fault no longer exists Note: See each fault bit description for more details on how to clear the individual fault bits when FLT_LTCH_DIS = 0. LPM_STATUS[0] is read only.

8.6.9 ADC_CONFIG Register (Offset = Ah) [Reset = FF3Ah]

ADC_CONFIG is shown in Table 8-23.

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Table 8-23. ADC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	FFh	Reserved
7-6	ADC_ISNS_SAMPLE_CONFIG	R/W	0h	These bits determine the sampling and conversion rate for the current sense (ISNS). The slower the sampling and conversion rate the lower the IQ consumption. 0h = Current sense and ADC conversion at max rate 1h = Current sense and ADC conversion at max rate 2h = Current sense and ADC conversion at one half max rate 3h = Current sense and ADC conversion at one quarter max rate
5	ADC_VDS_DIS	R/W	1h	This bit determines if the VDS sense funciton should be disabled for all channels. If disabled, this excludes VDS conversion for all channels in the ADC conversion sequence. Note: The VDS sense function can also be enabled or disabled per channel through the VDS_SNS_DIS_CHx bit in the CHx_CONFIG register. This bit must be set to 0 to enable/disable the function on a channel basis. 0h = VDS_SNS ADC function is enabled 1h = VDS SNS ADC functionality is disabled for all channels, VDS_SNS ADC conversion is excluded in the ADC conversion sequence for all channels
4	ADC_VSNS_DIS	R/W	1h	This bit determines if the VOUT sense (VSNS) funciton should be disabled for all channels. If disabled, this excludes the VOUT conversion for all channels in the ADC conversion sequence. Note: The VSNS function can also be enabled or disabled per channel through the VSNS_DIS_CHx bit in the CHx_CONFIG register. This bit must be set to 0 to enable/disable the function on a channel basis. 0h = VSNS ADC function is enabled 1h = VSNS ADC functionality is disabled for all channels, VSNS ADC conversion is excluded in the ADC conversion sequence for all channels
3	ADC_TSNS_DIS	R/W	1h	This bit determines if the temperature sense function is disabled for all channels. If disabled, this excludes the temperature sense conversion for all channels in the ADC conversion sequence. Note: The temperature sense function can only be enabled or disabled globally 0h = TSNS ADC function is enabled 1h = TSNS ADC functionality is disabled for all channels, TSNS ADC conversion is excluded in the ADC conversion sequence for all channels
2	ADC_ISNS_DIS	R/W	0h	This bit determines if the current sense (ISNS) function is disabled for all channels. If disabled, this excludes the ISNS conversion for all channels in the ADC conversion sequence Note: The ISNS function can also be enabled or disabled per channel through the ISNS_DIS_CHx in the CHx_CONFIG register. This bit must be set to 0 to enable/disable the function on a channel basis. 0h = ISNS ADC function is enabled 1h = ISNS ADC functionality is disabled for all channels, ISNS ADC conversion is excluded in the ADC conversion sequence for all channels
1	ADC_VBB_DIS	R/W	1h	This bit determines if the VBB_SNS function is disabled. If disabled, this excludes supply voltage VBB conversion in the ADC conversion sequence. 0h = VBB_SNS ADC function is enabled, VBB_SNS ADC conversion is included in the ADC conversion sequence 1h = VBB_SNS ADC function is disabled, VBB_SNS ADC conversion is excluded in the ADC conversion sequence

Table 8-23. ADC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADC_DIS	R/W	0h	This bit determines if the ADC function should be disabled. If disabled, no VDS_SNS, VSNS, TSNS, or ISNS is possible. The ADC is enabled by default. 0h = ADC function enabled 1h = All ADC function disabled

8.6.10 ADC_RESULT_VBB Register (Offset = Bh) [Reset = F800h]

ADC_RESULT_VBB is shown in Table 8-24.

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Table 8-24. ADC_RESULT_VBB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VBB_RDY	R	0h	This bit indicates if a new ADC result for VBB voltage conversion is available since the last read 0h = VBB ADC value not updated 1h = New VBB ADC value ready since last read
9-0	ADC_RESULT_VBB	R	0h	10-bit ADC result from the conversion of the VBB voltage

8.6.11 FLT_STAT_CH1 Register (Offset = Dh) [Reset = E000h]

FLT_STAT_CH1 is shown in Table 8-25.

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Table 8-25. FLT_STAT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	7h	Reserved
12	I2T_MOD_CH1	R	0h	This bit indicates if channel 1 in the I2T loop and is accumulating or decrementing. When channel 1 is not in the I2T loop the value will be 0 0h = I2T is off or the channel is not in the I2T loop 1h = Channel is in the I2T loop and is accumulating
11	LATCH_STAT_CH1	R	0h	This bit indicates if channel 1 has been latch off due to an overcurrent protection or thermal shutdown fault. The bit clears when the channel is toggled off and back on. Note: This bit does not signal when a shutdown occurs due to I2T 0h = This channel is not latched off 1h = This channel is currently latched off
10	FLT_CH1	R	0h	This bit indicates if channel 1 is currently in an auto retry wait time period (2ms), latch off, or in I2T cooldown 0h = This channel is currently not in auto retry wait time, latch off state, or I2T cooldown 1h = This channel is currently in auto retry wait time, latch off state, or I2T cooldown
9	SW_STATE_STAT_CH1	R	0h	This bit indicates the current state of channel 1 no matter which mode the device is in as long as SPI is functioning 0h = CH1 is OFF 1h = CH1 is ON
8	VOUT_ERR_CH1	R	0h	This bit indicates if the drain-to-source voltage (VDS) of channel 1 output when enabled is < 2V after the INRUSH_DURATION period. 0h = Output voltage is correct (< 2V) when this channel is enabled 1h = Output voltage is incorrect (> 2V) when this channel is supposed to be enabled or disabled
7	I2T_FLT_CH1	RC	0h	This bit indicates if an I2T fault has occured on channel 1. I2T_EN must be set to 1 in order for this bit indicate an I2T fault. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists Note: This bit does not indicate an overcurrent protection or thermal shutdown fault 0h = no I2T fault has occurred or I2T is not enabled 1h = I2T fault has occurred on this channel
6	LPM_WAKE_CH1	RC	0h	This bit indicates if channel 1 was the cause for the device to come out of MANUAL_LPM regardless of the cause (load step, short-circuit) 0h = The device was not in LPM or this channel was not the cause the device came out of MANUAL_LPM mode 1h = This channel was the reason the device came out of MANUAL_LPM
5	THERMAL_SD_CH1	RC	0h	This bit indicates if thermal shutdown fault has occurred on channel 1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and the channel temperature has fallen below the thermal shutdown hysteresis threshold 0h = No thermal shutdown fault has occurred on this channel 1h = A thermal shutdown fault has occurred on this channel

Table 8-25. FLT_STAT_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ILIMIT_CH1	RC	0h	This bit indicates if an overcurrent protection fault has occurred on channel 1 The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = No overcurrent protection fault has occurred on this channel 1h = Overcurrent protection fault has occurred on this channel
3	SHRT_VBB_CH1	RC	0h	This bit indicates if there was a short to VBB in the off-state on channel 1. The output of channel 2 is pulled down by the RSHRT_VBB internal resistor. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = No Short to VBB fault in off-state has occurred on this channel or short to VBB in off-state is not enabled 1h = Short to VBB fault in the off-state has occurred on this channel
2	OL_OFF_CH1	RC	0h	This bit indicates if there is an open load in the off-state on channel 1. The output of channel 1 is pulled up by the OL_PULLUP_STR setting. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = No off-state open load fault has occurred on this channel or off-state open load detection in off-state is not enabled 1h = Off-state open load fault has occurred on this channel
1	RESERVED	R	0h	Reserved
0	THERMAL_WRN_CH1	RC	0h	This bit indicates if the channel 1 FET temperature is above the overtemperature warning threshold. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = FET temperature is below the over-temperature warning threshold in this channel 1h = FET temperature is above the over-temperature warning threshold in this channel

8.6.12 PWM_CH1 Register (Offset = Eh) [Reset = F000h]

PWM_CH1 is shown in Table 8-26.

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Table 8-26. PWM_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11-9	PWM_FREQ_CH1	R/W	0h	Set the PWM frequency 0h = 0.8 Hz 1h = 3.4 Hz 2h = 13.8 Hz 3h = 111 Hz 4h = 221 Hz 5h = 425 Hz 6h = 885 Hz 7h = 1770 Hz
8-1	PWM_DTY_CH1	R/W	0h	These bits are used to set the duty cycle for the PWM operation for channel 1. Each bit is ~0.39% duty cycle, linearly up to 100% duty cycle
0	PWM_EN_CH1	R/W	0h	This bit enables PWM operation of channel 1. Note: The duty cycle of PWM > 200us. If fault will occur in FLT_STAT_CH1 register. PWM mode can only be enabled if CAP_CHRG_CH1[1:0] = 0 0h = Output follows CH1_ON setting 1h = Output is PWM according to duty cycle and frequency set if CH1_ON is high

8.6.13 ILIM_CONFIG_CH1 Register (Offset = Fh) [Reset = 0088h]

ILIM_CONFIG_CH1 is shown in Table 8-27.

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Table 8-27. ILIM_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved
13-12	CAP_CHRG_CH1	R/W	0h	These bits set the capacitive charging mode during the inrush period after turn on. When CAP_CHRG_CH1 = 00, these are bits are programmed as the overcurrent protection threshold during the INRUSH_DURATION_CH1 period. The channel will immediately turn off if the threshold is reached. When CAP_CHRG_CH1 = 10, these bits are programmed as the current limit regulation threshold. The channel will turn on into the current limit and will continue to regulate the current until the output is fully charged or there is a thermal shutdown event. Note: PWM and I2T is not enabled during the INRUSH_DURATION. 0h = No cap charging mode, IOCP value set by INRUSH_LIMIT_CH1 bits 1h = Not supported 2h = Current limit regulation mode, value set by INRUSH_LIMIT_CH1 bits 3h = Not supported
11	I2T_EN_CH1	R/W	0h	Enables the I2T functionality for channel 1. I2T can be enabled before the channel is enabled or while it is enabled, but the I2T calculation will only start after the inrush period ends. 0h = I2T functionality not enabled 1h = I2T functionality is enabled
10-8	INRUSH_DURATION_CH1	R/W	0h	These bits determine the inrush period duration during which the INRUSH_LIMIT_CH1 level applies. 0h = 0ms 1h = 2ms 2h = 4ms 3h = 6ms 4h = 10ms 5h = 20ms 6h = 50ms 7h = 100ms

Table 8-27. ILIM_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	INRUSH_LIMIT_CH1	R/W	8h	These bits determine the inrush current limit on channel 1 for the different capacitive charging modes set by CAP_CHRG_CH1 bits. If no cap charging mode (CAP_CHRG_CH1 = 00) is used, the values are: 0h = 10A 1h = 12.5A 2h = 15 A 3h = 17.5A 4h = 20A 5h = 22.5A 6h = 25A 7h = 32.5A 8h = 40A 9h = 47.5A Ah = 55A Note: The max INRUSH_LIMIT_CH1 value that is supported for parallel mode for CAP_CHRG_CH1 = 00 is 40A. If current regulation mode (CAP_CHRG_CH1 = 10) is used, the values are: 0h = 1.6A 1h = 2A 2h = 2.4A 3h = 2.8A 4h = 3.3A 5h = 3.6A 6h = 4.2A 7h = 5.5A 8h = 6.8A 9h = 8.1A Ah = 9.5A Bh = 11A Ch = 12A Other settings are not supported.
3-0	ILIMIT_SET_CH1	R/W	8h	These bits determine the overcurrent protection (I_{OCP}) threshold for channel 1 in steady state operation after the INRUSH_DURATION period expires. Note: The max ILIMIT_SET_CH1 value that is supported for parallel mode for CAP_CHRG_CH1 = 00 is 40A. 0h = 10A 1h = 12.5A 2h = 15 A 3h = 17.5A 4h = 20A 5h = 22.5A 6h = 25A 7h = 32.5A 8h = 40A 9h = 47.5A Ah = 55A Other settings are not supported.

8.6.14 CH1_CONFIG Register (Offset = 10h) [Reset = C002h]

CH1_CONFIG is shown in Table 8-28.

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Table 8-28. CH1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VSNS_DIS_CH1	R/W	1h	This bit determines if the VOUT VSNS ADC function for channel 1 is enabled. 0h = CH1 VOUT VSNS ADC functionality enabled 1h = CH1 VOUT VSNS ADC functionality is disabled
14	VDS_SNS_DIS_CH1	R/W	1h	This bit determines if the VDS_SNS ADC function for channel 1 is enabled. 0h = CH1 VDS_SNS ADC functionality enabled 1h = CH1 VDS_SNS ADC functionality is disabled
13	ISNS_DIS_CH1	R/W	0h	This bit determines if the ISNS ADC function for channel 1 is enabled. 0h = CH1 ISNS ADC functionality enabled 1h = CH1 ISNS ADC functionality is disabled
12-11	RESERVED	R/W	0h	Reserved
10	ISNS_SCALE_CH1	R/W	0h	This bit determines the voltage scaling of the channel 1 ISNS for the input to the ADC Note: It is recommended to only use the 8x voltage scaling option when in OL_ON_EN_CH1 = 1 mode and with I2T disabled (I2T_EN_CH1 = 0). If I2T is enabled (I2T_EN_CH1 = 1) and ISNS_SCALE_CH1 = 1, the 8x voltage scaling will be applied to the I2T algorithm which will provide different I2T trip thresholds and can cause the channel to turn off at a lower I2T threshold. 0h = ADC input voltage scale equals 1x 1h = ADC input voltage scale equals 8x
9	OL_ON_EN_CH1	R/W	0h	This bit determines if channel 1 should enter a mode with a higher RON and a lower KSNS value to more accurately measure lower output current. Note: It is recommended to only use OL_ON_EN_CH1 = 1 mode with I2T disabled (I2T_EN_CH1 = 0). If I2T is enabled (I2T_EN_CH1 = 1) and OL_ON_EN_CH1 = 1, the lower K_{SNS2} will be applied to the I2T algorithm which will provide different I2T trip thresholds and can cause the channel to turn off at a lower I2T threshold. The device can only enter this mode if there are no existing faults on the channel and the output current is below $I_{ENTRY\_OL\_ON}$. 0h = KSNS1 ratio and RON = RON 1h = KSNS2 ratio and RON = RON_OL
8-7	OL_SVBB_BLANK_CH1	R/W	0h	These bits determine the blanking time for open load or short to VBB faults in the OFF state for channel 1 0h = Blanking time is 0.4ms 1h = Blanking time is 1.0ms 2h = Blanking time is 2.0ms 3h = Blanking time is 4.0ms
6-5	OL_PU_STR_CH1	R/W	0h	These bits determine the pull-up current (I_pu) at the VOUT1 for the off-state open load detection circuitry. 0h = I_pu is 26.5µA 1h = I_pu is 60µA 2h = I_pu is 127µA 3h = I_pu is 260µA

Table 8-28. CH1_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	OL_SVBB_EN_CH1	R/W	0h	These bits are used to enable open load and short to supply detection in OFF state. Setting the bits to 10 turns on the pull up to see if there is an open load or short to supply in the off state with an output comparator. If OL_OFF_CH1 = 1, then either a short to supply or an open load fault exists. After this, the bits can be set to 01 to turn on a pull down to distinguish a short to supply from an open load in the off state. If there is a short to supply then SHRT_VBB_CH1 = 1 and if not then SHRT_VBB_CH1 = 0 and an open load exists. The above sequence is detailed in the 'Detection With Switch Disabled' section 0h = Disabled 1h = Enables an output pulldown to differentiate short to supply from open load. 2h = Enables a pull-up from VBB supply to output to detect if either an open load or short-to-battery exists. 3h = Only the output comparator is enabled, use external switches and pull-up/pull-down to detect open load or short-to-supply.
2	LATCH_CH1	R/W	0h	This bit determines if channel 1 should auto-retry or latch off after an overcurrent or thermal shutdown event has occurred. 0h = Channel 1 will auto retry after tRETRY expires and THYS is reached 1h = Channel 1 latches off until SW_STATE register is written to again
1-0	SLRT_CH1	R/W	2h	These bits determine the turn on and turn off slew rates for channel 1. 0h = 0.25V/µs 1h = 0.34V/µs 2h = 0.45V/µs 3h = 0.55V/µs

8.6.15 ADC_RESULT_CH1_I Register (Offset = 11h) [Reset = F000h]

ADC_RESULT_CH1_I is shown in Table 8-29.

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Table 8-29. ADC_RESULT_CH1_I Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11	ISNS_SCALE_EFF_CH1	R	0h	The bit indicates the voltage scaling factor used for the conversion 0h = 1x ISNS1 voltage scaling 1h = 8x ISNS1 voltage scaling
10	ISNS_RDY_CH1	R	0h	Making sure the ADC conversion is new from the last time this was read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_I	R	0h	ADC result (10-bits) from the conversion of the current in CH1

8.6.16 ADC_RESULT_CH1_T Register (Offset = 12h) [Reset = F800h]

ADC_RESULT_CH1_T is shown in Table 8-30.

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Table 8-30. ADC_RESULT_CH1_T Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	TSNS_RDY_CH1	R	0h	This bit indicates if a new ADC result for channel 1 TSNS conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_T	R	0h	10-bit ADC result from the conversion of channel 1 FET temperature (TSNS)

8.6.17 ADC_RESULT_CH1_V Register (Offset = 13h) [Reset = F800h]

ADC_RESULT_CH1_V is shown in Table 8-31.

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Table 8-31. ADC_RESULT_CH1_V Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VSNS_RDY_CH1	R	0h	This bit indicates if a new ADC result for channel 1 VOUT voltage (VSNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_V	R	0h	10-bit ADC result from the conversion of channel 1 VOUT voltage (VSNS)

8.6.18 ADC_RESULT_CH1_VDS Register (Offset = 14h) [Reset = F800h]

ADC_RESULT_CH1_VDS is shown in Table 8-32.

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Table 8-32. ADC_RESULT_CH1_VDS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VDSSNS_RDY_CH1	R	0h	This bit indicates if a new ADC result for channel 1 VDS voltage (VDSSNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_VDS	R	0h	10-bit ADC result from the conversion of channel 1 VDS voltage (VDSSNS)

8.6.19 I2T_CONFIG_CH1 Register (Offset = 15h) [Reset = 0000h]

I2T_CONFIG_CH1 is shown in Table 8-33.

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Table 8-33. I2T_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TCLDN_CH1	R/W	0h	These bits set the cool down time (or time to retry) after an I2T shutdown for Channel 1. Note: If setting 0x0 is used, the channel will remain off after an I2T shutdown with no retry. To retry in this setting, change the bits to 0.8s, 2.0s, or 4.0s options to allow the device to retry after an I2T shutdown. 0h = indefinite cooldown 1h = 0.8s 2h = 2.0s 3h = 4.0s
13-11	RESERVED	R/W	0h	Reserved
10-9	SWCL_DLY_TMR_CH1	R/W	0h	These bits set the timer at which Channel 1 will shut down if the IOUT current continuously exceeds the ISWCL level for the configured time. 0h = 0.2ms 1h = 0.4ms 2h = 1.0ms 3h = 2.0ms
8-7	ISWCL_CH1	R/W	0h	These bits set the delayed turn off current sense value ($I_{SWCL,700}$) for channel 1. Once the IOUT current exceeds the $I_{SWCL,700}$ value, a timer starts and will turn off the channel if the current remains above the $I_{SWCL,700}$ threshold for a duration of SWCL_DLY_TMR_CH1. The threshold should be set below the current sense saturation value ($I_{OUT\_SAT} = K_{SNS1} * I_{SNS\_SAT}$). The current threshold below assume R_{SNS} = 700Ω. To calculate the new $I_{SWCL,700}$ thresholds based on a different R_{SNS} value, the following equation can be used: $I_{SWCL,ADJ} = I_{SWCL,700} * (700 / R_{SNS})$ 0h = 19.55A 1h = 17.6A 2h = 16.05A 3h = 13.3A

Table 8-33. I2T_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-3	I2T_TRIP_CH1	R/W	0h	These bits set the I2T trip value for Channel 1. Note: For reference the equation for the I2T trip value is: $I2T = (I_{OUT1}{}^2 - NOM\_CUR\_CH1^2) * t$ The below values assume R_{SNS} = 700Ω. To calculate the new I2T trip values based on a different R_{SNS} value, the following equation can be used: $I2T_{ADJ} = I2T_{700} * (700 / R_{SNS})^2$ Note: The I2T_TRIP_CH1 value cannot be modified when the device is in the cool down time period. 0h = 8.8 A2s 1h = 13.1 A2s 2h = 26.3 A2s 3h = 39.4 A2s 4h = 52.5 A2s 5h = 65.6 A2s 6h = 78.8 A2s 7h = 91.9 A2s 8h = 109.4 A2s 9h = 126.9 A2s Ah = 144.4 A2s Bh = 166.3 A2s Ch = 192.5 A2s Dh = 218.8 A2s Eh = 262.5 A2s Fh = 350 A2s
2-0	NOM_CUR_CH1	R/W	0h	These bits set the nominal current value for channel 1 for the I2T function. If the I2T function is enabled for channel 1, above this value the device will enter the I2T accumulation mode. The nominal current values below assume R_{SNS} = 700Ω. To calculate the new I2T trip values based on a different R_{SNS} value, the following equation can be used: $NOM\_CUR\_CH1_{ADJ} = NOM\_CUR\_CH1_{700} * (700 / R_{SNS})$ Note: The NOM_CUR_CH1 value cannot be modified when the device is in the cool down time period. 0h = 4.0 A 1h = 5.0 A 2h = 5.7 A 3h = 6.5 A 4h = 7.5 A 5h = 9.0 A 6h = 12.0 A 7h = 15.0 A

8.6.20 FLT_STAT_CH2 Register (Offset = 16h) [Reset = E000h]

FLT_STAT_CH2 is shown in Table 8-34.

Return to the Summary Table.

Table 8-34. FLT_STAT_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	7h	Reserved
12	I2T_MOD_CH2	R	0h	This bit indicates if channel 2 in the I2T loop and is accumulating or decrementing. When channel 2 is not in the I2T loop the value will be 0 0h = I2T is off or the channel is not in the I2T loop 1h = Channel is in the I2T loop and is accumulating
11	LATCH_STAT_CH2	R	0h	This bit indicates if channel 2 has been latch off due to an overcurrent protection or thermal shutdown fault. The bit clears when the channel is toggled off and back on. Note: This bit does not signal when a shutdown occurs due to I2T 0h = This channel is not latched off 1h = This channel is currently latched off
10	FLT_CH2	R	0h	This bit indicates if channel 2 is currently in an auto retry wait time period (2ms), latch off, or in I2T cooldown 0h = This channel is currently not in auto retry wait time, latch off state, or I2T cooldown 1h = This channel is currently in auto retry wait time, latch off state, or I2T cooldown
9	SW_STATE_STAT_CH2	R	0h	This bit indicates the current state of channel 2 no matter which mode the device is in as long as SPI is functioning 0h = CH2 is OFF 1h = CH2 is ON
8	VOUT_ERR_CH2	R	0h	This bit indicates if the drain-to-source voltage (VDS) of channel 2 output when enabled is < 2V after the INRUSH_DURATION period. 0h = Output voltage is correct (< 2V) when this channel is enabled 1h = Output voltage is incorrect (> 2V) when this channel is supposed to be enabled or disabled
7	I2T_FLT_CH2	RC	0h	This bit indicates if an I2T fault has occured on channel 2. I2T_EN must be set to 1 in order for this bit indicate an I2T fault. The fault is latched and cleared when FLT_STAT_CH2 register is read and the fault condition no longer exists Note: This bit does not indicate an overcurrent protection or thermal shutdown fault 0h = no I2T fault has occurred or I2T is not enabled 1h = I2T fault has occurred on this channel
6	LPM_WAKE_CH2	RC	0h	This bit indicates if channel 2 was the cause for the device to come out of MANUAL_LPM regardless of the cause (load step, short-circuit) 0h = The device was not in LPM or this channel was not the cause the device came out of MANUAL_LPM mode 1h = This channel was the reason the device came out of MANUAL_LPM
5	THERMAL_SD_CH2	RC	0h	This bit indicates if thermal shutdown fault has occurred on channel 2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and the channel temperature has fallen below the thermal shutdown hysteresis threshold 0h = No thermal shutdown fault has occurred on this channel 1h = A thermal shutdown fault has occurred on this channel

Table 8-34. FLT_STAT_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ILIMIT_CH2	RC	0h	This bit indicates if an overcurrent protection fault has occurred on channel 2 The fault is latched and cleared when FLT_STAT_CH2 register is read and the fault condition no longer exists 0h = No overcurrent protection fault has occurred on this channel 1h = Overcurrent protection fault has occurred on this channel
3	SHRT_VBB_CH2	RC	0h	This bit indicates if there was a short to VBB in the off-state on channel 2. The output of channel 2 is pulled down by the RSHRT_VBB internal resistor. The fault is latched and cleared when FLT_STAT_CH2 register is read and the fault condition no longer exists 0h = No Short to VBB fault in off-state has occurred on this channel or short to VBB in off-state is not enabled 1h = Short to VBB fault in the off-state has occurred on this channel
2	OL_OFF_CH2	RC	0h	This bit indicates if there is an open load in the off-state on channel 2. The output of channel 2 is pulled up by the OL_PULLUP_STR setting. The fault is latched and cleared when FLT_STAT_CH2 register is read and the fault condition no longer exists 0h = No off-state open load fault has occurred on this channel or off-state open load detection in off-state is not enabled 1h = Off-state open load fault has occurred on this channel
1	RESERVED	R	0h	Reserved
0	THERMAL_WRN_CH2	RC	0h	This bit indicates if the channel 2 FET temperature is above the overtemperature warning threshold. The fault is latched and cleared when FLT_STAT_CH2 register is read and the fault condition no longer exists 0h = FET temperature is below the over-temperature warning threshold in this channel 1h = FET temperature is above the over-temperature warning threshold in this channel

8.6.21 PWM_CH2 Register (Offset = 17h) [Reset = F000h]

PWM_CH2 is shown in Table 8-35.

Return to the Summary Table.

Table 8-35. PWM_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11-9	PWM_FREQ_CH2	R/W	0h	Set the PWM frequency 0h = 0.8 Hz 1h = 3.4 Hz 2h = 13.8 Hz 3h = 111 Hz 4h = 221 Hz 5h = 425 Hz 6h = 885 Hz 7h = 1770 Hz
8-1	PWM_DTY_CH2	R/W	0h	These bits are used to set the duty cycle for the PWM operation for channel 2. Each bit is ~0.39% duty cycle, linearly up to 100% duty cycle
0	PWM_EN_CH2	R/W	0h	This bit enables PWM operation of channel 2. Note: The duty cycle of PWM > 200us. If fault will occur in FLT_STAT_CH2 register. PWM mode can only be enabled if CAP_CHRG_CH2[1:0] = 0 0h = Output follows CH2_ON setting 1h = Output is PWM according to duty cycle and frequency set if CH2_ON is high

8.6.22 ILIM_CONFIG_CH2 Register (Offset = 18h) [Reset = 0088h]

ILIM_CONFIG_CH2 is shown in Table 8-36.

Return to the Summary Table.

Table 8-36. ILIM_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved
13-12	CAP_CHRG_CH2	R/W	0h	These bits set the capacitive charging mode during the inrush period after turn on. When CAP_CHRG_CH1 = 00, these are bits are programmed as the overcurrent protection threshold during the INRUSH_DURATION_CH1 period. The channel will immediately turn off if the threshold is reached. When CAP_CHRG_CH1 = 10, these bits are programmed as the current limit regulation threshold. The channel will turn on into the current limit and will continue to regulate the current until the output is fully charged or there is a thermal shutdown event. Note: PWM and I2T is not enabled during the INRUSH_DURATION. 0h = No cap charging mode, IOCP value set by INRUSH_LIMIT_CH1 bits 1h = Not supported 2h = Current limit regulation mode, value set by INRUSH_LIMIT_CH1 bits 3h = Not supported
11	I2T_EN_CH2	R/W	0h	Enables the I2T functionality for channel 2. I2T can be enabled before the channel is enabled or while it is enabled, but the I2T calculation will only start after the inrush period ends. 0h = I2T functionality not enabled 1h = I2T functionality is enabled
10-8	INRUSH_DURATION_CH2	R/W	0h	These bits determine the inrush period duration during which the INRUSH_LIMIT_CH2 level applies. 0h = 0ms 1h = 2ms 2h = 4ms 3h = 6ms 4h = 10ms 5h = 20ms 6h = 50ms 7h = 100ms

Table 8-36. ILIM_CONFIG_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	INRUSH_LIMIT_CH2	R/W	8h	These bits determine the inrush current limit on channel 2 for the different capacitive charging modes set by CAP_CHRG_CH1 bits. If no cap charging mode (CAP_CHRG_CH2 = 00) is used, the values are: 0h = 10A 1h = 12.5A 2h = 15 A 3h = 17.5A 4h = 20A 5h = 22.5A 6h = 25A 7h = 32.5A 8h = 40A 9h = 47.5A Ah = 55A If current regulation mode (CAP_CHRG_CH2 = 10) is used, the values are: 0h = 1.6A 1h = 2A 2h = 2.4A 3h = 2.8A 4h = 3.3A 5h = 3.6A 6h = 4.2A 7h = 5.5A 8h = 6.8A 9h = 8.1A Ah = 9.5A Bh = 11A Ch = 12A Other settings are not supported.
3-0	ILIMIT_SET_CH2	R/W	8h	These bits determine the overcurrent protection (I_{OCP}) threshold for channel 2 in steady state operation after the INRUSH_DURATION period expires. 0h = 10A 1h = 12.5A 2h = 15 A 3h = 17.5A 4h = 20A 5h = 22.5A 6h = 25A 7h = 32.5A 8h = 40A 9h = 47.5A Ah = 55A Other settings are not supported.

8.6.23 CH2_CONFIG Register (Offset = 19h) [Reset = C002h]

CH2_CONFIG is shown in Table 8-37.

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Table 8-37. CH2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VSNS_DIS_CH2	R/W	1h	This bit determines if the VOUT VSNS ADC function for channel 2 is enabled. 0h = CH2 VOUT VSNS ADC functionality enabled 1h = CH2 VOUT VSNS ADC functionality is disabled
14	VDSSNS_DIS_CH2	R/W	1h	This bit determines if the VDS_SNS ADC function for channel 2 is enabled. 0h = CH2 VDS_SNS ADC functionality enabled 1h = CH2 VDS_SNS ADC functionality is disabled
13	ISNS_DIS_CH2	R/W	0h	This bit determines if the ISNS ADC function for channel 2 is enabled. 0h = CH2 ISNS ADC functionality enabled 1h = CH2 ISNS ADC functionality is disabled
12-11	RESERVED	R/W	0h	Reserved
10	ISNS_SCALE_CH2	R/W	0h	This bit determines the voltage scaling of the channel 2 ISNS for the input to the ADC Note: It is recommended to only use the 8x voltage scaling option when in OL_ON_EN_CH2 = 1 mode and with I2T disabled (I2T_EN_CH2 = 0). If I2T is enabled (I2T_EN_CH2 = 1) and ISNS_SCALE_CH2 = 1, the 8x voltage scaling will be applied to the I2T algorithm which will provide different I2T trip thresholds and can cause the channel to turn off at a lower I2T threshold. 0h = ADC input voltage scale equals 1x 1h = ADC input voltage scale equals 8x
9	OL_ON_EN_CH2	R/W	0h	This bit determines if channel 2 should enter a mode with a higher RON and a lower KSNS value to more accurately measure lower output current. Note: It is recommended to only use OL_ON_EN_CH2 = 1 mode with I2T disabled (I2T_EN_CH2 = 0). If I2T is enabled (I2T_EN_CH2 = 1) and OL_ON_EN_CH2 = 1, the lower K_{SNS2} will be applied to the I2T algorithm which will provide different I2T trip thresholds and can cause the channel to turn off at a lower I2T threshold. The device can only enter this mode if there are no existing faults on the channel and the output current is below $I_{ENTRY\_OL\_ON}$. 0h = KSNS1 ratio and RON = RON 1h = KSNS2 ratio and RON = RON_OL
8-7	OL_SVBB_BLANK_CH2	R/W	0h	These bits determine the blanking time for open load or short to VBB faults in the OFF state for channel 2 0h = Blanking time is 0.4ms 1h = Blanking time is 1.0ms 2h = Blanking time is 2.0ms 3h = Blanking time is 4.0ms
6-5	OL_PU_STR_CH2	R/W	0h	These bits determine the pull-up current (I_pu) at the VOUT1 for the off-state open load detection circuitry. 0h = I_pu is 26.5µA 1h = I_pu is 60µA 2h = I_pu is 127µA 3h = I_pu is 260µA

Table 8-37. CH2_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	OL_SVBB_EN_CH2	R/W	0h	These bits are used to enable open load and short to supply detection in OFF state. Setting the bits to 10 turns on the pull up to see if there is an open load or short to supply in the off state with an output comparator. If OL_OFF_CH2 = 1, then either a short to supply or an open load fault exists. After this, the bits can be set to 01 to turn on a pull down to distinguish a short to supply from an open load in the off state. If there is a short to supply then SHRT_VBB_CH2 = 1 and if not then SHRT_VBB_CH2 = 0 and an open load exists. The above sequence is detailed in the 'Detection With Switch Disabled' section 0h = Disabled 1h = Turns-on an output pulldown to differentiate Short to supply from open load. 2h = Turns on a pull-up from VBB supply to output to detect if either an open load or short-to-battery exists. 3h = Output comparator enabled, use external switches and pull-up/pull-down to detect open load or short-to-supply.
2	LATCH_CH2	R/W	0h	This bit determines if channel 2 should auto-retry or latch off after an overcurrent or thermal shutdown event has occurred. 0h = channel 2 will auto retry after tRETRY expires and THYS is reached 1h = channel 2 latches off until SW_STATE register is written to again
1-0	SLRT_CH2	R/W	2h	These bits determine the turn on and turn off slew rates for channel 2. 0h = 0.25V/µs 1h = 0.34V/µs 2h = 0.45V/µs 3h = 0.55V/µs

8.6.24 ADC_RESULT_CH2_I Register (Offset = 1Ah) [Reset = F000h]

ADC_RESULT_CH2_I is shown in Table 8-38.

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Table 8-38. ADC_RESULT_CH2_I Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11	ISNS_SCALE_EFF_CH2	R	0h	The bit indicates the voltage scaling factor used for the conversion 0h = 1x ISNS2 voltage scaling 1h = 8x ISNS2 voltage scaling
10	ISNS_RDY_CH2	R	0h	Making sure the ADC conversion is new from the last time this was read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH2_I	R	0h	ADC result (10-bits) from the conversion of the current in CH2

8.6.25 ADC_RESULT_CH2_T Register (Offset = 1Bh) [Reset = F800h]

ADC_RESULT_CH2_T is shown in Table 8-39.

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Table 8-39. ADC_RESULT_CH2_T Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	TSNS_RDY_CH2	R	0h	This bit indicates if a new ADC result for channel 2 TSNS conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH2_T	R	0h	10-bit ADC result from the conversion of channel 2 FET temperature (TSNS)

8.6.26 ADC_RESULT_CH2_V Register (Offset = 1Ch) [Reset = F800h]

ADC_RESULT_CH2_V is shown in Table 8-40.

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Table 8-40. ADC_RESULT_CH2_V Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VSNS_RDY_CH2	R	0h	This bit indicates if a new ADC result for channel 2 VOUT voltage (VSNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH2_V	R	0h	10-bit ADC result from the conversion of channel 2 VOUT voltage (VSNS)

8.6.27 ADC_RESULT_CH2_VDS Register (Offset = 1Dh) [Reset = F800h]

ADC_RESULT_CH2_VDS is shown in Table 8-41.

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Table 8-41. ADC_RESULT_CH2_VDS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VDSSNS_RDY_CH2	R	0h	This bit indicates if a new ADC result for channel 2 VDS voltage (VDSSNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH2_VDS	R	0h	10-bit ADC result from the conversion of channel 2 VDS voltage (VDSSNS)

8.6.28 I2T_CONFIG_CH2 Register (Offset = 1Eh) [Reset = 0000h]

I2T_CONFIG_CH2 is shown in Table 8-42.

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Table 8-42. I2T_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TCLDN_CH2	R/W	0h	These bits set the cool down time (or time to retry) after an I2T shutdown for channel 2. Note: If setting 0x0 is used, the channel will remain off after an I2T shutdown with no retry. To retry in this setting, change the bits to 0.8s, 2.0s, or 4.0s options to allow the device to retry after an I2T shutdown. 0h = indefinite cooldown 1h = 0.8s 2h = 2.0s 3h = 4.0s
13-11	RESERVED	R/W	0h	Reserved
10-9	SWCL_DLY_TMR_CH2	R/W	0h	These bits set the timer at which channel 2 will shut down if the I_{OUT} current continuously exceeds the ISWCL level for the configured time. 0h = 0.2ms 1h = 0.4ms 2h = 1.0ms 3h = 2.0ms
8-7	ISWCL_CH2	R/W	0h	These bits set the delayed turn off current sense value ($I_{SWCL,700}$) for channel 2. Once the I_{OUT} current exceeds the $I_{SWCL,700}$ value, a timer starts and will turn off the channel if the current remains above the $I_{SWCL,700}$ threshold for a duration of SWCL_DLY_TMR_CH2. The threshold should be set below the current sense saturation value ($I_{OUT\_SAT} = K_{SNS1} * I_{SNS\_SAT}$). The current threshold below assume R_{SNS} = 700Ω. To calculate the new $I_{SWCL,700}$ thresholds based on a different R_{SNS} value, the following equation can be used: $I_{SWCL,ADJ} = I_{SWCL,700} * (700 / R_{SNS})$ 0h = 19.55A 1h = 17.6A 2h = 16.05A 3h = 13.3A

Table 8-42. I2T_CONFIG_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-3	I2T_TRIP_CH2	R/W	0h	These bits set the I2T trip value for Channel 2. Note: For reference the equation for the I2T trip value is: $I2T = (I_{OUT2}{}^2 - NOM\_CUR\_CH2^2) * t$ The below values assume R_{SNS} = 700Ω. To calculate the new I2T trip values based on a different R_{SNS} value, the following equation can be used: $I2T_{ADJ} = I2T_{700} * (700 / R_{SNS})^2$ Note: The I2T_TRIP_CH2 value cannot be modified when the device is in the cool down time period. 0h = 8.8 A2s 1h = 13.1 A2s 2h = 26.3 A2s 3h = 39.4 A2s 4h = 52.5 A2s 5h = 65.6 A2s 6h = 78.8 A2s 7h = 91.9 A2s 8h = 109.4 A2s 9h = 126.9 A2s Ah = 144.4 A2s Bh = 166.3 A2s Ch = 192.5 A2s Dh = 218.8 A2s Eh = 262.5 A2s Fh = 350 A2s
2-0	NOM_CUR_CH2	R/W	0h	These bits set the nominal current value for channel 2 for the I2T function. If the I2T function is enabled for channel 2, above this value the device will enter the I2T accumulation mode. The nominal current values below assume R_{SNS} = 700Ω. To calculate the new I2T trip values based on a different R_{SNS} value, the following equation can be used: $NOM\_CUR\_CH2_{ADJ} = NOM\_CUR\_CH2_{700} * (700 / R_{SNS})$ Note: The NOM_CUR_CH2 value cannot be modified when the device is in the cool down time period. 0h = 4.0 A 1h = 5.0 A 2h = 5.7 A 3h = 6.5 A 4h = 7.5 A 5h = 9.0 A 6h = 12.0 A 7h = 15.0 A

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Figure 9-1 and Figure 9-2 shows the schematic of a typical application of the TPS2HCS08A-Q1 and TPS2HCS08B-Q1, respectively. It includes all standard external components. This section of the data sheet discusses the considerations in implementing commonly required application functionality. The circuit assumes no reverse polarity protection on the input supply, so additional components for protection are required.

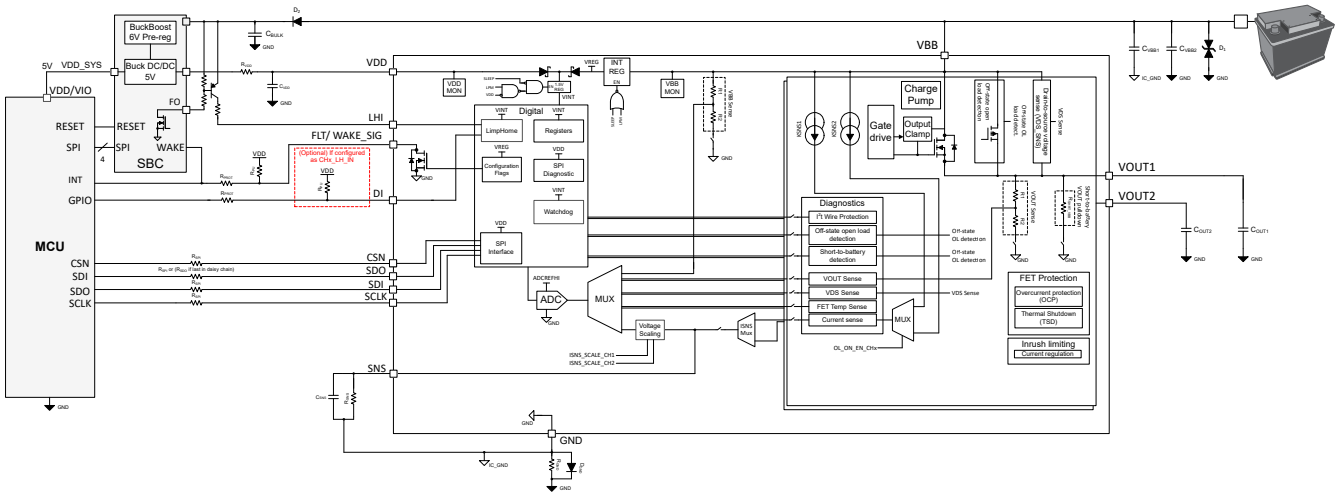

Figure 9-1. System Diagram - TPS2HCS08A-Q1

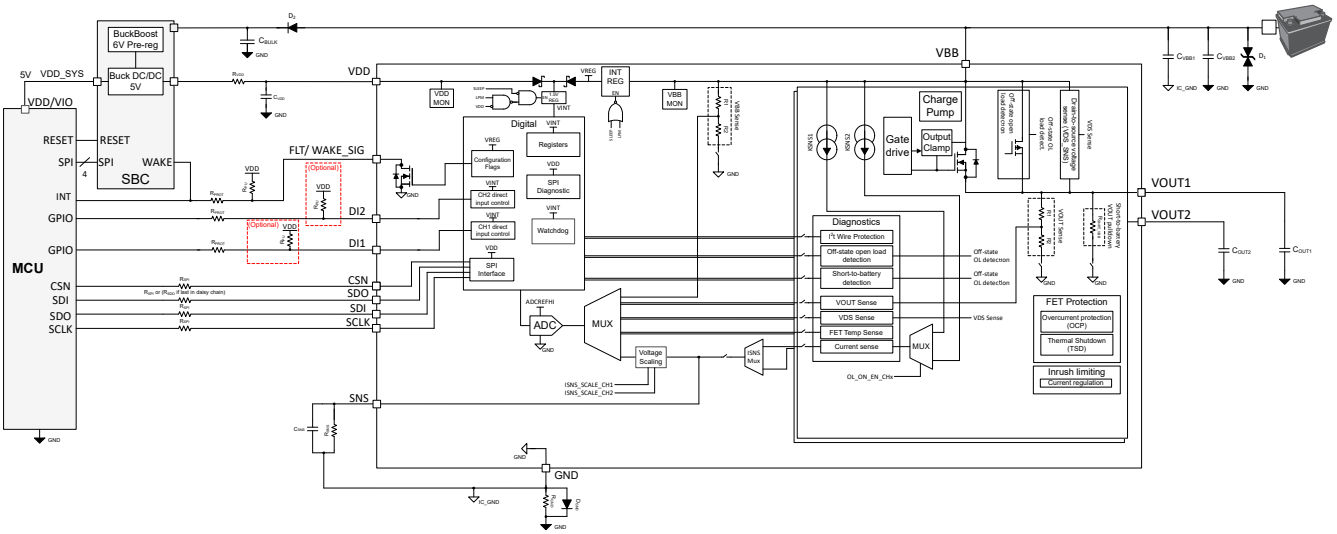

Figure 9-2. System Diagram - TPS2HCS08B-Q1

With the ground protection network, the device ground will be offset relative to the micro-controller ground. The same power supply (5V (recommended) or 3.3V) source should be used for the controller (MCU) I/O as well as the VDD supply input to the TPS2HCS08B-Q1 device.

Table 9-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{SPI}	22Ω	(Optional) For EMI or other transient limits on the SPI pins.
R_{SDO}	768Ω	Higher values to increase the total resistance to MCU VDD to 768 Ω for ground loss detection
R_{PROT}	10kΩ	Protect micro-controller and device GPIO pins
R_{PU}	4.7kΩ	Pull-up resistor
R_{SNS}	0.2-1.5kΩ	Translate the sense current into sense voltage for internal ADC input
C_{SNS}	1 - 4.7nF	Low-pass filter for the ADC input.
D_1	+/-36V	To suppress voltage transients (one for the module)
D_{GND}	BAS21 / Schottky Diode	To limit the voltage drop across R_{GND} during normal operation of the device. A low forward voltage diode is recommended and a schottky diode is suggested when the VDD is 3.3V. (**Note:** Recommended VDD operation is 5V for lower Iq)
R_{GND}	4.7kΩ	Maintain ground potential during negative output voltage excursions
R_{VDD}	10Ω	Limit the rate of rise / fall in VDD supply input- to the IC.
C_{VDD}	470nF	VDD supply voltage stability to system ground.
C_{VBB1}	1nF to IC_GND	(Optional) For improved emissions.
C_{VBB2}	100 – 2200nF to Module GND	Stabilize the input supply and filter out low frequency noise.
C_{OUTx}	22nF - 100nF	Filtering of voltage transients (for example, ESD, ISO7637-2). If MANUAL_LPM mode is used and a schottky or TVS diode is not used at the output, 100nF is the recommended capacitor value for hot short-circuit protection in MANUAL_LPM.

9.2 Typical Application

This application example demonstrates how the TPS2HC10S-Q1 device can be used to power ECU loads with large input capacitance. This is just one example of the many applications where this device can fit.

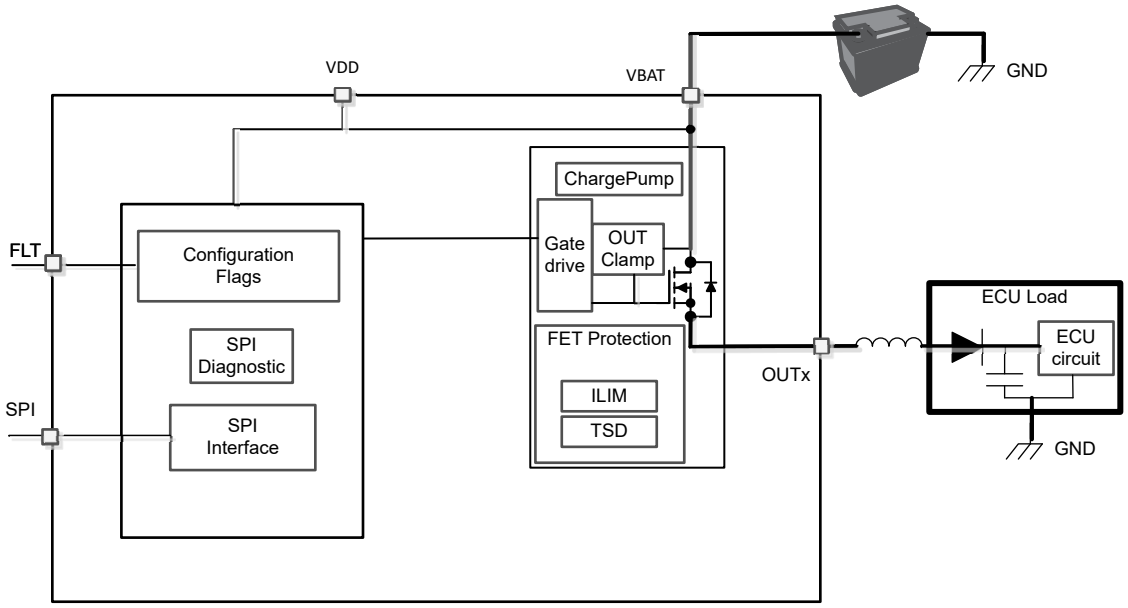

Figure 9-3. Block Diagram for Powering an ECU load with Input Capacitance

9.2.1 Design Requirements

For this design example, use the input parameters shown in Table 9-2.

Table 9-2. Design Parameters

DESIGN PARAMETER	CASE 1
V_{BB} range	8V to 16V
Input Capacitance of the ECU load	600µF
Maximum parallel load during the charging phase	3A
Time to charge	2ms
Ambient temperature	85°C

9.2.2 Detailed Design Procedure

9.2.2.1 Thermal Considerations

The output voltage ramps while the load capacitance is being charged. During this period, the power dissipation in the FET is high due to the large drain-to-source voltage. The power dissipation and the resultant increase in the silicon junction temperature limits the capacitance that can be charged before the device hits thermal shutdown. In general, lower the charging rate (current), the higher the value of capacitance that can be charged. But if a lower charging current is used, the charging time will be higher. In the application cases considered here, it is expected that the FET junction temperature will not reach the thermal shutdown threshold.

9.2.2.2 Configuring the Capacitive Charging Mode

The configuration parameters for the two channels are in the ILIM_CONFIG_CHx registers. The device offers a constant current charging mode designed for cases where there is a significant load current during charging phase. The current limit regulation value is set by the INRUSH_LIMIT_CHx bits ([7:4]) in the ILIM_CONFIG_CHx registers. The INRUSH_DURATION_CHx bits should be set such that the worst case expected capacitive charge time is below the programmed inrush duration. The recommended choice of bit settings for each application case is listed in the table below.

Table 9-3. Setting Capacitive Charging Mode Parameters

Bit Field in the ILIM_CONFIG_CHx Register	Case 1
CAP_CHRG_CHx	0x02h
INRUSH_DURATION_CHx	0x02h
INRUSH_LIMIT_CHx	0x06h

9.2.3 Application Curves

I_{CL_REG} - Capacitive Charging Performance (CAP_CHRG_CHx = 10)

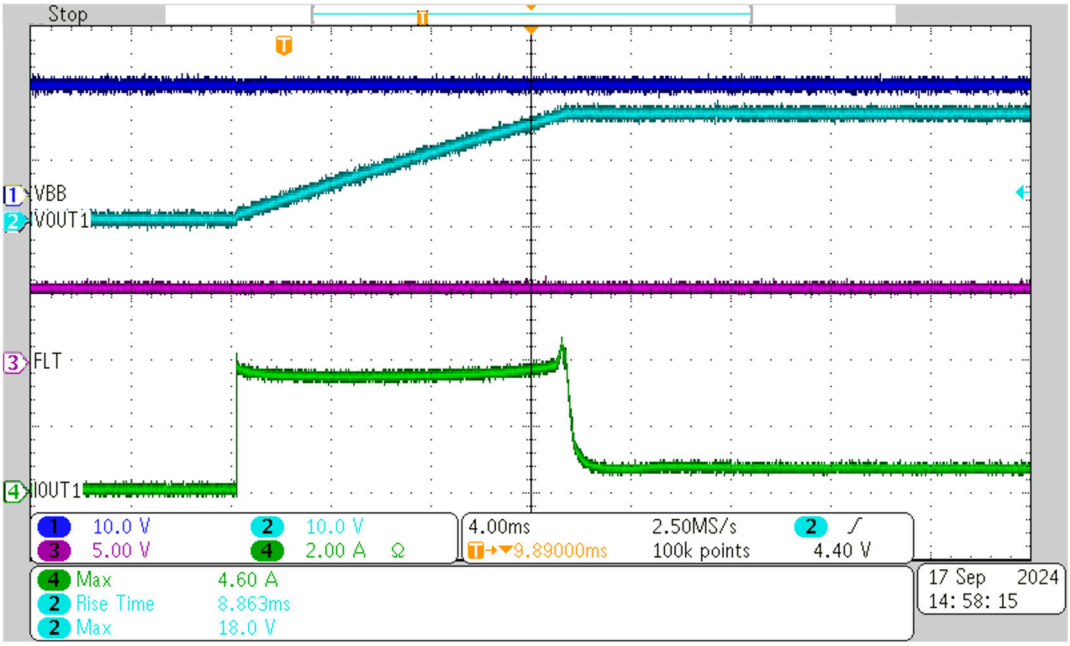

Figure 9-4. I_{CL_REG} - Current Limit Regulation, V_{BB} = 16V, T_{AMB} = 105C, INRUSH_DURATION = 0x7 (100ms), INRUSH_LIMIT_CHx = 0x6 (4.2A)

9.3 Power Supply Recommendations

The device is designed to operate in a 12V automotive system. The device works with two power supply inputs – a typically 12V battery input and a low voltage supply input (5V or 3.3V) typically generated with a DC-DC converter (recommended to reduce quiescent current draw from the battery) or LDO external to the IC from the battery.

The nominal supply voltage range is 6V to 18V as measured at the V_{BB} pin with respect to the GND pin of the device. In this range the device meets full parametric specifications as listed in the *Electrical Characteristics* table. The device is also designed to withstand voltage transients beyond this range like load dump. When operating outside of the nominal voltage range but within the operating voltage range, the device will exhibit normal functional behavior.

Table 9-4. Operating Voltage Range

V_{BB} VOLTAGE RANGE	NOTE
3V to 6V	Extended lower 12V automotive battery operation such as cold crank and start-stop. Device is fully functional and protected but some parametrics such as RON, current sense accuracy, over-current thresholds and timing parameters can deviate from specifications. Check the individual specifications in the *Electrical Characteristics* to confirm the voltage range it is applicable for.

Table 9-4. Operating Voltage Range (continued)

V_{BB} VOLTAGE RANGE	NOTE
6V to 18V	Nominal supply voltage, all parametric specifications apply.
18V to 24V	Extended upper 12V automotive battery operation such as double battery. Device is fully functional and protected but some parametrics such as RON, current sense accuracy, over-current thresholds, and timing parameters can deviate from specifications. Check the individual specifications in the Electrical Characteristics to confirm the voltage range it is applicable for. The device is short-circuit protected up to 125°C.
24V to 35V	Load dump voltage. Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.

9.4 Layout

9.4.1 Layout Guidelines

To achieve optimal thermal performance, connect the exposed pad to a large copper pour. On the top PCB layer, the pour may extend beyond the package dimensions as shown in the layout examples below. In addition to this, it is recommended to have a VBB plane on one or more internal PCB layers and/or on the bottom layer. Vias should connect these planes to the top VBB pour.

TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer.

The R_{SNS} and C_{SNS} components should be placed close to the SNS pin. If a ground network is used for reverse battery protection, the R_{SNS} and C_{SNS} should be connected from the SNS pin to the IC_GND net for accurate current sense measurements by the internal ADC.

If used in the design, C_{VBB1}, should be placed as close as possible to the VBB and GND pin of the device. If a ground network is used for reverse battery protection, the C_{VBB1} capacitor should be connected from the VBB net to the IC_GND net.

9.4.2 Layout Example

Figure 9-5 and Figure 9-6 below show example PCB layouts with and without a GND network, respectively. TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer. For TPS2HCS08B-Q1 device, DI and LHI pins in the below example PCB layouts would be replaced with DI1 and DI2 pins, respectively.

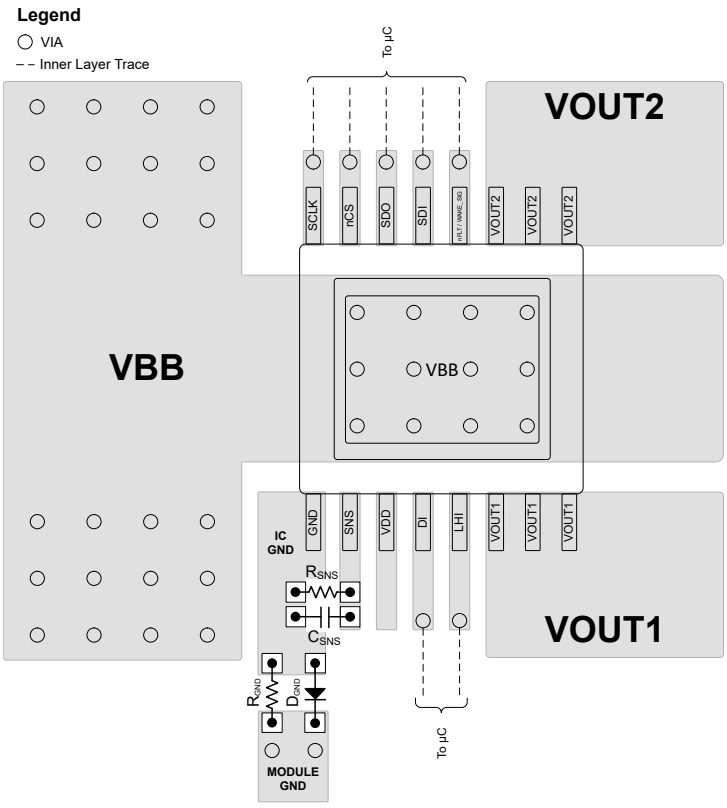

Figure 9-5. Layout Example with Ground Network

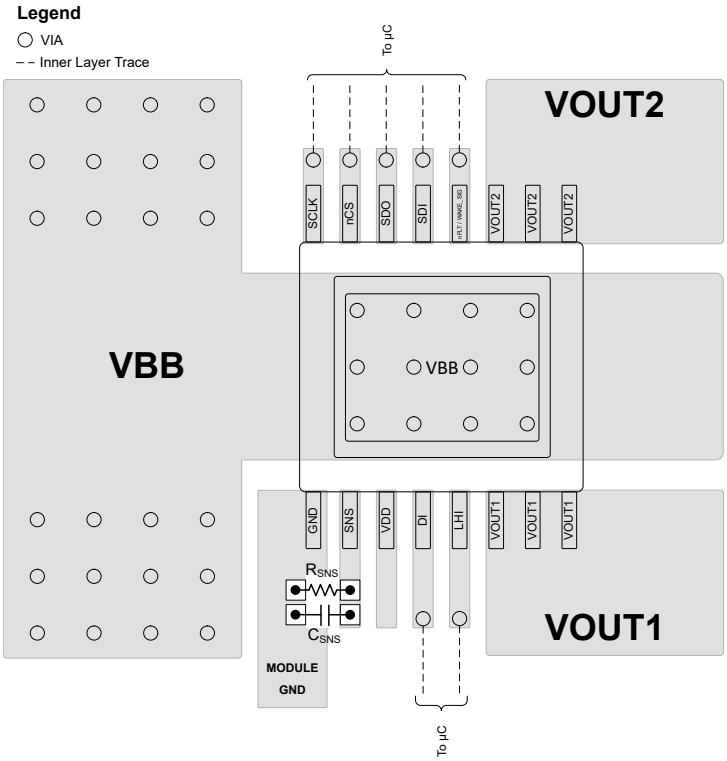

Figure 9-6. Layout Example without Ground Network

10 Device and Documentation Support

10.1 Documentation Support

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2HCS08AQPWPRQ1	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	2HS08A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

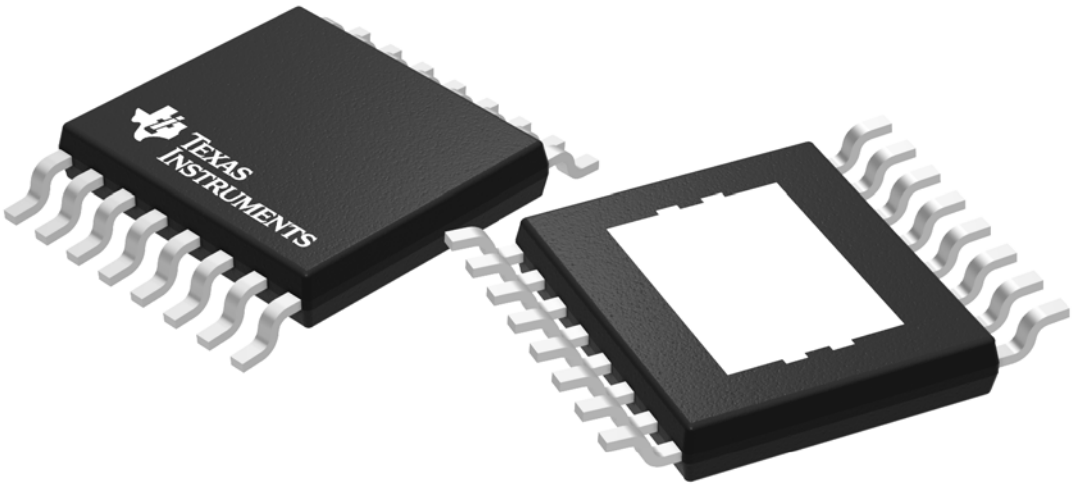
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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