TPS26744E-Q1 Automotive Dual-Port USB Type-C® PD Controller with 240W EPR and DisplayPort™ over USB Type-C®

ADVANCE INFORMATION

1 Features

- TPS26744E-Q1 is a fully configurable dual-port PD3.2 Source controller.
  - Extended Power Range (EPR) support
  - 40V tolerant VBUS
  - 24V tolerant CC and DP/DM pins
  - GUI tool to easily configure for various applications
  - Programmable Power Supply (PPS) support (source)
- USB Type-C Power Delivery (PD) controller
  - USB PD R3.2 compliant
  - USB Type-C R2.4 compliant
  - DisplayPort Alternate Mode support
  - 20 configurable GPIOs
  - Cable attach and orientation detection
  - Integrated VCONN switch. No external supply required to read eMarker
  - Physical layer and policy engine
  - Integrated LDO with input up to 40V
  - 1 I^2C controller port (I2C2)
  - 2 I^2C target ports (I2C1, I2C3)
  - UART and LIN support
  - Closed-chassis debugging
- Integrated flash memory supporting updates via I^2C gated by an authentication check
  - Closed-chassis flash updates via I2C4
- System power management
  - Across multiple ports and multiple devices
  - Thermal foldback
  - Power foldback
- Liquid detection and corrosion mitigation

2 Applications

- Automotive USB charging
- Automotive media hub
- Automotive head unit
- Automotive display module

3 Description

The TPS26744E-Q1 is a stand-alone dual-port USB Type-C and Power Delivery (PD) source controller for any automotive USB-C port application including extended power range (EPR) voltages. The TPS26744E-Q1 supports all USB-PD power negotiation options (fixed supply, programmable power supply (PPS), and adjustable power supply (AVS)) for standard power range (SPR) and EPR. The TPS26744E-Q1 automatically identifies USB-C cable capabilities, and adjusts for the maximum current allowed by the cable, without requiring an external 5V supply for VCONN. The TPS26744E-Q1 supports DisplayPort over USB-C and legacy D+/D- charging.

The TPS26744E-Q1 controls a DC/DC via I^2C or PWM to achieve a complete USB-C PD solution. The TPS26744E-Q1 has SYNC outputs to keep external DC/DC switching out-of-phase for each port, with dual-random spread-spectrum (DRSS).

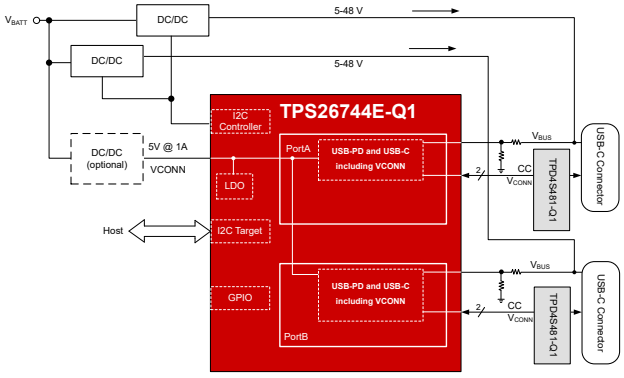
The TPS26744E-Q1 has integrated protections for thermal and input voltage monitoring for power foldback, VBUS high/low monitoring, and liquid detection along with corrosion mitigation.

The TPS26744E-Q1 also supports USB-C Alternate Modes such as DisplayPort. The TPS26744E-Q1 offers multiple interface options for the system including I^2C and LIN support, along with GPIOs that can be configured for various functions.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS26744E-Q1	32-QFN (RHB)	5.0mm x 5.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Device Comparison

Table 4-1. Device Comparison

Device	Number of Ports	EPR Support	DisplayPort Support	AEC Q100
TPS26744E-Q1	2	Yes	Yes	Yes
TPS26742E-Q1	2	Yes	No	Yes
TPS26742-Q1	2	No	No	Yes
TPS26743E-Q1	1	Yes	Yes	Yes
TPS26741-Q1	1	No	No	Yes
TPS26741E-Q1	1	Yes	No	Yes
TPS26742E	2	Yes	No	No

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5 Pin Configuration and Functions

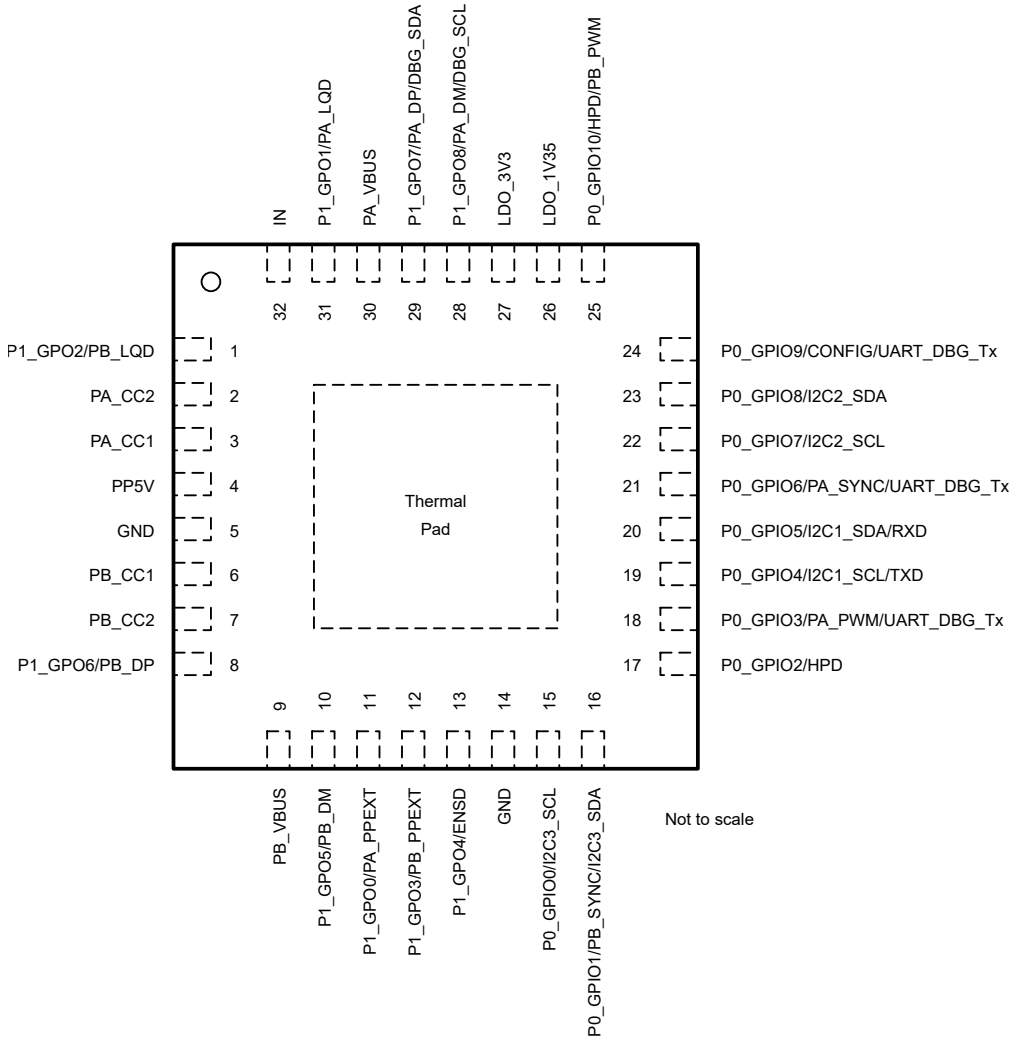

Figure 5-1. TPS26744E-Q1RHB Package, 32-Pin QFN (Top View)

Table 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
GND	5,14	GND	Ground reference pin. Ties to underside power pad.
IN	32	P	This is the input power supply for the device.
LDO_1V35	26	P	Output of internal LDO. Bypass with capacitance C_{LDO_1V35} to GND. This is not intended to source external circuits.

Table 5-1. Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
LDO_3V3	27	P	Output of internal LDO. Bypass with capacitance C_{LDO_3V3} to GND.
P0_GPIO0/I2C3_SCL	15	I/O	This pin supports multiple functions: General Purpose I/O, or SCL for I2C3.
P0_GPIO1/PB_SYNC/I2C3_SDA	16	I/O	This pin supports multiple functions: General Purpose I/O, SYNC output for PortB, or SDA for I2C3.
P0_GPIO2/HPD	17	I/O	This pin supports multiple functions: General Purpose I/O, or hot-plug detect (HPD).
P0_GPIO3/PA_PWM/UART_DBG_Tx	18	I/O	This pin supports multiple functions: General purpose I/O, PWM output, or UART debug output.
P0_GPIO4/I2C1_SCL/TXD	19	I/O	This pin supports multiple functions: General purpose I/O, SCL for the I2C1, or a LIN bus transmitter.
P0_GPIO5/I2C1_SDA/RXD	20	I/O	This pin supports multiple functions: General purpose I/O, SDA for I2C1, or a LIN bus receiver.
P0_GPIO6/PA_SYNC/UART_DBG_Tx	21	I/O	This pin supports multiple functions: General purpose I/O, SYNC output for PortA, or a debug output.
P0_GPIO7/I2C2_SCL	22	I/O	This pin supports multiple functions: General purpose I/O, or SCL for I2C2.
P0_GPIO8/I2C2_SDA	23	I/O	This pin supports multiple functions: General purpose I/O, SDA for I2C2.
P0_GPIO9/CONFIG/UART_DBG_Tx	24	I/O	This pin supports multiple functions: General purpose I/O, configuration input, or debug output.
P0_GPIO10/HPD/PB_PWM	25	I/O	This pin supports multiple functions: General purpose I/O, hot-plug-detect (HPD), or PWM output.
P1_GPO0/PA_PPEXT/ADCIN2	11	I/O	This pin supports multiple functions: General Purpose Output, ADC input, or external power path control for port A.
P1_GPO1/PA_LQD/ADCIN3	31	I/O	This pin supports multiple functions: General Purpose Output, an ADC input, or liquid detection on Port A.
P1_GPO2/PB_LQD/ADCIN4	1	I/O	This pin supports multiple functions: General Purpose Output, ADC input or liquid detection on Port B.
P1_GPO3/PB_PPEXT/ADCIN5	12	I/O	This pin supports multiple functions: General Purpose Output, ADC input, or external power path control for port B.
P1_GPO4/ENSD	13	I/O	This pin supports multiple functions: General Purpose Output, or enable shutdown mode input (ENSD). Do not pull this pin down externally unless enabling shutdown mode.
P1_GPO5/PB_DM/ADCIN15	10	I/O	This pin supports multiple functions: General Purpose Output, ADC input, or connect to the D- pin on Port B for BC1.2.
P1_GPO6/PB_DP/ADCIN14	8	I/O	This pin supports multiple functions: General Purpose Output, ADC input, or connect to the D+ pin on Port B for BC1.2.
P1_GPO7/PA_DP/DBG_SDA/ADCIN12	29	I/O	This pin supports multiple functions: General Purpose Output, ADC input, connect to the D+ pin on Port A for BC1.2, or the SDA connection to I2C4.
P1_GPO8/PA_DM/DBG_SCL/ADCIN13	28	I/O	This pin supports multiple functions: General Purpose Output, ADC input, connect to the D- pin on Port A for BC1.2, or the SCL connection to I2C4.
PA_CC1	3	I/O	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{Px_CCy}).
PA_CC2	2	I/O	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{Px_CCy}).
PA_VBUS	30	P	VBUS sense input for Port A. Bypass with capacitance C_{Px_VBUS} to GND.
PB_CC1	6	I/O	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{Px_CCy}).

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Table 5-1. Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
PB_CC2	7	I/O	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{Px_CCy}).
PB_VBUS	9	P	VBUS sense input for Port B. Bypass with capacitance C_{Px_VBUS} to GND.
PP5V	4	P	Input supply for VCONN and output of LDO from the IN pin. Bypass with capacitance C_{PP5V} to GND.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range (2)	PP5V	–0.3	7.0	V
	IN	–0.3	40	
	Px_VBUS	–0.3	40	V
	Px_DP, Px_DM, Px_LQD	–0.3	24	
	Px_CC1, Px_CC2	–0.5	24	
	P0_GPIOx	–0.3	V_{LDO_3V3} + 0.3 (4.1 MAX)	
	P1_GPO3, P1_GPO4	–0.3	6	
	P1_GPO0	–0.3	V_{LDO_3V3} + 0.3 (4.1 MAX)	
	I2Cx_SDA, I2Cx_SCL	–0.3	4	
Output voltage range (2)	LDO_1V35(3) (4)	–0.3	2	V
	LDO_3V3(3)	–0.3	4	
Source current	Positive source current on Px_CCy		Internally limited	A
	Current sunk or sourced by Px_GPIOy		0.005	
	Positive sink current for I2Cn_SDA, I2Cn_SCL		Internally limited	
	Positive source current for LDO_3V3, LDO_1V35		Internally limited	
T_J Operating junction temperature		–40	155	°C
T_{STG} Storage temperature		–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(3) Do not apply voltage to these pins.
(4) Do not apply any external load to this pin.

6.2 ESD Ratings

PARAMETER		TEST CONDITIONS		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except Px_CCy	±2000	V
			Pins Px_CCy	±6000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	Corner pins	±750	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	Non-Corner pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_I	Input voltage range (1)	IN (when used as Px_VCONN supply)	5	12	32	V
		IN(2)	4.5	12	32	
		PP5V (if supplied externally)	4.75	5	min(5.5, V_{IN})	
		Px_VBUS	0		31	
V_{IO}	I/O voltage range (1)	I2Cx_SDA, I2Cx_SCL	0		V_{LDO_3V3}	V
		P0_GPIOx	0		V_{LDO_3V3}	
		P1_GPO0, P1_GPO3, P1_GPO4	0		V_{LDO_3V3}	
		Px_CC1, Px_CC2	0		5.5	
		Px_DP, Px_DM, Px_LQD	0		5.5	
I_O	Output current (from PP5V)	Px_CC1, Px_CC2			350	mA
I_O	Output current (from LDO_3V3)	P0_GPIOx, P1_GPOx			1	mA
I_O	Output current (from internal LDO)	Sum of current from LDO_3V3 and P0_GPIOx and P1_GPOx.			5	mA
T_A	Ambient operating temperature		–40		105	°C
T_J	Operating junction temperature		–40		125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(2) When the device first powers up, $V_{ENSD} > V_{ENSD\_THLD}$ (rising) is required.

6.4 Thermal Information (RHB 5x5)

THERMAL METRIC(1)		DEVICE QFN (RHB) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance	21.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.5	°C/W
$R_{\theta JC}$ (bottom)	Junction-to-case (bottom GND pad) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{Px_VBUS}	Capacitance on Px_VBUS	50 V	1	4.7	10	µF
C_{IN}	Capacitance on IN		0.5	1		µF
C_{LDO_3V3}	Capacitance on LDO_3V3	6.3 V	2	4.7		µF
C_{LDO_1V35}	Capacitance on LDO_1V35			470		nF

6.5 Recommended Capacitance (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{PP5V}	Capacitance on PP5V, I_{LIMVC} = DisplayPort setting	10 V	25			µF
	Capacitance on PP5V, I_{LIMVC} = eMarker setting	10 V	5			
C_{PP5V2} [2]	Second capacitance on PP5V pin	10 V		100		nF
C_{Px_CCy}	Capacitance on Px_CCy pins			300		pF
C_{DPDM}	Capacitance on Px_DP and Px_DM when used in DCP mode	50V			1	nF

(1) Capacitance values do not include any derating or tolerance factors. For example, if 4.5 µF is required and the external capacitor value diminishes by 50% due to derating at the required operating voltage and has -10% tolerance, then the required external capacitor nominal value must be 10 µF.
(2) Placing this capacitor will improve ESD performance.

6.6 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN_LKG}	Leakage on the IN pin when 5V LDO disabled (PP5V supplied externally).	V_{PP5V} = 5V, 18V>V_{IN}>7V, 0ºC ≤ T_J ≤ 85ºC			30	µA
Outputs						
V_{PP5V}	Voltage on PP5V when sourced by the internal LDO	7V ≤ V_{IN} ≤ 18 V, V_{EN} = 2 V, Px_VCONN enabled.	4.5	4.63	4.75	V
V_{PP5V}	Voltage on PP5V when sourced by the internal LDO	4.5V ≤ V_{IN} < 7V, V_{EN} = 2 V, Px_VCONN disabled.	4.2	4.63	4.75	V
V_{LDO_3V3}	Voltage on LDO_3V3	V_{PP5V} > V_{PP5V_UVLO}	3.0	3.3	3.45	V
V_{LDO_1V35}	Output voltage of LDO_1V35	V_{LDO_3V3} ≥ 3.0V, up to maximum internal loading condition.		1.35		V

6.7 Power Consumption Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Active Mode						
$I_{IN,Act}$ [1]	current into IN	Active mode while erasing flash: V_{PP5V}=5.0V, V_{IN}=7V, this does include IDD_{ERASE}.			22	mA
	current into IN	Active mode while programming flash: V_{PP5V}=5.0V, V_{IN}=7V, this does include IDD_{PGM}.			22	mA
	current into IN	Active mode: V_{PP5V}=5.0V, V_{IN}=7V, this does not include IDD_{ERASE} or IDD_{PGM}.			15	mA
Sleep Mode						
$I_{IN,Sleep}$ [1]	current into IN	V_{IN}=12V, T_J = 25 ºC		2		mA
Idle Mode						
$I_{IN,Idle}$ [1]	current into IN	V_{IN}=12V		1.3		mA
Shutdown Mode						
$I_{IN,SD}$	Shutdown current into IN	V_{IN}=12V, V_{ENSD}=0V		1		mA

(1) Typical numbers are averaged over 1 second.

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6.8 Power Path Supervisory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overvoltage						
V_{PP5V_OVP}	VBUS over voltage (rising)	OVP detected when V_{Px_CCy} > V_{PP5V_OVP}, and VCONN being sourced through Px_CCy	5.85	6.15	6.55	V
	VBUS over voltage (falling)		5.4	5.7	6.0	
	VBUS over voltage (hysteresis)			0.45		
Undervoltage						
V_{PP5V_UVLO}	Voltage required on PP5V	Rising	3.9	4.1	4.3	V
		Falling	3.8	4.0	4.2	
		Hysteresis		0.1		
V_{VBUS_GOOD}	Comparator for Px_VBUS	Rising		3.75		V
		Falling		3.65		
		Hysteresis		0.10		
VBUS Discharge						
I_{DSCH}	VBUS discharge current (1)	30V ≥ V_{Px_VBUS} ≥ V_{LDO_3V3} , measure I_{Px_VBUS}		8		mA

(1) The discharge is enabled automatically when needed to meet USB specifications and disabled automatically when not needed.

6.9 CC Cable Detection Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Source (Rp pull-up)						
V_{SRC1}	Detach threshold for Rp3.0A applied to Px_CCy	Rising	2.56		2.74	V
		Falling	2.46		2.64	
		Hysteresis		0.1		
V_{SRC2}	Detach threshold for Rp1.5A or RpDef applied to Px_CCy	Rising	1.54		1.64	V
		Falling	1.51		1.61	
		Hysteresis		0.03		
V_{SRC3}	Ra/Rd detection threshold for RpDef applied to Px_CCy	Rising	0.20		0.24	V
		Falling	0.16	0.18	0.20	
		Hysteresis		0.04		
V_{SRC4}	Ra/Rd detection threshold for Rp1.5A applied to Px_CCy	Rising	0.39		0.44	V
		Falling	0.35		0.40	
		Hysteresis		0.04		
V_{SRC5}	Ra/Rd detection threshold for Rp3.0A applied to Px_CCy	Rising	0.79		0.84	V
		Falling	0.75		0.80	
		Hysteresis		0.04		
V_{OC}	Px_CCy open circuit voltage while Rp enabled, no load	V_{PP5V_UVLO} < V_{PP5V} < 5.5 V, R_{CC} = 47 kΩ	2.95			V
I_{RpDef}	Current source - USB Default	V_{PP5V} ≥ 4.5V, 0 < V_{Px_CCy} < 1.5 V, measure I_{Px_CCy}	73	80	87	µA
$I_{Rp1.5}$	Current source - 1.5A	V_{PP5V} ≥ 4.5V, 0 < V_{Px_CCy} < 1.5 V, measure I_{Px_CCy}	166	180	194	µA
$I_{Rp3.0}$	Current source - 3.0A	V_{PP5V} ≥ 4.5V, 0 < V_{Px_CCy} < 2.45 V, measure I_{Px_CCy}	304	330	356	µA
Type-C Sink (Rd pull-down)						

6.9 CC Cable Detection Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SNK1}	Open/Default detection threshold when Rd applied to Px_CCy	Rising	0.2		0.24	V
	Open/Default detection threshold when Rd applied to Px_CCy	Falling	0.16		0.20	
		Hysteresis		0.04		
V_{SNK2}	Default/1.5A detection threshold	Falling	0.62		0.68	V
	Default/1.5A detection threshold	Rising	0.63	0.66	0.69	
		Hysteresis		0.01		
V_{SNK3}	1.5A/3.0A detection threshold when Rd applied to Px_CCy	Falling	1.17		1.25	V
	1.5A/3.0A detection threshold when Rd applied to Px_CCy	Rising	1.22		1.3	
		Hysteresis		0.05		
R_{SNK}	Rd pulldown resistance	0.25 V ≤ V_{Px_CCy} ≤ 2.1 V, measure resistance on Px_CCy	4.6		5.6	kΩ
R_{VCONN_DIS}	VCONN discharge resistance	0V ≤ V_{Px_CCy} ≤ 5.5 V, measure resistance on Px_CCy	4.1		6.1	kΩ
Z_{Open}	Unpowered CC impedance	V_{IN}=0V, V_{Px_CCy} = 3.3V	126			kΩ
R_{Open}	Resistance from Px_CCy to GND when configured as open.	V_{Px_VBUS} = 0, V_{IN}=V_{PP5V}=5.0V, V_{Px_CCy}=5 V, measure resistance on Px_CCy	126			kΩ
Common (Source and Sink)						
R_a	Ra pulldown resistance	V_{Px_CCy} ≤ 0.25 V, measure resistance on Px_CCy, the minimum value is flexible in order to avoid needing any trim.			1200	Ω
t_{CC}	Default deglitch time for comparators on Px_CCy			3.6		ms

6.10 Px_VCONN Switch Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{VCONN}	Rdson of the VCONN path	V_{PP5V}=5V, I_{Px_CCy} = 350 mA, measure resistance from PP5V to Px_CCy		0.7		Ω
I_{LIMVC}	Short circuit current limit	eMarker-only setting, V_{PP5V}=5V, R_L=10mΩ , measure I_{Px_CCy}		50		mA
I_{LIMVC}	Short circuit current limit	V_{PP5V}=5V, R_L=10mΩ , measure I_{Px_CCy},		450		mA
V_{VCONN_RCP}	Reverse current protection threshold for Px_VCONN, sourcing VCONN through Px_CCy	V_{PP5V} ≥ 4.9 V, V_{Px_CCz} = V_{PP5V}, V_{Px_CCy} rising		200		mV
	Reverse current protection threshold for Px_VCONN, sourcing VCONN through CCx	V_{PP5V} ≥ 4.9 V, V_{Px_CCz} ≤ 4.0V, V_{Px_CCy} rising		340		
t_{VCILIM}	Current clamp flag deglitch time. If the overcurrent persists for longer than this the switch is disabled.			3		ms

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6.10 Px_VCONN Switch Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{VC_OVP}	Response time to V_{Px_CCy} > V_{PP5V_OVP}, while VCONN is sourced through Px_CCy	Enable Px_VCONN, apply 100 Ω load on PP5V, ramp V_{Px_CCy} up starting from 4.3V at 100 V/ms		150		µs
t_{VC_UVLO}	Response time to V_{PP5V} < V_{PP5V_UVLO}	R_L = 100 Ω, no external capacitance on Px_CCy, ramp V_{PP5V} from 5.5V to 3.5V at 10V/µs, measure time from UVLO detection until current < 10mA		4		µs
t_{VC_RCP}	Response time to V_{PP5V} < V_{Px_CCy}+V_{VCONN_RCP}	V_{PP5V}=5.5V, enable Px_VCONN, ramp V_{Px_CCy} from 4V to 21.5V at 10 V/µs		1		µs
t_{VCON}	From enable signal to Px_CCy at 90% of final value	I_L = 250 mA, V_{PP5V} = 5V, C_L=0		0.98		ms
t_{VCOFF}	From disable signal to Px_CCy at 10% of final value	I_L = 250 mA, V_{PP5V} = 5V, C_L=0		0.22		ms
t_{VCRISE}	Px_CCy from 10% to 90% of final value	I_L = 250 mA, V_{PP5V} = 5V, C_L=0		270		µs
t_{VCFALL}	Px_CCy from 90% to 10% of initial value	I_L = 250 mA, V_{PP5V} = 5V, C_L=0		250		µs
t_{iOS_VCONN}	Response time to short circuit	V_{PP5V}=5V, for short circuit R_L = 10mΩ. Measure time from short being applied until I_{VCONN} < I_{LIMVC}.			4.0	µs
		V_{PP5V}=5V, for short circuit R_L = 10mΩ. Measure time from short being applied until I_{VCONN} < I_{LIMVC}. eMarker-only setting.		0.6		

6.11 CC PHY Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
V_{TXHI}	Transmit high voltage on Px_CCy	Standard External load	1.05	1.125	1.2	V
V_{TXLO}	Transmit low voltage on Px_CCy	Standard External load	–75		75	mV
Z_{DRIVER}	Transmit output impedance while driving the CC line using Px_CCy		33	50	71.4	Ω
t_{TX_RISE}	Rise time. 10 % to 90 % amplitude points on Px_CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{Px_CCy}= 520 pF	300			ns
t_{TX_FALL}	Fall time. 90 % to 10 % amplitude points on Px_CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{Px_CCy}= 520 pF	300			ns
t_{UI}	Unit interval for data bit during transmission on Px_CCy		3.03		3.7	µs
Receiver						
C_{CC}	Receiver capacitance on Px_CCy(2)	Capacitance looking into the CC pin when in receiver mode			100	pF

6.11 CC PHY Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
tRxFilter (1)	Rx bandwidth limiting filter. Time constant of a single pole filter to limit broadband noise ingression		100			ns
V_{RX_SRC}	Threshold on Px_CCy for receiver comparator	Source mode (rising)	775	825	875	mV
		Source mode (falling)	500	550	600	
V_{RX_SNK}	Threshold on Px_CCy for receiver comparator	Sink mode (rising)	530	575	620	mV
		Sink mode (falling)	260	300	340	

(1) Broadband noise ingression is due to coupling in the cable interconnect.
(2) C_{CC} includes only the internal capacitance on a Px_CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding C_{Px_CCy} externally.

6.12 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD}	Temperature shutdown threshold	Temperature rising	140	158.5	175	°C
		Temperature falling	125	143.5	162	°C
		Hysteresis		15		°C
T_{SD_PP}	Temperature controlled shutdown threshold for each power path of the port.	Temperature rising	125	145	165	°C
		Temperature falling	110	130	150	°C
		Hysteresis		15		°C

6.13 Oscillator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC_24M}	24MHz oscillator		22.8	24	25.2	MHz

6.14 ADC Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	Least significant bit	3.6V max scaling, voltage divider of 3		3.52		mV
		6.0V max scaling, voltage divider of 5		5.86		mV
		51.2V max scaling, voltage divider of 42.7		50		mV
		See (1)		0.45		°C
GAIN_ERR	Gain error (including the input divider)	$0.05V \le V_{GPIOx} \le V_{LDO\_3V3}$	–2.7		2.7	%
		$2.7V \le V_{LDO\_3V3} \le 3.6V$	–2.4		2.4	
		$85^oC \le T_J \le 125^oC$	–12		12	
		$0.15V \le V_{Px\_CCy} \le 5.5V$	–3		3	
		$7V \le V_{IN} \le 31V$	–2.1		2.1	
		$0.6V \le V_{Px\_VBUS} \le 31V$	–2.1		2.1	

ADVANCE INFORMATION

6.14 ADC Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOS_ERR	Offset error (referred to the input pin)	$0.05V \le V_{GPIOx} \le V_{LDO\_3V3}$	–12.3		12.3	mV
		$2.7V \le V_{LDO\_3V3} \le 3.6V$	–12.3		12.3	mV
		$85^oC \le T_J \le 125^oC$	–2		2	°C
		$0.15V \le V_{Px\_CCy} \le 5.5V$	–20.5		20.5	mV
		$7V \le V_{IN} \le 31V$	–175		175	mV
		$0.6V \le V_{Px\_VBUS} \le 31V$	–175		175	mV

(1) Temperature in degC = (ADC data - 650)*0.45 + 25

6.15 Liquid Detection Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LQD}	Weak pullup on Px_LQD	$V_{PP5V} \ge 4.5V$, $0 < V_{Px\_LQD} < 2.0$ V, measure I_{Px_LQD}		40		µA
	Strong pullup on Px_LQD	$V_{PP5V} \ge 4.5V$, $0 < V_{Px\_LQD} < 2.0$ V, measure I_{Px_LQD}		80		
	Strong pullup on Px_LQD	$V_{PP5V} \ge 4.5V$, $0 < V_{Px\_LQD} < 2.0$ V, measure I_{Px_LQD}		160		

ADVANCE INFORMATION

6.15 Liquid Detection Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LQD}	Threshold on Px_LQD comparator (Rising)	setting 0		0.200		V
		setting 1		0.225		
		setting 2		0.250		
		setting 3		0.275		
		setting 4		0.300		
		setting 5		0.325		
		setting 6		0.350		
		setting 7		0.500		
		setting 8		0.700		
		setting 9		0.800		
		setting 10		0.850		
		setting 11		0.900		
		setting 12		0.950		
		setting 13		1.000		
		setting 14		1.050		
		setting 15		1.100		
		setting 16		1.150		
		setting 17		1.200		
		setting 18		1.250		
		setting 19		1.300		
		setting 20		1.350		
		setting 21		1.400		
		setting 22		1.450		
		setting 23		1.500		
		setting 24		1.550		
		setting 25		1.600		
		setting 26		1.650		
		setting 27		1.700		
		setting 28		1.750		
		setting 29		1.800		
		setting 30		1.850		
		setting 31		1.900		
V_{LQD_OVP}	OVP threshold on Px_LQD	Rising	6		9.5	V
V_{Px_LQD}	Px_LQD voltage when R_{LQD} and I_{LQD} applied	R_{LQD}=5kΩ, I_{LQD}=80µA		0.4		V
		R_{LQD}=10kΩ, I_{LQD}=40µA		0.4		
		R_{LQD}=12.5kΩ, I_{LQD}=160µA		2.0		
		R_{LQD}=25kΩ, I_{LQD}=80µA		2.0		
R_{LQD}	Weak pulldown on Px_LQD	V_{Px_LQD}=0.4V, I_{LQD}=80µA		5		kΩ
		V_{Px_LQD}=0.4V, I_{LQD}=40µA		10		
		V_{Px_LQD}=2.0V, I_{LQD}=160µA		12.5		
		V_{Px_LQD}=2.0V, I_{LQD}=80µA		25		

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6.16 Input/Output (I/O) Characteristics (P0_GPIOx)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input						
GPIO_VIH	P0_GPIOx high-Level input voltage, configured for V_{IO}=3.3V	V_{LDO_3V3} = 3.3V, 0.7*V_{IO}	2.31			V
GPIO_VIL	P0_GPIOx low-Level input voltage, configured for V_{IO}=3.3V	V_{LDO_3V3} = 3.3V, 0.3*V_{IO}			0.99	V
GPIO_HYS	P0_GPIOx input hysteresis voltage, configured for V_{IO}=3.3V	V_{LDO_3V3} = 3.3V, 0.05*V_{IO}		0.15		V
GPIO_ILKG	P0_GPIOx leakage current	V_{GPIOx}=V_{LDO_3V3}=3.3V, T_J≤85ºC	–2	–0.85	1	µA
Output						
GPIO_RPU	P0_GPIOx internal pull-up	Pull-up enabled		40		kΩ
GPIO_RPD	P0_GPIOx internal pull-down	Pull-down enabled		40		kΩ
GPIO_VOH	Output high voltage for P0_GPIOx	V_{LDO_3V3} = 3.3V, I_{GPIOx}=2mA	2.64			V
GPIO_VOL	Output low voltage for P0_GPIOx	V_{LDO_3V3} = 3.3V, I_{GPIOx}=2mA			0.4	V

6.17 Input/Output (I/O) Characteristics (P1_GPOx)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO_ILKG	GPIOx leakage current, GPIO_RPU and GPIO_RPD disabled	V_{GPIOx} = V_{LDO_3V3}	–1		1	µA
		V_{GPIOx} = 5.5 V, V_{LDO_3V3} = 3.3V (only applies to x=1, 2, and 5-8)	–1		1	
Output						
GPIO_RPU	GPIOx internal pull-up	Pull-up enabled		100		kΩ
GPIO_RPD	GPIOx internal pull-down	Pull-down enabled		100		kΩ
GPIO_VOH	GPIOx output high voltage	V_{LDO_3V3} = 3.3V, I_{P1_GPOx}= -2mA	2.9			V
GPIO_VOL	GPIOx output low voltage	V_{LDO_3V3} = 3.3V, I_{P1_GPOx}=2mA			0.4	V
Alternate functions						
V_{ENSD_THLD}	Input threshold for the ENSD functionality	rising		0.66		V
		falling		0.56		
		hysteresis		0.1		
T_{ENSD_DEG}	Deglitch time for ENSD input	V_{ENSD} < V_{ENSD_THLD} constantly for this time for ENSD to be deemed low			300	µs

6.18 I2C Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA and SCL Common Characteristics (Controller, Target)						
I_{OL}	Max output low current	V_{OL}=0.4 V	10	17.3		mA
I_{OL}	Max output low current	V_{OL}=0.6 V	15	23.6		mA
t_f	Fall time from 0.7*V_{IO} to 0.3*V_{IO}	C_b = 10 pF, Rp=14kΩ	0.3		120	ns
		C_b = 400 pF, Rp=330Ω	12		120	ns
t_{SP}	I2C pulse width suppressed				50	ns
C_I	Pin capacitance (internal)				10	pF

6.18 I2C Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_b	Capacitive load for each bus line (external)				400	pF
SDA and SCL Standard Mode Characteristics (Target)						
f_{SCL}	Clock frequency				100	kHz
$t_{VD;DAT}$	Valid data time	Transmitting Data, SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data, ACK signal from SCL low to SDA (out) low			3.45	µs
SDA and SCL Fast Mode Characteristics (Target)						
f_{SCL}	Clock frequency		100		400	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, ACK signal from SCL low to SDA (out) low			0.9	µs
SDA and SCL Fast Mode Plus Characteristics (Target)						
f_{SCL}	Clock frequency		400		1000	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, SCL low to SDA output valid			0.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, ACK signal from SCL low to SDA (out) low			0.45	µs
SDA and SCL Standard Mode Characteristics (Controller)						
f_{SCL}	Clock frequency for controller(1)			90		kHz
$t_{HD;STA}$	Start or repeated start condition hold time		4			µs
$t_{HD;DAT}$	Serial data hold time (Controller mode)		0	7.7		ns
t_{LOW}	Clock low time		4.7			µs
t_{HIGH}	Clock high time		4			µs
$t_{SU;STA}$	Start or repeated start condition setup time		4.7			µs
$t_{SU;DAT}$	Serial data setup time	Transmitting	250			ns
$t_{SU;STO}$	Stop condition setup time		4			µs
t_{BUF}	Bus free time between stop and start		4.7			µs
$t_{VD;DAT}$	Valid data time	Transmitting data, SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, ACK signal from SCL low to SDA (out) low			3.45	µs
SDA and SCL Fast Mode Characteristics (Controller)						
f_{SCL}	Clock frequency for controller (1)			325		kHz
$t_{HD;STA}$	Start or repeated start condition hold time		0.6			µs
$t_{HD;DAT}$	Serial data hold time (Controller mode)		0	3.9		ns
t_{LOW}	Clock low time		1.3			µs
t_{HIGH}	Clock high time		0.6			µs
$t_{SU;STA}$	Start or repeated start condition setup time		0.6			µs
$t_{SU;DAT}$	Serial data setup time	Transmitting	100			ns

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6.18 I2C Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU;STO}$	Stop condition setup time		0.6			µs
t_{BUF}	Bus free time between stop and start		1.3			µs
$t_{VD;DAT}$	Valid data time	Transmitting data, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, ACK signal from SCL low to SDA (out) low			0.9	µs
SDA and SCL Fast Mode Plus Characteristics (Controller)						
f_{SCL}	Clock frequency for controller (1)			708		kHz
$t_{HD;STA}$	Start or repeated start condition hold time		0.26			µs
$t_{HD;DAT}$	Serial data hold time (Controller mode)		0	3.2		ns
t_{LOW}	Clock low time		0.5			µs
t_{HIGH}	Clock high time		0.26			µs
$t_{SU;STA}$	Start or repeated start condition setup time		0.26			µs
$t_{SU;DAT}$	Serial data setup time	Transmitting	50			ns
$t_{SU;STO}$	Stop condition setup time		0.26			µs
t_{BUF}	Bus free time between stop and start		0.5			µs
$t_{VD;DAT}$	Valid data time	Transmitting data, SCL low to SDA output valid			0.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, ACK signal from SCL low to SDA (out) low			0.45	µs

(1) Actual frequency is dependent upon bus capacitance.

6.19 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				12	MHz

6.20 SYNC output

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYNC_NOM}	Nominal frequency of Px_SYNC output		0.1		2.2	MHz
N_{SYNC_NOM}	Configurable nominal SYNC frequency: $f_{SYNC\_NOM} = f_{OSC\_24M} / N_{SYNC\_NOM}$.		1		255	
f_{SYNC_SWING}	Frequency swing of Px_SYNC output		-10		10	%
N_{MOD}	Configurable modulation frequency: $f_{MOD} = 6000/N_{MOD}$.		461		666	
f_{MOD}	Modulation frequency of Px_SYNC output.		9		13	kHz

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6.21 PWM Timer

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N_{PWM}	Maximum number of bits in the PWM counter			13		Bits
T_{PWM_ON}	ON time of the PWM cycle		0		0.341	ms
T_{PWM_TOTAL}	Period of the PWM cycle		0		0.341	ms
T_{PWM_PERIOD}	Configurable period for PWM duty-cycle to automatically transition from 100% to 0% and back to 100%.		0.082		2.6	s

6.22 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Size						
	Flash size (per bank)			144		kB
	Number of banks			1		
Supply						
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
$NWEC_{(UPPER)}$	Erase/program cycle endurance (remaining flash)	-40°C ≤ T_J ≤ 105°C	10			k cycles
$NW_{(MAX)}$	Write operations per word line before sector erase (1)				83	write operations
Retention						
t_{RET_105}	Flash memory data retention	-40°C ≤ T_J ≤ 105°C	11.4			years

(1) This parameter specifies the maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.

6.23 Boot Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BOOT}	Time from LDO_3V3 going high until firmware enters 'APP' mode			1.5		s
t_{TFU}	Time required to update the FW image via I2C	f_{SCL} = 1MHz, using I2C1 or I2C4		13		s
		f_{SCL} = 400kHz, using I2C1 or I2C4		14		
		f_{SCL} = 100kHz, using I2C1 or I2C4		27		

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6.24 Typical Characteristics

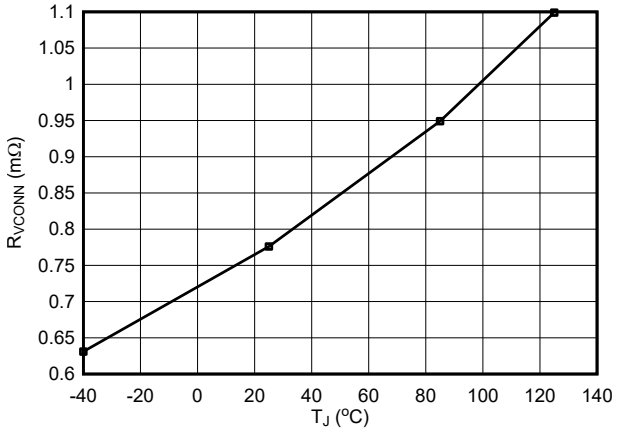

Figure 6-1. VCONN switch resistance

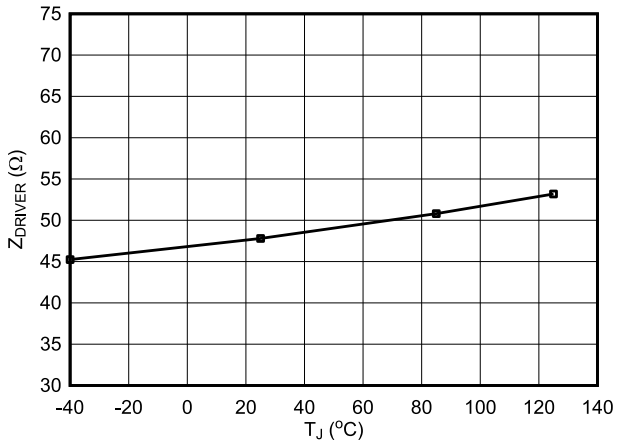

Figure 6-2. USB-PD PHY transmit impedance

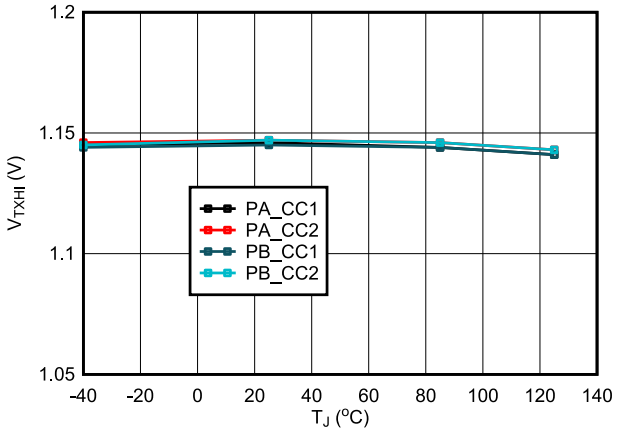

Figure 6-3. USB-PD PHY transmit high voltage

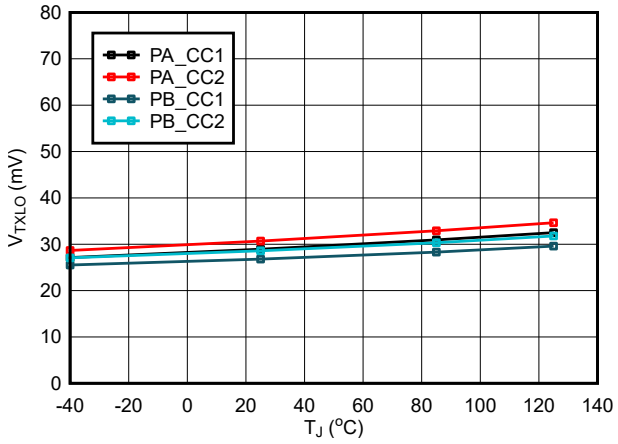

Figure 6-4. USB-PD PHY transmit low voltage

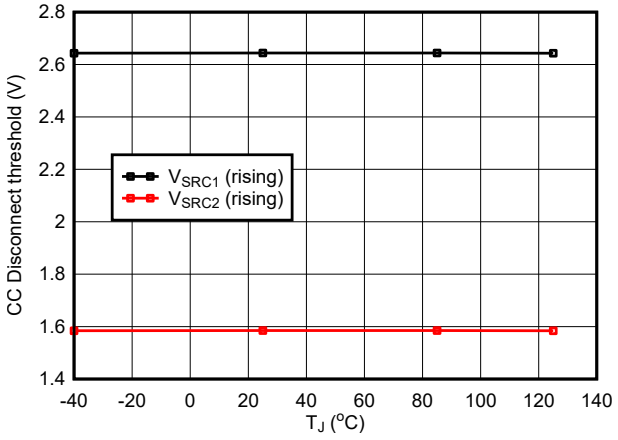

Figure 6-5. Disconnect voltage thresholds on Px_CCy pins

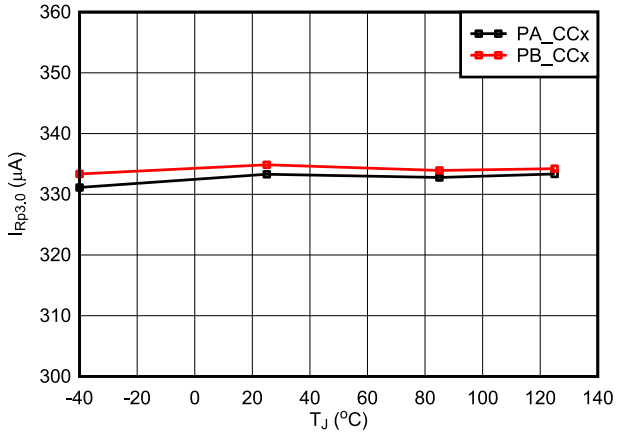

Figure 6-6. Strength of cable detect current source advertising 3A

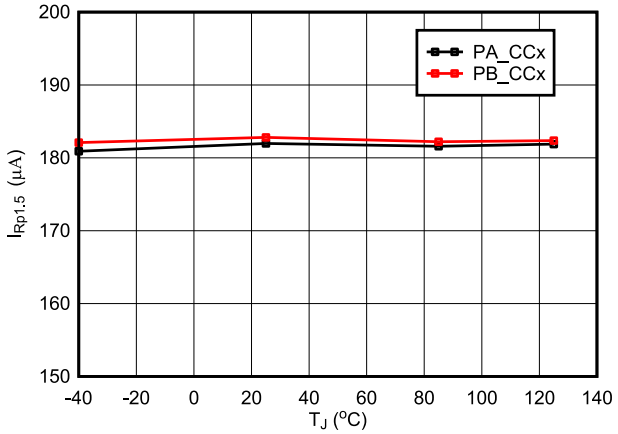

Figure 6-7. Strength of cable detect current source advertising 1.5A

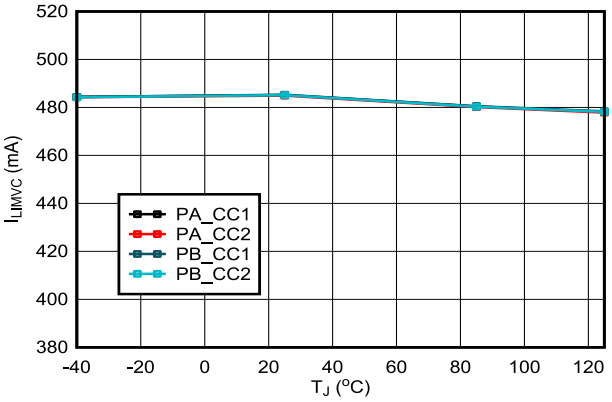

Figure 6-8. Current limit for VCONN switch.

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7 Parameter Measurement Information

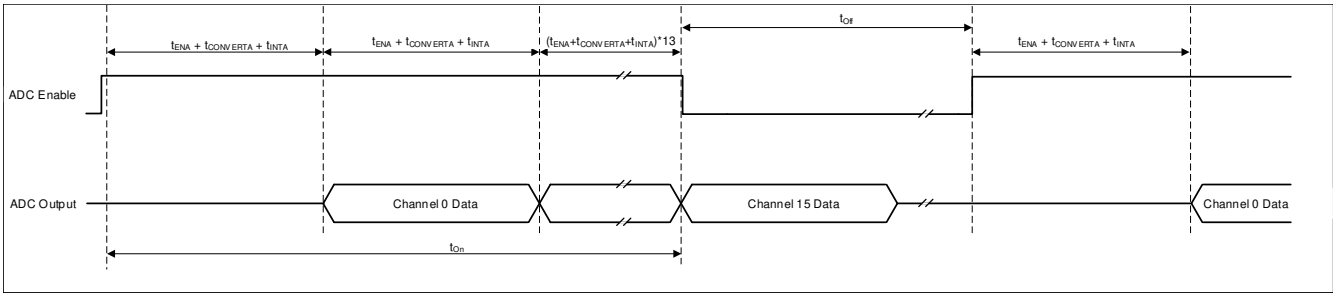


Figure 7-1. ADC Round Robin Conversion Timing

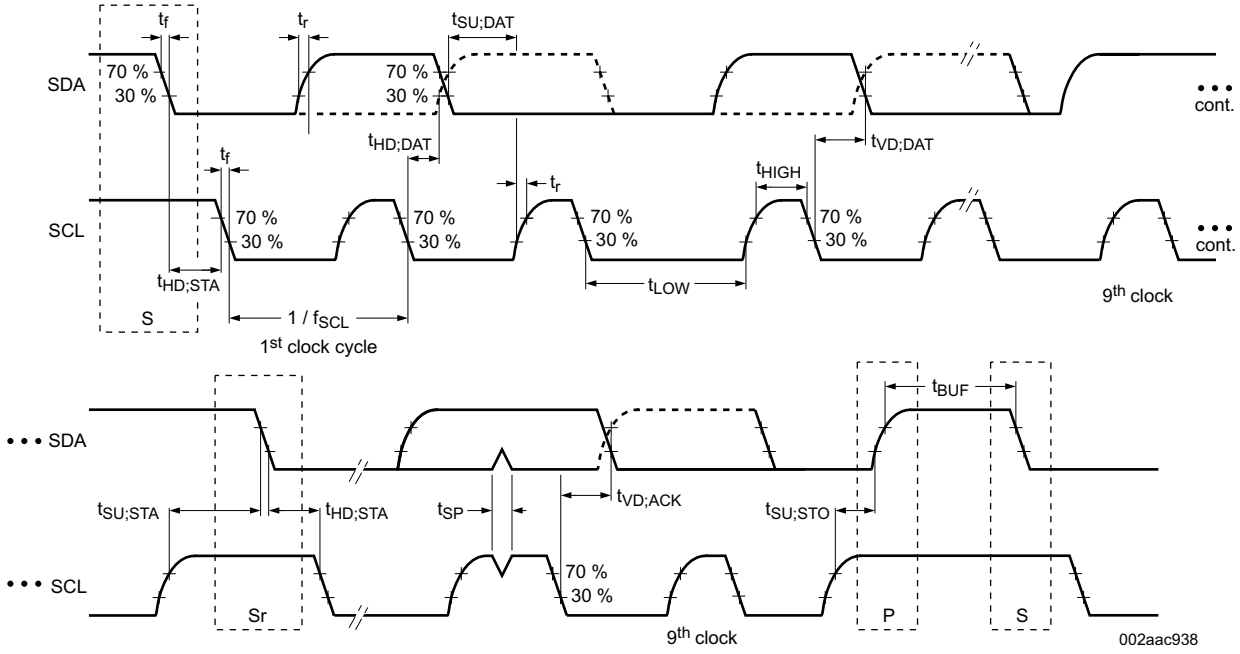


Figure 7-2. I²C Target Interface Timing

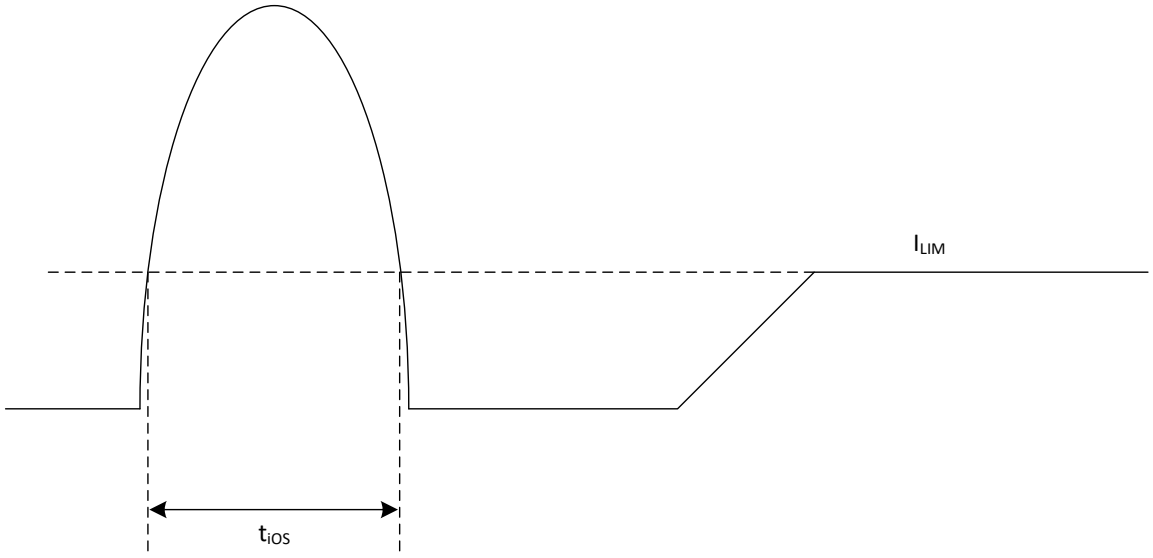


Figure 7-3. Short-Circuit Response Time for Internal Power Paths

8 Detailed Description

8.1 Overview

The TPS26744E-Q1 is a fully-integrated USB Type-C Source Power Delivery (USB-PD) management device providing cable plug and orientation detection for two USB Type-C connectors. The TPS26744E-Q1 communicates with the cable and another USB Type-C and PD device at the opposite end of the cable to negotiate power to be delivered. The TPS26744E-Q1 controls an external power supply (eg. DC/DC) for sourcing requested voltage and current to VBUS on the USB-C connector.

The TPS26744E-Q1 also handles message handshaking for DisplayPort Alternate Mode, along with converting messages into HPD logic levels and vice-versa. TPS26744E-Q1 has an integrated VCONN switch to power DisplayPort-capable cables.

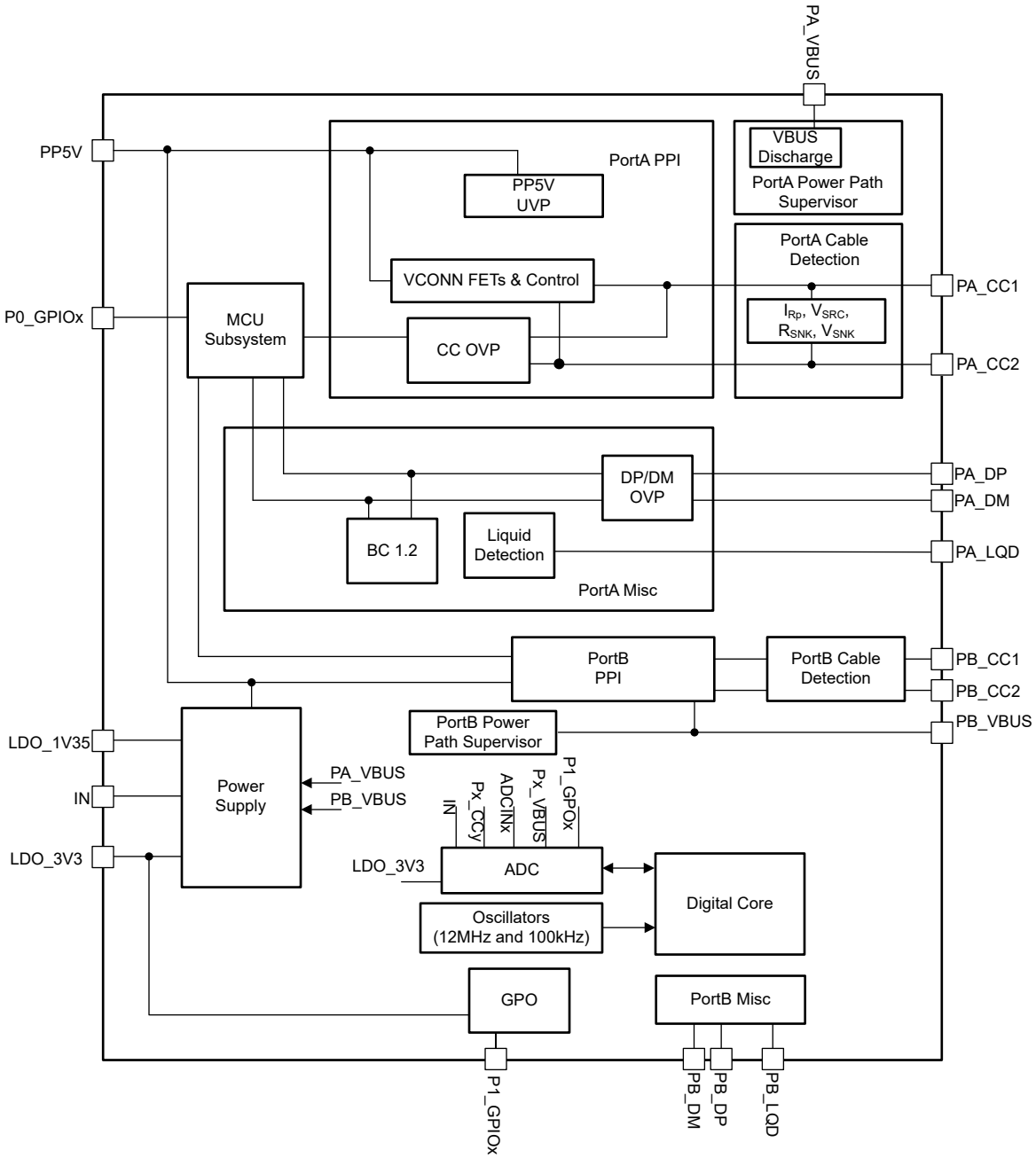
Each Type-C port controlled by the TPS26744E-Q1 is functionally identical and supports the full range of the USB Type-C and PD standards.

The TPS26744E-Q1 has many other features designed for automotive USB-C applications that are detailed in the following subsections.

- Power foldback
- Thermal foldback
- Flexible GPIOs
- System power sharing across multiple PD controllers
- Synchronizing output signals (Px_SYNC)
- Local interconnect network (LIN) support
- Liquid detection
- BC 1.2
- Pulse-width modulation (PWM)

ADVANCE INFORMATION

8.2 Functional Block Diagram



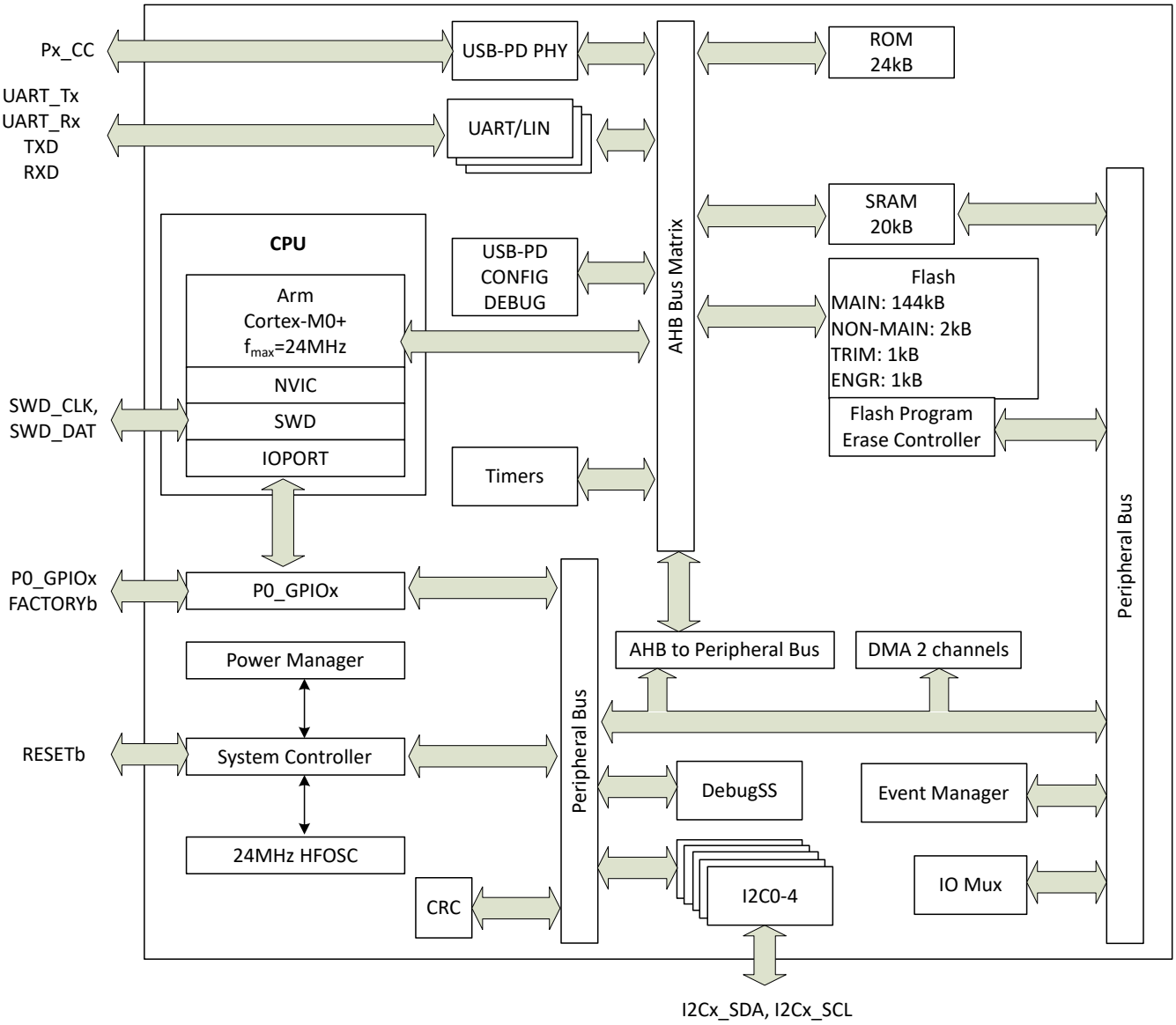


Figure 8-1. MCU Subsystem

8.3 Feature Description

8.3.1 Power Supply

The TPS26744E-Q1 power management block receives power and generates voltages to provide power to the TPS26744E-Q1 internal circuitry. These generated power rails are PP5V, LDO_3V3, and LDO_1V35. LDO_3V3 may also be used as a low-power output. PP5V may be driven externally as a high-power VCONN supply (see Section 8.3.3), but the internal LDO can be used to supply a low-power VCONN. The power supply path is shown in Figure 8-2.

When the PP5V rail is generated from the IN pin using the internal LDO there are two functional regions:

1. Functional Class A (ISO 16750-1) when the IN voltage is 4.5V or higher, the TPS26744E-Q1 has full functionality per the electrical characteristics. However, if the IN voltage is lower than 7V less current can be sourced to the PP5V pin.
2. Functional Class B (ISO 16750-1) when the IN voltage is above 3.5V and below 4.5V the TPS26744E-Q1 functions normally, but some parameters may exceed the limits given in the electrical characteristics. Note that IN below 3.5V may cause LDO_3V3 to fall below its UVLO and reset the TPS26744E-Q1.

When PP5V is used as the input supply for a high-power VCONN, the PP5V voltage cannot exceed the IN voltage because it creates a high leakage path from PP5V to IN. There are two functional regions based on PP5V voltage in this usage scenario:

1. Functional Class A (ISO 16750-1) when the PP5V voltage is 4.75V or higher, the TPS26744E-Q1 has full functionality per the electrical characteristics. When PP5V voltage is 4.5V or higher, the TPS26744E-Q1 has full functionality per the electrical characteristics except for the VCONN power-path.
2. Functional Class B (ISO 16750-1) when the PP5V voltage is above 3.5V and below 4.5V the TPS26744E-Q1 functions normally but some parameters may exceed the limits given in the electrical characteristics. The VCONN power path does not perform normally in this region. Note that PP5V below 3.5V may cause LDO_3V3 to fall below its UVLO and reset the TPS26744E-Q1.

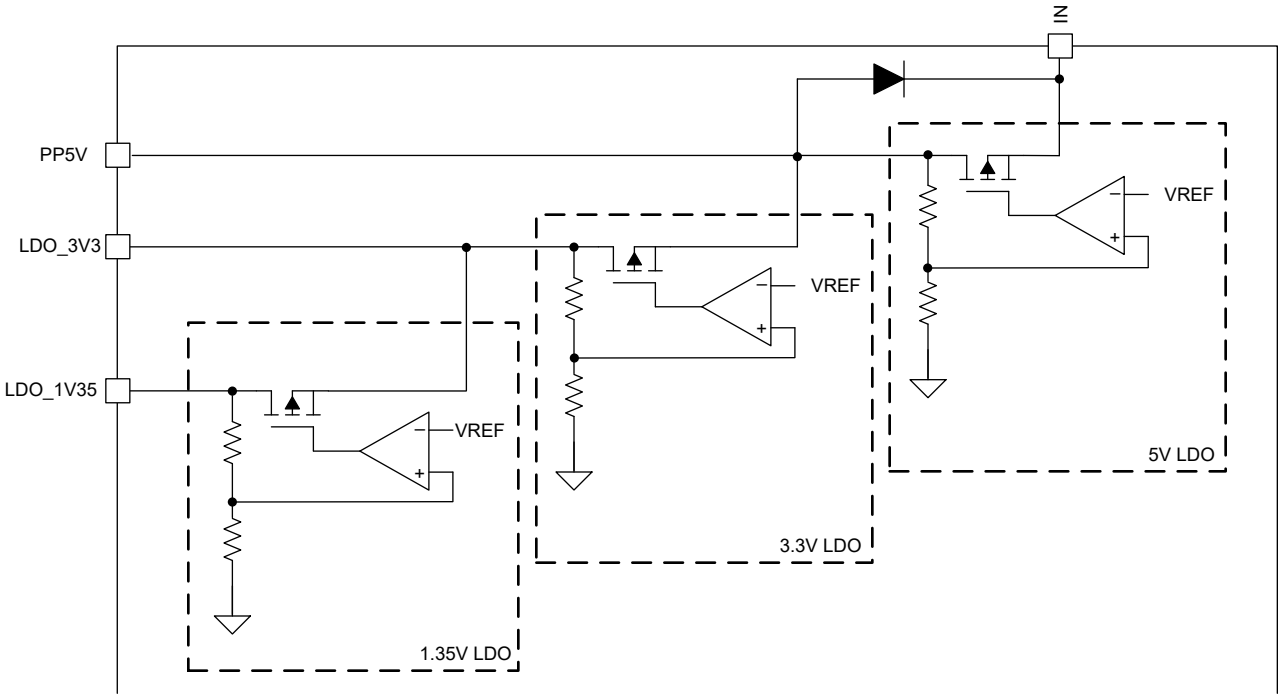


Figure 8-2. Power Supplies

8.3.1.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

8.3.2 Cable Plug and Orientation Detection

The following figure shows the plug and orientation detection block at each Px_CCy pin. Each pin has identical detection circuitry.

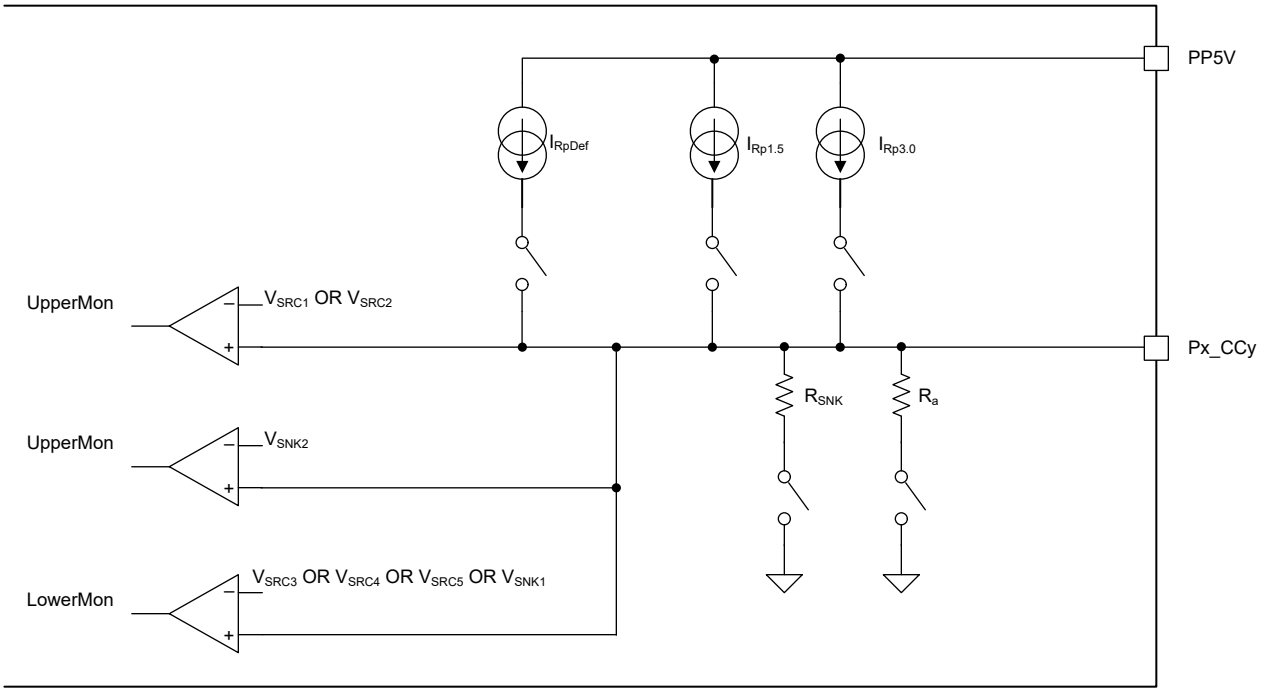


Figure 8-3. Plug and Orientation Detection Block

8.3.2.1 Configured as a Source

When configured as a Source, the TPS26744E-Q1 detects when a cable or a Sink is attached using the Px_CC1 and Px_CC2 pins. When in a disconnected state, the TPS26744E-Q1 monitors the voltages on these pins to determine what, if anything, is connected. See *USB Type-C Specification* for more information.

Table 8-1 shows the Cable Detect States for a Source.

Table 8-1. Cable Detect States for a Source

CC1	CC2	CONNECTION STATE	RESULTING ACTION
SRC.Open	SRC.Open	Nothing attached	Continue monitoring both CCy pins for attach. Power is not applied to VBUS or VCONN.
SRC.Rd	SRC.Open	Sink attached	Monitor CC1 for detach. Power is applied to VBUS but may not be applied to VCONN.
SRC.Open	SRC.Rd	Sink attached	Monitor CC2 for detach. Power is applied to VBUS but may not be applied to VCONN.
SRC.Ra	SRC.Open	Active Cable-No UFP attached	Monitor CC2 for a Sink attach and CC1 for cable detach. Power is not applied to VBUS or VCONN.
SRC.Open	SRC.Ra	Active Cable-No UFP attached	Monitor CC1 for a Sink attach and CC2 for cable detach. Power is not applied to VBUS or VCONN.
SRC.Ra	SRC.Rd	Active Cable-UFP Attached	Provide power on VBUS and VCONN (CC1) then monitor CC2 for a Sink detach. CC1 is not monitored for a detach.
SRC.Rd	SRC.Ra	Active Cable-UFP attached	Provide power on VBUS and VCONN (CC2) then monitor CC1 for a Sink detach. CC2 is not monitored for a detach.
SRC.Rd	SRC.Rd	Debug Accessory Mode attached	Sense either CCy pin for detach.
SRC.Ra	SRC.Ra	Corrosion Mitigation	Sense either CCy pin for detach.

When a TPS26744E-Q1 port is configured as a Source, a current $I_{Rp,Def}$ is driven out each CCy pin and each pin is monitored for different states. When a Sink is attached to the pin it applies a pull-down resistance of Rd to GND. The current $I_{Rp,Def}$ is then forced across the resistance Rd generating a voltage at the CCy pin. The TPS26744E-Q1 applies $I_{Rp,Def}$ until it applies voltage to VBUS, at which time it may change to $I_{Rp3.0A}$ or $I_{Rp1.5A}$.

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When the CCy pin is connected to an active cable VCONN input, the pull-down resistance is different (Ra). In this case the voltage on the CCy pin is lower and the TPS26744E-Q1 recognizes it as an active cable.

The voltage on CCy is monitored to detect a disconnection depending upon which Rp current source is active. When a connection has been recognized and the voltage on CCy subsequently rises above the disconnect threshold for t_{CC}, the TPS26744E-Q1 detects a disconnection.

8.3.2.2 Configured as a Sink

When a TPS26744E-Q1 port is configured as a Sink, the TPS26744E-Q1 presents a pull-down resistance R_{SNK} on each CCy pin and waits for a Source to attach and pull-up the voltage on the pin. The Sink detects an attachment by the presence of VBUS. The Sink determines the advertised current from the Source based on the voltage on the CCy pin.

The following table shows the connection states as a sink.

Table 8-2. Cable Detect States for a Sink

CC1	CC2	CONNECTION STATE	RESULTING ACTION
SNK.Open	SNK.Open	Nothing attached	Continue monitoring both CCy pins for attach.
SNK.Rp	SNK.Open	Source attached	Monitor CC1 for changes in advertised Rp and detach in some cases. Monitor VBUS to confirm attach or detect detach.
SNK.Open	SNK.Rp	Source attached	Monitor CC2 for changes in advertised Rp and detach in some cases. Monitor VBUS to detect detach.
SNK.Rp	SNK.Rp	Debug Accessory Attached	Compare CC1 and CC2 to detect orientation. Monitor VBUS for detach.

8.3.3 VCONN Power Path

The TPS26744E-Q1 features internal 5V VCONN sourcing power paths called Px_VCONN as shown in Figure 8-4. Each path contains programmable current clamping protection (I_{LIMVC}), overvoltage protection (OVP), UVLO protection, reverse-current protection (RCP) and overtemperature protection (OTSD).

When the Px_VCONN switch is enabled, it turns on with slew-rate control per the parameters t_{VCRISE} and t_{VCON}.

When the Px_VCONN switch is disabled, it turns off with slew-rate control per the parameters t_{VCFALL} and t_{VCOFF}. The turn off times for fault events are specified separately:

- RCP fault event: t_{VC_RCP}
- PP5V OVP fault event: t_{VC_OVP}
- PP5V UVLO fault event: t_{VC_UVLO}

Using the eMarker-only setting the internal LDO from the IN pin can supply sufficient current to the PP5V pin.

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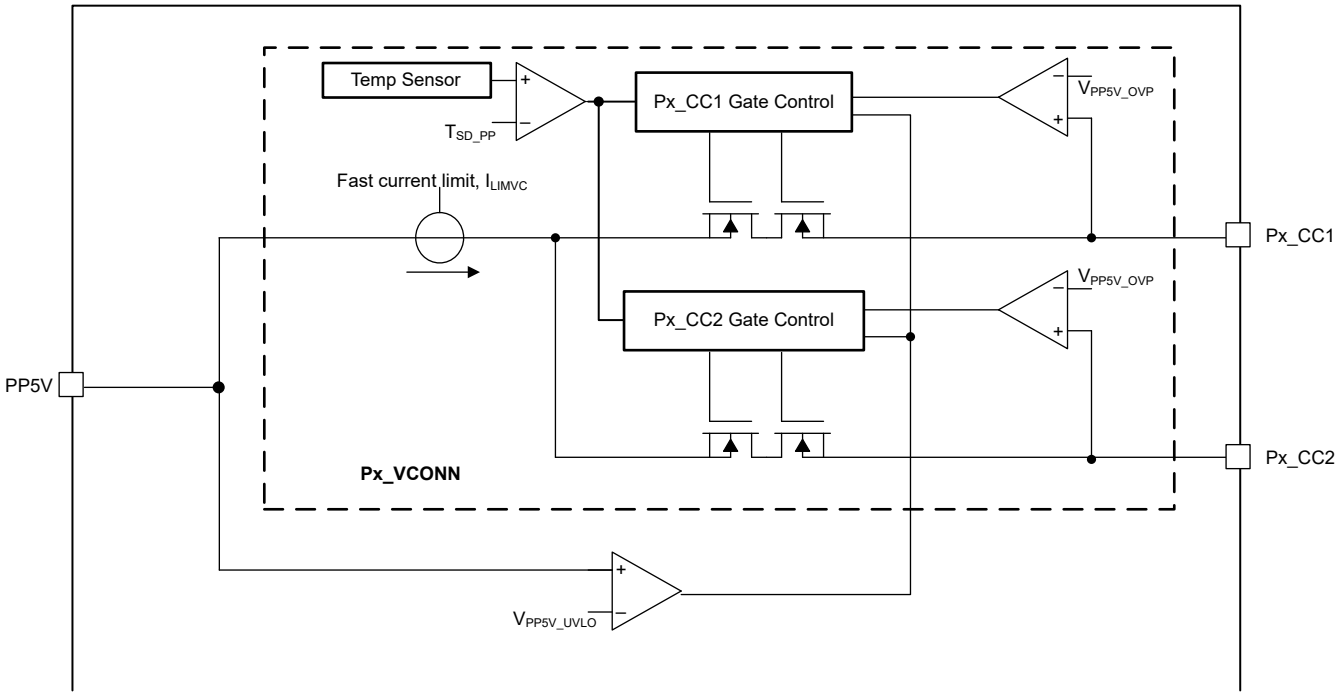

Figure 8-4. Px_VCONN Power Path

8.3.3.1 Current Clamp

When enabled and providing VCONN power the TPS26744E-Q1 Px_VCONN power switch clamps the current to I_{ILIMVC}. When the current through the Px_VCONN switch exceeds I_{ILIMVC}, the current clamping circuit activates within t_{iOS_VCONN} and the switch behaves as a constant current source.

8.3.3.2 Px_VCONN Local Overtemperature Shut Down (OTSD)

When Px_VCONN clamps the current, the temperature of the switch begins to increase. When the local temperature sensor for Px_VCONN detects that $T_J > T_{SD\_PP}$ the Px_VCONN switch is disabled within t_{VCOFF}. The port then enters the USB Type-C ErrorRecovery state.

8.3.3.3 Px_VCONN OVP

There is an OVP comparator at the output of Px_VCONN (that is the Px_CC1 or Px_CC2 pin) with a fixed threshold. If an OVP is detected ($V_{Px\_CCy} > V_{PP5V\_OVP}$) while Px_VCONN is enabled, then Px_VCONN is disabled within t_{VC_OVP} and the port enters into the Type-C ErrorRecovery state.

8.3.3.4 Px_VCONN UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}) while Px_VCONN is enabled, then Px_VCONN is disabled within t_{VC_UVLO} and the port enters into the Type-C ErrorRecovery state.

8.3.3.5 Px_VCONN RCP

If reverse current is detected, ($V_{Px\_CCy} - V_{PP5V}$) > V_{VC_RCP}, while the Px_VCONN path is enabled, then it is disabled within t_{VC_RCP}. If the RCP condition clears, then the Px_VCONN path is automatically enabled within t_{VCON}.

8.3.4 USB-PD Physical Layer

Figure 8-5 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block. This block is duplicated for the second TPS26744E-Q1 port.

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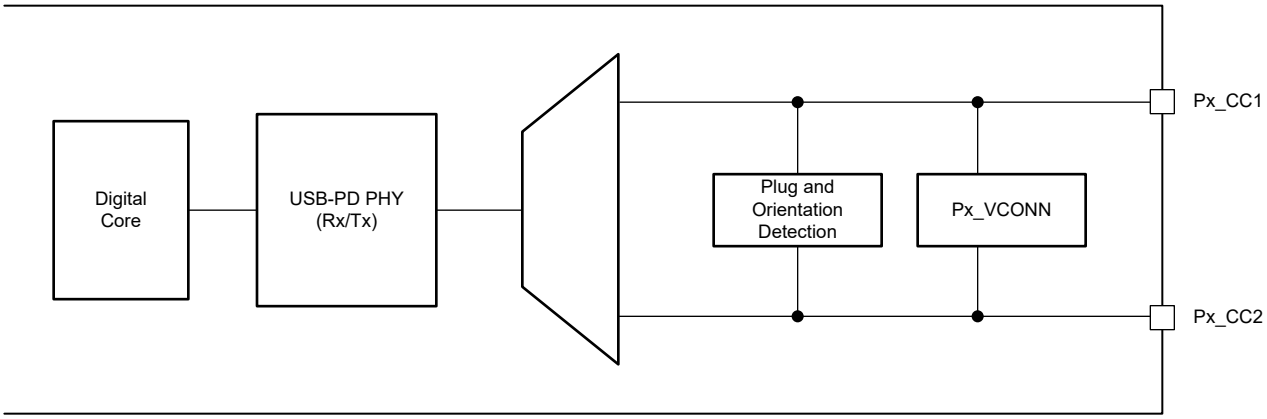

Figure 8-5. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using BMC signaling. The BMC signal is output on the same pin (Px_CC1 or Px_CC2) that is DC biased due to the Rp (or Rd) cable attach mechanism.

8.3.4.1 USB-PD Encoding and Signaling

Figure 8-6 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 8-7 illustrates the high-level block diagram of the baseband USB-PD receiver.

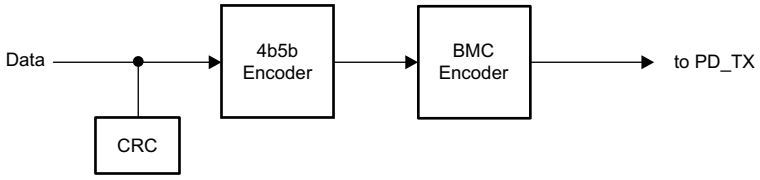

Figure 8-6. USB-PD Baseband Transmitter Block Diagram

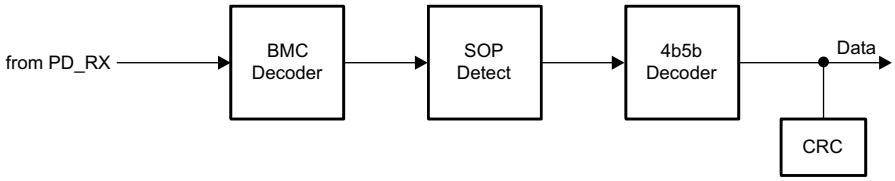

Figure 8-7. USB-PD Baseband Receiver Block Diagram

8.3.4.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS26744E-Q1 is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit period when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). Figure 8-8 illustrates Biphase Mark Coding.

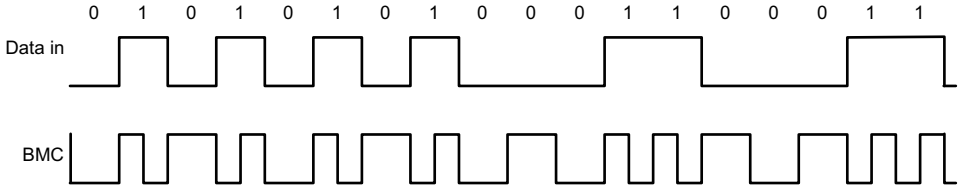

Figure 8-8. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the Px_CC1 or Px_CC2 pin with a tri-state driver. The tri-state driver is slew rate controlled to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to enable the receiver to clock the final bit of EOP.

8.3.4.3 USB-PD BMC Transmitter

The TPS26744E-Q1 transmits and receives USB-PD data over one of the Px_CC1 or Px_CC2 pins for a given CC pin pair (one pair per USB Type-C port). The Px_CC1 or Px_CC2 pins are also used to determine the cable orientation and maintain the cable/device attach detection. Thus, a DC bias exists on the Px_CCy pin. The transmitter driver overdrives the Px_CCy DC bias while transmitting, but returns to a Hi-Z state allowing the DC voltage to return to the Px_CCy pin when not transmitting. While either Px_CC1 or Px_CC2 may be used for transmitting and receiving, during a given connection only the one that mates with the CC pin of the plug is used; so there is no dynamic switching between Px_CC1 and Px_CC2. Figure 8-9 shows the USB-PD BMC TX and RX driver block diagram.

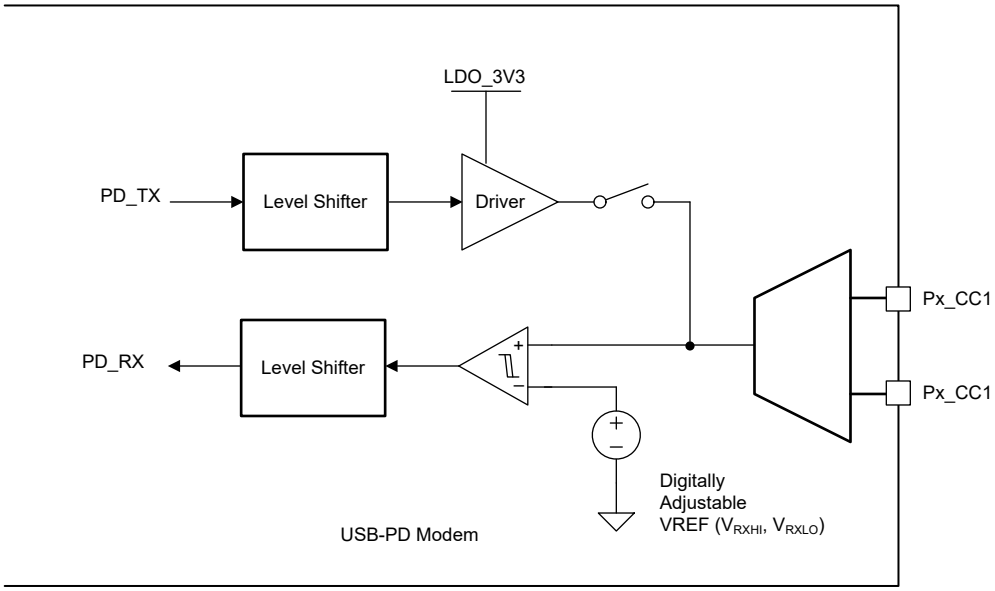

Figure 8-9. USB-PD BMC TX/Rx Block Diagram

Figure 8-10 shows the transmission of the BMC data on top of the DC bias. Note, the DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach, and the DC bias can be above or below the VOH of the transmitter driver.

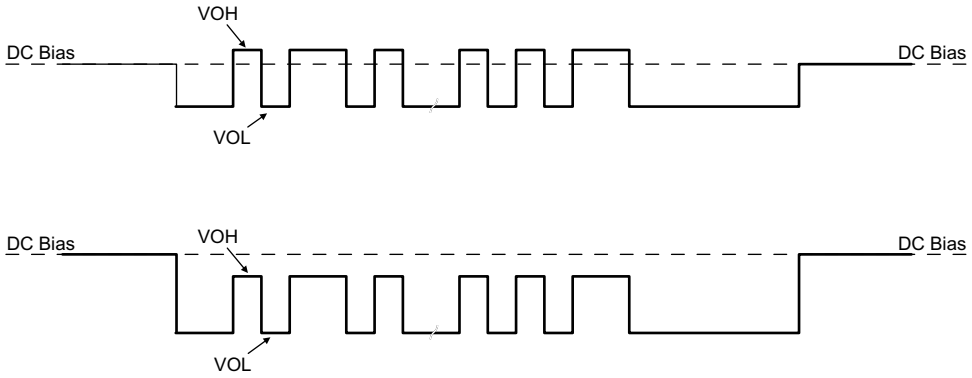

Figure 8-10. TX Driver Transmission with DC Bias

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The transmitter drives a digital signal onto the Px_CC1 or Px_CC2 pins. The signal peak, V_{TXHI}, is set to meet the TX masks defined in the *USB-PD Specifications*. Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of Z_{DRIVER}. Z_{DRIVER} is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. Z_{DRIVER} impacts the noise ingression in the cable.

Figure 8-11 shows the simplified circuit determining Z_{DRIVER}. It is specified such that noise at the receiver is bounded.

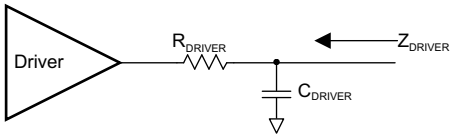

Figure 8-11. ZDRIVER Circuit

8.3.4.4 USB-PD BMC Receiver

The receiver block of the TPS26744E-Q1 is designed to receive a signal that follows the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

Figure 8-12 shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (Z_{BMCRX}). The *USB-PD Specification* also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

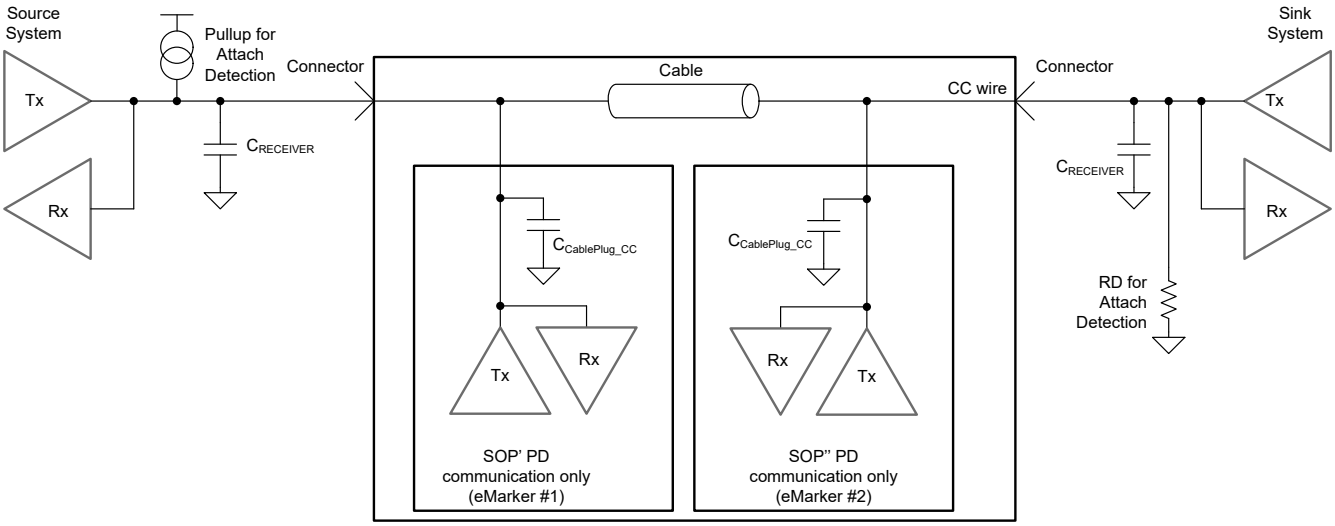

Figure 8-12. Example USB-PD Multi-Drop Configuration

8.3.4.5 Squelch Receiver

The TPS26744E-Q1 has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification.

8.3.5 DBG_SDA, DBG_SCL and DP/DM Overview

The pins that have Px_DP and Px_DM pin functions also have P1_GPOx pin functions. The pins that may be used for the PA_DP and PA_DM pin functions, may instead be used for the DBG_SCL and DBG_SDA pin functions. The DBG_SCL and DBG_SDA pin functions can be connected to the SBUx pins on the connector or

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to the D+/D- pins. This section shows the overall diagrams, and following subsections provide more details on each.

- The DBG_SCL and DBG_SDA pin functions provide access to I2C4 and UART from the MCU sub-system. This channel may be used for updating the flash (see Section 8.3.5.1).
- DP/DM charging functionality Section 8.3.5.2

The following sub-sections provide more details.

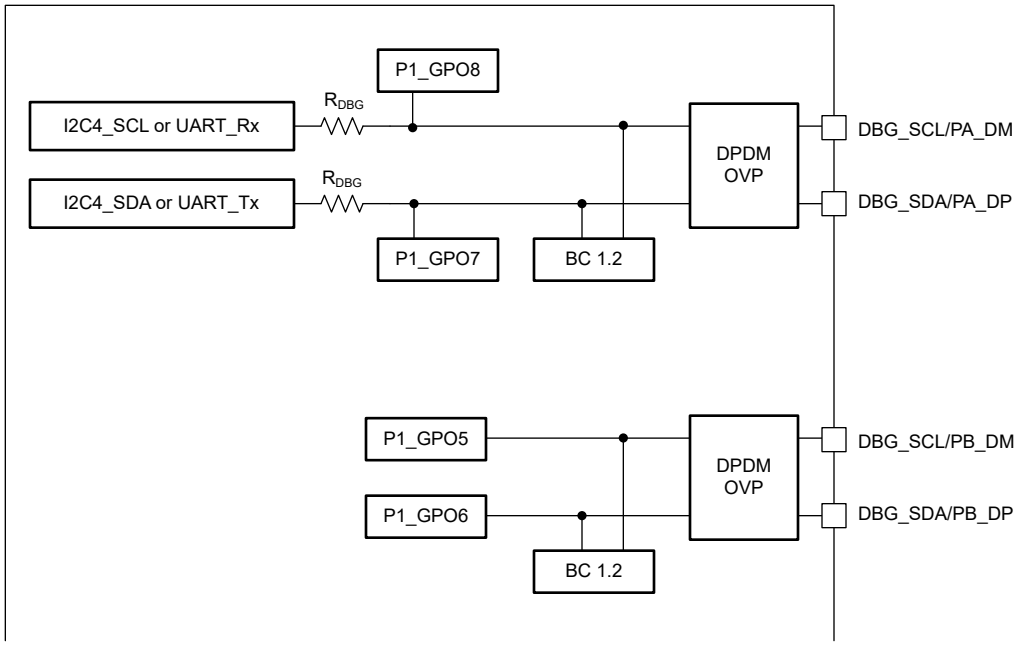

Figure 8-13. DP DM Hardware Functionality

8.3.5.1 Closed Chassis Debugging and Updating Flash

The DBG_SDA and DBG_SCL pins can be used to connect to a pin on the USB-C connector to gain access to I2C4 or UART. The I2C4 access provides capability to update the flash memory, but also provides a way to monitor or control TPS26744E-Q1 for debugging. This debug access can also be permanently disabled.

The DBG_SDA pin may also be used to output debug UART messages instead of being used for I2C4 access.

Note

Access to I2C4 is not available unless the TPS26744E-Q1 has been previously loaded with firmware that enables this feature.

8.3.5.1.1 I2C4 Access For Closed-chassis Debugging

If the PA_DM and PA_DP pin functions are required, then DBG_SDA and DBG_SCL are also be attached to the D+/D- pins on the connector. In other cases DBG_SDA/SCL may be connected to SBU1/SBU2. Both options are shown in the below figures. The TPS26744E-Q1 disables I2C4 until a debug accessory is detected (5.1kΩ on both CC pins) to avoid interfering with any other signaling.

The debug accessory intended for I2C4 access must provide the I2C pullups as illustrated in the following figures. Figure 8-14 illustrates using the D+/D- pins for I2C4 access. Note that the TPS26744E-Q1 can be configured to enable UART instead of I2C4.

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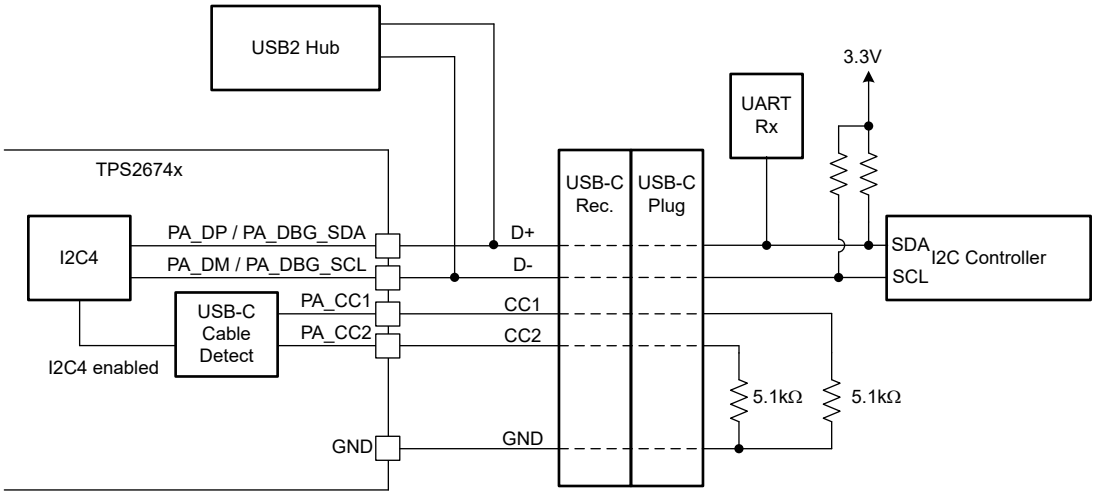

Figure 8-14. Connecting I2C4 to a Debug Accessory

The following figure shows the same configuration when connecting to a USB2 device instead of a debug accessory. In this case I2C4 remains disabled because the TPS26744E-Q1 only sees a 5.1kΩ resistor on one CC pin (since the cable only has one CC wire). In this case I2C4 remains disabled to allow D+/D- signaling.

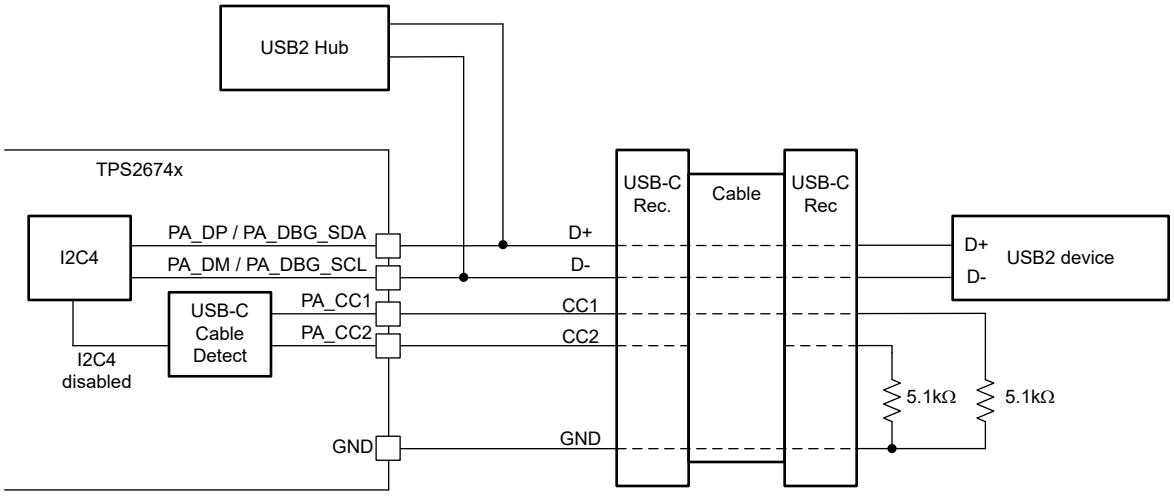

Figure 8-15. I2C4 Does Not Interfere with D+/D- Signaling

The following two figures illustrate using SBU1 and SBU2 for I2C4 access. Figure 8-16 shows connecting to a Debug Accessory and Figure 8-17 shows connecting to a DP source. The concept is the same as for the D+/D- pins described above. The PA_DBG pins can be connected in any similar way to an I2C controller for debug access.

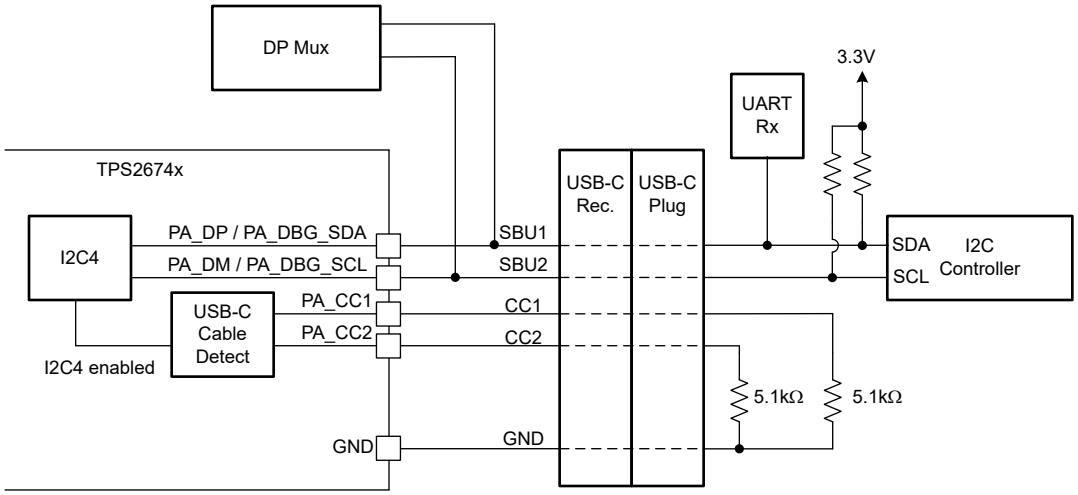

Figure 8-16. Connecting I2C4 to a Debug Accessory

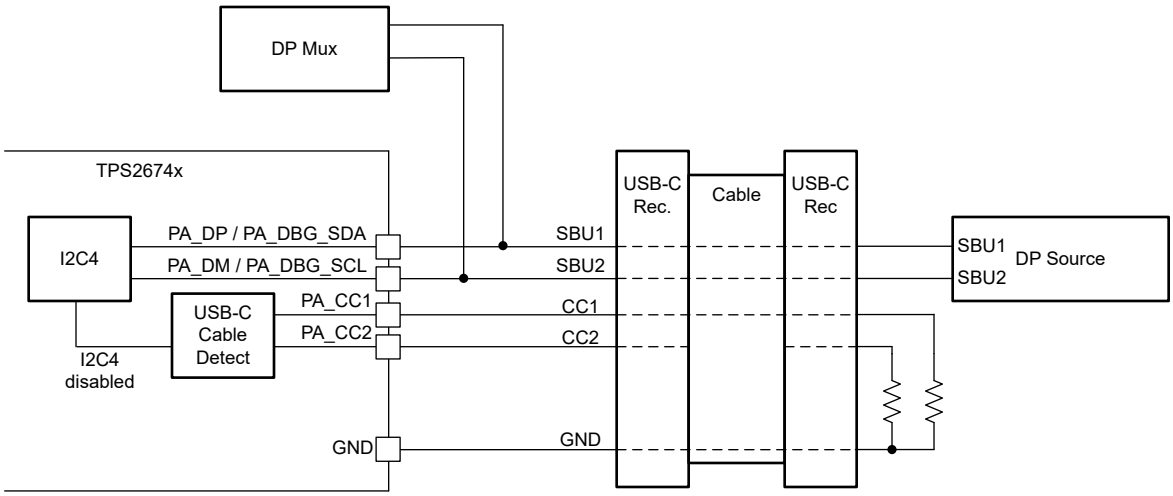

Figure 8-17. I2C4 Does Not Interfere With SBU Signaling

8.3.5.1.2 UART Access for Closed-chassis Debugging

The PA_DBG_SDA pin also has a UART_Tx capability for debug output messages. This capability is not enabled by default. The baud rate is configurable and the capacitance of the channel may cause achievable baud rate to vary. The kinds of debug messages output by the device is also configurable.

8.3.5.2 BC1.2 and Legacy Charging Functionality

The following figure shows the hardware used to implement BC1.2 functionality.

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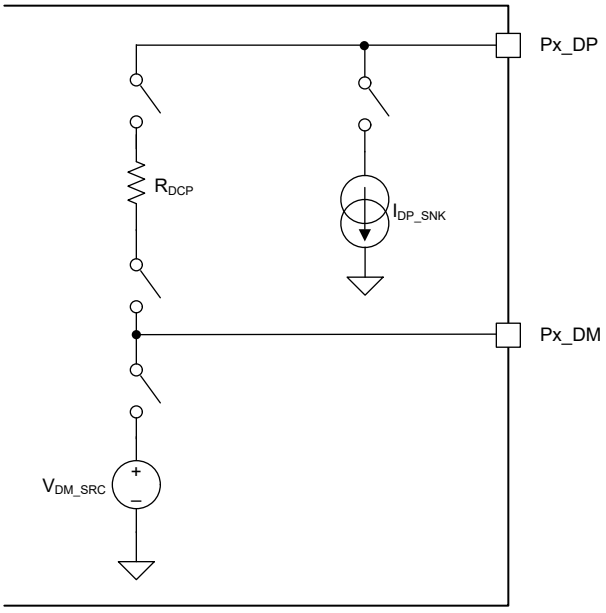

Figure 8-18. BC1.2 Legacy Charging Diagram

8.3.5.2.1 Charging Downstream Port (CDP) Mode

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5A per port. A CDP provides power and meets the USB 2.0 requirements for device enumeration. USB-2.0 communication is supported, and the host controller must be active to allow charging. The difference between CDP and SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 portable device and allows for additional current draw by the portable device.

The CDP handshaking process occurs in two steps. During step one, the portable device outputs a nominal 0.6V output on the DP line and reads the voltage input on the DM line. The portable device detects the connection as an SDP if the voltage is less than the nominal data-detect voltage of 0.3V. The portable device detects the connection as a CDP if the DM voltage is greater than the nominal data detect voltage of 0.3V and optionally less than 0.8V.

The second step is necessary for portable equipment to determine whether the equipment is connected to a CDP or a DCP. The portable device outputs a nominal 0.6V output on the DM line and reads the voltage input on the DP line. The portable device concludes the equipment is connected to a CDP if the data line being read remains less than the nominal data detects voltage of 0.3V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3V.

8.3.5.2.2 Dedicated Charging Port (DCP) Mode

A DCP only provides power and does not support data connection to an upstream port. The DCP functionality can be achieved by shorting the D+ and D- pins together near the USB-C connector. That leaves the Px_DP and Px_DM pins available for other functions in the system.

8.3.6 Liquid Detection

The TPS26744E-Q1 provides a Px_LQD pin for liquid detection. This pin may be connected to an appropriate pin on the USB-C receptacle for liquid detection. In most cases it is best to connect to either SBU1 or SBU2 as allowed by the USB-C specification since those are high-Z until needed for Alternate Mode or USB4 mode functionality.

The concept behind the liquid detection is to send a current pulse on the Px_LQD pin and measure how long it takes the pin voltage to reach a threshold. Liquids have capacitive and resistive components that slow the rise of the voltage and limit its maximum value. There are many factors that can affect the exact rise time so tunability is designed into the solution.

In order to limit the maximum Px_LQD voltage a weak pulldown resistor is used (R_{LQD}). Different pulldown options are available to pair with different current source strengths (I_{LQD}). The intention is to use liquid detection with a maximum voltage of approximately 2.0V. So the specifications are written around that use case. A secondary maximum pin voltage option is 0.4V in case there are clamps on the pins used for liquid detection.

Figure 8-19 illustrates the concept. At time 0, a current pulse is applied to the Px_LQD pin. Depending on the selected I_{LQD} and R_{LQD} there is a maximum expected pin voltage of V_{MAX}. Even in a dry receptacle there may be some capacitance that slows the rise time slightly, but liquids prone to cause corrosion have a slower rise time. A threshold (V_{LQD}) is chosen so that a dry receptacle (or a receptacle with distilled water) is *not* detected as a fault condition. The T_{RISE}(Liquid) threshold is programmable in FW up to ~5ms. If the rise time exceeds T_{RISE}(Liquid) then actions are taken to mitigate corrosion due to the presence of liquid. Once liquid is detected, it is rechecked periodically until no liquid is detected before resuming normal operation.

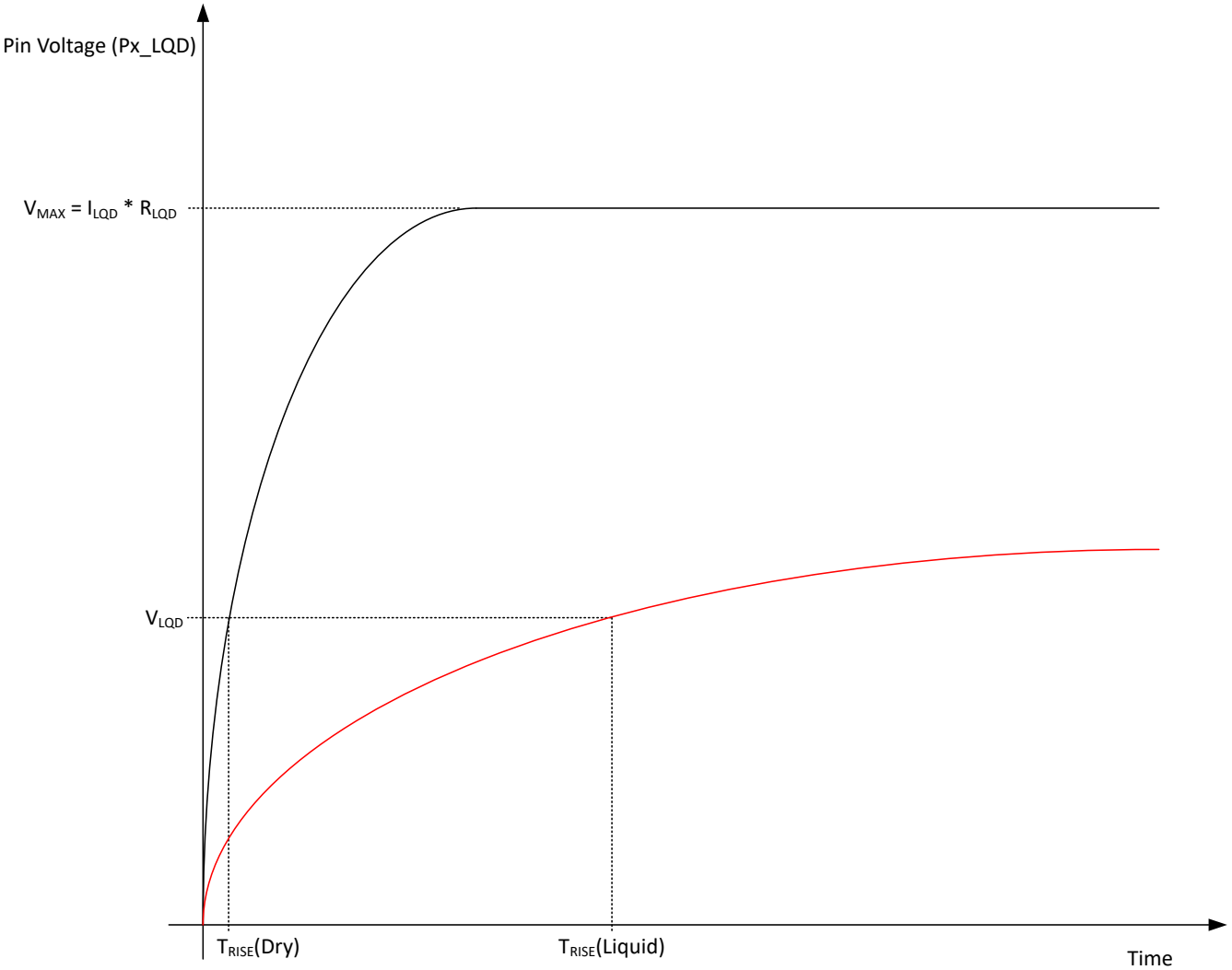

Figure 8-19. Pin Voltage Illustration

8.3.7 Local Interconnect Network (LIN) Support

The TPS26744E-Q1 supports communication using the LIN protocol as an alternative to I2C for controlling or monitoring power policy or other features. The TXD pin function is an output from TPS26744E-Q1, and the RXD pin function is an input into the TPS26744E-Q1.

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Note

If the TXD from multiple TPS26744E-Q1 are connected as shown in the following diagram, those P0_GPIOx pins must be configured as open-drain.

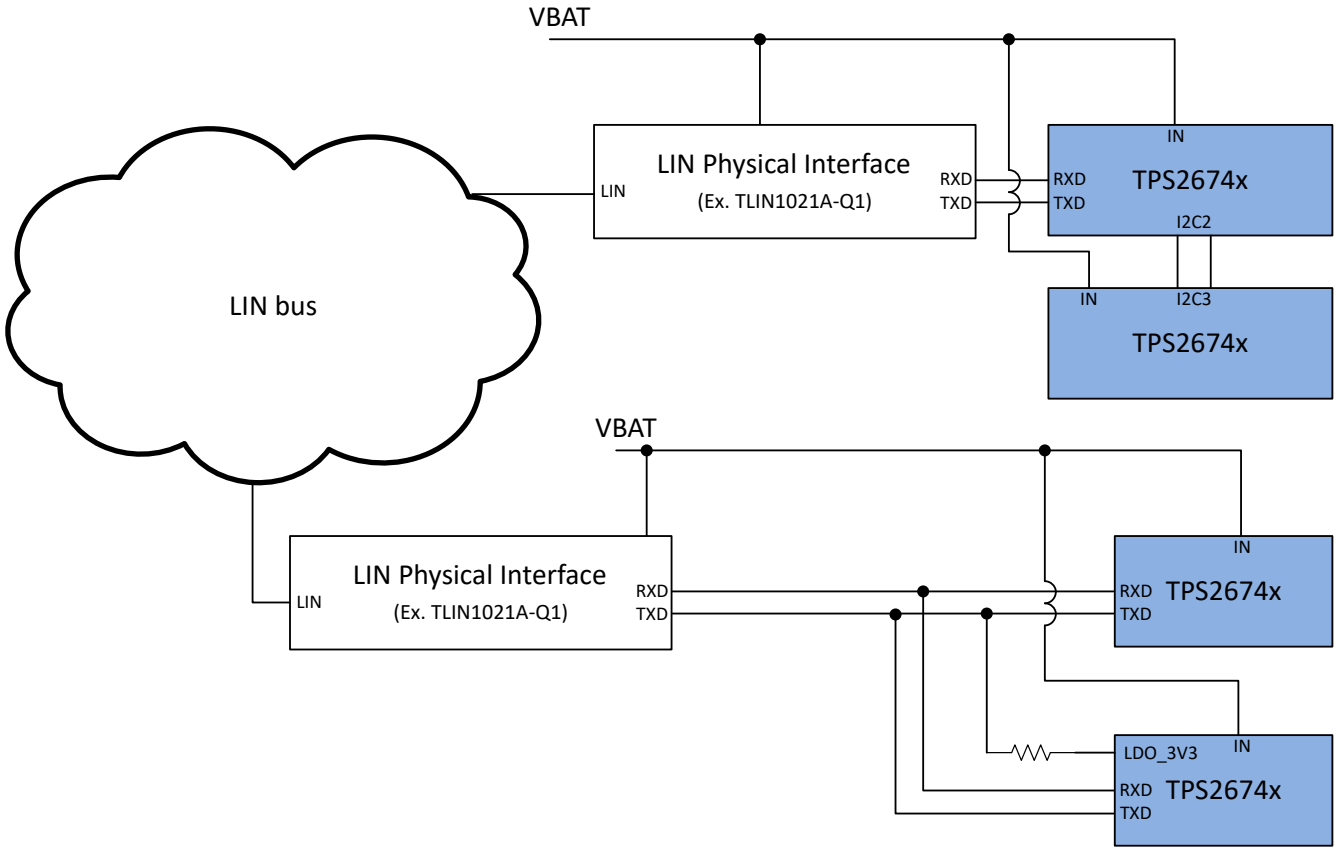

Figure 8-20. Example of Connecting to a LIN Bus

8.3.8 Thermal Shutdown

The TPS26744E-Q1 features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of T_{SD}. When the temperature falls below the threshold and clears the hysteresis the device resumes normal operation.

Each power path has a thermal shutdown monitor. When the temperature of a power-path exceeds T_{SD_PP} the associated Px_VCONN is disabled. When the temperature falls below the threshold and clears the hysteresis the power paths resume normal operation.

8.3.9 ADC

The TPS26744E-Q1 ADC is shown in Figure 8-21. The ADC is a successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read via I^2C and is also an input for the automatic ADC monitor circuits.

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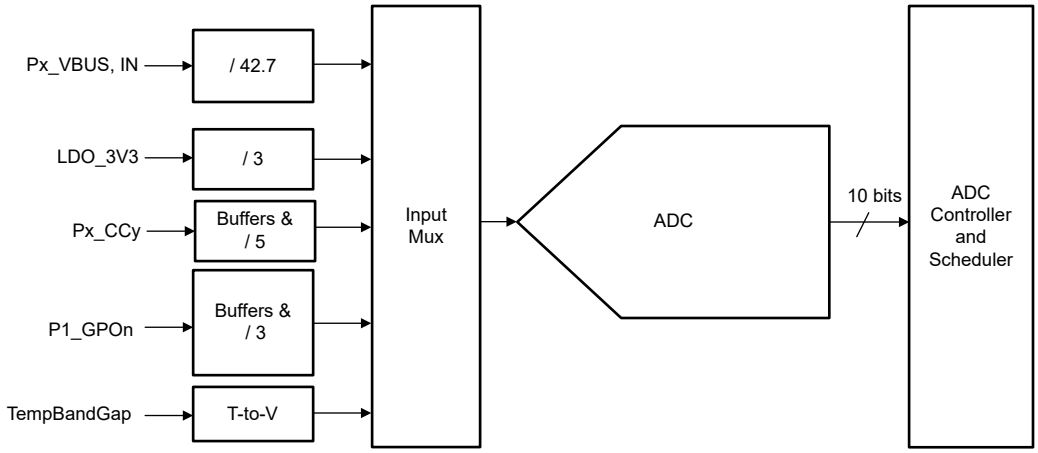

Figure 8-21. SAR ADC

8.3.9.1 ADC Divider Ratios

The ADC voltage inputs are each divided down to the full-scale input of 1.2 V.

The following table shows the divider ratios for each ADC input.

Table 8-3. ADC Inputs

CHANNEL	SIGNAL	TYPE	LSB	DIVIDER RATIO
0	LDO_3V3	Voltage	3.52mV	3
1	Reserved			
2	P1_GPO0	Voltage	3.52mV	3
3	P1_GPO1	Voltage	3.52mV	3
4	P1_GPO2	Voltage	3.52mV	3
5	P1_GPO3	Voltage	3.52mV	3
6	BandGapTemp	Temperature		N/A
7	IN	Voltage	50mV	42.7
8-11	Reserved			
12	P1_GPO7	Voltage	3.52mV	3
13	P1_GPO8	Voltage	3.52mV	3
14	P1_GPO6	Voltage	3.52mV	3
15	P1_GPO5	Voltage	3.52mV	3
16	PA_VBUS	Voltage	50mV	42.7
17	PA_CC1	Voltage	5.86mV	5
18	PA_CC2	Voltage	5.86mV	5
19-23	Reserved			
24	PB_VBUS	Voltage	50mV	42.7
25	PB_CC1	Voltage	5.86mV	5
26	PB_CC2	Voltage	5.86mV	5
27-31	Reserved			

8.3.10 VIN Power Foldback

When the voltage at the IN pin is too low it may require too much current from the battery in order to provide the full-power normally offered on VBUS. The TPS26744E-Q1 can monitor the IN voltage and reduce the VBUS output power when it droops.

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8.3.11 Thermal Foldback

The TPS26744E-Q1 can measure system temperature and adjust the output power to each USB-C port to reduce temperature if necessary. To accurately sense system temperature an NTC can be connected to a P1_GPOx pin that has an ADC input as shown in the following figure. Alternatively, an I^2C capable NTC can be used.

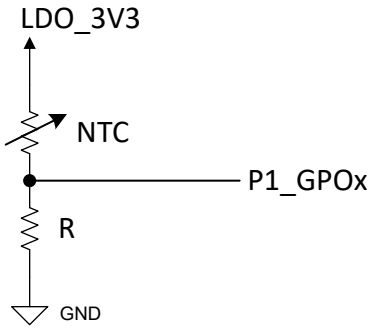

Figure 8-22. Example of using an NTC to sense temperature.

8.3.12 DisplayPort Hot-Plug Detect (HPD)

The TPS26744E-Q1 supports the DisplayPort over USB Type-C as a DP source or DP sink. The TPS26744E-Q1 supports the HPD converter functions on P0_GPIOx pins. The PD messaging events are translated into high or low on the corresponding HPD pin in a DisplayPort transmitter system. On the other hand, a DisplayPort receiver system translates high or low status on the HPD pin PD messages that it transmits.

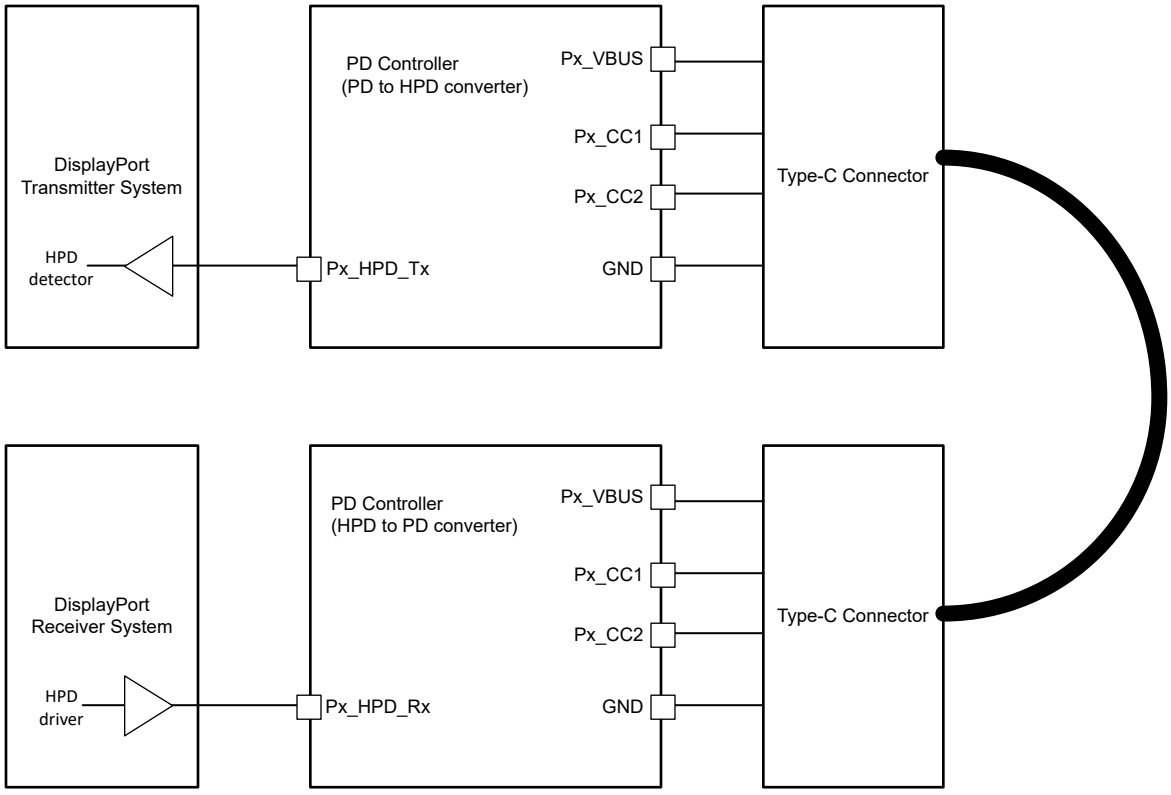

Figure 8-23. Illustration of How a PD-to-HPD Converter Passes the HPD Signal Along in a DisplayPort System

8.3.13 General GPIO

The TPS26744E-Q1 has groups of GPIO pins labeled P1_GPOx, and P0_GPIOx with each group having specific properties summarized in the table below. The following subsections describe the functionality of each group in more detail. GPIO/GPO pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC.

Table 8-4. Comparison of GPIO/GPO Types

	P0_GPIOx	P1_GPOx	P2_GPOx(1)
Type	Push-pull or open-drain	Push-pull or open-drain	Open-drain
Max voltage	V_{LDO_3V3}	V_{LDO_3V3}	5.5V
Output supply	LDO_3V3	LDO_3V3	N/A
weak pull-up	40k	100k	N/A
weak pull-down	40k	100k	N/A
Input supply reference	LDO_3V3	LDO_3V3	N/A
ADC input	No	Yes for some pins.	

1. These pin functions are not available on all devices. Check the pin list.

8.3.13.1 P0_GPIOx

The following figure shows the GPIO I/O buffer for P0_GPIOx pins.

The following table lists functionalities of each IO. There are certain mux functions that can be assigned to multiple P0_GPIOx pins, but only one at a time. These mux options provide flexibility to select the set of mux functions needed in a particular system.

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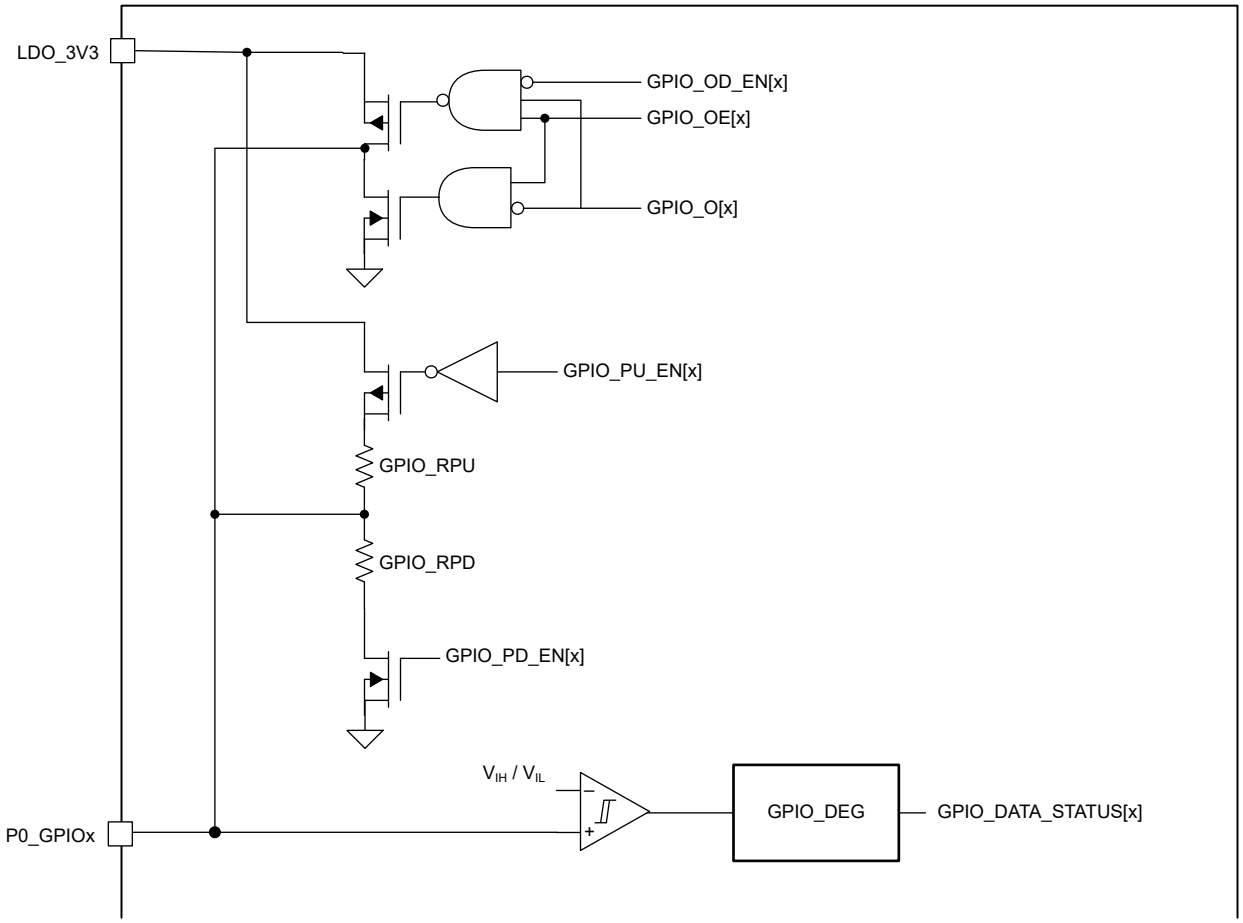

Figure 8-24. P0_GPIOx Buffer Diagram

Table 8-5. P0_GPIOx Functionality Table

Pin Name	Primary Muxed Functionality	Other Available Options
P0_GPIO0	I2C3_SCL	I2C2_SCL, PB_PWM
P0_GPIO1	PB_SYNC	I2C2_SDA, I2C3_SDA
P0_GPIO2	PB_HPD (Rx or Tx)	PA_HPD (Rx or Tx)
P0_GPIO3	PA_PWM	UART_DBG_Tx(2)
P0_GPIO4	I2C1_SCL	TXD(1)
P0_GPIO5	I2C1_SDA	RXD(1)
P0_GPIO6	PA_SYNC	UART_DBG_Tx(2)
P0_GPIO7	I2C2_SCL	I2C3_SCL, PB_PWM
P0_GPIO8	I2C2_SDA	I2C3_SDA, PB_SYNC
P0_GPIO9	UART_DBG_Tx(2)	I2C4_SCL, PA_HPD (Rx or Tx) , PB_HPD_Rx
P0_GPIO10	PA_HPD (Rx or Tx)	I2C4_SDA, PB_PWM , PB_HPD_Rx

1. Only one of the UART_Rx/UART_Tx or the LIN (TXD, RXD) functions can be used at a time.
2. UART_DBG_Tx can only be assigned to one pin at a time.

8.3.13.2 P1_GPOx

Figure 8-25 shows the GPIO I/O buffer for the P1_GPOx pins. These pins are fail-safe. A subset of the GPOs are ADC inputs see Table 8-6.

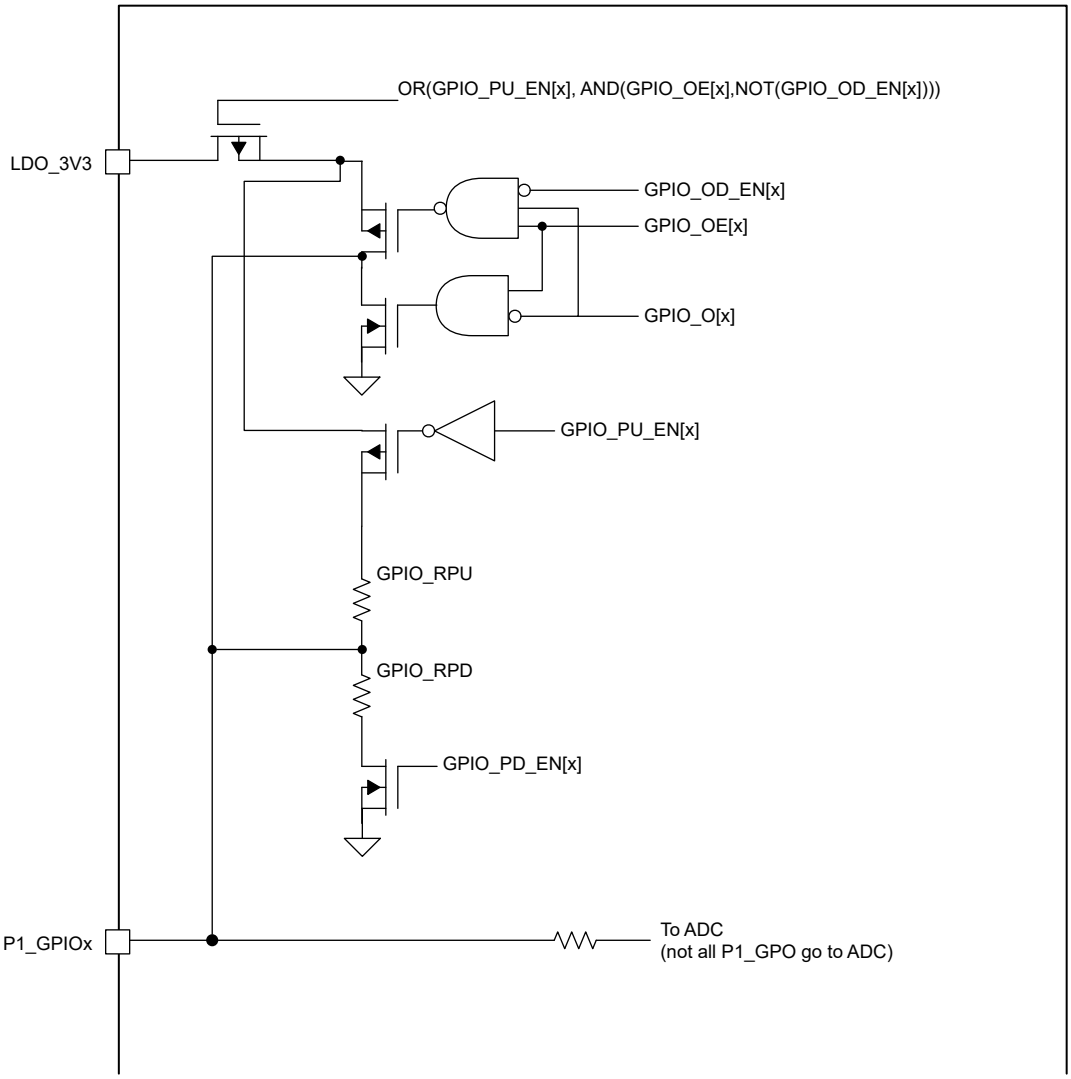

Figure 8-25. P1_GPOx Buffer

Table 8-6. P1_GPOx Functionality Table (ADCINx = ADC Input Channel x)

Pin Name	Special Functionality	Muxed Functionality	GPIO functionality
P1_GPO0	ADCIN2	PA_PPEXT	Push-Pull, weak pullup, weak pulldown
P1_GPO1	ADCIN3	PA_LQD	Open-drain output
P1_GPO2	ADCIN4	PB_LQD	Open-drain output
P1_GPO3	ADCIN5	PB_PPEXT	Push-Pull, weak pullup, weak pulldown
P1_GPO4		ENSD	Push-Pull, weak pullup, weak pulldown
P1_GPO5	PB_DM, ADCIN15		Open-drain output
P1_GPO6	PB_DP, ADCIN14		Open-drain output
P1_GPO7	PA_DP, ADCIN12, DBG_SDA		Open-drain output
P1_GPO8	PA_DM, ADCIN13, DBG_SCL		Open-drain output

8.3.14 ENSD Functionality

If the ENSD pin is low while the ENSD pin function is enabled then the device stays in the shutdown mode (see $I_{IN,SD}$). When ENSD is asserted to force entry into the shutdown mode, it must be held low for longer than the deglitch time (T_{ENSD_DEG}).

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The ENSD pin is pulled up internally via the GPIO_RPU resistor. Therefore, any load stronger than 510kΩ *may* prevent the device from booting, and any load stronger than 110kΩ prevents the device from booting. Therefore, when the P1_GPO4 pin is configured as an output GPO instead of ENSD functionality, the pin cannot be loaded externally while the TPS26744E-Q1 is powering on. An external pullup to LDO_3V3 can also be applied.

8.3.15 Px_SYNC Output

Many DC/DC controllers have a SYNC input for their switching loop. The TPS26744E-Q1 has Px_SYNC pins to drive this signal to the DC/DC on each port to prevent simultaneous switching of different DC/DC controllers in the system.

The internal HF_OSC clock is divided down to create a HF_SYNC clock used to drive a square wave to the selected P0_GPIO pin at f_{SYNC_NOM}. The PB_SYNC signal can be configured to have 0º, 90º, 180º, or 270º phase delay relative to the PA_SYNC signal.

The TPS26744E-Q1 also supports cycle-to-cycle dithering following a triangular frequency profile. The modulation frequency of this triangular wave is f_{MOD}, and max swing is f_{SYNC_SWING}.

The TPS26744E-Q1 also includes dual-random spread spectrum (DRSS) on the Px_SYNC signal by adding pseudorandom variation $f_{DITH}(t)$.

Combining all the configurations, the SYNC frequency f_{SYNC} (and therefore the time between rising edges on Px_SYNC) changes in time according to:

$$f_{SYNC}(t) = f_{SYNC\_NOM} + f_{SYNC\_SWING} * \text{triangular}(2*\pi*f_{MOD}(t)*t) + f_{DITH}(t)$$

The P0_GPIOx used for the Px_SYNC functionality can be configured for open-drain or push-pull mode, and the weak pullup or pulldown resistors may be configured.

8.3.16 Pulse-Width Modulation (PWM) Output

The TPS26744E-Q1 has a PWM module that may be used for various purposes such as controlling an LED or creating a dynamic voltage reference. The PWM module can be configured to have a duty cycle that is dynamic or fixed. The application firmware can also dynamically set the duty-cycle, for example to drive the VBUS voltage output from a DC/DC regulator.

When setting a fixed duty cycle the T_{PWM_ON} and T_{PWM_TOTAL} can be configured to control the duty-cycle (DC) T_{PWM_ON} / T_{PWM_TOTAL}. The application firmware can set the DC as needed in different applications based on USB-PD or other kinds of events.

When using the dynamic duty-cycle option the duty-cycle can vary periodically over T_{PWM_PERIOD}. The variation can be configured as sinusoidal, triangular, or sawtooth.

The P0_GPIOx used for the Px_PWM functionality can be configured for open-drain or push-pull mode, and the weak pullup or pulldown resistors may be configured.

8.3.17 I²C Interface

The TPS26744E-Q1 has multiple I²C ports. The following table lists the type and typical usage for each port. The target ports provide general status information about the TPS26744E-Q1, as well as the ability to control the behavior of the device. The controller port allow the TPS26744E-Q1 to control other target devices in the system.

Table 8-7. I²C Summary

I2C Bus	Type	Typical Usage
I2C1	Target	Connect to a host controller. May be used for updating flash memory. This I²C port has R/W access via the Host Interface.
I2C2	Controller	Connect to external DC/DC, USB Type-C mux, or other target devices.
I2C3	Target	For systems that require two I2C targets.

8.3.17.1 I²C Interface Hardware

The TPS26744E-Q1 features multiple I²C interfaces that each use an I²C I/O driver like the one shown below. This I/O consists of an open-drain output and an input comparator referenced to LDO_3V3 followed by de-glitching.

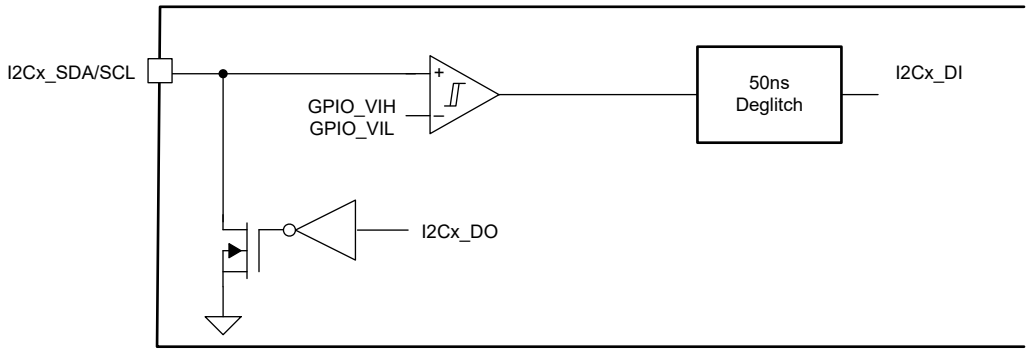

Figure 8-26. I²C Buffer

8.3.17.2 I²C Interface Description

The TPS26744E-Q1 supports Standard, Fast mode, and Fast-mode plus I²C interfaces. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A controller sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The controller sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to enable proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. The controller receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

Figure 8-27 shows the start and stop conditions of the transfer. Figure 8-28 shows the SDA and SCL signals for transferring a bit. Figure 8-29 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

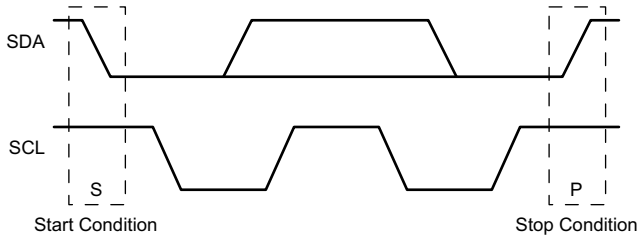

Figure 8-27. I²C Definition of Start and Stop Conditions

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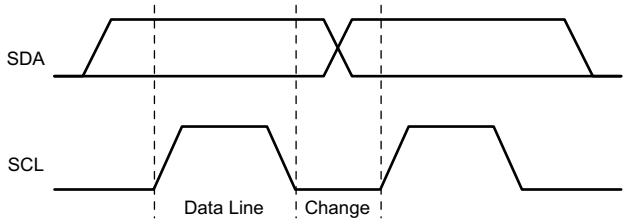


Figure 8-28. I²C Bit Transfer

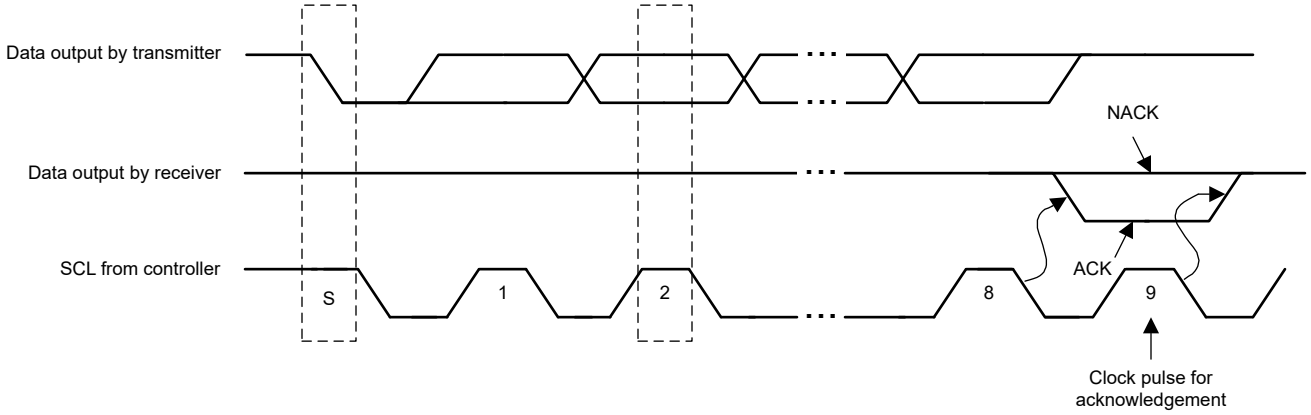


Figure 8-29. I²C Acknowledgment

8.3.17.3 I²C Clock Stretching

The TPS26744E-Q1 features clock stretching for the I²C protocol. The TPS26744E-Q1 target I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The controller communicating with the target must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the target is clock stretching, the clock line remains low.

The controller must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

8.3.17.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C controller and a single TPS26744E-Q1. The I²C target sub-address is used to receive or respond to Host Interface protocol commands. Figure 8-30 and Figure 8-31 show the write and read protocol for the I²C target interface, and a key is included in Figure 8-32 to explain the terminology used. The TPS26744E-Q1 Host interface utilizes a different unique address to identify each of the two USB Type-C ports controlled by the TPS26744E-Q1. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

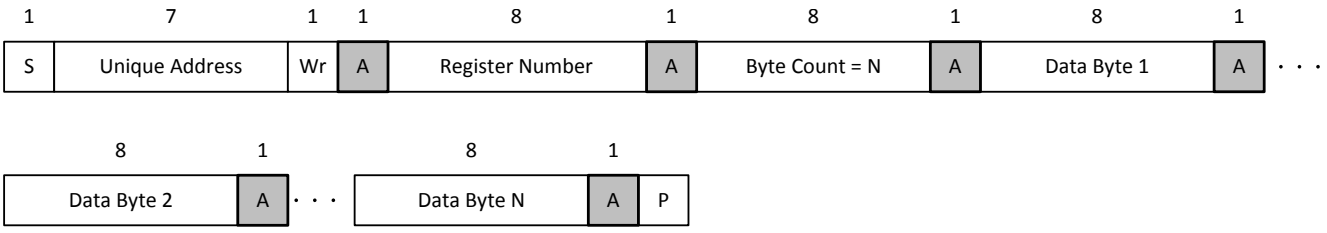


Figure 8-30. I²C Unique Address Write Register Protocol

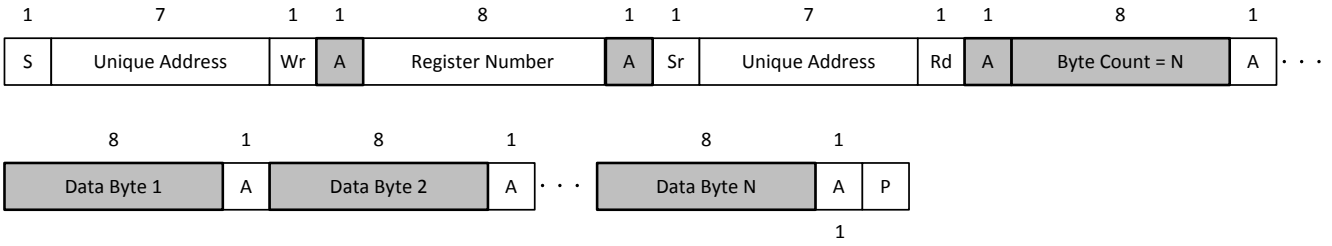
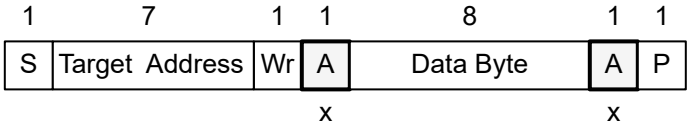


Figure 8-31. I²C Unique Address Read Register Protocol



S Start condition
SR Repeated start condition
Rd Read (bit value of 1)
Wr Write (bit value of 0
X Field is required to have the value x
A Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)
P Stop condition

Controller-to-target

Target-to-controller

• • • Continuation of protocol

Figure 8-32. I²C Read/Write Protocol Key

8.3.17.5 I²C Address Setting

When multiple TPS26744E-Q1 devices are used in the same system, the I2C1 bus of each device may be connected. This enables an external I²C controller to control both devices via only the I2C1 bus. Therefore, the target addresses of the I²C target ports are set to the default value based on the CONFIG pin as shown in the following table. See Section 8.4.1 for details about configuring the CONFIG pin to select the default target address.

These addresses are available during BOOT and can be used to update the flash memory.

Table 8-8. I2C Default Target Addresses (before loading configurations from flash)

I2C port	Port	Default Target Address (see I²C address index from CONFIG decoding)			
		CONFIG = #1	CONFIG = #2	CONFIG = #3	CONFIG = #4
I2C1 / I2C4	A	0x20	0x21	0x22	0x23
	B	0x24	0x25	0x26	0x27

8.3.18 System Power Management (SPM) Across Ports

The TPS26744E-Q1 can be connected to multiple other PD controllers to enable system power sharing across multiple ports. One of the TPS26744E-Q1 is configured as the Controller, and the other is configured as a Target. In the following diagram the I2C2 port from one device is connected to the I2C3 port from another device. Since the I2C2 is the controller port, it makes that device the Controller in the SPM context as well.

The SPM controller also handles power sharing for all ports within the SPM controller.

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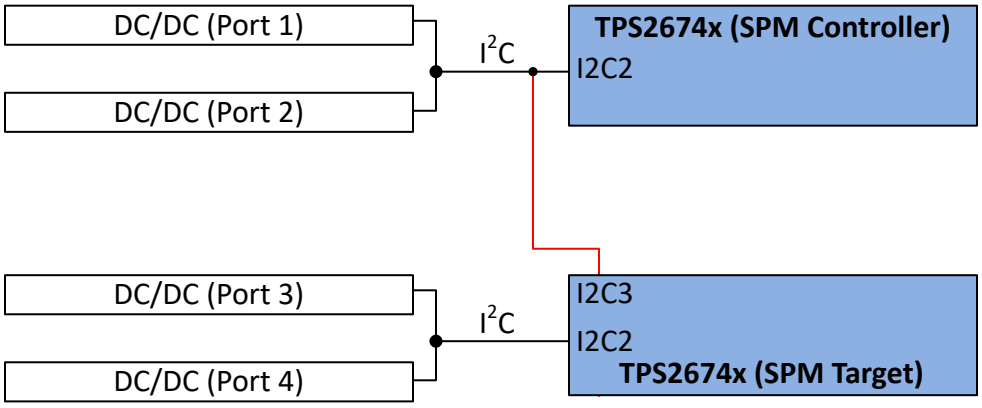


Figure 8-33. Illustration of Device-to-Device SPM

8.4 Device Functional Modes

8.4.1 Pin Strapping to Configure Default Behavior (CONFIG)

The CONFIG pin is used to configure the default I2C address index as summarized in the following table.

The UART_Tx pin function can be enabled on the CONFIG pin without affecting I2C1 address decoding. When transmitting, the UART_Tx pin function overdrives the external resistance.

Table 8-9. CONFIG decoding

R_{UP}	R_{DOWN}	CONFIG decoding	I^2C address index
∞	>500kΩ	00	#1
>500kΩ	∞	01	#2
< 5kΩ	∞	10	#3
∞	< 5kΩ	11	#4

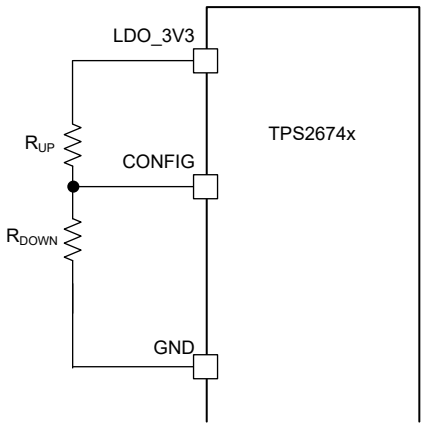


Figure 8-34. I2C_ADDR pin configuration.

8.4.2 Power States

The TPS26744E-Q1 may operate in one of four different power states: Active, Idle, Sleep or Shutdown. The functionality available in each state is summarized in the following table. The device automatically transitions between the power states based on the circuits that are active and required, see Figure 8-35. In the Sleep State the TPS26744E-Q1 detects a Type-C connection or other activity that requires moving to the Active state. Transitioning between the Active mode to the Idle mode requires a period of time (T) without any of the following activity:

- Incoming USB PD message
- Change in CC status
- GPIO input event
- I^2C transactions
- Voltage alert
- Fault alert

During boot mode, the TPS26744E-Q1 remains in the Active State.

In order to enter the Sleep State both ports must meet the state entry condition, that is, CC detached and no activity.

The Shutdown mode is entered when the ENSD pin is configured as active (which is the default at power-on) and the ENSD pin is pulled low. Entering the Shutdown mode overrides any other power state condition. It is important to note that the device is non-functional while in the Shutdown mode. The ENSD pin is configured by default at power-on so the device is non-functional if the ENSD pin is pulled low.

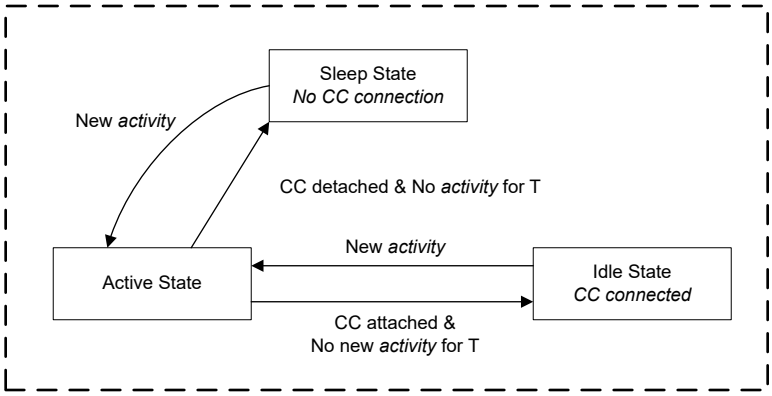


Figure 8-35. Flow Diagram For Power States

Table 8-10. Power Consumption States

	Active Mode $I_{IN,Act}$	Idle Mode $I_{IN,Idle}$	Sleep Mode $I_{IN,Sleep}$	Shutdown Mode
PA_VCONN	ON	OFF	OFF	OFF
PB_VCONN	ON	OFF	OFF	OFF
external PA_CCx termination	Rp	Rp	Rp	don't care
external PA_CCy termination	open	open	Rp	don't care
external PB_CCx termination	Rp	Rp	Rp	don't care
external PB_CCy termination	open	open	Rp	don't care
Liquid detection	ON, Px_LQD held low	OFF	OFF	OFF
USB-PD PHY	Transmitting on both ports	Squelch Rx enabled ready to wake on both ports	OFF	OFF
I2C traffic	I2C1, I2C2, I2C3, and I2C4 all active	No activity, monitoring for wake only	No activity, monitoring for wake only	don't care
CPU	Active, reading and writing to SRAM	Sleep	Sleep	Disabled
Flash	Actively executing from flash.	Inactive	Inactive	Inactive

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS26744E-Q1 firmware implements a host interface over I^2C to allow for the configuration and control of all device options. Initial device configuration is stored in flash and is loaded after the contents of flash are authenticated. The TPS26744E-Q1 configuration and host interface allow the device to be customized for each specific application. The configuration can be generated through the Application Customization GUI.

9.2 Typical Application

9.2.1 System Examples

The TPS26744E-Q1 supports USB-PD charging in the extended power range (EPR) for two USB-C ports.

The TPS26744E-Q1 also supports USB-PD messaging to enter into DisplayPort Alternate Mode. The TPS26744E-Q1 converts the hot-plug-detect (HPD) signal into USB-PD messages for a DisplayPort receiver system, or converts USB-PD messages into the hot-plug-detect (HPD) signal for a DisplayPort transmitting system. An external 5V source is required for the PP5V pin in DisplayPort systems in order to provide the necessary power to the USB-C cable via a CC pin (VCONN).

When a system has more than two USB-C ports, multiple TPS26744E-Q1 can be connected via I2C. One of the TPS26744E-Q1 acts as the System Power Mangement (SPM) controller, while the others act as targets.

If a system has an MCU, it may connect to I2C1 on the TPS26744E-Q1 in order to have access to monitor status and control certain behaviors and configurations.

The Px_LQD pins of the TPS26744E-Q1 may be connected to SBU1, SBU2, D+ or D- on the USB-C receptacle. When configured this allows the TPS26744E-Q1 to detect liquids and implement corrosion mitigation and protect the USB-C connector.

9.2.1.1 Dual-Port with DisplayPort

The diagram below illustrates how TPS26744E-Q1 can be used in a 2-port DisplayPort-capable system. The TPS26744E-Q1 uses I2C2 to control external DC/DCs to provide the necessary voltage and/or current on each port individually. Since DisplayPort requires high-power VCONN an external 5V supply is connected to the PP5V in this system example.

The TPS26744E-Q1 hot-plug-detect (HPD) signal interfaces with the DisplayPort system.

External OVP solutions are shown to protect Px_CCy, Px_DP/DM, and Px_LQD pins from shorting to VBUS in the connector.

Port A in the following figure does not have a voltage divider on VBUS, while Port B does have a VBUS voltage divider. The external OVP is not needed on Port A because of the lower maximum nominal voltage.

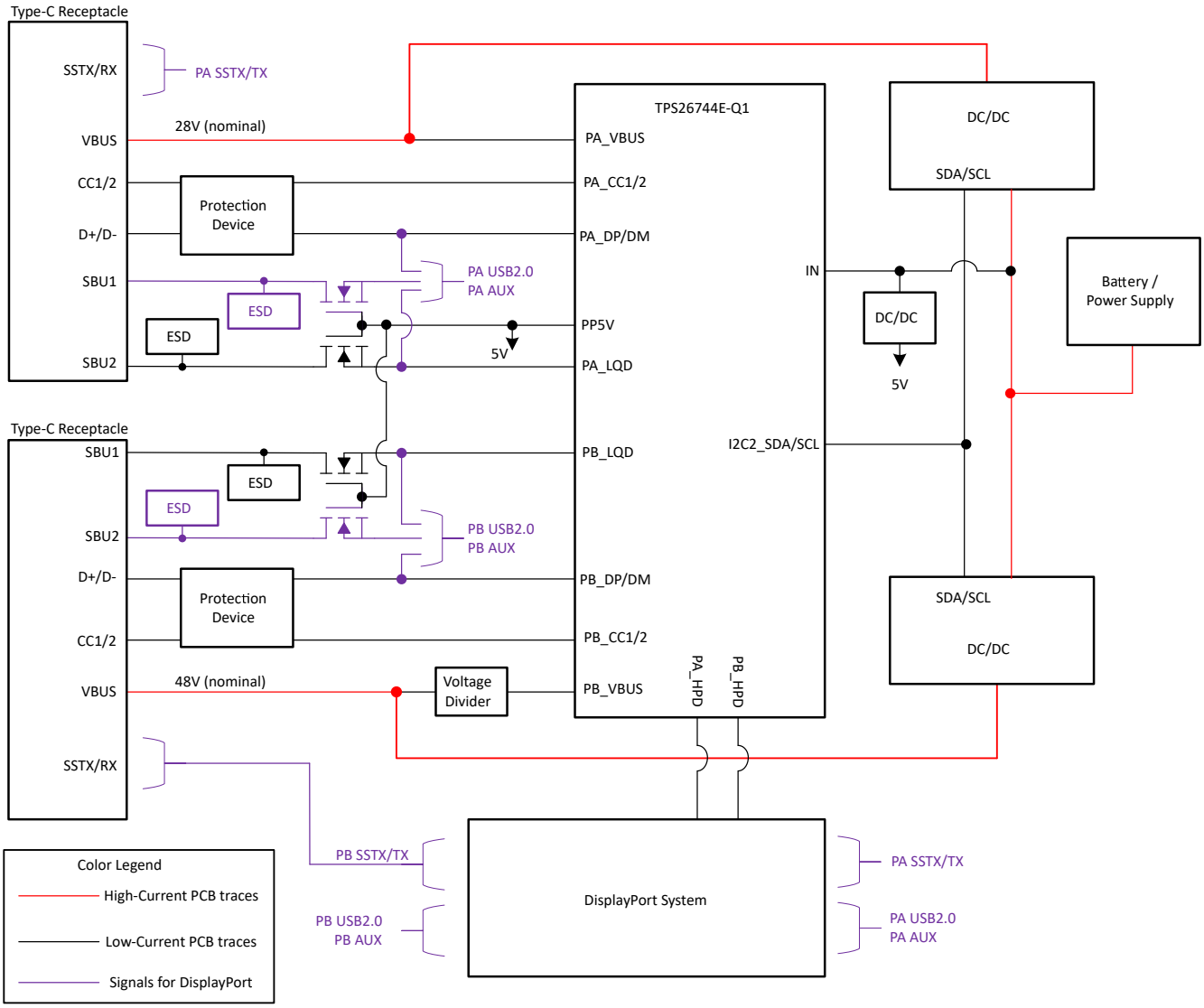


Figure 9-1. Dual-Port EPR Charger With DisplayPort

ADVANCE INFORMATION

9.3 Power Supply Recommendations

9.3.1 Input Power Supply

The IN pin is the primary power input for the device. An internal 5V LDO takes IN as an input to create 5V on the PP5V pin. However, in some systems an external 5V may be applied to the PP5V, in which case the IN pin may be shorted to the PP5V pin so that $V_{IN} \geq V_{PP5V}$. Connect the recommended capacitance C_{IN} from the IN pin to the GND pin. Place C_{IN} as close to the pin as possible. The IN pin is not be allowed to go below the voltage on the PP5V pin.

9.3.2 5V Power Supply

Some internal circuitry is powered from 5V. The 5V LDO steps the voltage down from IN to 5V. The 5V LDO provides power to the internal 3.3V LDO, as well as internal analog circuits including Px_VCONN in some cases. Connect the recommended capacitance C_{PP5V} from the PP5V pin to the GND pin, and as close to the PP5V pin as possible.

9.3.3 3.3V Power Supply

Some internal circuitry is powered from 3.3V. The 3.3V LDO steps the voltage down from PP5V to 3.3V. The 3.3V LDO provides power to the internal 1.35V LDO and other internal circuits. Connect the recommended capacitance C_{LDO_3V3} from the LDO_3V3 pin to the GND pin, and as close to the LDO_3V3 pin as possible.

9.3.4 1.35V Power Supply

Some internal circuitry is powered from 1.35V. The 1.35V LDO steps the voltage down from LDO_3V3 to 1.35V. The 1.35V LDO provides power to all internal low-voltage digital circuits which includes the digital core, and memory. Connect the recommended capacitance C_{LDO_1V35} from the LDO_1V35 pin to the GND pin, and as close to the LDO_1V35 pin as possible.

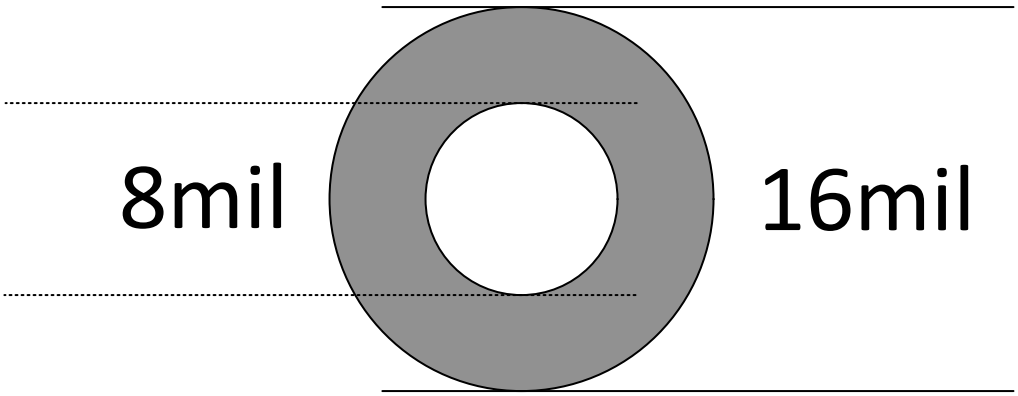
9.4 Layout

9.4.1 Layout Guidelines

Proper routing and placement maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. Best practice is to consult with board manufacturing to verify manufacturing capabilities.

Recommended Via Size

Recommended Via Size Proper via stitching is recommended to carrying current for the VBUS power paths and grounding. The recommended minimum via size is shown below, but larger vias are an option for low density PCB designs. A single via is capable of carrying 1A, verify the tolerance with the board manufacturing. Vias are recommended to be tented when located close to the PD controller.



ADVANCE INFORMATION

Minimum Trace Widths

Below are the minimum trace widths for analog and digital pins. The trace width limitations are also defined by the board manufacturing process used. Consult with manufacturing for determining the minimum trace widths and tolerance

Table 9-1. Minimum Trace Width

Route	Minimum Width (mils)
VIN, PP5V	10 (External Layers), 20 (Internal Layers)
PA_CC1, PA_CC2, PB_CC1, PB_CC2	10
LDO_1V35, LDO_3V3, PA_VBUS, PB_VBUS	10
P0_GPIOX/*, P1_GPOX/*	4 (Or Manufacturing Limit)
Component GND	16

9.4.2 Layout Example

Schematic

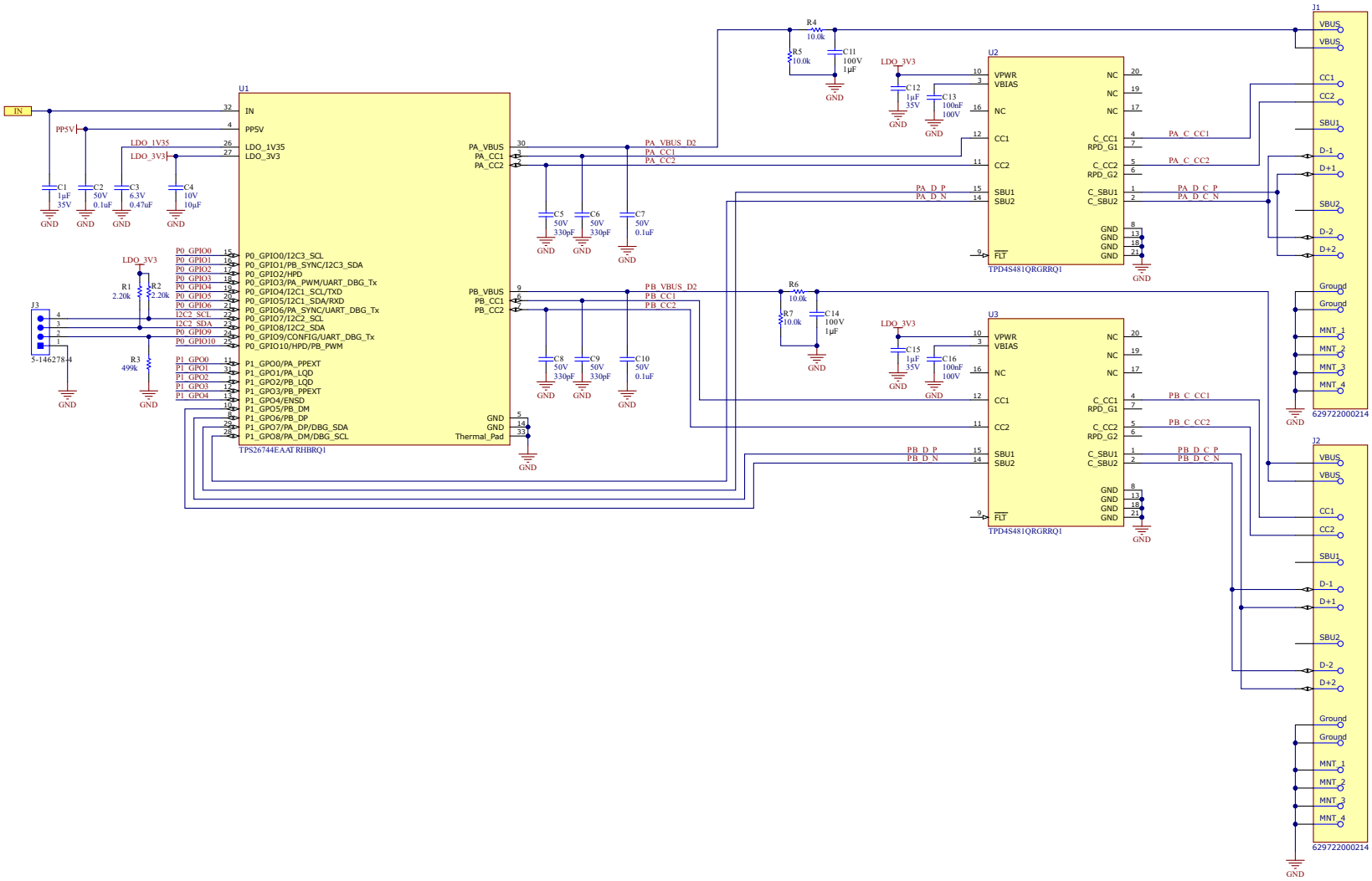
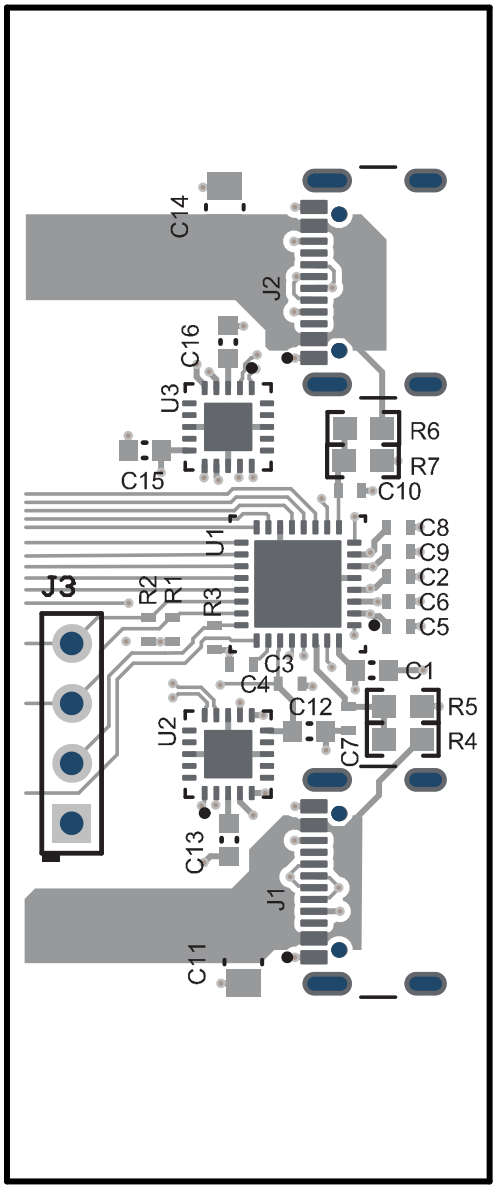
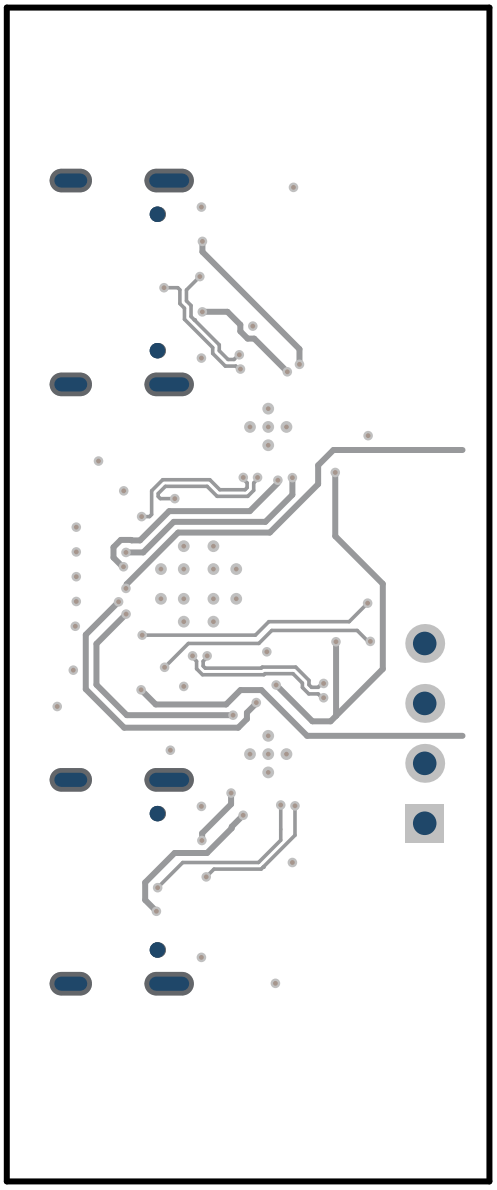


Figure 9-2. Reference Schematic

Table 9-2. Composite Views

Top Composite	Bottom Composite
	

ADVANCE INFORMATION

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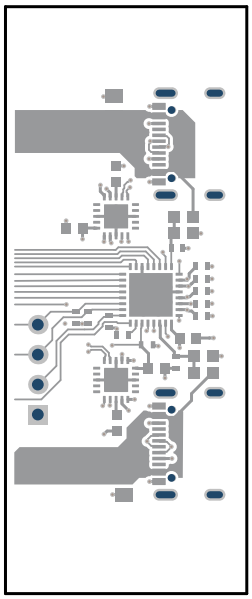
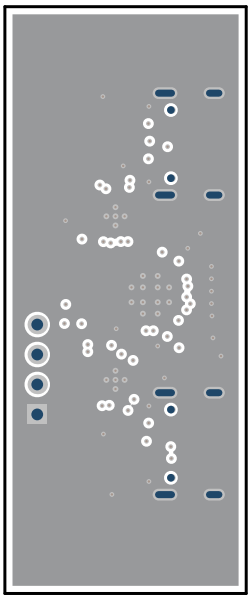
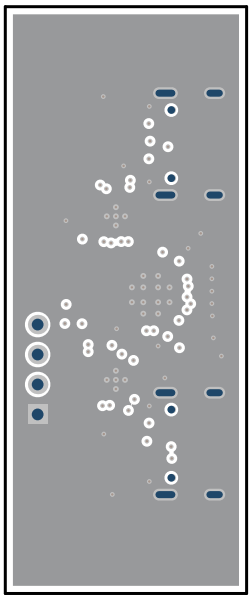
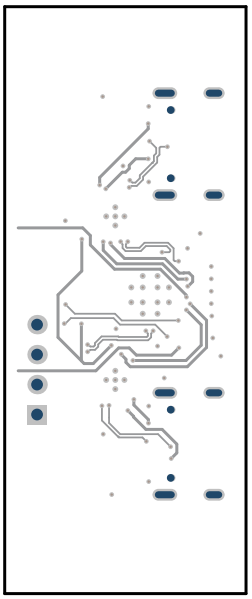
Table 9-3. Copper and Routing Layers

Top Layer 1	GND Layer 2	GND Layer 3	Bottom Layer 4
			

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

- *USB-PD Specifications*
- *USB Power Delivery Specification*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2025	*	Advance Information

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
P26744EAATRHBRQ1	PREVIEW	VQFN	RHB	32	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	–40 to 125	P26744E AA

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

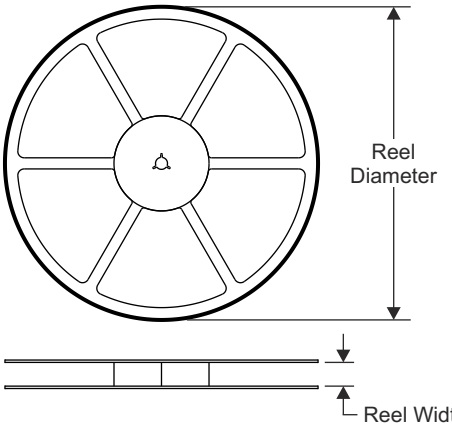
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

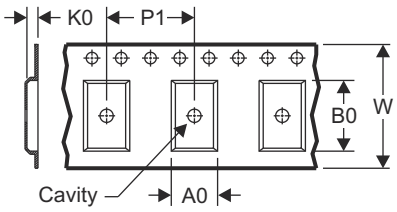
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

12.2 Tape and Reel Information

REEL DIMENSIONS

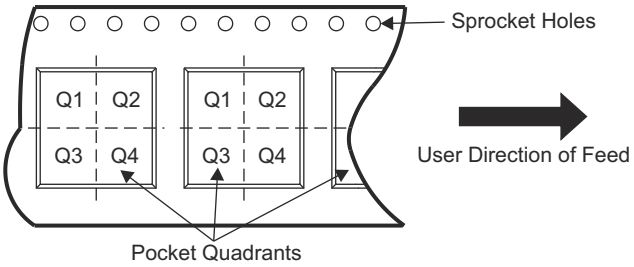


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

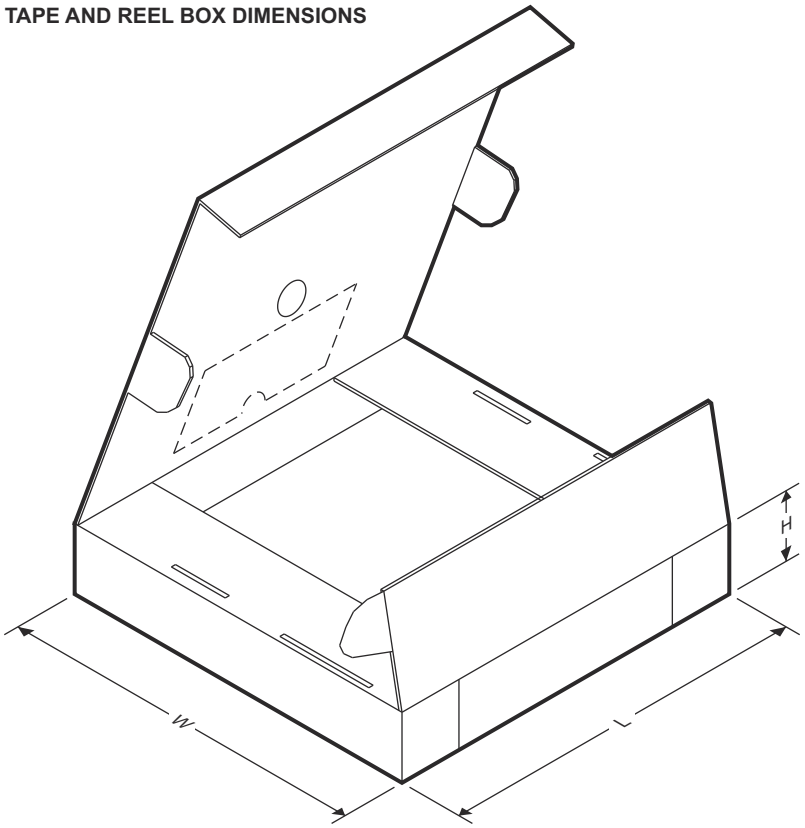
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
P26744EAATRHBRQ1	VQFN	RHB0032A A	32	5000	330	12.4	5.3	5.3	1.1	8	12	Q2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
P26744EAATRHBRQ1	VQFN	RHB0032AA	32	5000	5	5	1

ADVANCE INFORMATION

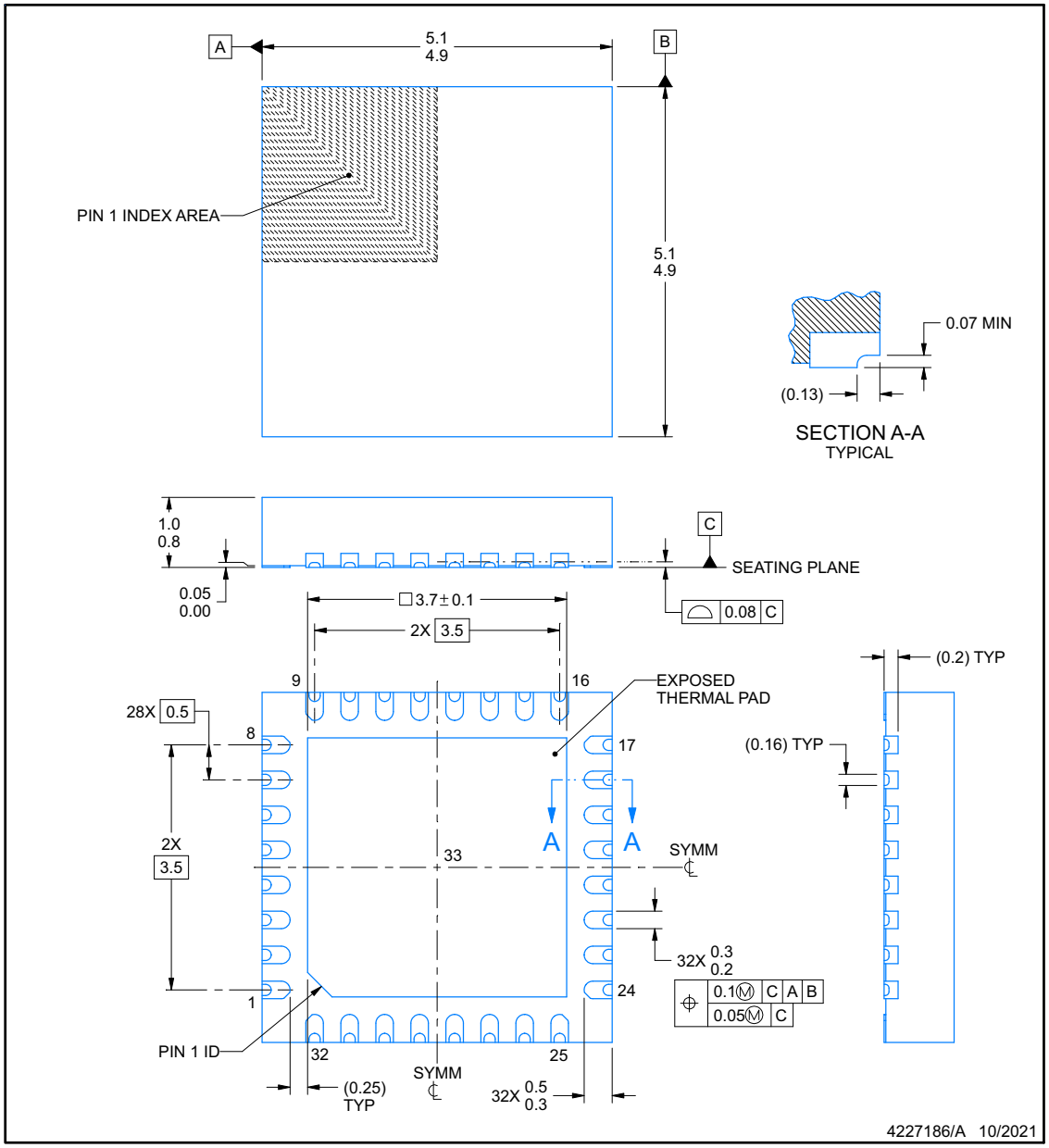
ADVANCE INFORMATION

PACKAGE OUTLINE

RHB0032AA

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

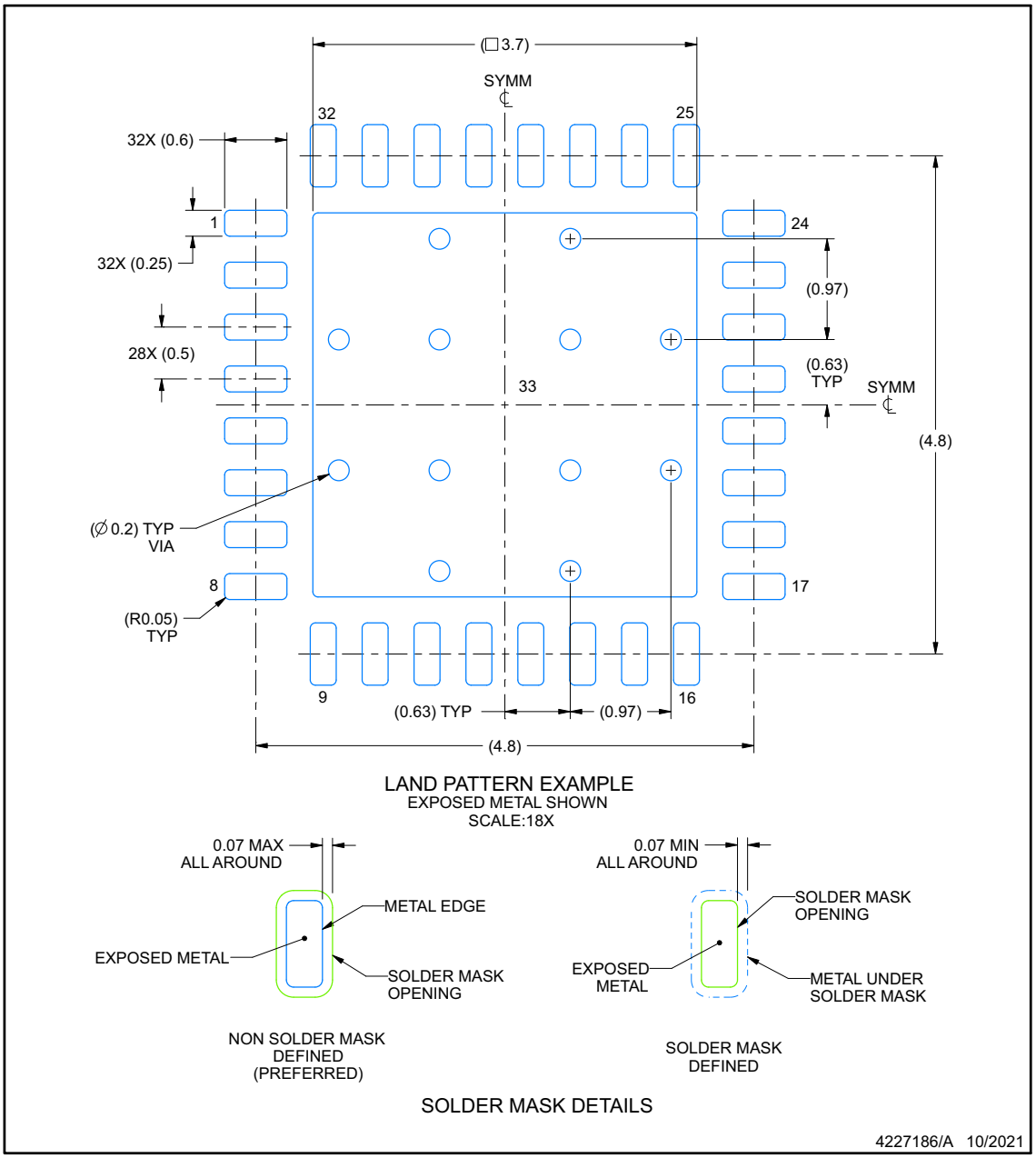
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032AA

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

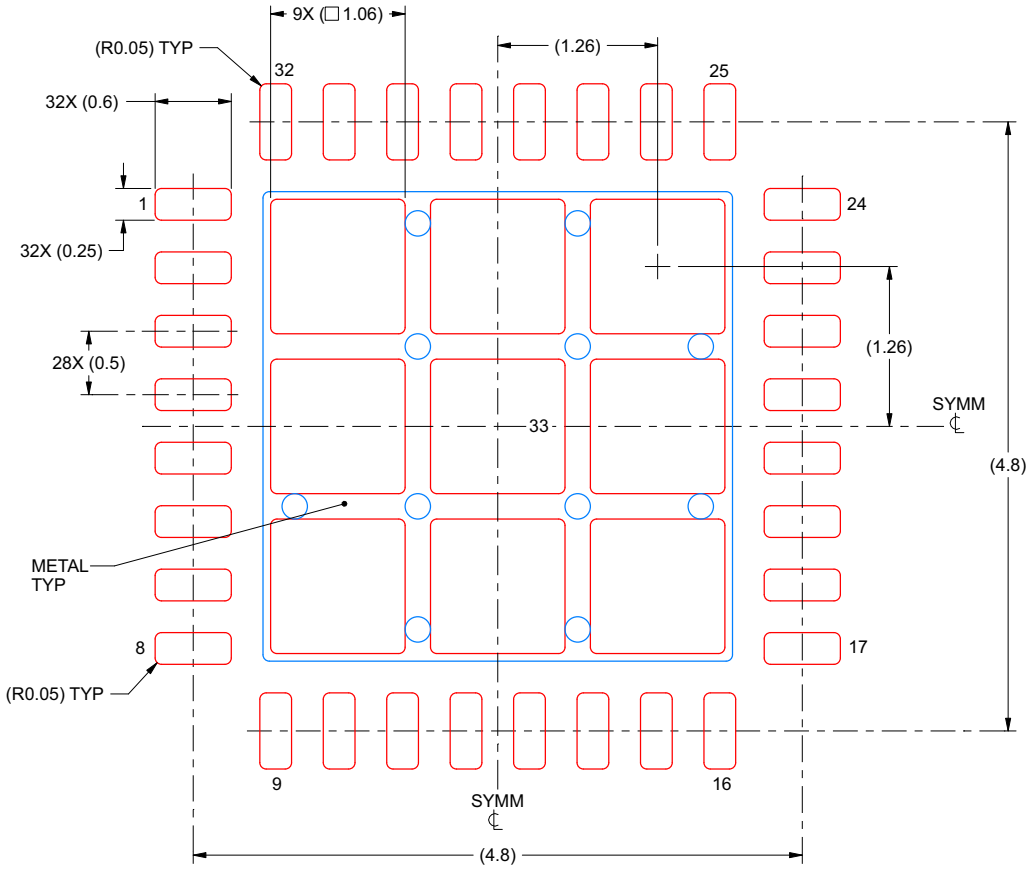
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RHB0032AA — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4227186/A 10/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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