# TPS23882 Type-3 2-Pair 8-Channel PoE 2 PSE Controller with SRAM and 200 mΩ $R_{SENSE}$

## 1 Features

- IEEE 802.3bt PSE solution for PoE 2 *Type-3 2-Pair* Power Over Ethernet applications
- Compatible with TI's *FirmPSE* system firmware
- *SRAM Programmable memory*
- Programmable power limiting accuracy ±3%
- 200-mΩ Current sense resistor
- Legacy PD capacitance measurement
- Selectable 2-pair port power allocations
  - 4 W, 7 W, 15.4 W, or 30 W
- Dedicated 14-bit integrating current ADC per port
  - Noise immune MPS for DC disconnect
  - 2% Current sensing accuracy
- 1- or 3-Bit fast port shutdown input
- Auto-class discovery and power measurement
- *Never Fooled* 4-Point detection
- Inrush and operational foldback protection
- 425-mA and 1.25-A Selectable current limits
- Port re-mapping
- 8-Bit or 16-bit I²C communication
- Flexible processor controlled operating modes
  - Auto, semi auto and manual / diagnostic
- Per Port voltage monitoring and telemetry
- –40°C to +125°C Temperature operation

## 2 Applications

- Video recorder (NVR, DVR, and so forth)
- Small business switch
- Campus and branch switches

## 3 Description

The TPS23882 is an 8-channel power sourcing equipment (PSE) controller engineered to insert power onto Ethernet cables in accordance with the IEEE 802.3bt standard. The PSE controller can detect powered devices (PDs) that have a valid signature, complete mutual identification, and apply power.

The TPS23882 improves on the TPS2388 with reduced current sense resistors, SRAM programmability, programmable power limiting, capacitance measurement, and compatibility with TI's *FirmPSE* system firmware (see *Device Comparison Table*).

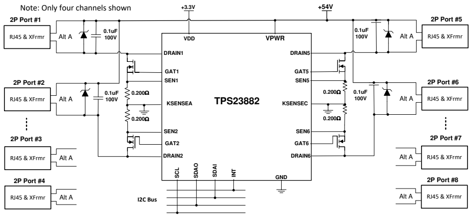
Programmable SRAM enables in-field firmware upgradability over I²C to ensure IEEE compliance and interoperability with the latest PoE enabled devices. Dedicated per port ADCs provide continuous port current monitoring and the ability to perform parallel classification measurements for faster port turn on times. A 1.25-A port current limit and adjustable power limiting allows for the support of non-standard applications above 60-W sourced. The 200-mΩ current sense resistor and external FET architecture allow designs to balance size, efficiency, thermal and solution cost requirements.

Port remapping and pin-to-pin compatibility with the TPS2388, TPS23880, and TPS23881 devices eases migration from previous generation PSE designs and enables interchangeable 2-layer PCB designs to accommodate different system PoE power configurations.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS23882 | VQFN (56) | 8.00 mm × 8.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Schematic**

## Table of Contents

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (May 2020) to Revision D (August 2020) | Page |
|---|---|
| • Updated the numbering format for tables, figures and cross-references throughout the document | 1 |

| Changes from Revision B (October 2019) to Revision C (May 2020) | Page |
|---|---|
| • Deleted Autonomous operation description throughout data sheet for clarification | 4 |
| • Changed Gate 1-8 MAX voltage from 12 to 13 V in the Absolute Maximum Ratings table | 7 |

| Changes from Revision A (September 2019) to Revision B (December 2019) | Page |
|---|---|
| • Fixed typo in device number on first page | 1 |

| Changes from Revision * (August 2019) to Revision A (September 2019) | Page |
|---|---|
| • Changed from Advance Information to Production Data | 1 |
| • First Public Release | 1 |

## 5 Device Comparison Table

Table 5-1 summarizes the primary differences between the available 2-Pair PSE devices.

| KEY FEATURES | TPS23880 | TPS23881 | TPS23882 |
|---|---|---|---|
| Compatible with TI's *FirmPSE* system firmware | N/A | Yes | Yes |
| Pin to Pin compatible | Yes | Yes | Yes |
| Number of PSE Channels | 8 | 8 | 8 |
| Supported IEEE 802.3 PSE Types | PoE 2<br>802.3bt Type 3 or 4<br>(2 or 4 Pair) | PoE 2<br>802.3bt Type 3 or 4<br>(2 or 4 Pair) | PoE 2<br>802.3bt Type 3 (2-Pair) |
| $R_{SENSE}$ | 0.255 Ω | 0.200 Ω | 0.200 Ω |
| 2-Pair $P_{CUT}$ programable ranges | 0.5 W to 54 W | 2 W to 65 W | 2 W to 65 W |
| 4-Pair $P_{CUT}$ programable ranges | 0.5 W to 108 W | 4 W to 127 W | N/A |
| 90+ W 4-pair $P_{CUT}$ accuracy | ±3.0 % | ±2.5 % | N/A |
| Channel capacitance measurement range | N/A | 1 µF to 12 µF | 1 µF to 12 µF |
| ULA Packaging | No | Yes (TPS23881A) | N/A |
| $I^2C$ Programmable SRAM Memory | 16 kB | 16 kB | 16 kB |

**Table 5-1. 2-Pair PSE Key Feature Comparisons**

| KEY FEATURES | TPS23861 | TPS2388 | TPS23881 | TPS23882 |
|---|---|---|---|---|
| Compatible with TI's *FirmPSE* system firmware | N/A | N/A | Yes | Yes |
| Pin to Pin compatible | N/A | Yes | Yes | Yes |
| Number of PSE Channels | 4 | 8 | 8 | 8 |
| Supported IEEE 802.3 PSE Types | PoE 1<br>802.3at Type 1 or 2 | PoE 1<br>802.3at Type 1 or 2 | PoE 2<br>802.3bt Type 3 or 4<br>(2 or 4 Pair) | PoE 2<br>802.3bt Type 3 (2-Pair) |
| $R_{SENSE}$ | 0.255 Ω | 0.255 Ω | 0.200 Ω | 0.200 Ω |
| 2-Pair $P_{CUT}$ programable ranges | N/A<br>$I_{CUT}$ adjustable up to 920 mA | N/A<br>$I_{CUT}$ adjustable up to 920 mA | 2 W to 65 W | 2 W to 65 W |
| $T_{MPS}$ | 15 ms | 15 ms | 3 ms | 3 ms |
| Port Current Limit (1x / 2x) | 425 mA / 1060 mA | 425 mA / 1060 mA | 425 mA / 1250 mA | 425 mA / 1250 mA |
| Channel capacitance measurement range | N/A | N/A | 1 µF to 12 µF | 1 µF to 12 µF |
| PD Autoclass Discovery and Power Measurement | N/A | N/A | Yes | Yes |
| $I^2C$ Programmable SRAM Memory | N/A | N/A | 16 kB | 16 kB |

# 6 Pin Configuration and Functions

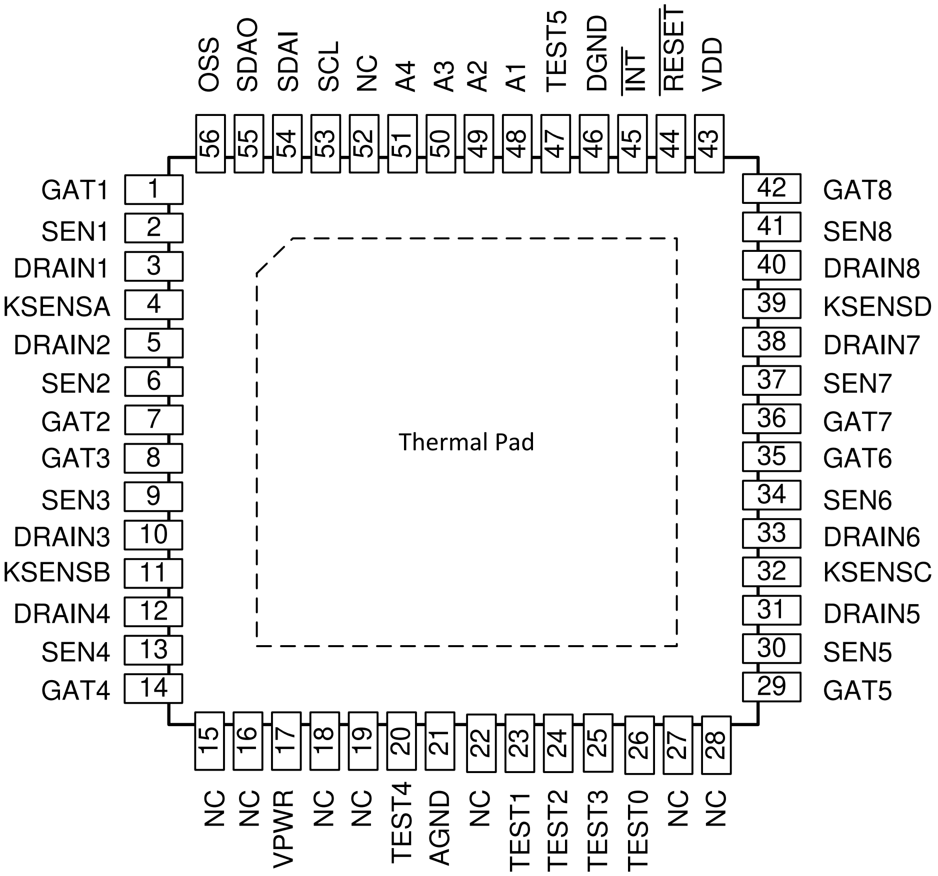

**Figure 6-1. RTQ Package With Exposed Thermal Pad 56-Pin VQFN Top View**

## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| A1-4 | 48–51 | I | $I^2C$ A1-A4 address lines. These pins are internally pulled up to VDD. |
| AGND | 21 | — | Analog ground. Connect to GND plane and exposed thermal pad. |
| DGND | 46 | — | Digital ground. Connect to GND plane and exposed thermal pad. |
| DRAIN1-8 | 3, 5, 10, 12, 31, 33, 38, 40 | I | Channel 1-8 output voltage monitor. |
| GAT1-8 | 1, 7, 8, 14, 29, 35, 36, 42 | O | Channel 1-8 gate drive output. |
| $\overline{\text{INT}}$ | 45 | O | Interrupt output. This pin asserts low when a bit in the interrupt register is asserted. This output is open-drain. |
| KSENSA/B | 4, 11 | I | Kelvin point connection for SEN1-4 |
| KSENSC/D | 32, 39 | I | Kelvin point connection for SEN5-8 |
| NC | 15, 16, 18, 19 | O | No connect pins. These pins are internally biased at 1/3 and 2/3 of VPWR in order to control the voltage gradient from VPWR. Leave open. |
| | 22, 27, 28, 52 | — | No connect pin. Leave open. |
| OSS | 56 | I | Channel 1-8 fast shutdown. This pin is internally pulled down to DGND. |
| $\overline{\text{RESET}}$ | 44 | I | Reset input. When asserted low, the TPS23882 is reset. This pin is internally pulled up to VDD. |
| SCL | 53 | I | Serial clock input for $I^2C$ bus. |
| SDAI | 54 | I | Serial data input for $I^2C$ bus. This pin can be connected to SDAO for non-isolated systems. |
| SDAO | 55 | O | Serial data output for $I^2C$ bus. This pin can be connected to SDAI for non-isolated systems. This output is open-drain. |
| SEN1-8 | 2, 6, 9, 13, 30, 34, 37, 41 | I | Channel 1-8 current sense input. |
| TEST0-5 | 20, 23, 24, 25, 26, 47 | I/O | Used internally for test purposes only. Leave open. |
| Thermal pad | — | — | The DGND and AGND terminals must be connected to the exposed thermal pad for proper operation. |
| VDD | 43 | — | Digital supply. Bypass with 0.1 µF to DGND pin. |
| VPWR | 17 | — | Analog 54-V positive supply. Bypass with 0.1 µF to AGND pin. |

## 6.1 Detailed Pin Description

The following descriptions refer to the pinout and the functional block diagram.

**DRAIN1-DRAIN8:** Channels 1-8 output voltage monitor and detect sense. Used to measure the port output voltage, for port voltage monitoring, port power good detection and foldback action. Detection probe currents also flow into this pin.

The TPS23882uses an innovative 4-point technique to provide reliable PD detection and avoids powering an invalid load. The discovery is performed by sinking two different current levels via the DRAINn pin, while the PD voltage is measured from VPWR to DRAINn. If prior to starting a new detection cycle the port voltage is >2.5 V, an internal 100-kΩ resistor is connected in parallel with the port and a 400-ms detect backoff period is applied to allow the port capacitor to be discharged before the detection cycle starts.

There is an internal resistor between each DRAINn pin and VPWR in any operating mode except during detection or while the port is ON. If the port n is not used, DRAINn can be left floating or tied to GND.

**GAT1-GAT8:** Channels 1-8 gate drive outputs are used for external N-channel MOSFET gate control. At port turn on, it is driven positive by a low current source to turn the MOSFET on. GATn is pulled low whenever any of the input supplies are low or if an overcurrent timeout has occurred. GATn is also pulled low if the port is turned off by use of manual shutdown inputs. Leave floating if unused.

For improved design robustness, the current foldback functions limit the power dissipation of the MOSFET during low resistance load or short-circuit events and during the inrush period at port turn on. There is also fast overload protection comparator for major faults like a direct short that forces the MOSFET to turn off in less than a microsecond.

The circuit leakage paths between the GATn pin and any nearby DRAINn pin, GND or Kelvin point connection must be minimized (< 250 nA), to ensure correct MOSFET control.

**$\overline{\text{INT}}$:** This interrupt output pin asserts low when a bit in the interrupt register is asserted. This output is open-drain.

**KSENSA, KSENSB, KSENSC, KSENSD:** Kelvin point connection used to perform a differential voltage measurement across the associated current sense resistors.

Each KSENS is shared between two neighbor SEN pins as following: KSENSA with SEN1 and SEN2, KSENSB with SEN3 and SEN4, KSENSC with SEN5 and SEN6, KSENSD with SEN7 and SEN8. To optimize the measurement accuracy, ensure proper PCB layout practices are followed.

**OSS:** Fast shutdown, active high. This pin is internally pulled down to DGND, with an internal 1-µs to 5-µs deglitch filter.

The turn off procedure is similar to a port reset using Reset command (1Ah register). The 3-bit OSS function allows for a series of pulses on the OSS pin to turn off individual or multiple ports with up to 8 levels of priority.

**$\overline{\text{RESET}}$:** Reset input, active low. When asserted, the TPS23882 resets, turning off all ports and forcing the registers to their power-up state. This pin is internally pulled up to VDD, with internal 1-µs to 5-µs deglitch filter. The designer can use an external RC network to delay the turn-on. There is also an internal power-on-reset which is independent of the $\overline{\text{RESET}}$ input.

**SCL:** Serial clock input for I$^2$C bus.

**SDAI:** Serial data input for I$^2$C bus. This pin can be connected to SDAO for non-isolated systems.

**SDAO:** Open-drain I$^2$C bus output data line. Requires an external resistive pull-up. The TPS23882 uses separate SDAO and SDAI lines to allow optoisolated I$^2$C interface. SDAO can be connected to SDAI for non-isolated systems.

**A4-A1:** I$^2$C bus address inputs. These pins are internally pulled up to VDD. See *Section 9.6.2.13* for more details.

**SEN1-8:** Channel current sense input relative to KSENSn (see KSENSn description). A differential measurement is performed using KSENSA-D Kelvin point connection. Monitors the external MOSFET current by use of a 0.200-Ω current sense resistor connected to GND. Used by current foldback engine and also during classification. Can be used to perform load current monitoring via ADC conversion.

When the TPS23882 performs the classification measurements, the current flows through the external MOSFETs. This avoids heat concentration in the device and makes it possible for the TPS23882 to perform classification measurements on multiple ports at the same time. For the current limit with foldback function, there is an internal 2-µS analog filter on the SEN1-8 pins to provide glitch filtering. For measurements through an ADC, an anti-aliasing filter is present on the SEN1-8 pins. This includes the port-powered current monitoring, port policing, and DC disconnect.

If the port is not used, tie SENn to GND.

**VDD:** 3.3-V logic power supply input.

**VPWR:** High voltage power supply input. Nominally 54 V.

**AGND and DGND:** Ground references for internal analog and digital circuitry respectively. Not connected together internally. Both pins require a low resistance path to the system GND plane. If a robust GND plane is used to extract heat from the device's thermal pad, these pins may be connected together through the thermal pad connection on the pcb.

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | VPWR | –0.3 | 70 | V |
| | VDD | –0.3 | 4 | V |
| | OSS, RESET, A1-A4 | –0.3 | 4 | V |
| | SDAI, SDAO, SCL, INT | –0.3 | 4 | V |
| | SEN1-8, KSENSA, KSENSB, KSENSC, KSENSD | –0.3 | 3 | V |
| | GATE1-8 | –0.3 | 13 | V |
| | DRAIN1-8 | –0.3 | 70 | V |
| | AGND-GDND | –0.3 | 0.3 | V |
| Sink Current | INT, SDA | | 20 | mA |
| Lead Temperature 1/6mm from case for 10 seconds | | | 260 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under*Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2) | ± 500 | |

(1) JEDEC documentJEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC documentJEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{VDD}$ | | 3 | 3.3 | 3.6 | V |
| $V_{VPWR}$ | | 44 | 54 | 57 | V |
| | Voltage Slew rate on VPWR | | | 1 | V/µs |
| $f_{SCL}$ | $I^2C$ Clock Frequency | | | 400 | kHz |
| $T_J$ | Junction temperature | –40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | TPS23882 | UNIT |
|---|---|---|---|
| | | RTQ Package (VQFN) | |
| | | 56 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 25.3 | °C/W |
| $R_{θJC(top)}$ | Junction-to-case (top) thermal resistance | 9.7 | °C/W |
| $R_{θJB}$ | Junction-to-board thermal resistance | 3.7 | °C/W |
| $Ψ_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $Ψ_{JB}$ | Junction-to-board characterization parameter | 3.7 | °C/W |
| $R_{θJC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 7.5 Electrical Characteristics

Conditions are –40 < $T_J$ < 125 °C unless otherwise noted.$V_{VDD}$ = 3.3 V,$V_{VPWR}$ = 54 V, $V_{DGND}$ = $V_{AGND}$,DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, 2xFBn =0. Positive currents are into pins. $R_S$ = 0.200 Ω, to KSENSA (SEN1 orSEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY VPWR** | | | | | | |
| $I_{VPWR}$ | VPWR Current consumption | VVPWR = 54 V | | 10 | 12.5 | mA |
| $V_{UVLOPW\_F}$ | VPWR UVLO falling threshold | Check internal oscillator stops operating | 14.5 | | 17.5 | V |
| $V_{UVLOPW\_R}$ | VPWR UVLO rising threshold | | 15.5 | | 18.5 | V |
| $V_{PUV\_F}$ | VPWR Undervoltage falling threshold | VPUV threshold | 25 | 26.5 | 28 | V |
| **INPUT SUPPLY VDD** | | | | | | |
| $I_{VDD}$ | VDD Current consumption | | | 6 | 12 | mA |
| $V_{UVDD\_F}$ | VDD UVLO falling threshold | For channel deassertion | 2.1 | 2.25 | 2.4 | V |
| $V_{UVDD\_R}$ | VDD UVLO rising threshold | | 2.45 | 2.6 | 2.75 | V |
| $V_{UVDD\_HYS}$ | Hysteresis VDD UVLO | | | 0.35 | | V |
| $V_{UVW\_F}$ | VDD UVLO warning threshold | VDD falling | 2.6 | 2.8 | 3 | V |
| **A/D CONVERTERS** | | | | | | |
| $T_{CONV\_I}$ | Conversion time | All ranges, each channel | 0.64 | 0.8 | 0.96 | ms |
| $T_{CONV\_V}$ | Conversiontime | All ranges, each channel | 0.82 | 1.03 | 1.2 | ms |
| $T_{INT\_CUR}$ | Integration time, Current | Each channel, channel ON current | 82 | 102 | 122 | ms |
| $T_{INT\_DET}$ | Integration time, Detection | | 13.1 | 16.6 | 20 | ms |
| $T_{INT\_channelV}$ | Integration time, Channel Voltage | channel powered | 3.25 | 4.12 | 4.9 | ms |
| $T_{INT\_inV}$ | Integration time, Input Voltage | | 3.25 | 4.12 | 4.9 | ms |
| | Input voltage conversion scale factor and accuracy | VVPWR = 57 V | 15175 | 15565 | 15955 | Counts |
| | | | 55.57 | 57 | 58.43 | V |
| | | VVPWR = 44 V | 11713 | 12015 | 12316 | Counts |
| | | | 42.89 | 44 | 45.10 | V |
| | Powered Channel voltage conversion scale factor and accuracy | VVPWR - VDRAINn = 57 V | 15175 | 15565 | 15955 | Counts |
| | | | 55.57 | 57 | 58.43 | V |
| | | VVPWR - VDRAINn = 44 V | 11713 | 12015 | 12316 | Counts |
| | | | 42.89 | 44 | 45.10 | V |
| $\delta V/V_{Channel}$ | Voltage reading accuracy | | –2.5 | | 2.5 | % |
| | Powered Channel current conversion scale factor and accuracy | Channel current = 770 mA | 8431 | 8604 | 8776 | Counts |
| | | | 754.5 | 770 | 785.4 | mA |
| | | Channel Current = 100 mA | 1084 | 1118 | 1152 | Counts |
| | | | 97 | 100 | 103 | mA |
| $\delta I/I_{Channel}$ | Current reading accuracy | Channel Current =100 mA | –3 | | 3 | % |
| | | Channel Current =770 mA | –2 | | 2 | |
| $\delta R/R_{Channel}$ | Resistance reading accuracy | 15 kΩ ≤ $R_{Channel}$ ≤ 33 kΩ, $C_{Channel}$ ≤ 0.25 µF | –7 | | 7 | % |
| $I_{bias}$ | Sense Pin bias current | Channel ON or during class | –2.5 | | 0 | µA |

## 7.5 Electrical Characteristics (continued)

Conditions are –40 < $T_J$ < 125 °C unless otherwise noted.$V_{VDD}$ = 3.3 V,$V_{VPWR}$ = 54 V, $V_{DGND}$ = $V_{AGND}$,DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, 2xFBn =0. Positive currents are into pins. $R_S$ = 0.200 Ω, to KSENSA (SEN1 orSEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **GATE 1-8** | | | | | | |
| $V_{GOH}$ | Gate drive voltage | $V_{GATEn}$ , $I_{GATE}$ = -1 µA | 10 | | 12.5 | V |
| $I_{GO-}$ | Gate sinking current with Power-on Reset, OSS detected or channel turnoff command | $V_{GATEn}$ = 5 V | 60 | 100 | 190 | mA |
| $I_{GO\ short-}$ | Gate sinking current with channel short-circuit | $V_{GATEn}$ = 5 V,<br>$V_{SENn}$ ≥ $V_{short}$ (or $V_{short2X}$ if 2X mode) | 60 | 100 | 190 | mA |
| $I_{GO+}$ | Gate sourcing current | $V_{GATEn}$ = 0 V, default selection | 39 | 50 | 63 | µA |
| $t_{D\_off\_OSS}$ | Gate turnoff time from 1-bit OSS input | From OSS to VGATEn < 1 V, VSENn = 0 V, MbitPrty = 0 | 1 | | 5 | µs |
| $t_{OSS\_OFF}$ | Gate turnoff time from 3-bit OSS input | From Start bit falling edge to VGATEn < 1 V, VSENn = 0 V, MbitPrty = 1 | 72 | | 104 | µs |
| $t_{P\_off\_CMD}$ | Gate turnoff time from channel turnoff command | From Channel off command (POFFn = 1) to $V_{GATEn}$ < 1 V, $V_{SENn}$ = 0 V | | | 300 | µs |
| $t_{P\_off\_RST}$ | Gate turnoff time with /RESET | From /RESET low to $V_{GATEn}$ < 1 V, $V_{SENn}$ = 0 V | 1 | | 5 | µs |
| **DRAIN 1-8** | | | | | | |
| $V_{PGT}$ | Power-Good threshold | Measured at $V_{DRAINn}$ | 1 | 2.13 | 3 | V |
| $V_{SHT}$ | Shorted FET threshold | Measured at $V_{DRAINn}$ | 4 | 6 | 8 | V |
| $R_{DRAIN}$ | Resistance from DRAINn to VPWR | Any operating mode except during detection or while the Channel is ON, including in device RESET state | 80 | 100 | 190 | kΩ |
| **AUTOCLASS** | | | | | | |
| $t_{Class\_ACS}$ | Start of Autoclass Detection | Measured from the start of Class | 90 | | 100 | ms |
| $t_{AUTO\_PSE1}$ | Start of Autoclass Power Measurement | Measured from the end of Inrush | 1.4 | | 1.6 | s |
| | | Measured from setting the MACx bit while channel is already powered | | | 10 | ms |
| $t_{AUTO}$ | Duration of Autoclass Power Measurement | | 1.7 | 1.8 | 1.9 | s |
| $t_{AUTO\_window}$ | Autoclass Power Measurement Sliding Window | | 0.15 | | 0.3 | s |
| $P_{AC}$ | Autoclass Channel Power conversion scale factor and accuracy | VPWR = 52 V, VDRAINn = 0 V, Channel current = 770 mA | 76 | 80 | 84 | Counts |
| | | VPWR = 50 V, VDRAINn = 0 V, Channel current = 100 mA | 9 | 10 | 11 | |

## 7.5 Electrical Characteristics (continued)

Conditions are –40 < $T_J$ < 125 °C unless otherwise noted.$V_{VDD}$ = 3.3 V,$V_{VPWR}$ = 54 V, $V_{DGND}$ = $V_{AGND}$,DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, 2xFBn =0. Positive currents are into pins. $R_S$ = 0.200 Ω, to KSENSA (SEN1 orSEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DETECTION** | | | | | | |
| $I_{DISC}$ | Detection current | First and 3rd detection points VVPWR - VDRAINn = 0 V | 145 | 160 | 190 | µA |
| | | 2nd and 4th detection points VVPWR - VDRAINn = 0 V | 235 | 270 | 300 | |
| $\Delta I_{DISC}$ | 2nd – 1st detection currents | VVPWR - VDRAINn = 0 V | 98 | 110 | 118 | µA |
| $V_{det\_open}$ | Open circuit detection voltage | Measured as VVPWR - VDRAINn | 23.5 | 26 | 29 | V |
| $R_{REJ\_LOW}$ | Rejected resistance low range | | 0.86 | | 15 | kΩ |
| $R_{REJ\_HI}$ | Rejected resistance high range | | 33 | | 100 | kΩ |
| $R_{ACCEPT}$ | Accepted resistance range | | 19 | 25 | 26.5 | kΩ |
| $R_{SHORT}$ | Shorted Channel threshold | | | | 360 | Ω |
| $R_{OPEN}$ | Open Channel Threshold | | 400 | | | kΩ |
| $t_{DET}$ | Detection Duration | Time to complete a detection | 275 | 350 | 425 | ms |
| $t_{DET\_BOFF}$ | Detect backoff pause between discovery attempts | VVPWR - VDRAINn > 2.5 V | 300 | 400 | 500 | ms |
| | | VVPWR - VDRAINn < 2.5 V | 20 | | 100 | ms |
| $t_{DET\_DLY}$ | Detection delay | From command or PD attachment to Channel detection complete | | | 590 | ms |
| | Capacitance Measurement | Cport = 10uF | 8.5 | 10 | 11.5 | uF |
| **CLASSIFICATION** | | | | | | |
| $V_{CLASS}$ | Classification Voltage | VVPWR - VDRAINn, VSENn ≥ 0 mV $I_{channel}$ ≥ 180 µA | 15.5 | 18.5 | 20.5 | V |
| $I_{CLASS\_Lim}$ | Classification Current Limit | VVPWR - VDRAINn = 0 V | 65 | 75 | 90 | mA |
| $I_{CLASS\_TH}$ | Classification Threshold Current | Class 0-1 | 5 | | 8 | mA |
| | | Class 1-2 | 13 | | 16 | mA |
| | | Class 2-3 | 21 | | 25 | mA |
| | | Class 3-4 | 31 | | 35 | mA |
| | | Class 4-Class overcurrent | 45 | | 51 | mA |
| $t_{LCE}$ | Classification Duration (1st Finger) | From detection complete | 95 | | 105 | ms |
| $t_{CLE2/3}$ | Classification Duration (2nd & 3th Finger) | From Mark complete | 6.5 | | 12 | ms |
| **MARK** | | | | | | |
| $V_{MARK}$ | Mark Voltage | 4 mA ≥ $I_{Channel}$ ≥ 180 µA VVPWR - VDRAINn | 7 | | 10 | V |
| $I_{MARK\_Lim}$ | Mark Sinking Current Limit | VVPWR - VDRAINn = 0 V | 60 | 75 | 90 | mA |
| $t_{ME}$ | Mark Duration | | 6 | | 12 | ms |

## 7.5 Electrical Characteristics (continued)

Conditions are –40 < $T_J$ < 125 °C unless otherwise noted.$V_{VDD}$ = 3.3 V,$V_{VPWR}$ = 54 V, $V_{DGND}$ = $V_{AGND}$,DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, 2xFBn =0. Positive currents are into pins. $R_S$ = 0.200 Ω, to KSENSA (SEN1 orSEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC DISCONNECT** | | | | | | |
| $V_{IMIN}$ | DC disconnect threshold | | 0.8 | 1.3 | 1.8 | mV |
| $t_{MPDO}$ | PD Maintain Power signature dropout time limit | TMPDO = 00 | 320 | | 400 | ms |
| | | TMPDO = 01 | 75 | | 100 | ms |
| | | TMPDO = 10 | 150 | | 200 | ms |
| | | TMPDO = 11 | 600 | | 800 | ms |
| $t_{MPS}$ | PD Maintain Power Signature time for validity | | | 2.5 | 3 | ms |
| **PORT POWER POLICING** | | | | | | |
| $\delta P_{CUT}/P_{CUT}$ | PCUT tolerance | POL ≤ 15W | 0 | 5 | 10 | % |
| $\delta P_{CUT}/P_{CUT}$ | PCUT tolerance | 15W < POL < 60W | 0 | 3 | 6 | % |
| $t_{OVLD}$ | PCUT time limit | TOVLD = 00 | 50 | | 70 | ms |
| | | TOVLD = 01 | 25 | | 35 | |
| | | TOVLD = 10 | 100 | | 140 | |
| | | TOVLD = 11 | 200 | | 280 | |
| **PORT CURRENT INRUSH** | | | | | | |
| $V_{Inrush}$ | IInrush limit, ALTIRNn = 0 | VVPWR - VDRAINn = 1 V | 19 | 30 | 41 | mV |
| | | VVPWR - VDRAINn = 10 V | 19 | 30 | 41 | |
| | | VVPWR - VDRAINn = 15 V | 33 | 44 | 55 | |
| | | VVPWR - VDRAINn = 30 V | 80 | | 90 | |
| | | VVPWR - VDRAINn = 55 V | 80 | | 90 | |
| | IInrush limit, ALTIRNn = 1 | VVPWR - VDRAINn = 1 V | 19 | 30 | 41 | |
| | | VVPWR - VDRAINn = 10 V | 36 | 47 | 58 | |
| | | VVPWR - VDRAINn = 15 V | 53 | 64 | 75 | |
| | | VVPWR - VDRAINn = 30 V | 80 | | 90 | |
| | | VVPWR - VDRAINn = 55 V | 80 | | 90 | |
| $t_{START}$ | Maximum current limit duration in start-up | TSTART = 00 | 50 | | 70 | ms |
| | | TSTART = 01 | 25 | | 35 | |
| | | TSTART = 10 | 100 | | 140 | |

## 7.5 Electrical Characteristics (continued)

Conditions are –40 < $T_J$ < 125 °C unless otherwise noted.$V_{VDD}$ = 3.3 V,$V_{VPWR}$ = 54 V, $V_{DGND}$ = $V_{AGND}$,DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, 2xFBn =0. Positive currents are into pins. $R_S$ = 0.200 Ω, to KSENSA (SEN1 orSEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PORT CURRENT FOLDBACK** | | | | | | |
| $V_{LIM}$ | ILIM 1X limit, 2xFB = 0 and ALTFBn = 0 | VDRAINn = 1 V | 80 | | 90 | mV |
| | | VDRAINn = 15 V | 80 | | 90 | |
| | | VDRAINn = 30 V | 51 | 58 | 65 | |
| | | VDRAINn = 50 V | 23 | 30 | 37 | |
| | ILIM 1X limit, 2xFB = 0 and ALTFBn = 1 | VDRAINn = 1 V | 80 | | 90 | |
| | | VDRAINn = 25 V | 80 | | 90 | |
| | | VDRAINn = 40 V | 45 | 51 | 57 | |
| | | VDRAINn = 50 V | 23 | 30 | 37 | |
| $V_{LIM2X}$ | ILIM 2X limit, 2xFB = 1 and ALTFBn = 0 | VDRAINn = 1 V | 245 | 250 | 262 | mV |
| | | VDRAINn = 10 V | 164 | 180 | 196 | |
| | | VDRAINn = 30 V | 51 | 58 | 64 | |
| | | VDRAINn = 50 V | 23 | 30 | 37 | |
| | ILIM 2X limit, 2xFB = 1 and ALTFBn = 1 | VDRAINn = 1 V | 245 | 250 | 262 | |
| | | VDRAINn = 20 V | 139 | 147 | 155 | |
| | | VDRAINn = 40 V | 45 | 51 | 57 | |
| | | VDRAINn = 50 V | 23 | 30 | 37 | |
| $t_{LIM}$ | ILIM time limit | 2xFBn = 0 | 55 | 60 | 65 | ms |
| | 2xFBn = 1 | TLIM = 00 | 55 | 60 | 65 | |
| | | TLIM = 01 | 15 | 16 | 17 | |
| | | TLIM = 10 | 10 | 11 | 12 | |
| | | TLIM = 11 | 6 | 6.5 | 7 | |
| **SHORT CIRCUIT DETECTION** | | | | | | |
| $V_{short}$ | $I_{SHORT}$ threshold in 1X mode and during inrush | | 205 | | 245 | mV |
| $V_{short2X}$ | $I_{SHORT}$ threshold in 2X mode | | 280 | | 320 | |
| $t_{D\_off\_SEN}$ | Gate turnoff time from SENn input | 2xFBn = 0, VDRAINn = 1 V<br>From VSENn pulsed to 0.425 V. | | | 0.9 | µs |
| | | 2xFBn = 1, VDRAINn = 1 V<br>From VSENn pulsed to 0.62 V. | | | 0.9 | |
| **CURRENT FAULT RECOVERY (BACKOFF) TIMING** | | | | | | |
| $t_{ed}$ | Error delay timing. Delay before next attempt to power a channel following power removal due to error condition | $P_{CUT}$ , $I_{LIM}$ or $I_{Inrush}$ fault Semi-auto mode | 0.8 | 1 | 1.2 | s |
| $δI_{fault}$ | Duty cycle of $I_{channel}$ with current fault | | 5.5 | | 6.7 | % |
| **THERMAL SHUTDOWN** | | | | | | |
| | Shutdown temperature | Temperature rising | 135 | 146 | | °C |
| | Hysteresis | | | 7 | | °C |

## 7.5 Electrical Characteristics (continued)

Conditions are –40 < $T_J$ < 125 °C unless otherwise noted.$V_{VDD}$ = 3.3 V,$V_{VPWR}$ = 54 V, $V_{DGND}$ = $V_{AGND}$,DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, 2xFBn =0. Positive currents are into pins. $R_S$ = 0.200 Ω, to KSENSA (SEN1 orSEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL I/O (SCL, SDAI, A1-A4, /RESET, OSS unless otherwise stated)** | | | | | | |
| $V_{IH}$ | Digital input High | | 2.1 | | | V |
| $V_{IL}$ | Digital input Low | | | | 0.9 | V |
| $V_{IT\_HYS}$ | Input voltage hysteresis | | 0.17 | | | V |
| $V_{OL}$ | Digital output Low | SDAO at 9mA | | | 0.4 | V |
| | Digital output Low | /INT at 3mA | | | 0.4 | V |
| $R_{pullup}$ | Pullup resistor to VDD | /RESET, A1-A4, TEST0 | 30 | 50 | 80 | kΩ |
| $R_{pulldown}$ | Pulldown resistor to DGND | OSS, TEST1, TEST2 | 30 | 50 | 80 | kΩ |
| $t_{FLT\_INT}$ | Fault to /INT assertion | Time to internally register an Interrupt fault, from Channel turn off | | 50 | 500 | µs |
| $T_{RESETmin}$ | /RESET input minimum pulse width | | | | 5 | µs |
| $T_{bit\_OSS}$ | 3-bit OSS bit period | MbitPrty = 1 | 24 | 25 | 26 | µs |
| $t_{OSS\_IDL}$ | Idle time between consecutive shutdown code transmission in 3-bit mode | MbitPrty = 1 | 48 | 50 | | µs |
| $t_{r\_OSS}$ | Input rise time of OSS in 3-bit mode | 0.8 V → 2.3 V, MbitPrty = 1 | 1 | | 300 | ns |
| $t_{f\_OSS}$ | Input fall time of OSS in 3-bit mode | 2.3 V → 0.8 V, MbitPrty = 1 | 1 | | 300 | ns |
| **I2C TIMING REQUIREMENTS** | | | | | | |
| $t_{POR}$ | Device power-on reset delay | | | | 20 | ms |
| $f_{SCL}$ | SCL clock frequency | | 10 | | 400 | kHz |
| $t_{LOW}$ | LOW period of the clock | | 0.5 | | | µs |
| $t_{HIGH}$ | HIGH period of the clock | | 0.26 | | | µs |
| $t_{fo}$ | SDAO output fall time | SDAO, 2.3 V → 0.8 V, Cb = 10 pF, 10 kΩ pull-up to 3.3 V | 10 | | 50 | ns |
| | | SDAO, 2.3 V → 0.8 V, Cb = 400 pF, 1.3 kΩ pull-up to 3.3 V | 10 | | 50 | ns |
| $C_{I2C}$ | SCL capacitance | | | | 10 | pF |
| $C_{I2C\_SDA}$ | SDAI, SDAO capacitance | | | | 6 | pF |
| $t_{SU,DATW}$ | Data setup tme (Write operation) | | 50 | | | ns |
| $t_{HD,DATW}$ | Data hold time (Write operation) | | 0 | | | ns |
| $t_{HD,DATR}$ | Data hold time (Read operation) | | 150 | | 400 | ns |
| $t_{fSDA}$ | Input fall times of SDAI | 2.3 V → 0.8 V | 20 | | 120 | ns |
| $t_{rSDA}$ | Input rise times of SDAI | 0.8 V → 2.3 V | 20 | | 120 | ns |
| $t_r$ | Input rise time of SCL | 0.8 V → 2.3 V | 20 | | 120 | ns |
| $t_f$ | Input fall time of SCL | 2.3 V → 0.8 V | 20 | | 120 | ns |
| $t_{BUF}$ | Bus free time between a STOP and START condition | | 0.5 | | | µs |
| $t_{HD,STA}$ | Hold time After (Repeated) START condition | | 0.26 | | | µs |
| $t_{SU,STA}$ | Repeated START condition setup time | | 0.26 | | | µs |
| $t_{SU,STO}$ | STOP condition setup time | | 0.26 | | | µs |
| $t_{DG}$ | Suppressed spike pulse width, SDAI and SCL | | 50 | | | ns |
| $t_{WDT\_I2C}$ | I2C Watchdog trip delay | | 1.1 | 2.2 | 3.3 | sec |

## 7.6 Typical Characteristics

Conditions are –40 < $T_J$ < 125 °C unless otherwise noted.$V_{VDD}$ = 3.3 V, $V_{VPWR}$ = 54 V, $V_{DGND}$ = $V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, 2xFBn = 0. Positive currents are into pins. $R_S$ = 0.200 Ω, to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

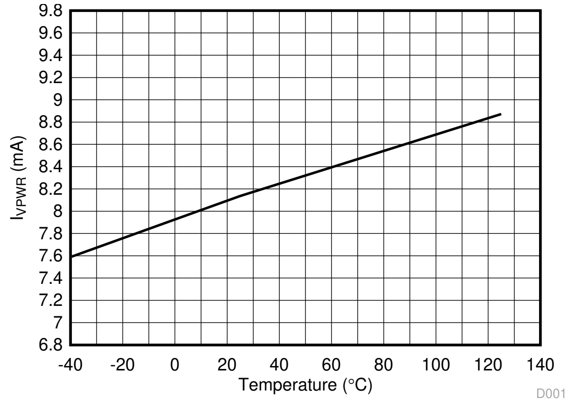

Figure 7-1. VPWR Current Consumption vs Temperature

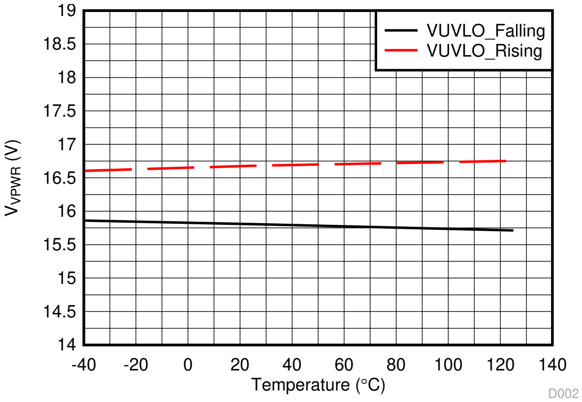

Figure 7-2. VPWR UVLO Thresholds vs Temperature

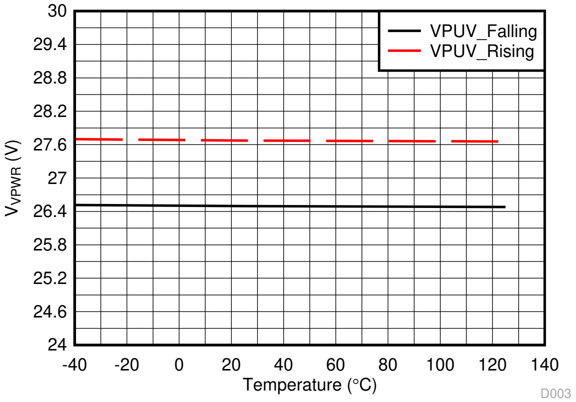

Figure 7-3. VPUV Thresholds vs Temperature

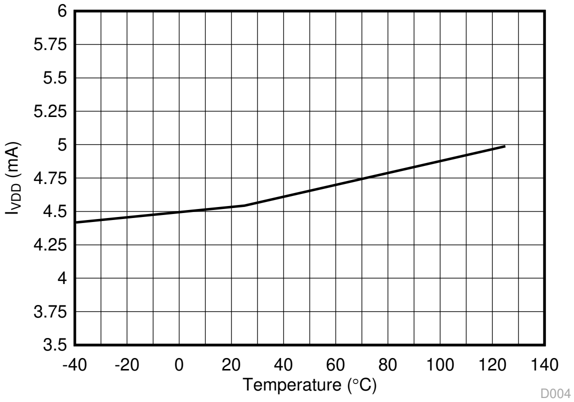

Figure 7-4. VDD Current Consumption vs Temperature

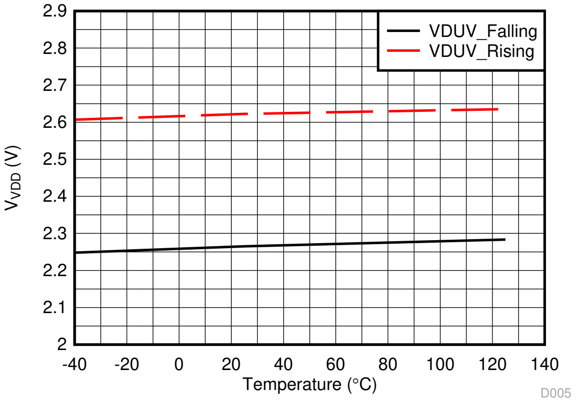

Figure 7-5. VDUV Thresholds vs Temperature

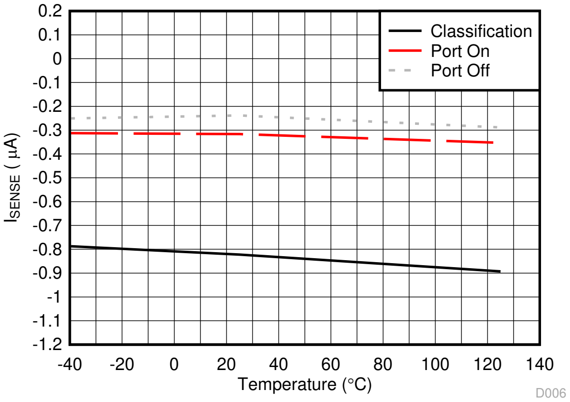

Figure 7-6. SENSE Pin Bias Current vs Temperature

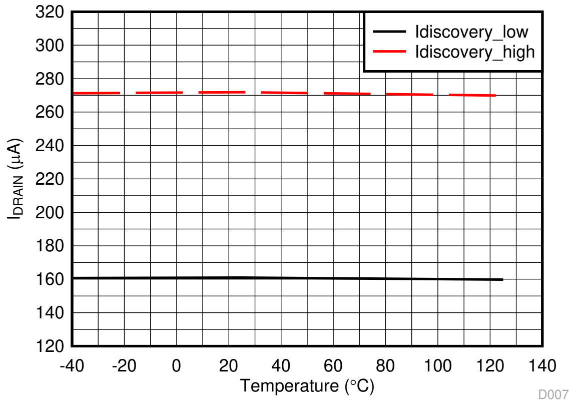

Figure 7-7. Discovery Currents vs Temperature

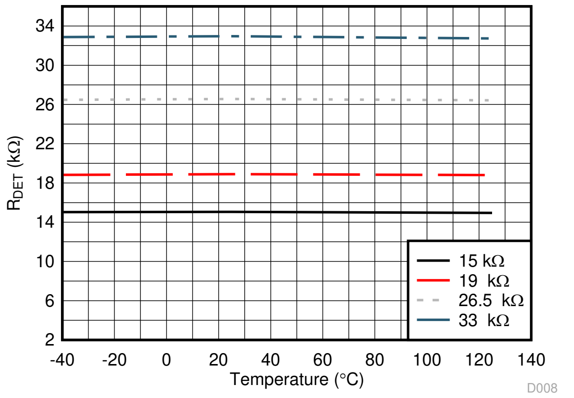

Figure 7-8. Discovery Resistance Measurement vs Temperature

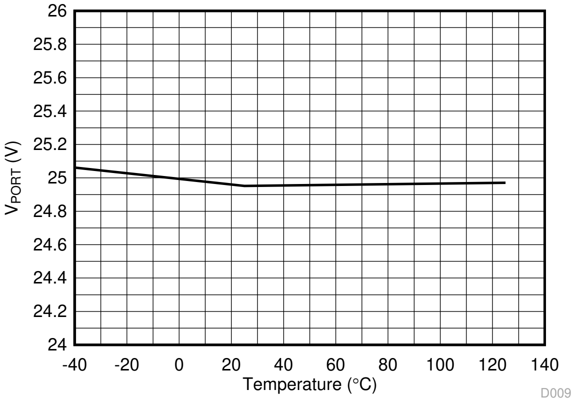

Figure 7-9. Discovery Open Circuit Voltage vs Temperature

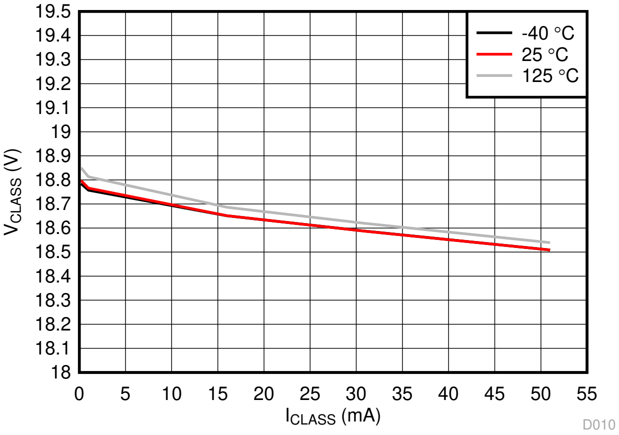

Figure 7-10. Classification Voltage vs $I_{CLASS}$ and Temperature

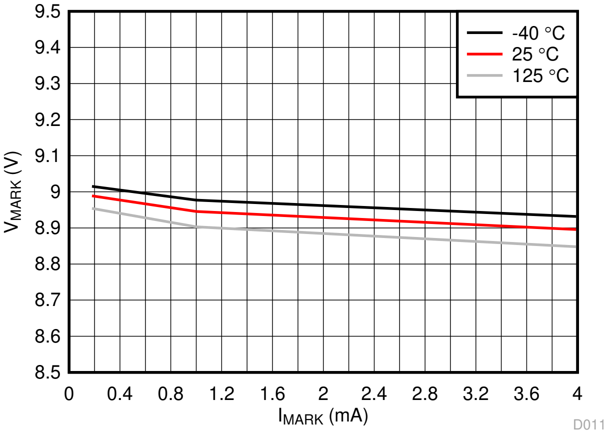

Figure 7-11. Mark Voltage vs $I_{MARK}$ and Temperature

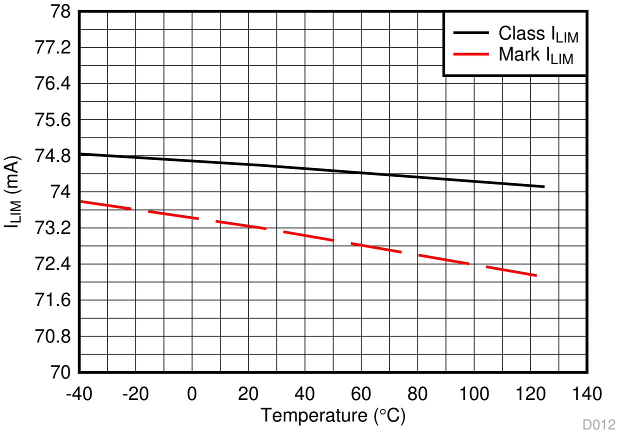

Figure 7-12. Classification and Mark Current Limit vs Temperature

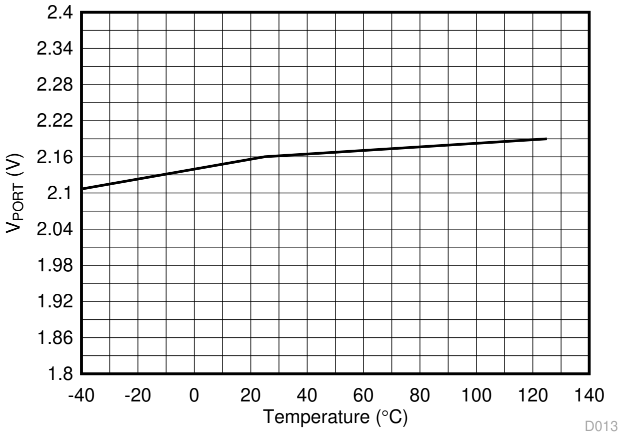

**Figure 7-13. Power Good Threshold vs Temperature**

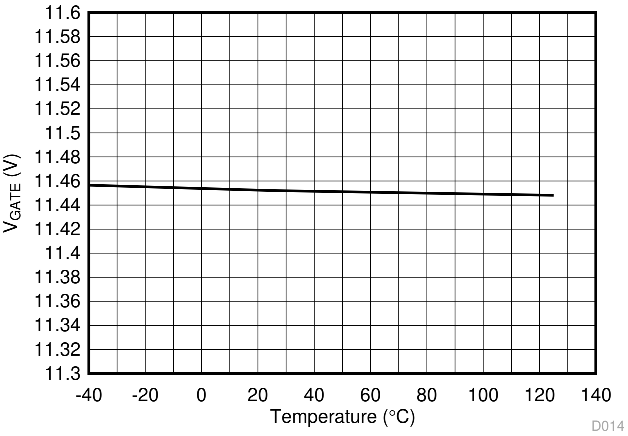

**Figure 7-14. Gate Voltage (Port On) vs Temperature**

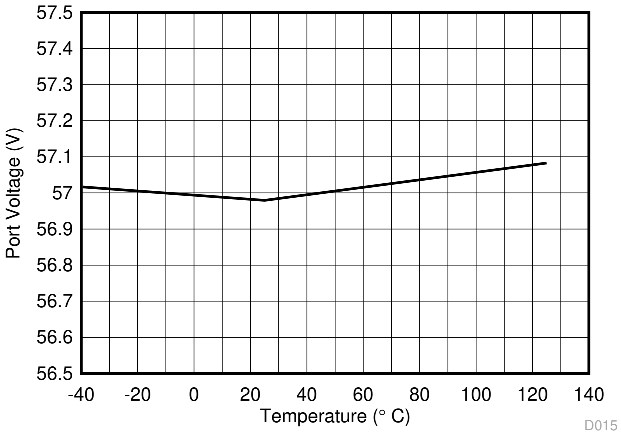

**Figure 7-15. Port Voltage ADC Measurement vs Temperature**

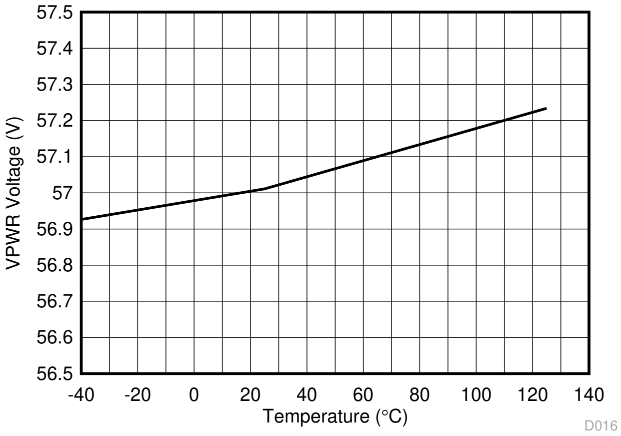

**Figure 7-16. VPWR Voltage ADC Measurement vs Temperature**

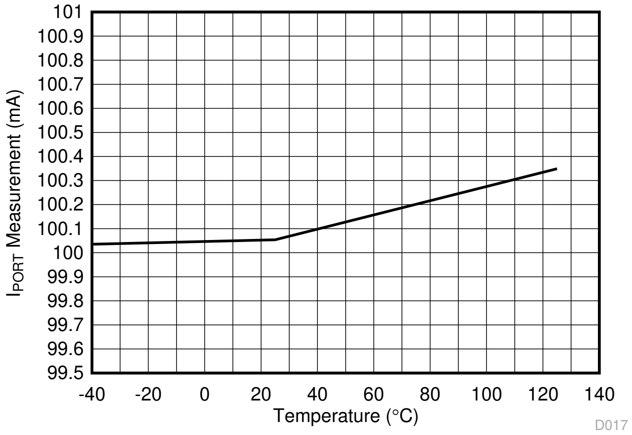

**Figure 7-17. Port Current ADC Measurement (100mA) vs Temperature**

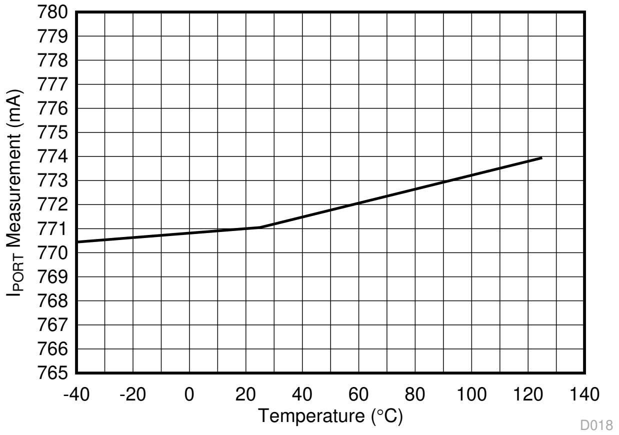

**Figure 7-18. Port Current ADC Measurement (770mA) vs Temperature**

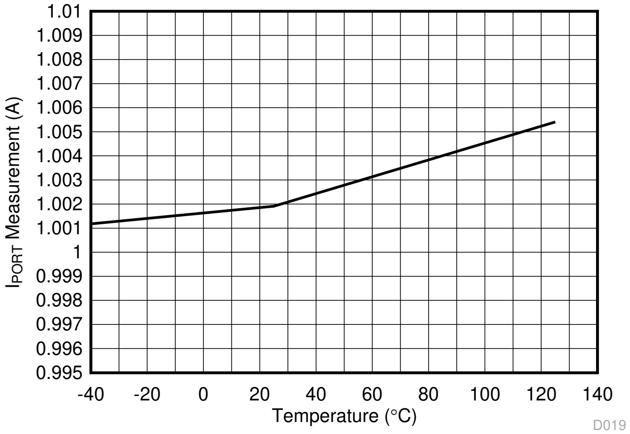

Figure 7-19. Port Current ADC Measurement (1 A) vs Temperature

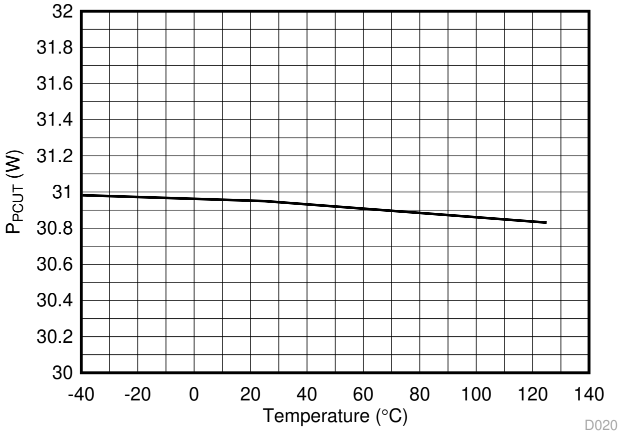

Figure 7-20. PCut Threshold (30W) vs Temperature

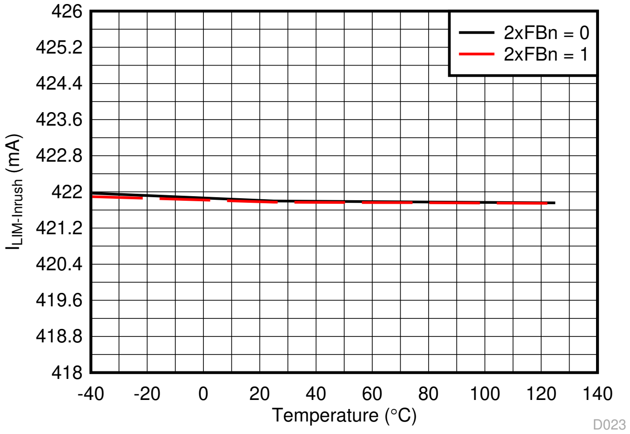

Figure 7-21. Inrush Current Limit vs Temperature

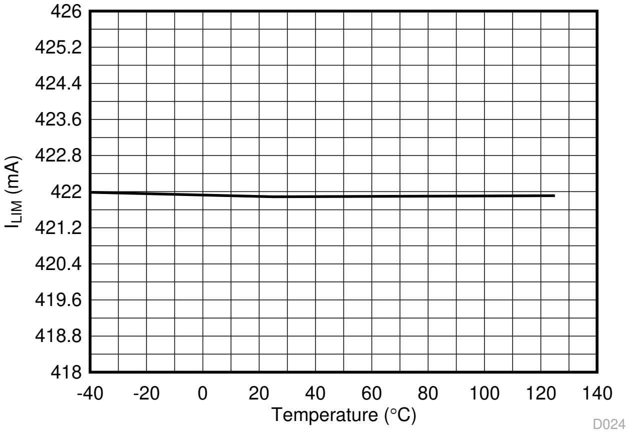

Figure 7-22. 1x Mode (2xFBn = 0) Current Limit vs Temperature

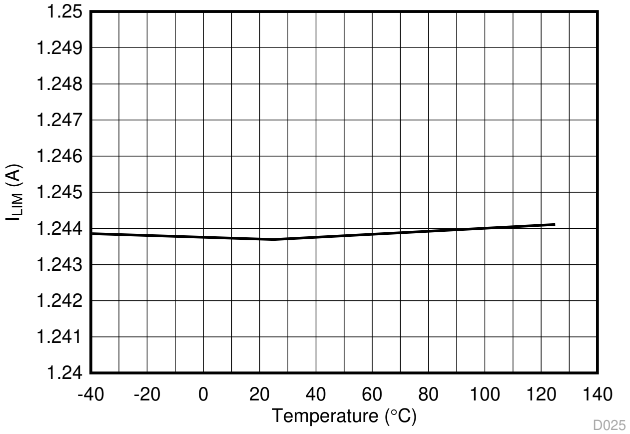

Figure 7-23. 2x Mode (2xFBn = 1) Current Limit vs Temperature

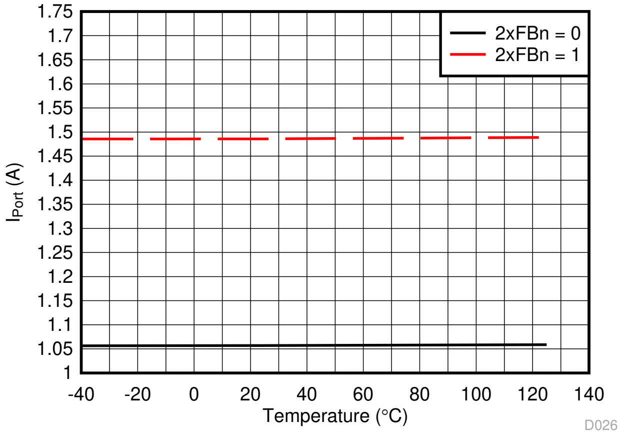

Figure 7-24. $I_{SHORT}$ Threshold vs Temperature

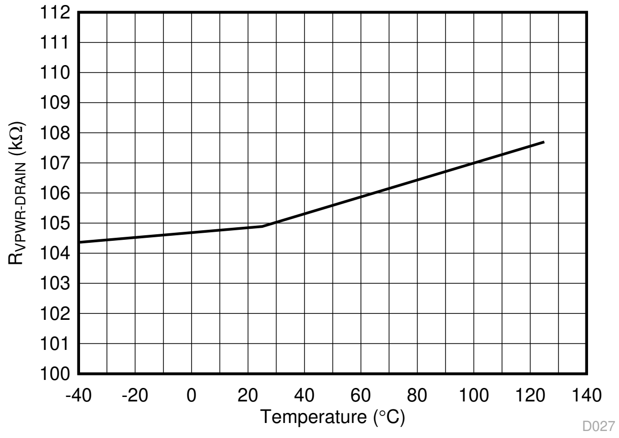

Figure 7-25. $R_{OFF}$ (VPWR to DRAIN) vs Temperature

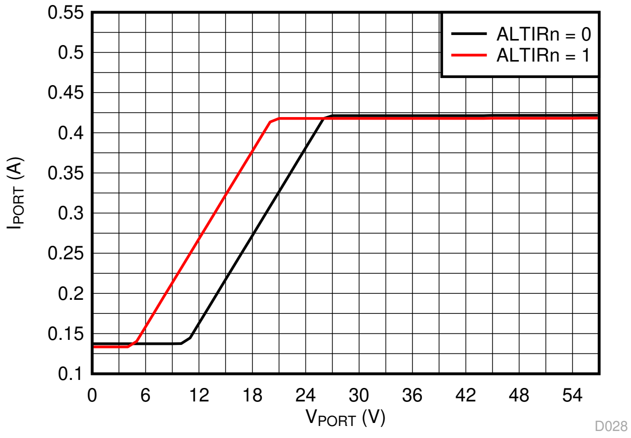

Figure 7-26. Inrush Current Foldback vs Port Voltage

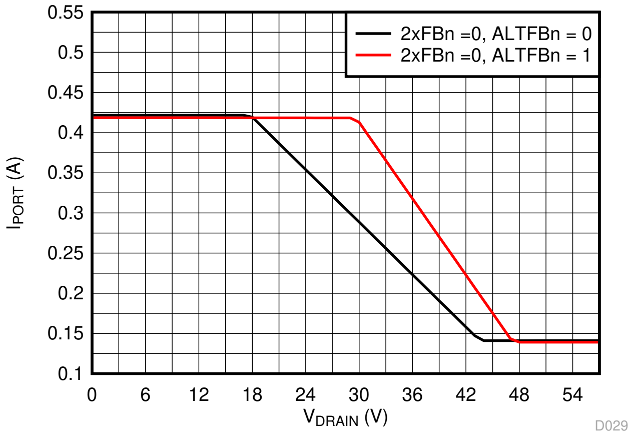

Figure 7-27. 1x Mode (2xFBn = 0) Current Foldback vs Drain Voltage

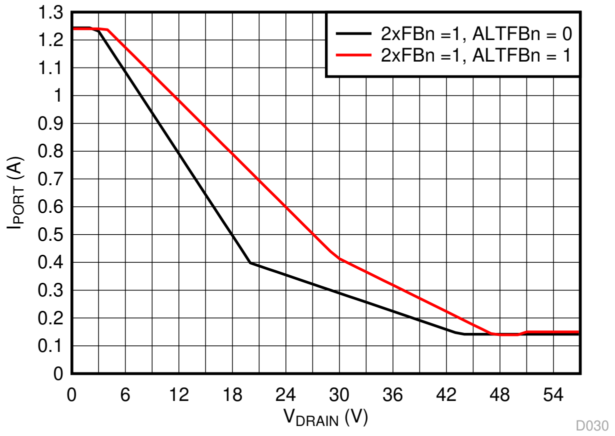

Figure 7-28. 2x Mode (2xFBn = 1) Current Foldback vs Drain Voltage

# 8 Parameter Measurement Information

## 8.1 Timing Diagrams

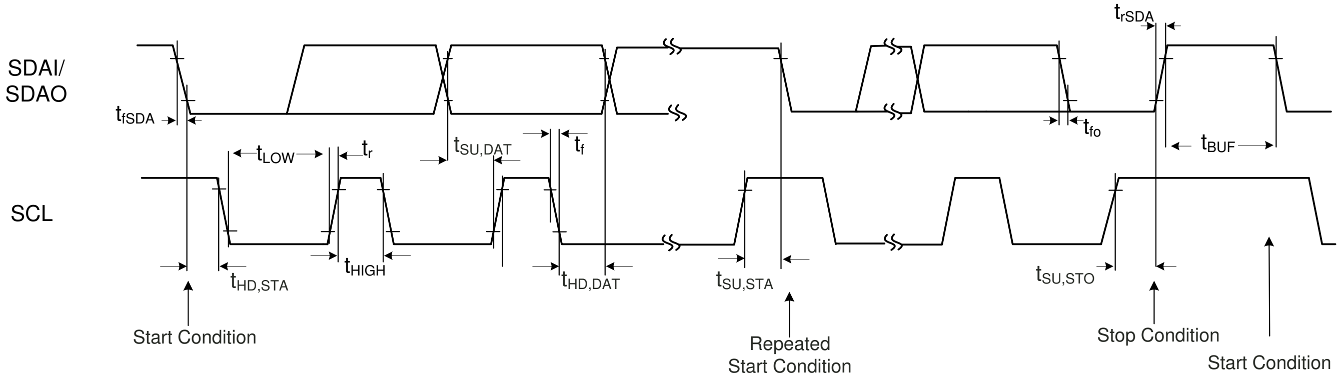

Figure 8-1. I²C Timings

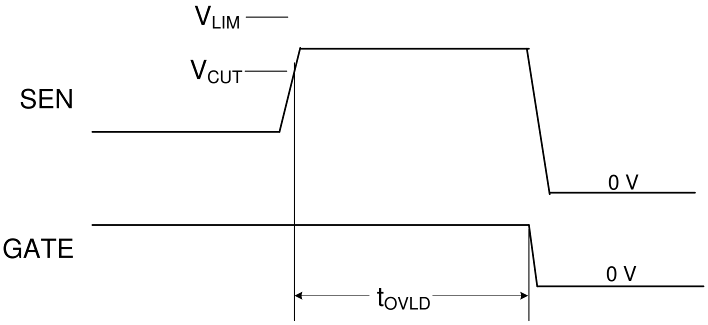

Figure 8-2. Overcurrent Fault Timing

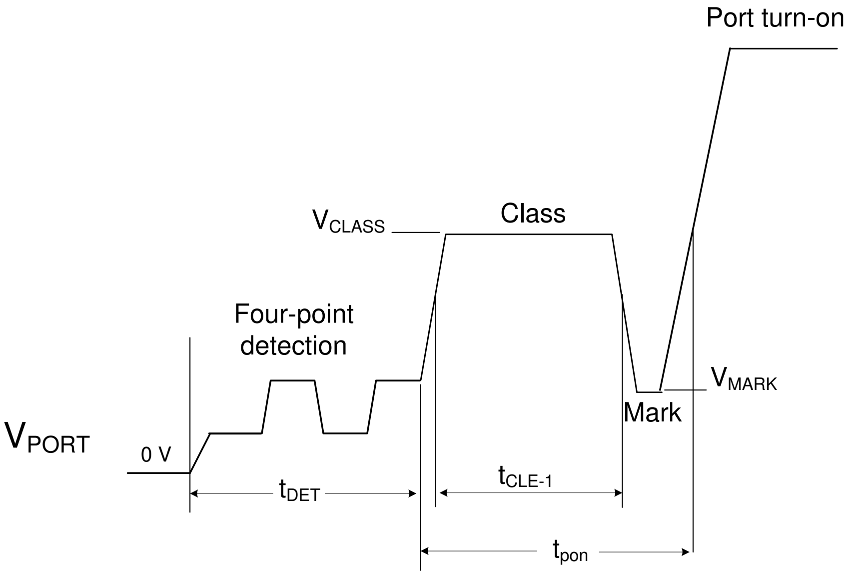

Figure 8-3. 2-Pair Detection, 1-Event Classification and Turn On

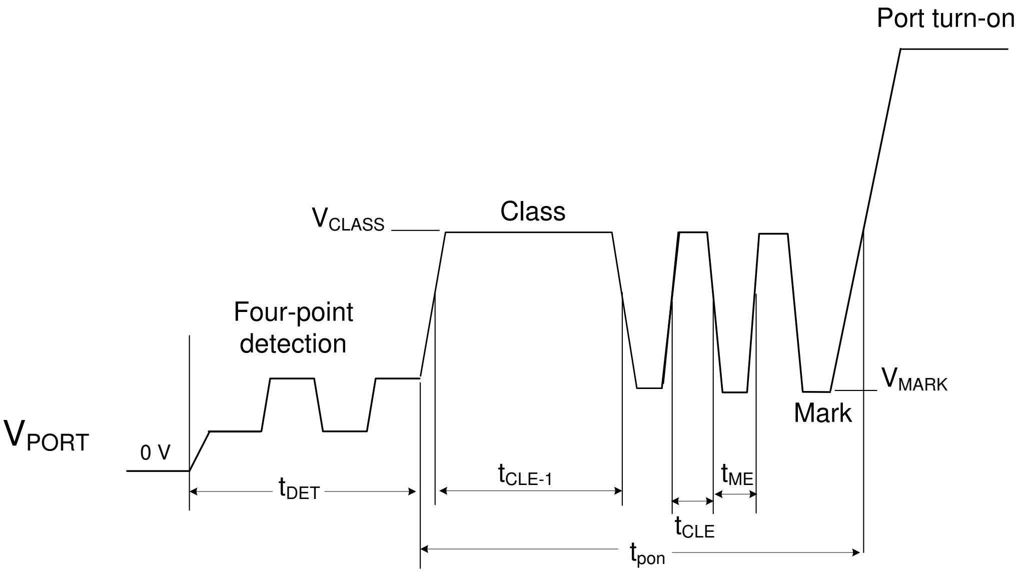

Figure 8-4. 2-Pair Detection, 3-Event Classification and Turn On

# 9 Detailed Description

## 9.1 Overview

The TPS23882 is an eight-channel PSE for Power over Ethernet applications. Each of the eight channels provides detection, classification, protection, and shutdown in compliance with the IEEE 802.3bt standard.

Basic PoE features include the following:

- Performs high-reliability 4-point load detection
- Performs multi-finger classification including the 100-ms long first class finger for Autoclass discovery and to identify as a 802.3bt complainant PSE
- Enables power with protective fold-back current limiting, and an adjustable $P_{CUT}$ threshold
- Shuts down during faults such as overcurrent or outputs shorts
- Performs a maintain power signature function to ensure power is removed if the load is disconnected
- Undervoltage lockout occurs if VPWR falls below $V_{PUV\_F}$ (typical 26.5 V).

Enhanced features include the following:

- Programable SRAM memory
- Dedicated 14-bit integrating current ADCs per port
- Port re-mapping capability
- 8- and 16-bit access mode selectable
- 1- and 3-bit port shutdown priority

### 9.1.1 Operating Modes

#### *9.1.1.1 Auto*

The port performs detection and classification (if valid detection occurs) continuously. Registers are updated each time a detection or classification occurs. The port power is automatically turned on based on the Power Allocation settings in register 0x29 if a valid classification is measured.

#### *9.1.1.2 Semiauto*

The port performs detection and classification (if valid detection occurs) continuously. Registers are updated each time a detection or classification occurs. The port power is not automatically turned on. A Power Enable command is required to turn on the port.

#### *9.1.1.3 Manual/Diagnostic*

***The use of this mode is intended for system diagnostic purposes only in the event that ports cannot be powered in accordance with the IEEE 802.3bt standard from Semiauto or Auto modes.***

The port performs the functions as configured in the registers. There is no automatic state change. Singular detection and classification measurements will be performed when commanded. Ports will be turned on immediately after a Power Enable command without any detection or classification measurements. Even though multiple classification events may be provided, the port voltage will reset immediately after the last finger, resetting the PD.

#### *9.1.1.4 Power Off*

The port is powered off and does not perform a detection, classification, or power-on. In this mode, Status and Enable bits for the associated port are reset.

### 9.1.2 PoE Compliance Terminology

With the release of the IEEE 802.3bt standard, compliant PoE equipment has expanded to include four different "Types" of devices that support power over 2-Pair or 4-Pair, in either Single or Dual signature configurations, with classifications ranging from 0 to 8. Different manufactures have used varying terminology over time to describe their equipment capabilities, and it can become difficult to identify how to correctly categorize and brand a particular piece of equipment. For this reason and in conjunction with the Ethernet Alliance (EA), the industry leading providers of PoE equipment and devices have agreed to transition to using the "PoE 1" and "PoE 2" banding per the table below Table 9-1.

**Table 9-1. Summary Table of PoE Compliance Terminology**

| Brand / Acronym | IEEE Standard | Clause | Clause Title | Types | Classes | EA Certified Logo |
|---|---|---|---|---|---|---|
| PoE 1 | 802.3af | 33 | Power over Ethernet over 2-Pairs | 1 | 0 - 3 | Gen 1 Class 1-4 |
| | 802.3at | | | 2 | 0 - 4 | |
| PoE 2 | 802.3bt | 145 | Power over Ethernet | 3 | 1 - 6, or 1-4 DS(1) | Gen 2 Class 1-8 |
| | | | | 4 | 7 - 8, or 5 DS(1) | |

(1) "DS" is used to designate "Dual Signature" PDs

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**Note**

By design PoE 2 PSEs are fully interoperable with any existing PoE 1 equipment, and although not all functionality may be enabled, PoE 2 PDs connected to PoE 1 PSEs are required to limit their power consumption to the PSE presented power capabilities see Power Allocation and Power Demotion.

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### 9.1.3 PoE 2 Type-3 2-Pair PoE

Upon release of the new IEEE 802.3bt standard, the IEEE introduced two new "Types" of PoE equipment. The addition of Type-3 and Type-4 equipment are most commonly associated with the addition of 4-Pair PoE and their available power increases of to up to 90 W sourced from a PSE port. However, the new PoE 2 Type-3 designation also applies to new 2-Pair PoE equipment as well. Most notably, the new 802.3bt standard supports a reduced $T_{MPS}$ time (6 ms vs. 60 ms) and a new feature called Autoclass, and by definition any device that supports these new features is designated as Type-3 equipment even if power is only provided over 2-pairs (one alternative pairset) in an ethernet cable. Since the TPS23882 supports these new features including its use of the 100ms long first class finger to identify itself as an IEEE 802.3bt PSE, it is officially classified as a Type-3 PSE even through power delivery is limited to 2-pair.

Please note that as the 802.3at standard created "type-2" equipment that was fully interoperable with the previous PoE 1 Type-1 (802.3af) equipment, any new 802.3bt Type-3 equipment including the TPS23882 is fully operable with any existing PoE 1 Type-1 (.af) and Type-2 (.at) equipment.

### 9.1.4 *Requested* Class versus *Assigned* Class

The *requested* class is the classification the PSE measures during mutual identification prior to turnon, whereas the *assigned* class is the classification level the channel was powered on with based on the power allocation setting in register 0x29h. In most cases where the power allocation equals or exceeds the *requested* class, the *requested* and *assigned* classes will be the same. However, in the case of power demotion, these values will differ.

For example: If a 4-pair Class 8 PD is connected to a 30 W (Class 4) configured PSE port, the *requested* class reports "Class 8", while the *assigned* class reports "Class 4".

The **requested** classification results are available in registers 0x0C-0F

The **assigned** classification results are available in registers 0x4C-4F

**Note**

There is no Assigned Class assigned for ports/channels powered out of Manual/Diagnostic mode.

### 9.1.5 Power Allocation and Power Demotion

The Power Allocation settings in register 0x29 sets the maximum power level a port will power on. Settings for each Class level from 2-pair 4 W (Class 1) up to 2-pair 30 W (Class 4) have been provided to maximize system design flexibility.

**Note**

The Power Allocation settings in register 0x29 do not set the power limit for a given port. The port and channel power limiting is configured with the 2P (registers 0x1E- x 21) policing registers

During a turn on attempt, if a PD presents a classification level greater than the power allocation setting for a port, the TPS23882 limits the number of classification fingers presented to the PD prior to turn on based on the power allocation settings in register 0x29. This behavior is called *Power Demotion* as it is the number of fingers presented to the PD that sets the maximum level of power the PD is allowed to draw before the PSE is allowed to disable it.

**Note**

The IEEE 802.3 standard requires PDs that are power demoted by a PSE to limit their total power draw below the Type/class level set by the number of fingers presented by the PSE during mutual identification.

In a 2-pair system, Power demotion is limited to either 30 W (3-fingers) or 15.4 W (1-finger) as there is no other physical means of indicating to a PD over the physical layer that less than 15.4 W is available.

If register 0x29 is configured for either 4 W (class 1) or 7 W (Class 2), and a Class 3 or higher device is connected, the port will not be powered and a Start Fault will be reported along with an "Insufficient Power" indication provided in register 0x24.

**Table 9-2. 2-Pair Power Demotion Table**

| Power Allocation Register 0x29 | Assigned Class Value (based on the PD connected at the port) | | | | |
|---|---|---|---|---|---|
| | Class 1 PD | Class 2 PD | Class 3 PD | Class 4 PD | Class 5+ PDs |
| 2-Pair 4 W | Class 1 | **Start Fault Insufficient Power** | **Start Fault Insufficient Power** | **Start Fault Insufficient Power** | **Start Fault Insufficient Power** |
| 2-Pair 7 W | Class 1 | Class 2 | **Start Fault Insufficient Power** | **Start Fault Insufficient Power** | **Start Fault Insufficient Power** |
| 2-Pair 15.5 W | Class 1 | Class 2 | Class 3 | Class 3 | Class 3 |

**Table 9-2. 2-Pair Power Demotion Table (continued)**

| Power Allocation Register 0x29 | Assigned Class Value (based on the PD connected at the port) | | | | |
|---|---|---|---|---|---|
| | Class 1 PD | Class 2 PD | Class 3 PD | Class 4 PD | Class 5+ PDs |
| 2-Pair 30 W | Class 1 | Class 2 | Class 3 | Class 4 | Class 4 |

### 9.1.6 Programmable SRAM

The TPS23882 device has been designed to include programmable SRAM that accommodates future firmware updates to support interoperability and/or compliance issues that may arise as new equipment is introduced in conjunction with the release of the IEEE 802.3bt standard.

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**Note**

The latest version of firmware and SRAM release notes may be accessed from the *TI mySecure Software* webpage.

The SRAM Release Notes and ROM Advisory document includes more detailed information regarding any know issues and changes that were associated with each firmware release.

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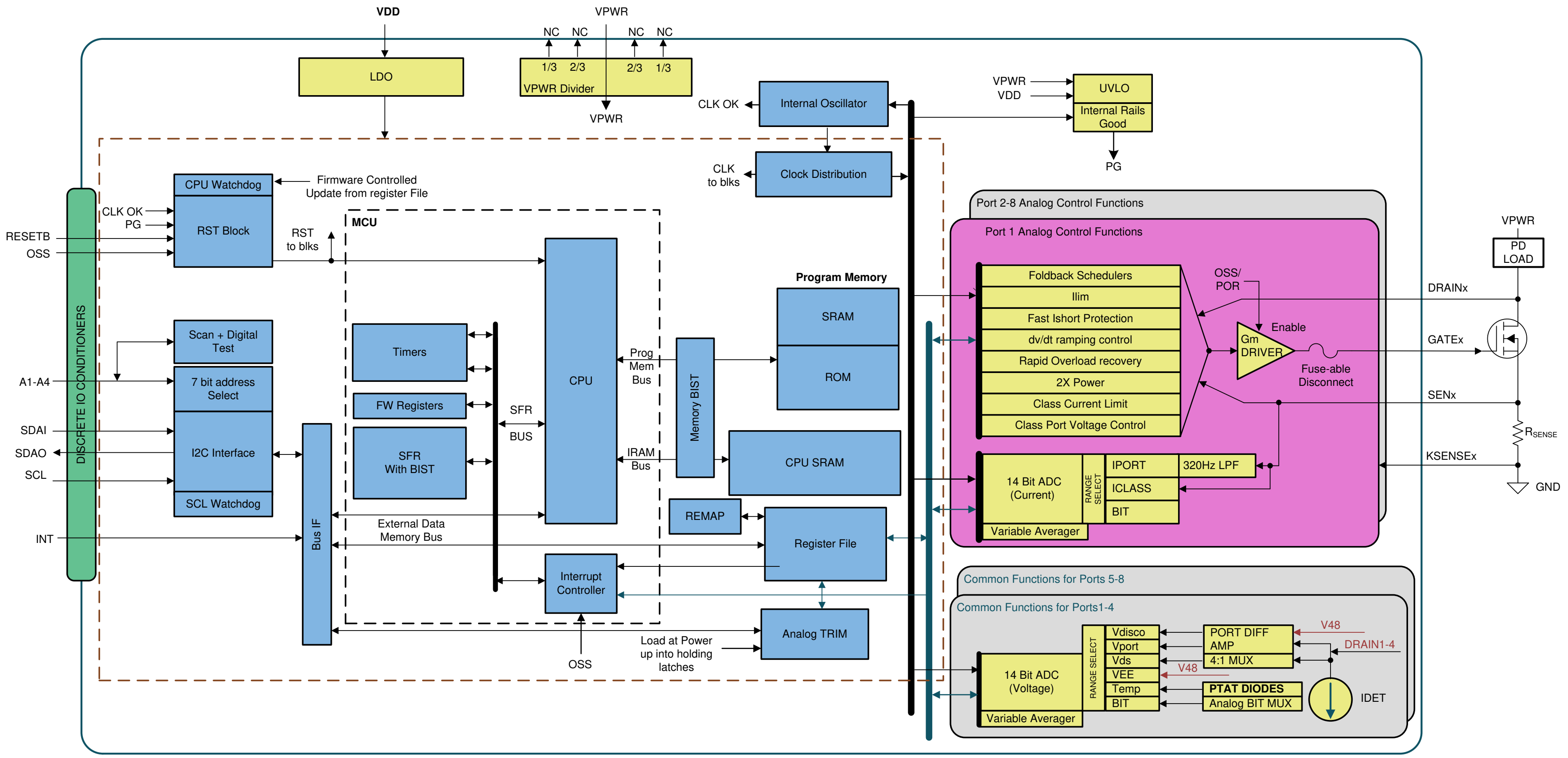
Upon power up, it is recommended that the TPS23882 device's SRAM be programmed with the latest version of SRAM code via the $I^2C$ to ensure proper operation and IEEE complaint performance. All $I^2C$ traffic other than those commands required to program the SRAM should be deferred until after the SRAM programming sequences are completed.

For systems that include multiple TPS23882 devices, the 0x7F "global" broadcast I2C address may be used to programmed all of the devices at the same time.

For more detailed instructions on the SRAM programing procedures please refer to Section 9.6.2.67 and the *How to Load TPS2388x SRAM Code* document on TI.com.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Port Remapping

The TPS23882 provides port remapping capability, from the logical ports to the physical channels and pins.

The remapping is between any channel of a 4-port group (1 to 4, 5 to 8).

The following example is applicable to 0x26 register = 00111001, 00111001b.

- Logical port 1 (5) ↔ Physical channel 2 (6)
- Logical port 2 (6) ↔ Physical channel 3 (7)
- Logical port 3 (7) ↔ Physical channel 4 (8)
- Logical port 4 (8) ↔ Physical channel 1 (5)

**Note**

The device ignores any remapping command unless all four ports are in off mode.

If the TPS23882 receives an incorrect configuration, it ignores the incorrect configuration and retains the previous configuration. The ACK is sent as usual at the end of communication. For example, if the same remapping code is received for more than one port, then a read back of the Re-Mapping register (0x26) would be the last valid configuration.

Note that if an IC reset command (1Ah register) is received, the port remapping configuration is kept unchanged. However, if there is a Power-on Reset or if the $\overline{\text{RESET}}$ pin is activated, the Re-Mapping register is reinitialized to a default value.

### 9.3.2 Port Power Priority

The TPS23882 supports 1- and 3-bit shutdown priority, which are selected with the MbitPrty bit of General Mask register (0x17).

The 1-bit shutdown priority works with the Port Power Priority (0x15) register. An OSSn bit with a value of 1 indicates that the corresponding port is treated as low priority, while a value of 0 corresponds to a high priority. As soon as the OSS input goes high, the low-priority ports are turned off.

The 3-bit shutdown priority works with the Multi Bit Power Priority (0x27/28) register, which holds the priority settings. A port with “000” code in this register has highest priority. Port priority reduces as the 3-bit value increases, with up to 8 priority levels. See Figure 9-1.

The multi bit port priority implementation is defined as the following:

- OSS code ≤ Priority setting (0x27/28 register): Port is disabled
- OSS code > Priority setting (0x27/28 register): Port remains active

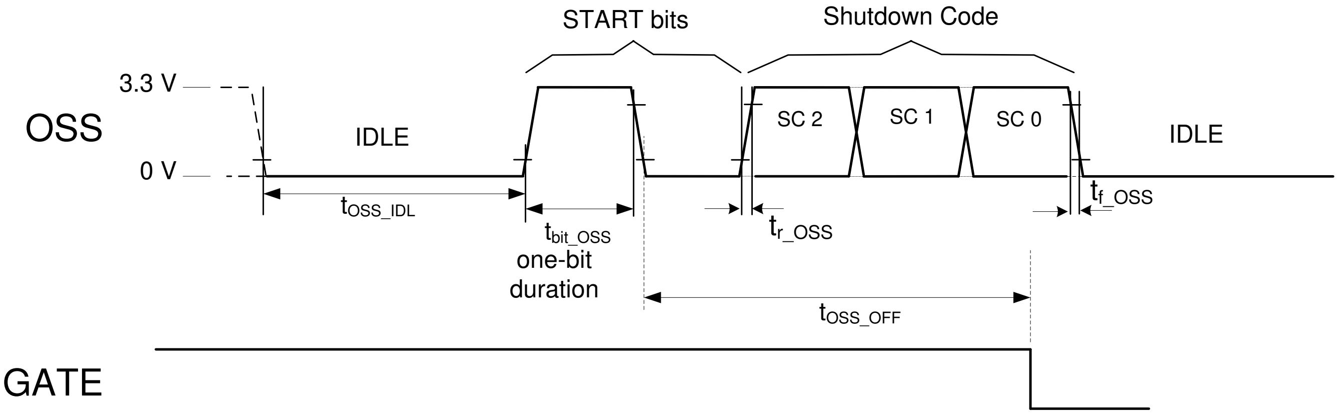


**Figure 9-1. Multi Bit Priority Port Shutdown if Lower-Priority Port**

**Note**

Prior to setting the MbitPrty bit from 0 to 1, make sure the OSS input is in the idle (low) state for a minimum of 200 µs, to avoid any port misbehavior related to loss of synchronization with the OSS bit stream.

**Note**

The OSS input has an internal 1-µs to 5-µs deglitch filter. From the idle state, a pulse with a longer duration is interpreted as a valid start bit. Ensure that the OSS signal is noise free.

### 9.3.3 Analog-to-Digital Converters (ADC)

The TPS23882 features 10 multi-slope integrating converters. Each of the first eight converters is dedicated to current measurement for one channel and operate independently to perform measurements during classification and when the channel is powered on. When the channel is powered, the converter is used for current (100-ms averaged) monitoring, power policing, and DC disconnect. Each of the last two converters are shared within a group of four channels for discovery (16.6-ms averaged), port powered voltage monitoring, power-good status, and FET short detection. These converters are also used for general-purpose measurements including input voltage (1 ms) and die temperature.

The ADC type used in the TPS23882 differs from other similar types of converters in that the ADCs continuously convert while the input signal is sampled by the integrator, providing inherent filtering over the conversion period. The typical conversion time of the current converters is 800 µs, while the conversion time is 1 ms for the other converters. Powered-device detection is performed by averaging 16 consecutive samples which provides significant rejection of noise at 50-Hz or 60-Hz line frequency. While a port is powered, digital averaging provides a channel current measurement integrated over a 100-ms time period. Note that an anti-aliasing filter is present for powered current monitoring.

**Note**

During powered mode, current conversions are performed continuously. Also, in powered mode, the $t_{START}$ timer must expire before any current or voltage ADC conversion can begin.

### 9.3.4 I$^2$C Watchdog

An I$^2$C Watchdog timer is available on the TPS23882 device. The timer monitors the I$^2$C, SCL line for clock edges. When enabled, a timeout of the watchdog resets the I$^2$C interface along with any active ports. This feature provides protection in the event of a hung software situation or I$^2$C bus hang-up by slave devices. In the latter case, if a slave is attempting to send a data bit of 0 when the master stops sending clocks, then the slave my drive the data line low indefinitely. Because the data line is driven low, the master cannot send a STOP to clean up the bus. Activating the I$^2$C watchdog feature of the TPS23882 clears this deadlocked condition. If the timer of two seconds expires, the ports latch off and the WD status bit is set. Note that WD Status will be set even if the watchdog is not enabled. The WD status bit may only be cleared by a device reset or writing a 0 to the WDS status bit location. The 4-bit watchdog disable field shuts down this feature when a code of 1011b is loaded. This field is preset to 1011b whenever the TPS23882 is initially powered. See *I$^2$C WATCHDOG Register* for more details.

### 9.3.5 Current Foldback Protection

The TPS23882 features two types of foldback mechanisms for complete MOSFET protection.

During inrush, at channel turn on, the foldback is based on the channel voltage as shown in Figure 9-2. Note that the inrush current profile remains the same, regardless of the state of the 2xFBn bits in register 0x40.

After the channel is powered and the Power Good is valid, a dual-slope operational foldback is used, providing protection against partial and total short-circuit at port output, while still being able to maintain the PD powered during normal transients at the PSE input voltage. Note that setting the 2xFBn bit selects the 2× curve and clearing it selects the 1× curve. See Figure 9-3.

In addition to the default foldback curves, the TPS23882 has individually enabled *alternative* foldback curves for both inrush and powered operation. These curves have been designed to accommodate certain loads that do not fully comply with the IEEE standard and requires additional power to be turned on or remain powered. See Figure 9-2 and Figure 9-3.

**Note**

If using the Alternative Foldback curves (ALTIRn or ALTFBn = 1), designers need to account for the additional power dissipation that can occur in the FETs under these conditions.

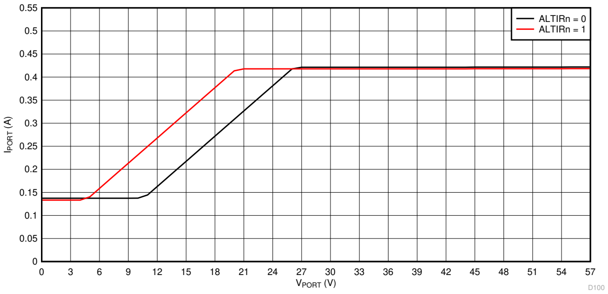


**Figure 9-2. Foldback During Inrush (at Port Turn On): $I_{LIM}$ vs $V_{port}$**

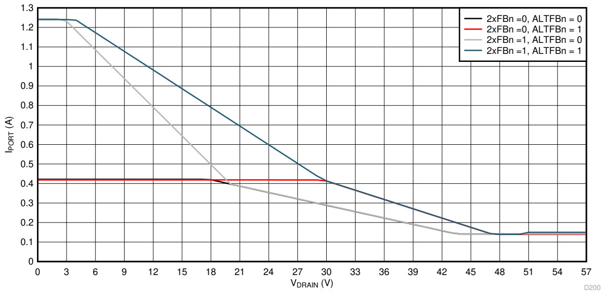


**Figure 9-3. Foldback When the Port is Already ON: $I_{LIM}$ vs $V_{drain}$**

## 9.4 Device Functional Modes

### 9.4.1 Detection

To eliminate the possibility of false detection, the TPS23882 uses a TI proprietary 4-point detection method to determine the signature resistance of the PD device. A false detection of a valid 25-kΩ signature can occur with 2-point detection type PSEs in noisy environments or if the load is highly capacitive.

Detection 1 and Detection 2 are merged into a single detection function which is repeated. Detection 1 applies I1 (160 µA) to a channel, waits approximately 60 ms, then measures the channel voltage (V1) with the integrating ADC. Detection 2 then applies I2 (270 µA) to the channel, waits another approximately 60 ms, then measures the channel voltage again (V2). The process is then repeated a second time to capture a third (V3) and fourth (V4) channel voltage measurements. Multiple comparisons and calculations are performed on all four measurement point combinations to eliminate the effects of a nonlinear or hysteretic PD signature. The resulting channel signature is then sorted into the appropriate category.

**Note**

The detection resistance measurement result is also available in the Channel Detect Resistance registers (0x44 - 0x47).

### 9.4.2 Classification

Hardware classification (class) is performed by supplying a voltage and sampling the resulting current. To eliminate the high power of a classification event from occurring in the power controller chip, the TPS23882 uses the external power FET for classification.

During classification, the voltage on the gate node of the external MOSFET is part of a linear control loop. The control loop applies the appropriate MOSFET drive to maintain a differential voltage between VPWR and DRAIN of 18.5 V. During classification the voltage across the sense resistor in the source of the MOSFET is measured and converted to a class level within the TPS23882. If a load short occurs during classification, the MOSFET gate voltage reduces to a linearly controlled, short-circuit value for the duration of the class event.

Classification results are read through the $I^2C$ Detection Event and Channel-n Discovery Registers. The TPS23882 also supports 1, and 3 finger classification for PDs ranging from Class 0 through Class 4, using the Power Enable and Port Power Allocation registers. Additionally, by providing a 3rdclass finger during discovery in Semi Auto mode, the TPS23882 is capable of identifying if a 4-pair Class 5-8 PD is connected to the port.

### 9.4.3 DC Disconnect

Disconnect is the automated process of turning off power to the port. When the port is unloaded or at least falls below minimum load, it is required to turn off power to the port and restart detection. In DC disconnect, the voltage across the sense resistors is measured. When enabled, the DC disconnect function monitors the sense resistor voltage of a powered port to verify the port is drawing at least the minimum current to remain active. The $T_{DIS}$ timer counts up whenever the port current is below the disconnect threshold (6.5 mA typical). If a timeout occurs, the port is shut down and the corresponding disconnect bit in the Fault Event Register is set. In the case of a PD implementing MPS (maintain Power Signature) current pulsing, the $T_{DIS}$ counter is reset each time the current goes continuously higher than the disconnect threshold for at least 3 ms.

The $T_{DIS}$ duration is set by the $T_{MPDO}$ Bits of the Timing Configuration register (0x16).

## 9.5 $I^2C$ Programming

### 9.5.1 $I^2C$ Serial Interface

The TPS23882 features a 3-wire $I^2C$ interface, using SDAI, SDAO, and SCL. Each transmission includes a START condition sent by the master, followed by the device address (7-bit) with R/W bit, a register address byte, then one or two data bytes and a STOP condition. The recipient sends an acknowledge bit following each byte transmitted. SDAI/SDAO is stable while SCL is high except during a START or STOP condition.

Figure 9-4 and Figure 9-5 show read and write operations through $I^2C$ interface, using configuration A or B (see Table 9-23 for more details). The parametric read operation is applicable to ADC conversion results. The TPS23882 features quick access to the latest addressed register through $I^2C$ bus. When a STOP bit is received, the register pointer is not automatically reset.

It is also possible to perform a write operation to many TPS23882 devices at the same time. The slave address during this broadcast access is 0x7F, as shown in *Section 9.6.2.13*. Depending on which configuration (A or B) is selected, a global write proceeds as following:

- Config A: Both 4-port devices (1 to 4 and 5 to 8) are addressed at same time.
- Config B: The whole device is addressed.

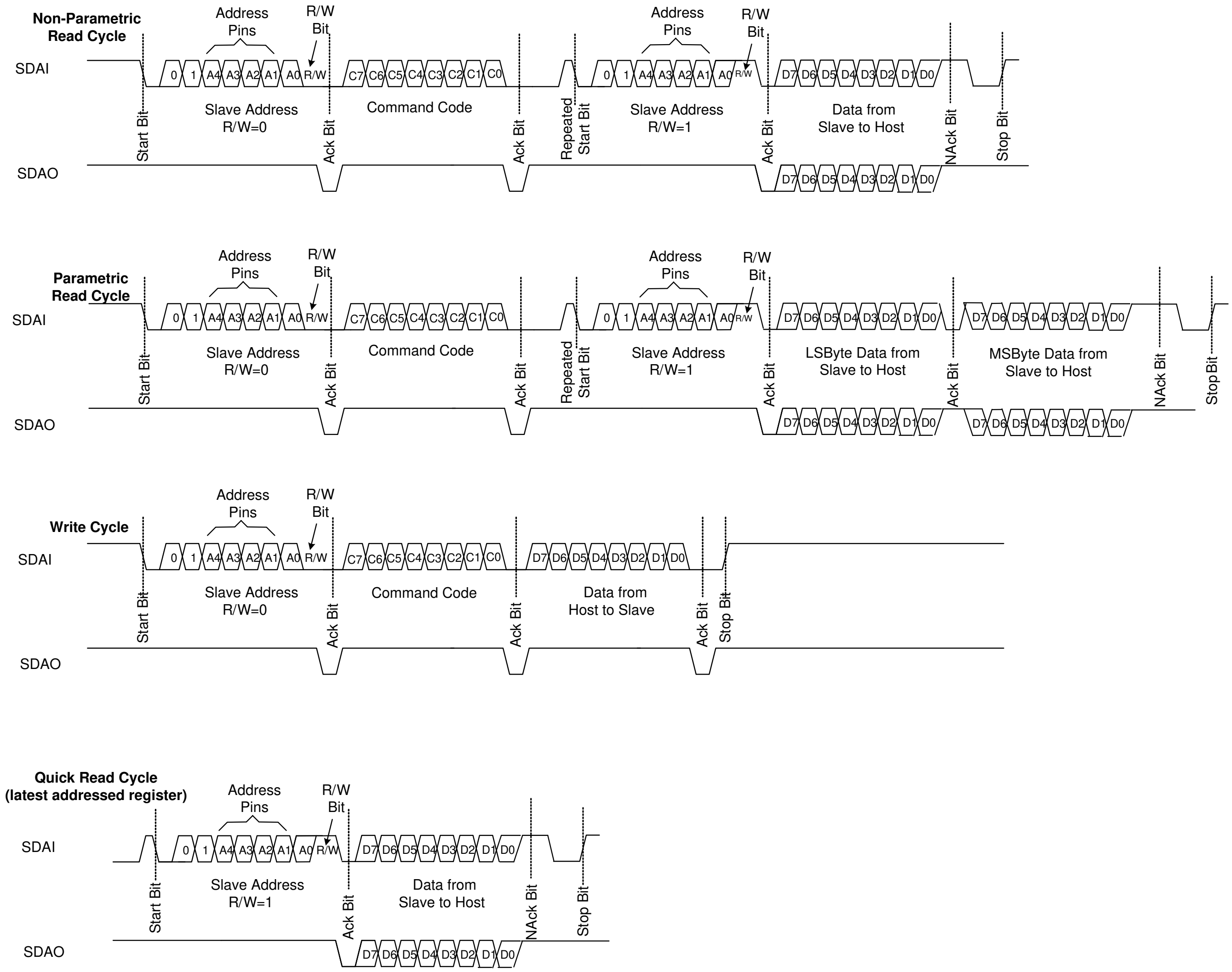


Figure 9-4. I$^2$C interface Read and Write Protocol – Configuration A

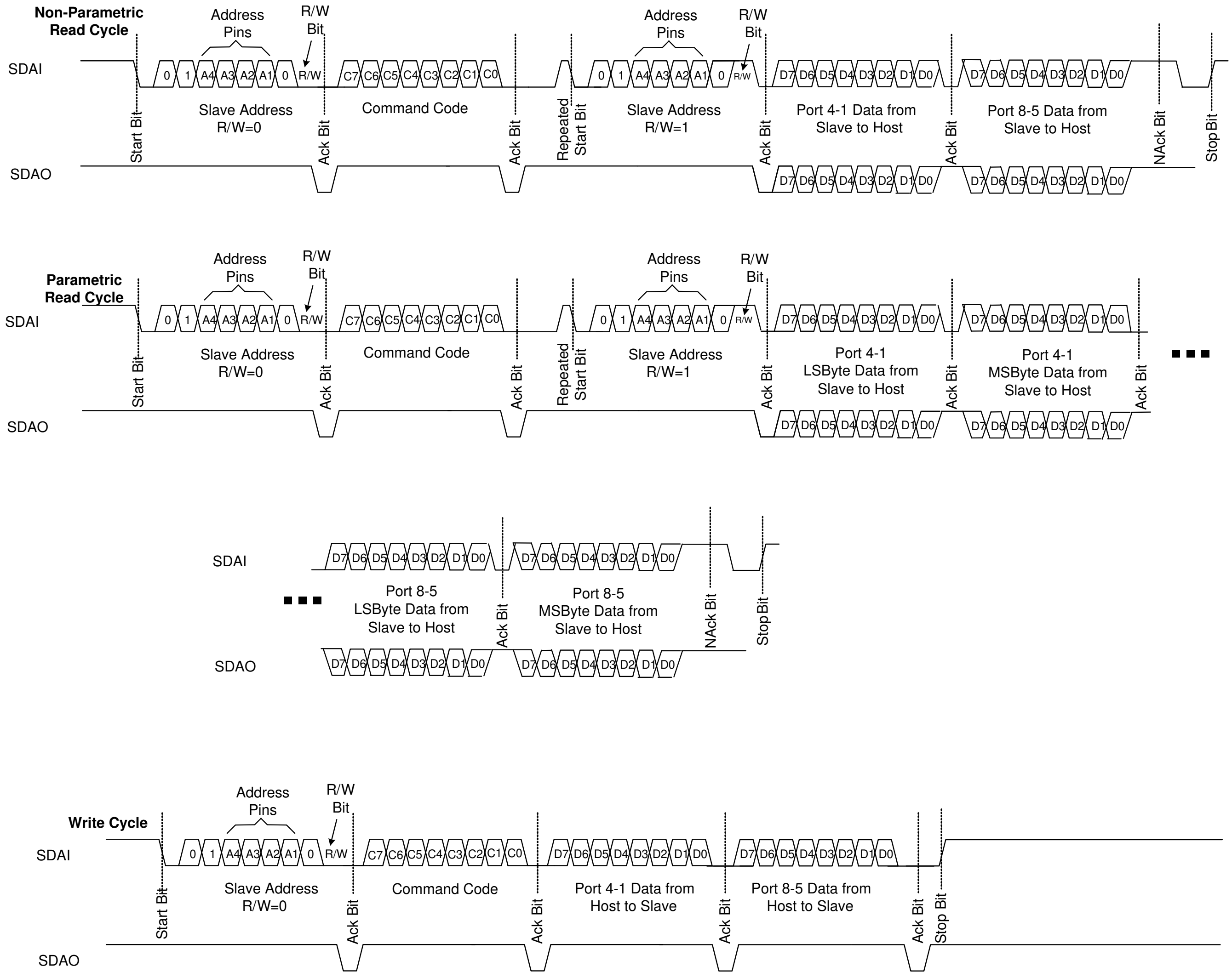


Figure 9-5. I$^2$C interface Read and Write Protocol – Configuration B

## 9.6 Register Maps

### 9.6.1 Complete Register Set

**Table 9-3. Main Registers**

| Cmd Code | Register or Command Name | $I^2C$ R/W | Data Byte | RST State | Bits Description | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **INTERRUPTS** | | | | | | | | | | | | |
| 00h | INTERRUPT | RO | 1 | 1000,0000b (1) | SUPF | STRTF | IFAULT | CLASC | DETC | DISF | PGC | PEC |
| 01h | INTERRUPT MASK | R/W | 1 | 1000,0000b | SUMSK | STMSK | IFMSK | CLMSK | DEMSK | DIMSK | PGMSK | PEMSK |
| **EVENT** | | | | | | | | | | | | |
| 02h | POWER EVENT | RO | 1 | 0000,0000b | Power Good status change | | | | Power Enable status change | | | |
| 03h | | CoR | 1 | | PGC4 | PGC3 | PGC2 | PGC1 | PEC4 | PEC3 | PEC2 | PEC1 |
| 04h | DETECTION EVENT | RO | 1 | 0000,0000b | Classification | | | | Detection | | | |
| 05h | | CoR | 1 | | CLSC4 | CLSC3 | CLSC2 | CLSC1 | DETC4 | DETC3 | DETC2 | DETC1 |
| 06h | FAULT EVENT | RO | 1 | 0000,0000b | Disconnect occurred | | | | PCUT fault occurred | | | |
| 07h | | CoR | 1 | | DISF4 | DISF3 | DISF2 | DISF1 | PCUT4 | PCUT3 | PCUT2 | PCUT1 |
| 08h | START/ILIM EVENT | RO | 1 | 0000,0000b | ILIM fault occurred | | | | START fault occurred | | | |
| 09h | | CoR | 1 | | ILIM4 | ILIM3 | ILIM2 | ILIM1 | STRT4 | STRT3 | STRT2 | STRT1 |
| 0Ah | SUPPLY/FAULT EVENT | RO | 1 | 0111,0000b (2) | TSD | VDUV | VDWRN | VPUV | Rsvrd | Rsvrd | OSSE | RAMFLT |
| 0Bh | | CoR | 1 | | | | | | | | | |
| **STATUS** | | | | | | | | | | | | |
| 0Ch | CHANNEL 1 DISCOVERY | RO | 1 | 0000,0000b | Requested CLASS Channel 1 | | | | DETECT Channel 1 | | | |
| 0Dh | CHANNEL 2 DISCOVERY | RO | 1 | 0000,0000b | Requested CLASS Channel 2 | | | | DETECT Channel 2 | | | |
| 0Eh | CHANNEL 3 DISCOVERY | RO | 1 | 0000,0000b | Requested CLASS Channel 3 | | | | DETECT Channel 3 | | | |
| 0Fh | CHANNEL 4 DISCOVERY | RO | 1 | 0000,0000b | Requested CLASS Channel 4 | | | | DETECT Channel 4 | | | |
| 10h | POWER STATUS | RO | 1 | 0000,0000b | PG4 | PG3 | PG2 | PG1 | PE4 | PE3 | PE2 | PE1 |
| 11h | PIN STATUS | RO | 1 | 0,A[4:0],0,0 | Rsvd | SLA4 | SLA3 | SLA2 | SLA1 | SLA0 | Rsvd | Rsvd |
| **CONFIGURATION** | | | | | | | | | | | | |
| 12h | OPERATING MODE | R/W | 1 | 0000,0000b | Channel 4 Mode | | Channel 3 Mode | | Channel 2 Mode | | Channel 1 Mode | |
| 13h | DISCONNECT ENABLE | R/W | 1 | 0000 ,1111b | Rsvd | Rsvd | Rsvd | Rsvd | DCDE4 | DCDE3 | DCDE2 | DCDE1 |
| 14h | DETECT/CLASS ENABLE | R/W | 1 | 0000,0000b | CLE4 | CLE3 | CLE2 | CLE1 | DETE4 | DETE3 | DETE2 | DETE1 |
| 15h | PWRPR/PCUT DISABLE | R/W | 1 | 0000,0000b | OSS4 | OSS3 | OSS2 | OSS1 | DCUT4 | DCUT3 | DCUT2 | DCUT1 |
| 16h | TIMING CONFIG | R/W | 1 | 0000,0000b | TLIM | | TSTART | | TOVLD | | TMPDO | |
| 17h | GENERAL MASK | R/W | 1 | 1000,0000b | INTEN | Rsvd | nbitACC | MbitPrty | CLCHE | DECHE | Rsvd | |

**Table 9-3. Main Registers (continued)**

| Cmd Code | Register or Command Name | $I^2C$ R/W | Data Byte | RST State | Bits Description | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PUSH BUTTONS** | | | | | | | | | | | | |
| 18h | DETECT/CLASS Restart | WO | 1 | 0000,0000b | RCL4 | RCL3 | RCL2 | RCL1 | RDET4 | RDET3 | RDET2 | RDET1 |
| 19h | POWER ENABLE | WO | 1 | 0000,0000b | POFF4 | POFF3 | POFF2 | POFF1 | PWON4 | PWON3 | PWON2 | PWON1 |
| 1Ah | RESET | WO | 1 | 0000,0000b | CLRAIN | CLINP | Rsvd | RESAL | RESP4 | RESP3 | RESP2 | RESP1 |
| **GENERAL/SPECIALIZED** | | | | | | | | | | | | |
| 1Bh | ID | RO | 1 | 0101,0101b | MFR ID | | | | | IC Version | | |
| 1Ch | AUTOCLASS | R/O | 1 | 0000,0000b | AC4 | AC3 | AC2 | AC1 | Rsvrd | Rsvrd | Rsvrd | Rsvrd |
| 1Dh | RESERVED | R/W | 1 | 0000,0000b | Rsrvd | | | | | | | |
| 1Eh | 2P POLICE 1 CONFIG | R/W | 1 | 1111,1111b | 2-Pair POLICE Channel 1 | | | | | | | |
| 1Fh | 2P POLICE 2 CONFIG | R/W | 1 | 1111,1111b | 2-Pair POLICE Channel 2 | | | | | | | |
| 20h | 2P POLICE 3 CONFIG | R/W | 1 | 1111,1111b | 2-Pair POLICE Channel 3 | | | | | | | |
| 21h | 2P POLICE 4CONFIG | R/W | 1 | 1111,1111b | 2-Pair POLICE Channel 4 | | | | | | | |
| 22h | CAP MEASUREMENT(3) | R/W | 1 | 0000,0000b | Rsvd | CDET4 | Rsvd | CDET3 | Rsvd | CDET2 | Rsvd | CDET1 |
| 23h | Reserved | R/W | 1 | 0000,0000b | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd |
| 24h | Power-on FAULT | RO | 1 | 0000,0000b | PF Channel 4 | | PF Channel 3 | | PF Channel 2 | | PF Channel 1 | |
| 25h | | CoR | 1 | | | | | | | | | |
| 26h | RE-MAPPING | R/W | 1 | 1110,0100b | Physical re-map Logical Port 4 | | Physical re-map Logical Port 3 | | Physical re-map Logical Port 2 | | Physical re-map Logical Port 1 | |
| 27h | Multi-Bit Priority 21 | R/W | 1 | 0000,0000b | Rsvd | Channel 2 | | | Rsvd | Channel 1 | | |
| 28h | Multi-Bit Priority 43 | R/W | 1 | 0000,0000b | Rsvd | Channel 4 | | | Rsvd | Channel 3 | | |
| 29h | Port Power Allocation | R/W | 1 | 0000,0000b | Rsvd | MC34 | | | Rsvd | MC12 | | |
| 2A - 2Bh | Reserved | R/W | 1 | 1111,1111b | Rsrvd | | | | | | | |
| 2Ch | TEMPERATURE | RO | 1 | 0000,0000b | Temperature (bits 7 to 0) | | | | | | | |
| 2Dh | Reserved | R/W | 1 | 0000,0000b | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd |
| 2Eh | INPUT VOLTAGE | RO | 2 | 0000,0000b | Input Voltage: LSByte | | | | | | | |
| 2Fh | | RO | | 0000,0000b | Rsvd | Rsvd | Input Voltage: MSByte (bits 13 to 8) | | | | | |
| **EXTENDED REGISTER SET – PARAMETRIC MEASUREMENT** | | | | | | | | | | | | |
| 30h | Channel 1 CURRENT | RO | 2 | 0000,0000b | Channel 1 Current: LSByte | | | | | | | |
| 31h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 1 Current: MSByte (bits 13 to 8) | | | | | |
| 32h | Channel 1 VOLTAGE | RO | 2 | 0000,0000b | Channel 1 Voltage: LSByte | | | | | | | |
| 33h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 1 Voltage: MSByte (bits 13 to 8) | | | | | |

(1) SUPF bit reset state shown is at Power up only
(2) VDUV, VPUV and VDWRN bits reset state shown is at Power up only
(3) Capacitance Measurement is only supported if SRAM code is programmed

## Table 9-4. Main Registers

| Cmd Code | Register or Command Name | $I^2C$ R/W | Data Byte | RST State | Bits Description | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 34h | Channel 2 CURRENT | RO | 2 | 0000,0000b | Channel 2 Current: LSByte | | | | | | | |
| 35h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 2 Current: MSByte (bits 13 to 8) | | | | | |
| 36h | Channel 2 VOLTAGE | RO | 2 | 0000,0000b | Channel 2 Voltage: LSByte | | | | | | | |
| 37h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 2 Voltage: MSByte (bits 13 to 8) | | | | | |
| 38h | Channel 3 CURRENT | RO | 2 | 0000,0000b | Channel 3 current: LSByte | | | | | | | |
| 39h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 3 Current: MSByte (bits 13 to 8) | | | | | |
| 3Ah | Channel 3 VOLTAGE | RO | 2 | 0000,0000b | Channel 3 Voltage: LSByte | | | | | | | |
| 3Bh | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 3 Voltage: MSByte (bits 13 to 8) | | | | | |
| 3Ch | Channel 4 CURRENT | RO | 2 | 0000,0000b | Channel 4 current: LSByte | | | | | | | |
| 3Dh | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 4 Current: MSByte (bits 13 to 8) | | | | | |
| 3Eh | Channel 4 VOLTAGE | RO | 2 | 0000,0000b | Channel 4 Voltage: LSByte | | | | | | | |
| 3Fh | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 4 Voltage: MSByte (bits 13 to 8) | | | | | |
| **CONFIGURATION/OTHERS** | | | | | | | | | | | | |
| 40h | CHANNEL FOLDBACK | R/W | 1 | 0000,0000b | 2xFB4 | 2xFB3 | 2xFB2 | 2xFB1 | Rsvd | Rsvd | Rsvd | Rsvd |
| 41h | FIRMWARE REVISION | RO | 1 | RRRR,RRRRb | Firmware Revision | | | | | | | |
| 42h | I2C WATCHDOG | R/W | 1 | 0001,0110b | Rsvd | Rsvd | Rsvd | Watchdog Disable | | | | WDS |
| 43h | DEVICE ID | RO | 1 | 0011,0011b | Device ID number | | | | Silicon Revision number | | | |
| **SIGNATURE MEASUREMENTS** | | | | | | | | | | | | |
| 44h | Ch1 DETECT RESISTANCE | RO | 1 | 0000,0000b | Channel 1 Resistance | | | | | | | |
| 45h | Ch2 DETECT RESISTANCE | RO | 1 | 0000,0000b | Channel 2 Resistance | | | | | | | |
| 46h | Ch3 DETECT RESISTANCE | RO | 1 | 0000,0000b | Channel 3 Resistance | | | | | | | |
| 47h | Ch4 DETECT RESISTANCE | RO | 1 | 0000,0000b | Channel 4 Resistance | | | | | | | |
| 48h | Ch1 CAP MEASUREMENT (3) | RO | 1 | 0000,0000b | Channel 1 Capacitance | | | | | | | |
| 49h | Ch2 CAP MEASUREMENT (3) | RO | 1 | 0000,0000b | Channel 2 Capacitance | | | | | | | |
| 4Ah | Ch3 CAP MEASUREMENT (3) | RO | 1 | 0000,0000b | Channel 3 Capacitance | | | | | | | |
| 4Bh | Ch4 CAP MEASUREMENT (3) | RO | 1 | 0000,0000b | Channel 4 Capacitance | | | | | | | |

**Table 9-4. Main Registers (continued)**

| Cmd Code | Register or Command Name | $I^2C$ R/W | Data Byte | RST State | Bits Description | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ASSIGNED CHANNEL STATUS | | | | | | | | | | | | |
| 4Ch | ASSIGNED CLASS CHANNEL 1 | RO | 1 | 0000,0000b | Assigned CLASS Channel 1 | | | | Previous CLASS Channel 1 | | | |
| 4Dh | ASSIGNED CLASS CHANNEL 2 | RO | 1 | 0000,0000b | Assigned CLASS Channel 2 | | | | Previous CLASS Channel 2 | | | |
| 4Eh | ASSIGNED CLASS CHANNEL 3 | RO | 1 | 0000,0000b | Assigned CLASS Channel 3 | | | | Previous CLASS Channel 3 | | | |
| 4Fh | ASSIGNED CLASS CHANNEL 4 | RO | 1 | 0000,0000b | Assigned CLASS Channel 4 | | | | Previous CLASS Channel 4 | | | |
| AUTOCLASS CONFIGURATION/MEASUREMENTS | | | | | | | | | | | | |
| 50h | AUTOCLASS CONTROL | R/W | 1 | 0000,0000b | MAC4 | MAC3 | MAC2 | MAC1 | AAC4 | AAC3 | AAC2 | AAC1 |
| 51h | CHANNEL 1 AUTOCLASS PWR | RO | 1 | 0000,0000b | Rsrvd | Channel 1 AutoClass Power | | | | | | |
| 52h | CHANNEL 2 AUTOCLASS PWR | RO | 1 | 0000,0000b | Rsrvd | Channel 2 AutoClass Power | | | | | | |
| 53h | CHANNEL 3 AUTOCLASS PWR | RO | 1 | 0000,0000b | Rsrvd | Channel 3 AutoClass Power | | | | | | |
| 54h | CHANNEL 4 AUTOCLASS PWR | RO | 1 | 0000,0000b | Rsrvd | Channel 4 AutoClass Power | | | | | | |
| MISCELLANEOUS | | | | | | | | | | | | |
| 55h | ALTERNATIVE FOLDBACK | R/W | 1 | 0000,0000b | ALTFB4 | ALTFB3 | ALTFB 2 | ALTFB1 | ALTIR4 | ALTIR3 | ALTIR2 | ALTIR1 |
| 56h - 5Fh | RESERVED | R/W | 1 | 0000,0000b | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd |
| SRAM | | | | | | | | | | | | |
| 60h | SRAM CONTROL | R/W | 1 | 0000,0000b | PROG_SEL | CPU_RST | Rsrvd | PAR_EN | RAM_EN | PAR_SEL | RZ/W | CLR_PTR |
| 61h | SRAM DATA | R/W | - | - | SRAM DATA - Read and Write (continuous) | | | | | | | |
| 62h | START ADDRESS | R/W | 1 | 0000,0000b | Programming Start Address (LSB) | | | | | | | |
| 63h | | R/W | 1 | 0000,0000b | Programming Start Address (MSB) | | | | | | | |
| 64h - 6Fh | RESERVED | R/W | 1 | 0000,0000b | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd |

### 9.6.2 Detailed Register Descriptions

#### *9.6.2.1 INTERRUPT Register*

COMMAND = 00h with 1 Data Byte, Read only

Active high, each bit corresponds to a particular event that occurred. Each bit can be individually reset by doing a read at the corresponding event register address, or by setting bit 7 of Reset register.

Any active bit of Interrupt register activates the $\overline{\text{INT}}$ output if its corresponding Mask bit in INTERRUPT Mask register (01h) is set, as well as the INTEN bit in the General Mask register.

**Figure 9-6. INTERRUPT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SUPF | STRTF | IFAULT | CLASC | DETC | DISF | PGC | PEC |
| R-1 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-5. INTERRUPT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SUPF | R | 1 | Indicates that a Supply Event Fault or SRAM memory fault occurred<br>SUPF = TSD \|\| VDUV \|\| VDWRN \|\| VPUV \|\| RAMFLT<br>1 = At least one Supply Event Fault or SRAM memory fault occurred<br>0 = No such event occurred |
| 6 | STRTF | R | 0 | Indicates that a $t_{START}$ Fault occurred on at least one channel.<br>STRTF = STRT1 \|\| STRT2 \|\| STRT3 \|\| STRT4<br>1 = $t_{START}$ Fault occurred for at least one channel<br>0 = No $t_{START}$ Fault occurred |
| 5 | IFAULT | R | 0 | Indicates that a $t_{OVLD}$ or $t_{LIM}$ Fault occurred on at least one channel.<br>IFAULT = PCUT1 \|\| PCUT2 \|\| PCUT3 \|\| PCUT4 \|\| ILIM1 \|\| ILIM2 \|\| ILIM3 \|\| ILIM4<br>1 = $t_{OVLD}$ and/or $t_{LIM}$ Fault occurred for at least one channel<br>0 = No $t_{OVLD}$ nor $t_{LIM}$ Fault occurred |
| 4 | CLASC | R | 0 | Indicates that at least one classification cycle occurred on at least one channel<br>CLASC = CLSC1 \|\| CLSC2 \|\| CLSC3 \|\| CLSC4<br>1 = At least one classification cycle occurred for at least one channel<br>0 = No classification cycle occurred |
| 3 | DETC | R | 0 | Indicates that at least one detection cycle occurred on at least one channel<br>DETC = DETC1 \|\| DETC2 \|\| DETC3 \|\| DETC4<br>1 = At least one detection cycle occurred for at least one channel<br>0 = No detection cycle occurred |
| 2 | DISF | R | 0 | Indicates that a disconnect event occurred on at least one channel.<br>DISF = DISF1 \|\| DISF2 \|\| DISF3 \|\| DISF4<br>1 = Disconnect event occurred for at least one channel<br>0 = No disconnect event occurred |
| 1 | PGC | R | 0 | Indicates that a power good status change occurred on at least one channel.<br>PGC = PGC1 \|\| PGC2 \|\| PGC3 \|\| PGC4<br>1 = Power good status change occurred on at least one channel<br>0 = No power good status change occurred |

### Table 9-5. INTERRUPT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 0 | PEC | R | 0 | Indicates that a power enable status change occurred on at least one channel<br>PEC = PEC1 \|\| PEC2 \|\| PEC3 \|\| PEC4<br>1 = Power enable status change occurred on at least one channel<br>0 = No power enable status change occurred |

### 9.6.2.2 INTERRUPT MASK Register

COMMAND = 01h with 1 Data Byte, Read/Write

Each bit corresponds to a particular event or fault as defined in the Interrupt register.

Writing a 0 into a bit will mask the corresponding event/fault from activating the $\overline{\text{INT}}$ output.

Note that the bits of the Interrupt register always change state according to events or faults, regardless of the state of the state of the Interrupt Mask register.

Note that the INTEN bit of the General Mask register must also be set in order to allow an event to activate the $\overline{\text{INT}}$ output.

**Figure 9-7. INTERRUPT MASK Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SUMSK | STMSK | IFMSK | CLMSK | DEMSK | DIMSK | PGMSK | PEMSK |
| R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-6. INTERRUPT MASK Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SUMSK | R/W | 1 | Supply Event Fault mask bit.<br>1 = Supply Event Fault will activate the $\overline{\text{INT}}$ output.<br>0 = Supply Event Fault will have no impact on $\overline{\text{INT}}$ output. |
| 6 | STMSK | R/W | 0 | $t_{START}$ Fault mask bit.<br>1 = $t_{START}$ Fault will activate the $\overline{\text{INT}}$ output.<br>0 = $t_{START}$ Fault will have no impact on $\overline{\text{INT}}$ output. |
| 5 | IFMSK | R/W | 0 | $t_{OVLD}$ or $t_{LIM}$ Fault mask bit.<br>1 = $t_{OVLD}$ and/or $t_{LIM}$ Fault occurrence will activate the $\overline{\text{INT}}$ output<br>0 = $t_{OVLD}$ and/or $t_{LIM}$ Fault occurrence will have no impact on $\overline{\text{INT}}$ output |
| 4 | CLMSK | R/W | 0 | Classification cycle mask bit.<br>1 = Classification cycle occurrence will activate the $\overline{\text{INT}}$ output.<br>0 = Classification cycle occurrence will have no impact on $\overline{\text{INT}}$ output. |
| 3 | DEMSK | R/W | 0 | Detection cycle mask bit.<br>1 = Detection cycle occurrence will activate the $\overline{\text{INT}}$ output.<br>0 = Detection cycle occurrence will have no impact on $\overline{\text{INT}}$ output. |
| 2 | DIMSK | R/W | 0 | Disconnect event mask bit.<br>1 = Disconnect event occurrence will activate th $\overline{\text{INT}}$ output.<br>0 = Disconnect event occurrence will have no impact on $\overline{\text{INT}}$ output. |
| 1 | PGMSK | R/W | 0 | Power good status change mask bit.<br>1 = Power good status change will activate the $\overline{\text{INT}}$ output.<br>0 = Power good status change will have no impact on $\overline{\text{INT}}$ output. |
| 0 | PEMSK | R/W | 0 | Power enable status change mask bit.<br>1 = Power enable status change will activate the $\overline{\text{INT}}$ output.<br>0 = Power enable status change will have no impact on $\overline{\text{INT}}$ output. |

### *9.6.2.3 POWER EVENT Register*

COMMAND = 02h with 1 Data Byte, Read only

COMMAND = 03h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual channel.

A read at each location (02h or 03h) returns the same register data with the exception that the Clear on Read command clears all bits of the register.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

**Figure 9-8. POWER EVENT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PGC4 | PGC3 | PGC2 | PGC1 | PEC4 | PEC3 | PEC2 | PEC1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

**Table 9-7. POWER EVENT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | PGC4–PGC1 | R or CR | 0 | Indicates that a power good status change occurred.<br>1 = Power good status change occurred<br>0 = No power good status change occurred |
| 3–0 | PEC4–PEC1 | R or CR | 0 | Indicates that a power enable status change occurred.<br>1 = Power enable status change occurred<br>0 = No power enable status change occurred |

#### *9.6.2.4 DETECTION EVENT Register*

COMMAND = 04h with 1 Data Byte, Read only

COMMAND = 05h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual channel.

A read at each location (04h or 05h) returns the same register data with the exception that the Clear on Read command clears all bits of the register. These bits are cleared when channel-n is turned off.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

**Figure 9-9. DETECTION EVENT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLSC4 | CLSC3 | CLSC2 | CLSC1 | DETC4 | DETC3 | DETC2 | DETC1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

**Table 9-8. DETECTION EVENT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | CLSC4–CLSC1 | R or<br>CR | 0 | Indicates that at least one classification cycle occurred if the CLCHE bit in General Mask register is low. Conversely, it indicates when a change of class occurred if the CLCHE bit is set.<br>1 = At least one classification cycle occurred (if CLCHE = 0) or a change of class occurred (CLCHE = 1)<br>0 = No classification cycle occurred (if CLCHE = 0) or no change of class occurred (CLCHE = 1) |
| 3–0 | DETC4–DETC1 | R or<br>CR | 0 | Indicates that at least one detection cycle occurred if the DECHE bit in General Mask register is low. Conversely, it indicates when a change in detection occurred if the DECHE bit is set.<br>1 = At least one detection cycle occurred (if DECHE = 0) or a change in detection occurred (DECHE = 1)<br>0 = No detection cycle occurred (if DECHE = 0) or no change in detection occurred (DECHE = 1) |

#### *9.6.2.5 FAULT EVENT Register*

COMMAND = 06h with 1 Data Byte, Read only

COMMAND = 07h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual channel.

A read at each location (06h or 07h) returns the same register data with the exception that the Clear on Read command clears all bits of the register. These bits are cleared when channel-n is turned off.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

**Figure 9-10. FAULT EVENT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DISF4 | DISF3 | DISF2 | DISF1 | PCUT4 | PCUT3 | PCUT2 | PCUT1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

**Table 9-9. FAULT EVENT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | DISF4–DISF1 | R or CR | 0 | Indicates that a disconnect event occurred.<br>1 = Disconnect event occurred<br>0 = No disconnect event occurred |
| 3–0 | PCUT4–PCUT1 | R or CR | 0 | Indicates that a $t_{OVLD}$ Fault occurred.<br>1 = $t_{OVLD}$ Fault occurred<br>0 = No $t_{OVLD}$ Fault occurred |

Clearing a PCUT event has no impact on the TLIM or TOVLD counters.

### 9.6.2.6 START/ILIM EVENT Register

COMMAND = 08h with 1 Data Byte, Read only

COMMAND = 09h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual channel.

A read at each location (08h or 09h) returns the same register data with the exception that the Clear on Read command clears all bits of the register. These bits are cleared when channel-n is turned off.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

**Figure 9-11. START/ILIM EVENT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ILIM4 | ILIM3 | ILIM2 | ILIM1 | STRT4 | STRT3 | STRT2 | STRT1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

**Table 9-10. START/ILIM EVENT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | ILIM4–ILIM1 | R or CR | 0 | Indicates that a $t_{LIM}$ fault occurred, which means the channel has limited its output current to $I_{LIM}$ or the folded back $I_{LIM}$ for more than $t_{LIM}$.<br>1 = $t_{LIM}$ fault occurred<br>0 = No $t_{LIM}$ fault occurred |
| 3–0 | STRT4–STRT1 | R or CR | 0 | Indicates that a $t_{START}$ fault occurred during turn on.<br>1 = $t_{START}$ fault or class/detect error occurred<br>0 = No $t_{START}$ fault or class/detect error occurred |

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**Note**

When a Start Fault is reported and the PECn bit in Power Event register is set, then there is an Inrush fault.

When a Start Fault is reported and the PECn bit is **not** set, then the Power-On Fault register (0x24h) will indicate the cause of the fault.

In AUTO mode, STRTn faults will not be reported and register 0x24h will not be updated due to invalid discovery results.

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#### *9.6.2.7 SUPPLY and FAULT EVENT Register*

COMMAND = 0Ah with 1 Data Byte, Read only

COMMAND = 0Bh with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

A read at each location (0Ah or 0Bh) returns the same register data with the exception that the Clear on Read command clears all bits of the register.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

**Figure 9-12. SUPPLY and FAULT EVENT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TSD | VDUV | VDWRN | VPUV | Rsvrd | Rsvrd | OSSE | RAMFLT |
| R | R | R | R | R | R | R | R |
| CR | CR | CR | CR | CR | CR | CR | CR |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

**Table 9-11. SUPPLY and FAULT EVENT Register Field Descriptions**

| Bit | Field | Type | POR/RST | Description |
|---|---|---|---|---|
| 7 | TSD | R or CR | 0 / P | Indicates that a thermal shutdown occurred. When there is thermal shutdown, all channels are turned off and are put in OFF mode. The internal circuitry continues to operate however, including the ADCs. Note that at as soon as the internal temperature has decreased below the low threshold, the channels can be turned back ON regardless of the status of the TSD bit.<br>1 = Thermal shutdown occurred<br>0 = No thermal shutdown occurred |
| 6 | VDUV | R or CR | 1 / P | Indicates that a VDD UVLO occurred.<br>1 = VDD UVLO occurred<br>0 = No VDD UVLO occurred |
| 5 | VDWRN | R or CR | 1 / P | Indicates that the VDD has fallen under the UVLO warning threshold.<br>1 = VDD UV Warning occurred<br>0 = No VDD UV warning occurred |
| 4 | VPUV | R or CR | 1 / P | Indicates that a VPWR undervoltage occurred.<br>1 = VPWR undervoltage occurred<br>0 = No VPWR undervoltage occurred |
| 3-2 | Rsvrd | R or CR | 0 / 0 | Reserved |
| 1 | OSSE | R or CR | 0 / 0 | Indicates that an OSS Event occurred<br>1 = one or more channels with a group of 4 were disabled due to the assertion of the OSS pin or provided 3-bit OSS code<br>0 = No OSS events occurred |
| 0 | RAMFLT | R or CR | 0 / 0 | Indicates that a SRAM fault has occurred<br>1 = SRAM fault occurred<br>0 = No SRAM fault occurred |

**Note**

The RST condition of "P" indicates that the previous state of these bits will be preserved following a device reset using the $\overline{\text{RESET}}$ pin. Thus, pulling the $\overline{\text{RESET}}$ input low will not clear the TSD, VDUV, VDWRN, or VPUV bits.

**Note**

While the VPUV bit is set, any PWONn commands will be ignored until $V_{VPWR}$ > 30 V.

During VPUV undervoltage condition, the Detection Event register (CLSCn, DETCn) is not cleared, unless VPWR also falls below the VPWR UVLO falling threshold (approximately18 V).

A clear on Read will not effectively clear VDUV bit as long as the VPWR undervoltage condition is maintained.

**Note**

In 1-bit mode (MbitPrty = 0 in reg 0x17), the OSSE bit will be set anytime a channel within a group of 4 has OSS enabled and the OSS pin is asserted.

In 3-bit mode (MbitPrty = 1 in reg 0x17), the OSSE bit will be set anytime a 3-bit priority code is sent that is equal to or greater than the MBPn settings in registers 0x27 and 0x28 channel for a group of 4 channels.

#### 9.6.2.7.1 Detected SRAM Faults and "Safe Mode"

The TPS23882 is configured with internal SRAM memory fault monitoring, and in the event that an error is detected with the SRAM memory, the device will enter “safe mode”. While in “Safe mode” the FW Revision value in register 0x41 will be set to 0xFFh.

Any channels that are currently powered will remain powered, but the majority of the operation will be disabled until the SRAM can be reloaded. The device UVLO and Thermal Shutdown features in addition to the disconnect and current foldback functions for the powered channels will be preserved in “safe mode”.

Any channels that were not powered prior to the SRAM fault detection will be set to OFF mode (see register 0x12h description for additional changes that will occur as a result of the change to OFF mode). Port Remapping (0x26h) and any other channel configuration settings (ie Power Allocation 0x29h) will be preserved.

Upon detection of a SRAM fault the “RAM_EN” bit in 0x60 will be cleared and the RAMFLT bit will be set in register 0x0A. The internal firmware will continue to run in “safe mode” until this bit is set again by the host after the SRAM is reloaded or a POR (Power on Reset) event occurs. In order to ensure a smooth transition into and out of “safe mode”, any I2C commands other than those to reprogram the SRAM need to be deferred until after the SRAM is reloaded and determined to be “valid” (see register 0x60 SRAM programing descriptions).

**Note**

Once set, the RAMFLT bit will remain set even after the device is removed from safe mode. it is recommend that this bit be cleared prior to setting the RAM_EN bit in register 0x60 following the SRAM reload.

**Note**

The PAR_EN bit in reg 0x60 must be set and the corresponding SRAM_Parity code (available for download from the *TI mySecure Software* webpage) must be loaded into the device in order for the SRAM fault monitoring to be active.

Please refer to the *How to Load TPS2388x SRAM Code* document for more information on the recommended SRAM programming procedure.

#### *9.6.2.8 CHANNEL 1 DISCOVERY Register*

COMMAND = 0Ch with 1 Data Byte, Read Only

**Figure 9-13. CHANNEL 1 DISCOVERY Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REQUESTED CLASS Ch1 | | | | DETECT Ch1 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### *9.6.2.9 CHANNEL 2 DISCOVERY Register*

COMMAND = 0Dh with 1 Data Byte, Read Only

**Figure 9-14. CHANNEL 2 DISCOVERY Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REQUESTED CLASS Ch2 | | | | DETECT Ch2 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### *9.6.2.10 CHANNEL 3 DISCOVERY Register*

COMMAND = 0Eh with 1 Data Byte, Read Only

**Figure 9-15. CHANNEL 3 DISCOVERY Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REQUESTED CLASS Ch3 | | | | DETECT Ch3 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### *9.6.2.11 CHANNEL 4 DISCOVERY Register*

COMMAND = 0Fh with 1 Data Byte, Read Only

**Figure 9-16. CHANNEL 4 DISCOVERY Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REQUESTED CLASS Ch4 | | | | DETECT Ch4 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Bit Descriptions:** These bits represent the most recent **"requested"** classification and detection results for channel n. These bits are cleared when channel n is turned off.

### Table 9-12. CHANNEL n DISCOVERY Register Field Descriptions

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7–4</td><td>RCLASS Ch-n</td><td>R</td><td>0</td><td>Most recent classification result on channel n.<br>The selection is as following:
<table>
<tr><th colspan="4">RCLASS Ch-n</th><th>Requested Class</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Unknown</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Class 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Class 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Class 3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Class 4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Reserved – read as Class 0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Class 0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Class Overcurrent</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Class 5 - 4-Pair Single Signature</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Class 6 - 4-Pair Single Signature</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Class 7 - 4-Pair Single Signature</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Class 8 - 4-Pair Single Signature</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Class 4+ - Type-1 Limited</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Class 5 - 4-Pair Dual Signature</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Class Mismatch</td></tr>
</table>
</td></tr>
<tr><td>3–0</td><td>DETECT Ch-n</td><td>R</td><td>0</td><td>Most recent detection result on channel n.<br>The selection is as following:
<table>
<tr><th colspan="4">DETECT Ch-n</th><th>Detection Status</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Unknown</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Short-circuit</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Too Low</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Valid</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Too High</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Open Circuit</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>MOSFET fault</td></tr>
</table>
</td></tr>
</table>

“Requested” vs. “Assigned” Classification: The “requested” class is the classification the PSE measures during Mutual Identification prior to turn on, whereas the “assigned” class is the classification level the channel was powered on with based on the Power Allocation setting in register 0x29h. The “assigned” classification values are available in registers 0x4C-4F

---

**Note**

Due to the need to power on after 1 class finger, the "Class 4+ - Type 1 Limited" Requested Class is reported anytime a Class 4 or higher PD is powered with register 0x29 configured for 15.5W.

Upon being powered, devices that present a class 0 signature during discovery will be given an assigned class of "Class 3"

Even though the TPS23882 is a 2-pair PSE controller, due to the use of 3-finger classification, it is still capable of identifying if a Class 5+ 4-pair PDs is connected.

---

#### *9.6.2.12 POWER STATUS Register*

COMMAND = 10h with 1 Data Byte, Read only

Each bit represents the actual power status of a channel.

Each bit xx1-4 represents an individual channel.

These bits are cleared when channel-n is turned off, including if the turn off is caused by a fault condition.

**Figure 9-17. POWER STATUS Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PG4 | PG3 | PG2 | PG1 | PE4 | PE3 | PE2 | PE1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-13. POWER STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | PG4–PG1 | R | 0 | Each bit, when at 1, indicates that the channel is on and that the voltage at DRAINn pin has gone below the power good threshold during turn on.<br>These bits are latched high once the turn on is complete and can only be cleared when the channel is turned off or at RESET/POR.<br>1 = Power is good<br>0 = Power is not good |
| 3–0 | PE4–PE1 | R | 0 | Each bit indicates the ON/OFF state of the corresponding channel.<br>1 = Channel is on<br>0 = Channel is off |

### 9.6.2.13 PIN STATUS Register

COMMAND = 11h with 1 Data Byte, Read Only

**Figure 9-18. PIN STATUS Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SLA4 | SLA3 | SLA2 | SLA1 | SLA0 | 0 | 0 |
| 0 | A4 pin | A3 pin | A2 pin | A1 pin | 0/1[1] | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) If Configuration A, it can be 0 or 1. If configuration B, it is 0.

**Table 9-14. PIN STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 6-3 | SLA4-SLA1 | R | See above | I$^2$C device address, as defined while using pins A4-A1. |
| 2 | SLA0 | R | | SLA0 bit is internally defined to 0 or 1<br>0 = Channel 1-4<br>1 = Channels 5-8 |
| 7, 1-0 | - | R | | Reserved |

| DESCRIPTION | BINARY DEVICE ADDRESS | | | | | | | ADDRESS PINS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 6 | 5 | 4 | 3 | 2 | 1 | 0 | A4 | A3 | A2 | A1 |
| Broadcast access | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | X | X | X |
| Slave 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0/1 | GND | GND | GND | GND |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0/1 | GND | GND | GND | HIGH |
| | 0 | 1 | 0 | 0 | 1 | 0 | 0/1 | GND | GND | HIGH | GND |
| | 0 | 1 | 0 | 0 | 1 | 1 | 0/1 | GND | GND | HIGH | HIGH |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0/1 | GND | HIGH | GND | GND |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0/1 | GND | HIGH | GND | HIGH |
| | 0 | 1 | 0 | 1 | 1 | 0 | 0/1 | GND | HIGH | HIGH | GND |
| | 0 | 1 | 0 | 1 | 1 | 1 | 0/1 | GND | HIGH | HIGH | HIGH |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0/1 | HIGH | GND | GND | GND |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0/1 | HIGH | GND | GND | HIGH |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0/1 | HIGH | GND | HIGH | GND |
| | 0 | 1 | 1 | 0 | 1 | 1 | 0/1 | HIGH | GND | HIGH | HIGH |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0/1 | HIGH | HIGH | GND | GND |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0/1 | HIGH | HIGH | GND | HIGH |
| | 0 | 1 | 1 | 1 | 1 | 0 | 0/1 | HIGH | HIGH | HIGH | GND |
| Slave 15 | 0 | 1 | 1 | 1 | 1 | 1 | 0/1 | HIGH | HIGH | HIGH | HIGH |

### *9.6.2.14 OPERATING MODE Register*

COMMAND = 12h with 1 Data Byte, Read/Write

**Figure 9-19. OPERATING MODE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| C4M1 | C4M0 | C3M1 | C3M0 | C2M1 | C2M0 | C1M1 | C1M0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-15. OPERATING MODE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CnM1–CnM0 | R/W | 0 | Each pair of bits configures the operating mode per channel.<br>The selection is as following:<br>**M1** \| **M0** \| **Operating Mode**<br>0 \| 0 \| OFF<br>0 \| 1 \| Diagnostic/Manual<br>1 \| 0 \| Semiauto<br>1 \| 1 \| Auto |

**OFF MODE:**

In OFF mode, the Channel is OFF and neither detection nor classification is performed independent of the DETE, CLSE or PWON bits.

The table below depicts what bits will be cleared when a channel is changed to OFF mode from any other operating mode:

**Table 9-16. Transition to OFF Mode**

| Register | Bits to be reset |
|---|---|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

**Note**

it may take upwards of 5 ms before all of the registers are cleared following a change to OFF mode.

Only the bits associated with the channel/port ("n") being set into OFF mode will be cleared. Those bits associated with channels/ports remaining in operation will not be changed.

In the event either the PGn or PEn bits were changed from a 1 to a zero, the corresponding PGCn and PECn bits will be set in the POWER EVENT register 0x02h.

Also, a change of mode from semiauto to manual/diagnostic mode or OFF mode will cancel any ongoing cooldown time period.

## DIAGNOSTIC/MANUAL MODE:

In Manual/Diagnostic mode, there is no automatic state change. The channel remains idle until DETE, CLSE (0x14h or 0x18h), or PWON command is provided. Upon the setting of the DETE and/or CLSE bits, the channel will perform a singular detection and/or classification cycle on the corresponding channel.

---

**Note**

Setting a PWONn bit in register 0x19 results in the immediate turn on of that channel.

There is no Assigned Class assigned for ports/channels powered out of Manual/Diagnostic mode. Any settings such as the port power policing and 1x/2x foldback selection that are typically configure based on the assigned class result need to manually configured by the user.

---

**Note**

Setting a PWONn bit in register 0x19 results in the immediate turn on of that channel.

---

## SEMI AUTO MODE:

In Semi Auto mode, as long as the Channel is unpowered, detection and classifications may be performed continuously depending if the corresponding class and detect enable bits are set (register 0x14h).

**Table 9-17. Channel Behavior in Semi Auto Mode**

| CLEn | DETn | Channel Operation |
|---|---|---|
| 0 | 0 | Idle |
| 0 | 1 | Cycling Detection Measurements only |
| 1 | 0 | Idle |
| 1 | 1 | Cycling Detection and Classification Measurements |

### AUTO MODE:

In **Auto mode**, channels will automatically power on any valid detection and classification signature based on the Port Power Allocation settings in 0x29. The channels will remain idle until DETE and CLSE (0x14 or 0x18) are set, or a PWON command is given.

Prior to setting DETE and CLE or sending a PWON command in AUTO mode, the following registers need to be configured according to the system requirements and configuration:

| Register | Bits |
|---|---|
| 0x26 | Port Re-mapping |
| 0x29 | Port Power Allocation |
| 0x50 | Auto AC Enable |
| 0x55 | Alternative Inrush and Powered Foldback Enable |

**Note**

Changes to these registers after the DETE and CLE bits are set in Auto mode may result in undesired or non IEEE complaint operation.

The following registers may be configured or changed after turn on if changes to the default operation are desired as these values are internally set during power on based on the port configuration and resulting assigned PD class:

| Register | Bits |
|---|---|
| 0x1E-21 | 2-Pair Policing |
| 0x40 | 2x Foldback Enable |

#### 9.6.2.15 DISCONNECT ENABLE Register

COMMAND = 13h with 1 Data Byte, Read/Write

**Bit Descriptions:** Defines the disconnect detection mechanism for each channel.

**Figure 9-20. DISCONNECT ENABLE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | DCDE4 | DCDE3 | DCDE2 | DCDE1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-18. DISCONNECT ENABLE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | — | R/W | 0 | |
| 3–0 | DCDE4–DCDE1 | R/W | 1 | DC disconnect enable<br>1 = DC Disconnect Enabled<br>0 = DC Disconnect Disabled<br>Look at the TIMING CONFIGURATION register for more details on how to define the TDIS time period. |

DC disconnect consists in measuring the Channel DC current at SENn, starting a timer ($T_{DIS}$) if this current is below a threshold and turning the Channel off if a time-out occurs. Also, the corresponding disconnect bit (DISFn) in the FAULT EVENT register is set accordingly. The $T_{DIS}$ counter is reset each time the current rises above the disconnect threshold for at least 3 msec. The counter does not decrement below zero.

#### *9.6.2.16 DETECT/CLASS ENABLE Register*

COMMAND = 14h with 1 Data Byte, Read/Write

During $t_{OVLD}$, $t_{LIM}$ or $t_{START}$ cool down cycle, any Detect/Class Enable command for that channel will be delayed until end of cool-down period. Note that at the end of cool down cycle, one or more detection/class cycles are automatically restarted as described previously, if the class and/or detect enable bits are set.

**Figure 9-21. DETECT/CLASS ENABLE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLE4 | CLE3 | CLE2 | CLE1 | DETE4 | DETE3 | DETE2 | DETE1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-19. DETECT/CLASS ENABLE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | CLE4-CLE1 | R/W | 0 | Classification enable bits. |
| 3–0 | DETE4-DETE1 | R/W | 0 | Detection enable bits. |

**Bit Descriptions:**

Detection and classification enable for each channel.

When in Manual mode, setting a bit means that only one cycle (detection or classification) is performed for the corresponding channel. The bit is automatically cleared by the time the cycle has been completed.

Note that similar result can be obtained by writing to the Detect/Class Restart register 0x18.

It is also cleared if a turn off (Power Enable register) command is issued.

When in semiauto mode, as long as the port is kept off, detection and classification are performed continuously, as long as the class and detect enable bits are kept set, but the class will be done only if the detection was valid. A Detect/Class Restart PB command can also be used to set the CLEn and DETEn bits, if in semiauto mode.

### *9.6.2.17 Power Priority / 2Pair PCUT Disable Register Name*

COMMAND = 15h with 1 Data Byte, R/W

**Figure 9-22. Power Priority / 2P-PCUT Disable Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OSS4 | OSS3 | OSS2 | OSS1 | DCUT4 | DCUT3 | DCUT2 | DCUT1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-20. Power Priority / 2P-PCUT Disable Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | OSS4-OSS1 | R/W | 0 | Power priority bits:<br>When the MBitPrty bit in 0x17 =0:<br>1 = When the OSS signal is asserted, the corresponding channel is powered off.<br>0 = OSS signal has no impact on the channel. |
| 3–0 | DCUT4-DCUT1 | R/W | 0 | 2-Pair PCUT disable for each channel. Used to prevent removal of the associated channel's power due to a 2-Pair PCUT fault, regardless of the programming status of the Timing Configuration register. Note that there is still monitoring of ILIM faults.<br>1: Channel's PCUT is disabled. This means that an PCUT fault alone will not turn off this channel.<br>0: Channel's PCUT is enabled. This enables channel turn off if there is PCUT fault. |

---

**Note**

If the MbitPrty bit = 1 (0x17h): The OSSn bits must be cleared to ensure proper operation. Refer to registers 0x27/28h for more information on the Multi-bit priority shutdown feature.

---

**Note**

If DCUT = 1 for a channel, the channel will not be automatically turned off during a PCUT fault condition. However, the PCUT fault flag will still be operational, with a fault timeout equal to $t_{OVLD}$.

Any change in the state of DCUTn bits will result in the resetting of the $T_{OVLD}$ timer for that channel.

---

The OSSn bits are used to determine which channels are shut down in response to an external assertion of the OSS fast shutdown signal.

The turn off procedure due to OSS is similar to a channel reset or change to OFF mode, with the exception that OSS does not cancel any ongoing fault cool down timers. the table below includes the bits that will be cleared when a channel is disabled due to OSS:

**Table 9-21. Channel Turn Off with OSS**

| Register | Bits to be reset |
|---|---|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

**Note**

it may take upwards of 5 ms before all of the registers are cleared following an OSS event.

Only the bits associated with the channel/port ("n") with OSS enabled will be cleared. Those bits associated with channels/ports remaining in operation will not be changed.

### *9.6.2.18 TIMING CONFIGURATION Register*

COMMAND = 16h with 1 Data Byte, Read/Write

**Bit Descriptions**: These bits define the timing configuration for **all four** channels.

**Figure 9-23. TIMING CONFIGURATION Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TLIM | | TSTART | | TOVLD | | TMPDO | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-22. TIMING CONFIGURATION Register Field Descriptions**

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7 –6</td><td>TLIM</td><td>R/W</td><td>0</td><td>ILIM fault timing, which is the output current limit time duration before channel turn off.<br>When a 2xFBn bit in register 0x40 = 0, the $t_{LIM}$ used for the associated channel is always the nominal value (about 60 ms).<br>This timer is active and increments to the settings defined below after expiration of the TSTART time window and when the channel is limiting its output current to $I_{LIM}$. If the ILIM counter is allowed to reach the programmed time-out duration specified below, the channel will be powered off. The 1-second cool down timer is then started, and the channel can not be turned-on until the counter has reached completion.<br>In other circumstances (ILIM time-out has not been reached), while the channel current is below $I_{LIM}$, the same counter decrements at a rate 1/16th of the increment rate. The counter does not decrement below zero. The ILIM counter is also cleared in the event of a turn off due to a Power Enable or Reset command, a DC disconnect event or the OSS input.<br>Note that in the event the TLIM setting is changed while this timer is already active for a channel, this timer is automatically reset then restarted with the new programmed time-out duration.<br>Note that at the end of cool down cycle, when in semiauto mode, a detection cycle is automatically restarted if the detect enable bit is set. Also note that the cool down time count is immediately canceled with a reset command, or if the OFF or Manual mode is selected.<br>If 2xFBn bit is asserted in register 0x40, then $t_{LIM}$ for associated channel is programmable with the following selection:
<table>
<tr><th colspan="2">TLIM</th><th>Minimum $t_{LIM}$ (ms)</th></tr>
<tr><td>0</td><td>0</td><td>58</td></tr>
<tr><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>1</td><td>6</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>TSTART (or TINRUSH)</td><td>R/W</td><td>0</td><td>START fault timing, which is the maximum allowed overcurrent time during inrush. If at the end of TSTART period the current is still limited to $I_{Inrush}$, the channel is powered off.<br>This is followed by a 1-second cool down period, during which the channel can not be turned-on<br>Note that at the end of cool down cycle, when in semiauto mode, a detection cycle is automatically restarted if the class and detect enable bits are set.<br>Note that in the event the TSTART setting is changed while this timer is already active for a channel, this new setting is ignored and will be applied only next time the channel is turned ON.<br>The selection is as following:
<table>
<tr><th colspan="2">TSTART</th><th>Nominal $t_{START}$ (ms)</th></tr>
<tr><td>0</td><td>0</td><td>60</td></tr>
<tr><td>0</td><td>1</td><td>30</td></tr>
<tr><td>1</td><td>0</td><td>120</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
</table>

### Table 9-22. TIMING CONFIGURATION Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3–2 | TOVLD | R/W | 0 | PCUT fault timing, which is the overcurrent time duration before turn off. This timer is active and increments to the settings defined below after expiration of the TSTART time window and when the current meets or exceeds $P_{CUT}$, or when it is limited by the current foldback. If the PCUT counter is allowed to reach the programmed time-out duration specified below, the channel will be powered off. The 1-second cool down timer is then started, and the channel can not be turned-on until the counter has reached completion.<br>In other circumstances (PCUT time-out has not been reached), while the current is below $P_{CUT}$, the same counter decrements at a rate 1/16th of the increment rate. The counter does not decrement below zero. The PCUT counter is also cleared in the event of a turn off due to a Power Enable or Reset command, a DC disconnect event or the OSS input<br>Note that in the event the TOVLD setting is changed while this timer is already active for a channel, this timer is automatically reset then restarted with the new programmed time-out duration.<br>Note that at the end of cool down cycle, when in semiauto mode, a detection cycle is automatically restarted if the detect enable bit is set. Also note that the cool down time count is immediately canceled with a reset command, or if the OFF or Manual mode is selected.<br>Note that if a DCUTn bit is high in the Power Priority/PCUT Disable register, the PCUT fault timing for the associated channel is still active. However, even though the channel will not be turned off when the tOVLD time expires, the PCUT fault bits will still be set.<br>The selection is as following: |
| 1–0 | TMPDO | R/W | 0 | Disconnect delay, which is the time to turn off a channel once there is a disconnect condition, and if the dc disconnect detect method has been enabled.<br>The TDIS counter is reset each time the current goes continuously higher than the disconnect threshold for nominally 15 ms.<br>The counter does not decrement below zero.<br>The selection is as following: |

| TOVLD | | Nominal $t_{OVLD}$ (ms) |
|---|---|---|
| 0 | 0 | 60 |
| 0 | 1 | 30 |
| 1 | 0 | 120 |
| 1 | 1 | 240 |

| TMPDO | | Nominal $t_{MPDO}$ (ms) |
|---|---|---|
| 0 | 0 | 360 |
| 0 | 1 | 90 |
| 1 | 0 | 180 |
| 1 | 1 | 180 |

**Note**

The PGn and PEn bits (Power Status register) are cleared when there is a TLIM, TOVLD, TMPDO, or TSTART fault condition.

**Note**

The settings for $t_{LIM}$ set the minimum timeout based on the IEEE compliance requirements.

#### *9.6.2.19 GENERAL MASK Register*

COMMAND = 17h with 1 Data Byte, Read/Write

**Figure 9-24. GENERAL MASK Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INTEN | – | nbitACC | MbitPrty | CLCHE | DECHE | – | – |
| R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-23. GENERAL MASK Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | INTEN | R/W | 1 | $\overline{\text{INT}}$ pin mask bit. Writing a 0 will mask any bit of Interrupt register from activating the $\overline{\text{INT}}$ output, whatever the state of the Interrupt Mask register. Note that activating INTEN has no impact on the event registers.<br>1 = Any unmasked bit of Interrupt register can activate the $\overline{\text{INT}}$ output<br>0 = $\overline{\text{INT}}$ output cannot be activated |
| 6 | – | R/W | 0 | |
| 5 | nbitACC | R/W | 0 | I$^2$C Register Access Configuration bit.<br>1 = Configuration B. This means 16-bit access with a single device address (A0 = 0).<br>0 = Configuration A. This means 8-bit access, while the 8-channel device is treated as 2 separate 4-channel devices with 2 consecutive slave addresses.<br>See register 0x11 for more information on the I2C address programming |
| 4 | MbitPrty | R/W | 0 | Multi Bit Priority bit. Used to select between 1-bit shutdown priority and 3-bit shutdown priority.<br>1 = 3-bit shutdown priority. Register 0x27 and 0x28 need to be followed for priority and OSS action.<br>0 = 1-bit shutdown priority. Register 0x15 needs to be followed for priority and OSS action |
| 3 | CLCHE | R/W | 0 | Class change Enable bit. When set, the CLSCn bits in Detection Event register only indicates when the result of the most current classification operation differs from the result of the previous one.<br>1 = CLSCn bit is set only when a change of class occurred for the associated channel.<br>0 = CLSCn bit is set each time a classification cycle occurred for the associated channel. |
| 2 | DECHE | R/W | 0 | Detect Change Enable bit. When set, the DETCn bits in Detection Event register only indicates when the result of the most current detection operation differs from the result of the previous one.<br>1 = DETCn bit is set only when a change in detection occurred for the associated channel.<br>0 = DETCn bit is set each time a detection cycle occurred for the associated channel. |
| 1 | – | R/W | 0 | |
| 0 | – | R/W | 0 | |

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**Note**

If the MbitPrty bit needs to be changed from 0 to 1, make sure the OSS input pin is in the idle (low) state for a minimum of 200 µsec prior to setting the MbitPrty bit, to avoid any misbehavior related to loss of synchronization with the OSS bit stream.

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### Note

Only the nbitACC bit for channels 1-4 needs to be set to enable 16-bit I$^2$C operation.

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### Table 9-24. nbitACC = 1: Register Operations in 8-Bit (Config A) and 16-bit (Config B) I$^2$C Mode

| Cmd Code | Register or Command Name | Bits Description | Configuration A (8-bit) | Configuration B (16-bit) |
|---|---|---|---|---|
| 00h | INTERRUPT | INT bits P1-4, P5-8 | Separate mask and interrupt result per group of 4 channels.<br>The Supply event bit is repeated twice. | |
| 01h | INTERRUPT MASK | MSK bits P1-4, P5-8 | | |
| 02h | POWER EVENT | PGC_PEC P4-1, P8-5 | Separate event byte per group of 4 channels. | |
| 03h | | | | |
| 04h | DETECTION EVENT | CLS_DET P4-1, P8-5 | | |
| 05h | | | | |
| 06h | FAULT EVENT | DIS_PCUT P4-1, P8-5 | | |
| 07h | | | | |
| 08h | START/ILIM EVENT | ILIM_STR P4-1, P8-5 | | |
| 09h | | | | |
| 0Ah | SUPPLY/FAULT EVENT | TSD, VDUV, VDUW, VPUV , RAMFLT OSSE4-1, OSSE8-5 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the **same** results for TSD, VDUV, VPUV and RAMFLT. The PCUTxx and OSSEx bits will. have separate status per group of 4 channels.<br>Clearing at least one VPUV/VDUV also clears the other one. | |
| 0Bh | | | | |
| 0Ch | CHANNEL 1 DISCOVERY | CLS&DET1_CLS&DET5 | Separate Status byte per channel | |
| 0Dh | CHANNEL 2 DISCOVERY | CLS&DET2_CLS&DET6 | | |
| 0Eh | CHANNEL 3 DISCOVERY | CLS&DET3_CLS&DET7 | | |
| 0Fh | CHANNEL 4 DISCOVERY | CLS&DET4_CLS&DET8 | | |
| 10h | POWER STATUS | PG_PE P4-1, P8-5 | Separate status byte per group of 4 channels | |
| 11h | PIN STATUS | A4-A1,A0 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the **same** result, except that A0 = 0 (channel 1 to 4) or 1 (channel 5 to 8). | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the **same** result, including A0 = 0. |
| 12h | OPERATING MODE | MODE P4-1, P8-5 | Separate Mode byte per group of 4 channels. | |
| 13h | DISCONNECT ENABLE | DCDE P4-1, P8-5 | Separate DC disconnect enable byte per group of 4 channels. | |
| 14h | DETECT/CLASS ENABLE | CLE_DETE P4-1, P8-5 | Separate Detect/Class Enable byte per group of 4 channels. | |
| 15h | PWRPR/2P-PCUT DISABLE | OSS_DCUT P4-1, P8-5 | Separate OSS/DCUT byte per group of 4 channels. | |
| 16h | TIMING CONFIG | TLIM_TSTRT_TOVLD_TMPDO P4-1,<br>P8-5 | Separate Timing byte per group of 4 channels. | |
| 17h | GENERAL MASK | P4-1, P8-5 including n-bit access | Separate byte per group of 4 channels.<br>n-bit access: Setting this in at least one of the virtual quad register space is enough to enter Config B mode. To go back to config A, clear both.<br>MbitPrty: Setting this in at least one of the virtual quad register space is enough to enter 3-bit shutdown priority. To go back to 1-bit shutdown, clear both MbitPrty bits. | |
| 18h | DETECT/CLASS Restart | RCL_RDET P4-1, P8-5 | Separate DET/CL RST byte per group of 4 channels | |
| 19h | POWER ENABLE | POF_PWON P4-1, P8-5 | Separate POF/PWON byte per group of 4 channels | |
| 1Ah | RESET | P4-1, P8-5 | Separate byte per group of 4 channels, Clear Int pin and Clear All int. | Separate byte per group of 4 channels. |
| 1Bh | ID | | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the **same** result unless modified through I$^2$C. | |
| 1Ch | AUTOCLASS | AC4-1, AC8-5 | Separate byte per group of 4 channels. | |
| 1Eh | 2P POLICE 1/5 CONFIG | POL1, POL5 | Separate Policing byte per channel. | |
| 1Fh | 2P POLICE 2/6 CONFIG | POL2, POL6 | | |
| 20h | 2P POLICE 3/7 CONFIG | POL3, POL7 | | |
| 21h | 2P POLICE 4/8 CONFIG | POL4, POL8 | | |

## Table 9-24. nbitACC = 1: Register Operations in 8-Bit (Config A) and 16-bit (Config B) $I^2C$ Mode (continued)

| Cmd Code | Register or Command Name | Bits Description | Configuration A (8-bit) | Configuration B (16-bit) |
|---|---|---|---|---|
| 22h | CAP MEASUREMENT | CDET4-1, CDET8-5 | Separate capacitance measurement enable bytes per group of 4 channels. | |
| 24h | Power-on FAULT | PF P4-1, P8-5 | Separate Power-on FAULT byte per group of 4 channels | |
| 25h | | | | |
| 26h | PORT REMAPPING | Logical P4-1, P8-5 | Separate Remapping byte per group of 4 channels.<br>Reinitialized only if POR or RESET pin. Kept unchanged if 0x1A IC reset or CPU watchdog reset. | |
| 27h | Multi-Bit Priority 21 / 65 | MBP2-1, MBP6-5 | Separate MBP byte per group of 2 channels | |
| 28h | Multi-Bit Priority 43 / 87 | MBP4-3, MBP8-7 | Separate MBP byte per group of 2 channels | |
| 29h | PORT POWER ALLOCATION | MC34-12, MC78-56 | Separate MCnn byte per group of 4 channels | |
| 2Ch | TEMPERATURE | TEMP P1-4, P5-8 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) must show the **same** result. | |
| 2Eh | INPUT VOLTAGE | VPWR P1-4, P5-8 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) must show the **same** result. | |
| 2Fh | | | | |
| 30h | CHANNEL 1 CURRENT | I1, I5 | Separate 2-byte per group of 4 channels | Separate 2-byte per group of 4 channels.<br>2-byte Read at 0x30 gives I1<br>4-byte Read at 0x30 gives I1, I5. |
| 31h | | | N/A | 2-byte Read at 0x31 gives I5. |
| 32h | CHANNEL 1 VOLTAGE | V1, V5 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x32 gives V1<br>4-byte Read at 0x32 gives V1, V5. |
| 33h | | | N/A | 2-byte Read at 0x33 gives V5. |
| 34h | CHANNEL 2 CURRENT | I2, I6 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x34 gives I2<br>4-byte Read at 0x34 gives I2, I6. |
| 35h | | | N/A | 2-byte Read at 0x35 gives I6. |
| 36h | CHANNEL 2 VOLTAGE | V2, V6 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x36 gives V2<br>4-byte Read at 0x36 gives V2, V6. |
| 37h | | | N/A | 2-byte Read at 0x37 gives V6. |
| 38h | CHANNEL 3 CURRENT | I3, I7 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x38 gives I3<br>4-byte Read at 0x38 gives I3, I7. |
| 39h | | | N/A | 2-byte Read at 0x39 gives I7. |
| 3Ah | CHANNEL 3 VOLTAGE | V3, V7 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x3A gives V3<br>4-byte Read at 0x3A gives V3, V7. |
| 3Bh | | | N/A | 2-byte Read at 0x3B gives V7. |
| 3Ch | CHANNEL 4 CURRENT | I4, I8 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x3C gives I4<br>4-byte Read at 0x3C gives I4, I8. |
| 3Dh | | | N/A | 2-byte Read at 0x3D gives I8. |
| 3Eh | CHANNEL 4 VOLTAGE | V4, V8 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x3E gives V4<br>4-byte Read at 0x3E gives V4, V8. |
| 3Fh | | | N/A | 2-byte Read at 0x3F gives V8. |
| 40h | OPERATIONAL FOLDBACK | 2xFB4-1, 2xFB8-5 | Separate 2xFBn config byte per group of 4 channels. | |
| 41h | FIRMWARE REVISION | FRV P1-4, P5-8 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) must show the **same** result. | |
| 42h | I2C WATCHDOG | P1-4, P5-8 | IWD3-0: if at least one of the two 4-port settings is different than 1011b, the watchdog is enabled for all 8 channels.<br>WDS: Both 8-bit registers (channel 1 to 4 and channel 5 to 8) must show the **same** WDS result. Each WDS bit needs to be cleared individually through $I^2C$. | |
| 43h | DEVICE ID | DID_SR P1-4, P5-8 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the **same** result . | |
| 44h | CHANNEL 1 RESISTANCE | RDET1, RDET5 | Separate byte per channel.<br>Detection resistance always updated, detection good or bad. | |
| 45h | CHANNEL 2 RESISTANCE | RDET2, RDET6 | | |
| 46h | CHANNEL 3 RESISTANCE | RDET3, RDET7 | | |
| 47h | CHANNEL 4 RESISTANCE | RDET4, RDET8 | | |

### Table 9-24. nbitACC = 1: Register Operations in 8-Bit (Config A) and 16-bit (Config B) I²C Mode (continued)

| Cmd Code | Register or Command Name | Bits Description | Configuration A (8-bit) | Configuration B (16-bit) |
|---|---|---|---|---|
| 4Ch | CHANNEL 1 ASSIGNED CLASS | ACLS&PCLS1_ACLS&PCLS5 | Separate Status byte per channel | |
| 4Dh | CHANNEL 2 ASSIGNED CLASS | ACLS&PCLS2_ACLS&PCLS6 | | |
| 4Eh | CHANNEL 3 ASSIGNED CLASS | ACLS&PCLS3_ACLS&PCLS7 | | |
| 4Fh | CHANNEL 4 ASSIGNED CLASS | ACLS&PCLS4_ACLS&PCLS8 | | |
| 50h | AUTOCLASS CONTROL | MAC4-1, AAC4-1, MAC8-5, AAC8-5 | Separate Auto Class control bytes per 4 channels | |
| 51h | AUTOCLASS POWER 1/5 | PAC1, PAC5 | Separate Auto Class Power Measurement byte per channel | |
| 52h | AUTOCLASS POWER 2/6 | PAC2, PAC6 | | |
| 53h | AUTOCLASS POWER 3/7 | PAC3, PAC7 | | |
| 54h | AUTOCLASS POWER 4/8 | PAC4, PAC8 | | |
| 55h | ALTERNATIVE FOLDBACK | ALTFB4-1, ALTIR4-1, ALTFN8-5, ALTIR8-5 | Separate Alternative Foldback byte per group of 4 channels | |
| 60h | SRAM CONTROL | SRAM CNTRL BITS | These bits must be configured for the lower virtual quad (A0=0, CH 1-4)). These bits have no functionality for the upper virtual quad (A0=1, Ch 5-8) device | |
| 61h | SRAM DATA | | Streaming data input is independent of I²C configuration | |
| 62h | START ADDRESS (LSB) | | These bits must be configured for the lower virtual quad (A0=0, CH 1-4)). These bits have no functionality for the upper virtual quad (A0=1, Ch 5-8) device | |
| 63h | START ADDRESS (MSB) | | These bits must be configured for the lower virtual quad (A0=0, CH 1-4)). These bits have no functionality for the upper virtual quad (A0=1, Ch 5-8) device | |

#### *9.6.2.20 DETECT/CLASS RESTART Register*

COMMAND = 18h with 1 Data Byte, Write Only

Push button register.

Each bit corresponds to a particular cycle (detect or class restart) per channel. Each cycle can be individually triggered by writing a 1 at that bit location, while writing a 0 does not change anything for that event.

In Diagnostic/Manual mode, a single cycle (detect or class restart) will be triggered when these bits are set while in Semi Auto mode, it sets the corresponding bit in the Detect/Class Enable register 0x14.

A Read operation will return 00h.

During $t_{OVLD}$, $t_{LIM}$ or $t_{START}$ cool down cycle, any Detect/Class Restart command for that channel will be accepted but the corresponding action will be delayed until end of cool-down period.

**Figure 9-25. DETECT/CLASS RESTART Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RCL4 | RCL3 | RCL2 | RCL1 | RDET4 | RDET3 | RDET2 | RDET1 |
| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 9-25. DETECT/CLASS RESTART Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | RCL4–RCL1 | W | 0 | Restart classification bit |
| 3–0 | RDET4–RDET1 | W | 0 | Restart detection bits |

These bits may be used in place of completing a "Read-Modify-Write" sequence in register 0x14 to enable detection and classification on a per channel basis.

#### *9.6.2.21 POWER ENABLE Register*

COMMAND = 19h with 1 Data Byte, Write Only

Push button register.

Used to initiate a channel(s) turn on or turn off in any mode except OFF mode.

**Figure 9-26. POWER ENABLE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| POFF4 | POFF3 | POFF2 | POFF1 | PWON4 | PWON3 | PWON2 | PWON1 |
| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 9-26. POWER ENABLE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | POFF4–POFF1 | W | 0 | Channel power off bits |
| 3–0 | PWON4–PWON1 | W | 0 | Channel power on bits |

**Note**

Writing a “1” at POFFn and PWONn on same Channel during the same write operation turns the Channel off.

**Note**

The $t_{OVLD}$, $t_{LIM}$, $t_{START}$ and disconnect events have priority over the PWON command. During $t_{OVLD}$, $t_{LIM}$ or $t_{START}$, cool down cycle, any channel turn on using Power Enable command will be ignored and the Channel will be kept off.

**PWONn in Diagnostic/Manual Mode:**

If the PSE controller is configured in Diagnostic mode, writing a “1” at that PWONn bit location will immediately turn on the associated Channel.

**PWONn in Semi Auto Mode:**

While in Semi Auto mode, writing a “1” at a PWONn bit will attempt to turn on the associated Channel. If the detection or class results are invalid, the Channel is not turned on, and there will be no additional attempts to turn on the Channel until this push button is reasserted and the channel will resume its configured semi auto mode operation.

**Note**

In Semi Auto mode, the Power Allocation (0x29h) value needs to be set prior to issuing a PWON command. Any changes to the Power Allocation value after a PWON command is given may be ignored.

**Table 9-27. Channel Response to PWONn Command in Semi Auto Mode**

| CLEn | DETEn | Channel Operation | Result of PWONn Command |
|---|---|---|---|
| 0 | 0 | Idle | Singular Turn On attempted with Full DET and CLS cycle |
| 0 | 1 | Cycling Detection Measurements only | Singular Turn On attempted with Full DET and CLS cycle |
| 1 | 0 | Idle | Singular Turn On attempted with Full DET and CLS cycle |
| 1 | 1 | Cycling Detection and Classification Measurements | Singular Turn On attempted after next (or current) DET and CLS cycle |

In semi auto mode with DETE and CLE set, as long as the PWONx command is received prior to the start of classification, the Channel will be powered immediately after classification is complete provided the classification result is valid and the power allocations settings (see register 0x29h) are sufficient to enable power on.

**PWONn in Auto Mode:**

In Auto mode with DETE or CLE set to 0, a PWONx command will initiate a singular detection and classification cycle and the port/channel will be powered immediately after classification is complete provided the classification result is valid and the power allocations settings (see register 0x29h) are sufficient to enable power on.

In Auto mode with DETE and CLE = 1, there is no need for a PWON command. The port/channel will automatically attempt to turn on after each detection and classification cycle.

**Note**

In Auto mode, the Power Allocation (0x29h) value needs to be set prior to issuing a PWON command. Any changes to the Power Allocation value after a PWON command is given may be ignored.

### Table 9-28. Channel Response to PWONn Command in Auto Mode

| CLEn | DETEn | Channel Operation | Result of PWONn Command |
|---|---|---|---|
| 0 | 0 | Idle | Singular Turn On attempted with Full DET and CLS cycle |
| 0 | 1 | Cycling Detection Measurements only | Singular Turn On attempted with Full DET and CLS cycle |
| 1 | 0 | Idle | Singular Turn On attempted with Full DET and CLS cycle |
| 1 | 1 | Cycling Detection and Classification Measurements | NA - Channel will power automatically after a valid detection and classification |

**PWOFFn in any Mode:**

The channel is immediately disabled and the following registers are cleared:

**Table 9-29. Channel Turn Off with PWOFFn Command**

| Register | Bits to be Reset |
|---|---|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

**Note**

It may take upwards of 5ms after PWOFFn command for all register values to be updated.

Only the bits associated with the channel/port ("n") with PWOFFn set will be cleared. Those bits associated with channels/ports remaining in operation will not be changed.

#### 9.6.2.22 RESET Register

COMMAND = 1Ah with 1 Data Byte, Write Only

Push button register.

Writing a 1 at a bit location triggers an event while a 0 has no impact. Self-clearing bits.

**Figure 9-27. RESET Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLRAIN | CLINP | – | RESAL | RESP4 | RESP3 | RESP2 | RESP1 |
| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 9-30. RESET Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CLRAIN | W | 0 | Clear all interrupts bit. Writing a 1 to CLRAIN clears all event registers and all bits in the Interrupt register. It also releases the $\overline{\text{INT}}$ pin |
| 6 | CLINP | W | 0 | When set, it releases the $\overline{\text{INT}}$ pin without any impact on the Event registers nor on the Interrupt register. |
| 5 | – | W | 0 | |
| 4 | RESAL | W | 0 | Reset all bits when RESAL is set. Results in a state similar to a power-up reset. Note that the VDUV and VPUV bits (Supply Event register) follow the state of VDD and VPWR supply rails. |
| 3–0 | RESP4–RESP1 | W | 0 | Reset channel bits. Used to force an immediate channel(s) turn off in any mode, by writing a 1 at the corresponding RESPn bit location(s). |

Setting the RESAL bit will result in all of the I2C register being restored to the RST condition with the exception of those in the following table:

| Register | Bits | RESAL Result |
|---|---|---|
| 0x00 | All | Pre RESAL value will remain |
| 0x0A/B | TSD, VPUV, VDWRN, and VPUV | |
| 0x26 | All | |
| 0x2C and 0x2E | All | |
| 0x41 | All | |

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**Note**

Setting the RESAL bit for only one group of four channels (1-4 or 5-8) will result in only those four channels being reset.

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**Note**

After using the CLINP command, the $\overline{\text{INT}}$ pin will not be reasserted for any interrupts until all existing interrupts have been cleared.

Setting the RESPn bit will immediate turn off the associated channel and clear the registers according to the following table:

**Table 9-31. Channel Turn Off with RESPn Command**

| Register | Bits to be Reset |
|---|---|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

**Note**

Only the bits associated with the channel/port ("n") with RESPn set will be cleared. Those bits associated with channels/ports remaining in operation will not be changed.

it may take upwards of 5 ms before all of the registers are cleared following a RESPn command.

The RESPn command will cancel any ongoing cool down cycles .

Users need to wait at least 3ms before trying to reenable discovery or power on ports following a RESPn command.

#### *9.6.2.23 ID Register*

COMMAND = 1Bh with 1 Data Byte, Read/Write

**Figure 9-28. ID Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MFR ID | | | | | ICV | | |
| R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-32. ID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–3 | MFR ID | R/W | 01010b | Manufacture Identification number (0101,0) |
| 2–0 | ICV | R/W | 101b | IC version number (011) |

### 9.6.2.24 Connection Check and Auto Class Status Register

COMMAND = 1Ch with 1 Data Byte, Read Only

**Figure 9-29. Connection Check and Auto Class Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AC4 | AC3 | AC2 | AC1 | Rsvrd | Rsvrd | Rsvrd | Rsvrd |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-33. Connection Check and Auto Class Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | ACn | R | 0000b | Auto Class Detection Status<br>1 = PD supports Auto Class<br>0 = PD does not support Auto Class |
| 3-0 | Rsvrd | R | 00b | Reserved |

**Auto Class:**

The auto class detection measurement is completed at the end of the long classification finger, and if a PD is determined to support auto class, an auto class power measurement will be automatically completed after turn on in accordance with the IEEE auto class timing requirements.

---

**Note**

An Auto Class power measurement will be completed shortly after power on for all channels that are found to support auto class during classification.

These measurement results are available in registers (0x51h – 0x54h), and the auto class power measurements are provide per individual channel.

---

### 9.6.2.25 2-Pair Police Ch-1 Configuration Register

COMMAND = 1Eh with 1 Data Byte, Read/Write

**Figure 9-30. 2-Pair Police Ch-1 Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| POL1_7 | POL1_6 | POL1_5 | POL1_5 | POL1_3 | POL1_2 | POL1_1 | POL1_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### 9.6.2.26 2-Pair Police Ch-2 Configuration Register

COMMAND = 1Fh with 1 Data Byte, Read/Write

**Figure 9-31. 2-Pair Police Ch-2 Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| POL2_7 | POL2_6 | POL2_5 | POL2_4 | POL2_3 | POL2_2 | POL2_1 | POL2_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### 9.6.2.27 2-Pair Police Ch-3 Configuration Register

COMMAND = 20h with 1 Data Byte, Read/Write

**Figure 9-32. 2-Pair Police Ch-3 Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| POL3_7 | POL3_6 | POL3_5 | POL3_5 | POL3_3 | POL3_2 | POL3_1 | POL3_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### 9.6.2.28 2-Pair Police Ch-4 Configuration Register

COMMAND = 21h with 1 Data Byte, Read/Write

**Figure 9-33. 2-Pair Police Ch-4 Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| POL4_7 | POL4_6 | POL4_5 | POL4_4 | POL4_3 | POL4_2 | POL4_1 | POL4_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-34. 2-Pair Policing Register Fields Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–0 | POLn_7-POLn_0 | R/W | 1 | 1-byte defining 2-Pair $P_{CUT}$ **minimum** threshold.<br>The equation defining the $P_{CUT}$ is:<br>$P_{CUT} = (N \times PC_{STEP})$<br>Where, when assuming 0.200-Ω Rsense resistor is used:<br>$PC_{STEP} = 0.5$ W |

**Note**

These bits set the minimum threshold for the design. Internally, the typical PCUT threshold is set slightly above this value to ensure that the device does not trip a Pcut fault at or below the set value in this register due to part to part or temperature variation.

The contents of this register is reset to 0xFFh anytime the port is turned off or disabled either due to fault condition or user command

**Note**

Programmed values of less than 2W are not supported. If a value of less than 2W is programmed into these registers, the device will use 2W as the 2-pair Policing value.

**Power Policing:**

The TPS23882 implements a true Power Policing limit, where the device will adjust the policing limit based on both voltage and current variation in order to ensure a reliable power limit.

In Semi Auto and Auto modes, these bits are automatically set during power on based on the assigned class (see tables below). If an alternative value is desired, it needs to be set after the PEn bit is set in 0x10h, or it may also be configured prior to port turn on in combination with the use of the MPOLn bits in register 0x40 (see *Section 9.6.2.45*).

**Table 9-35. 2-Pair Policing Settings based on the Assigned Class**

| Assigned Class | POLn7-0 Settings | Minimum Power |
|---|---|---|
| Class 1 | 0000 1000 | 4W |
| Class 2 | 0000 1110 | 7W |
| Class 3 | 0001 1111 | 15.5W |
| Class 4 | 0011 1100 | 30W |

### 9.6.2.29 Capacitance (Legacy PD) Detection

COMMAND = 22h with 1 Data Byte, Write Only

Used to do enable capacitance measurement from Maunal mode

**Figure 9-34. Capacitance Detection Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | CDET4 | - | CDET3 | - | CDET2 | - | CDET1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 9-36. Capacitance Detection Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7, 5, 3, 1 | Reserved | R/W | 0 | |
| 6, 4, 2, 0 | CDETn | R/W | 0 | Enables Capacitance defection for channel "n"<br>0 = Capacitance defection disabled<br>1 = Capacitance detection enabled |

To complete a capacitance measurement on a channel, the channel must first be placed into diagnostic mode. Set the bits in register 0x22h to enable capacitance detection on the channel(s) desired. Then set the DETE bits in register 0x14h to begin the detection and process.

---

**Note**

The TPS23882 SRAM needs to be programmed in order for the capacitance measurement to operate properly.

The capacitance measurement is only supported in Manual/Diagnostic mode.

No capacitance measurement will be made if the result of the resistance detection is returned as "valid".

---

Upon completion of the capacitance measurement the DETCn bit will bet in register 0x04h, and the resistance and capacitance values will be updated in registers 0x44h - 0x4Bh.

### 9.6.2.30 Power-on Fault Register

COMMAND = 24h with 1 Data Byte, Read Only

COMMAND = 25h with 1 Data Byte, Clear on Read

**Figure 9-35. Power-on Fault Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PF4 | | PF3 | | PF2 | | PF1 | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; CR = Clear on Read; -n = value after reset

**Table 9-37. Power-on Fault Register Field Descriptions**

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7–0</td><td>PF4–PF1</td><td>R or CR</td><td>0</td><td>Represents the fault status of the classification and detection for channel n, following a failed turn on attempt with the PWONn command. These bits are cleared when channel n is turned off.<br>PFn: the selection is as follows:
<table>
<tr><th colspan="2">Fault Code</th><th>Power-on Fault Description</th></tr>
<tr><td>0</td><td>0</td><td>No fault</td></tr>
<tr><td>0</td><td>1</td><td>Invalid detection</td></tr>
<tr><td>1</td><td>0</td><td>Classification Error</td></tr>
<tr><td>1</td><td>1</td><td>Insufficient Power</td></tr>
</table>
</td></tr>
</table>

**Note**

When a Start Fault occurs and the PECn bit is not set, then this register will indicate the cause of the fault.

An insufficient power fault is reported anytime the reg 0x29 configuration will not allow a channel to be powered. See the section describing *Section 9.1.5*.

### *9.6.2.31 PORT RE-MAPPING Register*

COMMAND = 26h with 1 Data Byte, Read/Write

**Figure 9-36. PORT RE-MAPPING Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Physical Channel # of Logical Channel 4 | | Physical Channel # of Logical Channel 3 | | Physical Channel # of Logical Channel 2 | | Physical Channel # of Logical Channel 1 | |
| R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; CR = Clear on Read; -n = value after reset

**Table 9-38. PORT RE-MAPPING Register Field Descriptions**

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>POR / RST</th><th>Description</th></tr>
<tr><td>7–0</td><td>Physical Channel # of Logical Channel n</td><td>R/W</td><td>1110 0100b / P</td><td>
Used to re-map channels logically due to physical board constraints. Re-mapping is between any channel within 4-channel group (1-4 or 5-8). All channels of a group of four must be in OFF mode prior to receiving the port re-mapping command, otherwise the command will be ignored. By default there is no re-mapping.<br>
Each pair of bits corresponds to the logical port assigned.<br>
The selection per port is as follows:
<table>
<tr><th colspan="2">Re-Map Code</th><th>Physical Channel</th><th>Package Pins</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Drain1,Gat1,Sen1</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>Drain2,Gat2,Sen2</td></tr>
<tr><td>1</td><td>0</td><td>3</td><td>Drain3,Gat3,Sen3</td></tr>
<tr><td>1</td><td>1</td><td>4</td><td>Drain4,Gat4,Sen4</td></tr>
</table>
When there is no re-mapping the default value of this register is 1110,0100. The 2 MSbits with a value 11 indicate that logical channel 4 is mapped onto physical channel #4, the next 2 bits, 10, suggest logical channel 3 is mapped onto physical channel #3 and so on.<br>
Note: Code duplication is not allowed – that is, the same code cannot be written into the remapping bits of more than one port – if such a value is received, it will be ignored and the chip will stay with existing configuration.<br>
Note: Port remapping configuration is kept unchanged if 0x1A IC reset command is received.
</td></tr>
</table>

---

**Note**

The RST condition of "P" indicates that the previous state of these bits will be preserved following a device reset using the $\overline{\text{RESET}}$ pin. Thus, pulling the $\overline{\text{RESET}}$ input low will not overwrite any user changes to this register.

---

**Note**

After port remapping, TI recommends to do at least one detection-classification cycle before turn on.

### *9.6.2.32 Channels 1 and 2 Multi Bit Priority Register*

COMMAND = 27h with 1 Data Byte, Read/Write .

**Figure 9-37. Channels 1 and 2 MBP Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | MBP2_2 | MBP2_1 | MBP2_0 | – | MBP1_2 | MBP1_1 | MBP1_0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W–0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### *9.6.2.33 Channels 3 and 4 Multi Bit Priority Register*

COMMAND = 28h with 1 Data Byte, Read/Write

**Figure 9-38. Channels 3 and 4 MBP Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | MBP4_2 | MBP4_1 | MBP4_0 | – | MBP3_2 | MBP3_1 | MBP3_0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W–0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-39. Channels n MBP Register Field Descriptions**

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7–0</td><td>MBPn_2-0</td><td>R/W</td><td>0</td><td>MBPn_2-0: Multi Bit Priority bits, three bits per channel, if 3-bit shutdown priority has been selected (MbitPrty in General Mask register is high). It is used to determine which channel(s) is (are) shut down in response to a serial shutdown code received at the OSS shutdown input.<br>The turn off procedure (including register bits clearing) is similar to a channel reset using Reset command (1Ah register), except that it does not cancel any ongoing fault cool down time count.<br>The priority is defined as followings:<br>OSS code ≤ MBPn_2-0 : when the OSS code is received, the corresponding channel is powered off.<br>OSS code > MBPn_2-0 : OSS code has no impact on the channel
<table>
<tr><th colspan="3">MBPn_2-0 0x27/28 Register</th><th>Multi Bit Priority</th><th>OSS Code for Channel Off</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Highest</td><td>OSS = ‘000’</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td><td>OSS = ‘000’ or ‘001’</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3</td><td>OSS ≤ ‘010’</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4</td><td>OSS ≤ ‘011’</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td><td>OSS ≤ ‘100’</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>6</td><td>OSS = any code except ‘111’</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Lowest</td><td>OSS = any code</td></tr>
</table>
</td></tr>
</table>

The priority reduces as the 3-bit value increases. Thus, a channel with a "000" setting has the highest priority, while one with a "111" setting has the lowest.

It is permissible to apply the same settings to multiple channels. Doing so will result in all channels with the same setting will be disabled when the appropriate OSS code is presented.

The turn off procedure due to OSS is similar to a channel reset or change to OFF mode, with the exception that OSS does not cancel any ongoing fault cool down timers. the table below includes the bits that will be cleared when a channel is disabled due to OSS:

### Table 9-40. Channel Turn Off with MBP OSS

| Register | Bits to be Reset |
|---|---|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

---

**Note**

There is no memory of any preceding 3-bit OSS commands. Each 3-bit OSS command is processed immediately (prior to the end of the last OSS MBP pulse) based on the MBPn settings for each Channel. Any attempt to shutdown additional Channels thereafter will require additional 3-bit OSS commands.

---

### *9.6.2.34 Port Power Allocation Register*

COMMAND = 29h with 1 Data Byte, Read/Write

**Figure 9-39. Power Allocation Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Rsvrd | MC34_2 | MC34_1 | MC34_0 | Rsvrd | MC12_2 | MC12_1 | MC12_0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W–0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-41. Power Allocation Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 , 3 | Rsvrd | R/W | 0 | Reserved |
| 6 - 4 , 2 - 0 | MCnn_2-0 | R/W | 0 | MCnn_2-0: Port Power Allocation bits. These bits set the maximum power classification level that a given channel is allowed to power on<br>In Semi Auto mode these bits need to be set prior to issuing a PWONn command, while in Auto mode these bits need to be set prior to setting the DETE and CLE bits in 0x14. |

**Table 9-42. Power Allocation Settings**

| MCnn_2 | MCnn_1 | MCnn_0 | Power Allocation |
|---|---|---|---|
| 0 | 0 | 0 | 2-Pair 15.4W |
| 0 | 0 | 1 | 2-Pair 4 W |
| 0 | 1 | 0 | 2-Pair 7 W |
| 0 | 1 | 1 | 2-Pair 30W |
| 1 | x | x | Reserved |

**Note**

The Power Allocation (0x29h) value needs to be set prior to issuing a PWON command in Semi Auto or Auto modes, and prior to setting the DETE and CLE bits in Auto mode. Any changes to the Power Allocation value after a PWON command is given may be ignored.

**Note**

For 2-Pair wired ports, the MCnn_2-0 bits set the power allocation settings for both channels 1 and 2 and 3 and 4 concurrently.

It is possible to have channels 3 and 4 set to 15.4W while channels 1 and 2 are set to 30W, but it is not possible to have different power allocation settings between channels 1 and 2 or 3 and 4

**Note**

Setting register 0x29 to the 4 W Power Allocation configuration will only allow Class 1 PDs to be powered. Attempts to power any other class PDs will result in an insufficient power fault

Setting register 0x29 to the 7 W Power Allocation configuration will only allow Class 1 & 2 PDs to be powered. Attempts to power a class 3 or 4+ PDs will result in an insufficient power fault

### 9.6.2.35 TEMPERATURE Register

COMMAND = 2Ch with 1 Data Byte, Read Only

**Figure 9-40. TEMPERATURE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TEMP7 | TEMP6 | TEMP5 | TEMP4 | TEMP3 | TEMP2 | TEMP1 | TEMP0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-43. TEMPERATURE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–0 | TEMP7–TEMP0 | R | 0 | Bit Descriptions: Data conversion result. The I$^2$C data transmission is a 1-byte transfer.<br>8-bit Data conversion result of temperature, from –20°C to 125°C. The update rate is around once per second.<br>The equation defining the temperature measured is:<br>$T = -20 + N \times T_{STEP}$<br>Where $T_{STEP}$ is defined below as well as the full scale value:<br>**Mode** \| **Full Scale Value** \| **$T_{STEP}$**<br>Any \| 146.2°C \| 0.652°C |

### *9.6.2.36 INPUT VOLTAGE Register*

COMMAND = 2Eh with 2 Data Byte (LSByte first, MSByte second), Read only

**Figure 9-41. INPUT VOLTAGE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LSB:** | | | | | | | |
| VPWR7 | VPWR6 | VPWR5 | VPWR4 | VPWR3 | VPWR2 | VPWR1 | VPWR0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| **MSB:** | | | | | | | |
| – | – | VPWR13 | VPWR12 | VPWR11 | VPWR10 | VPWR9 | VPWR8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-44. INPUT VOLTAGE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 13–0 | VPWR13- VPWR0 | R | 0 | Bit Descriptions: Data conversion result. The $I^2C$ data transmission is a 2-byte transfer.<br>14-bit Data conversion result of input voltage.<br>The equation defining the voltage measured is:<br>$V = N \times V_{STEP}$<br>Where $V_{STEP}$ is defined below as well as the full scale value:<br>**Mode** / **Full Scale Value** / **$V_{STEP}$**<br>Any / 60 V / 3.662 mV<br>Note that the measurement is made between VPWR and AGND. |

### *9.6.2.37 CHANNEL 1 CURRENT Register*

COMMAND = 30h with 2 Data Byte, (LSByte First, MSByte second), Read Only

**Figure 9-42. CHANNEL 1 CURRENT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LSB:** | | | | | | | |
| I1_7 | I1_6 | I1_5 | I1_4 | I1_3 | I1_2 | I1_1 | I1_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| **MSB:** | | | | | | | |
| – | – | I1_13 | I1_12 | I1_11 | I1_10 | I1_9 | I1_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### *9.6.2.38 CHANNEL 2 CURRENT Register*

COMMAND = 34h with 2 Data Byte, (LSByte First, MSByte second), Read Only

**Figure 9-43. CHANNEL 2 CURRENT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LSB:** | | | | | | | |
| I2_7 | I2_6 | I2_5 | I2_4 | I2_3 | I2_2 | I2_1 | I2_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| **MSB:** | | | | | | | |
| – | – | I2_13 | I2_12 | I2_11 | I2_10 | I2_9 | I2_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### *9.6.2.39 CHANNEL 3 CURRENT Register*

COMMAND = 38h with 2 Data Byte, (LSByte First, MSByte second), Read Only

**Figure 9-44. CHANNEL 3 CURRENT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LSB:** | | | | | | | |
| I3_7 | I3_6 | I3_5 | I3_4 | I3_3 | I3_2 | I3_1 | I3_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| **MSB:** | | | | | | | |
| – | – | I3_13 | I3_12 | I3_11 | I3_10 | I3_9 | I3_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### *9.6.2.40 CHANNEL 4 CURRENT Register*

COMMAND = 3Ch with 2 Data Byte, (LSByte First, MSByte second), Read Only

**Figure 9-45. CHANNEL 4 CURRENT Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LSB:** | | | | | | | |
| I4_7 | I4_6 | I4_5 | I4_4 | I4_3 | I4_2 | I4_1 | I4_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| **MSB:** | | | | | | | |

**Figure 9-45. CHANNEL 4 CURRENT Register Format (continued)**

| – | – | I4_13 | I4_12 | I4_11 | I4_10 | I4_9 | I4_8 |
|---|---|---|---|---|---|---|---|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-45. CHANNEL n CURRENT Register Field Descriptions**

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>13-0</td><td>In_13- In_0</td><td>R</td><td>0</td><td>Bit Descriptions: Data conversion result. The I$^2$C data transmission is a 2-byte transfer.<br>Note that the conversion is done using a TI proprietary multi-slope integrating converter.<br>14-bit Data conversion result of current for channel n. The update rate is around once per 100 ms in powered state.<br>The equation defining the current measured is:<br>$I = N \times I_{STEP}$<br>Where $I_{STEP}$ is defined below as well as the full scale value, according to the operating mode:<br><table><tr><th>Mode</th><th>Full Scale Value</th><th>$I_{STEP}$</th></tr><tr><td>Powered and Classification</td><td>1.15 A (with0.255-Ω Rsense)</td><td>70.19 µA</td></tr></table>Note: in any of the following cases, the result through I$^2$C interface is automatically 0000<br>channel is in OFF mode<br>channel is OFF while in semiauto mode and detect/class is not enabled<br>channel is OFF while in semiauto mode and detection result is incorrect<br>In diagnostic/manual mode, if detect/class has been enabled at least once, the register retains the result of the last measurement</td></tr>
</table>

---

**Note**

1.46A is the theoretical full scale range of the ADC based on 14bits * Istep. However, due to the 1.25A channel current limit, the channel current will foldback and be disabled when the current exceeds the ILIM-2X threshold ($V_{LIM2X}$).

---

### Class Current Reading

Following the completion of any classification measurement on a channel, the measured classification current is reported in these registers until either a port current reading is completed following a port turn on or the port is disabled.

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**Note**

The scaling factor for the class current reading is decreased by a factor of 10x to 8.95uA/bit.

---

#### *9.6.2.41 CHANNEL 1 VOLTAGE Register*

COMMAND = 32h with 2 Data Byte, (LSByte First, MSByte second), Read Only

**Figure 9-46. CHANNEL 1 VOLTAGE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LSB:** | | | | | | | |
| V1_7 | V1_6 | V1_5 | V1_4 | V1_3 | V1_2 | V1_1 | V1_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| **MSB:** | | | | | | | |
| – | – | V1_13 | V1_12 | V1_11 | V1_10 | V1_9 | V1_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### *9.6.2.42 CHANNEL 2 VOLTAGE Register*

COMMAND = 36h with 2 Data Byte, (LSByte First, MSByte second), Read Only

**Figure 9-47. CHANNEL 2 VOLTAGE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LSB:** | | | | | | | |
| V2_7 | V2_6 | V2_5 | V2_4 | V2_3 | V2_2 | V2_1 | V2_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| **MSB:** | | | | | | | |
| – | – | V2_13 | V2_12 | V2_11 | V2_10 | V2_9 | V2_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### *9.6.2.43 CHANNEL 3 VOLTAGE Register*

COMMAND = 3Ah with 2 Data Byte, (LSByte First, MSByte second), Read Only

**Figure 9-48. CHANNEL 3 VOLTAGE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LSB:** | | | | | | | |
| V3_7 | V3_6 | V3_5 | V3_4 | V3_3 | V3_2 | V3_1 | V3_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| **MSB:** | | | | | | | |
| – | – | V3_13 | V3_12 | V3_11 | V3_10 | V3_9 | V3_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### *9.6.2.44 CHANNEL 4 VOLTAGE Register*

COMMAND = 3Eh with 2 Data Byte, (LSByte First, MSByte second), Read Only

**Figure 9-49. CHANNEL 4 VOLTAGE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LSB:** | | | | | | | |
| V4_7 | V4_6 | V4_5 | V4_4 | V4_3 | V4_2 | V4_1 | V4_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| **MSB:** | | | | | | | |

## Figure 9-49. CHANNEL 4 VOLTAGE Register Format (continued)

| – | – | V4_13 | V4_12 | V4_11 | V4_10 | V4_9 | V4_8 |
|---|---|---|---|---|---|---|---|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

## Table 9-46. CHANNEL n VOLTAGE Register Field Descriptions

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>13-0</td><td>Vn_13- Vn_0</td><td>R</td><td>0</td><td>Bit Descriptions: Data conversion result. The I$^2$C data transmission is a 2-byte transfer.<br>The equation defining the voltage measured is:<br>$V = N \times V_{STEP}$<br>Where $V_{STEP}$ is defined below as well as the full scale value:<br><table><tr><th>Mode</th><th>Full Scale Value</th><th>$V_{STEP}$</th></tr><tr><td>Powered</td><td>60 V</td><td>3.662 mV</td></tr></table><br>Note that a powered voltage measurement is made between VPWR and DRAINn.<br>Note: if a channel is OFF, the result through I$^2$C interface is automatically 0000.</td></tr>
</table>

#### *9.6.2.45 2x FOLDBACK SELECTION Register*

COMMAND = 40h with1 Data Byte Read/Write

**Figure 9-50. 2x FOLDBACK SELECTION Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 2xFB4 | 2xFB3 | 2xFB2 | 2xFB1 | MPOL4 | MPOL3 | MPOL2 | MPOL1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W -0 | R/W -0 | R/W -0 | R/W -0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-47. 2x FOLDBACK SELECTION Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | 2xFB4- 2xFB1 | R/W | 0 | When set, this activates the 2x Foldback mode for a channel which increases its $I_{LIM}$ and $I_{SHORT}$ levels normal settings, as shown in Figure 9-3. Note that the fault timer starts when the $I_{LIM}$ threshold is exceeded.<br>Notes:<br>1) At turn on, the inrush current profile is unaffected by these bits, as shown in Figure 9-2.<br>2) When a 2xFBn bit is deasserted, the $t_{LIM}$ setting used for the associated channel is always the nominal value (approximately 60 ms). If 2xFBn bit is asserted, then $t_{LIM}$ for associated channel is programmable as defined in the Timing Configuration register (0x16).<br>3) If the assigned class for a channel is class 4 or above, the 2xFB bit will be automatically set during turn on. |
| 3-0 | MPOL4 - MPOL1 | R/W | 0 | Manual Policing and Foldback configuration bits<br>0 = The internal device firmware automatically adjusts the Policing ($P_{CUT}$) and 2xFBn settings based on the assigned class during port turn on<br>1 = The Policing ($P_{CUT}$) and 2xFBn settings will not be changed during port turn on.<br>Note: Independent of these settings, the Policing ($P_{CUT}$) and 2xFBn settings are returned to their default values upon port turn off.<br>Note: Setting either bit for a 4P configured port disables the automatic configuration on **both** channels<br>The MPOLn bits are cleared upon port turn off. |

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**Note**

Refer to register 0x55h description for more information on additional Foldback and Inrush configuration options

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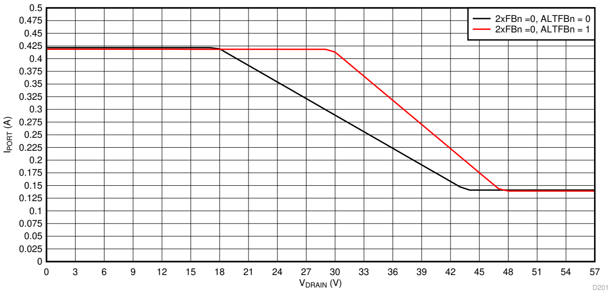

**Figure 9-51. 1x Mode (2xFBn = 0) Foldback Curves, $I_{PORT}$ vs $V_{DRAIN}$**

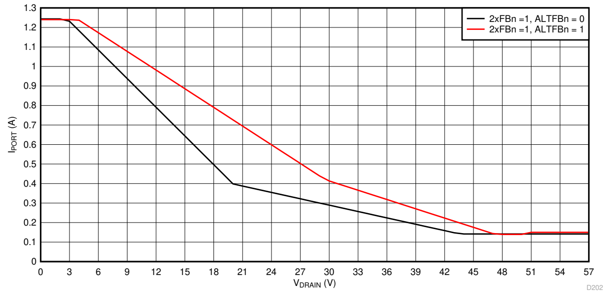

**Figure 9-52. 2x Mode (2xFBn = 1) Foldback Curves, $I_{PORT}$ vs $V_{DRAIN}$**

### *9.6.2.46 FIRMWARE REVISION Register*

COMMAND = 41h with 1 Data Byte, Read Only

**Figure 9-53. FIRMWARE REVISION Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FRV | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-48. FIRMWARE REVISION Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–0 | FRV | R | | Firmware Revision number |

After a RESET or POR fault this value will default to 0000, 0000b, but upon a “valid” SRAM load, this value will reflect the corresponding SRAM version of firmware (0x01h – 0xFEh).

**Note**

If the value of this register = 0xFFh, the device is running in “safe mode”, and the SRAM needs to be reprogrammed to resume normal operation.

#### 9.6.2.47 I2C WATCHDOG Register

COMMAND = 42h with 1 Data Byte, Read/Write

The I$^2$C watchdog timer monitors the I$^2$C clock line in order to prevent hung software situations that could leave ports in a hazardous state. The timer can be reset by either edge on SCL input. If the watchdog timer expires, all channels will be turned off and WDS bit will be set. The nominal watchdog time-out period is 2 seconds.

**Figure 9-54. I2C WATCHDOG Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | IWDD3 | IWDD2 | IWDD1 | IWDD0 | WDS |
| – | – | – | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-49. I2C WATCHDOG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4–1 | IWDD3–IWDD0 | R/W | 1011b | I$^2$C Watchdog disable. When equal to 1011b, the watchdog is masked. Otherwise, it is umasked and the watchdog is operational. |
| 0 | WDS | R/W | 0 | I$^2$C Watchdog timer status, valid even if the watchdog is masked. When set, it means that the watchdog timer has expired without any activity on I$^2$C clock line. Writing 0 at WDS location clears it.<br>Note that when the watchdog timer expires and if the watchdog is unmasked, all channels are also turned off. |

When the channels are turned OFF due to I$^2$C watchdog, the corresponding bits are also cleared:

**Table 9-50. I2C WATCHDOG Reset**

| Register | Bits to be Reset |
|---|---|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

The corresponding PGCn and PECn bits of Power Event register will also be set if there is a change. The corresponding PEn and PGn bits of Power Status Register are also updated accordingly.

**Note**

If the I$^2$C watchdog timer has expired, the Temperature and Input voltage registers will stop being updated until the WDS bit is cleared. The WDS bit must then be cleared to allow these registers to work normally.

### *9.6.2.48 DEVICE ID Register*

COMMAND = 43h with 1 Data Byte, Read Only

**Figure 9-55. DEVICE ID Register Format**

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="4">DID</td><td colspan="4">SR</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-51. DEVICE ID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–5 | DID | R | 0011b | Device ID number |
| 4–0 | SR | R | 0011b | Silicon Revision number |

#### 9.6.2.49 CHANNEL 1 DETECT RESISTANCE Register

COMMAND = 44h with 1 Data Byte, Read Only

Figure 9-56. CHANNEL 1 DETECT RESISTANCE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R1_7 | R1_6 | R1_5 | R1_4 | R1_3 | R1_2 | R1_1 | R1_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### 9.6.2.50 CHANNEL 2 DETECT RESISTANCE Register

COMMAND = 45h with 1 Data Byte, Read Only

Figure 9-57. CHANNEL 2 DETECT RESISTANCE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R2_7 | R2_6 | R2_5 | R2_4 | R2_3 | R2_2 | R2_1 | R2_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### 9.6.2.51 CHANNEL 3 DETECT RESISTANCE Register

COMMAND = 46h with 1 Data Byte, Read Only

Figure 9-58. CHANNEL 3 DETECT RESISTANCE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R3_7 | R3_6 | R3_5 | R3_4 | R3_3 | R3_2 | R3_1 | R3_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### 9.6.2.52 CHANNEL 4 DETECT RESISTANCE Register

COMMAND = 47h with 1 Data Byte, Read Only

Figure 9-59. CHANNEL 4 DETECT RESISTANCE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R4_7 | R4_6 | R4_5 | R4_4 | R4_3 | R4_2 | R4_1 | R4_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-52. DETECT RESISTANCE Register Fields Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | Rn_7- Rn_0 | R | 0 | 8-bit data conversion result of detection resistance for channel n.<br>Most recent 2-point Detection Resistance measurement result. The $I^2C$ data transmission is a 1-byte transfer.<br>Note that the register content is not cleared at turn off.<br>The equation defining the resistance measured is:<br>$R = N \times R_{STEP}$<br>Where $R_{STEP}$ is defined below as well as the full scale value:<br><table><tr><th>Useable Resistance Range</th><th>$R_{STEP}$</th></tr><tr><td>2 kΩ to 50 kΩ</td><td>195.3125 Ω</td></tr></table> |

### 9.6.2.53 CHANNEL 1 DETECT CAPACITANCE Register

COMMAND = 48h with 1 Data Byte, Read Only

**Figure 9-60. CHANNEL 1 DETECT CAPACITANCE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| C1_7 | C1_6 | C1_5 | C1_4 | C1_3 | C1_2 | C1_1 | C1_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### 9.6.2.54 CHANNEL 2 DETECT CAPACITANCE Register

COMMAND = 49h with 1 Data Byte, Read Only

**Figure 9-61. CHANNEL 2 DETECT CAPACITANCE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| C2_7 | C2_6 | C2_5 | C2_4 | C2_3 | C2_2 | C2_1 | C2_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### 9.6.2.55 CHANNEL 3 DETECT CAPACITANCE Register

COMMAND = 4Ah with 1 Data Byte, Read Only

**Figure 9-62. CHANNEL 3 DETECT CAPACITANCE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| C3_7 | C3_6 | C3_5 | C3_4 | C3_3 | C3_2 | C3_1 | C3_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### 9.6.2.56 CHANNEL 4 DETECT CAPACITANCE Register

COMMAND = 4Bh with 1 Data Byte, Read Only

**Figure 9-63. CHANNEL 4 DETECT CAPACITANCE Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| C4_7 | C4_6 | C4_5 | C4_4 | C4_3 | R4_2C | C4_1 | C4_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### Table 9-53. DETECT CAPACITANCE Register Fields Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | Cn_7- Cn_0 | R | 0 | 8-bit data conversion result of capacitance measurement for channel n.<br>Most recent capacitance measurement result. The $I^2C$ data transmission is a 1-byte transfer.<br>The equation defining the resistance measured is:<br>$C = N \times C_{STEP}$<br>Where $C_{STEP}$ is defined below as well as the full scale value:<br>**Useable Resistance Range** / **$C_{STEP}$**<br>1 µF to 12 µF / 0.05 µF<br>Note that the register content is not cleared at turn off.<br>Note: The capacitance measurement is only supported in Manual/Diagnostic mode.<br>Note: No capacitance measurement will be made if the result of the resistance detection is returned as "valid".<br>Note: The TPS23882 SRAM needs to be programmed in order for the capacitance measurement to operate properly. |

### *9.6.2.57 CHANNEL 1 ASSIGNED CLASS Register*

COMMAND = 4Ch with 1 Data Byte, Read Only

**Figure 9-64. CHANNEL 1 ASSIGNED CLASS Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ACLASS Ch1 | | | | PCLASS Ch1 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### *9.6.2.58 CHANNEL 2 ASSIGNED CLASS Register*

COMMAND = 4Dh with 1 Data Byte, Read Only

**Figure 9-65. CHANNEL 2 ASSIGNED CLASS Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ACLASS Ch2 | | | | PCLASS Ch2 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### *9.6.2.59 CHANNEL 3 ASSIGNED CLASS Register*

COMMAND = 4Eh with 1 Data Byte, Read Only

**Figure 9-66. CHANNEL 3 ASSIGNED CLASS Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ACLASS Ch3 | | | | PCLASS Ch3 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### *9.6.2.60 CHANNEL 4 ASSIGNED CLASS Register*

COMMAND = 4Fh with 1 Data Byte, Read Only

**Figure 9-67. CHANNEL 4 ASSIGNED CLASS Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ACLASS Ch4 | | | | PCLASS Ch4 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Bit Descriptions:** These bits represent the **"assigned"** and previous classification results for channel n. These bits are cleared when channel n is turned off.

### Table 9-54. CHANNEL n ASSIGNED CLASS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7–4 | ACLASS Ch-n | R | 0 | Assigned classification on channel n.<br>See Table 9-55 below |
| 3–0 | PCLASS Ch-n | R | 0 | Previous Class result on channel n.<br>See Table 9-56 below |

### Table 9-55. Assigned Class Designations

| ACLASS-Chn | | | | Assigned Class |
|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | |
| 0 | 0 | 0 | 0 | Unknown |
| 0 | 0 | 0 | 1 | Class 1 |
| 0 | 0 | 1 | 0 | Class 2 |
| 0 | 0 | 1 | 1 | Class 3 |
| 0 | 1 | 0 | 0 | Class 4 |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | Reserved |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | X | X | X | Reserved |

### Table 9-56. Previous Class Designations

| PCLASS-Chn | | | | Previous Class |
|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | |
| 0 | 0 | 0 | 0 | Unknown |
| 0 | 0 | 0 | 1 | Class 1 |
| 0 | 0 | 1 | 0 | Class 2 |
| 0 | 0 | 1 | 1 | Class 3 |
| 0 | 1 | 0 | 0 | Class 4 |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | Class 0 |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | Class 5 - 4-Pair |
| 1 | 0 | 0 | 1 | Class 6 - 4-Pair |
| 1 | 0 | 1 | 0 | Class 7 - 4-Pair |
| 1 | 0 | 1 | 1 | Class 8 - 4-Pair |
| 1 | 1 | X | X | Reserved |

**“Requested” vs. “Assigned” Classification:**

The “requested” class is the classification the PSE measures during Mutual Identification prior to turn on, whereas the “assigned” class is the classification level the Channel was powered on with based on the Power Allocation setting in register 0x29h. The “requested” classification values are available in registers 0x0C-0F

---

**Note**

Upon being powered, devices that present a class 0 signature during discovery will be given an assigned class of "Class 3"

---

**Note**

There is no Assigned Class assigned for ports/channels powered out of Manual/Diagnostic mode. Any settings such as the port power policing and 1x/2x foldback selection that are typically configure based on the assigned class result need to manually configured by the user.

---

**Previous Classification**

In certain circumstances the requested class result in 0x0C-0F can not properly reflect the actual classification of the PD connected to the port/channel. This will happen when a port has a power allocation limit of 15.4W and the PSE can only provide 1 classification finger during turn on. When this occurs and if the device is configured to run in Semi Auto mode with det and cls enabled, the 3-finger classification measurement that preceded the turn on detection and classification cycle will be stored here. This information can be useful in scenarios where a port had to be demoted to stay under the system power limit at turn on but additional power budget comes available later on.

---

**Note**

The Previous Classification results are only valid for channels being used in semi auto mode with ongoing discovery (DETE and CLE = 1).

### *9.6.2.61 AUTO CLASS CONTROL Register*

COMMAND = 50h with 1 Data Byte, Read/Write

**Figure 9-68. AUTO CLASS CONTROL Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MAC4 | MAC3 | MAC2 | MAC1 | AAC4 | AAC3 | AAC2 | AAC1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-57. AUTO CLASS CONTROL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 - 4 | MACn | R/W | 0 | Manual Auto Class Measurement bits<br>1 = Manual Auto Class Measurement enabled<br>0 = Manual Auto Class measurement complete<br>The auto class measurement will begin within 10ms of this bit being set. This bit will be cleared by the internal firmware within 1ms of the updated Autoclass measurement result(s) in 0x51-54h. |
| 3 -0 | AACn | R/W | 0 | Auto Class Auto Adjustment Enable bits<br>1 = Autoclass auto adjust is enabled and the corresponding PCUT settings will be automatically adjusted based on the measured autoclass power<br>0 = Autoclass auto adjust is disabled and it is up to the user to adjust the value of PCUT as desired. |

**Note**

Any MACn bits set prior to turn on will be ignored and cleared during turn on.

**Auto Class Pcut Adjustments:**

If the ACx bit(s) are set in register 0x50h, the TPS23882 will automatically adjust its PCUT value based on the auto class power measurement ($P_{AC}$ in registers 0x51-54) and Any Automatic Auto Class facilitated (AACn = 1) PCut adjustments will be made within 5 ms of the end of the auto class measurement period.

#### *9.6.2.62 CHANNEL 1 AUTO CLASS POWER Register*

COMMAND = 51h with 1 Data Byte, Read Only

**Figure 9-69. CHANNEL 1 AUTO CLASS POWER Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | PAC1_6 | PAC1_5 | PAC1_4 | PAC1_3 | PAC1_2 | PAC1_1 | PAC1_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### *9.6.2.63 CHANNEL 2 AUTO CLASS POWER Register*

COMMAND = 52h with 1 Data Byte, Read Only

**Figure 9-70. CHANNEL 2 AUTO CLASS POWER Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | PAC2_6 | PAC2_5 | PAC2_4 | PAC2_3 | PAC2_2 | PAC2_1 | PAC2_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### *9.6.2.64 CHANNEL 3 AUTO CLASS POWER Register*

COMMAND = 53h with 1 Data Byte, Read Only

**Figure 9-71. CHANNEL 3 AUTO CLASS POWER Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | PAC3_6 | PAC3_5 | PAC3_4 | PAC3_3 | PAC3_2 | PAC3_1 | PAC3_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### *9.6.2.65 CHANNEL 4 AUTO CLASS POWER Register*

COMMAND = 54h with 1 Data Byte, Read Only

**Figure 9-72. CHANNEL 4 AUTO CLASS POWER Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | PAC4_6 | PAC4_5 | PAC4_4 | PAC4_3 | PAC4_2 | PAC4_1 | PAC4_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-58. AUTO CLASS POWER Register Fields Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 6-0 | PACn_6-<br>PACn_0 | R | 0 | 8-bit data conversion result of the auto class power measurement for channel n.<br>Peak average power calculation result from channel voltage and current data conversion measurements taken during the auto class power measurement window.<br>The equation defining the auto class power measured is:<br>$P_{AC}= N \times P_{AC\_STEP}$<br>Where, when assuming 0.200-Ω Rsense resistor is used:<br>$PC_{STEP} = 0.5$ W |

### 9.6.2.66 ALTERNATIVE FOLDBACK Register

COMMAND = 55h with 1 Data Byte, Read/Write

**Figure 9-73. ALTERNATIVE FOLDBACK Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALTFB4 | ALTFB3 | ALTFB2 | ALTFB1 | ALTIR4 | ALTIR3 | ALTIR2 | ALTIR1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-59. ALTERNATIVE FOLDBACK Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | ALTFBn | R | 0 | Alternative Foldback Enable bits: Used to enable the operational alterative foldback curves while powered.<br>1 = Alternative Foldback is enabled<br>0 = Alternative Foldback is disabled<br>The ALTFBn bits should be set prior to issuing a PWONn command to ensure the desired foldback curve is being used. |
| 3-0 | ALTIRn | R | 0 | Alternative Inrush Enable bits: Used to enable the alterative foldback curves during inrush on channel n<br>1 = Alternative Inrush is enabled<br>0 = Alternative Inrush is disabled<br>Note: The ALTIRn bits need to be set prior to sending a PWONn command to ensure the desired inrush behavior is followed |

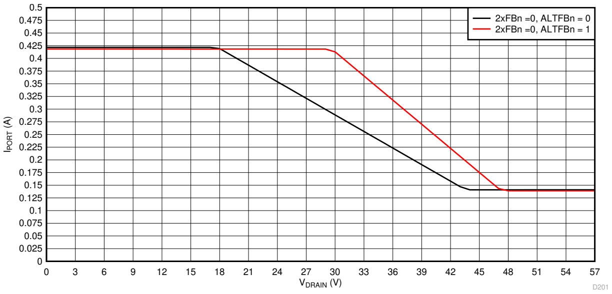

**Figure 9-74. 1x Mode (2xFBn = 0) Foldback Curves, $I_{PORT}$ vs $V_{DRAIN}$**

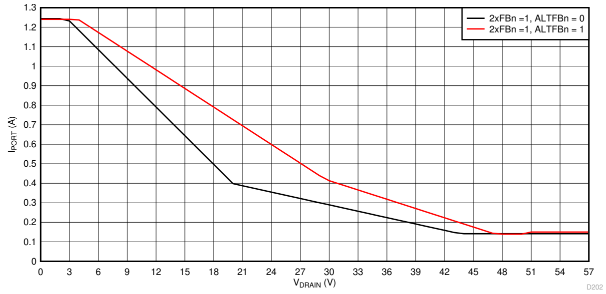

**Figure 9-75. 2x Mode (2xFBn = 1) Foldback Curves, $I_{PORT}$ vs $V_{DRAIN}$**

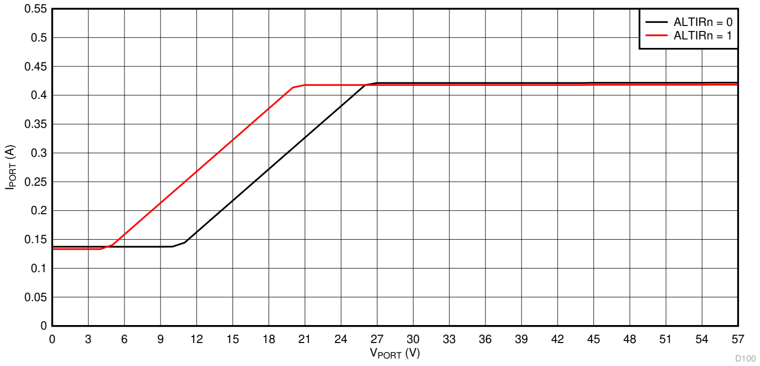

**Figure 9-76. Inrush Foldback Curves, $I_{PORT}$ vs $V_{PORT}$**

### *9.6.2.67 SRAM CONTROL Register*

COMMAND = 60h with 1 Data Byte, Read/Write

**Figure 9-77. SRAM CONTROL Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PROG_SEL | CPU_RST | - | PAR_EN | RAM_EN | PAR_SEL | R/WZ | CLR_PTR |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9-60. SRAM CONTROL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PROG_SEL | R/W | 0 | I2C Programming select bit.<br>1 = SRAM I2C read/write is enabled<br>0 = SRAM I2C read/write is disabled. |
| 6 | CPU_RST | R/W | 0 | CPU Reset bit<br>1 = Internal CPU is held in RESET<br>0 = Internal CPU is active<br>This is strictly a CPU reset. Toggling this bit reset the cpu only and will not change any contents of the $I^2C$ registers |
| 5 | Reserved | R/W | 0 | Reserved |
| 4 | PAR_EN | R/W | 0 | SRAM Parity Enable bit:<br>1 = SRAM Parity Check will be enabled<br>0 = SRAM Parity Check will be disabled<br>It is recommended that the Parity function be enable whenever SRAM is being used |
| 3 | RAM_EN | R/W | 0 | SRAM Enable bit<br>1 = SRAM will be enabled and the internal CPU will run from both SRAM and internal ROM<br>0 = Internal CPU will run from internal ROM only<br>This bit needs to be set to a 1 after SRAM programing to enable the utilization of the SRAM code |
| 2 | PAR_SEL | R/W | 0 | SRAM Parity Select bit: Setting this bit to a 1 in conjunction with the RZ/W bit enables access to the SRAM Parity bits.<br>1 = Parity bits read/write is enabled<br>0 = Parity bits read/write is disabled |
| 1 | R/WZ | R/W | 0 | SRAM Read/Write select bit:<br>0 = SRAM Write – SRAM data is written with a write to 0x61h<br>1 = SRAM Read – SRAM data is read with a read from 0x61h<br>SRAM data can be continuously read/written over I2C until a STOP bit is sent. |
| 0 | CLR_PTR | R/W | 0 | Clear Address Pointer bit:<br>1 = Resets the memory address pointer<br>0 = Releases pointer for use<br>In order to ensure proper programming, this bit should be toggled (0-1-0) to writing or reading the SRAM or Parity memory. |

#### 9.6.2.67.1 SRAM START ADDRESS (LSB) Register

COMMAND = 62h with 1 Byte, Read/Write

**Figure 9-78. SRAM START ADDRESS (LSB) Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SA_7 | SA_6 | SA_5 | SA_4 | SA_3 | SA_2 | SA_1 | SA_0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### 9.6.2.67.2 SRAM START ADDRESS (MSB) Register

COMMAND = 63h with 1 Byte, Read/Write

**Figure 9-79. SRAM START ADDRESS (MSB) Register Format**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SA_15 | SA_14 | SA_13 | SA_12 | SA_11 | SA_10 | SA_9 | SA_8 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### 9.6.2.67.3

**Table 9-61. SRAM START ADDRESS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | SA_15- SA_0 | R/W | 0 | SRAM and Parity Programing Start Address bits:<br>the value entered into these registers sets the start address location for the SRAM or Parity programming |

**SRAM Programming:**

Upon power up, it is recommended that the TPS23882 device's SRAM be programmed with the latest version of SRAM code via the I$^2$C to ensure proper operation and IEEE complaint performance. All I$^2$C traffic other than those commands required to program the SRAM should be deferred until after the SRAM programming sequences are completed.

**Note**

The latest version of firmware and SRAM release notes may be accessed from the *TI mySecure Software* webpage.

The SRAM Release Notes and ROM Advisory document includes more detailed information regarding any know issues and changes that were associated with each firmware release.

**Note**

The SRAM programming control must be completed at the lower I2C address (Channels 1-4, A0 = 0). Configuring this registers for the upper I2C device address (Channels 5-8) will not program the SRAM

For systems that include multiple TPS23882 devices, the 0x7F "global" broadcast I2C address may be used to programmed all of the devices at the same time.

**Note**

The SRAM programming needs to be delayed at least 50ms from the initial power on (VPWR and VDD above UVLO) of the device to allow for the device to complete its internal hardware initialization process

**Note**

For more detailed instructions on the SRAM programing procedures please refer the *How to Load TPS2388x SRAM Code* document on TI.com.

**0x60h setup for SRAM Programming:** Prior to programming/writing the SRAM, the following bits sequence needs to be completed in register 0x60h:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PROG_SEL | CPU_RST | - | PAR_EN | RAM_EN | PAR_SEL | R/WZ | CLR_PTR |
| 0 → 1 | 0 → 1 | 0 | 0 | 0 | 0 | 1 → 0 | 0 → 1 → 0 |

The same sequence is required to read the SRAM with the exception that the R/WZ bit needs to be set to “1”.

If the device is in “Safe Mode”, the same sequence as above may be used to reprogram the SRAM.

An I$^2$C write to 0x61h following this sequence actively programs the SRAM program memory starting from the address set in registers 0x62h and 63h.

**0x60h setup for SRAM Parity Programming:** Following the programming of the SRAM program memory, the following bits sequence needs to be completed in register 0x60h in order to configure the device to program the Parity memory:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PROG_SEL | CPU_RST | - | PAR_EN | RAM_EN | PAR_SEL | R/WZ | CLR_PTR |
| 0 → 1 | 0 → 1 | 0 | 0 | 0 | 0 → 1 | 1 → 0 | 0 → 1 → 0 |

The same sequence is required to read the Parity with the exception that the R/WZ bit needs to be set to “1".

An I$^2$C write to 0x61h following this sequence actively programs the Parity memory starting from the address set in registers 0x62h and 63h.

**0x60h setup to run from SRAM Program Memory:** Upon completion of programming, the following bits sequence needs to be completed in register 0x60h in order to enable the device to run properly out of SRAM:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PROG_SEL | CPU_RST | - | PAR_EN | RAM_EN | PAR_SEL | R/WZ | CLR_PTR |
| 1 → 0 | 1 → 0 | 0 | 0 → 1 | 0 → 1 | 1 → 0 | 0 | 0 |

Within 1ms of the completion of the above sequence, the device will complete a compatibility check on the SRAM

If the SRAM load is determined to be “Valid”: Register 0x41h will have a value between 0x01h and 0xFEh, and the device will return to normal operation.

If the SRAM load is determined to be “Invalid”:

- 0x41h will be set to 0xFFh
- The RAM_EN bit will be internally cleared
- The device will operating in “safe mode” until another programming attempt is completed

# 10 Application and Implementation

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**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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## 10.1 Application Information

The TPS23882 is an 8-channel, IEEE 802.3bt ready PoE PSE controller and can be used in high port count semiauto or fully micro-controller managed applications (The MSP430FR5969 micro-controller is recommended for most applications). Subsequent sections describe detailed design procedures for applications with different requirements including host control.

The schematic of Figure 10-1 depicts semiauto mode operation of the TPS23882, providing functionality to power PoE loads. The TPS23882 can do the following:

1. Performs load detection.
2. Performs classification including the 100ms long finger for Autoclass discovery and 80.23bt reduce $T_{MPS}$ support
3. Enables power on with protective foldback current limiting, and Port power policing ($P_{CUT}$) value.
4. Shuts down in the event of fault loads and shorts.
5. Performs Maintain Power Signature function to insure removal of power if load is disconnected.
6. Undervoltage lock out occurs if VPWR falls below $V_{PUV\_F}$ (typical 26.5 V).

Following a power-off command, disconnect or shutdown due to a Start, $P_{CUT}$ or $I_{LIM}$ fault, the port powers down. Following port power off due to a disconnect, the TPS23882 will immediate restart the detection and classification cycles if the DETE and CLE bits are set in register 0x14. If the shutdown is due to a start, $P_{CUT}$ or $I_{LIM}$ fault, the TPS23882 enters into a cool-down period during which any Detect/Class Enable Command for that port will be delayed. At the end of cool down cycle, one or more detection/class cycles are automatically restarted if the class and/or detect enable bits are set. If a port is disabled using the power off command, the DETE and CLE bits will be cleared and these bits will need to be reset over $I^2C$ in order for detection and classification to resume.

### 10.1.1 Introduction to PoE

Power-over-Ethernet (PoE) is a means of distributing power to Ethernet devices over the Ethernet cable using either data or spare pairs. PoE eliminates the need for power supplies at the Ethernet device. Common applications of PoE are security cameras, IP Phones and wireless access points (WAP). The host or mid-span equipment that supplies power is the power source equipment (PSE). The load at the Ethernet connector is the powered device (PD). PoE protocol between PSE and PD controlling power to the load is specified by IEEE 802.3bt standard. Transformers are used at Ethernet host ports, mid-spans and hubs, to interface data to the cable. A DC voltage can be applied to the center tap of the transformer with no effect on the data signals. As in any power transmission line, a relatively high voltage (approximately 50 V) is used to keep currents low and minimize the effects of IR drops in the line to preserve power delivery to the load. Standard 2-Pair PoE delivers approximately 13 W to a type 1 PD, and 25.5 W to a type 2 PD, whereas standard 4-Pair PoE will be capable of delivering approximately 51 W to a type 3 PD and 71 W to a type 4 PD.

#### *10.1.1.1 2-Pair Versus 4-Pair Power and the New IEEE802.3bt Standard*

The IEEE 802.3at-2009 standard previously expanded PoE power delivery from 15.4W (Commonly referred to as .af or Type-1 PoE) to 30 W (.at or Type-2 PoE) of sourced power from the PSE (Power Sourcing Equipment) over 2-pairs of ethernet wires (Commonly known as either the Alt-A or Alt-B pair sets). The IEEE 802.3bt standard further expands power delivery up to 90 W sourced from a PSE by allowing for power delivery over both the ALT-A and ALT-B pairsets in parallel. Two new PoE equipment "Types" have also been created as part of the new standard. Type 3 PSE equipment will be capable of sourcing up to 60 W of power over 4-pair or 30 W over 2-pair while supporting the new MPS requirements. Type 4 PSE equipment will be capable of sourcing up to 90 W of power over 4-pair. The TPS23882 has been designed to be comply with the 2-Pair Type-3 requirements.

The Maintain Power Signature (or MPS) requirements have also been updated for the new standard. The previous version of the standard only required PSEs to maintain power on a port if the PD (Powered Device) current exceeded 10 mA for at least 60 ms every 300 ms to 400 ms. By decreasing these requirements to 6 ms every 320 ms to 400 ms, the minimum power requirement to maintain PoE power have been reduced by a factor of nearly 10.

## 10.2 Typical Application

This typical application shows an eight (2-Pair) port, semiauto mode application using a MSP430 or similar micro-controller. Operation in any mode requires I²C host support. The TPS23882 provides useful telemetry in multi-port applications to aid in implementing port power management.

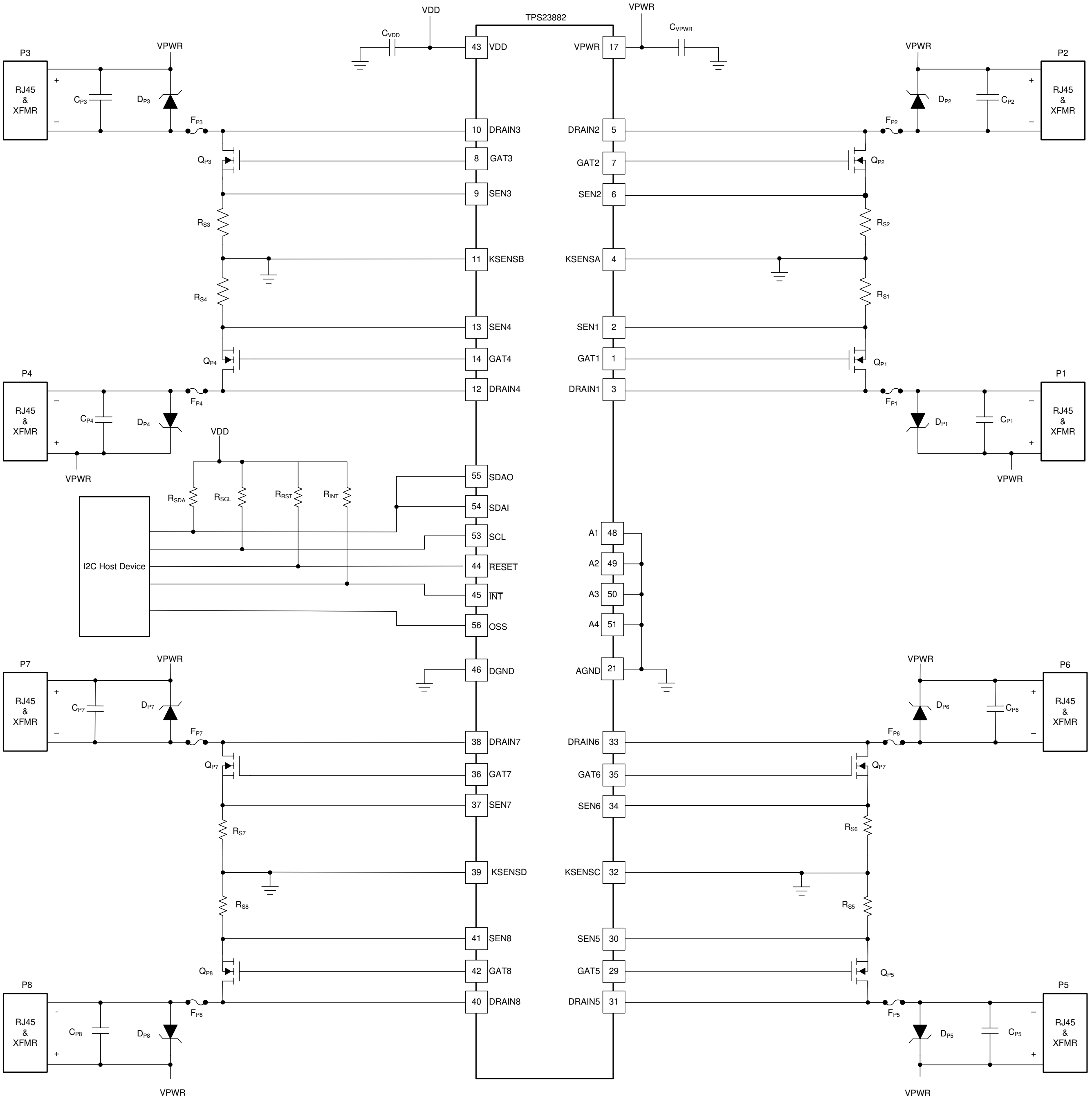

**Figure 10-1. Eight 2-Pair Port Application**

### 10.2.1 Design Requirements

TPS23882 devices are used in the eight port configuration and are managed by the $I^2C$ host device. The $I^2C$ address for TPS23882 is programmed using the A4..A1 pins. When using multiple TPS23882 devices in a system, each device requires by a unique $I^2C$ address. See *Section 9.6.2.13* for more information on how to program the TPS23882 $I^2C$ address.

A MCU is not required to operate the TPS23882 device, but some type of $I^2C$ master/host controller device is required to program the internal SRAM and initialize the basic $I^2C$ register configuration of the TPS23882.

It is recommended that the $\overline{\text{RESET}}$ pin be connected to a micro-controller or other external circuitry.

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**Note**

The $\overline{\text{RESET}}$ pin must be held low until both VPWR and VDD are above their UVLO thresholds.

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Refer to the *TPS23882EVM User's Guide* for more detailed information.

### 10.2.2 Detailed Design Procedure

Refer to the *TPS23882EVM User's Guide* for more detailed information on component selection and layout recommendations.

#### *10.2.2.1 Connections on Unused Channels*

On unused channels, it is recommended to ground the SENx pin and leave the GATx pin open. DRAINx pins can be grounded or left open (leaving open may slightly reduce power consumption). Figure 10-2 shows an example of an unused PORT2.

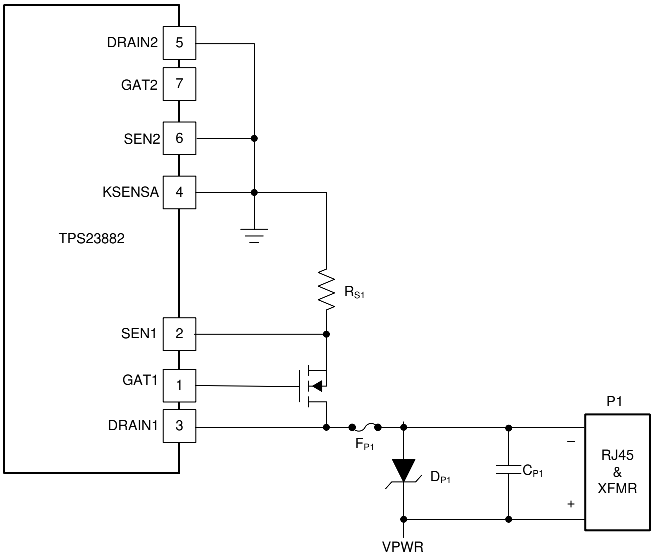

**Figure 10-2. Unused PORT2 Connections**

#### 10.2.2.2 Power Pin Bypass Capacitors

- **$C_{VPWR}$:** 0.1 µF, 100 V, X7R ceramic at pin 17 (VPWR)
- **$C_{VDD}$:** 0.1 µF, 5 V, X7R ceramic at pin 43 (VDD)

#### 10.2.2.3 Per Port Components

- **$C_{Pn}$**: 0.1-µF, 100-V, X7R ceramic between VPWR and Pn-
- **$R_{Sn}$**: Each channel's current sense resistor is a 0.2-Ω. A 1%, 0.25-W resistor in an 0805 SMT package is recommended. If a 30W Policing ($P_{CUT}$) threshold is selected, the maximum power dissipation for the resistor becomes approximately 93.3 mW.

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**Note**

> For systems requiring either more accurate system power monitoring or precise Port Power Policing accuracy, it is recommend that 0.1% $R_{SENSE}$ resistors be used.

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- **$Q_{Pn}$**: The port MOSFET can be a small, inexpensive device with average performance characteristics. $BV_{DSS}$ should be 100 V minimum. Target a MOSFET $R_{DS(on)}$ at $V_{GS}$ = 10 V of between 50 mΩ and 150 mΩ. The MOSFET GATE charge ($Q_G$) and input capacitance ($C_{ISS}$) should be less than 50 nC and 2000 pF respectively. The maximum power dissipation for $Q_{Pn}$ with RDS(on) = 100 mΩ at 640 mA nominal policing ($I_{CUT}$) threshold is approximately 45 mW.

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**Note**

> In addition to the MOSFET $R_{DS(on)}$ and $BV_{DSS}$ characteristics, the power MOSFET SOA ratings also need to be taken into consideration when selecting these components for your system design. It is recommended that a MOSFET be chosen with an SOA rating that exceeds the inrush and operational foldback characteristic curves as shown in Figure 9-2 and Figure 9-3. When using the standard current foldback (ALTIRn or ALTFBn = 0) options, the CSD19538Q3A 100V N-Channel MOSFET is recommended.

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- **$F_{Pn}$**: The port fuse should be a slow blow type rated for at least 60 VDC and above approximately 2 x $P_{CUT}$ (max). The cold resistance should be below 200 mΩ to reduce the DC losses. The power dissipation for FPn with a cold resistance of 180 mΩ at maximum $P_{CUT}$ is approximately 150 mW.
- **$D_{PnA}$**: The port TVS should be rated for the expected port surge environment. $D_{PnA}$ should have a minimum reverse standoff voltage of 58 V and a maximum clamping voltage of less than 95 V at the expected peak surge current

#### *10.2.2.4 System Level Components (not shown in the schematic diagrams)*

The system TVS and bulk VPWR capacitance work together to protect the PSE system from surge events which could cause VPWR to surge above 70 V. The TVS and bulk capacitors should be placed on the PCB such that all TPS23882 ports are adequately protected.

- **TVS:** The system TVS should be rated for the expected peak surge power of the system and have a minimum reverse standoff voltage of 58 V. Together with the VPWR bulk capacitance, the TVS must prevent the VPWR rail from exceeding 70 V.
- **Bulk Capacitor:** The system bulk capacitor(s) should be rated for 100 V and can be of aluminum electrolytic type. Two 47-µF capacitors can be used for each TPS23882 on board.
- **Distributed Capacitance:**In higher port count systems, it may be necessary to distribute 1-uF, 100-V, X7R ceramic capacitors across the 54-V power bus. One capacitor per each TPS23882 pair is recommended.
- **Digital I/O Pullup Resistors:** $\overline{\text{RESET}}$ and A1-A4 are internally pulled up to VDD, while OSS is internally pulled down, each with a 50-kΩ (typical) resistor. A stronger pull-up/down resistor can be added externally such as a 10 kΩ, 1%, 0.063 W type in a SMT package. SCL, SDAI, SDAO, and INT require external pull-up resistors within a range of 1 kΩ to 10 kΩ depending on the total number of devices on the bus .
- **Ethernet Data Transformer (per port):** The Ethernet data transformer must be rated to operate within the IEEE802.3bt standard in the presence of the DC port current conditions. The transformer is also chosen to be compatible with the Ethernet PHY. The transformer may also be integrated into the RJ45 connector and cable terminations.
- **RJ45 Connector (per port):** The majority of the RJ45 connector requirements are mechanical in nature and include tab orientation, housing type (shielded or unshielded), or highly integrated. An integrated RJ45 consists of the Ethernet data transformer and cable terminations at a minimum. The integrated type may also contain the port TVS and common mode EMI filtering.
- **Cable Terminations (per port):** The cable terminations typically consist of series resistor (usually 75 Ω) and capacitor (usually 10 nF) circuits from each data transformer center tap to a common node which is then bypassed to a chassis ground (or system earth ground) with a high-voltage capacitor (usually 1000 pF to 4700 pF at 2 kV).

### 10.2.3 Application Curves

Unless otherwise noted, measurements taken on the TPS23882 EVM and Sifos PSA-3000 PowerSync Analyzer with PSA3202 test cards. Test conditions are $T_J$ = 25 °C, $V_{VDD}$ = 3.3 V, $V_{VPWR}$ = 54 V, $V_{DGND}$ = $V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, 2xFBn = 0. Positive currents are into pins. $R_S$ = 0.200 Ω, to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

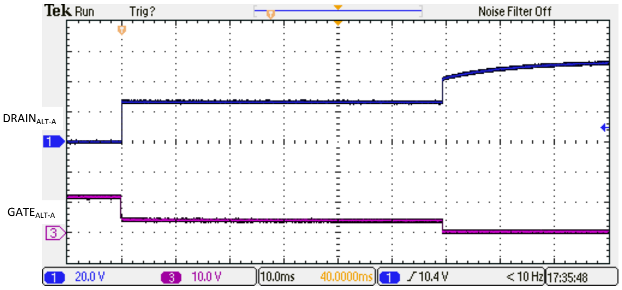


Figure 10-3. $I_{LIM}$ Foldback and Turn Off

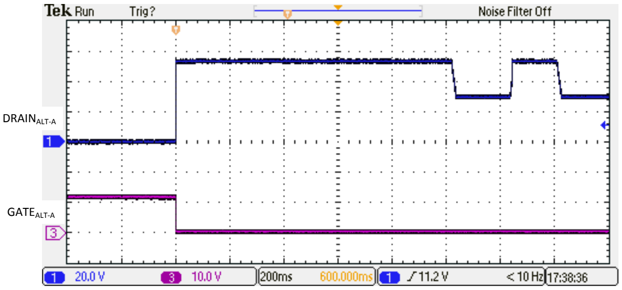


Figure 10-4. Backoff due to PCut Fault

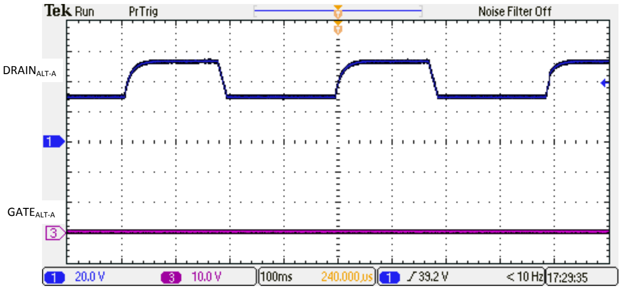


Figure 10-5. Open Circuit Detection Signature

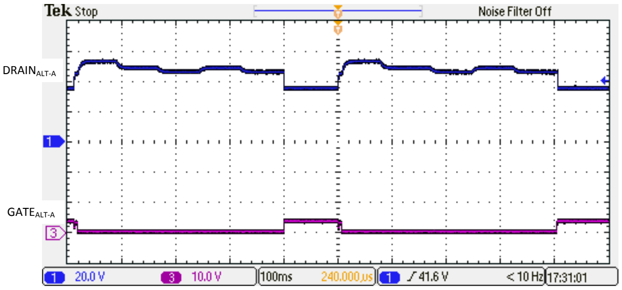


Figure 10-6. Semi-Auto Mode Discovery with a Valid Class 0-3 Load

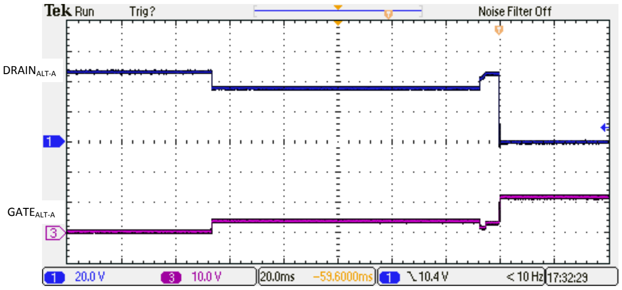


Figure 10-7. 1-Finger Classification and Turn On

### 10.2.3 Application Curves

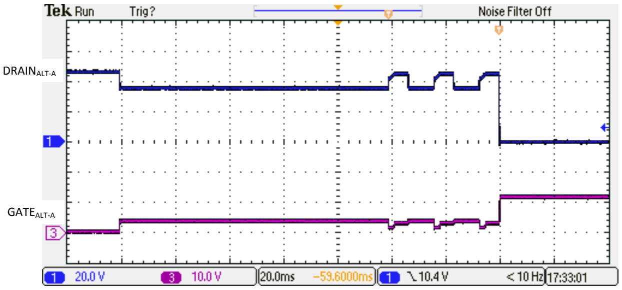


Figure 10-8. 3-Finger Classification and Turn On

### 10.2.3 Application Curves (continued)

# 11 Power Supply Recommendations

## 11.1 VDD

The recommended VDD supply voltage requirement is 3.3 V, ±0.3 V. The TPS23882 requires approximately 6 mA typical and 12 mA maximum from the VDD supply. The VDD supply can be generated from VPWR with a buck-type regulator (A LM5017 based device is recommended) for a higher port count PSE using multiple TPS23882 devices operating in semiauto mode. The power supply design must ensure the VDD rail rises monotonically through the VDD UVLO thresholds without any droop under the UVLO_fall threshold as the loads are turned on. This is accomplished with proper bulk capacitance across the VDD rail for the expected load current steps over worst case design corners. Furthermore, the combination of decoupling capacitance and bulk storage capacitance must hold the VDD rail above the UVLO_fall threshold during any expected transient outages once power is applied.

## 11.2 VPWR

Although the supported VPWR supply voltage range is 44 V to 57 V, as with the 802.3at standard for Type-2 PoE, a 50 V minimum supply is required to comply with 2-Pair Type-3 (up to 30W) IEEE requirements. The TPS23882 requires approximately 10-mA typical and 12-mA maximum from the VPWR supply, but the total output current required from the VPWR supply depends on the number and type of ports required in the system. The TPS23882 can be configured to support either 15.5 W, or 30 W per port and the power limit is set proportionally at turn on. The port power limit, $P_{CUT}$, is also programmable to provide even greater system design flexibility. However, it is generally recommend to size the VPWR supply accordingly to the PoE Type to be supported. As an example, a 130 W or greater power supply would be recommended for eight type 1 (15.5 W each) ports, or a 250 W or greater power supply is recommended for eight 2-pair type 3 (30 W) ports, assuming maximum port and standby currents.

---

**Note**

In IEEE complaint applications, only 4-Pair configured ports are capable of supporting power levels greater than 30 W.

---

# 12 Layout

## 12.1 Layout Guidelines

### 12.1.1 Kelvin Current Sensing Resistors

Load current in each PSE channel is sensed as the voltage across a low-end current-sense resistor with a value of 200 mΩ. For more accurate current sensing, kelvin sensing of the low end of the current-sense resistor is provided through pins KSENSA for channels 1 and 2, KSENSB for channels 3 and 4, KSENSC for channels 5 and 6 and KSENSD for channels 7 and 8.

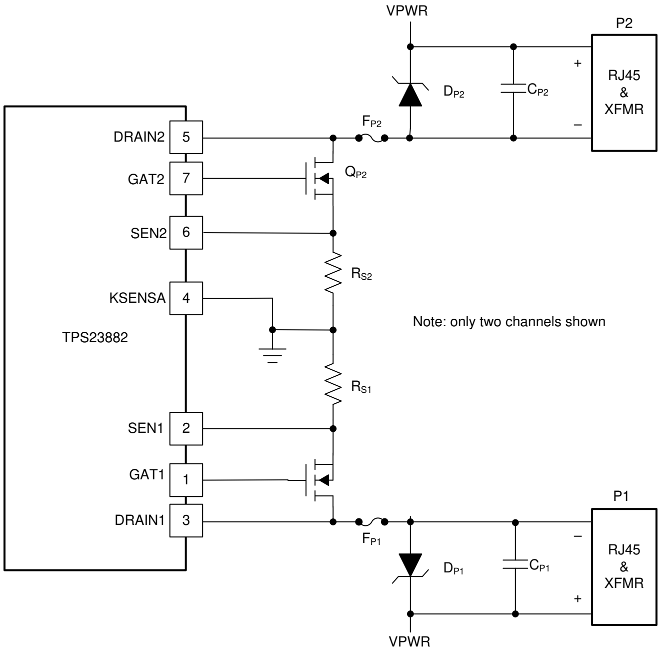


Figure 12-1. Kelvin Current-Sense Connection

KSENSA is shared between SEN1 and SEN2, KSENSB is shared between SEN3 and SEN4, KSENSC is shared between SEN5 and SEN6, and KSENSD is shared between SEN7 and SEN8. To optimize the accuracy of the measurement, the PCB layout must be done carefully to minimize impact of PCB trace resistance. Refer to Figure 12-2 as an example.

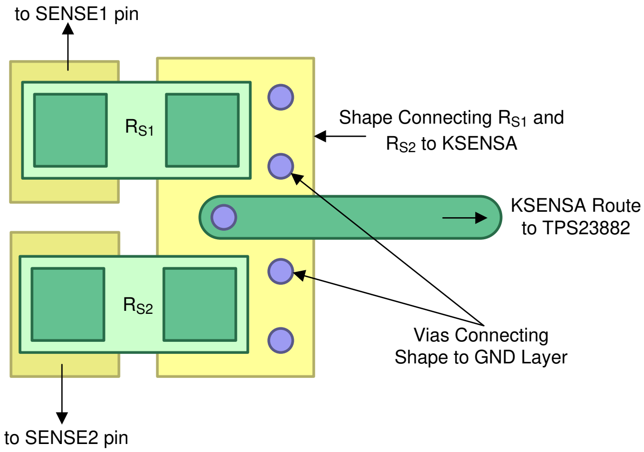
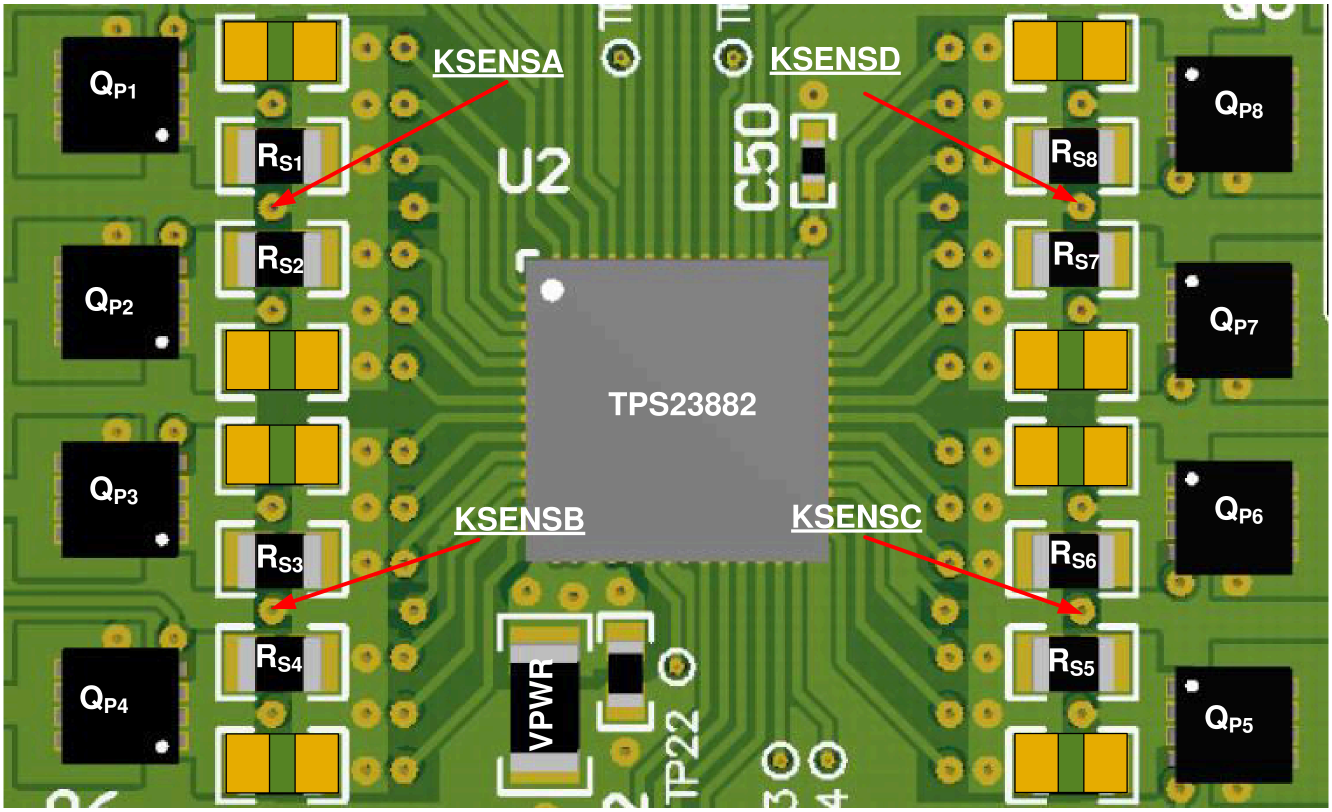


Figure 12-2. Kelvin Sense Layout Example

## 12.2 Layout Example



Note: PCB layout includes footprints for optional parallel $R_{SENSE}$ resistors

**Figure 12-3. Eight Port Layout Example (Top Side)**

### 12.2.1 Component Placement and Routing Guidelines

#### *12.2.1.1 Power Pin Bypass Capacitors*

- **$C_{VPWR}$:** Place close to pin 17 (VPWR) and connect with low inductance traces and vias according to Figure 12-3.
- **$C_{VDD}$:** Place close to pin 43 (VDD) and connect with low inductance traces and vias according to Figure 12-3.

#### *12.2.1.2 Per-Port Components*

- **$R_{SnA}$ / $R_{SnB}$:** Place according to in a manner that facilitates a clean Kelvin connection with KSENSEA/B/C/D.
- **$Q_{Pn}$:** Place $Q_{Pn}$ around the TPS23882 as illustrated in Figure 12-3. Provide sufficient copper from $Q_{Pn}$ drain to $F_{Pn}$.
- **$F_{Pn}$, $C_{Pn}$, $D_{PnA}$, $D_{PnB}$:** Place this circuit group near the RJ45 port connector (or port power interface if a daughter board type of interface is used as illustrated in Figure 12-3). Connect this circuit group to $Q_{Pn}$ drain or GND (TPS23882- AGND) using low inductance traces.

# 13 Device and Documentation Support

## 13.1 Documentation Support

### 13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS23882EVM User's Guide*
- *IEEE 802.3bt Ready PSE Daughter Card for 24-port PSE System*
- Texas Instruments, *How to Load TPS2388x SRAM and Parity Code Over I2C Application Report*
- *TI mySecure Software*

## 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 13.4 Trademarks

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All trademarks are the property of their respective owners.

## 13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS23882RTQR | Active | Production | QFN (RTQ) \| 56 | 2000 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | TPS23882 |
| TPS23882RTQR.A | Active | Production | QFN (RTQ) \| 56 | 2000 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | TPS23882 |
| TPS23882RTQR.B | Active | Production | QFN (RTQ) \| 56 | 2000 \| LARGE T&R | - | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | TPS23882 |
| TPS23882RTQT | Active | Production | QFN (RTQ) \| 56 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | TPS23882 |
| TPS23882RTQT.A | Active | Production | QFN (RTQ) \| 56 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | TPS23882 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

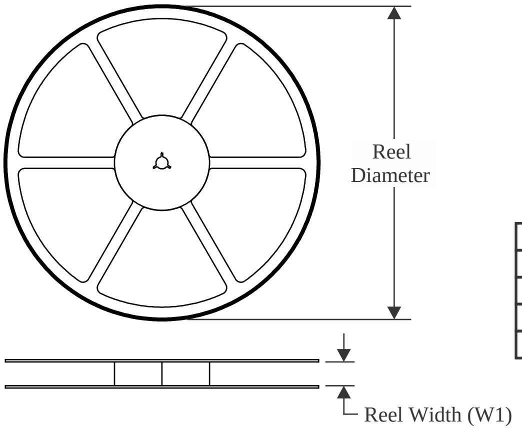
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

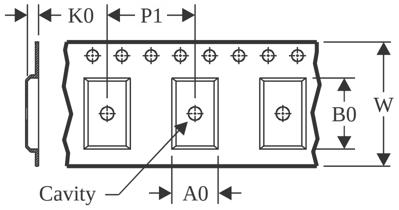
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

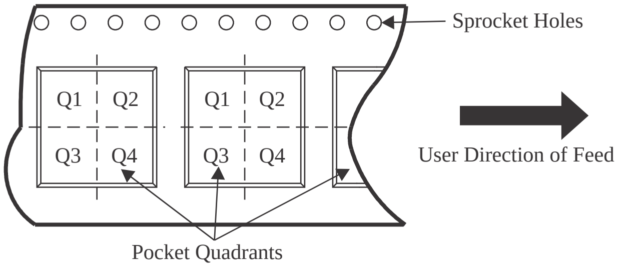


TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

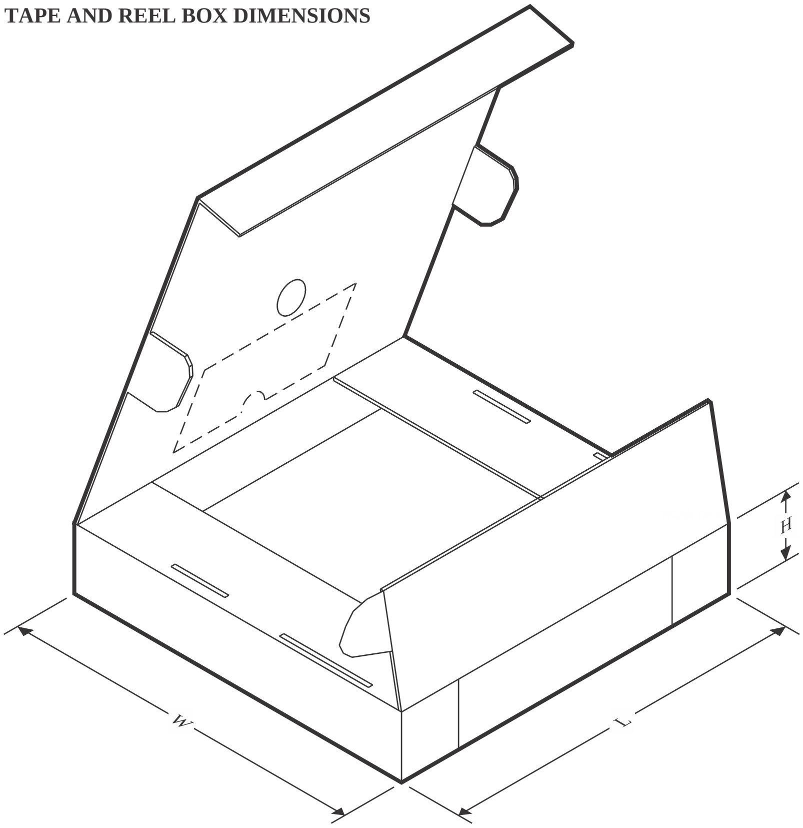
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS23882RTQR | QFN | RTQ | 56 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS23882RTQT | QFN | RTQ | 56 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |

## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS23882RTQR | QFN | RTQ | 56 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS23882RTQT | QFN | RTQ | 56 | 250 | 210.0 | 185.0 | 35.0 |

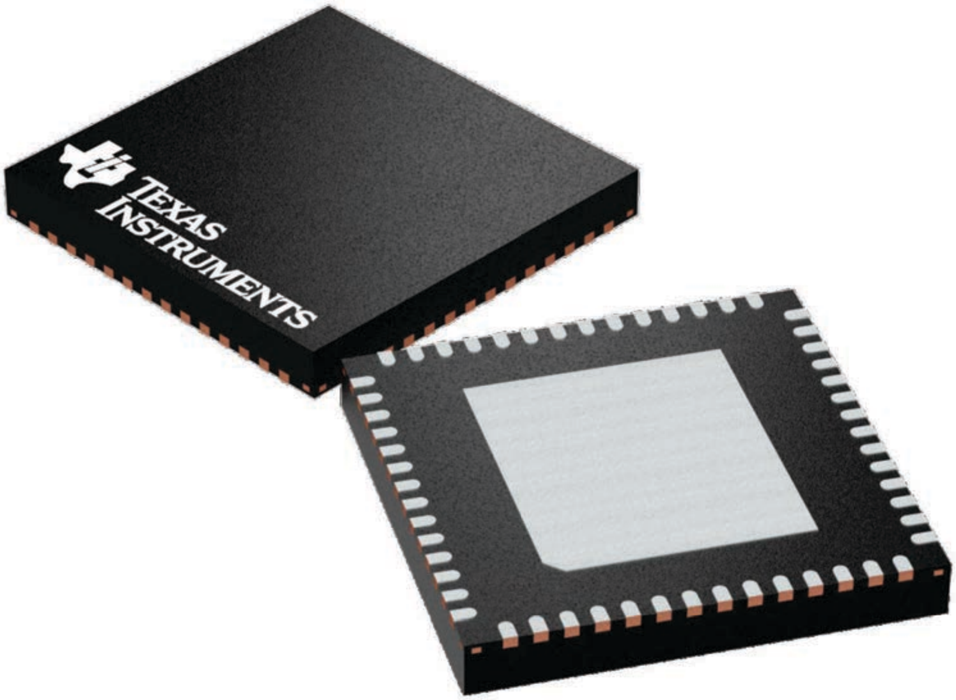
# GENERIC PACKAGE VIEW

**RTQ 56**

**VQFN - 1 mm max height**

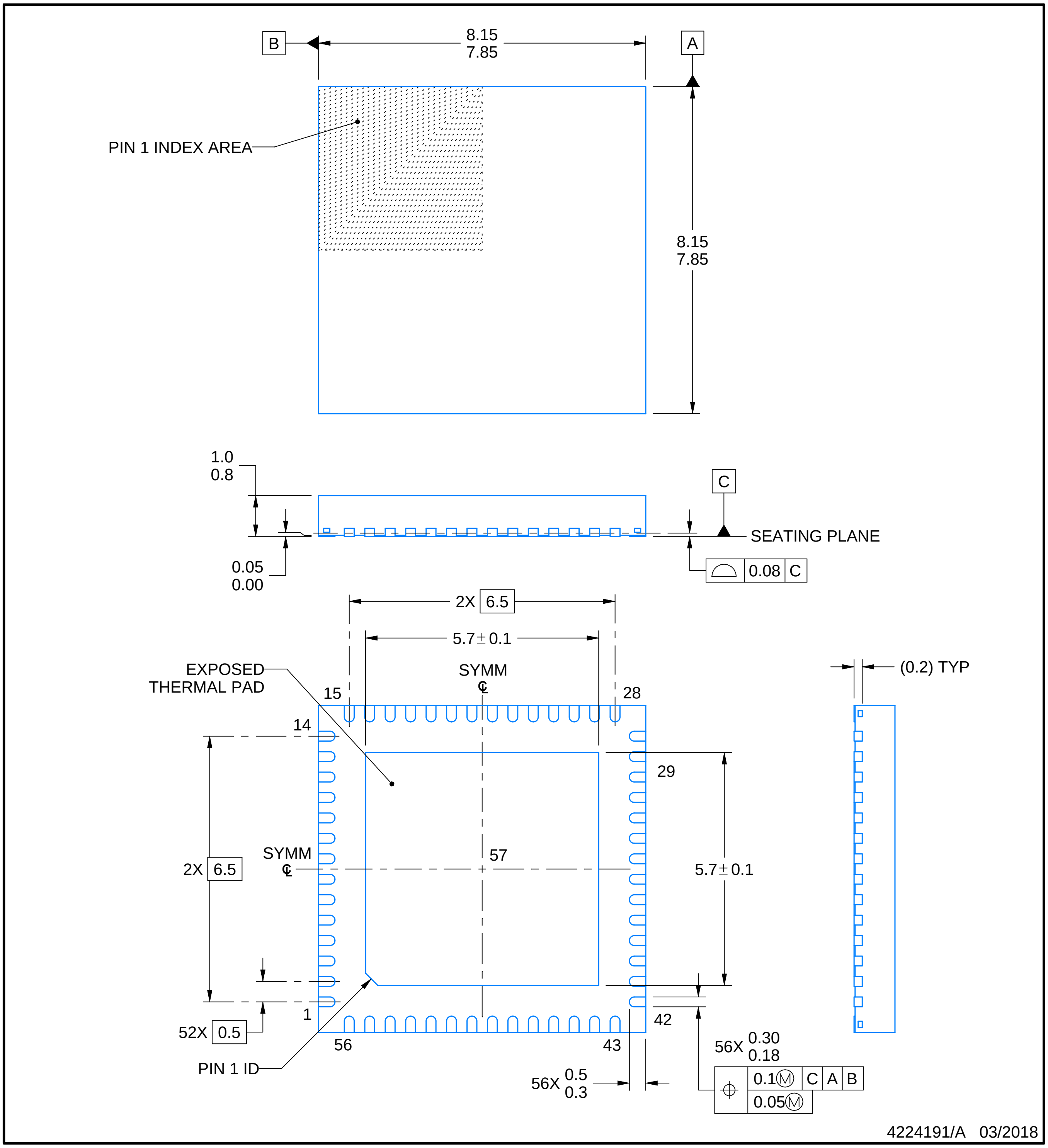
**8 x 8, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD



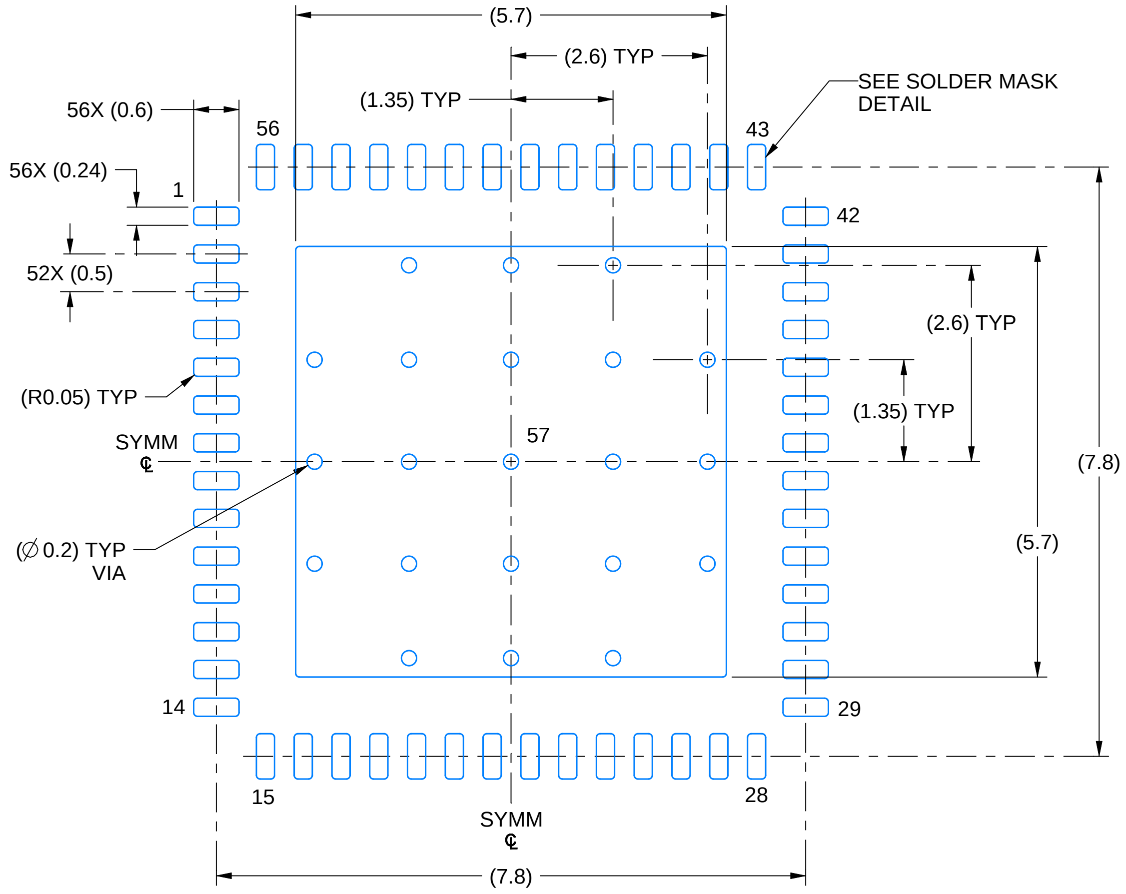
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224653/A

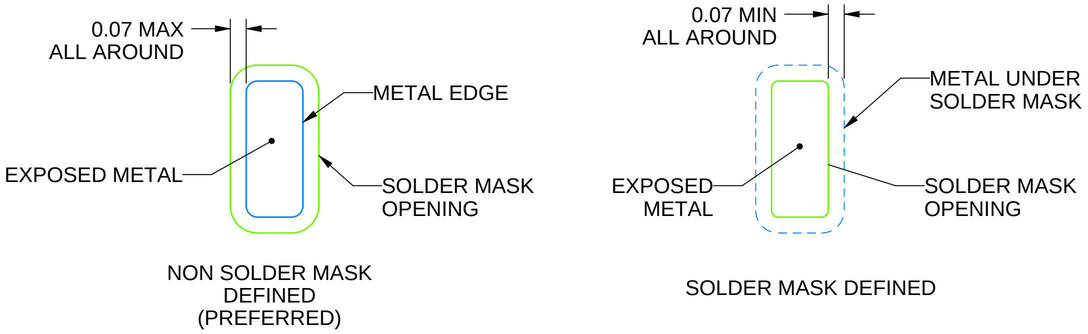


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

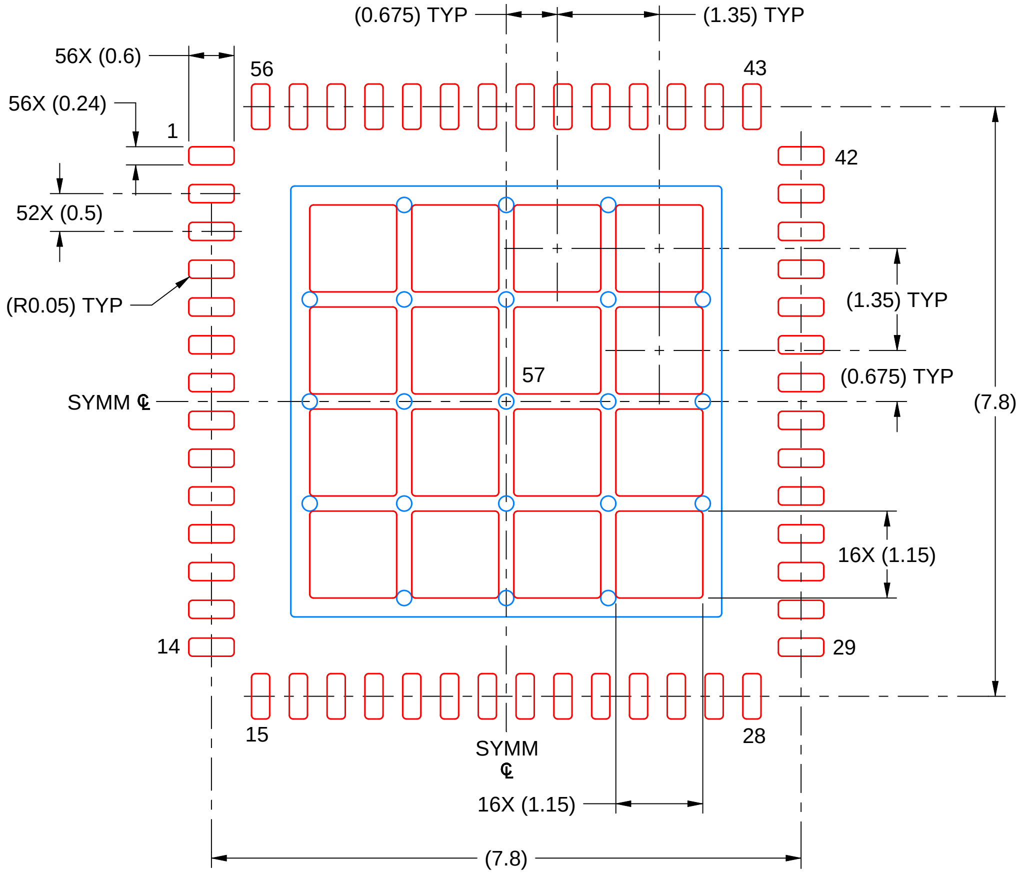


SOLDER MASK DETAILS

4224191/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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