TPS2296xC 5.5-V, 3-A, 13-mΩ On-Resistance Load Switch With Reverse Current Protection and Controlled Turn-On

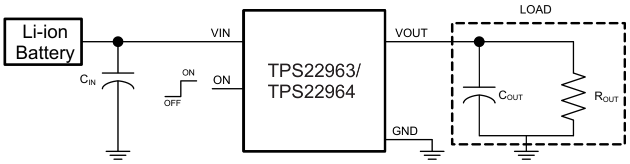
1 Features

- Integrated N-Channel Load Switch
- Input Voltage Range: 1 V to 5.5 V
- Internal Pass-FET R_{DSON} = 8 mΩ (Typ)
- Ultra-Low ON-Resistance
  - R_{ON} = 13 mΩ (Typ) at V_{IN} = 5 V
  - R_{ON} = 14 mΩ (Typ) at V_{IN} = 3.3 V
  - R_{ON} = 18 mΩ (Typ) at V_{IN} = 1.8 V
- 3A Maximum Continuous Switch Current
- Reverse Current Protection (When Disabled)
- Low Shutdown Current (760 nA)
- Low Threshold 1.3-V GPIO Control Input
- Controlled Slew-Rate to Avoid Inrush Current
- Quick Output Discharge (TPS22964 only)
- Six Terminal Wafer-Chip-Scale Package (Nominal Dimensions Shown - See Addendum for Details)
  - 0.9 mm x 1.4 mm, 0.5 mm Pitch, 0.5 mm Height (YZP)
- ESD Performance Tested Per JESD 22
  - 2-kV Human-Body Model (A114-B, Class II)
  - 500-V Charged-Device Model (C101)

2 Applications

- Smartphones
- Notebook Computer and Ultrabook™
- Tablet PC Computer
- Solid State Drives (SSD)
- DTV/IP Set Top Box
- POS Terminals and Media Gateways

4 Simplified Schematic



3 Description

The TPS22963/64 is a small, ultra-low R_{ON} load switch with controlled turn on. The device contains a low R_{DSON} N-Channel MOSFET that can operate over an input voltage range of 1 V to 5.5 V and switch currents of up to 3 A. An integrated charge pump biases the NMOS switch in order to achieve a low switch ON-Resistance. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage GPIO control signals. The rise time of the TPS22963/64 device is internally controlled in order to avoid inrush current.

The TPS22963/64 provides reverse current protection. When the power switch is disabled, the device will not allow the flow of current towards the input side of the switch. The reverse current protection feature is active only when the device is disabled so as to allow for intentional reverse current (when the switch is enabled) for some applications.

The TPS22963/64 is available in a small, space-saving 6-pin WCSP package and is characterized for operation over the free air temperature range of –40°C to 85°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2296xC	DSBGA (6)	1.40 mm x 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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5 Revision History

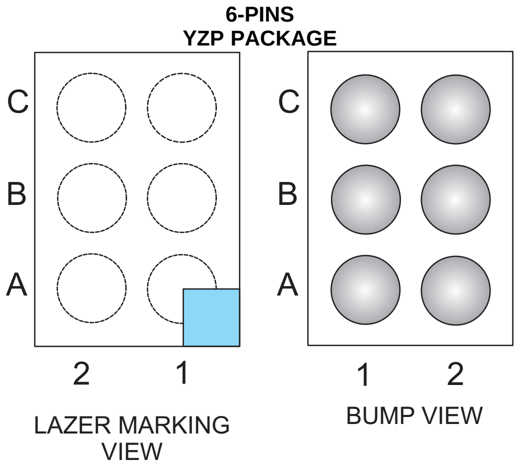
Changes from Original (June 2013) to Revision A	**Page**
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

6 Device Comparison Table

	R_{ON} (Typ) at 3.3 V	Rise Time (Typ) at 3.3 V(1)	Quick Output Discharge (QOD)(2)	Maximum Output Current	Enable
TPS22963C	14 mΩ	715 µs	No	3 A	Active High
TPS22964C	14 mΩ	715 µs	Yes	3 A	Active High

(1) Additional rise time options are possible. Contact factory for more information.
(2) This feature discharges the output of the switch to ground through a 273 Ω resistor, preventing the output from floating (only in TPS22964C).

7 Pin Configuration and Functions



Pin Assignments (YZP Package)

C	GND	ON
B	VOUT	VIN
A	VOUT	VIN
	1	**2**

Pin Functions

PIN		I/O	DESCRIPTION
TPS22963/64	**NAME**		
C1	GND	-	Ground
C2	ON	I	Switch control input, active high. Do not leave floating
A1, B1	VOUT	O	Switch output
A2, B2	VIN	I	Switch input. Use a bypass capacitor to ground (ceramic)

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	–0.3	6	V
V_{OUT}	Output voltage range	–0.3	6	V
V_{ON}	ON pin voltage range	–0.3	6	V
I_{MAX}	Maximum continuous switch current		3	A
I_{PLS}	Maximum pulsed switch current, 100 µs pulse, 2% duty cycle, T_A = –40°C to 85°C		4	A
T_A	Operating free air temperature range	–40	85	°C
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range	–65	150	°C

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1		5.5	V
V_{OUT}	Output voltage range		0		5.5	V
$V_{IH, ON}$	High-level ON voltage	V_{IN} = 2.5 V to 5.5 V	1.3		5.5	V
		V_{IN} = 1 V to 2.49 V	1.1		5.5	
$V_{IL, ON}$	Low-level ON voltage	V_{IN} = 2.5 V to 5.5 V	0		0.6	V
		V_{IN} = 1 V to 2.49 V	0		0.4	
C_{IN}	Input capacitor			1(1)		µF

(1) Refer to the application section

8.4 Thermal Information

THERMAL METRIC(1)		TPS2296xC	UNIT
		YZP	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.0	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	1.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.8	
ψ_{JT}	Junction-to-top characterization parameter	5.7	
ψ_{JB}	Junction-to-board characterization parameter	22.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

V_{IN} = 1 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{Q,\ VIN}$	Quiescent current	I_{OUT} = 0, V_{ON} = V_{IN} = 5 V	Full		66.5	96	µA
		I_{OUT} = 0, V_{ON} = V_{IN} = 4.5 V	Full		57	82	
		I_{OUT} = 0, V_{ON} = V_{IN} = 3.3 V	Full		38	60	
		I_{OUT} = 0, V_{ON} = V_{IN} = 2.5 V	Full		33.3	55	
		I_{OUT} = 0, V_{ON} = V_{IN} = 1.8 V	Full		28.3	45	
		I_{OUT} = 0, V_{ON} = V_{IN} = 1.2 V	Full		22.8	36	
		I_{OUT} = 0, V_{ON} = V_{IN} = 1.1 V	Full		21.6	34	
		I_{OUT} = 0, V_{ON} = V_{IN} = 1 V	Full		20.3	33	
$I_{SD,\ VIN}$	Shut down current	V_{ON} = 0, V_{IN} = 5 V, V_{OUT} = 0 V	Full		0.76	2	µA
		V_{ON} = 0, V_{IN} = 1 V, V_{OUT} = 0 V	Full		0.07	0.8	
R_{ON}	On-resistance	V_{IN} = 5 V, I_{OUT} = –200 mA	25°C		13.3	21	mΩ
			Full			26	
		V_{IN} = 4.5 V, I_{OUT} = –200 mA	25°C		13.3	21	mΩ
			Full			26	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA	25°C		13.8	22	mΩ
			Full			27	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA	25°C		15.4	24	mΩ
			Full			29	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA	25°C		18.2	28	mΩ
			Full			33	
		V_{IN} = 1.2 V, I_{OUT} = –200 mA	25°C		25.6	37	mΩ
			Full			44	
		V_{IN} = 1.1 V, I_{OUT} = –200 mA	25°C		28.7	41	mΩ
			Full			50	
		V_{IN} = 1 V, I_{OUT} = –200 mA	25°C		33.8	48	mΩ
			Full			60	
$V_{HYS,\ ON}$	ON pin hysteresis	V_{IN} = 5 V	Full		115		mV
		V_{IN} = 4.5 V	Full		105		
		V_{IN} = 3.3 V	Full		80		
		V_{IN} = 2.5 V	Full		65		
		V_{IN} = 1.8 V	Full		50		
		V_{IN} = 1.2 V	Full		35		
		V_{IN} = 1.1 V	Full		30		
		V_{IN} = 1 V	Full		30		
I_{ON}	ON pin leakage current	V_{ON} = 1.1 V to 5.5 V	Full			150	nA
$I_{RC,\ VIN}$	Reverse current when disabled	V_{IN} = V_{ON} = 0 V, V_{OUT} = 5 V	25°C		–0.02		µA
			85°C		–2.1		
R_{PD}(1)	Output pulldown resistance	V_{ON} = 0 V, I_{OUT} = 2 mA	Full		273	325	Ω

(1) Available in TPS22964 only.

8.6 Switching Characteristics

PARAMETER		TEST CONDITION	TPS22963/64 TYP	UNIT
V_{IN} = 5.0 V, T_A = 25°C (unless otherwise noted)				
t_{ON}	Turn-ON time	R_{OUT} = 10Ω, C_{IN} = 1μF, C_{OUT} = 0.1μF	928	μs
t_{OFF}	Turn-OFF time	R_{OUT} = 10Ω, C_{IN} = 1μF, C_{OUT} = 0.1μF	2.5	
t_R	VOUT rise time	R_{OUT} = 10Ω, C_{IN} = 1μF, C_{OUT} = 0.1μF	890	
t_F	VOUT fall time	R_{OUT} = 10Ω, C_{IN} = 1μF, C_{OUT} = 0.1μF	2.1	
t_D	Delay time	R_{OUT} = 10Ω, C_{IN} = 1μF, C_{OUT} = 0.1μF	561	
V_{IN} = 4.5 V, T_A = 25°C (unless otherwise noted)				
t_{ON}	Turn-ON time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	905	μs
t_{OFF}	Turn-OFF time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	2.6	
t_R	VOUT rise time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	859	
t_F	VOUT fall time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	2.1	
t_D	Delay time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	560	
V_{IN} = 3.3 V, T_A = 25°C (unless otherwise noted)				
t_{ON}	Turn-ON time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	836	μs
t_{OFF}	Turn-OFF time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	2.8	
t_R	VOUT rise time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	715	
t_F	VOUT fall time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	2	
t_D	Delay time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	553	
V_{IN} = 1.8 V, T_A = 25°C (unless otherwise noted)				
t_{ON}	Turn-ON time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	822	μs
t_{OFF}	Turn-OFF time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	2.8	
t_R	VOUT rise time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	651	
t_F	VOUT fall time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	2	
t_D	Delay time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	558	
V_{IN} = 1.2 V, T_A = 25°C (unless otherwise noted)				
t_{ON}	Turn-ON time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	852	μs
t_{OFF}	Turn-OFF time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	3.2	
t_R	VOUT rise time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	535	
t_F	VOUT fall time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	1.8	
t_D	Delay time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	594	
V_{IN} = 1.1 V, T_A = 25°C (unless otherwise noted)				
t_{ON}	Turn-ON time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	861	μs
t_{OFF}	Turn-OFF time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	3.5	
t_R	VOUT rise time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	518	
t_F	VOUT fall time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	1.9	
t_D	Delay time	R_{OUT} = 10 Ω, C_{IN} = 1 μF, C_{OUT} = 0.1 μF	604	

8.7 Typical Electrical Characteristics

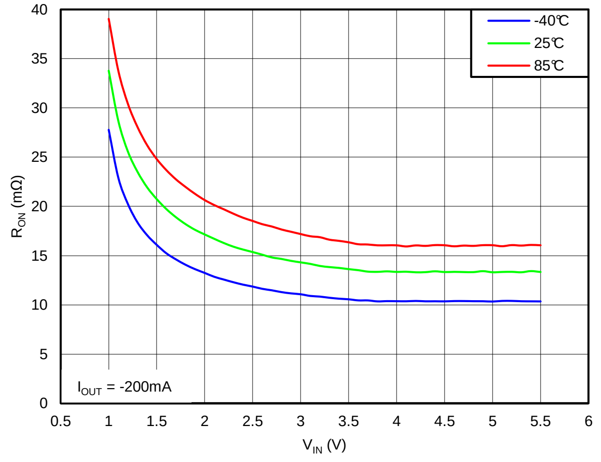


Figure 1. On Resistance vs V_{IN}

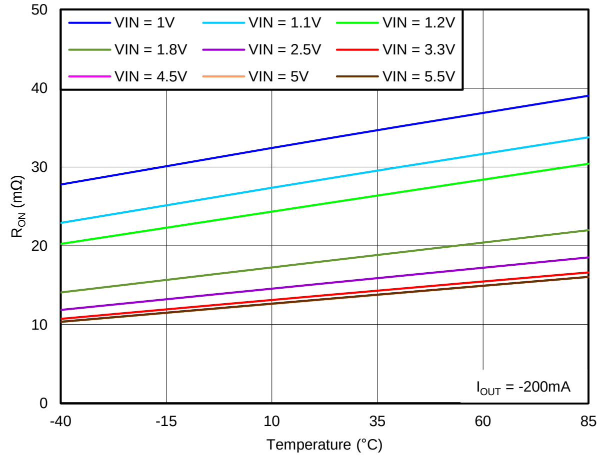


Figure 2. On Resistance vs Temperature

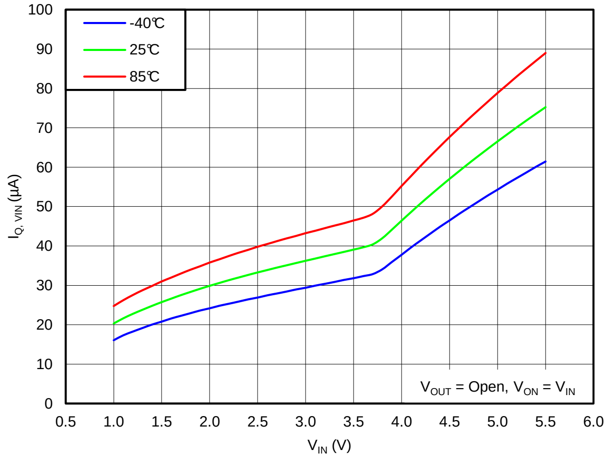


Figure 3. Quiescent Current vs V_{IN}

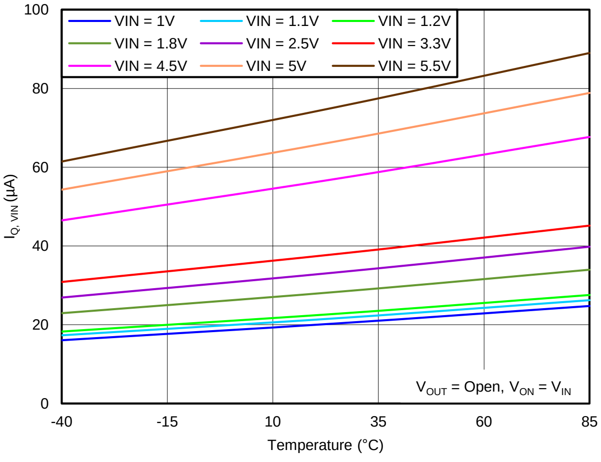


Figure 4. Quiescent Current vs Temperature

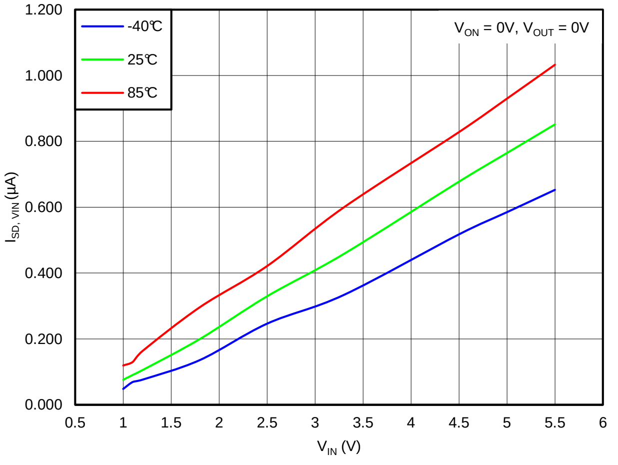


Figure 5. Shut Down Current vs V_{IN}

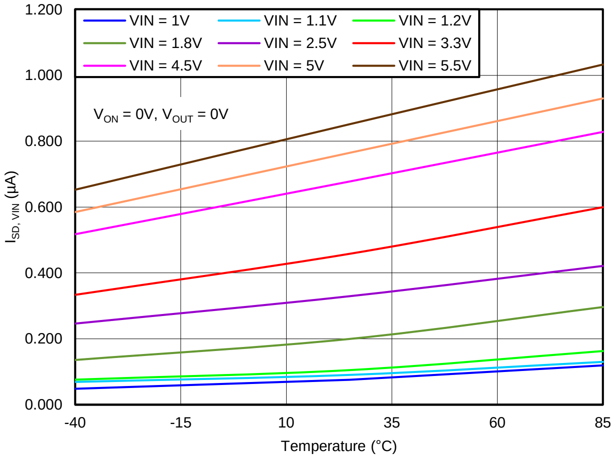


Figure 6. Shut Down Current vs Temperature

Typical Electrical Characteristics (continued)

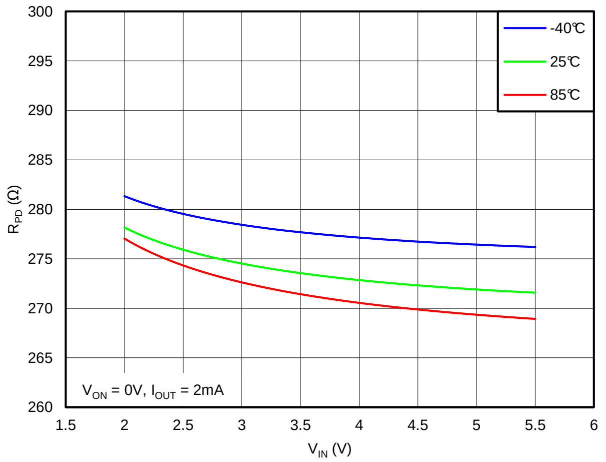


Figure 7. Output Pulldown Resistance vs V_{IN}

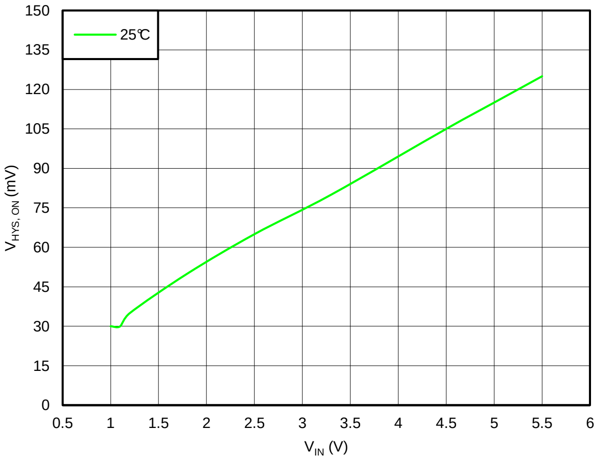


Figure 8. On Pin Hysteresis vs V_{IN}

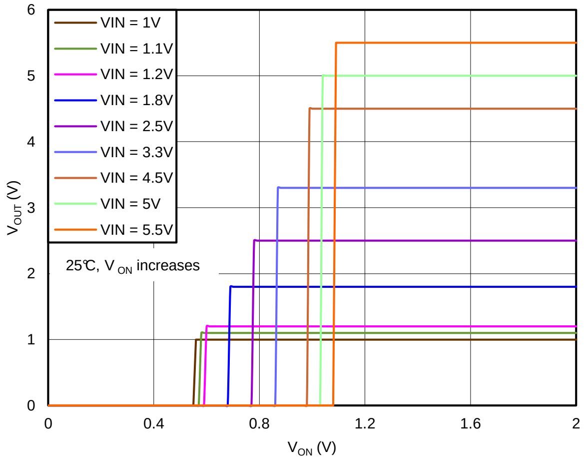


Figure 9. Output Voltage vs V_{ON} Rising

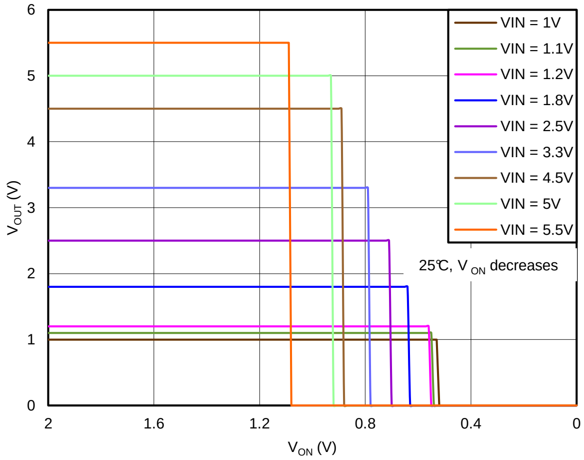


Figure 10. Output Voltage vs V_{ON} Falling

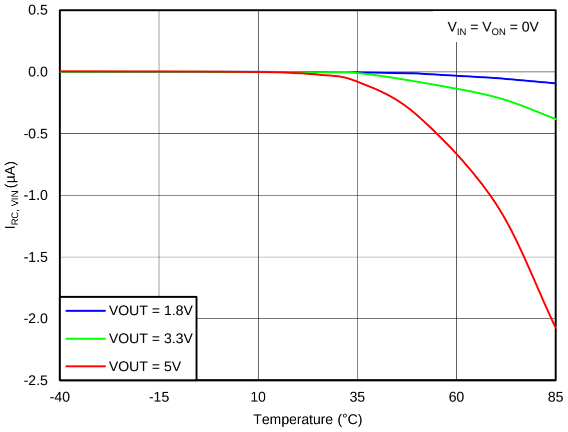


Figure 11. Reverse Current When Disabled vs Temperature

8.8 Typical Switching Characteristics

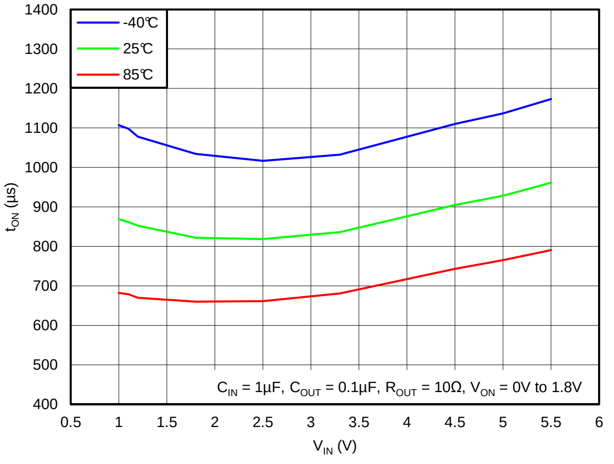


Figure 12. Turn-On Time vs V_{IN}

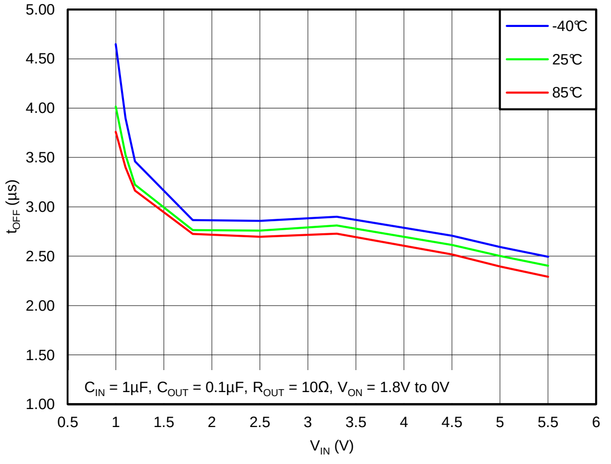


Figure 13. Turn-Off Time vs V_{IN}

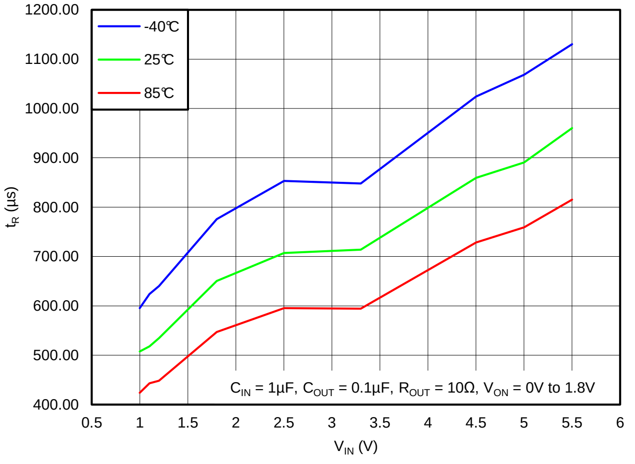


Figure 14. V_{OUT} Rise Time vs V_{IN}

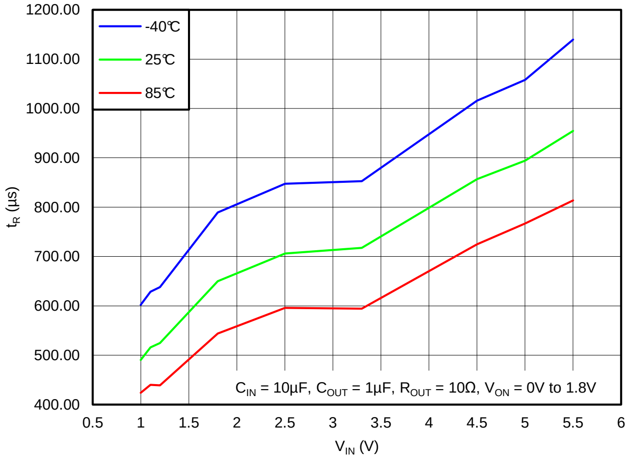


Figure 15. V_{OUT} Rise Time vs V_{IN}

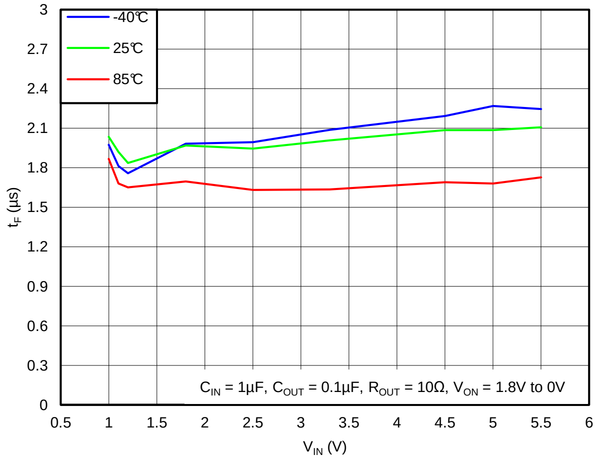


Figure 16. V_{OUT} Fall Time vs V_{IN}

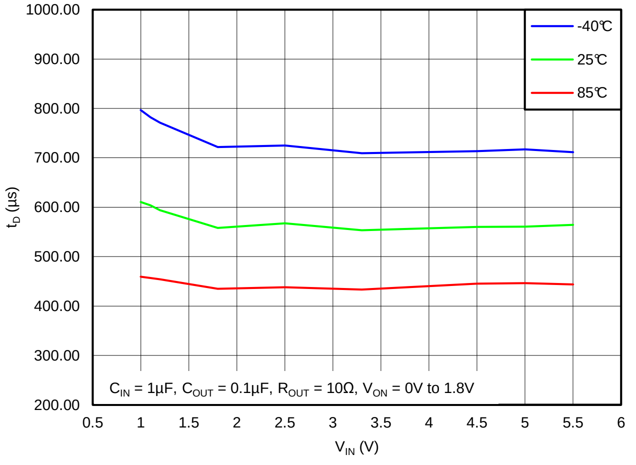
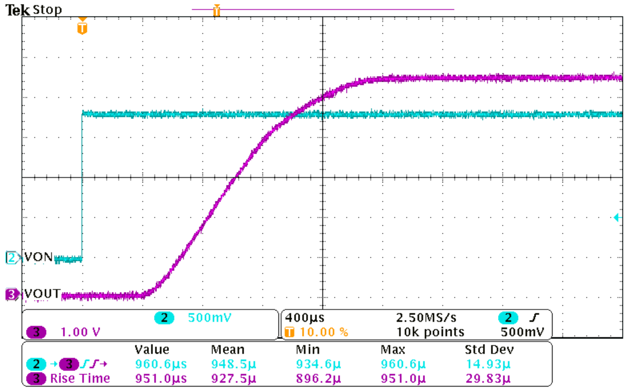


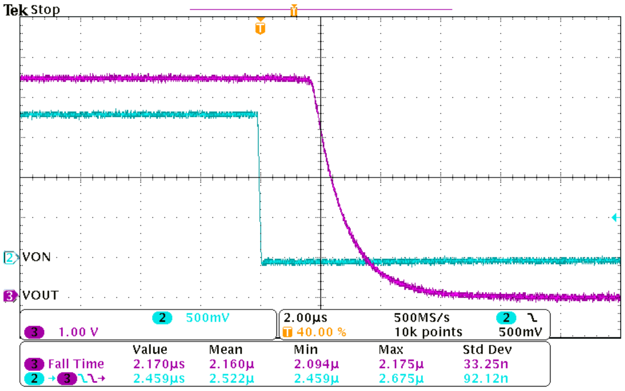
Figure 17. Delay Time vs V_{IN}

8.9 Typical AC Scope Captures at T_A = 25ºC



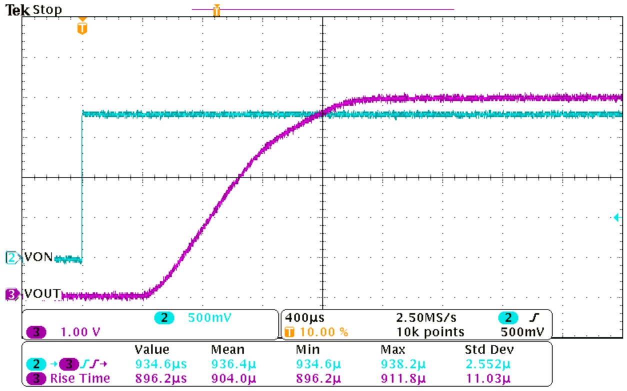
	Value	Mean	Min	Max	Std Dev
2 → 3 ʃʃ→	960.6µs	948.5µ	934.6µ	960.6µ	14.93µ
3 Rise Time	951.0µs	927.5µ	896.2µ	951.0µ	29.83µ

Figure 18. Turn-On Response Time (V_{IN} = 5.5 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



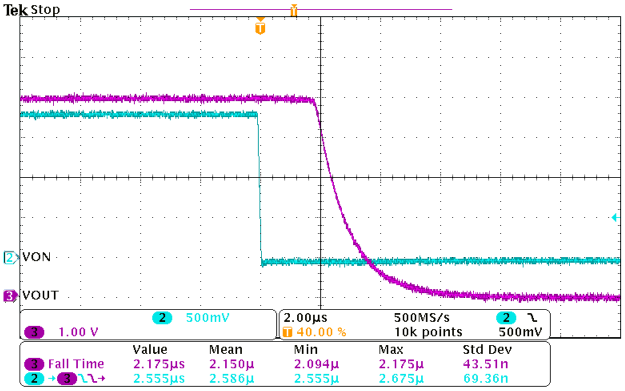
	Value	Mean	Min	Max	Std Dev
3 Fall Time	2.170µs	2.160µ	2.094µ	2.175µ	33.25n
2 → 3 ʅʅ→	2.459µs	2.522µ	2.459µ	2.675µ	92.12n

Figure 19. Turn-Off Response Time (V_{IN} = 5.5 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



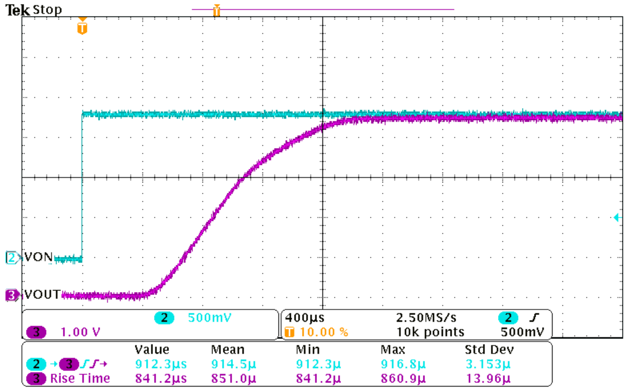
	Value	Mean	Min	Max	Std Dev
2 → 3 ʃʃ→	934.6µs	936.4µ	934.6µ	938.2µ	2.552µ
3 Rise Time	896.2µs	904.0µ	896.2µ	911.8µ	11.03µ

Figure 20. Turn-On Response Time (V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



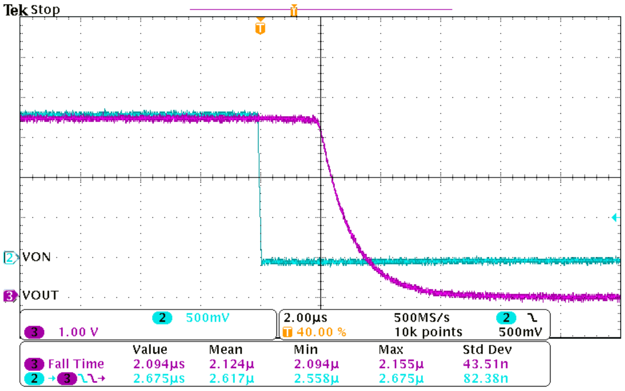
	Value	Mean	Min	Max	Std Dev
3 Fall Time	2.175µs	2.150µ	2.094µ	2.175µ	43.51n
2 → 3 ʅʅ→	2.555µs	2.586µ	2.555µ	2.675µ	69.36n

Figure 21. Turn-Off Response Time (V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



	Value	Mean	Min	Max	Std Dev
2 → 3 ʃʃ→	912.3µs	914.5µ	912.3µ	916.8µ	3.153µ
3 Rise Time	841.2µs	851.0µ	841.2µ	860.9µ	13.96µ

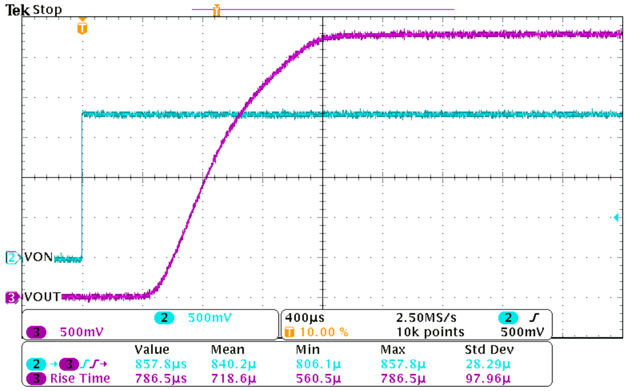
Figure 22. Turn-On Response Time (V_{IN} = 4.5 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



	Value	Mean	Min	Max	Std Dev
3 Fall Time	2.094µs	2.124µ	2.094µ	2.155µ	43.51n
2 → 3 ʅʅ→	2.675µs	2.617µ	2.558µ	2.675µ	82.38n

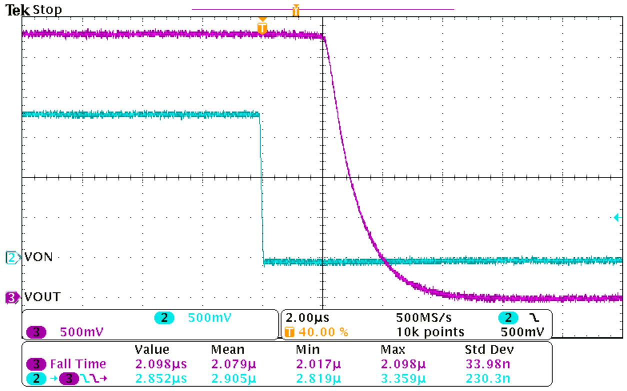
Figure 23. Turn-Off Response Time (V_{IN} = 4.5 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)

Typical AC Scope Captures at T_A = 25ºC (continued)



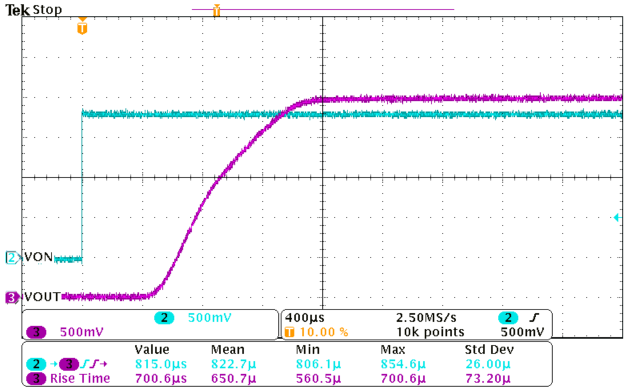
	Value	Mean	Min	Max	Std Dev
2 → 3 ↗↗→	857.8µs	840.2µ	806.1µ	857.8µ	28.29µ
3 Rise Time	786.5µs	718.6µ	560.5µ	786.5µ	97.96µ

Figure 24. Turn-On Response Time (V_{IN} = 3.3 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



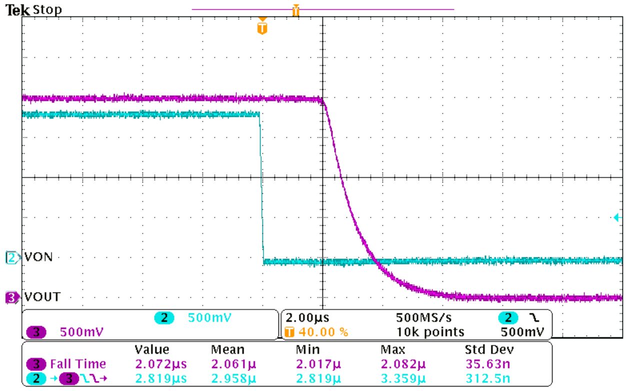
	Value	Mean	Min	Max	Std Dev
3 Fall Time	2.098µs	2.079µ	2.017µ	2.098µ	33.98n
2 → 3 ↘↘→	2.852µs	2.905µ	2.819µ	3.359µ	230.3n

Figure 25. Turn-Off Response Time (V_{IN} = 3.3 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



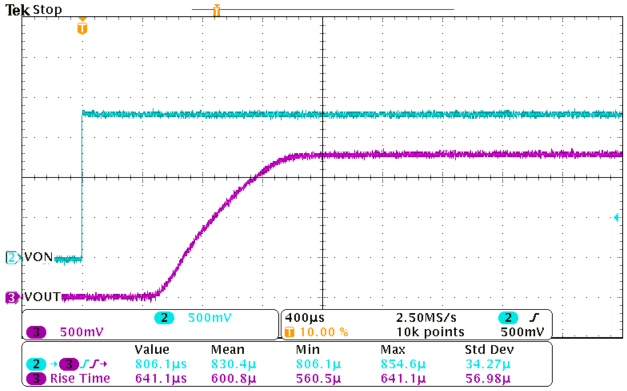
	Value	Mean	Min	Max	Std Dev
2 → 3 ↗↗→	815.0µs	822.7µ	806.1µ	854.6µ	26.00µ
3 Rise Time	700.6µs	650.7µ	560.5µ	700.6µ	73.20µ

Figure 26. Turn-On Response Time (V_{IN} = 2.5 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



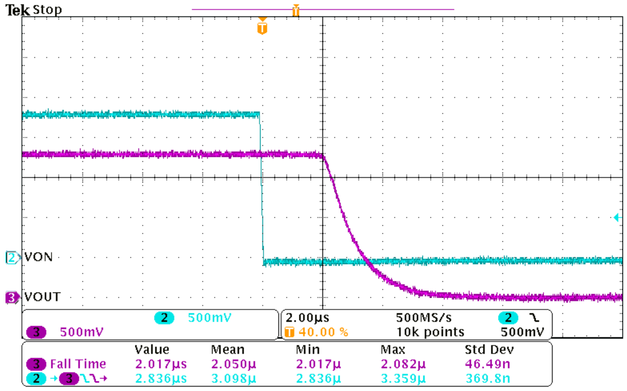
	Value	Mean	Min	Max	Std Dev
3 Fall Time	2.072µs	2.061µ	2.017µ	2.082µ	35.63n
2 → 3 ↘↘→	2.819µs	2.958µ	2.819µ	3.359µ	312.5n

Figure 27. Turn-Off Response Time (V_{IN} = 2.5 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



	Value	Mean	Min	Max	Std Dev
2 → 3 ↗↗→	806.1µs	830.4µ	806.1µ	854.6µ	34.27µ
3 Rise Time	641.1µs	600.8µ	560.5µ	641.1µ	56.98µ

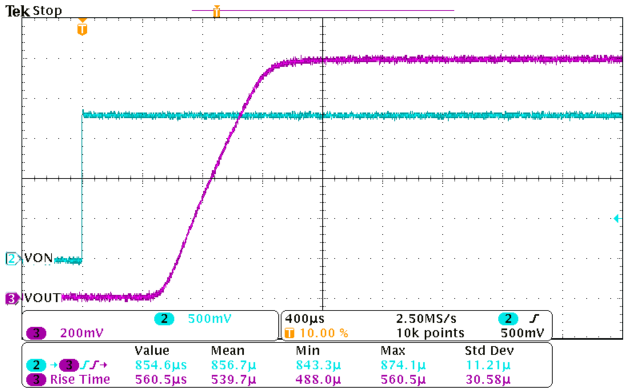
Figure 28. Turn-On Response Time (V_{IN} = 1.8 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



	Value	Mean	Min	Max	Std Dev
3 Fall Time	2.017µs	2.050µ	2.017µ	2.082µ	46.49n
2 → 3 ↘↘→	2.836µs	3.098µ	2.836µ	3.359µ	369.8n

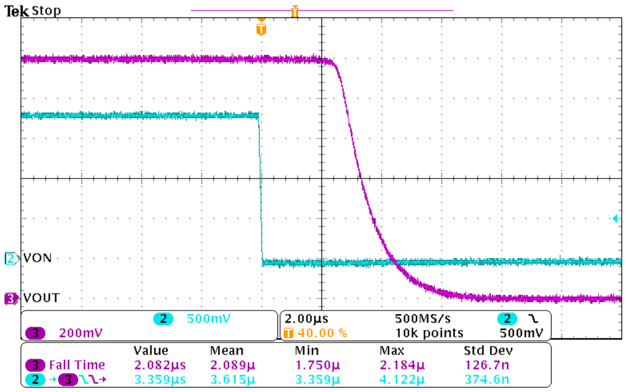
Figure 29. Turn-Off Response Time (V_{IN} = 1.8 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)

Typical AC Scope Captures at T_A = 25ºC (continued)



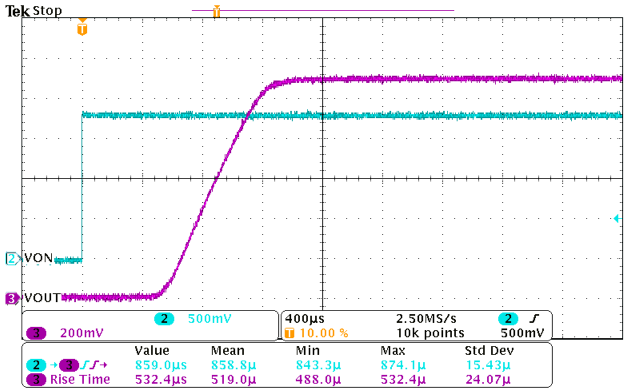
	Value	Mean	Min	Max	Std Dev
2 → 3 ∫∫→	854.6µs	856.7µ	843.3µ	874.1µ	11.21µ
3 Rise Time	560.5µs	539.7µ	488.0µ	560.5µ	30.58µ

Figure 30. Turn-On Response Time (V_{IN} = 1.2 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



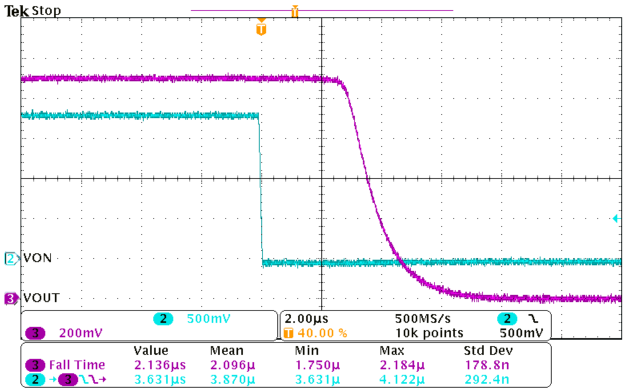
	Value	Mean	Min	Max	Std Dev
3 Fall Time	2.082µs	2.089µ	1.750µ	2.184µ	126.7n
2 → 3 ʅʅ→	3.359µs	3.615µ	3.359µ	4.122µ	374.6n

Figure 31. Turn-Off Response Time (V_{IN} = 1.2 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



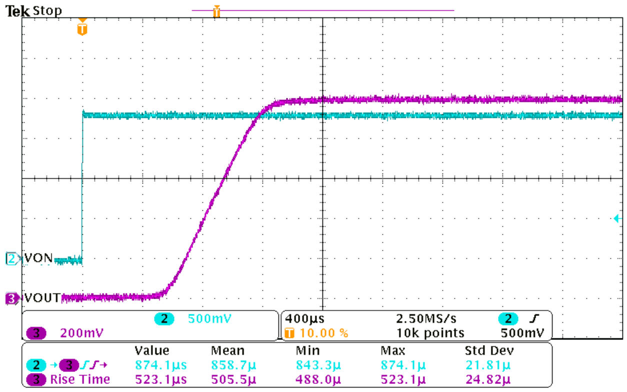
	Value	Mean	Min	Max	Std Dev
2 → 3 ∫∫→	859.0µs	858.8µ	843.3µ	874.1µ	15.43µ
3 Rise Time	532.4µs	519.0µ	488.0µ	532.4µ	24.07µ

Figure 32. Turn-On Response Time (V_{IN} = 1.1 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



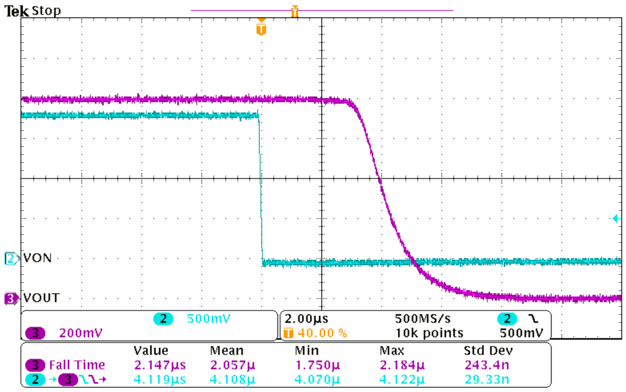
	Value	Mean	Min	Max	Std Dev
3 Fall Time	2.136µs	2.096µ	1.750µ	2.184µ	178.8n
2 → 3 ʅʅ→	3.631µs	3.870µ	3.631µ	4.122µ	292.4n

Figure 33. Turn-Off Response Time (V_{IN} = 1.1 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



	Value	Mean	Min	Max	Std Dev
2 → 3 ∫∫→	874.1µs	858.7µ	843.3µ	874.1µ	21.81µ
3 Rise Time	523.1µs	505.5µ	488.0µ	523.1µ	24.82µ

Figure 34. Turn-On Response Time (V_{IN} = 1 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)



	Value	Mean	Min	Max	Std Dev
3 Fall Time	2.147µs	2.057µ	1.750µ	2.184µ	243.4n
2 → 3 ʅʅ→	4.119µs	4.108µ	4.070µ	4.122µ	29.33n

Figure 35. Turn-Off Response Time (V_{IN} = 1 V, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, R_{OUT} = 10 Ω)

9 Parametric Measurement Information

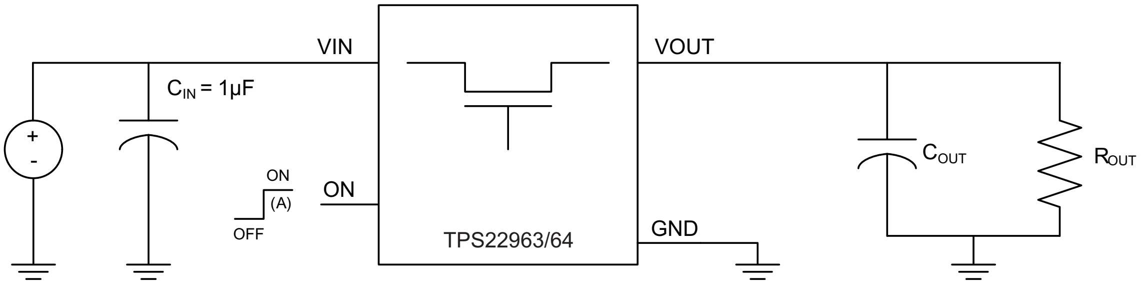
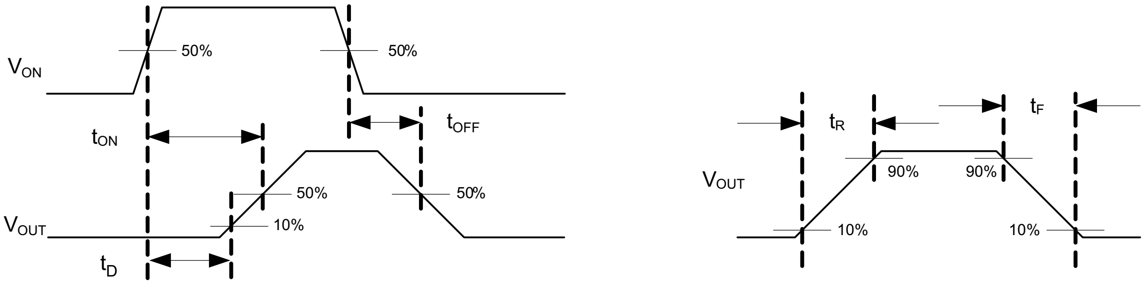


Figure 36. Test Circuit



A. Rise and fall times of the control signal are 100 ns.

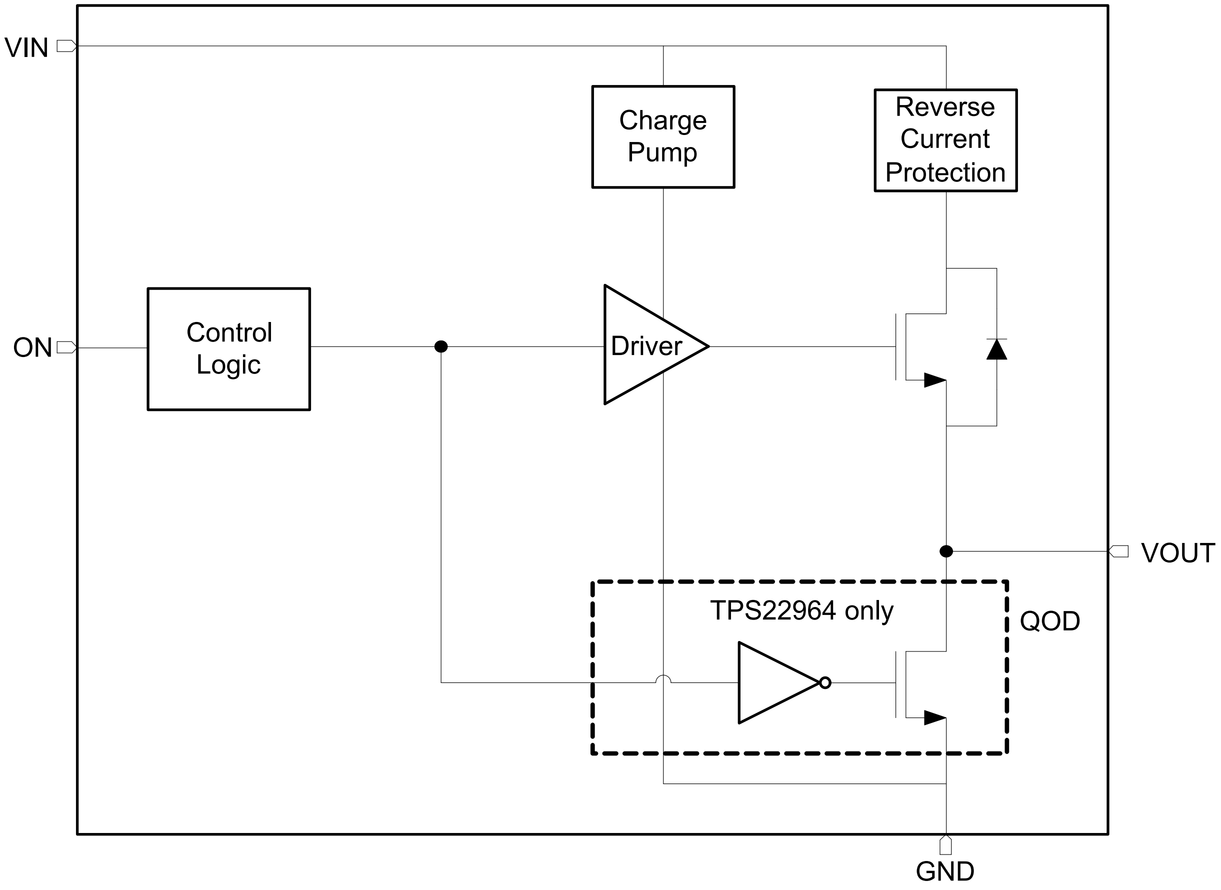
Figure 37. Timing Waveforms

10 Detailed Description

10.1 Overview

The TPS22963/64 is a single channel, 3-A load switch in a small, space saving CSP-6 package. These devices implement an N-channel MOSFET to provide an ultra-low On-resistance for a low voltage drop across the device. A controlled rise time is used in applications to limit the inrush current.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 On/Off Control

The ON pin controls the state of the switch. It is an active “High” pin and has a low threshold making it capable of interfacing with low voltage GPIO control signals. It can be used with any microcontroller with 1.2 V, 1.8 V, 2.5 V, 3.3 V or 5.5 V GPIOs. Applying V_{IH} on the ON pin will put the switch in the ON-state and V_{IL} will put the switch in the OFF-state.

10.3.2 Quick Output Discharge

The TPS22964 includes the Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistance with a typical value of 273Ω is connected between the output and ground. This resistance pulls down the output and prevents it from floating when the device is disabled.

10.4 Device Functional Modes

Table 1. Function Table

ON	VIN to VOUT	OUTPUT DISCHARGE(1) (2)
L	OFF	ACTIVE
H	ON	DISABLED

(1) This feature discharges the output of the switch to ground through a 273 Ω resistor, preventing the output from floating.
(2) This feature is in the TPS22964 device only (not in the TPS22963).

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

11.1.1 Input Capacitor

It is recommended to place a capacitor (C_{IN}) between VIN and GND pins of TPS22963/64. This capacitor helps to limit the voltage drop on the input voltage supply when the switch turns ON into a discharged load capacitor. A 1-µF ceramic capacitor that is placed close to the IC pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop in high current applications.

11.1.2 Output Capacitor

It is recommended to place a capacitor (C_{OUT}) between VOUT and GND pins of TPS22963/64. This capacitor acts as a low pass filter along with the switch ON-resistance to remove any voltage glitches coming from the input voltage source. It is generally recommended to have C_{IN} greater than C_{OUT} so that once the switch is turned ON, C_{OUT} can charge up to V_{IN} without V_{IN} dropping significantly. A 0.1-µF ceramic capacitor that is placed close to the IC pins is usually sufficient.

Application Information (continued)

11.1.3 Standby Power Reduction

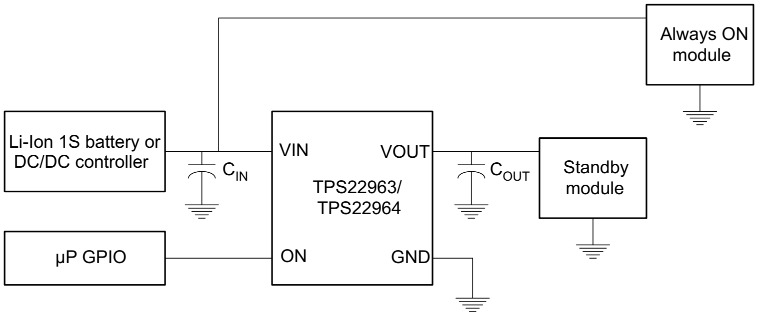


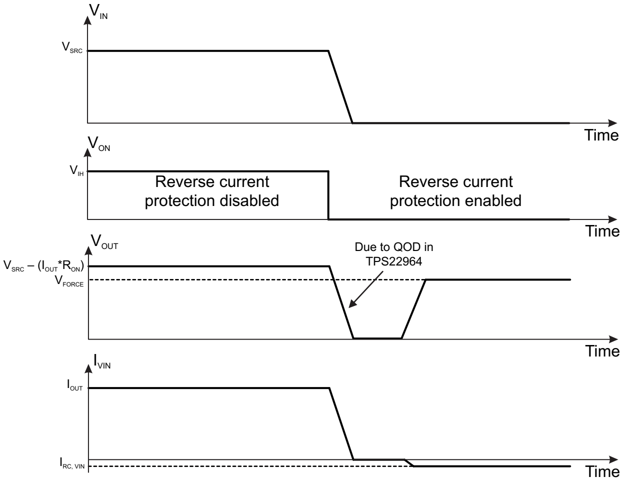
Figure 38. Standby Power Reduction

Any end equipment that is being powered from the battery has a need to reduce current consumption in order to keep the battery charged for a longer time. TPS22963/64 helps to accomplish this by turning off the supply to the modules that are in standby state and hence significantly reduces the leakage current overhead of the standby modules.

11.1.4 Reverse Current Protection

The reverse current protection feature prevents the current to flow from VOUT to VIN when TPS22963/64 is disabled. This feature is particularly useful when the output of TPS22963/64 needs to be driven by another voltage source after TPS22963/64 is disabled (for example in a power multiplexer application). In order for this feature to work, TPS22963/64 has to be disabled and either of the following conditions shall be met: V_{IN} > 1 V or V_{OUT} > 1 V.

Figure 39 demonstrates the ideal behavior of reverse current protection circuit in TPS22963/64. After the device is disabled via the ON pin and VOUT is forced to an external voltage V_{FORCE}, a very small amount of current given by $I_{RC,VIN}$ will flow from VOUT to VIN. This will prevent any extra current loading on the voltage source supplying the V_{FORCE} voltage.



I_{VIN} = Current through VIN pin.

V_{SRC} = Input voltage applied to the device.

V_{FORCE} = External voltage source forced at VOUT pin of the device.

I_{OUT} = Output load current.

Figure 39. Reverse Current Protection

Application Information (continued)

11.1.5 Power Supply Sequencing Without a GPIO Input

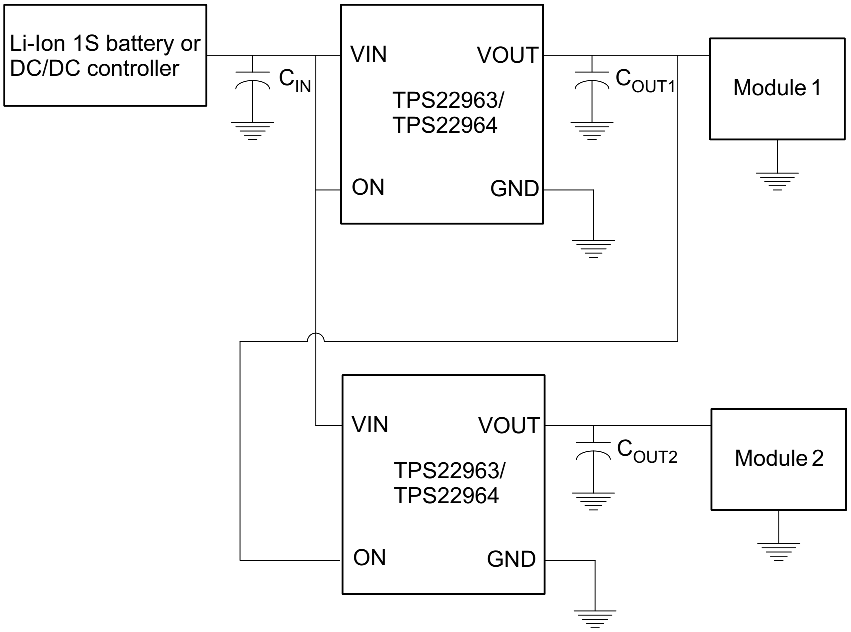


Figure 40. Power Supply Sequencing Without a GPIO Input

In many end equipments, there is a need to power up various modules in a pre-determined manner. TPS22963/64 can solve the problem of power sequencing without adding any complexity to the overall system. Figure 40 shows the configuration required for powering up two modules in a fixed sequence. The output of the first load switch is tied to the enable of the second load switch, so when Module 1 is powered the second load switch is enabled and Module 2 is powered.

11.2 Typical Application

TPS22963/64 is an ultra-low ON-resistance, 3-A integrated load switch that is capable of interfacing directly with 1S battery in portable consumer devices such as smartphones, tablets etc. Its wide input voltage range (1 V to 5.5 V) makes it suitable to be used for lower voltage rails as well inside different end equipments to accomplish power sequencing, inrush current control and reducing leakage current in sub-systems that are in standby mode. Figure 41 shows the typical application circuit of TPS22963/64.

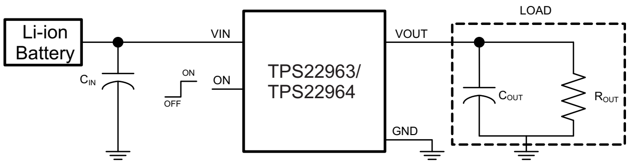


Figure 41. Typical Application Circuit

11.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
C_L	4.7 µF
Maximum Acceptable Inrush Current	30 mA

11.2.2 Detailed Design Procedure

11.2.2.1 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where

- C = output capacitance
- dV = output voltage
- dt = rise time (1)

The TPS22963/64 offers a controlled rise time for minimizing inrush current. This device can be selected based upon the minimum acceptable rise time which can be calculated using the design requirements and the inrush current equation. An output capacitance of 4.7 µF will be used since the amound of inrush current increases with output capacitance:

$$30\ \text{mA} = 4.7\ \mu\text{F} \times 3.3\ \text{V} / dt \quad (2)$$

$$dt = 517\ \mu\text{s} \quad (3)$$

To ensure an inrush current of less than 30 mA, a device with a rise time greater than 517 µs must be used. The TPS22963/64 has a typical rise time of 715 µs at 3.3 V which meets the above design requirements.

11.2.3 Application Curves

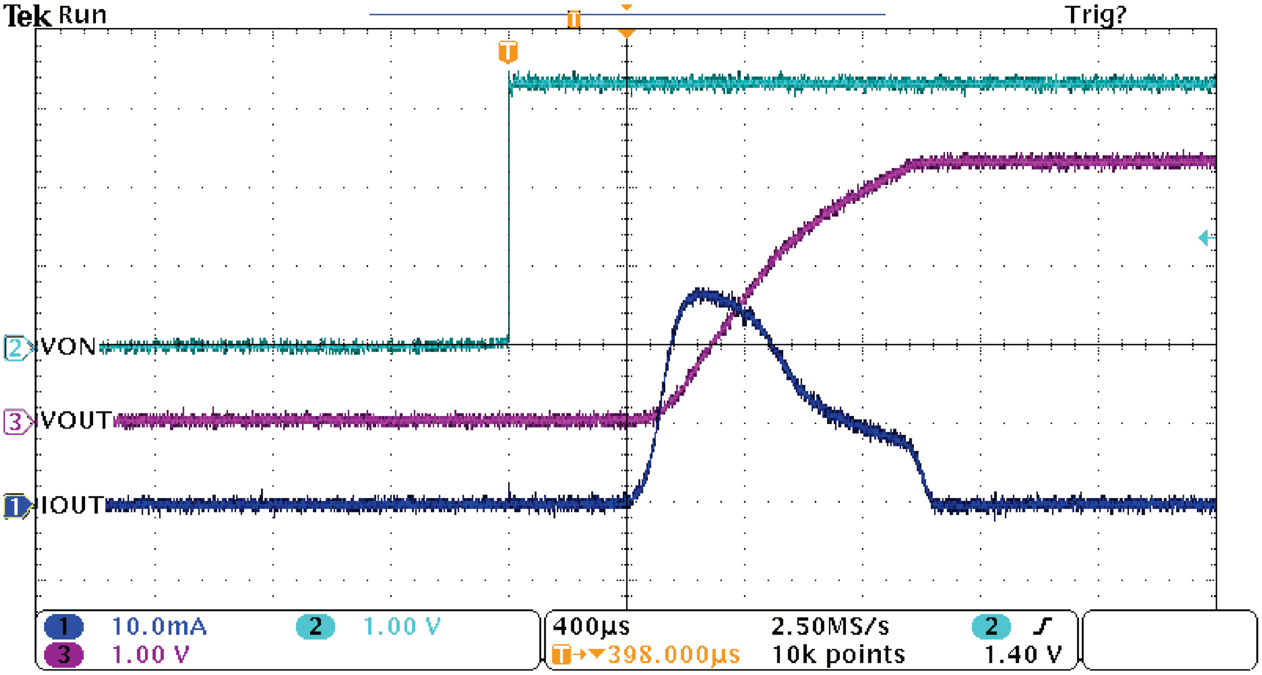


Figure 42. TPS22963/64 Inrush Current with 4.7 µF Output Capacitor

12 Power Supply Recommendations

The device is designed to operate with a VIN range of 1 V to 5.5 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1 µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient

13 Layout

13.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT and GND will help minimize the parasitic electrical effects.

For higher reliability, the maximum IC junction temperature, $T_{J(max)}$, should be restricted to 125˚C under normal operating conditions. Junction temperature is directly proportional to power dissipation in the device and the two are related by Equation 4.

$$T_J = T_A + \Theta_{JA} \times P_D \tag{4}$$

where

- T_J = Junction temperature of the device
- T_A = Ambient temperature
- P_D = Power dissipation inside the device
- Θ_{JA} = Junction to ambient thermal resistance. See Thermal Information section of the datasheet. This parameter is highly dependent on board layout.

13.2 Layout Example

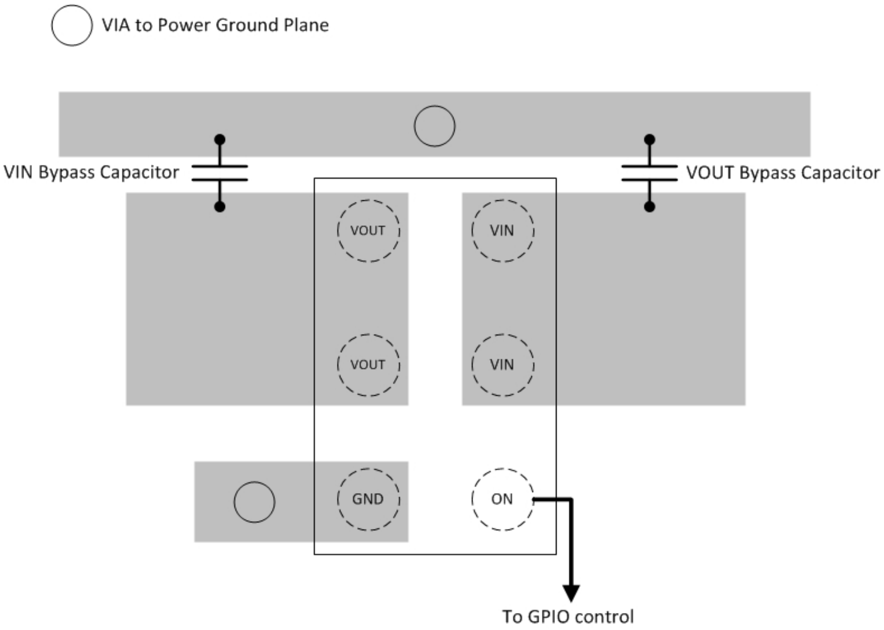


Figure 43. Layout Example

14 Device and Documentation Support

14.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS22963C	Click here	Click here	Click here	Click here	Click here
TPS22964C	Click here	Click here	Click here	Click here	Click here

14.2 Trademarks

Ultrabook is a trademark of Intel Corporation in the U.S. and/or other countries.
All other trademarks are the property of their respective owners.

14.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22963CYZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BD
TPS22963CYZPR.A	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BD
TPS22963CYZPT	Active	Production	DSBGA (YZP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BD
TPS22963CYZPT.A	Active	Production	DSBGA (YZP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BD
TPS22964C2YZPR	Active	Production	DSBGA (YZP) | 6	6000 | JUMBO T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DK
TPS22964C2YZPR.A	Active	Production	DSBGA (YZP) | 6	6000 | JUMBO T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DK
TPS22964CYZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DK
TPS22964CYZPR.A	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DK
TPS22964CYZPT	Active	Production	DSBGA (YZP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DK
TPS22964CYZPT.A	Active	Production	DSBGA (YZP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

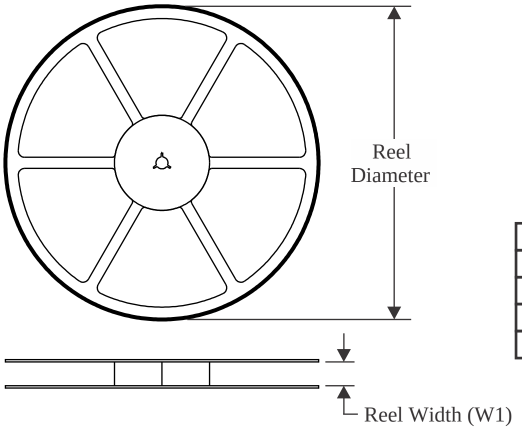
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

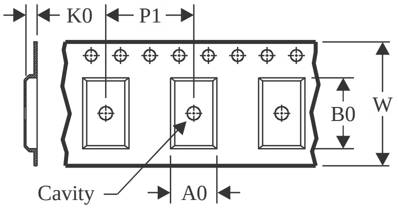
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

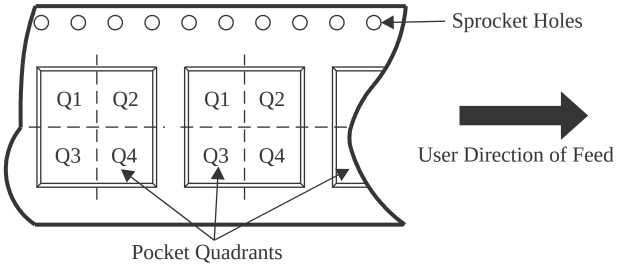


REEL DIMENSIONS



TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

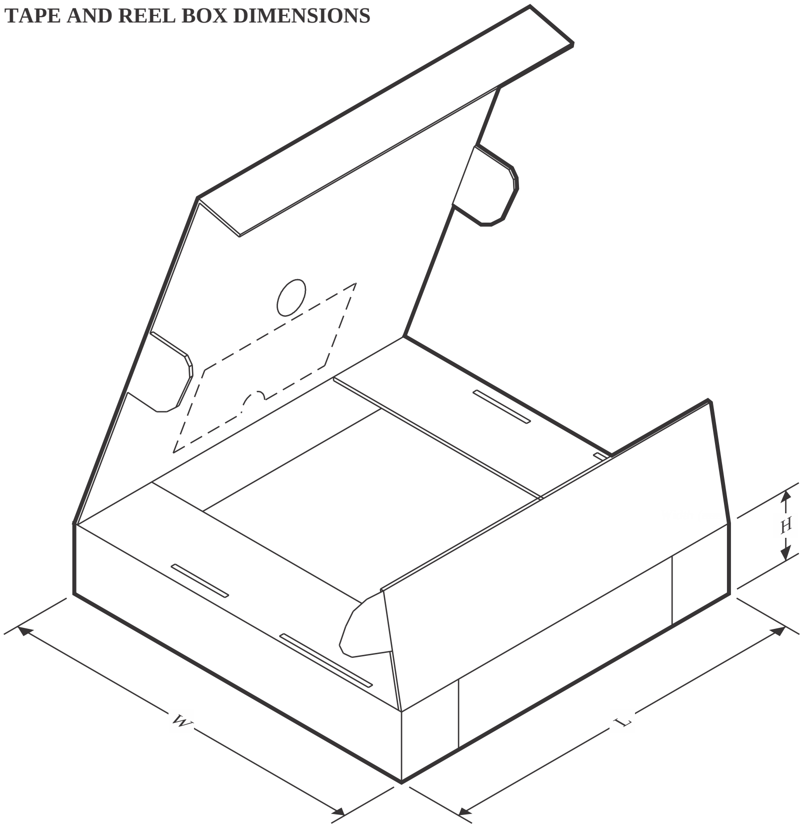


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22963CYZPR	DSBGA	YZP	6	3000	180.0	8.4	1.04	1.54	0.56	4.0	8.0	Q1
TPS22963CYZPT	DSBGA	YZP	6	250	180.0	8.4	1.04	1.54	0.56	4.0	8.0	Q1
TPS22964C2YZPR	DSBGA	YZP	6	6000	180.0	8.4	1.04	1.57	0.6	2.0	8.0	Q1
TPS22964CYZPR	DSBGA	YZP	6	3000	180.0	8.4	1.04	1.57	0.6	4.0	8.0	Q1
TPS22964CYZPR	DSBGA	YZP	6	3000	180.0	8.4	1.04	1.54	0.56	4.0	8.0	Q1
TPS22964CYZPT	DSBGA	YZP	6	250	180.0	8.4	1.04	1.54	0.56	4.0	8.0	Q1
TPS22964CYZPT	DSBGA	YZP	6	250	180.0	8.4	1.04	1.57	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

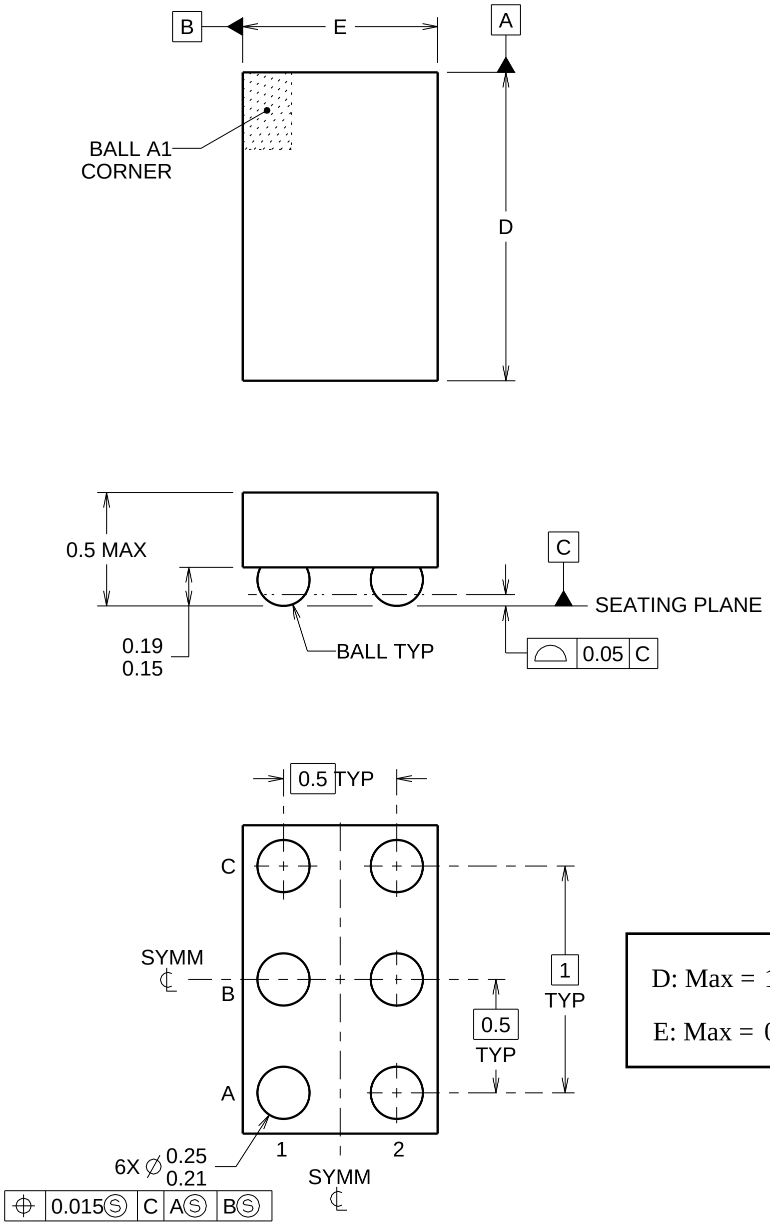
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22963CYZPR	DSBGA	YZP	6	3000	182.0	182.0	20.0
TPS22963CYZPT	DSBGA	YZP	6	250	182.0	182.0	20.0
TPS22964C2YZPR	DSBGA	YZP	6	6000	182.0	182.0	20.0
TPS22964CYZPR	DSBGA	YZP	6	3000	182.0	182.0	20.0
TPS22964CYZPR	DSBGA	YZP	6	3000	182.0	182.0	20.0
TPS22964CYZPT	DSBGA	YZP	6	250	182.0	182.0	20.0
TPS22964CYZPT	DSBGA	YZP	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.472 mm, Min =1.412 mm

E: Max = 0.972 mm, Min =0.912 mm

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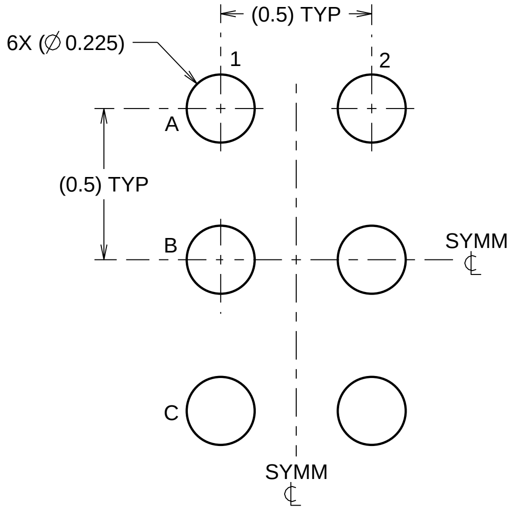
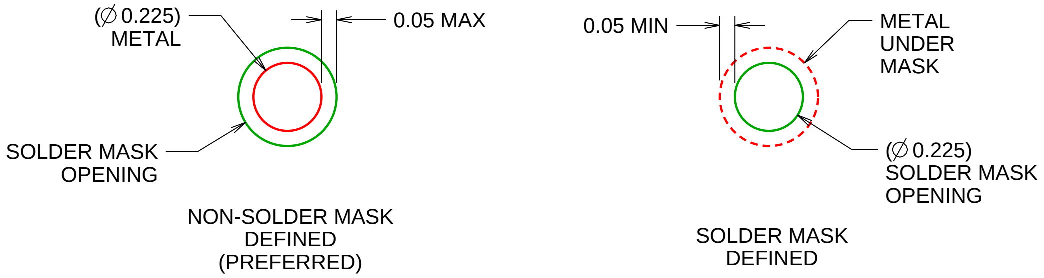
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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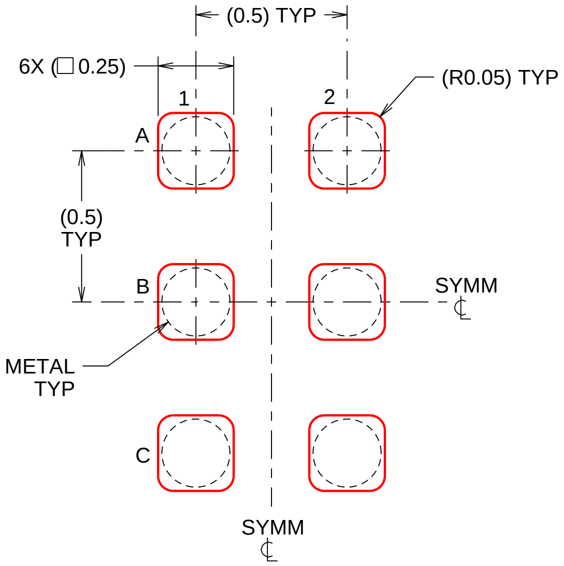
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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