TPS2295x-Q1 5.7-V, 5-A, 14-mΩ On-Resistance, Automotive Load Switch

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Integrated single channel load switch
- Input voltage range: 0.7 V to 5.7 V
- R_{ON} resistance
  - R_{ON} = 14 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
- 5-A maximum continuous switch current
- Adjustable Undervoltage Lockout Threshold (UVLO)
- Adjustable voltage supervisor with Power Good (PG) indicator
- Adjustable output slew rate control
- Enhanced quick output discharge remains active after power is removed (TPS22954-Q1 only)
  - 15 Ω (typ.) discharges 100 µF within 10 ms
- Reverse current blocking when disabled (TPS22953-Q1 only)
- Automatic restart after supervisor fault detection when enabled
- Thermal shutdown
- Low quiescent current ≤ 50 µA
- SON 10-pin package with thermal pad
- ESD performance tested per JESD 22
  - 2-kV HBM and 750-V CDM

2 Applications

- Infotainment and cluster head unit
- Automotive cluster display
- ADAS surround view system ECU
- Body control module and gateway

3 Description

The TPS2295x-Q1 are small, single channel load switches with controlled turn-on. The devices contain an N-channel MOSFET that can operate over an input voltage range of 0.7 V to 5.7 V and can support a maximum continuous current of 5 A.

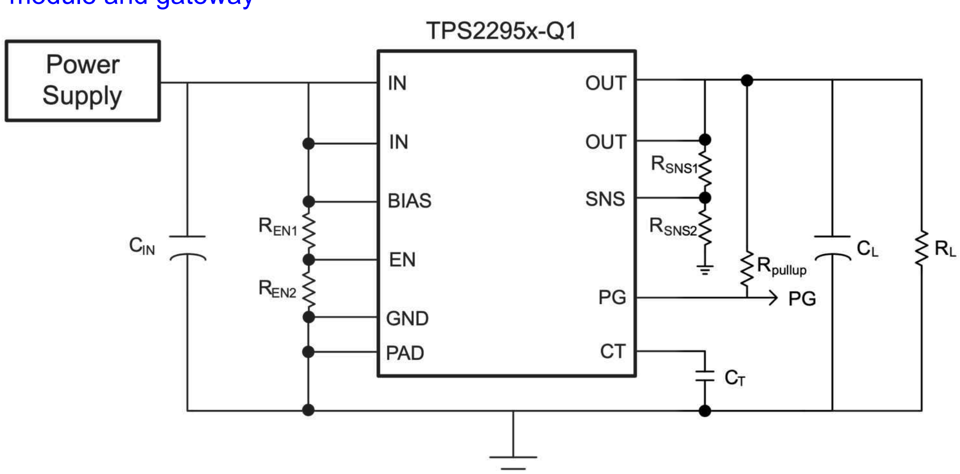
The integrated adjustable Undervoltage Lockout (UVLO) and adjustable Power Good (PG) threshold provides voltage monitoring as well as robust power sequencing. The adjustable rise-time control of the device greatly reduces inrush current for a wide variety of bulk load capacitances, thereby reducing or eliminating power supply droop. The switch is independently controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals. A 15-Ω on-chip load is integrated into the device for a quick discharge of the output when the switch is disabled. The enhanced Quick Output Discharge (QOD) remains active for a short time after power is removed from the device to finish discharging the output.

The TPS2295x-Q1 are available in small, space-saving 10-SON packages with integrated thermal pad, allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TPS2295x-Q1	WSON (10)	2.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (June 2022)	**Page**
• Changed status from "Advance Information" to "Production Data"	1

5 Device Comparison Table

Device	Quick Output Discharge	Reverse Current Blocking	Package (Pin)	Body Size	Pin Pitch
TPS22954-Q1	Yes	No	DQC (10)	2.00 mm × 3.00 mm	0.5 mm
TPS22953-Q1	No	Yes	DQC (10)	2.00 mm × 3.00 mm	0.5 mm

6 Pin Configuration and Functions

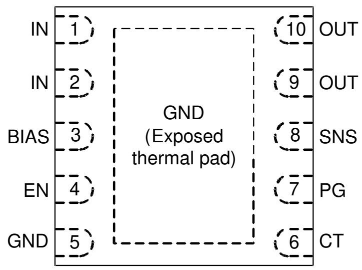


Figure 6-1. DQC/DSQ Package 10-Pin WSON Top View

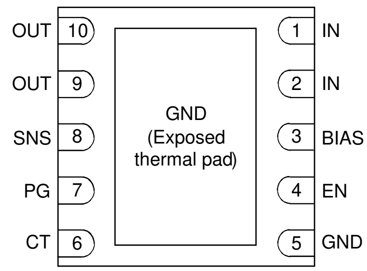


Figure 6-2. DQC/DSQ Package 10-Pin WSON Bottom View

Table 6-1. Pin Functions

PIN[(1)]		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input. Bypass this input with a ceramic capacitor to GND.
2			
3	BIAS	I	Bias pin and power supply to the device
4	EN	I	Active high switch to enable and disable the output. Also acts as the input UVLO pin. Use external resistor divider to adjust the UVLO level. Do not leave floating.
5	GND	—	Device ground
6	CT	O	V_{OUT} slew rate control. Place ceramic cap from CT to GND to change the V_{OUT} slew rate of the device and limit the inrush current. Rate the CT Capacitor to 25 V or higher.
7	PG	O	Power Good. This pin is open drain which pulls low when the voltage on EN or SNS is below their respective VIL levels.
8	SNS	I	Sense pin. Use external resistor divider to adjust the power good level. Do not leave floating.
9	OUT	O	Switch output
10			
—	Thermal Pad	—	Exposed thermal pad. Tie to GND.

(1) Pinout applies to all package versions.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{EN}, V_{SNS}, V_{PG}	EN, SNS, and PG voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current, T_A = 70°C		5	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		7	A
T_J	Maximum junction temperature	Internally Limited		
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100- 002[(1)] HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100- 011 CDM ESD classification level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	0.7	V_{BIAS}	V
V_{BIAS}	Bias voltage	2.5	5.7	V
V_{OUT}	Output voltage	0.9	5.7	V
V_{EN}, V_{SNS}, V_{PG}	EN, SNS, and PG voltage	0	5.7	V
TA	Operating free-air temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

7.3 Thermal Information

THERMAL METRIC [(1)]		TPS2295x-Q1	UNIT
		DQC (WSON)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.4 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and the recommended VBIAS voltage range of 2.5 V to 5.7 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{EN}	V_{IH}, Rising threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	650	700	750	mV
	V_{IL}, Falling threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	560	600	640	mV
V_{SNS}	V_{IH}, Rising threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	465	515	565	mV
	V_{IL}, Falling threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	410	455	500	mV
t_{BLANK}	Blanking time for EN and SNS	EN or SNS rising	–40°C to +125°C		100		µs
$t_{DEGLITCH}$	Deglitch time for EN and SNS	EN or SNS falling	–40°C to +125°C		5		µs
t_{DIS}	Output discharge time (TPS22954 only)	C_L = 100µF	–40°C to +125°C			10	ms
$t_{RESTART}$	Output restart time	SNS falling	–40°C to +125°C		2		ms
t_{RCB}	Response time for reverse current blocking (TPS22953 only)	V_{OUT} = V_{BIAS} EN falling	–40°C to +125°C		10		µs
T_{SD}	Thermal shutdown	Junction temperature rising	-	130	150	170	°C
TSD_{HYS}	Thermal shutdown hysteresis	Junction temperature falling	-		20		°C
$I_{RCB,IN}$	Input reverse blocking current (TPS22953 only)	V_{OUT} = 5V, V_{IN} = V_{EN} = 0V, V_{BIAS} = 0V to 5.7V	25°C		0.01	2	mΩ
			–40°C to +85°C			5	mΩ
			–40°C to +125°C			11	mΩ

7.5 Electrical Characteristics – VBIAS = 5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, BIAS}$	BIAS quiescent current	I_{OUT} = 0, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 5 V		–40°C to +85°C		34	45	µA
				–40°C to +125°C			50	
$I_{SD,BIAS}$	BIAS shutdown current	V_{OUT} = 0 V, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 0 V to V_{IL}		–40°C to +85°C		5	7	µA
				–40°C to +125°C			8	
$I_{SD, IN}$	Input shutdown current	V_{EN} = 0 V to V_{IL}, V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +85°C		0.02	4	µA
				–40°C to +125°C			13	
			V_{IN} = 3.3 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.8 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.2 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
			V_{IN} = 0.7 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
I_{EN}	EN pin leakage current	V_{EN} = 0 V to 5.7 V		–40°C to +125°C			0.1	µA
I_{SNS}	SNS pin leakage current	VSNS ≤ V_{BIAS}		–40°C to +125°C			0.1	µA

7.5 Electrical Characteristics – VBIAS = 5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} = 5 V	25°C		14	20	mΩ
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 3.3 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.8 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.5 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.2 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 0.7 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
R_{PD}	Output pull down resistance (TPS22954 only)	V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0 V		25°C		15	28	Ω
				–40°C to +125°C			30	Ω

7.6 Electrical Characteristics – VBIAS = 3.3 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 3.3 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, BIAS}$	BIAS quiescent current	I_{OUT} = 0, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 3.3 V		–40°C to +85°C		19	35	µA
				–40°C to +125°C			37	
$I_{SD,BIAS}$	BIAS shutdown current	V_{OUT} = 0 V, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 0 V to V_{IL}		–40°C to +85°C		4	6	µA
				–40°C to +125°C			7	
$I_{SD, IN}$	Input shutdown current	V_{EN} = 0 V to V_{IL}, V_{OUT} = 0 V	V_{IN} = 3.3 V	–40°C to +85°C		0.01	3	µA
				–40°C to +125°C			10	
			V_{IN} = 1.8 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.2 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
			V_{IN} = 0.7 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
I_{EN}	EN pin leakage current	V_{EN} = 0 V to 5.7 V		–40°C to +125°C			0.1	µA
I_{SNS}	SNS pin leakage current	VSNS ≤ V_{BIAS}		–40°C to +125°C			0.1	µA

7.6 Electrical Characteristics – VBIAS = 3.3 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 3.3 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} = 3.3 V	25°C		15	21	mΩ
				–40°C to +85°C			24	
				–40°C to +125°C			25	
			V_{IN} = 1.8 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.5 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.2 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 0.7 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
R_{PD}	Output pull down resistance (TPS22954 only)	$V_{IN} = V_{OUT} = V_{BIAS}$, V_{EN} = 0 V		25°C		13	28	Ω
				–40°C to +125°C			30	Ω

7.7 Electrical Characteristics – VBIAS = 2.5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 2.5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q,\ BIAS}$	BIAS quiescent current	I_{OUT} = 0, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 2.5 V		–40°C to +85°C		16	25	µA
				–40°C to +125°C			27	
$I_{SD,BIAS}$	BIAS shutdown current	V_{OUT} = 0 V, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 0 V to V_{IL}		–40°C to +85°C		4	5	µA
				–40°C to +125°C			6	
$I_{SD,\ IN}$	Input shutdown current	V_{EN} = 0 V to V_{IL}, V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +85°C		0.01	3	µA
				–40°C to +125°C			10	
			V_{IN} = 1.8 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.2 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
			V_{IN} = 0.7 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
I_{EN}	EN pin leakage current	V_{EN} = 0 V to 5.7V		–40°C to +125°C			0.1	µA
I_{SNS}	SNS pin leakage current	VSNS ≤ V_{BIAS}		–40°C to +125°C			0.1	µA

7.7 Electrical Characteristics – VBIAS = 2.5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 2.5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} = 2.5 V	25°C		16	23	mΩ
				–40°C to +85°C			26	
				–40°C to +125°C			27	
			V_{IN} = 1.8 V	25°C		15	22	
				–40°C to +85°C			25	
				–40°C to +125°C			26	
			V_{IN} = 1.5 V	25°C		15	22	
				–40°C to +85°C			25	
				–40°C to +125°C			26	
			V_{IN} = 1.2 V	25°C		15	22	
				–40°C to +85°C			24	
				–40°C to +125°C			25	
			V_{IN} = 0.7 V	25°C		14	21	
				–40°C to +85°C			24	
				–40°C to +125°C			25	
R_{PD}	Output pull down resistance (TPS22954 only)	V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0 V		25°C		12	28	Ω
				–40°C to +125°C			30	Ω

7.8 Switching Characteristics – CT = 1000 pF

All typical values are at 25°C unless otherwise noted

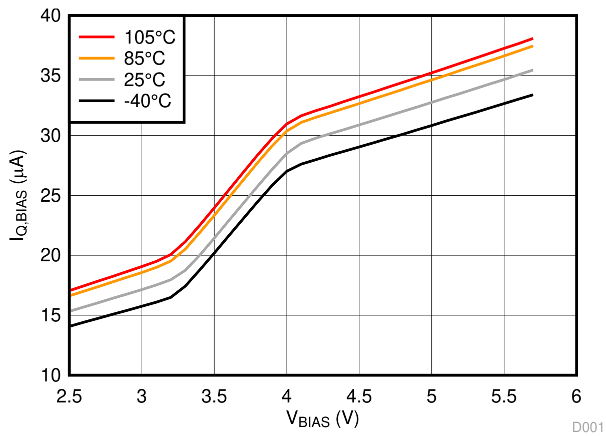
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 5 V, V_{EN} = V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1265		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1492		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		519		µs
V_{IN} = 2.5 V, V_{EN} = V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		813		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6.1		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		765		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		430		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		476		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6.2		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		245		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		353		µs
V_{IN} = 2.5 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		813		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		4.9		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		765		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		430		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		476		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6.1		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		245		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		353		µs

7.9 Switching Characteristics – CT = 0 pF

All typical values are at 25°C unless otherwise noted

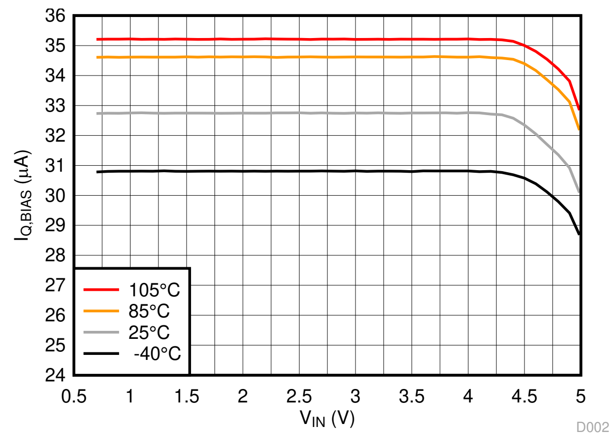
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 5 V, V_{EN} = V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		235		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		140		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		165		µs
V_{IN} = 2.5 V, V_{EN} = V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		200		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		79		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		160		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		170		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		32		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		154		µs
V_{IN} = 2.5 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		200		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		79		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		160		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		170		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		32		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		154		µs

7.10 Typical DC Characteristics



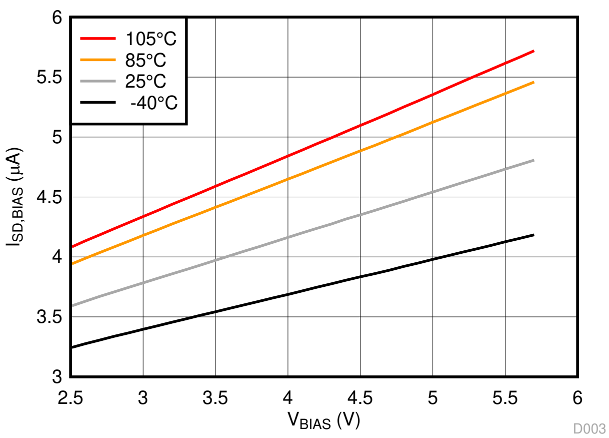
V_{IN} = 1.8 V V_{EN} = 5.7 V V_{OUT} = 0 V

Figure 7-1. $I_{Q,BIAS}$ vs V_{BIAS}



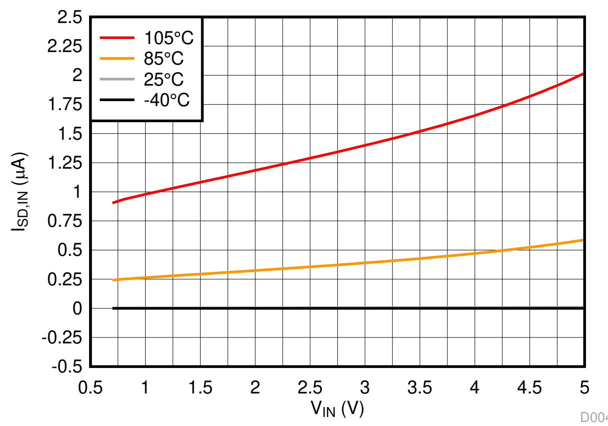
V_{BIAS} = 5 V V_{EN} = 5.7 V V_{OUT} = 0 V

Figure 7-2. $I_{Q,BIAS}$ vs V_{IN}



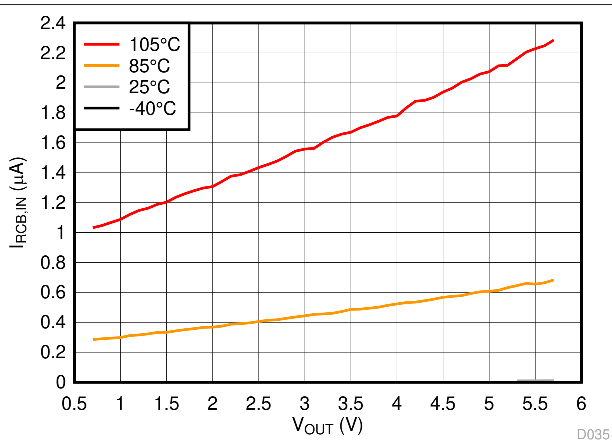
V_{IN} = 1.8 V V_{EN} = 0 V V_{OUT} = 0 V

Figure 7-3. $I_{SD,BIAS}$ vs V_{BIAS}



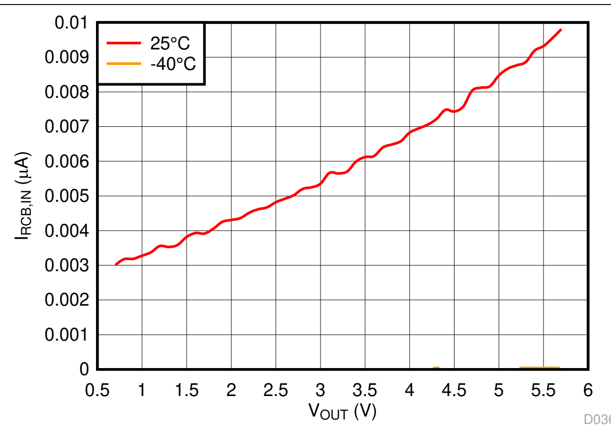
V_{BIAS} = 5 V V_{EN} = 0 V V_{OUT} = 0 V

Figure 7-4. $I_{SD,IN}$ vs V_{IN}



V_{BIAS} = 0 V to 5.7 V V_{EN} = 0 V V_{IN} = 0 V

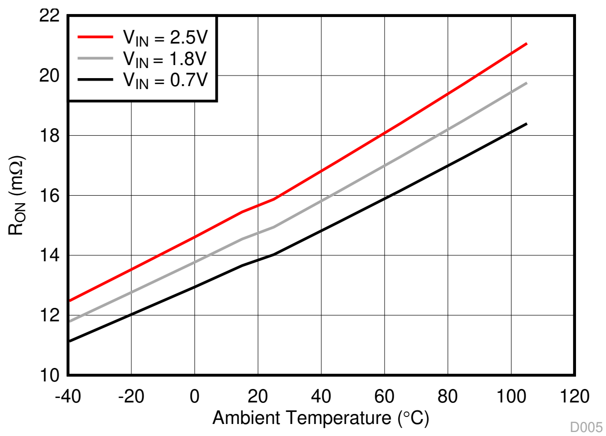
Figure 7-5. $I_{RCB,IN}$ vs V_{OUT}



V_{BIAS} = 0 V to 5.7 V V_{EN} = 0 V V_{IN} = 0 V

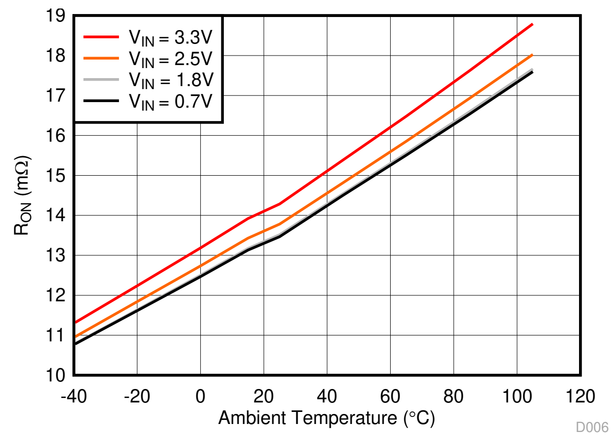
Figure 7-6. $I_{RCB,IN}$ vs V_{OUT}

7.10 Typical DC Characteristics (continued)



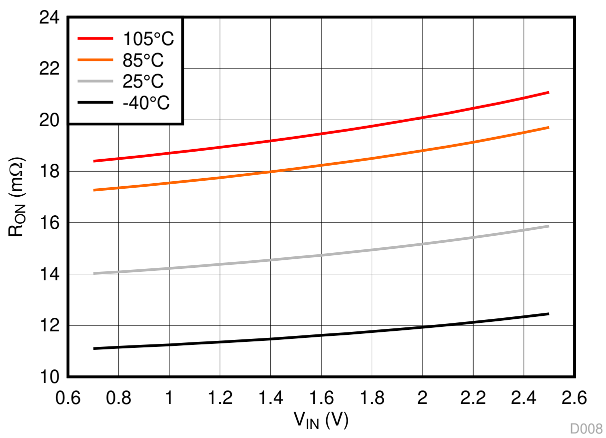
V_{BIAS} = 2.5 V Iout = –200 mA V_{EN} = 5 V

Figure 7-7. R_{ON} vs Temperature, V_{BIAS} = 2.5 V



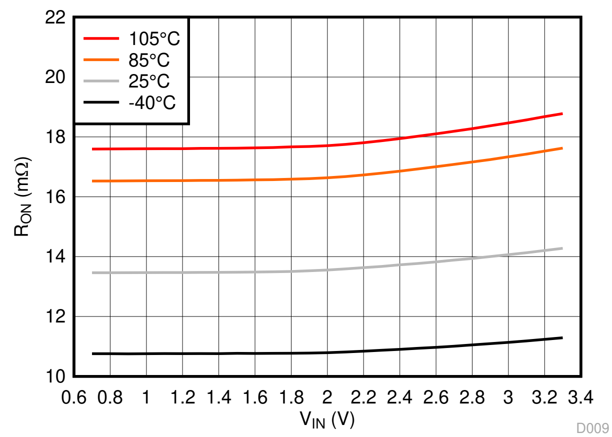
V_{BIAS} = 3.3 V Iout = –200 mA V_{EN} = 5 V

Figure 7-8. R_{ON} vs Temperature, V_{BIAS} = 3.3 V



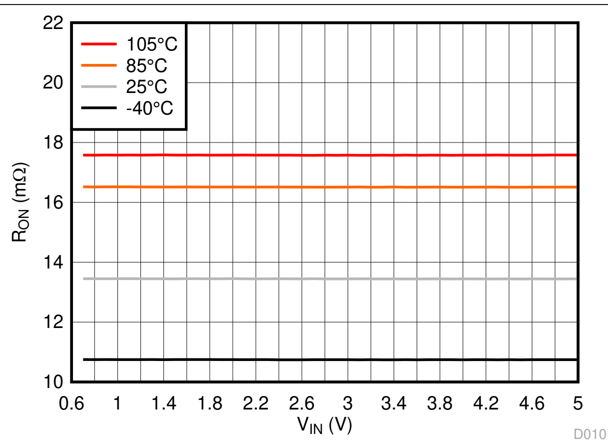
V_{BIAS} = 2.5 V Iout = –200 mA V_{EN} = 5 V

Figure 7-9. R_{ON} vs V_{IN}, V_{BIAS} = 2.5 V



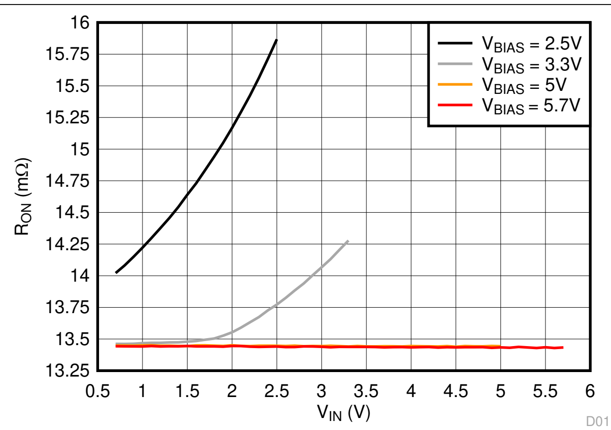
V_{BIAS} = 3.3 V Iout = –200 mA V_{EN} = 5 V

Figure 7-10. R_{ON} vs V_{IN}, V_{BIAS} = 3.3 V



V_{BIAS} = 5 V Iout = –200 mA V_{EN} = 5 V

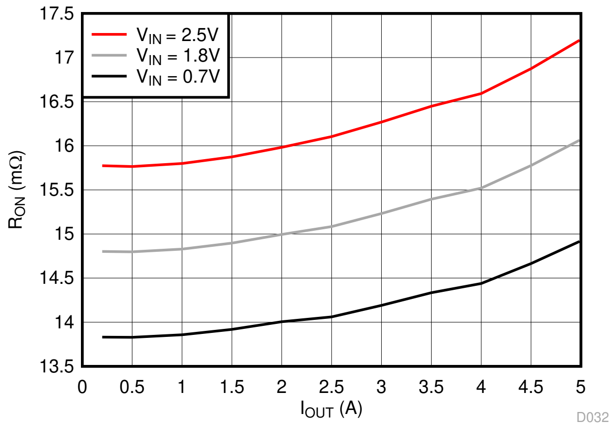
Figure 7-11. R_{ON} vs V_{IN}, V_{BIAS} = 5 V



T_A = 25°C Iout = –200 mA V_{EN} = 5 V

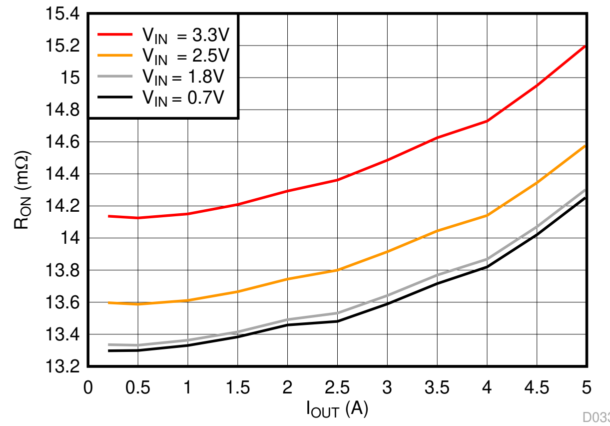
Figure 7-12. R_{ON} vs V_{IN}

7.10 Typical DC Characteristics (continued)



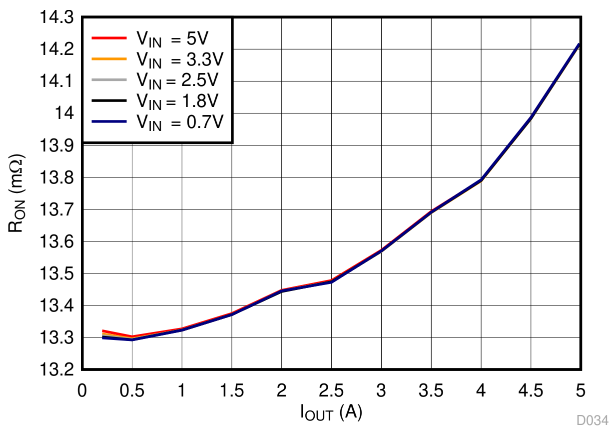
V_{BIAS} = 2.5 V V_{EN} = 5 V

Figure 7-13. R_{ON} vs I_{OUT}, V_{BIAS} = 2.5 V



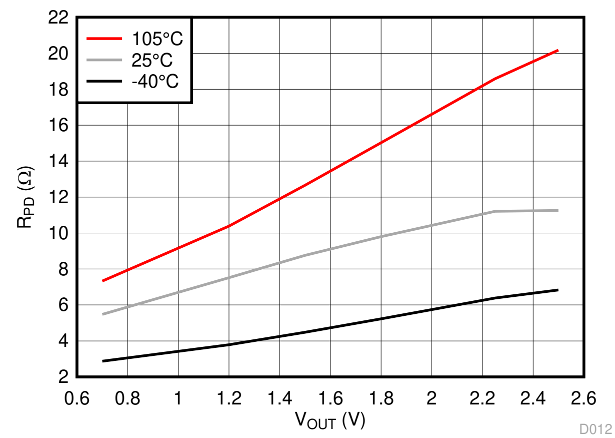
V_{BIAS} = 3.3 V V_{EN} = 5 V

Figure 7-14. R_{ON} vs I_{OUT}, V_{BIAS} = 3.3 V



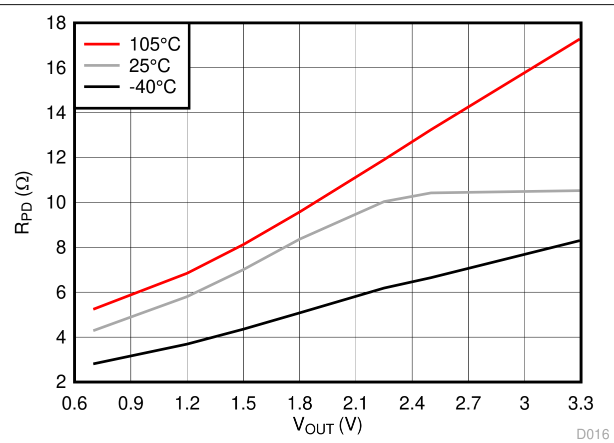
V_{BIAS} = 5 V V_{EN} = 5 V

Figure 7-15. R_{ON} vs I_{OUT}, V_{BIAS} = 5 V



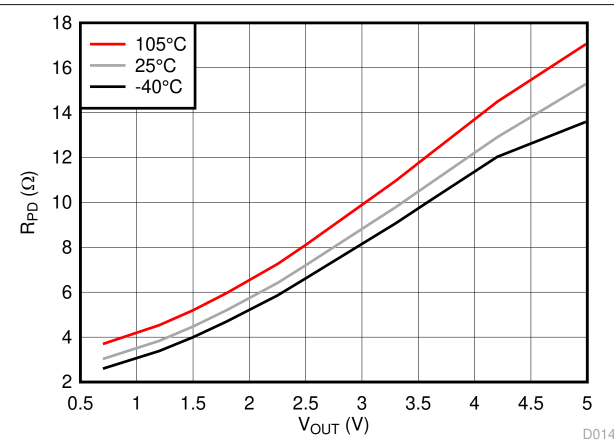
V_{BIAS} = 2.5 V V_{IN} = V_{OUT} V_{EN} = 0 V

Figure 7-16. R_{PD} vs V_{OUT}, V_{BIAS} = 2.5 V



V_{BIAS} = 3.3 V V_{IN} = V_{OUT} V_{EN} = 0 V

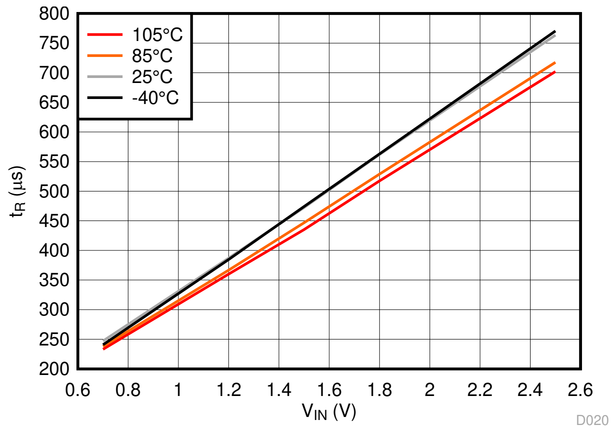
Figure 7-17. R_{PD} vs V_{OUT}, V_{BIAS} = 3.3 V



V_{BIAS} = 5 V V_{IN} = V_{OUT} V_{EN} = 0 V

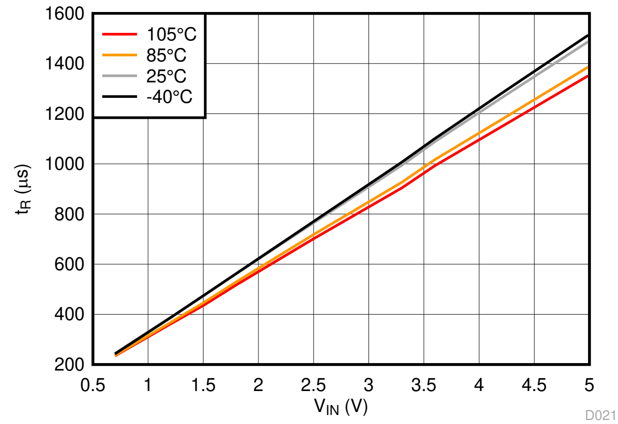
Figure 7-18. R_{PD} vs V_{OUT}, V_{BIAS} = 5 V

7.11 Typical Switching Characteristics



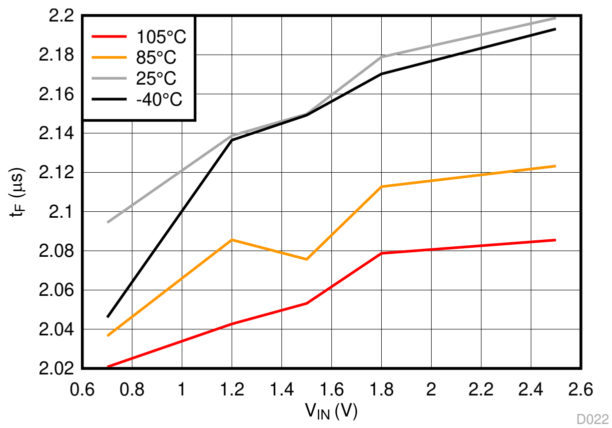
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = Low to High

Figure 7-19. t_R vs V_{IN}, V_{BIAS} = 2.5 V



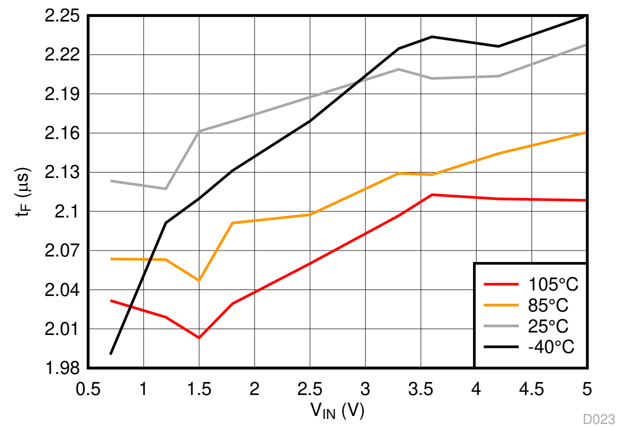
V_{BIAS} = 5 V CT = 1000 pF V_{EN} = Low to High

Figure 7-20. t_R vs V_{IN}, V_{BIAS} = 5 V



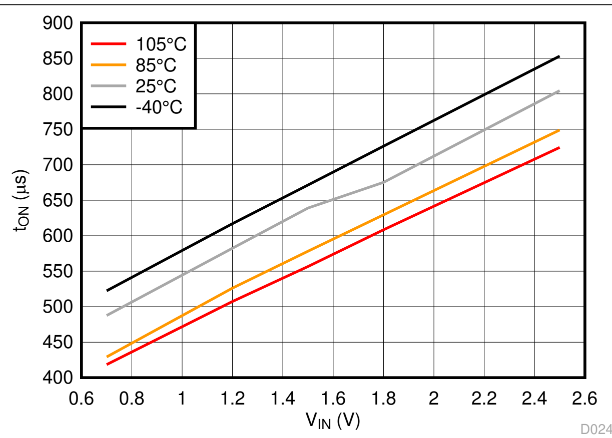
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-21. t_F vs V_{IN}, V_{BIAS} = 2.5 V



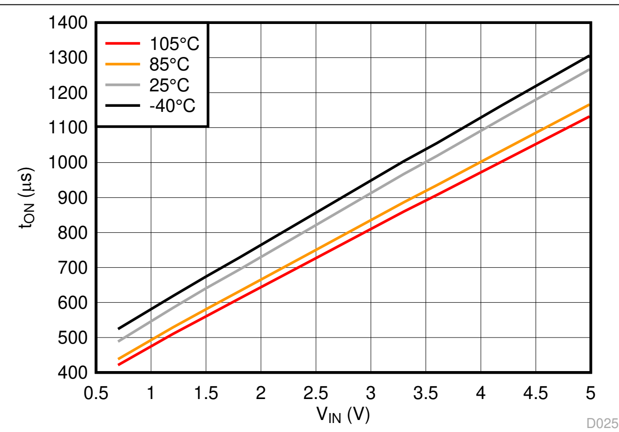
V_{BIAS} = 5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-22. t_F vs V_{IN}, V_{BIAS} = 5 V



V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = Low to High

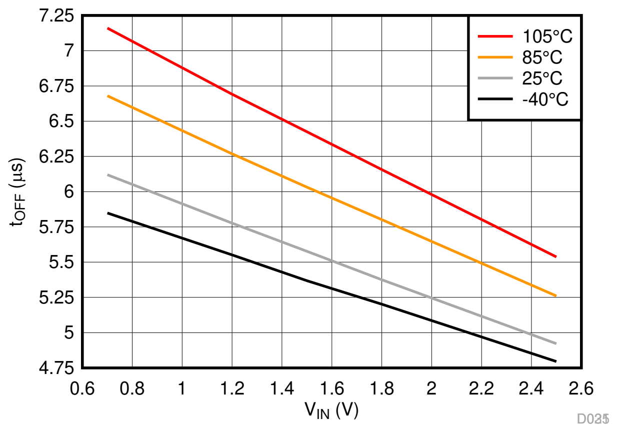
Figure 7-23. t_{ON} vs V_{IN}, V_{BIAS} = 2.5 V



V_{BIAS} = 5 V CT = 1000 pF V_{EN} = Low to High

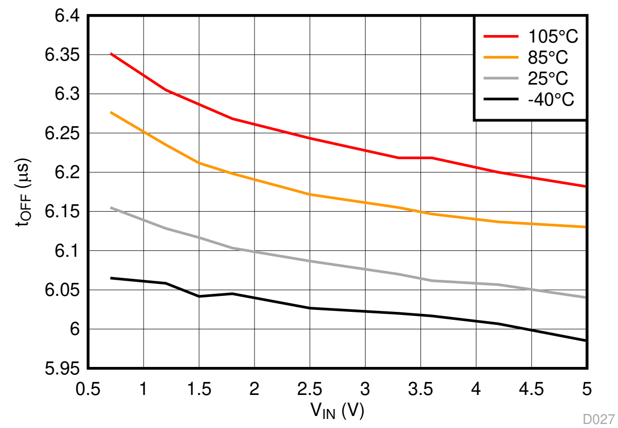
Figure 7-24. t_{ON} vs V_{IN}, V_{BIAS} = 5 V

7.11 Typical Switching Characteristics



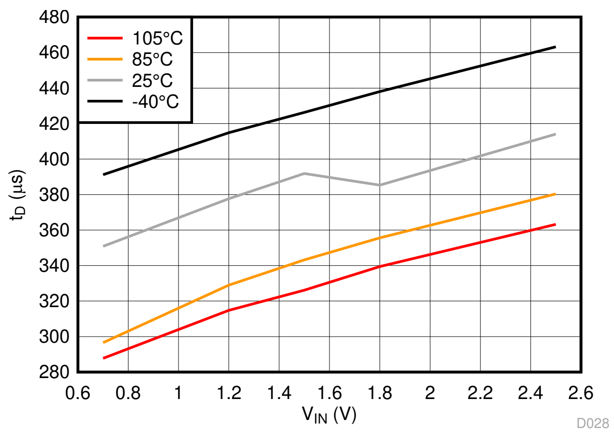
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-25. t_{OFF} vs V_{IN}, V_{BIAS} = 2.5 V



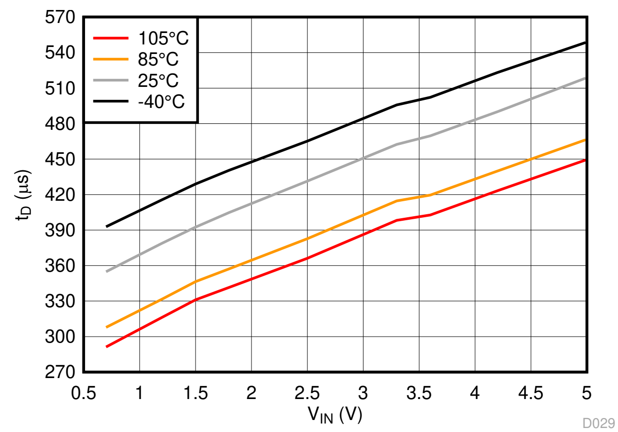
V_{BIAS} = 5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-26. t_{OFF} vs V_{IN}, V_{BIAS} = 5 V



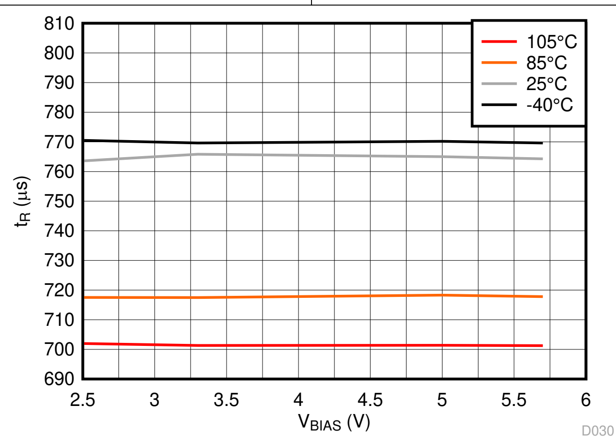
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = Low to High

Figure 7-27. t_D vs V_{IN}, V_{BIAS} = 2.5 V



V_{BIAS} = 5 V CT = 1000 pF V_{EN} =Low to High

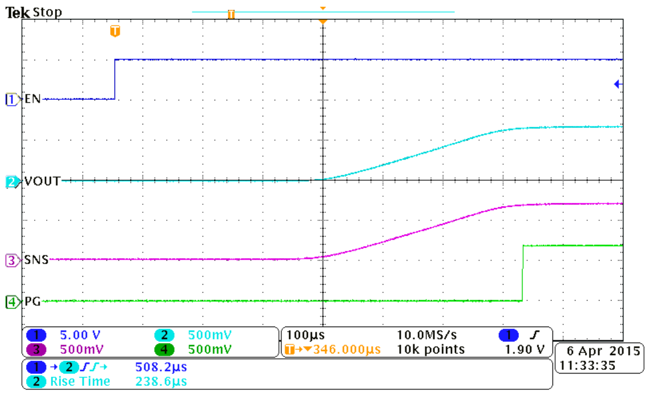
Figure 7-28. t_D vs V_{IN}, V_{BIAS}= 5 V



V_{IN} = 2.5 V CT = 1000 pF V_{EN} = Low to High

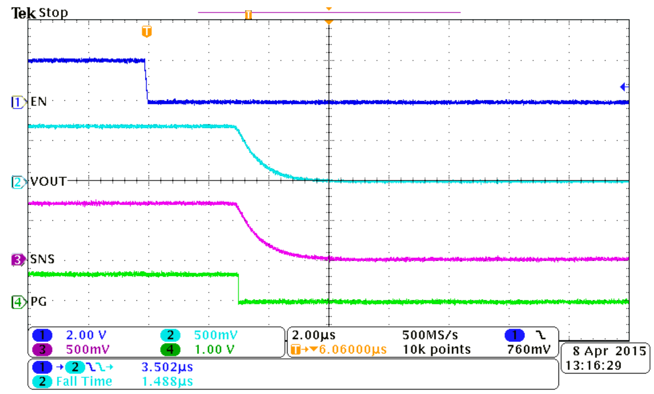
Figure 7-29. t_R vs V_{BIAS}

7.11 Typical Switching Characteristics (continued)



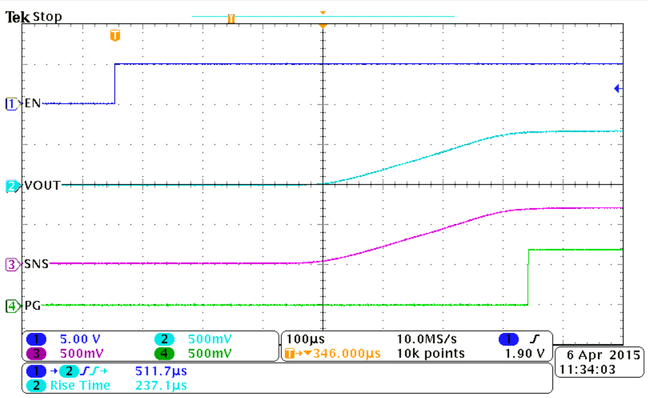
V_{IN} = 0.7 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-30. Turn-on Waveform, V_{BIAS} = 2.5 V



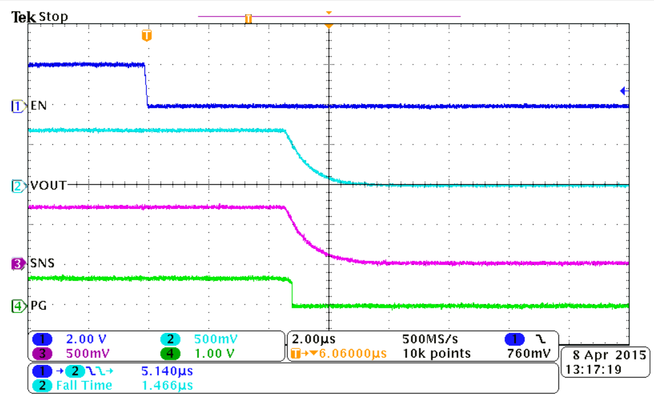
V_{IN} = 0.7 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-31. Turn-off Waveform, V_{BIAS} = 2.5 V



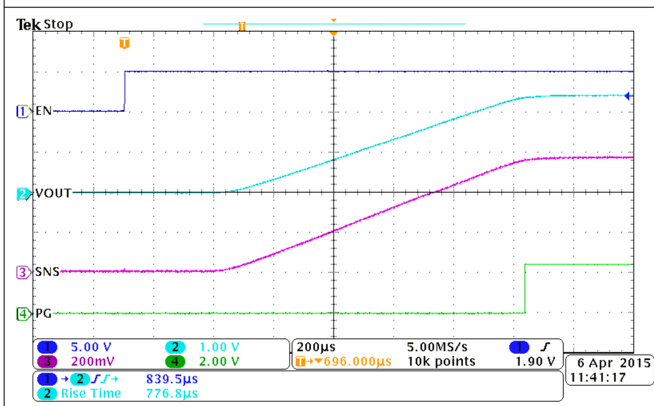
V_{IN} = 0.7 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-32. Turn-on Waveform, V_{BIAS} = 5 V



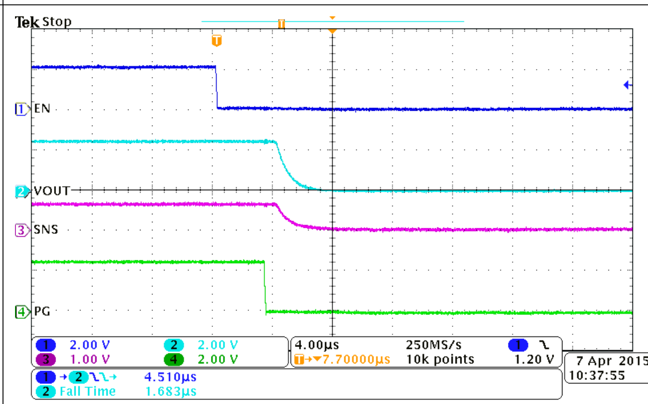
V_{IN} = 0.7 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-33. Turn-off Waveform, V_{BIAS} = 5 V



V_{IN} = 2.5 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

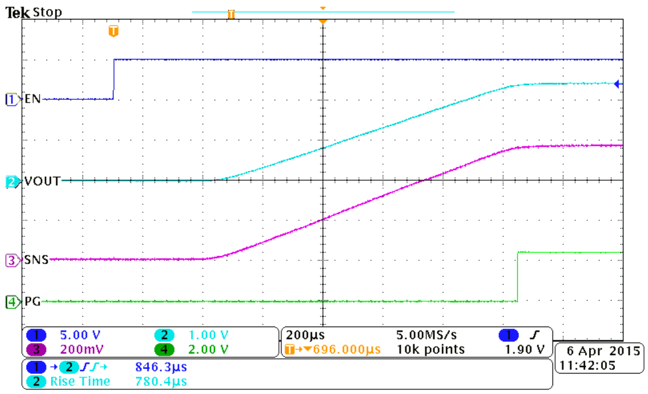
Figure 7-34. Turn-on Waveform, V_{BIAS} = 2.5 V



V_{IN} = 2.5 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

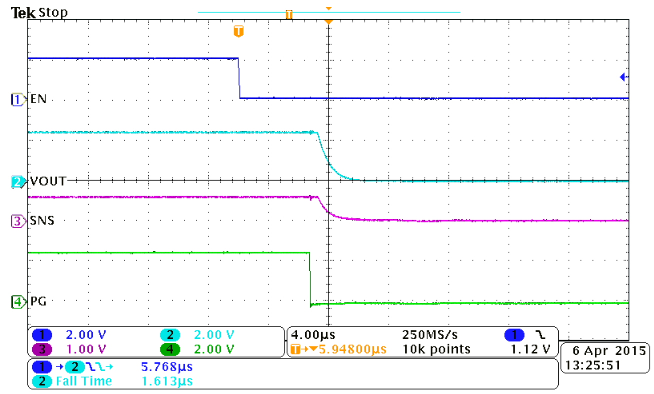
Figure 7-35. Turn-off Waveform, V_{BIAS} = 2.5 V

7.11 Typical Switching Characteristics (continued)



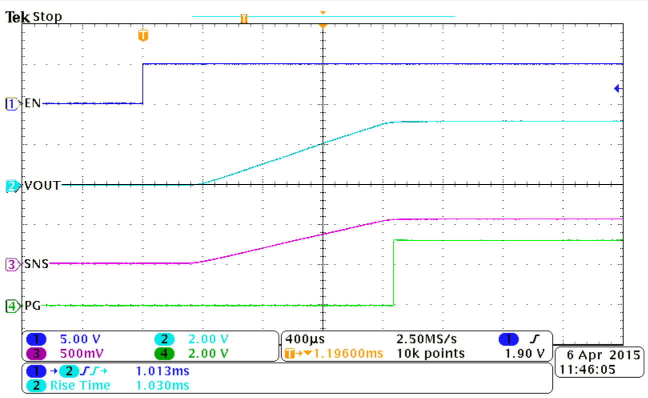
V_{IN} = 2.5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-36. Turn-on Waveform, V_{BIAS} = 5 V



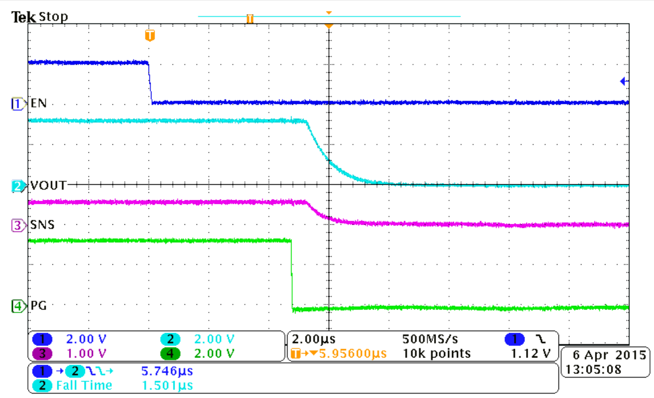
V_{IN} = 2.5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-37. Turn-off Waveform, V_{BIAS} = 5 V



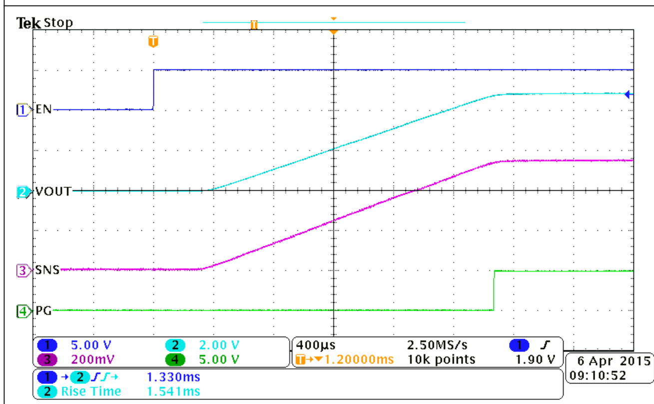
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-38. Turn-on Waveform, V_{BIAS} = 5 V



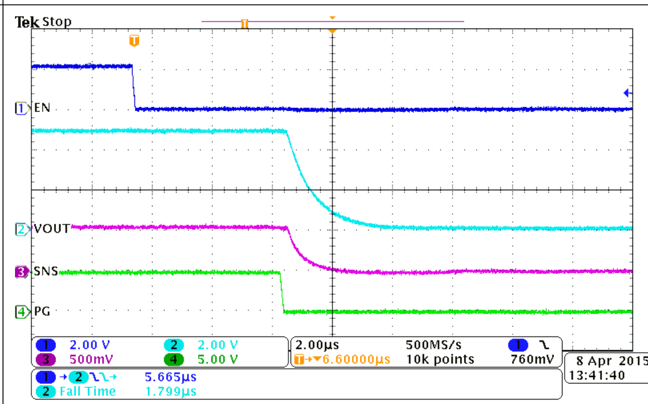
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-39. Turn-off Waveform, V_{BIAS} = 5 V



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

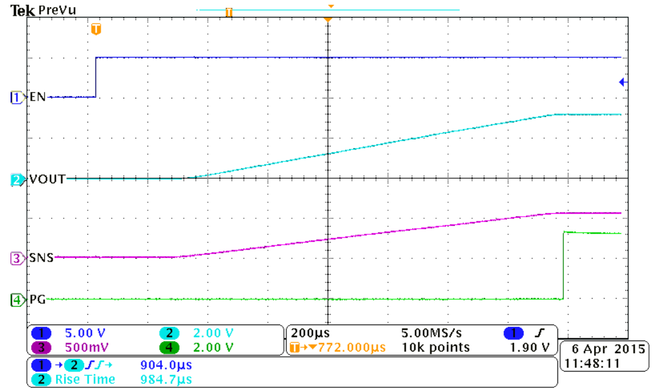
Figure 7-40. Turn-on Waveform, V_{BIAS} = 5 V



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

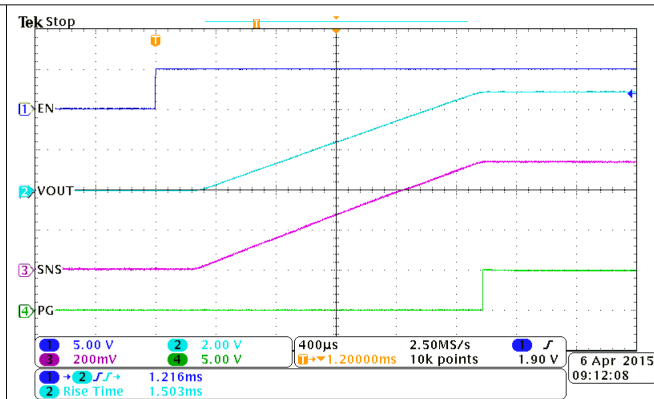
Figure 7-41. Turn-off Waveform, V_{BIAS} = 5 V

7.11 Typical Switching Characteristics (continued)



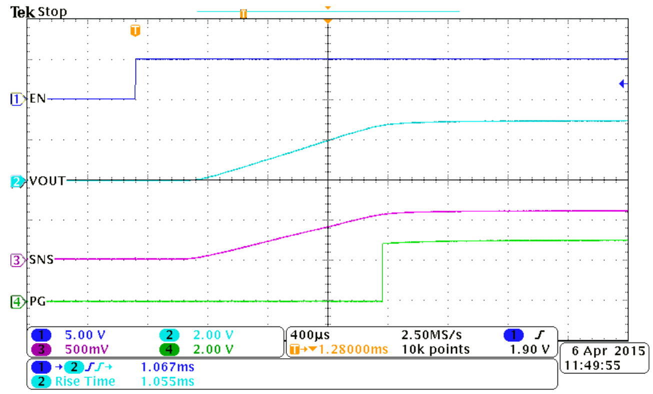
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = Open

Figure 7-42. Turn-on Waveform, No Load



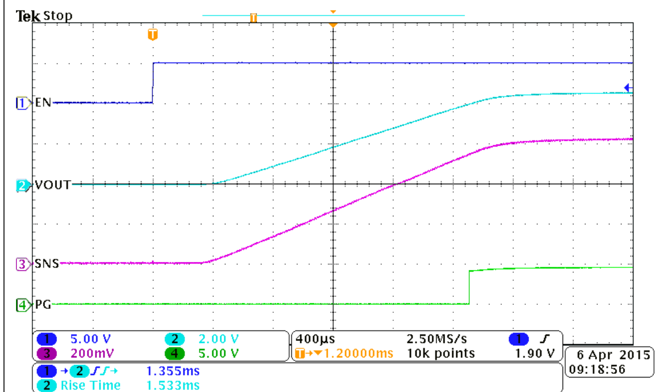
V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = Open

Figure 7-43. Turn-on Waveform, No Load



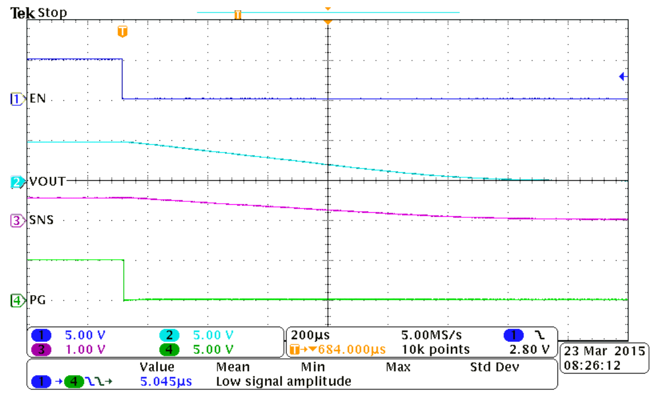
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 1 Ω

Figure 7-44. Turn-on Waveform, Heavy Load



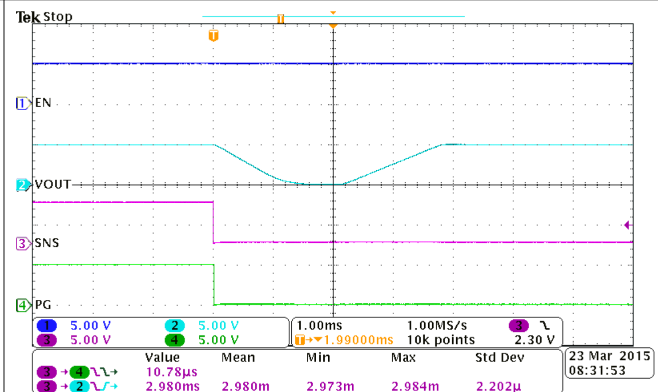
V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 1 Ω

Figure 7-45. Turn-on Waveform, Heavy Load



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = 10 Ω

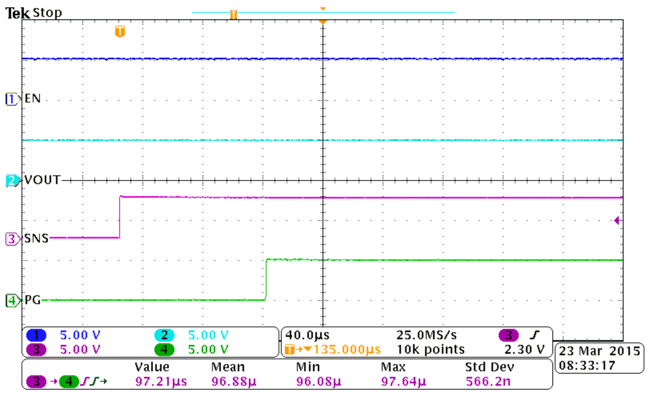
Figure 7-46. PG Response to EN Falling ($t_{DEGLITCH}$)



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = 10 Ω

Figure 7-47. PG Response to SNS Falling With Auto-Restart ($t_{DEGLITCH}$ and $t_{RESTART}$)

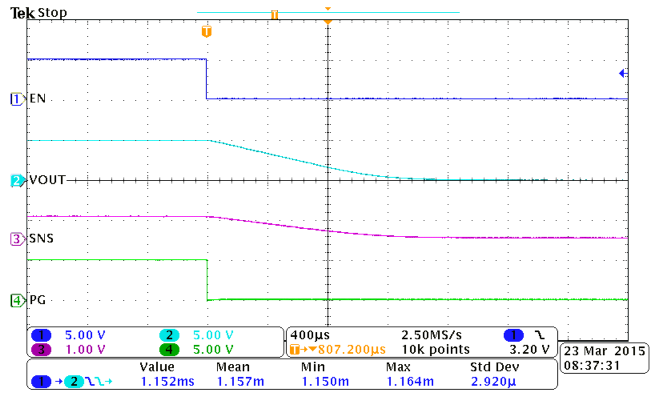
7.11 Typical Switching Characteristics (continued)



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF

C_{IN} = 1 µF C_L = 100 µF R_L = 10 Ω

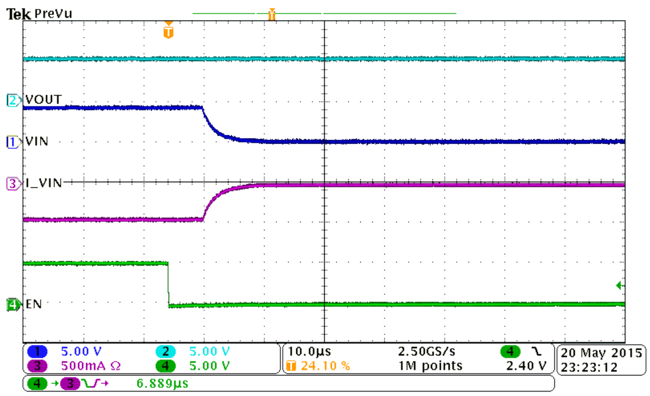
Figure 7-48. PG Response to SNS Rising (t_{BLANK})



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF

C_{IN} = 1 µF C_L = 100 µF R_L = None

Figure 7-49. Quick Output Discharge of 100-µF Load (t_{DIS})

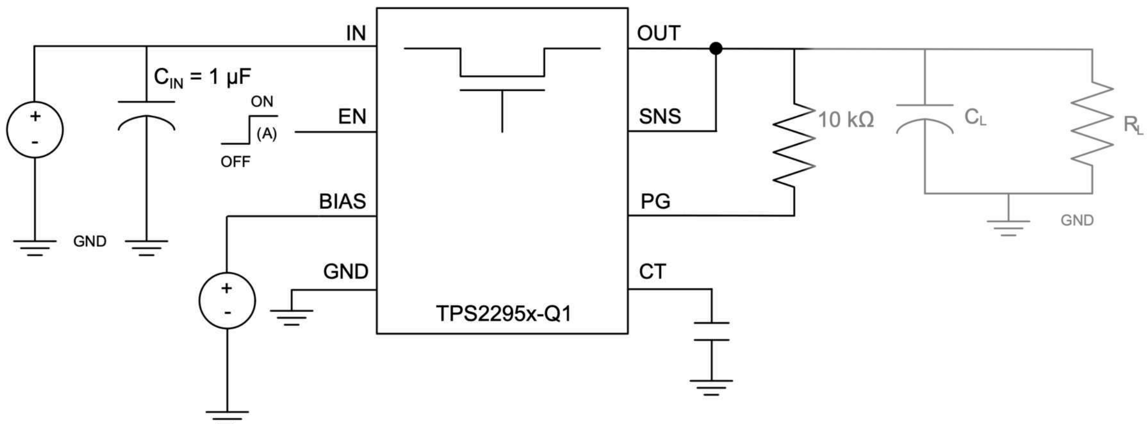


V_{IN} = 10 Ω to GND V_{BIAS} = 5 V

C_{IN} = 0.2 µF V_{OUT} = 5 V

Figure 7-50. Reverse Current Blocking Response Time (t_{RCB})

8 Parameter Measurement Information



A. Rise and fall times of the control signal is 100 ns.

Figure 8-1. Timing Test Circuit

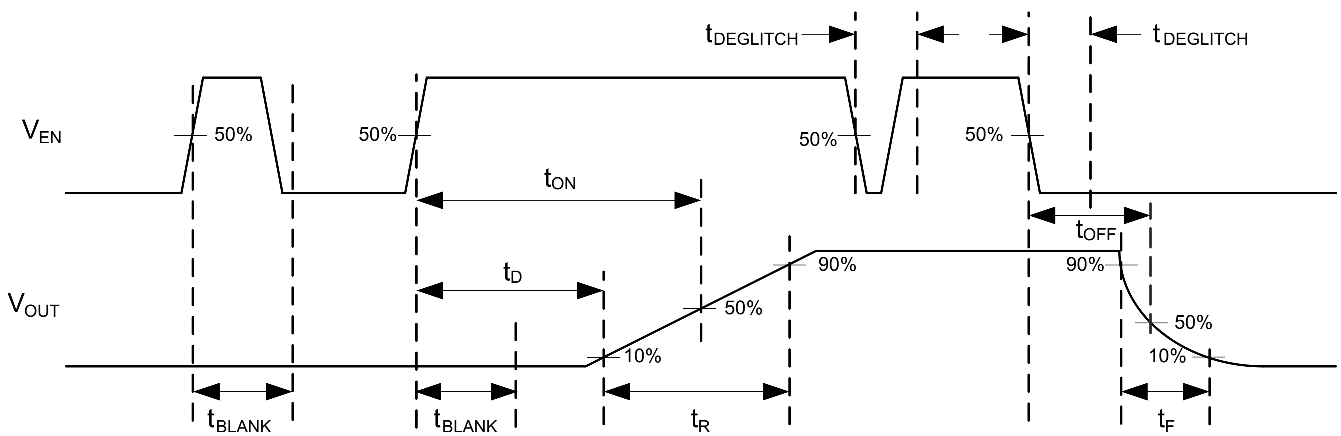


Figure 8-2. Timing Waveforms

9 Detailed Description

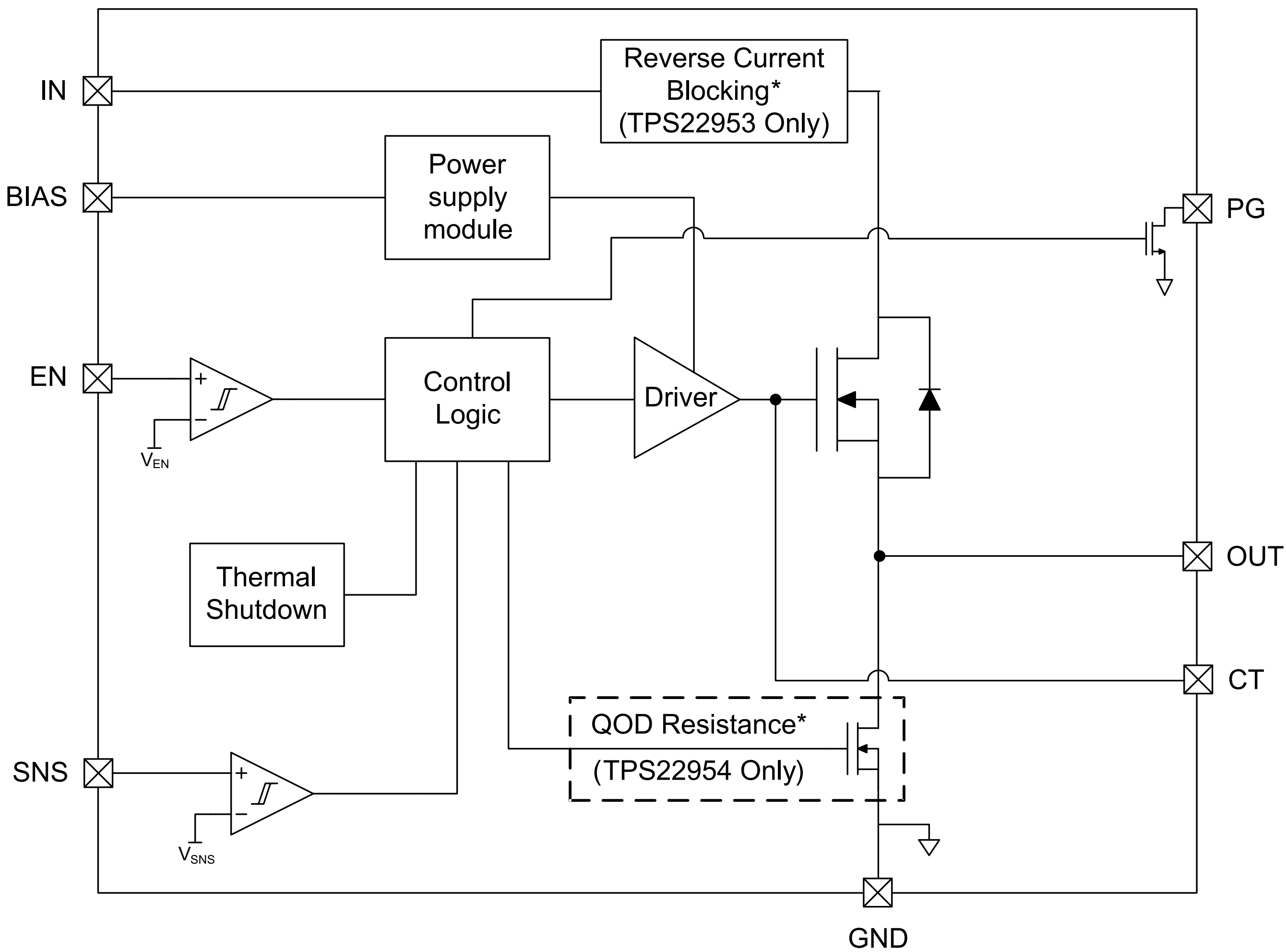
9.1 Overview

The TPS2295x-Q1 are 5.7-V, 5-A load switches in 10-pin SON packages. To reduce voltage drop for low voltage, high current rails the device implements a low-resistance N-channel MOSFET, which reduces the drop out voltage through the device at high currents. The integrated adjustable Undervoltage Lockout (UVLO) and adjustable Power Good (PG) threshold provides voltage monitoring as well as robust power sequencing.

The adjustable rise-time control of the device greatly reduces inrush current for a wide variety of bulk load capacitances, thereby reducing or eliminating power supply droop. The switch is independently controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals. A 15-Ω, on-chip load resistor integrates into the device for output quick discharge when the switch turns off.

During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated power monitoring functionality, control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

9.2 Functional Block Diagram



(*) Only active when the switch is disabled.

9.3 Feature Description

9.3.1 On and Off Control (EN Pin)

The EN pin controls the state of the switch. When the voltage on EN exceeds $V_{IH,EN}$ the switch enables. When EN goes below $V_{IL,EN}$ the switch disables.

The EN pin has a blanking time of t_{BLANK} on the rising edge after the $V_{IH,EN}$ threshold has been exceeded. The EN pin also has a de-glitch time of $t_{DEGLITCH}$ when the voltage has gone below $V_{IL,EN}$.

The EN pin can also be configured through an external resistor divider to monitor a voltage signal for input UVLO. See Equation 1 and Figure 9-1 on how to configure the EN pin for input UVLO.

$$V_{IH,EN} = V_{IN} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \tag{1}$$

where

- $V_{IH,EN}$ is the rising threshold of the EN pin (see the *Electrical Characteristics* table)
- V_{IN} is the input voltage being monitored (this can be V_{IN}, V_{BIAS}, or an external power supply)
- R_{EN1}, R_{EN2} are the resistor divider values

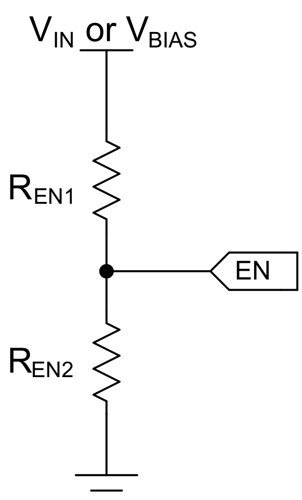


Figure 9-1. Resistor Divider (EN Pin)

9.3.2 Voltage Monitoring (SNS Pin)

The SNS pin of the device can be used to monitor the output voltage of the device or another voltage rail. The pin can be configured with an external resistor divider to set the desired trip point for the voltage being monitored or be tied to OUT directly. If the voltage on the SNS pin exceeds $V_{IH,SNS}$, the voltage being monitored on the SNS pin is considered to be valid high. The voltage on the SNS pin must be greater than $V_{IH,SNS}$ for at least t_{BLANK} before PG is asserted high. If the voltage on the SNS pin goes below $V_{IL,SNS}$, then the switch powers cycle (that is, the switch is disabled and re-enabled). For proper functionality of the device, this pin must not be left floating. If a resistor divider is not being used for voltage sensing, this pin can be tied directly to V_{OUT}.

The SNS pin has a blanking time of t_{BLANK} on the rising edge after the $V_{IH,SNS}$ threshold has been exceeded. The SNS pin has a de-glitch time of $t_{DEGLITCH}$ when the voltage has gone below $V_{IL,SNS}$.

See Equation 2 and Figure 9-2 on how to configure the SNS pin for voltage monitoring.

$$V_{IH,SNS} = V_{OUT} \times \frac{R_{SNS2}}{R_{SNS1} + R_{SNS2}} \tag{2}$$

where

- $V_{IH,SNS}$ is the the rising threshold of the SNS pin (see *Electrical Characteristics* table)
- V_{OUT} is the voltage on the OUTpin
- R_{SNS1}, R_{SNS2} are the resistor divider values

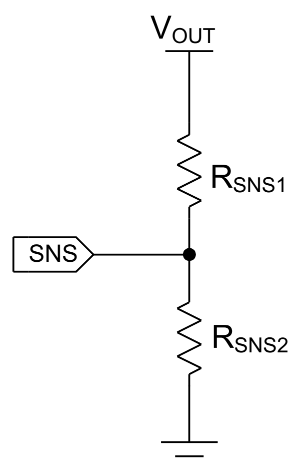


Figure 9-2. Voltage Divdier (SNS Pin)

9.3.3 Power Good (PG Pin)

The PG pin is only asserted high when the voltage on EN exceeds $V_{IH,EN}$ and the voltage on SNS exceeds $V_{IH,SNS}$. There is a t_{BLANK} time, typically 100 µs, between the SNS voltage exceeding $V_{IH,SNS}$ and PG being asserted high. If the voltage on EN goes below $V_{IL,EN}$ or the voltage on SNS goes below $V_{IL,SNS}$, PG is de-asserted. There is a $t_{DEGLITCH}$ time, typically 5 µs, between the EN voltage or SNS voltage going below their respective V_{IL} levels and PG being pulled low.

PG is an open drain pin and must be pulled up with a pullup resistor. Be sure to never exceed the maximum operating voltage on this pin. If PG is not being used in the application, tie it to GND for proper device functionality.

For proper PG operation, the BIAS voltage must be within the recommended operating range. In systems that are very sensitive to noise or have long PG traces, TI recommends to add a small capacitance from PG to GND for decoupling.

9.3.4 Supervisor Fault Detection and Automatic Restart

The falling edge of the SNS pin below $V_{IL,SNS}$ is considered a fault case and causes the load switch to be disabled for $t_{RESTART}$ (typically 2 ms). After the $t_{RESTART}$ time, the switch is automatically re-enabled as long as EN is still above $V_{IH,EN}$. In the case, the SNS pin is being used to monitor V_{OUT} or a downstream voltage. The restart helps to protect against excessive overcurrent if there is a quick short to GND. See Figure 9-3.

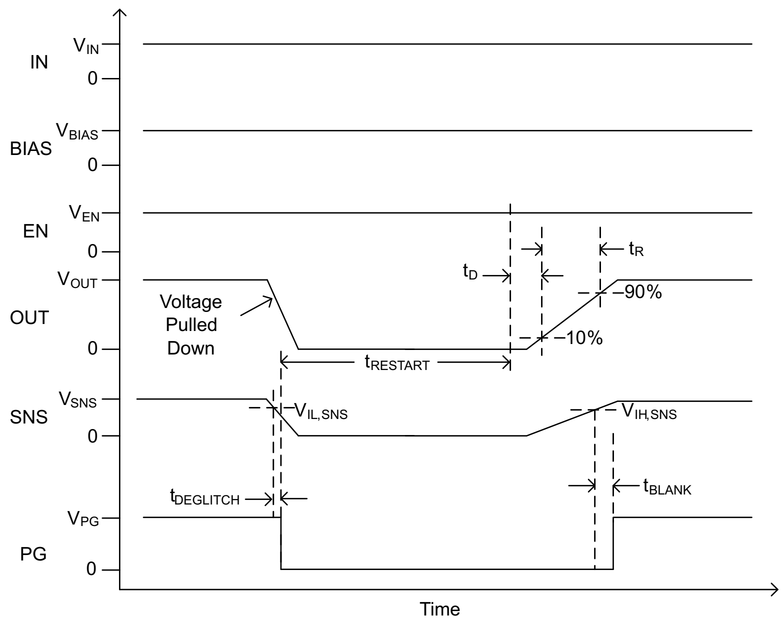


Figure 9-3. Automatic Restart After Quick Short to GND

9.3.5 Manual Restart

The falling edge of the SNS pin below $V_{IL,SNS}$ is considered a fault case and causes the load switch to be disabled for $t_{RESTART}$ (typically 2 ms). The SNS pin can be driven by an MCU to manually reset the load switch. After the $t_{RESTART}$ time, the switch is automatically re-enabled as long as EN is still above $V_{IH,EN}$, even is SNS is held low. The PG pin stays low until the switch is re-enabled and the SNS pin rises above $V_{IH,SNS}$. See Figure 9-4.

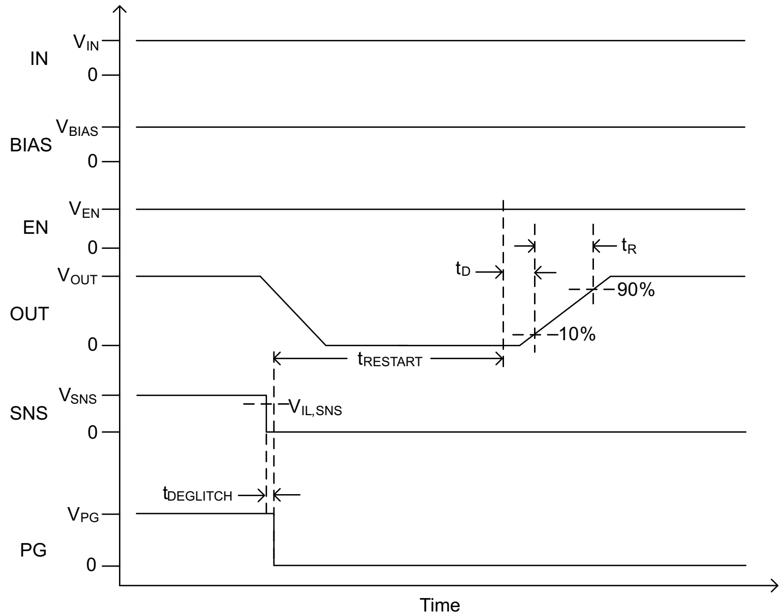


Figure 9-4. Manual Restart (SNS Held Low)

If the SNS pin is brought above $V_{IH,SNS}$ within the $t_{RESTART}$ time, the switch still waits to re-enable. The PG pin also stays low until t_{BLANK} after switch is re-enabled. In this case, PG indicates when the switch is enabled and capable of being reset again. See Figure 9-5.

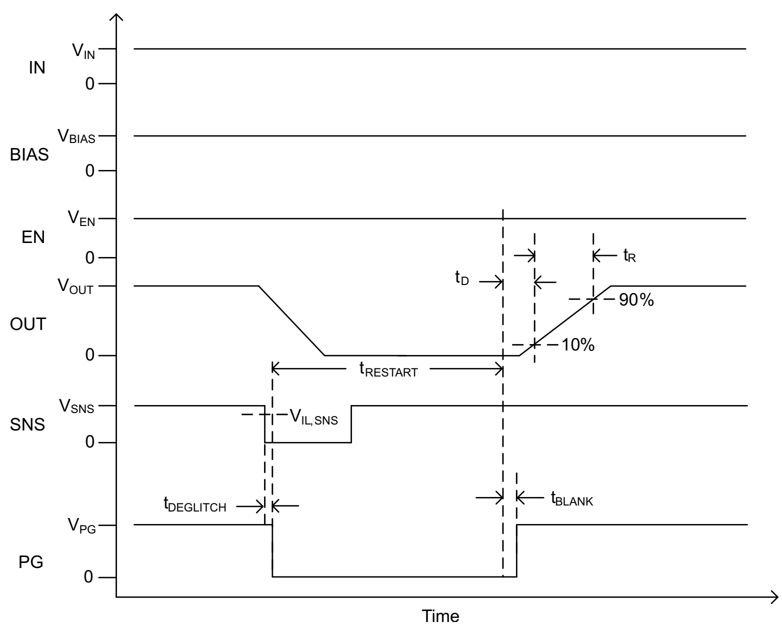


Figure 9-5. Manual Restart (SNS Toggled Low to High)

9.3.6 Thermal Shutdown

If the junction temperature of the device exceeds T_{SD}, the switch disables. The device enables after the junction temperature drops by TSD_{HYS} as long as EN is still greater than $V_{IH,EN}$.

9.3.7 Reverse Current Blocking (TPS22953-Q1 Only)

When the switch disables (either by de-asserting EN or SNS, triggering thermal shutdown, or losing power), the reverse current blocking (RCB) feature of the device engages within t_{RCB}, typically 10 µs. After the RCB engages, the reverse current from the OUT pin to the IN pin is limited to $I_{RCB,IN}$, typically 0.01 µA.

9.3.8 Quick Output Discharge (QOD) (TPS22954-Q1 Only)

The Quick Output Discharge (QOD) transistor is engaged indefinitely whenever the switch is disabled and the recommended V_{BIAS} voltage is met. During this state, the QOD resistance (R_{PD}) discharges V_{OUT} to GND. TI does not recommend to apply a continuous DC voltage to OUT when the device is disabled.

The QOD transistor can remain active for a short period of time even after V_{BIAS} loses power. This brief period of time is defined as t_{DIS}. For best results, TI recommends the device get disabled before V_{BIAS} goes below the minimum recommended voltage. The waveform in Figure 9-6 shows the behavior when power is applied and then removed in a typical application.

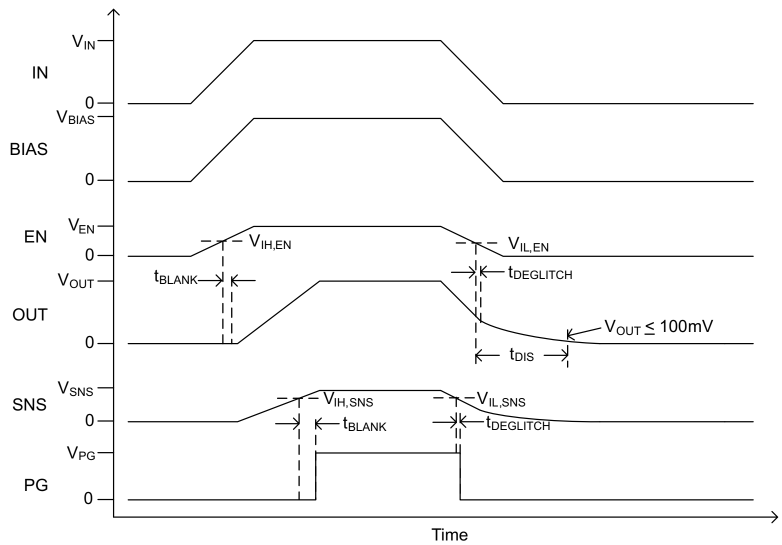


Figure 9-6. Power Applied and Then Removed in a Typical Application

At the end of the t_{DIS} time, it is not assured that V_{OUT} is 0 V because the final voltage is dependent upon the initial voltage and the C_L capacitor. The final V_{OUT} can be calculated with Equation 3 for a given initial voltage and C_L capacitor.

$$V_f = V_o \times e^{\frac{-t}{RC}} \quad (3)$$

where

- V_f is the final V_{OUT} voltage
- V_o is the initial V_{OUT} voltage
- R is the the value of the output discharge resistor, R_{PD} (see the *Electrical Characteristics* table)
- C is the output bulk capacitance on OUT

9.3.9 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \le V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics* table. See Figure 9-7 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} increases. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

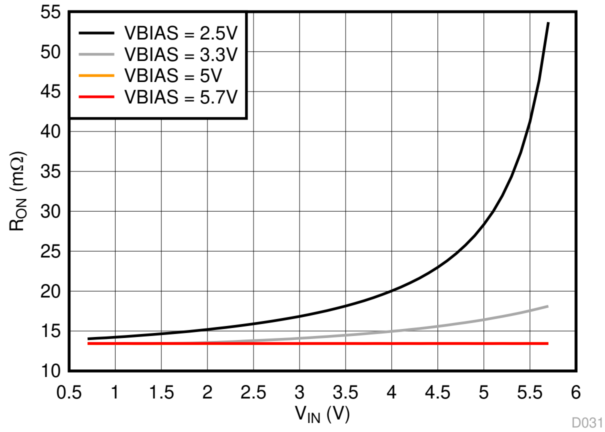


Figure 9-7. R_{ON} When V_{IN} > V_{BIAS}

9.3.10 Adjustable Rise Time (CT Pin)

A capacitor to GND on the CT pin sets the slew rate for V_{OUT}. An appropriate capacitance value must be placed on CT such that the I_{MAX} and I_{PLS} specifications of the device are not violated. The capacitor to GND on the CT pin must be rated for 25 V or higher. Equation 4 shows an approximate formula for the relationship between CT (except for CT = open) and the slew rate for any V_{BIAS}.

$$SR = 0.35 \times CT + 20 \quad (4)$$

where

- SR is the slew rate (in μs/V).
- CT is the capacitance value on the CT terminal (in pF).
- The units for the constant 20 are μs/V.
- The units for the constant 0.35 are μs/(V*pF).

Rise time can be calculated by multiplying the input voltage (typically 10% to 90%) by the slew rate. Table 9-1 contains rise time values measured on a typical device.

Table 9-1. Rise Time

CTx (pF)	RISE TIME (μs) 10% – 90%, C_L = 0.1 μF, V_{BIAS} = 2.5 V to 5.7 V, R_L = 10-Ω LOAD. TYPICAL VALUES AT 25°C, 25-V X7R 10% CERAMIC CAP					
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	0.7 V
Open	140	98	62	54	46	32
220	444	301	175	150	124	81
470	767	518	299	255	210	133
1000	1492	994	562	474	387	245
2200	3105	2050	1151	961	787	490
4700	6420	4246	2365	1980	1612	998
10000	14059	9339	5183	4331	3533	2197

9.3.11 Power Sequencing

The TPS2295x-Q1 operates regardless of power-on and power-off sequencing order. The order in which voltages are applied to IN, BIAS, and EN does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions. If voltage is applied to EN before IN and BIAS, the slew rate of VOUT is not controlled. Also, turning off IN or BIAS while EN is high does not damage the device.

9.4 Device Functional Modes

Table 9-2 describes what the OUT pin is connected to for a particular device as determined by the EN pin.

Table 9-2. Function Table

EN	TPS22953-Q1	TPS22954-Q1
L	OPEN	R_{PD} to GND
H	IN	IN

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available on www.ti.com for further aid.

10.1.1 Input to Output Voltage Drop

The input to output voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics* table of this data sheet. After the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} voltage conditions, use Equation 5 to calculate the input to output voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \tag{5}$$

where

- ΔV is the voltage drop from IN to OUT
- I_{LOAD} is the load current
- R_{ON} is the On-Resistance of the device for a specific V_{IN} and V_{BIAS}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.1.2 Thermal Considerations

The maximum IC junction temperature must be restricted to just under the thermal shutdown (T_{SD}) limit of the device. Use Equation 6 to calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \tag{6}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation.
- $T_{J(max)}$ is the maximum allowable junction temperature before hitting thermal shutdown (see the *Electrical Characteristics* table).
- T_A is the ambient temperature of the device.
- θ_{JA} is the junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

10.1.3 Automatic Power Sequencing

The PG pin of the TPS2295x-Q1 allows for automatic sequencing of multiple system rails or loads. The accurate SNS voltage monitoring ensures the first rail is up before the next starts to turn on. This approach provides robust system sequencing and reduces the total inrush current by preventing overlap. Figure 10-1 shows how two rails can be sequenced. There is no limit to the number of rails that can be sequenced in this way.

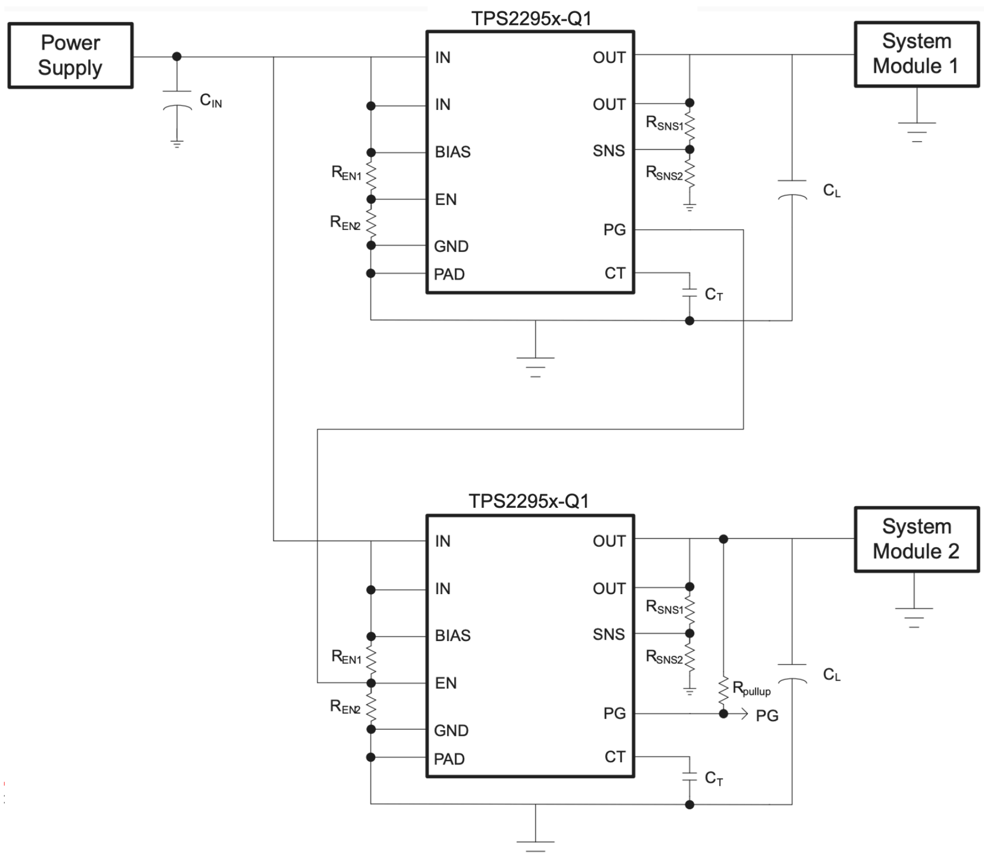


Figure 10-1. Power Sequencing with PG Control Schematic

10.1.4 Monitoring a Downstream Voltage

The SNS pin can be used to monitor other system voltages in addition to V_{OUT}. The status of the monitored voltage are indicated by the PG pin which can be pulled up to V_{OUT} or another voltage. Figure 10-2 shows an example of the TPS2295x-Q1 monitoring the output of a downstream DC/DC regulator. In this case, the switch turns on when the power supply is above the UVLO, but the PG is not asserted until the DC/DC regulator has started up.

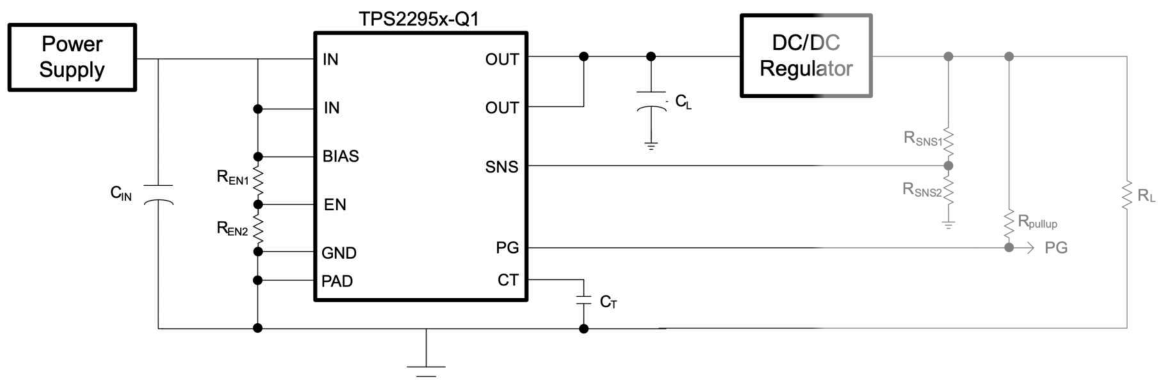


Figure 10-2. Monitoring a Downstream Voltage Schematic

In this application, if the DC/DC Regulator is shut down, the supervisor registers this as a fault case and resets the load switch.

10.1.5 Monitoring the Input Voltage

The SNS pin can also be used to monitor V_{IN} in the case a MCU GPIO is being used to control the EN. This event allows PG to report on the status of the input voltage when the switch is enabled. See Figure 10-3.

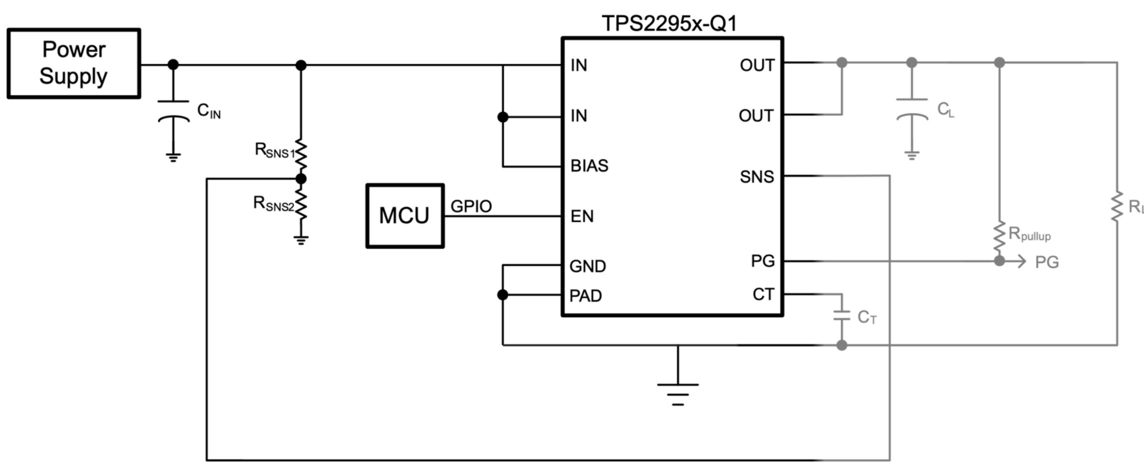


Figure 10-3. Monitoring the Input Voltage Schematic

10.1.6 Break-Before-Make Power MUX (TPS22953-Q1 Only)

The reverse current blocking feature of the TPS22953-Q1 makes it suitable for power multiplexing (MUXing) between two power supplies with different voltages. The SNS and PG pin can be configured to implement break-before-make logic. The circuit in Figure 10-4 shows how the detection of power supply 1 can be used to disable the load switch for power supply 2. By tying the SNS of Load Switch 1 directly to the input, its PG pin is pulled up as soon as the device is enabled.

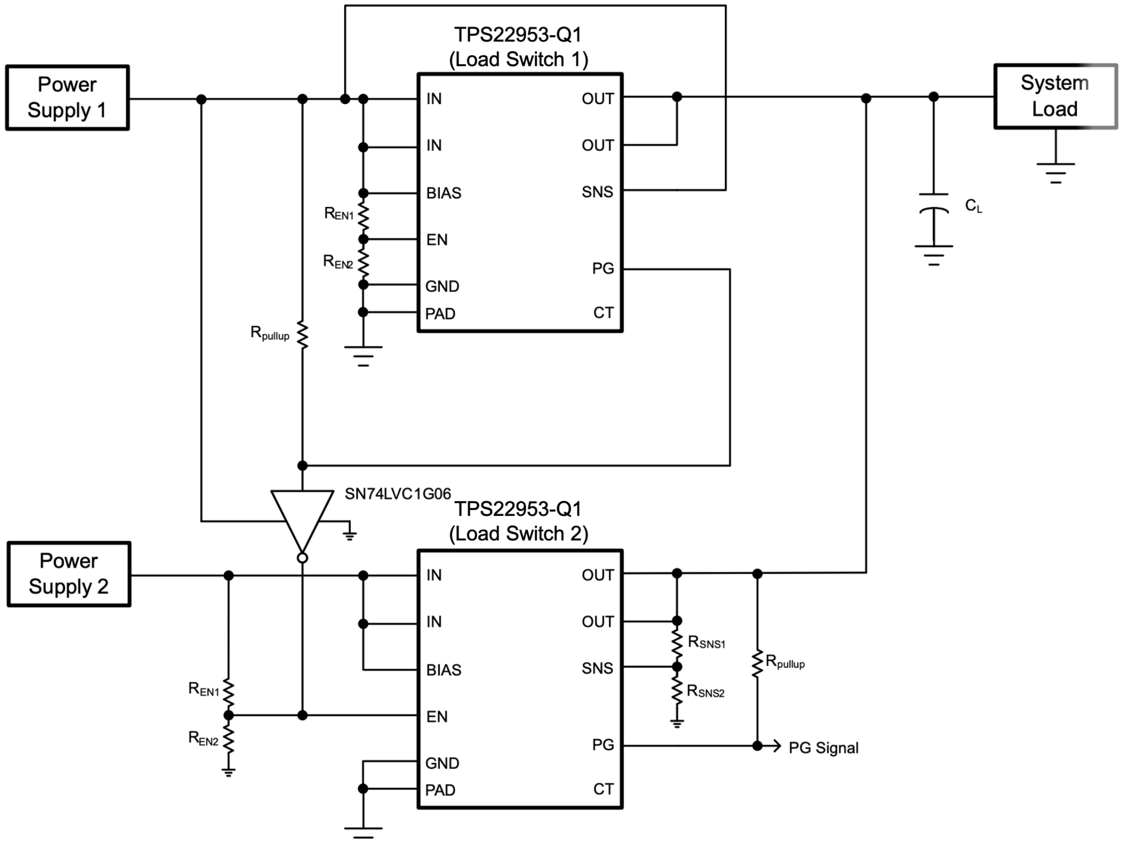


Figure 10-4. Break-Before-Make Power MUX Schematic

The break-before-make logic ensures that power supply 2 is completely disconnected before power supply 1 is connected. This approach provides very robust reverse current blocking. However, in most cases, this aproach also results in a dip in the output voltage when switching between supplies.

The amount of voltage dip depends on the loading, the output capacitance, and the turn-on delay of the load switch. In this application, leaving the CT pin open results in the shortest turn-on delay and minimizes the output voltage dip.

Table 10-1 summarizes the logic of the PG Signal for Figure 10-4.

Table 10-1. Break-Before-Make PG Signal

PG Signal	Indication
H	Power supply 1 not present. System powered from power supply 2.
L	Power supply 1 present. System powered from power supply 1.

10.1.7 Make-Before-Break Power MUX (TPS22953-Q1 Only)

The reverse current blocking feature of the TPS22953-Q1 makes it suitable for power multiplexing (MUXing) between two power supplies with different voltages. The SNS and PG pin can be configured to implement make-before-break logic. The circuit in Figure 10-5 shows how the detection of Load Switch 1 turning on can be used to disable the load switch for power supply 2. By tying SNS to the Load, the PG is pulled up when the output voltage starts to rise. This event disables an active low load switch such as the TPS22910A.

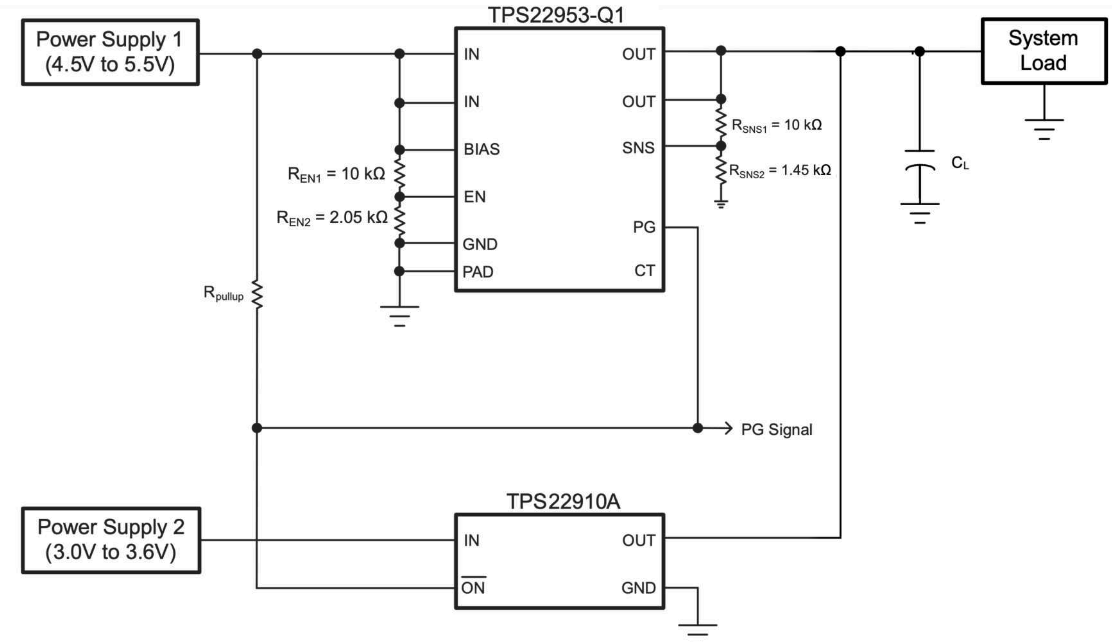


Figure 10-5. Make-Before-Break Power MUX Schematic

The make-before-break logic ensures that power supply 2 is not disconnected until power supply 1 is connected. Unlike break-before-make logic, this approach is ideal for preventing voltage dip on the output when switching between supplies. However, in most cases, this approach also results in temporary reverse current flow.

The TPS22910A is well suited for this application because it can detect and block reverse current even before it is disabled by the TPS22953-Q1 PG signal. Also, the active low enable of the TPS22910A eliminates the need for an inverter as shown in the previous example.

To ensure correct logic, the SNS pin must be configured to toggle PG when the load voltage is between the two supply voltages (3.6 V to 4.5 V). The SNS resistor values in Figure 10-5 are assuming a tolerance of ±1% or better.

Table 10-2 summarizes the logic of the PG Signal for Figure 10-5.

Table 10-2. Make-Before-Break PG Signal

PG Signal	Indication
H	Power supply 1 present. System powered from power supply 1.
L	Power supply 1 not present. System powered from power supply 2.

10.2 Typical Application

This application demonstrates how the TPS2295x-Q1 can be used to limit inrush current to output capacitance.

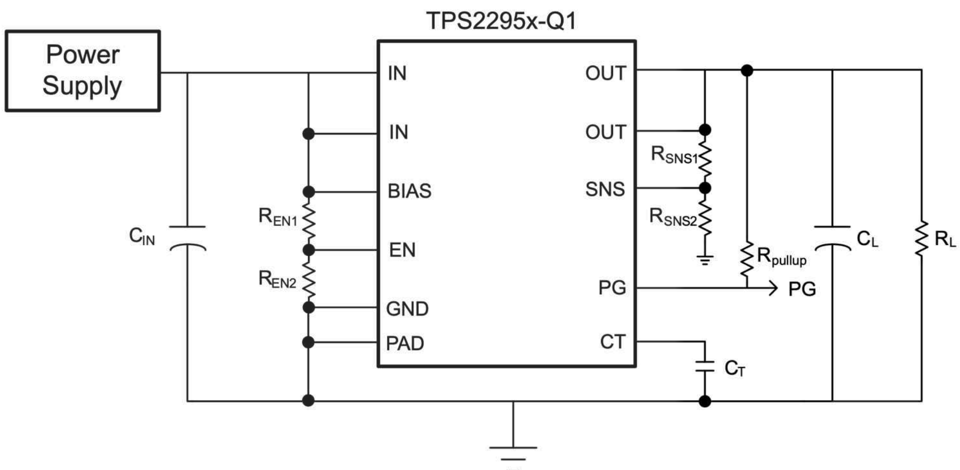


Figure 10-6. Powering a Downstream Module Schematic

10.2.1 Design Requirements

For this design example, use the input parameters shown in Table 10-3.

Table 10-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	47 µF
Maximum acceptable inrush current	150 mA
R_L	None

10.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following:

- Input voltage
- BIAS voltage
- Load current
- Load capacitance
- Maximum acceptable inrush current

10.2.2.1 Inrush Current

Use Equation 7 to determine how much inrush current is caused by the C_L capacitor.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \quad (7)$$

where

- I_{INRUSH} is the amount of inrush caused by C_L
- C_L is the load capacitance on V_{OUT}
- dt is the V_{OUT} rise time (typically 10% to 90%)
- dV_{OUT} is the change in V_{OUT} Voltage (typically 10% to 90%)

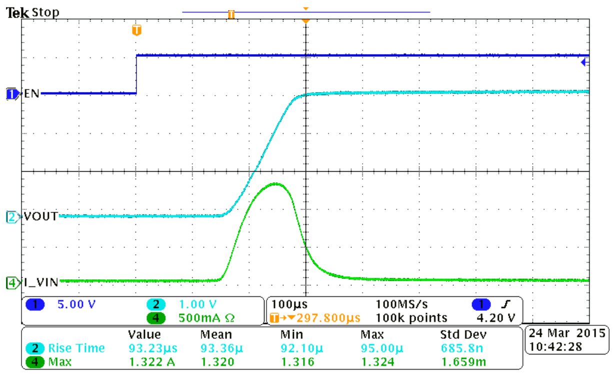
In this case, a Slew Rate slower than 314 μs/V is required to meet the maximum acceptable inrush requirement. Equation 4 can be used to estimate the CT capacitance (as shown in Equation 8 and Equation 9) required for this slew rate.

$$314\ \mu s/V = 0.35 \times CT + 20 \quad (8)$$

$$CT = 840\ pF \quad (9)$$

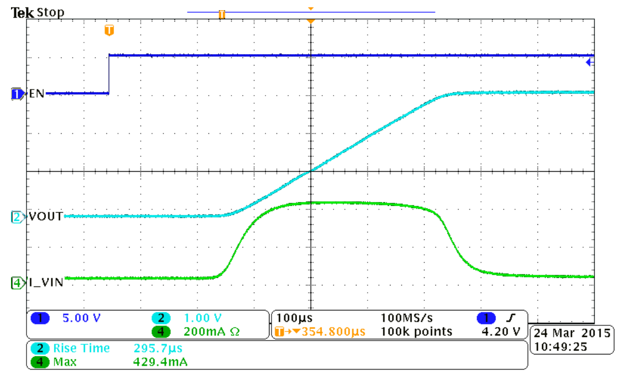
10.2.3 Application Curves

The following Application Curves show the inrush with multiple different CT values. These curves show only a CT capacitance greater than 840 pF results in the acceptable inrush current of 150 mA.



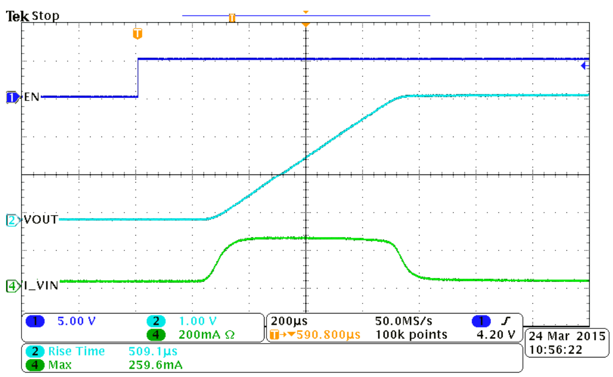
CT = 0 pF

Figure 10-7. Inrush with CT = 0 pF



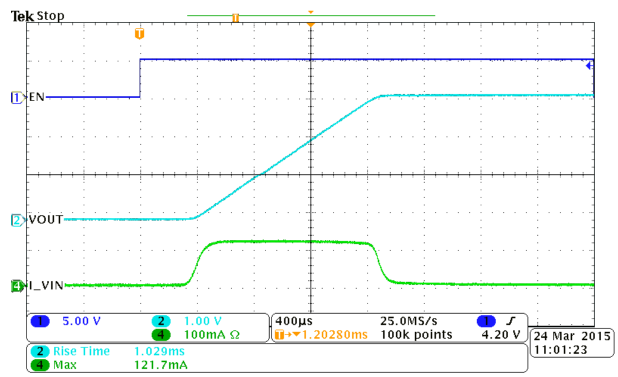
CT = 220 pF

Figure 10-8. Inrush with CT = 220 pF



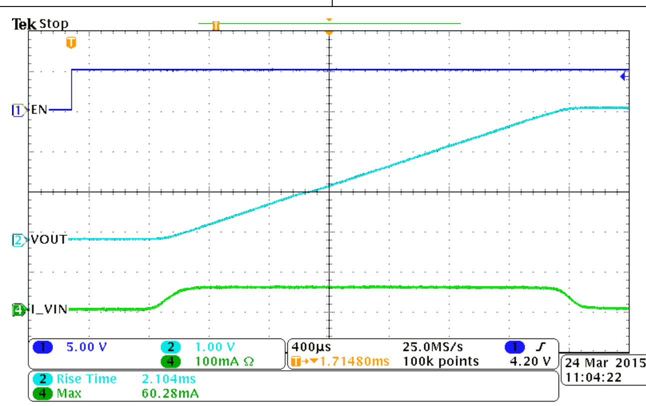
CT = 470 pF

Figure 10-9. Inrush with CT = 470 pF



CT = 1000 pF

Figure 10-10. Inrush with CT = 1000 pF



CT = 2200 pF

Figure 10-11. Inrush with CT = 2200 pF

11 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.7 V and a V_{IN} range of 0.7 V to 5.7 V. The power supply must be well regulated and placed as close to the device terminals as possible. The power supply must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This action causes the load switch to turn on more slowly. Not only does this event reduce transient inrush current, but it also gives the power supply more time to respond to the load current step.

12 Layout

12.1 Layout Guidelines

- Input and Output traces must be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The CT Capacitor must be placed as close as possible to the device to minimize parasitic trace capacitance. TI recommends to cutout copper on other layers directly below CT to minimize parasitic capacitance.
- The IN terminal must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- The OUT terminal must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- The BIAS terminal must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric.

12.2 Layout Example

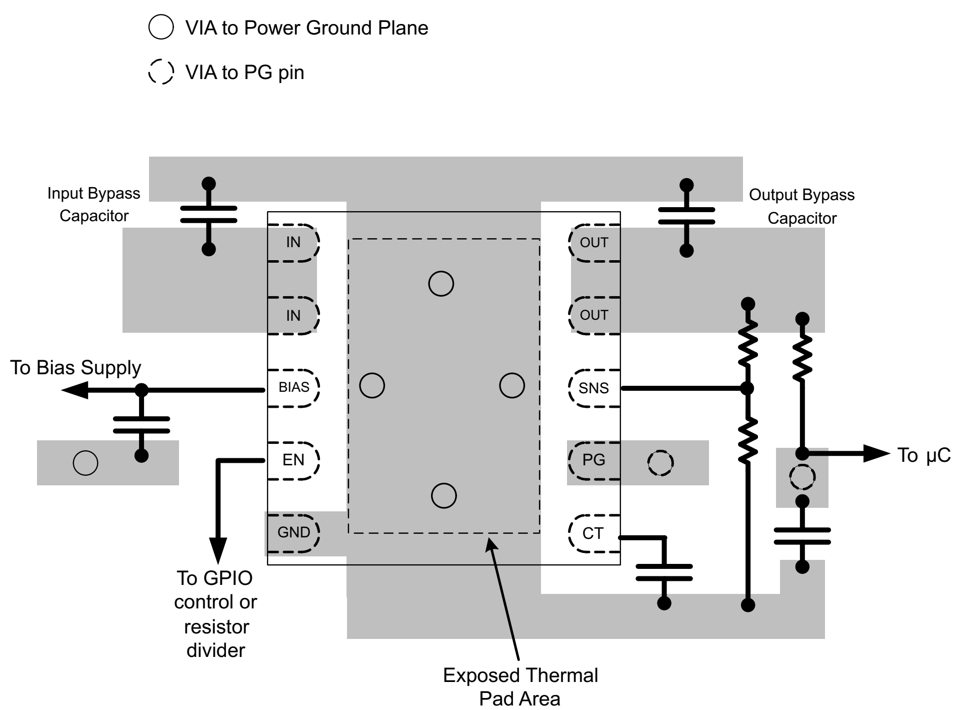


Figure 12-1. Recommended Board Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS22953/54 5.7-V, 5-A, 14-mΩ On-Resistance Load Switch* user's guide
- Texas Instruments, *Basics of Load Switches* application note
- Texas Instruments, *Managing Inrush Current* application note
- Texas Instruments, *Reverse Current Protection in Load Switches* application note
- Texas Instruments, *Quiescent Current vs Shutdown Current for Load Switch Power Consumption* application note
- Texas Instruments, *Load Switch Thermal Considerations* application note

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS22953QDQCRQ1	Active	Preproduction	WSON (DQC) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS22953QDQCRQ1.A	Active	Preproduction	WSON (DQC) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS22954QDQCRQ1	Active	Preproduction	WSON (DQC) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS22954QDQCRQ1.A	Active	Preproduction	WSON (DQC) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS22953QDQCRQ1	Active	Production	WSON (DQC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	953Q1
TPS22953QDQCRQ1.A	Active	Production	WSON (DQC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	953Q1
TPS22954QDQCRQ1	Active	Production	WSON (DQC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	954Q1
TPS22954QDQCRQ1.A	Active	Production	WSON (DQC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	954Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22953-Q1, TPS22954-Q1 :

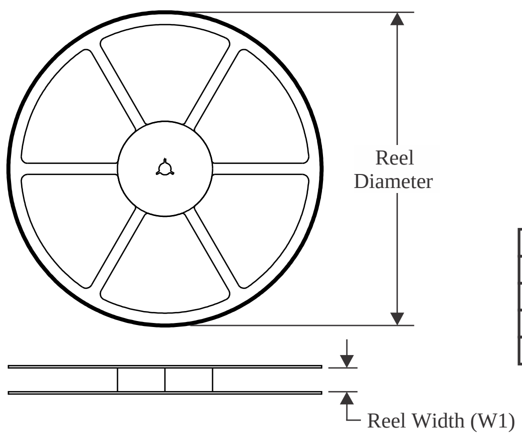
- Catalog : TPS22953, TPS22954

NOTE: Qualified Version Definitions:

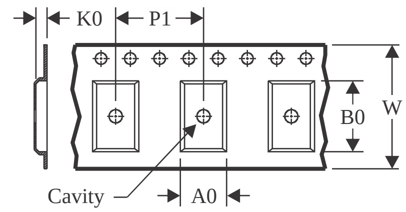
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

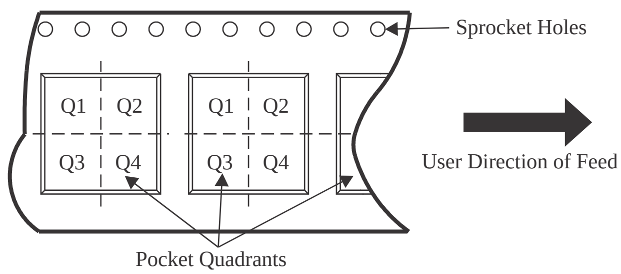


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

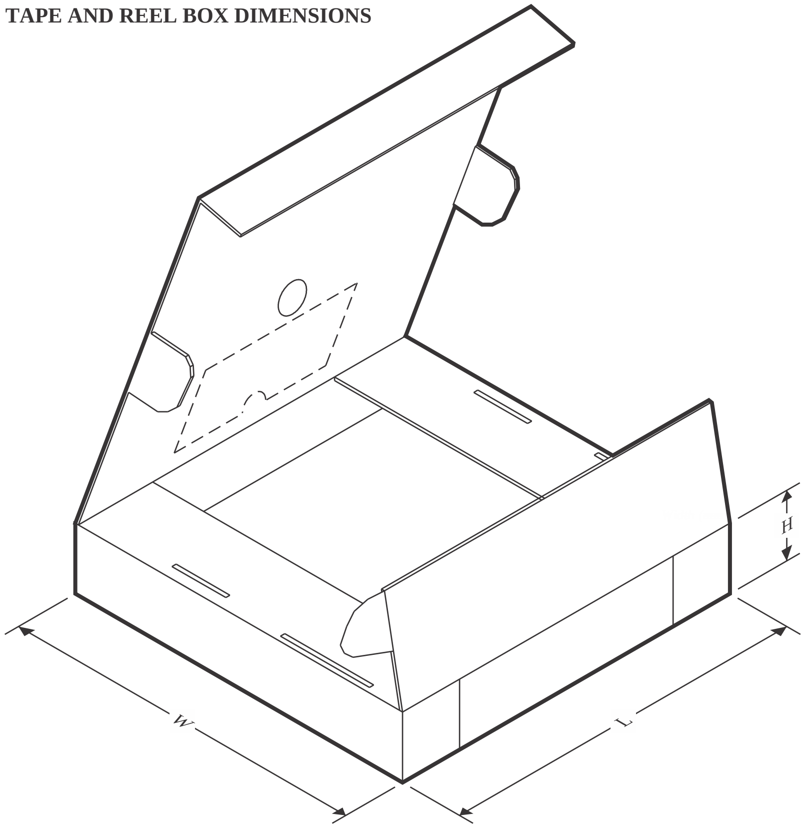
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22953QDQCRQ1	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22954QDQCRQ1	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

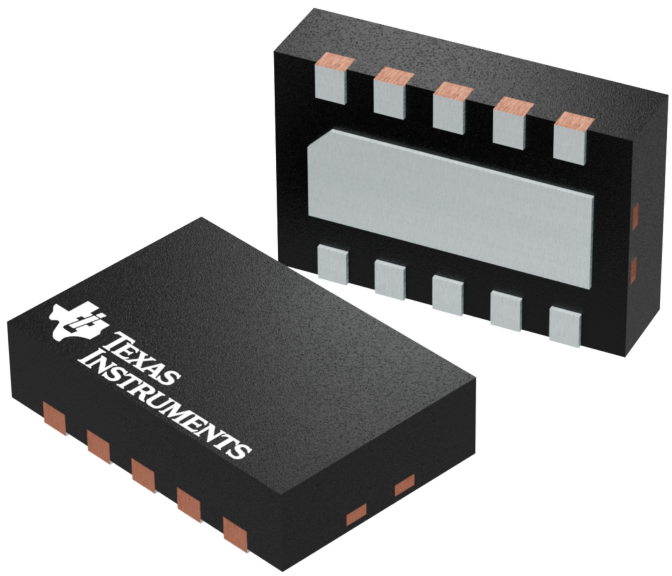


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22953QDQCRQ1	WSON	DQC	10	3000	210.0	185.0	35.0
TPS22954QDQCRQ1	WSON	DQC	10	3000	210.0	185.0	35.0

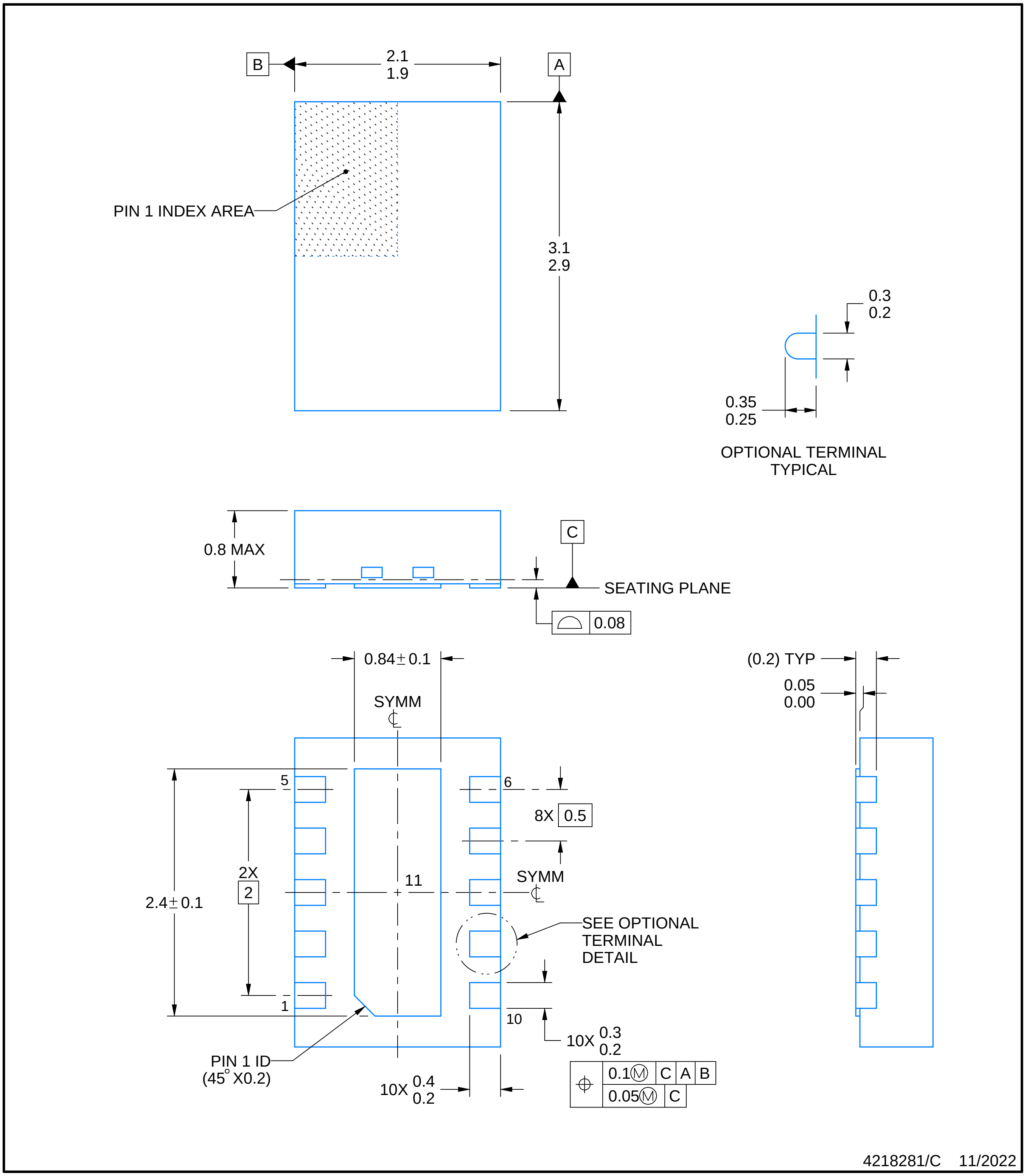
DQC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



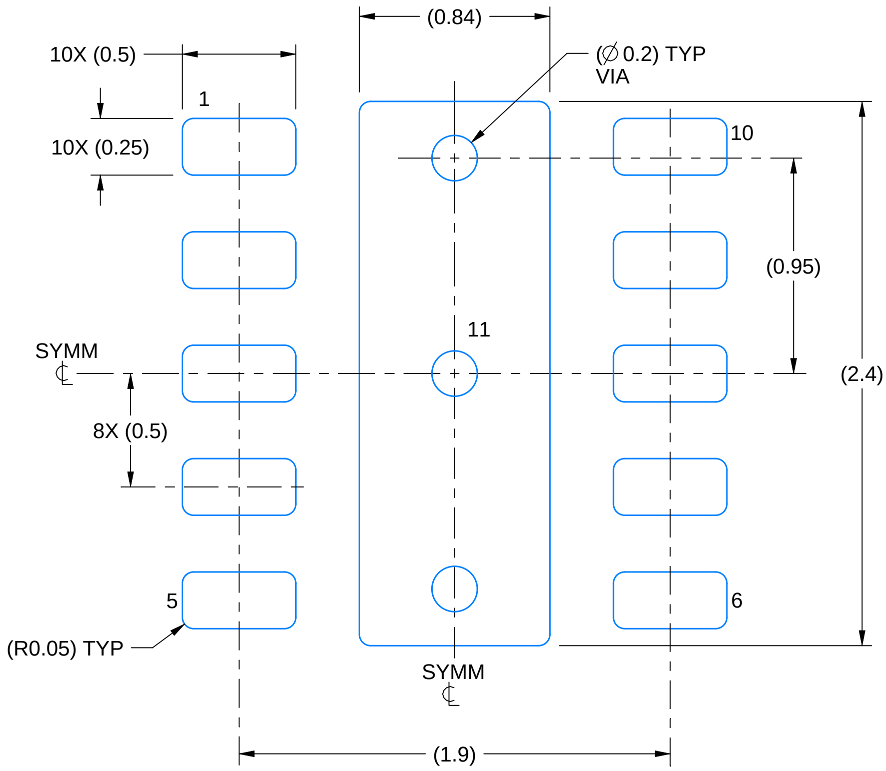
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4209674/B

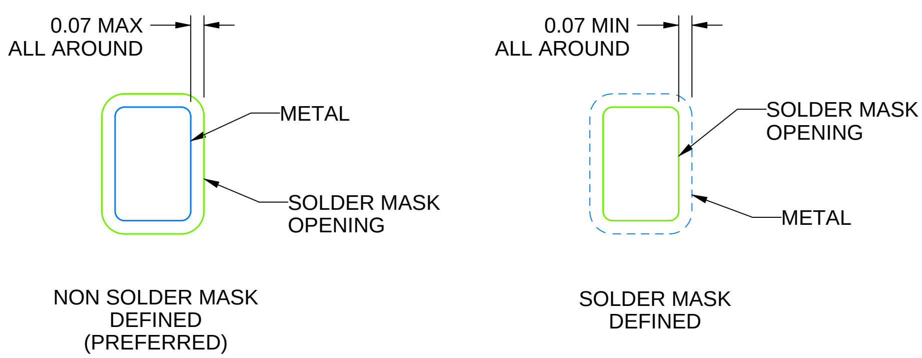


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 30X



SOLDER MASK DETAILS

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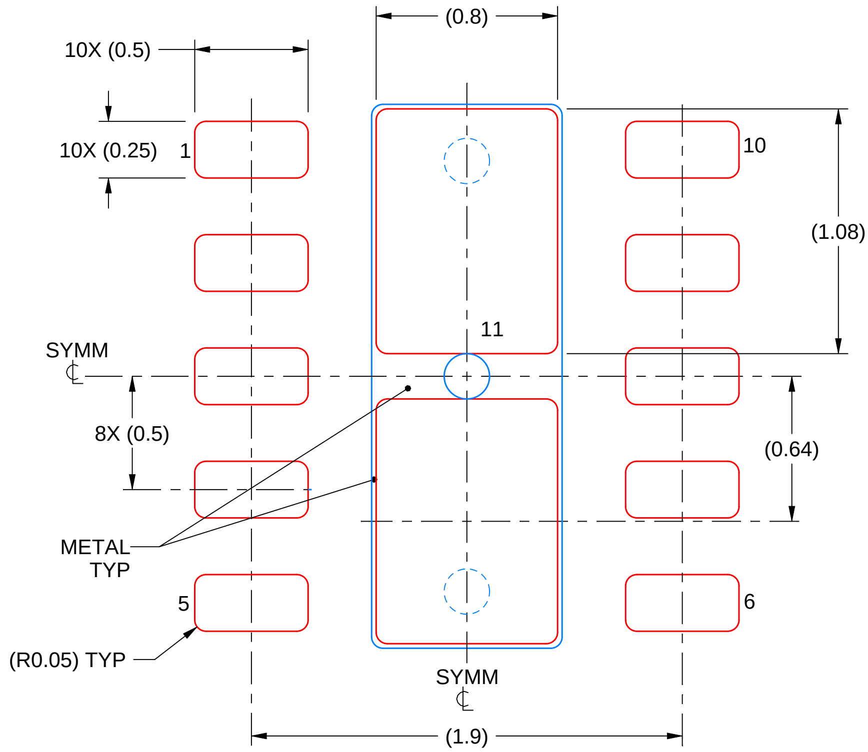
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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