









SLVSEN5B - OCTOBER 2018-REVISED MAY 2019



TPS22919

TPS22919 5.5 V, 1.5 A, 90-m Ω Self-Protected Load Switch with Controlled Rise Time

Features

- Input operating voltage range (V_{IN}): 1.6 V to 5.5 V
- Maximum continuous current (I_{MAX}): 1.5 A
- On-Resistance (R_{ON}):
 - 5-V V_{IN}: 89 m Ω (typical)
 - 3.6-V V_{IN}: 90 mΩ (typical)
 - 1.8-V V_{IN}: 105 mΩ (typical)
- Output short protection (I_{SC}): 3 A (typical)
- Low power consumption:
 - ON state (I_O): 8 μA (typical)
 - OFF state (I_{SD}): 2 nA (typical)
- Smart ON pin pull down (R_{PD}):
 - ON ≥ V_{IH} (I_{ON}): 100 nA (maximum)
 - ON ≤ V_{II} (R_{PD}): 530 kΩ (typical)
- Slow Turn ON timing to limit inrush current (t_{ON}):
 - 5.0 V Turn ON time (t_{ON}): 1.95 ms at 3.2 mV/μs
 - 3.6 V Turn ON time (t_{ON}): 1.75 ms at 2.7 mV/μs
 - 1.8 V Turn ON time (t_{ON}): 1.5 ms at 1.8 mV/μs
- Adjustable output discharge and fall time:
 - Internal QOD resistance = 24 Ω (typical)

2 Applications

- Personal electronics
- Set top box
- **HDTV**
- Multi function printer

3 Description

The TPS22919 device is a small, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.6 V to 5.5 V and can support a maximum continuous current of 1.5 A.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. When power is first applied, a Smart Pull Down is used to keep the ON pin from floating until system sequencing is complete. Once the pin is deliberately driven High (>VIH), the Smart Pull Down will be disconnected to prevent unnecessary power

The TPS22919 load switch is also self-protected, meaning that it will protect itself from short circuit events on the output of the device. It also has thermal shutdown to prevent any damage from overheating.

TPS22919 is available in a standard SC-70 package characterized for operation over a iunction temperature range of -40°C to 125°C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22919DCK	SC-70 (6)	2.1 mm × 2.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

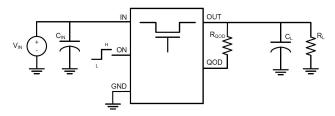




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Product Folder Links: TPS22919

4 Revision History

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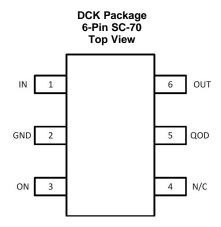
Changes from Original (October 2018) to Revision A

Page

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5 Pin Configuration and Functions



Pin Functions

PIN		1/0	DESCRIPTION
NO.	NAME	1/0	DESCRIPTION
1	IN	ı	Switch input.
2	GND	_	Device ground.
3	ON	I	Active high switch control input. Do not leave floating.
4	NC	_	No connect pin, leave floating.
5	QOD	0	 Quick Output Discharge pin. This functionality can be enabled in one of three ways. Placing an external resistor between VOUT and QOD Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) Disabling QOD by leaving pin floating See the Fall Time (t_{FALL}) and Quick Output Discharge (QOD) section for more information.
6	VOUT	0	Switch output.



6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	-0.3	6	V
V _{OUT}	Maximum Output Voltage Range	-0.3	6	V
V _{ON}	Maximum ON Pin Voltage Range	-0.3	6	V
V_{QOD}	Maximum QOD Pin Voltage Range	-0.3	6	V
I _{MAX}	Maximum Continuous Current		1.5	А
I _{PLS}	Maximum Pulsed Current (2 ms, 2% Duty Cycle)		2.5	Α
TJ	Junction temperature	Internally Limit	ed	°C
T _{STG}	Storage temperature	-65	150	°C
T _{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

⁽¹⁾ Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins ⁽¹⁾	±2000		
	Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins (2)	±1000	V	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP MAX	UNIT
V_{IN}	Input Voltage Range	1.6	5.5	V
V _{OUT}	Output Voltage Range	0	5.5	V
V_{IH}	ON Pin High Voltage Range	1	5.5	V
V_{IL}	ON Pin Low Voltage Range	0	0.35	V
T _A	Ambient Temperature	-40	105	°C

6.4 Thermal Information

		TPS22919	
	THERMAL METRIC ⁽¹⁾	DCK (SC-70)	UNIT
		PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	142.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	52.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	68.8	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.



6.5 Electrical Characteristics

Typical values at VIN = 3.6V unless otherwise specified

	PARAMETER	TEST CO	ONDITIONS	TJ	MIN	TYP	MAX	UNIT
Input Sup	oly (VIN)							
	VIII Ociona di Ociona di	V SV VOUT	0	25°C		8	15	μΑ
I _{Q, VIN}	VIN Quiescent Current	V _{ON} ≥ V _{IH} , VOUT	= Open	-40°C to 125°C			20	μΑ
	VIN Object design Comment	V 4V VOLIT	OND	25°C		2	20	nA
I _{SD, VIN}	VIN Shutdown Current	V _{ON} ≤ V _{IL} , VOUT	= GND	-40°C to 125°C			800	nA
ON-Resist	ance (RON)							
				25°C		89	125	mΩ
			V 5.V	-40°C to 85°C			150	mΩ
			$V_{IN} = 5 V$	-40°C to 105°C			175	mΩ
				-40°C to 125°C			200	mΩ
				25°C		90	150	mΩ
Ь	ON Ctata Danistanaa	I _{OUT} = -200 mA	V _{IN} = 3.6 V	-40°C to 85°C			200	mΩ
R _{ON}	ON-State Resistance			-40°C to 105°C			225	mΩ
				-40°C to 125°C			250	mΩ
				25°C		105	300	mΩ
				-40°C to 85°C			400	mΩ
			V _{IN} = 1.8 V	-40°C to 105°C			450	mΩ
				-40°C to 125°C			500	mΩ
Output Sh	ort Protection (ISC)	·						
	Chart Circuit Comment Limit	V _{OUT} ≤ V _{IN} - 1.5 \	J	-40°C to 125°C		3		Α
I _{SC}	Short Circuit Current Limit	V _{OUT} ≤ V _{SC}		-40°C to 125°C	30	500	900	mA
V _{SC}	Output Short Detection Threshold	V _{IN} - V _{OUT}		-40°C to 125°C	0.3	0.36	0.46	V
t _{SC}	Output Short Reponse Time	$V_{IN} = 1.6V \text{ to } 5.5^{\circ}$ applied	V, 10mΩ short	-40°C to 125°C		2		μs
-	Thermal Shutdown			Rising		180		°C
T _{SD}	Thermal Shuldown			Falling		145		°C
Enable Pir	n (ON)							
I _{ON}	ON Pin Leakage	$V_{ON} \ge V_{IH}$		-40°C to 125°C			100	nA
R _{PD, ON}	Smart Pull Down Resistance	$V_{ON} \le V_{IL}$		-40°C to 125°C		530		kΩ
Quick-out _l	out Discharge (QOD)							
R _{PD, QOD}	QOD Pin Internal Discharge Resistance	V _{ON} ≤ V _{IL}		-40°C to 125°C		24		Ω

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of CL = 0.1 μ F, RL = 100 Ω

P	ARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		VIN = 5.0 V			1950		μs
t _{ON}	Turn ON Time	VIN = 3.6 V			1750		μs
		VIN = 1.8 V		1500		μs	
VIN = 5.0 V		VIN = 5.0 V			1280		μs
t _R	t _R Output Rise Time	VIN = 3.6 V		1100		μs	
		VIN = 1.8 V			750		μs
		VIN = 5.0 V			3.2		mV/μs
SR _{ON}	Turn ON Slew VIN = 3.6 V				2.7		mV/μs
	raio	VIN = 1.8 V			1.8		mV/μs
t _{OFF}	Turn OFF Time	VIN = 1.8 V to 5.0V	$R_L = 100\Omega, C_L = 0.1uF$		6		μs



Switching Characteristics (continued)

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of CL = 0.1 μ F, RL = 100 Ω

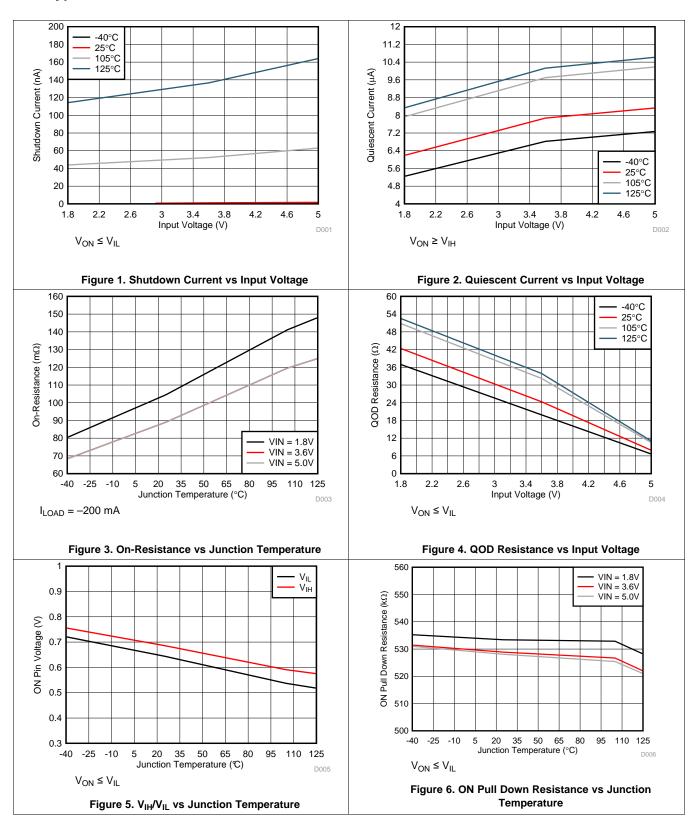
P	PARAMETER TEST CONDITIONS		NDITIONS	MIN	TYP	MAX	UNIT
		$R_L = 100\Omega$	$C_L = 0.1 uF, R_{QOD} = Short$		10		μs
t _{FALL} Output Fall Time		$C_L = 10uF, R_{QOD} = Short$		0.4		ms	
	R _L = Open ⁽²⁾	$C_L = 10 uF, R_{QOD} = 100 \Omega$		3.5		ms	
			$C_L = 100 uF, R_{QOD} = Short$		4		ms

⁽¹⁾ Output may not discharge completely if QOD is not connected to VOUT

⁽²⁾ See the *Timing Application* section for information on how R_L and C_L affect Fall Time.

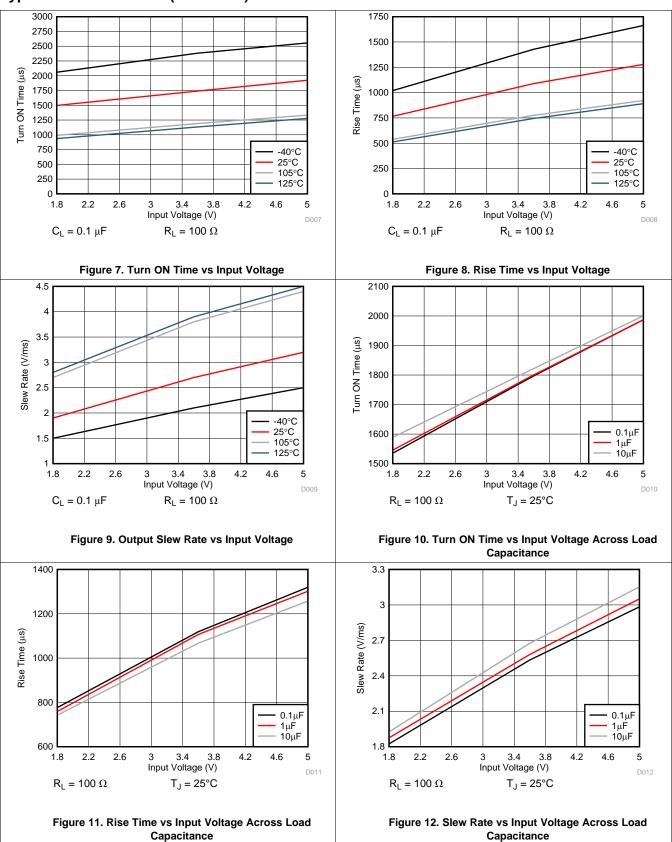


6.7 Typical Characteristics



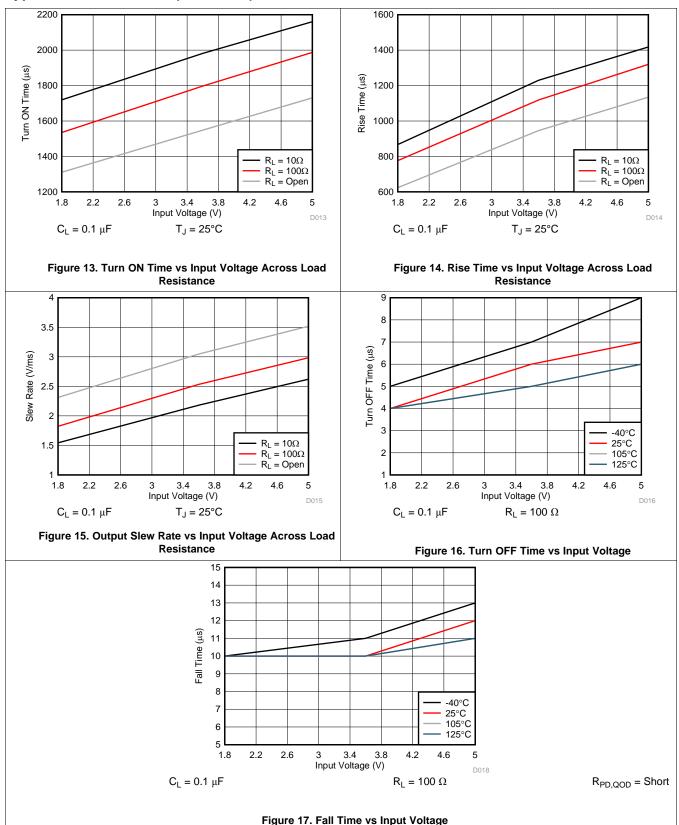
TEXAS INSTRUMENTS

Typical Characteristics (continued)





Typical Characteristics (continued)

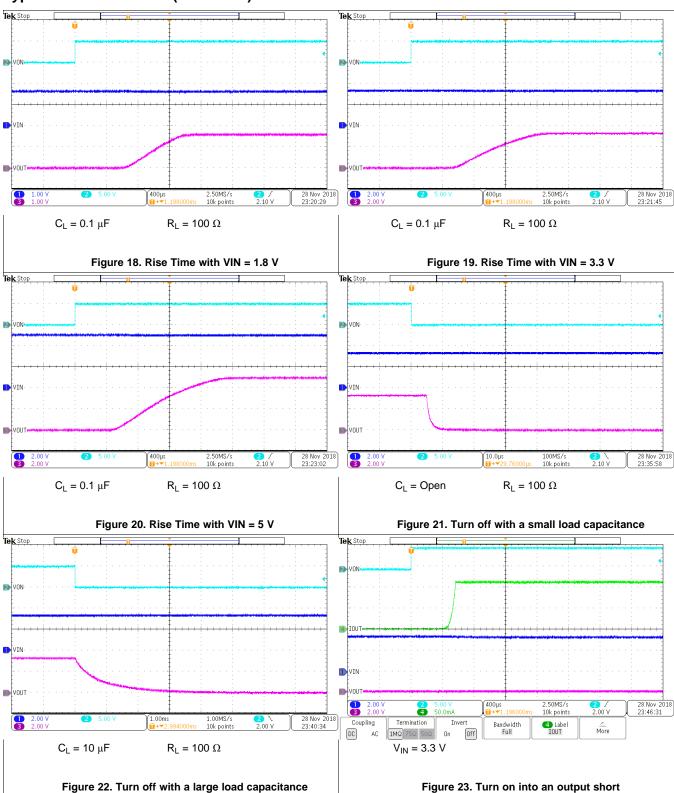


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Typical Characteristics (continued)

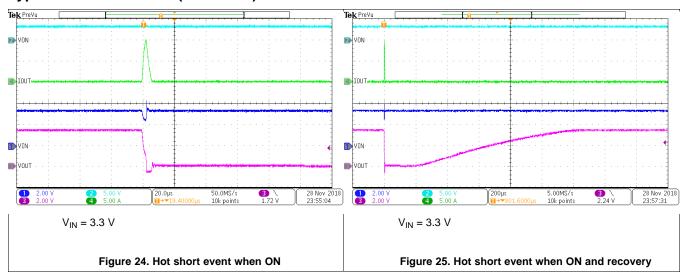


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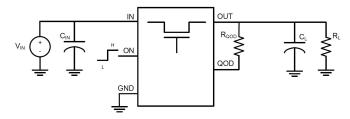


Typical Characteristics (continued)



7 Parameter Measurement Information

7.1 Test Circuit and Timing Waveforms Diagrams



- (1) Rise and fall times of the control signal are 100 ns
- (2) Turn-off times and fall times are dependent on the time constant at the load. For the TPS22919 devices, the internal pull-down resistance QOD is enabled when the switch is disabled. The time constant is $(R_{QOD} + R_{PD,QOD} || R_L) \times C_L$.

Figure 26. Test Circuit

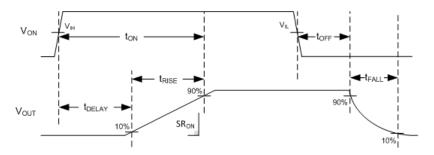


Figure 27. Timing Waveforms



8 Detailed Description

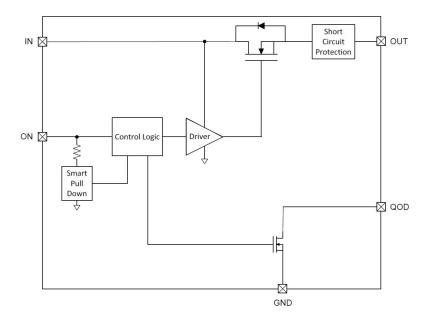
8.1 Overview

The TPS22919 device is a 5.5-V, 1.5-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device.

The TPS22919 device has a slow slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The TPS22919 load switch is also self-protected, meaning that it will protect itself from short circuit events on the output of the device. It also has thermal shutdown to prevent any damage from overheating.

8.2 Functional Block Diagram



Product Folder Links: TPS22919

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8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to VIN, a Smart Pull Down is used to keep the ON pin from floating until the system sequencing is complete. Once the ON pin is deliberately driven high (\geq V_{IH}), the Smart Pull Down is disconnected to prevent unnecessary power loss. See Table 1 when the ON Pin Smart Pull Down is active.

Table 1. Smart-ON Pull Down

VON	Pull Down
≤ V _{IL}	Connected
≥ V _{IH}	Disconnected

8.3.2 Output Short Circuit Protection (I_{SC})

The device will limit current to the output in case of output shorts. When a short occurs, the large VIN to VOUT voltage drop causes the switch to limit the output current (I_{SC}) within (t_{SC}). When the output is below the hard short threshold (V_{SC}), a lower limit is used to minimize the power dissipation while the fault is present. The device will continue to limit the current until it reaches its thermal shutdown temperature. At this time, the device will turn off until its temperature has lowered by the thermal hysteresis (35°C typical) before turning on again.

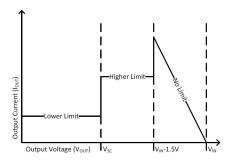


Figure 28. Output Short Circuit Current Limit

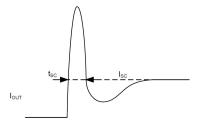


Figure 29. Output Short Circuit Response

8.3.3 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22919 device includes a QOD pin that can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance QOD (R_{PD,QOD}).
- QOD pin connected to VOUT pin using an external resistor R_{QOD}. After the switch becomes disabled, the
 discharge rate is controlled by the value of the total discharge resistance. To adjust the total discharge
 resistance, Equation 1 can be used:

$$R_{DIS} = R_{PD,QOD} + R_{QOD}$$

Where:

• R_{DIS} = Total output discharge resistance (Ω)



- R_{PD,QOD} = Internal pulldown resistance (Ω)
- R_{QOD} = External resistance placed between the VOUT and QOD pins (Ω)

(1)

 QOD pin is unused and left floating. Using this method, there will be no quick output discharge functionality, and the output will remain floating after the switch is disabled.

The fall times of the device depend on many factors including the total discharge resistance (R_{DIS}) and the output capacitance (C_L). To calculate the approximate fall time of V_{OUT} use Equation 2.

$$t_{FALL} = 2.2 \times (R_{DIS} || R_L) \times C_L$$

Where:

- t_{FALL} = Output Fall Time from 90% to 10% (μs)
- R_{DIS} = Total QOD + R_{QOD} Resistance (Ω)
- R_L = Output Load Resistance (Ω)
- C_L = Output Load Capacitance (μF)

(2)

8.3.3.1 QOD When System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN} . Past a certain V_{IN} level, the strength of the R_{PD} will be reduced. If there is still remaining charge on the output capacitor, this will result in longer fall times. For further information regarding this condition, see the Setting Fall Time for Shutdown Power Sequencing section.

8.4 Device Functional Modes

Table 2 describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

Table 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22919 VOUT				
L	QOD pin connected to VOUT with R _{QOD}	GND (R _{PD, QOD} + R _{QOD})				
L	QOD pin tied to VOUT directly	GND (R _{PD, QOD})				
L	QOD pin left open	Floating				
Н	N/A	VIN				



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22919 devices can be used to power downstream modules.

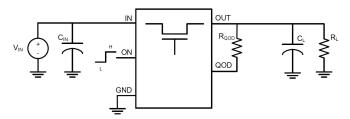


Figure 30. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in Table 3 as the design parameters:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V _{IN})	3.6 V
Load Current / Resistance (R _L)	1 kΩ
Load Capacitance (C _L)	47 μF
Minimum Fall Time (t _F)	40 ms
Maximum Inrush Current (I _{RUSH})	150 mA

(3)



9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use Equation 3 to find the maximum slew rate value to limit inrush current for a given capacitance:

(Slew Rate) =
$$I_{RUSH} \div C_{L}$$

where

- I_{INRUSH} = maximum acceptable inrush current (mA)
- C_I = capacitance on VOUT (μF)
- Slew Rate = Output Slew Rate during turn on (mV/μs)

Based on Equation 3, the required slew rate to limit the inrush current to 150 mA is 3.2 mV/ μ s. The TPS22919 has a slew rate of 2.3 mV/ μ s, so the inrush current will be below 150 mA.

9.2.2.2 Setting Fall Time for Shutdown Power Sequencing

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS22919 device, adding a load switch to each power rail can be used to manage the power down sequencing. To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down.

Once the required fall time is determined, the maximum external discharge resistance (R_{DIS}) value can be found using Equation 2:

$$t_{\text{FALL}} = 2.2 \times (R_{\text{DIS}} \mid\mid R_{\text{L}}) \times C_{\text{L}} \tag{4}$$

$$R_{DIS} = 630 \Omega \tag{5}$$

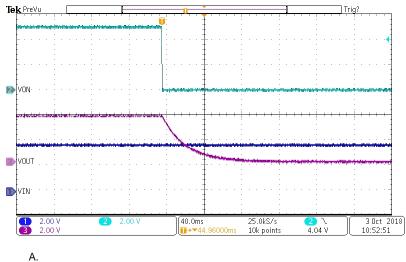
Equation 1 can then be used to calculate the R_{QOD} resistance needed to achieve a particular discharge value:

$$R_{DIS} = QOD + R_{QOD}$$
 (6)

$$R_{QOD} = 600 \Omega \tag{7}$$

To ensure a fall time greater than, choose an R_{OOD} value greater than 600 Ω .

9.2.2.3 Application Curves



 $C_L = 47 \mu F$

Figure 31. Fall Time ($R_{QOD} = 1 \text{ k}\Omega$)



10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.



11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

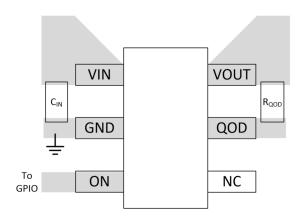


Figure 32. Recommended Board Layout

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125° C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 8:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A}}{\theta_{JA}}$$

where

- P_{D(MAX)} = maximum allowable power dissipation
- T_{J(MAX)} = maximum allowable junction temperature (125°C for the TPS22919 devices)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. Refer to the Thermal Parameters table. This parameter is highly dependent upon board layout.

Product Folder Links: TPS22919

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
PTPS22919DCKR	Obsolete	Preproduction	SC70 (DCK) 6	-	-	Call TI	Call TI	-40 to 125	
TPS22919DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	1CS
TPS22919DCKR.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1CS
TPS22919DCKT	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	1CS
TPS22919DCKT.A	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1CS

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF TPS22919:

Automotive: TPS22919-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22919DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TPS22919DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22919DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
TPS22919DCKT	SC70	DCK	6	250	210.0	185.0	35.0



SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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