TPLD1201-Q1 Automotive Programmable Logic Device with 8-GPIO

1 Features

- Operating characteristics
  - Extended temperature range: -40°C to 125°C
  - Wide supply voltage range: 1.71V to 5.5V
  - Qualified for automotive applications
- Configurable macro-cells
  - 2-, 3-, and 4-bit lookup tables
  - D-type flip-flops and latches with and without reset/set option
  - 8-bit pipe delay
  - Counters and delay generator
  - Programmable deglitch filter or edge detector
  - Discrete analog comparators
  - Voltage reference
  - Oscillator
- Flexible digital I/O features
  - All digital signals can be routed to any GPIO
  - Digital input modes: digital in with and without Schmitt-trigger, low-voltage digital in
  - Digital output modes: push-pull, open-drain NMOS, tri-state
- Development tools
  - InterConnect Studio
  - Evaluation module
  - TPLD programming board

2 Applications

- Factory automation and control
- Communications equipment
- Retail automation and payment
- Test and measurement
- Pro audio, video and signage
- Personal electronics
- Automotive

3 Description

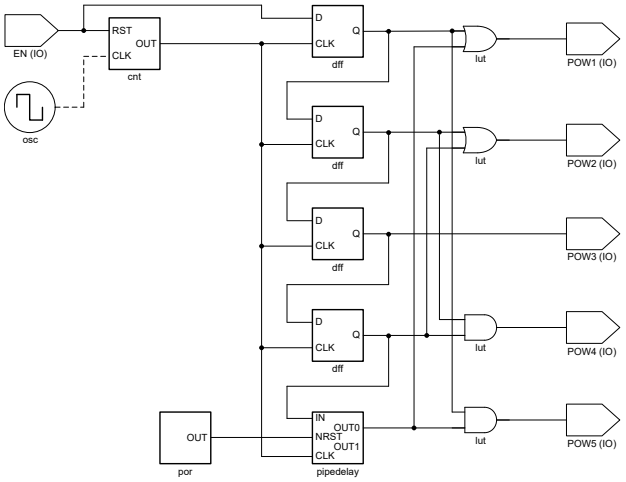
The TPLD1201-Q1 is part of the TI programmable logic device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic, and analog blocks. TPLD provides a fully integrated, low power solution to implement common system functions, such as timing delays, voltage monitors, system resets, power sequencers, I/O expanders, and more. This device features configurable I/O structures that extends compatibility within mixed-signal environments, reducing the number of discrete components required.

System designers can create circuits and configure the macro-cells, I/O pins, and interconnections by temporarily emulating the non-volatile memory or by permanently programming the one-time programmable (OTP) through InterConnect Studio. The TPLD1201-Q1 is supported by a hardware and software ecosystem with application notes, reference designs, and design examples. Visit ti.com for more information and access to design tools.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE
TPLD1201-Q1	DGS (VSSOP, 10)	4.9mm × 3.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

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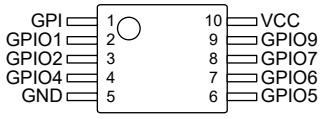
4 Pin Configuration and Functions



Not to scale

Figure 4-1. DGS Package, 10-Pin VSSOP (Top View)

Table 4-1. Pin Functions

PIN			DESCRIPTION	
NAME	DGS	TYPE(1)	Primary function	Secondary function (if any)
GPI	1	I	General-purpose input(3)	
GPIO1	2	I/O	General-purpose I/O	ACMP0 IN+
GPIO2	3	I/O	General-purpose I/O	External VREF IN/ACMP0 or ACMP1 IN-
GPIO4	4	I/O	General-purpose I/O with output enable (OE)(4)	ACMP1 IN+
GND	5	P	Ground	
GPIO5	6	I/O	General-purpose I/O	
GPIO6	7	I/O	General-purpose I/O	
GPIO7	8	I/O	General-purpose I/O with output enable (OE)(4)	Internal VREF OUT
GPIO9	9	I/O	General-purpose I/O	External OSC IN
VCC	10	P	Supply voltage	
NC	—	—	Not internally connected(2)	
NC	—	—	Not internally connected(2)	

(1) P = power, I/O = input/output, I = Input
(2) Pins not internally connected must be grounded or left floating
(3) The general-purpose input (GPI) pin will sustain a high-voltage (VPP) during programming. Take special precaution with peripherals connected to this pin if performing in-system programming.
(4) The output enable (OE) connection is available through the connection mux and can be configured in InterConnect Studio.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage on V_{CC} relative to GND		-0.5	7	V
V_I	Input voltage		-0.5	V_{CC} + 0.5	V
V_O	Output voltage		-0.5	V_{CC} + 0.5	V
I_{IOK}	Input-output clamp current	V_{IO} < 0 or V_{IO} > V_{CC}	-50	50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	-50	50	mA
I_{DC}	Maximum average or DC current (through each pin)	Push-pull 1X		12	mA
		Push-pull 2X		17	
		Open-drain NMOS 1X		18	
		Open-drain NMOS 2X		28	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC specification JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
V_{CC}	Supply voltage			1.71	5.5	V
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
V_{AI}	Analog input voltage	Positive input (ACMP IN+)		0	V_{CC}	V
		Negative input (ACMP IN-, Ext. VREF)		0.15	1.2	
V_{IH}	High-level input voltage	Logic input	1.71V to 5.5V	0.7 × V_{CC}		V
		Low-voltage logic input	1.8V ± 0.09V	0.95		
		Low-voltage logic input	3.3V ± 0.3V	1.2		
		Low-voltage logic input	5V ± 0.5V	1.3		
V_{IL}	Low-level input voltage	Logic input	1.71V to 5.5V		0.3 × V_{CC}	V
		Low-voltage logic input	1.8V ± 0.09V		0.40	
		Low-voltage logic input	3.3V ± 0.3V		0.55	
		Low-voltage logic input	5V ± 0.5V		0.65	
$F_{(EXT)}$	External Oscillator Frequency		1.8V ± 0.09V		8	MHz
			3.3V ± 0.3V		8	
			5V ± 0.5V		8	
T_A	Ambient temperature			–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPLD1201 DGS (VSSOP) 10-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	152.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	88.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	87.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Supply and Power-on Reset								
V_{PORR}	Power-on reset voltage, V_{CC} rising		V_I = V_{CC} or GND, I_O = 0	1.71V to 5.5V	1.25	1.30	1.40	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		V_I = V_{CC} or GND, I_O = 0	1.71V to 5.5V	1.20	1.26	1.35	V
t_{SU}	Startup time		from V_{CC} rising past V_{PORR}	1.71V to 5.5V		245		µs
V_{PP}	Programming voltage				7.5		8	V
Digital IO								
V_{T+}	Positive-going input threshold voltage	Logic Input with Schmitt Trigger		1.8V ± 0.09V	0.94		1.27	V
				3.3V ± 0.3V	1.55		2.30	
				5V ± 0.5V	2.21		3.19	
V_{T-}	Negative-going input threshold voltage	Logic Input with Schmitt Trigger		1.8V ± 0.09V	0.58		0.94	V
				3.3V ± 0.3V	1.1		1.79	
				5V ± 0.5V	1.63		2.7	
V_{HYS}	Schmitt trigger hysteresis (V_{T+} − V_{T-})	Logic Input with Schmitt Trigger		1.8V ± 0.09V	0.20		0.51	V
				3.3V ± 0.3V	0.33		0.61	
				5V ± 0.5V	0.42		0.75	
V_{HYS}	GPI Hysteresis Voltage	Hysteresis voltage applicable to the IN0		1.71V to 5.5V			0.2	V
V_{OH}	High-level output voltage	Push-pull 1X or Open-drain PMOS 1X	I_{OH} = -100µA	1.8V ± 0.09V	1.68			V
		Push-pull 2X or Open-drain PMOS 2X			1.69			
		Push-pull 1X or Open-drain PMOS 1X	I_{OH} = -3mA	3.3V ± 0.3V	2.60			
		Push-pull 2X or Open-drain PMOS 2X			2.71			
		Push-pull 1X or Open-drain PMOS 1X	I_{OH} = -5mA	5V ± 0.5V	3.99			
		Push-pull 2X or Open-drain PMOS 2X			4.13			
V_{OL}	Low-level output voltage	Push-pull 1X	I_{OL} = 100µA	1.8V ± 0.09V			0.038	V
		Push-pull 2X					0.034	
		Open-drain NMOS 1X					0.045	
		Open-drain NMOS 2X					0.02	
		Push-pull 1X	I_{OL} = 3mA	3.3V ± 0.3V			0.1	
		Push-pull 2X					0.1	
		Open-drain NMOS 1X					0.1	
		Open-drain NMOS 2X					0.1	
		Push-pull 1X	I_{OL} = 5mA	5V ± 0.5V			0.12	
		Push-pull 2X					0.12	
		Open-drain NMOS 1X					0.12	
		Open-drain NMOS 2X					0.12	
I_I	Input leakage current	All pins	V_I = V_{CC}	1.71V to 5.5V			±1	µA
			V_I = GND	1.71V to 5.5V			±1	

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{OZ}	Off-state (high-Z state) output current	IO1, IO2, IO5, IO6, IO9	V_O = 0 to 5.5V				0.06	µA
F_{OUT}	Max output frequency(1)	Push-pull 1X or Push-pull 2X	15pF Load capacitance	1.8V ± 0.09V			5	MHz
				3.3V ± 0.3V			12	
				5V ± 0.5V			12	
$R_{pu(int)}$	Internal pull-up resistance					1		MΩ
						100		kΩ
						10		kΩ
$R_{pd(int)}$	Internal pull-down resistance					1		MΩ
						100		kΩ
						10		kΩ
C_I	Input pin capacitance	each input pin	V_I = V_{CC} or GND	1.71V to 5.5V		1.2		pF
C_{IO}	Input-output pin capacitance	each I/O pin	V_{IO} = V_{CC} or GND	1.71V to 5.5V		2.0		pF
Analog Comparator								
t_{start}	Start time	ACMP power on delay	Bandgap always on	1.71V to 5.5V		130		µs
V_{AI}	Input voltage	Positive input		1.71V to 5.5V	0		V_{CC}	V
		Negative input			0		1.2	
V_{offset}	Input offset voltage	T_A = 25°C	V_{HYS} = 0 mV, Gain = 1, VREF= 50mV - 1200mV	1.71V to 5.5V	-10		10	mV
		–40°C < T_A ≤ 125°C			-15		15	
dV_{IO}/dT	Input offset voltage drift	–40°C < T_A ≤ 125°C	V_{HYS} = 0 mV, Gain = 1, VREF= 50mV - 1200mV	1.71V to 5.5V			±8.5	µV/°C
I_B	Input bias current						1	µA
C_{ID}	Input capacitance, differential					3		pF
C_{IM}	Input capacitance, common mode					3		pF
PROP	Propagation delay, response time	Gain = 1, Vref = 50mV - 1200mV, Overdrive = 50mV	Low to High, Low bandwidth enabled	1.71V to 5.5V	1.5			µs
			High to Low Low bandwidth enabled		2.5			
			Low to High, Low bandwidth disabled		0.25			
			High to Low Low bandwidth disabled		0.15			
Analog Comparator - Hysteresis								

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{HYS}	Built-in hysteresis	V_{HYS} = 25mV	T_A = 25°C	1.71V to 5.5V	16	21.6	35	mV
			-40°C to 125°C		15		40	
		V_{HYS} = 50mV	T_A = 25°C		42	50.7	62	
			-40°C to 125°C		40		65	
		V_{HYS} = 200mV	T_A = 25°C		170	202	240	
			-40°C to 125°C		165		245	
Analog Comparator - Input Gain								
R_{sin}	Series input resistance	Gain = 0.5		1.71V to 5.5V		1		MΩ
		Gain = 0.33				0.75		
		Gain = 0.25				1		
G_{err}	Gain error	Gain = 0.5		1.71V to 5.5V	-1		1	%
		Gain = 0.33			-1.25		2.75	
		Gain = 0.25			-1.5		2.5	
Voltage Reference								
VREF	Internal VREF error	T_A = 25°C	VREF = 150mV - 300mV	1.71V to 5.5V	-8.5		8.5	%
		–40°C < T_A ≤ 125°C			-9		9	
		T_A = 25°C	VREF = 350mV - 600mV		-3		3	
		–40°C < T_A ≤ 125°C			-4		4	
		T_A = 25°C	VREF = 650mV - 1000mV		-2.5		2.5	
		–40°C < T_A ≤ 125°C			-4		4	
		T_A = 25°C	VREF = 1050mV - 1200mV		-3		3	
		–40°C < T_A ≤ 125°C			-3.7		3.7	
VREF	VREF error	T_A = 25°C	VREF = 150mV - 300mV	1.71V to 5.5V	-10.2		10.2	%
		–40°C < T_A ≤ 125°C			-11		11	
		T_A = 25°C	VREF = 350mV - 600mV		-5		5	
		–40°C < T_A ≤ 125°C			-5.5		5.5	
		T_A = 25°C	VREF = 650mV - 1000mV		-3.3		3.3	
		–40°C < T_A ≤ 125°C			-4.3		4.3	
		T_A = 25°C	VREF = 1050mV - 1200mV		-4		4	
		–40°C < T_A ≤ 125°C			-5		5	
I_{LOAD}	Output Current			1.71V to 5.5V			500	µA
dV_{OUT}/dT	Output voltage temperature drift			1.71V to 5.5V			550	ppm/°C
dV_{OUT}/dI_{LOAD}	Load regulation			1.71V to 5.5V		0.1	1	mV/µA

(1) Open drain switching performance will be limited by pull-up resistors used

5.6 Supply Current Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC} = 1.8V ± 0.09V			V_{CC} = 3.3V ± 0.3V			V_{CC} = 5V ± 0.5V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Standby											

5.6 Supply Current Characteristics (continued)

T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8V ± 0.09V			V_{CC} = 3.3V ± 0.3V			V_{CC} = 5V ± 0.5V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Quiescent current		Inputs = static, Outputs = open, I_O = 0, OSC powered off		3.41			3.66			4.00		µA
Oscillator													
I_{CC}	Quiescent current	OSC0 enabled: 25kHz	Predivide = 1		3.21			5.24			10.1		µA
			Predivide = 2		3.14			5.17			10.1		
			Predivide = 4		3.53			5.11			10.1		
			Predivide = 8		3.08			5.28			10.0		
		OSC0 enabled: 2MHz	Predivide = 1		42.9			56.0			84.9		
			Predivide = 2		35.9			49.0			79.2		
			Predivide = 4		32.5			45.6			75.5		
			Predivide = 8		30.7			43.8			73.8		
Analog Comparator													
I_{CC}	Quiescent current	Discrete analog comparator (ACMP)	External VREF, IN+ = 0V		24.8			26.2			26.8		µA
			Additional ACMP		3.2			4.7			4.7		
Voltage Reference													
I_{CC}	Quiescent current	Voltage reference (VREF)			16.8			18.3			19.9		µA

5.7 Switching Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Digital IO									
t_{pd}	Delay	Digital input	Push-pull output	Rising	1.8V ± 0.09V		46.2		ns
				Falling			39.1		
				Rising	3.3V ± 0.3V		27.2		
				Falling			24.5		
				Rising	5V ± 0.5V		22.1		
				Falling			21.1		
t_{pd}	Delay	Digital input with Schmitt trigger	Push-pull output	Rising	1.8V ± 0.09V		49.5		ns
				Falling			41.5		
				Rising	3.3V ± 0.3V		29.3		
				Falling			25.3		
				Rising	5V ± 0.5V		23.9		
				Falling			21.5		

5.7 Switching Characteristics (continued)

T_A = 25°C (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Delay		Low-voltage digital input	Push-pull output	Rising	1.8V ± 0.09V		45.0		ns
					Falling			48.1		
					Rising	3.3V ± 0.3V		25.4		
					Falling			30.3		
					Rising	5V ± 0.5V		19.6		
					Falling			28.6		
t_{pd}	Delay		Digital input	Open-drain NMOS output	Rising	1.8V ± 0.09V				ns
					Falling			38.8		
					Rising	3.3V ± 0.3V				
					Falling			24.3		
					Rising	5V ± 0.5V				
					Falling			20.9		
t_{pd}	Delay	Output enable from pin	OE	Push-pull output	Hi-Z to 1	1.8V ± 0.09V		45.0		ns
						3.3V ± 0.3V		26.5		
						5V ± 0.5V		21.7		
					Hi-Z to 0	1.8V ± 0.09V		43.2		ns
						3.3V ± 0.3V		22.6		
						5V ± 0.5V		18.3		
Configurable Use Logic										
t_{pd}	Delay	2-bit LUT	IN	OUT	Rising	1.8V ± 0.09V		1.14		ns
					Falling			1.32		
					Rising	3.3V ± 0.3V		1.14		
					Falling			1.31		
					Rising	5V ± 0.5V		1.16		
					Falling			1.35		
t_{pd}	Delay	3-bit LUT	IN	OUT	Rising	1.8V ± 0.09V		1.31		ns
					Falling			1.53		
					Rising	3.3V ± 0.3V		1.31		
					Falling			1.53		
					Rising	5V ± 0.5V		1.31		
					Falling			1.53		
t_{pd}	Delay	4-bit LUT	IN	OUT	Rising	1.8V ± 0.09V		1.53		ns
					Falling			1.86		
					Rising	3.3V ± 0.3V		1.53		
					Falling			1.86		
					Rising	5V ± 0.5V		1.53		
					Falling			1.86		
t_{pd}	Delay	DFF/Latch	CLK	Q	Rising	1.8V ± 0.09V		1.42		ns
					Falling			1.44		
					Rising	3.3V ± 0.3V		1.42		
					Falling			1.44		
					Rising	5V ± 0.5V		1.42		
					Falling			1.44		

5.7 Switching Characteristics (continued)

T_A = 25°C (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Delay	DFF/Latch	nRST/nSET	Q	Rising	1.8V ± 0.09V		1.58		ns
					Falling			1.58		
					Rising	3.3V ± 0.3V		1.58		
					Falling			1.58		
					Rising	5V ± 0.5V		1.58		
					Falling			1.58		
Counter/Delay										
t_{pd}	Delay	Counter - Delay mode	Rising edge of IN	Rising edge of OUT	Falling edge triggered	1.8V ± 0.09V		2.21		ns
			Falling edge of IN	Falling edge of OUT	Rising edge triggered			2.01		
			Rising edge of IN	Rising edge of OUT	Falling edge triggered	3.3V ± 0.3V		2.21		
			Falling edge of IN	Falling edge of OUT	Rising edge triggered			2.01		
			Rising edge of IN	Rising edge of OUT	Falling edge triggered	5V ± 0.5V		2.21		
			Falling edge of IN	Falling edge of OUT	Rising edge triggered			2.01		
t_{pw}	Pulse width	Counter - Edge detect mode	Rising edge of OUT	Falling edge of OUT	Rising edge detect	1.8V ± 0.09V		57.6		ns
						3.3V ± 0.3V		61.4		
						5V ± 0.5V		62.0		
					Falling edge detect	1.8V ± 0.09V		56.0		
						3.3V ± 0.3V		59.6		
						5V ± 0.5V		60.4		
					Both edge detect	1.8V ± 0.09V		55.9		
						3.3V ± 0.3V		59.7		
						5V ± 0.5V		60.5		
Oscillator										
f_{err}	Oscillator frequency error				OSC025 kHz	1.8V ± 0.09V	-5		5	%
						3.3V ± 0.3V	-5		5	
						5V ± 0.5V	-5		5	
					OSC0 2MHz	1.8V ± 0.09V	-5		5	%
						3.3V ± 0.3V	-5		5	
						5V ± 0.5V	-5		5	
t_{d_osc}	Oscillator startup delay				OSC025 kHz	1.8V ± 0.09V		11.5		µs
						3.3V ± 0.3V		10.5		
						5V ± 0.5V		9.9		
					OSC0 2MHz	1.8V ± 0.09V		3.3		µs
						3.3V ± 0.3V		2.7		
						5V ± 0.5V		2.5		

5.7 Switching Characteristics (continued)

T_A = 25°C (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{set_osc}	Oscillator startup settling time				OSC025 kHz	1.8V ± 0.09V		1		µs
						3.3V ± 0.3V		1		
						5V ± 0.5V		1		
					OSC0 2MHz	1.8V ± 0.09V		7		µs
						3.3V ± 0.3V		7		
						5V ± 0.5V		7		
t_{d_err}	Delay error				OSC (Forced power on)	1.71V to 5.5V	0		1	CLK cycle
Programmable Filter										
t_{pflt_pw}	Pulse width	Programmable filter - Edge detect mode	Rising edge of OUT	Falling edge of OUT	1 cell	1.8V ± 0.09V		154.0		ns
						3.3V ± 0.3V		157.3		
						5V ± 0.5V		158.7		
					2 cells	1.8V ± 0.09V		256.2		ns
						3.3V ± 0.3V		259.7		
						5V ± 0.5V		260.8		
					3 cells	1.8V ± 0.09V		356.2		ns
						3.3V ± 0.3V		360.3		
						5V ± 0.5V		361.5		
					4 cells	1.8V ± 0.09V		455.3		ns
						3.3V ± 0.3V		459.6		
						5V ± 0.5V		461.4		
t_{pflt_pd}	Delay	Programmable filter - Edge detect mode			Any cells	1.8V ± 0.09V		22.0		ns
						3.3V ± 0.3V		21.4		
						5V ± 0.5V		21.3		
t_{pflt_d}	Delay	Programmable filter - Both edge delay mode	Rising/Falling edge of IN	Rising/Falling edge of OUT	1 cell	1.8V ± 0.09V		176.0		ns
						3.3V ± 0.3V		178.7		
						5V ± 0.5V		161.0		
					2 cells	1.8V ± 0.09V		278.2		ns
						3.3V ± 0.3V		281.1		
						5V ± 0.5V		282.1		
					3 cells	1.8V ± 0.09V		378.2		ns
						3.3V ± 0.3V		352.1		
						5V ± 0.5V		382.8		
					4 cells	1.8V ± 0.09V		477.3		ns
						3.3V ± 0.3V		481.0		
						5V ± 0.5V		482.7		

5.8 Typical Characteristics

T_A = 25°C

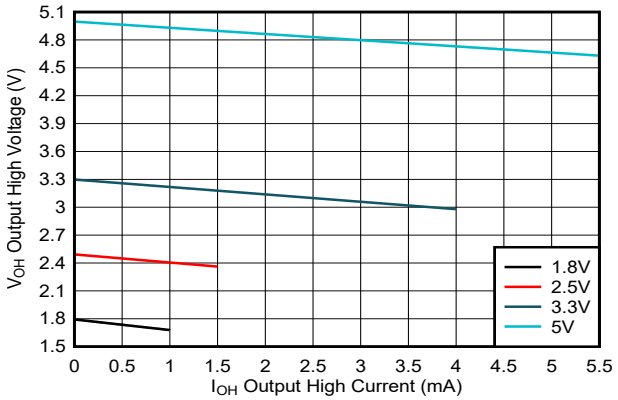


Figure 5-1. Typical 1X Push-Pull Output Voltage in the High State (V_{OH})

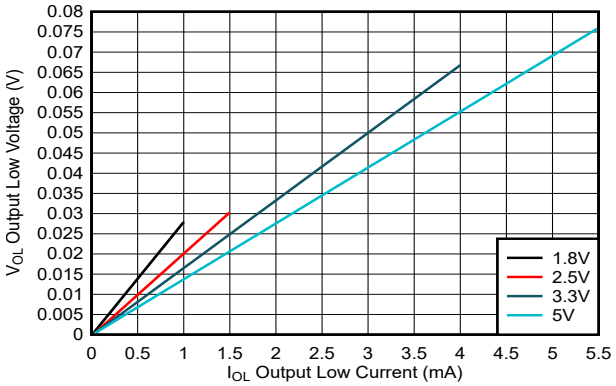


Figure 5-2. Typical 1X Push-Pull Output Voltage in the Low State (V_{OL})

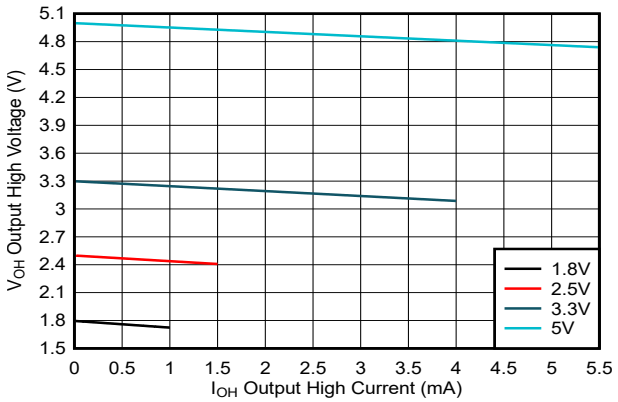


Figure 5-3. Typical 2X Push-Pull Output Voltage in the High State (V_{OH})

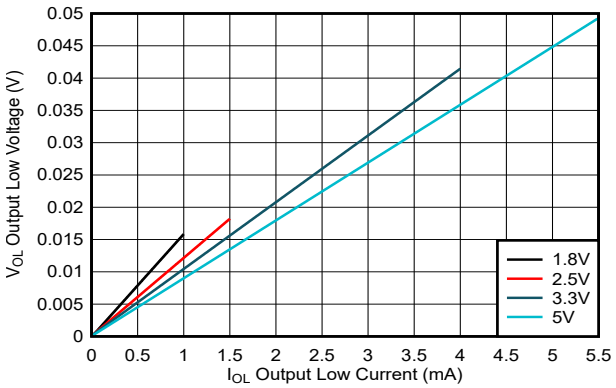


Figure 5-4. Typical 2X Push-Pull Output Voltage in the Low State (V_{OL})

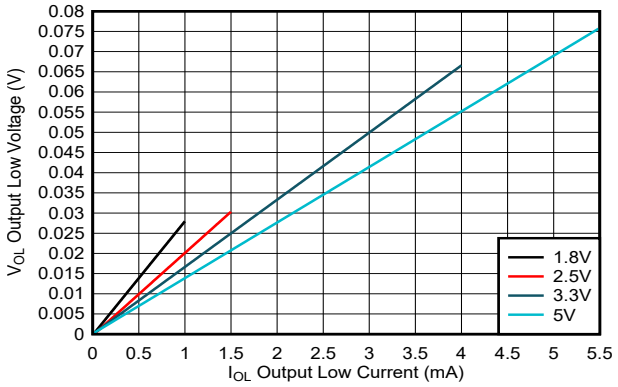


Figure 5-5. Typical 1X Open-Drain NMOS Output Voltage in the Low State (V_{OL})

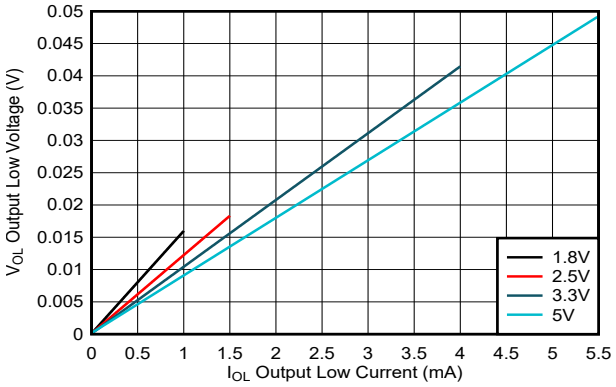


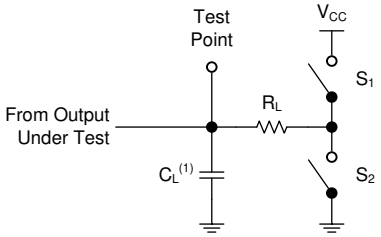
Figure 5-6. Typical 2X Open-Drain NMOS Output Voltage in the Low State (V_{OL})

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

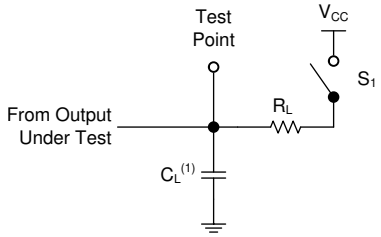
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



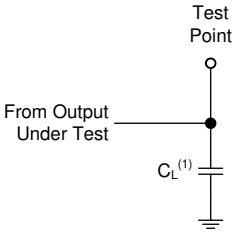
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 6-2. Load Circuit for Open-Drain Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 6-3. Load Circuit for Push-Pull Outputs

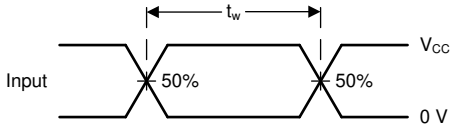


Figure 6-4. Voltage Waveforms, Pulse Duration

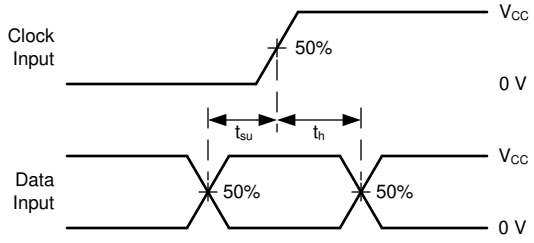
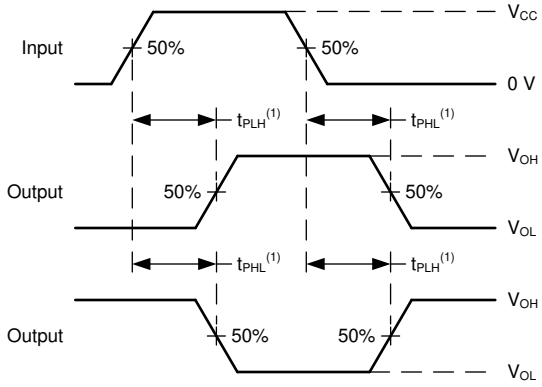


Figure 6-5. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-6. Voltage Waveforms Propagation Delays

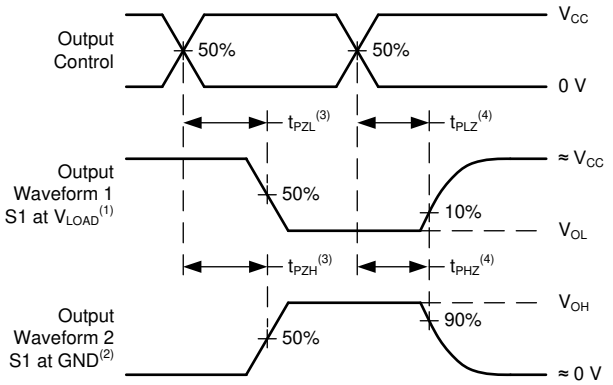
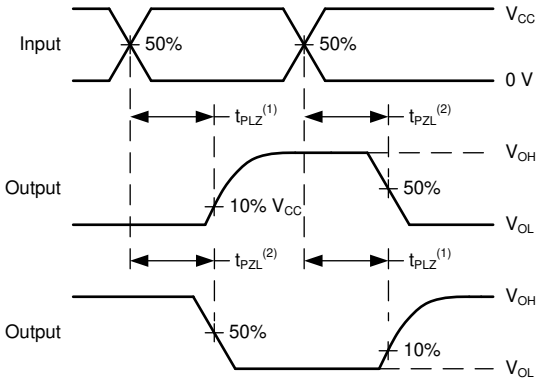
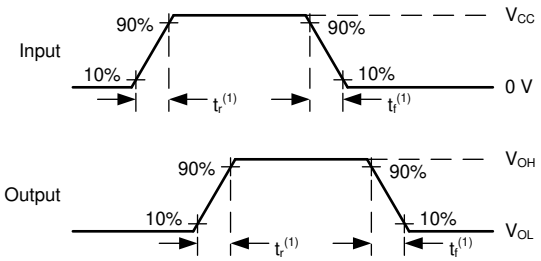


Figure 6-7. Voltage Waveforms Propagation Delays



(1) The greater between t_{PLZ} and t_{PZL} is the same as t_{pd}.

Figure 6-8. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-9. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The TPLD1201-Q1 is part of the TI programmable logic device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic, and analog blocks to provide an integrated, compact, low power solution to implement common system functions.

The TPLD1201-Q1 has one GPI and seven GPIOs that can be configured as a digital input, digital output, digital input or output, or analog input or output.

The TPLD1201-Q1 has a system of interconnects, further referred to as the connection mux, to configure the routing of internal macro-cells and I/O pins. Each connection mux input is hardwired to a specific digital macro-cell output, such as digital I/O, lookup tables, and analog comparator outputs. The connection mux allows each of the digital inputs to only connect to one output so that bus contention does not occur.

The TPLD1201-Q1 features the following macro-cells:

- Configurable use logic blocks:
  - Two 2-bit lookup tables (LUT)
  - Two 3-bit LUTs
  - Two 2-bit LUTs or D-type flip-flops (DFF) or latches
  - Two 3-bit LUTs or DFF or latches with reset/set option
  - One 3-bit LUT or Pipe delay
  - One 4-bit LUT or 8-bit counter (CNT) or delay generator (DLY)
- Three 8-bit CNT/DLYs
- One programmable deglitch filter (PFLT) or edge detector (EDET)
- One oscillator (OSC) to generate either a 25kHz or 2MHz clock
- Two analog comparators (ACMP)
- Voltage reference (VREF) with option to output to analog IO

The InterConnect Studio software environment enables a simple drag-and-drop interface to build custom circuit designs and configure the macro-cells, I/O pins, and interconnections. In addition to circuit creation, InterConnect Studio has the ability to simulate digital and analog functionality to verify designs and provide a typical power consumption estimate. Once circuit designs are finalized, InterConnect Studio can temporarily emulate the design in the non-volatile memory or permanently program the one-time programmable (OTP). The OTP can be locked to prevent readback of its contents.

7.2 Functional Block Diagram

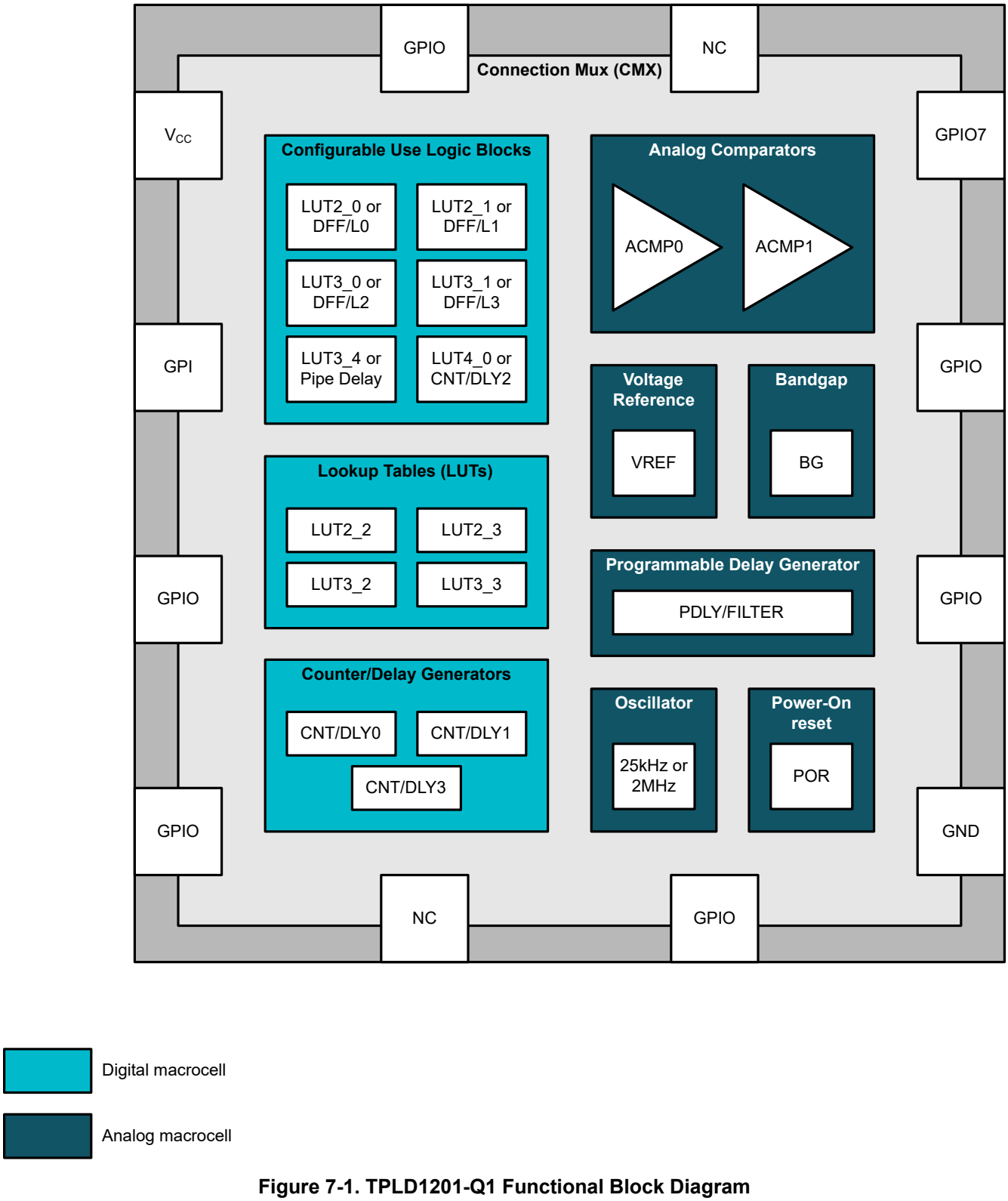


Figure 7-1. TPLD1201-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 I/O Pins

TPLD1201-Q1 has one input and seven multifunction I/O pins. GPIO pins can function as either a user defined input, output, or a special function.

7.3.1.1 Input Modes

The following options are available when configuring pins as an input:

- Digital input without Schmitt-trigger
- Digital input with Schmitt-trigger
- Low-voltage digital input

The low-voltage digital input has lower V_{IH}/V_{IL} specifications than the digital input without Schmitt trigger. This allows for up-translation from any voltage domain lower than V_{CC} that meets the low-voltage digital input V_{IH} and V_{IL} specifications.

The following pins also have the option to operate as a special function:

- IO9: external clock input
- IO1: positive input of analog comparator 0
- IO2: negative input of analog comparators
- IO4: positive input of analog comparator 1
- IO7: internal voltage reference output

7.3.1.2 Output Modes

The following options are available with programmable drive strengths when configuring pins as an output:

- Push-pull output
- Open-drain NMOS output
- Open-drain PMOS output

7.3.1.3 Pull-Up or Pull-Down Resistors

All I/O pins have the option of user-selectable resistors that can be connected to the pin structure. The selectable values on these resistors are 10kΩ, 100kΩ and 1MΩ. The internal resistors can be configured as either pull-up or pull-down. When designing in InterConnect Studio, any pin left unused in a design are configured with a 1MΩ pull-down by default. Furthermore, following a power-on event, all ports are in a Hi-Z state until the power-on reset sequence has completed.

Table 7-1. Pin Configuration Options

GPIO	IO Selection	OE	IO Options	Resistor	Resistor Value
IN0	PIN not used	—	—	Pull-Down	1MΩ
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Down	10kΩ
					100kΩ
					1MΩ
NOTE: GPI/IN0 also has the option to reset the device while powered on. Unlike POR, External Reset will only reset the internal logic and routing, inputs, and outputs. The NVM retains its previous state. If GPI Reset is enabled, ensure the input mode is set to Digital Input without Schmitt trigger. Users may select whether the External Reset is *Disabled*, *Level sensitive*, or *Edge triggered*. When *Level sensitive* is selected, if the input is High, then the device is in reset mode where all internal devices are reset. When this pin goes Low, then the device will begin the reset power on sequence. When *Edge triggered* is selected, the edge detector can be configured to Rising edge or Falling edge, and an edge on GPI/IN0 resets the device and begins the reset power on sequence.					

Table 7-1. Pin Configuration Options (continued)

GPIO	IO Selection	OE	IO Options	Resistor	Resistor Value
IO1, IO2	Pin not used	—	—	Pull Down	1MΩ
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ
	Digital output	1	Push-pull (1X, 2X)	Floating	—
			Open-drain NMOS (1X, 2X) Open-drain PMOS (1X, 2X)	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ
	Digital input/output	0	Analog input	—	—
		1	Open-drain NMOS (1X, 2X)	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ
	Analog input/output	—	Analog input/output	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ

Table 7-1. Pin Configuration Options (continued)

GPIO	IO Selection	OE	IO Options	Resistor	Resistor Value
IO4, IO7	Pin not used	—	—	Pull-Down	1MΩ
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ
	Digital output	1/0	Push-pull (1X, 2X)	Floating	—
			Open-drain NMOS (1X, 2X) 3-state output (1X, 2X)	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ
	Digital input/output	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input Analog input (IO4 only)	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ
		1	Push-pull (1X, 2X) Open-drain NMOS (1X, 2X)	Shared with above	
	Analog input/output	—	Analog input/output	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ

Table 7-1. Pin Configuration Options (continued)

GPIO	IO Selection	OE	IO Options	Resistor	Resistor Value
IO5, IO6, IO9	Pin not used	—	—	Pull Down	1MΩ
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ
	Digital output	1	Push-pull (1X, 2X)	Floating	—
			Open-drain NMOS (1X, 2X) Open-drain PMOS (1X, 2X)	Floating	—
				Pull-Up	10kΩ
					100kΩ
					1MΩ
				Pull-Down	10kΩ
					100kΩ
					1MΩ

7.3.2 Connection Mux

The TPLD1201-Q1 has a system of interconnects, referred to as the connection mux, to configure the routing of internal macro-cells and I/O pins. The connection mux has 32 inputs and 44 outputs. Each of the 32 inputs of the connection mux is hardwired to particular macro-cells, including I/O pins, LUTs, analog comparators, other digital resources, VCC, and GND. The input to a digital macro-cell uses a 5-bit register to select one of these 32 input lines.

7.3.3 Configurable Use Logic Blocks

Combinational logic is supported through lookup tables (LUTs) within the TPLD1201-Q1 including two 2-bit LUTs and two 3-bit LUTs. Inputs and outputs for the combination function macro-cells are configured from the connection mux with specific logic functions being defined by the state of OTP bits.

The TPLD1201-Q1 has seven combinational function blocks (macro-cells) that can serve more than one logic or timing function. In each case, they can serve as a lookup table (LUT), or as another logic or timing function. See the following list for the functions that can be implemented in these logic blocks:

- Two 2-bit LUTs
- Two 3-bit LUTs
- Two 2-bit LUTs or D-type flip-flops or latches
- Two 3-bit LUTs or D-type flip-flops or latches with reset/set option
- One 3-bit LUT or Pipe delay
- One 4-bit LUT or 8-bit counter or delay generator

7.3.3.1 2-Bit LUT Macro-Cell

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection mux and produces a single output, which goes back into the connection mux.

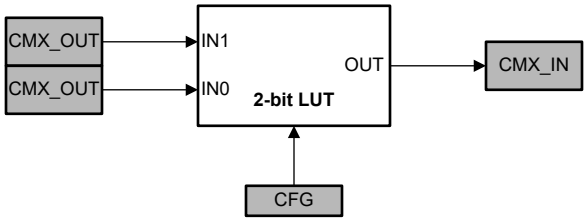


Figure 7-2. 2-Bit LUT Block Diagram

These LUTs can be configured to any 2-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-2 provides the truth table for a 2-bit LUT.

Table 7-2. 2-Bit LUT Truth Table

IN1	IN0	OUT
0	0	User defined
0	1	
1	0	
1	1	

Each 2-bit LUT has 4 bits in the OTP to define their output function.

7.3.3.2 3-Bit LUT Macro-Cell

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection mux and produces a single output, which goes back into the connection mux.

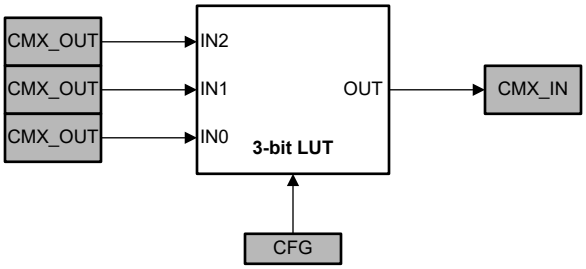


Figure 7-3. 3-Bit LUT Block Diagram

These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-3 provides the truth tables for a 3-bit LUT.

Table 7-3. 3-Bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	User defined
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Each 3-bit LUT has 8 bits in the OTP to define their output function.

7.3.3.3 2-Bit LUT or D Flip-Flop or Latch Macro-Cell

This configurable use logic block can serve as either a 2-bit LUT, or as a D flip-flop/latch.

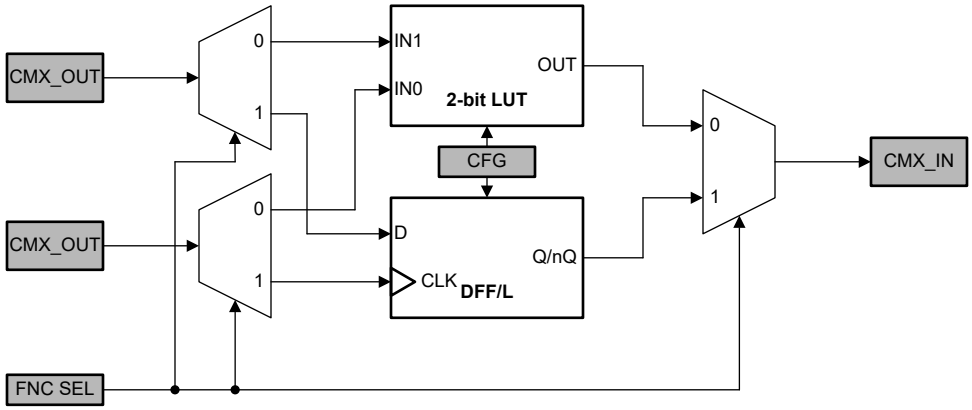


Figure 7-4. 2-Bit LUT or DFF or Latch Block Diagram

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection mux and produces a single output, which goes back into the connection mux. These LUTs can be configured to any 2-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-4 provides the truth table for a 2-bit LUT.

Table 7-4. 2-Bit LUT Truth Table

IN1	IN0	OUT
0	0	User defined
0	1	
1	0	
1	1	

Each 2-bit LUT has 4 bits in the OTP to define their output function.

When used to implement a sequential logic element, the two input signals from the connection mux go to the data (D) and clock (CLK) inputs of the flip-flop/latch, with the output going back to the connection mux. This macro-cell has initial state parameters, as well as clock and output polarity parameters.

The operation of the D flip-flop/latch will follow the following functional descriptions:

- The clock polarity is configurable and can be set to non-inverted (CLKPOL = 0, CLK) or inverted (CLKPOL = 1, nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q will not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is Low).
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 7-5 and Table 7-6 provides the truth tables for the D flip-flop and D latch, respectively.

Table 7-5. D Flip-Flop Truth Table

CLKPOL	CLK	D	Q	nQ
0	↓	0	Q_0	nQ_0
	↑	0	0	1
	↓	1	Q_0	nQ_0
	↑	1	1	0
1	↓	0	0	1
	↑	0	Q_0	nQ_0
	↓	1	1	0
	↑	1	Q_0	nQ_0

Table 7-6. D Latch Truth Table

CLKPOL	CLK	D	Q	nQ
0	0	0	0	1
	1	0	Q_0	nQ_0
	0	1	1	0
	1	1	Q_0	nQ_0
1	0	0	Q_0	nQ_0
	1	0	0	1
	0	1	Q_0	nQ_0
	1	1	1	0

7.3.3.4 3-Bit LUT or D Flip-Flop or Latch with Set or Reset Macro-Cell

This configurable use logic blocks can serve as either a 3-bit LUT, or as a D flip-flop/latch with a reset/set.

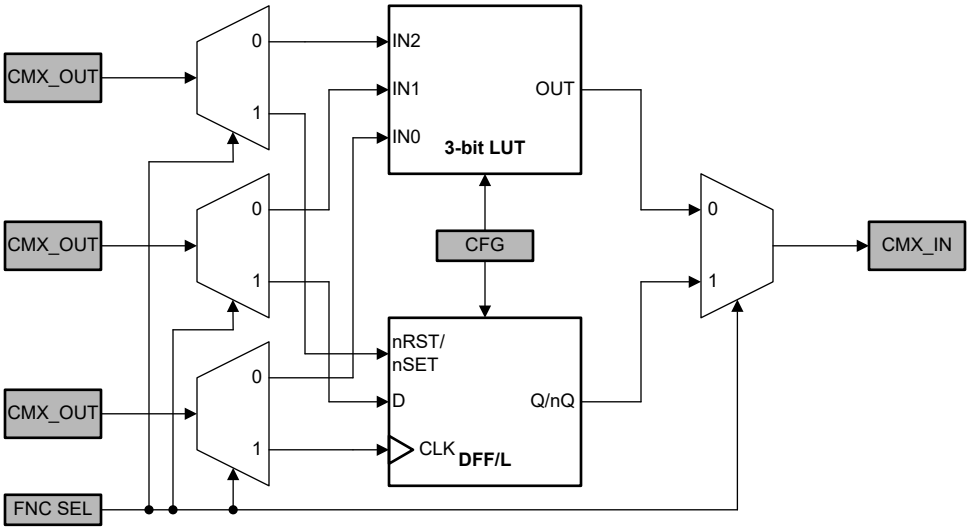


Figure 7-5. 3-Bit LUT or DFF or Latch with nRST or nSET Block Diagram

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection mux and produces a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-7 provides the truth table for a 3-bit LUT.

Table 7-7. 3-Bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	User defined
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Each 3-bit LUT has 8 bits in the OTP to define their output function.

When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop/latch, with the output going back to the connection mux. This macro-cell has initial state, clock polarity, reset/set polarity, and output polarity parameters.

The operation of the D flip-flop/latch will follow the following function descriptions:

- The clock polarity is configurable and can be set to non-inverted (CLKPOL = 0, CLK) or inverted (CLKPOL = 1, nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q will not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is Low).
- These DFF/latches have an option for an active-low reset/set.
  - nRST: when the input is high, the DFF/latch is in normal operation; and when low, Q is reset to 0.
  - nSET: when the input is high, the DFF/latch is in normal operation; and when low, Q is set to 1.
- If reset/set is not desired, users may tie this input to V_{CC} or another constant high source.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 7-8 and Table 7-9 provides the truth tables for the D flip-flop and D latch with reset/set, respectively.

Table 7-8. D Flip-Flop With nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	Q_0	nQ_0
			↑	0	0	1
			↓	1	Q_0	nQ_0
			↑	1	1	0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	0	1
			↑	0	Q_0	nQ_0
			↓	1	1	0
			↑	1	Q_0	nQ_0

Table 7-9. D Latch With nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		0	0	0	1
			1	0	Q_0	nQ_0
			0	1	1	0
			1	1	Q_0	nQ_0

Table 7-9. D Latch With nRST/nSET Truth Table (continued)

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		0	0	Q_0	nQ_0
			1	0	0	1
			0	1	Q_0	nQ_0
			1	1	1	0

7.3.3.5 3-Bit LUT or Pipe Delay Macro-cell

This macro-cell can serve as either a 3-bit LUT or as a pipe delay.

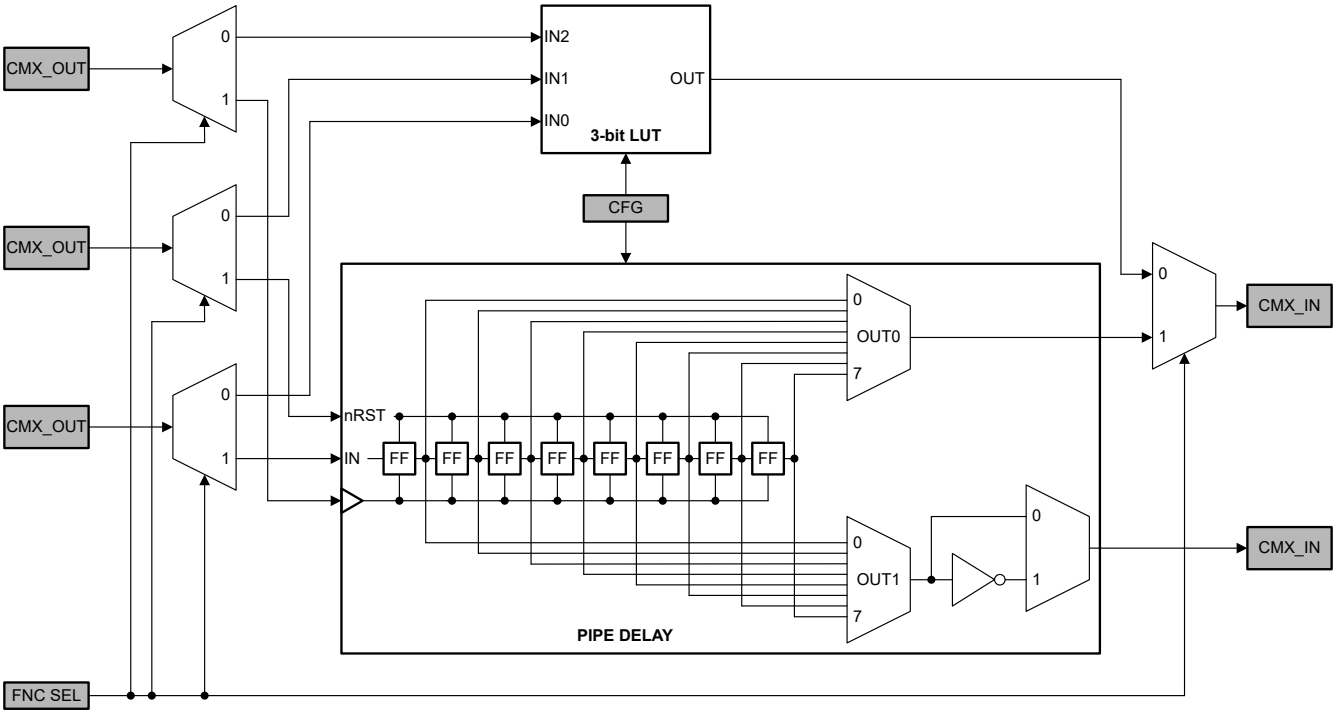


Figure 7-6. 3-Bit LUT or Pipe Delay Block Diagram

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection mux and produces a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-10 provides the truth table for a 3-bit LUT.

Table 7-10. 3-Bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	User defined
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Each 3-bit LUT has 8 bits in the OTP to define their output function.

When used to implement a pipe delay, the three input signals from the connection mux go to the delay input (IN), clock (CLK), and reset (nRST) inputs for the flip-flop/latch, with two outputs going back to the connection mux. With this macro-cell, users can select the number of delay stages per output (from 1 to 8) and the output polarity for OUT1.

The pipe delay is an 8-stage delay composed of 8 DFFs. The DFF cells are tied in series where the output of each delay cell goes to the next DFF cell. There are delay output points for each set of the OUT0 and OUT1 outputs to a mux that is used to control the selection of the amount of delay for each pipe delay output.

For normal pipe delay functionality, the nRST input should be high. If nRST input is low, the pipe delay macro-cell is in a reset state and all outputs are low.

Figure 7-7 shows an example of the pipe delay macro-cell with 2 stages of delay selected.

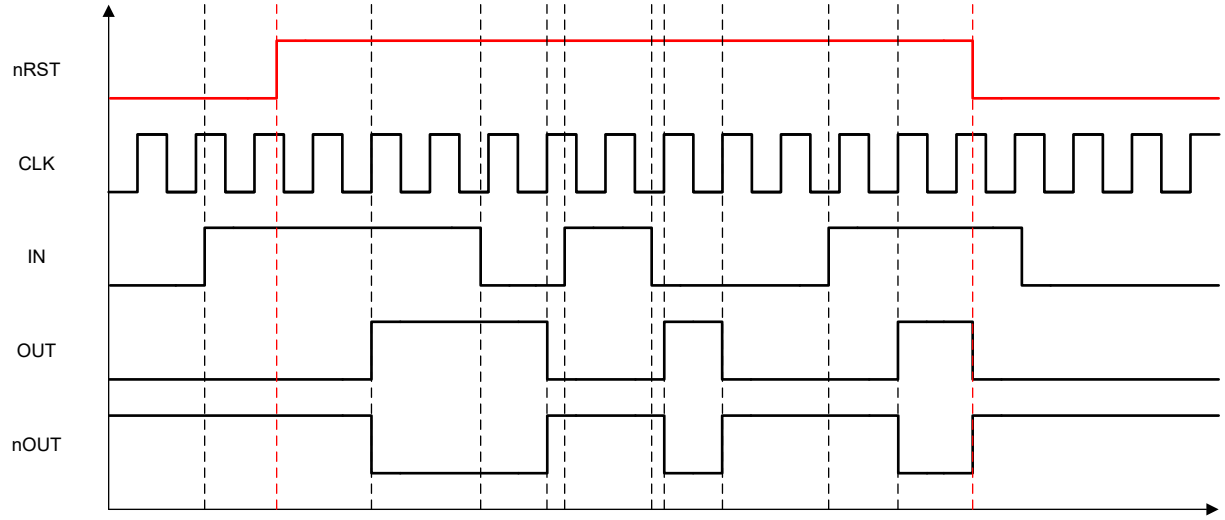


Figure 7-7. Pipe Delay Macro-Cell Timing Example (Delay = 2)

7.3.3.6 4-Bit LUT or 8-Bit Counter or Delay Macro-Cell

This macro-cell can serve as either a 4-bit LUT or as a counter/delay generator (CNT/DLY).

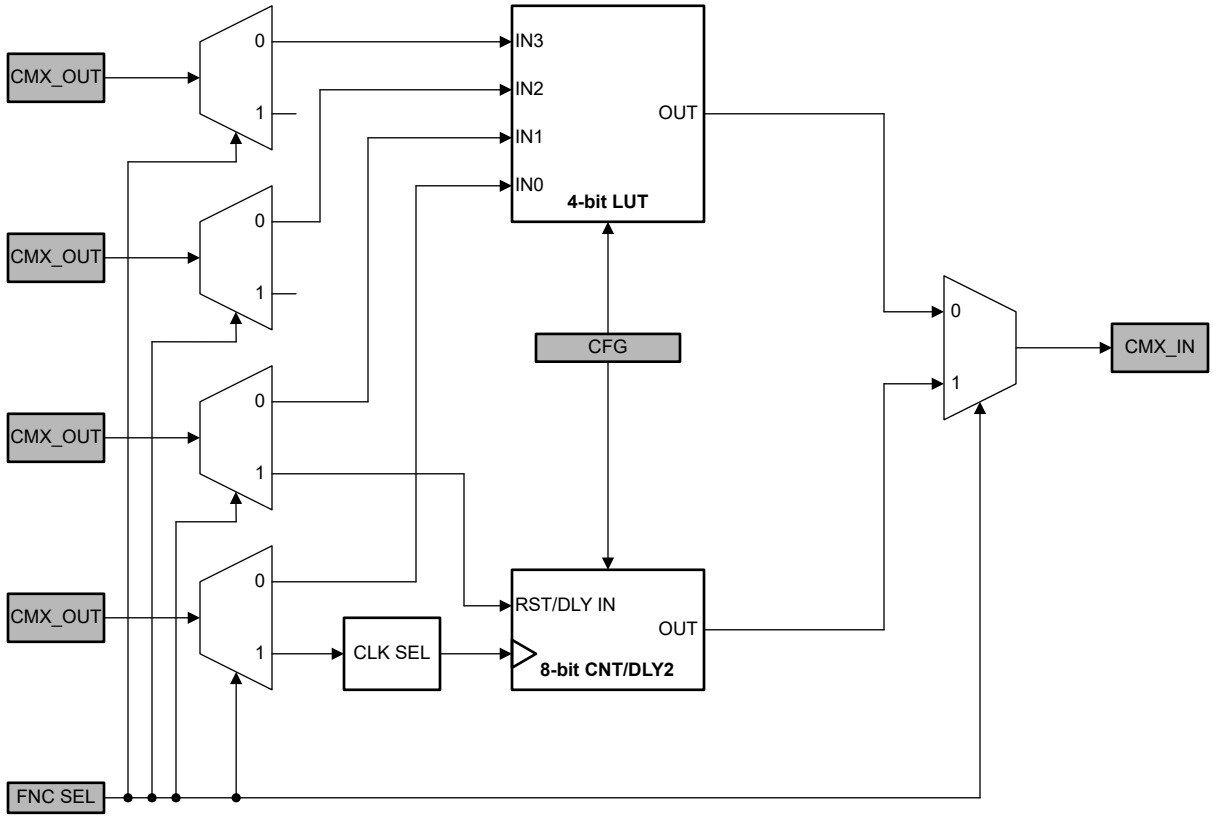


Figure 7-8. 4-Bit LUT or 8-Bit CNT/DLY Block Diagram

When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection mux and produces a single output, which goes back into the connection mux. This LUT can be configured to any 4-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-11 provides the truth table for a 4-bit LUT.

Table 7-11. 4-Bit LUT Truth Table

IN3	IN2	IN1	IN0	OUT
0	0	0	0	User defined
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Each 4-bit LUT has 16 bits in the OTP to define their output function.

When used to implement 8-bit counter/delay function, the two input signals from the connection mux go to the clock (CLK) and reset (RST/DLY IN) for the counter/delay macro-cell, with the output going back to the connection mux. As a counter, the macro-cell counts to the given data value and generates a pulse when it reaches the set value or is reset. As a delay, it postpones rising or falling edges for the duration that is a function of the register value.

For more information on CNT/DLY macro-cell, see Section 7.3.4.

7.3.4 8-Bit Counters and Delay Generators (CNT/DLY)

The counters/delay generators are 8-bit, supporting counter data values from 1 to 255. For flexibility, the clock source for each of these macro-cells can be configured as the internal oscillator, a divided clock derived from an oscillator (OSC/4, /12, /24, /64, /4096), or an external clock source coming from the connection mux. There is also the option to chain from the output of the previous CNT/DLY macro-cell to implement longer counter/delay circuits. Note that the counter/delay macro-cell is rising edge triggered, that is the counter will increment/decrement on rising clock edges.

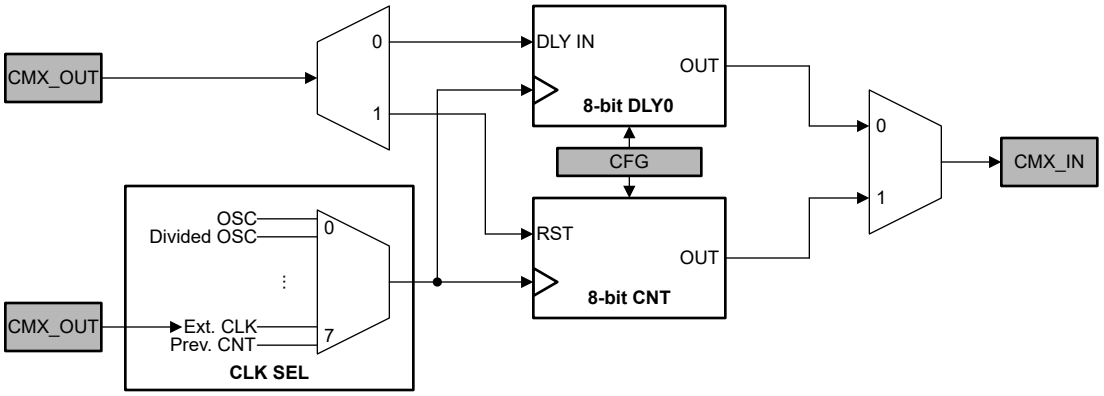


Figure 7-9. CNT/DLY Block Diagram

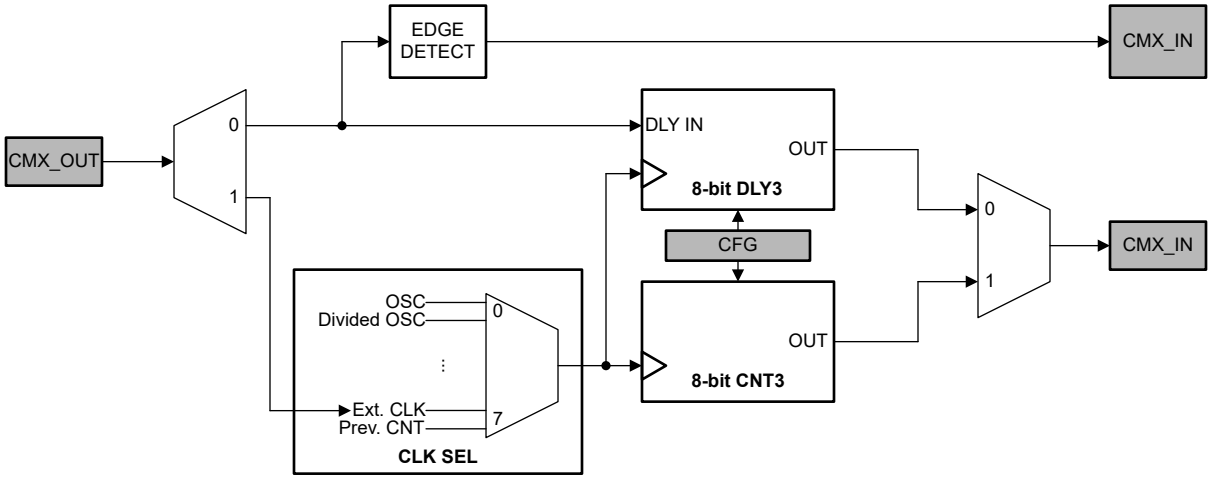


Figure 7-10. CNT/DLY3 Block Diagram

As a counter/delay (CNT/DLY) macro-cell, users may select from the following modes: delay, counter.

CNT/DLY3, when in Delay mode, also has an optional edge detector that will generate a short pulse on the specified edge in addition to the delayed output.

7.3.4.1 Delay Mode

When configured as a Delay generator (DLY), this macro-cell delays the input based on counter DATA and CLK input frequency and postpones rising and/or falling edges. The initial output value of this macro-cell after device startup can also be configured to Bypass Initial, Initial Low, or Initial High. The edge on which to delay is selected by the Edge select parameter and can be configured as:

- Rising: only delay on rising edges of IN.
- Falling: only delay on falling edges of IN.
- Both: delay on both rising and falling edges of IN.

For delay applications, it is recommended to use larger counter data values for less error. If an input pulse width is shorter than the specified delay time, the pulse will be filtered out. This feature can be useful for deglitching.

If the on-chip oscillator is used, a delay error or offset is introduced depending on whether the OSC is set to "forced power on" or "auto power on". An additional 2 clock cycles are included in the delay calculation for clock synchronization.

The delay time is calculated by DELAY = (DATA + (t_{d_err} or t_{d_os}) + 3)/f_{CLK}.

When the OSC is set to "auto power on" and DLY macro-cells are triggered subsequently before the previous output is present, the OSC will continue to clock and the DLY will begin on the next rising edge. Thus, the subsequent delays can be calculated as if the OSC were set to "forced power on".

Figure 7-11 shows an example of the Delay macro-cell operation set to both edge delay and data = 1.

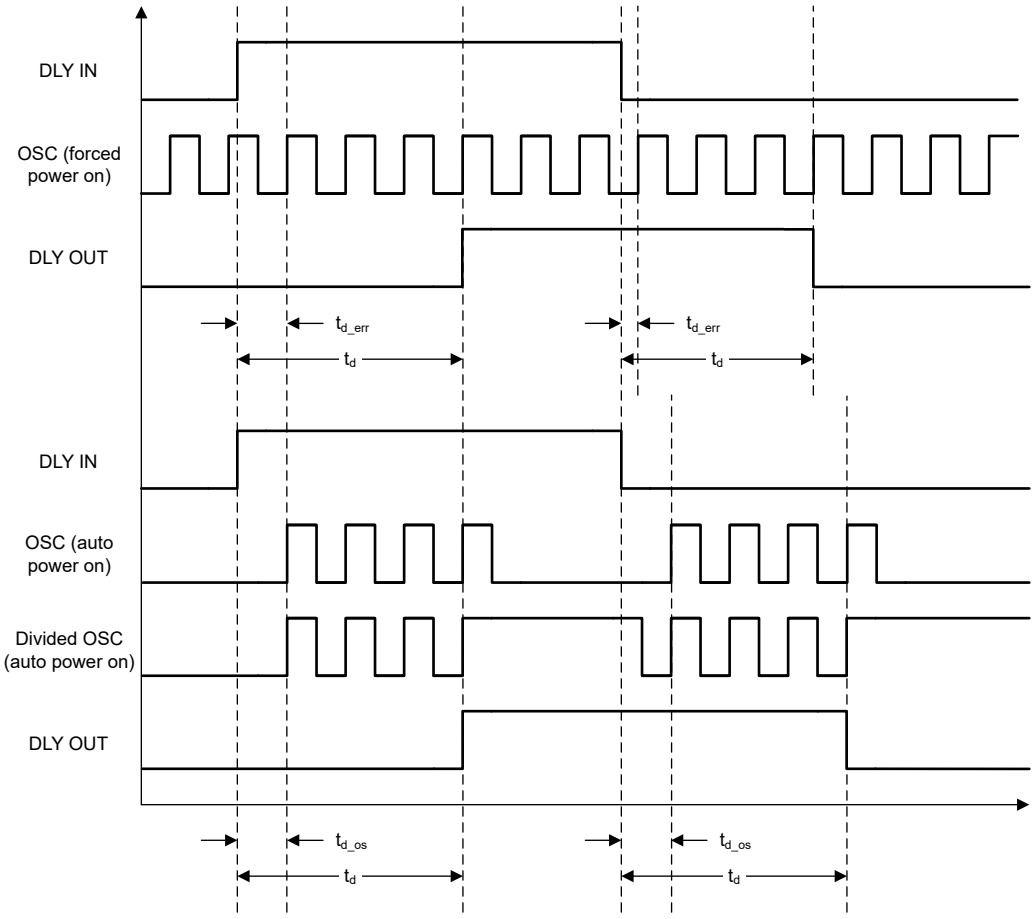


Figure 7-11. Delay Output Timing Example (Both Edge Delay and DATA = 1)

Figure 7-12 shows an example timing of Delay macro-cells with respect to the edge selected and data = 3.

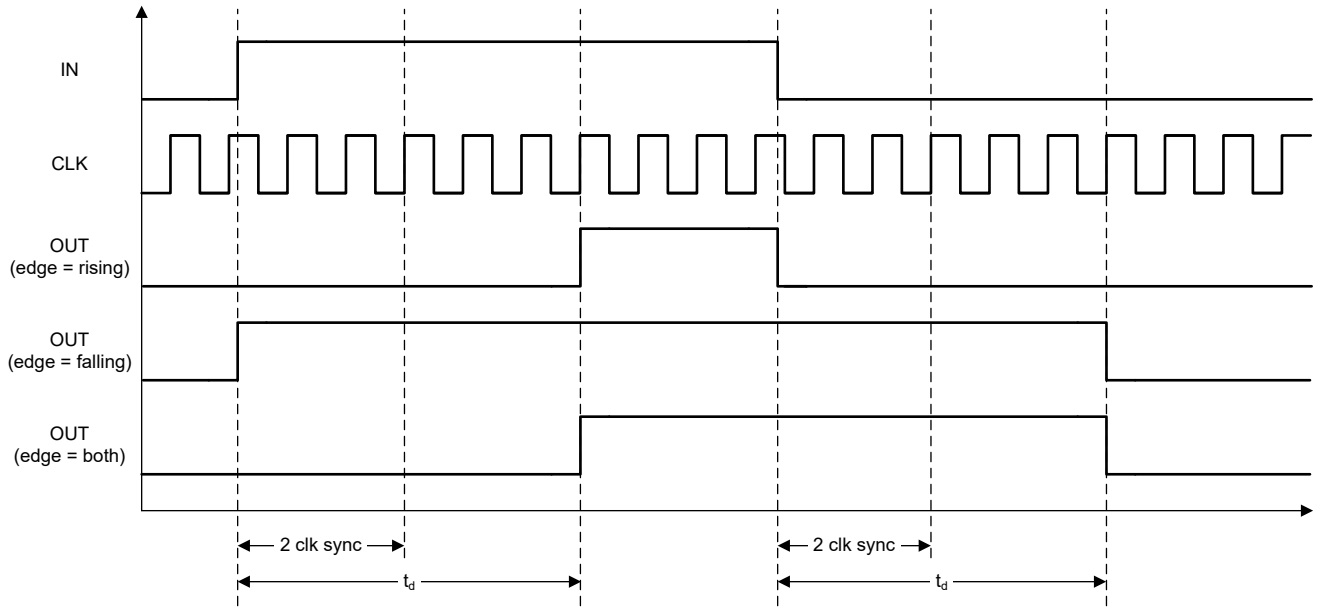


Figure 7-12. Delay Output Timing Example (DATA = 3)

7.3.4.2 Edge Detector Mode

When CNT/DLY3 is configured as a Delay, this macro-cell has the option to generate a pulse of approximately 20ns width when a valid edge is detected. The edge on which the Edge detector generates a pulse is determined by the Edge select parameter and can be configured as:

- Rising: only rising edges of IN generate a pulse.
- Falling: only falling edges of IN generate a pulse.
- Both: both rising and falling edges of IN generate a pulse.

The image below shows an example of how the EDET option operates with respect to the Edge select parameter.

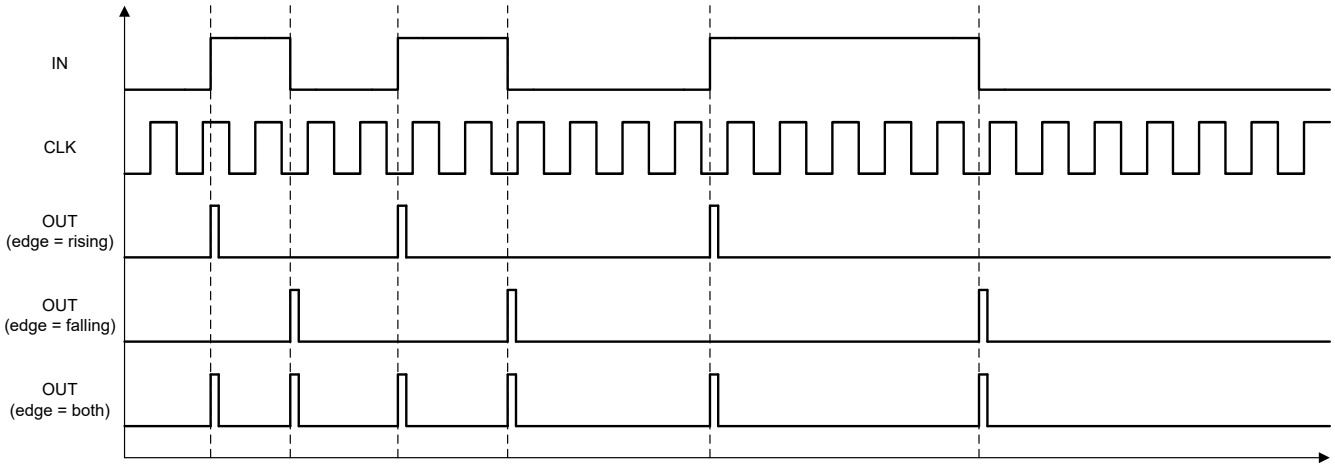


Figure 7-13. Edge Detector Output Timing Example

7.3.4.3 Reset Counter Mode

When configured as a Counter (CNT) and a valid edge appears on the IN input, this macro-cells resets the internal counter to 0 and begins counting down from DATA on the next rising clock edge. Then, the macro-cell outputs a pulse for the duration of one CLK period when the count reaches 0 and wrap around to the value in DATA. The counter will continually operate until another reset is received. The edge on which the Counter is reset is determined by the Edge select parameter and can be configured as:

- Rising: only rising edges of IN reset the counter.
- Falling: only falling edges of IN reset the counter.
- Both: both rising and falling edges of IN reset the counter.
- High Level Reset: the counter is reset to 0 whenever IN is High; after reset, the counter output stays Low until the next rising CLK edge, then operates normally.

The counter time is calculated by COUNT = (DATA + 1)/f_{CLK}. After a reset, an additional 2 clock cycles is added for clock synchronization with an option to bypass. Note, bypassing the clock synchronization may result in the counter resetting to an unknown value.

Note

Counters are initialized with DATA = 0 after POR.

Figure 7-14 and Figure 7-15 show examples of Counter output timing diagrams with respect to the Edge select parameter with DATA = 1 and DATA = 3, respectively.

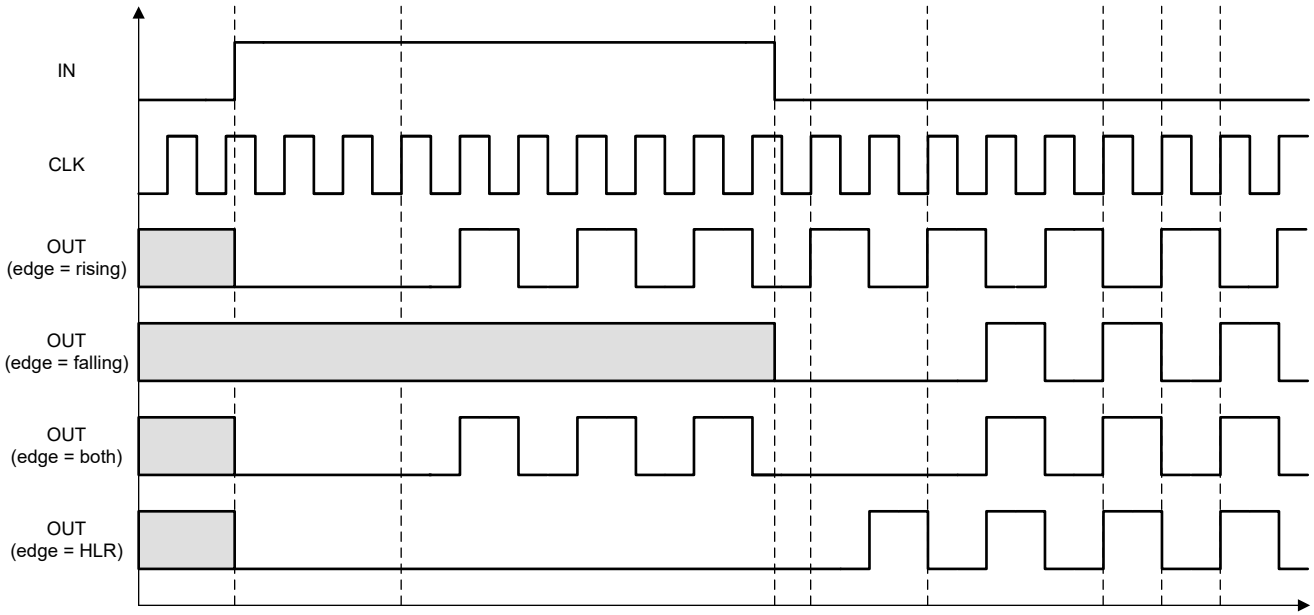


Figure 7-14. Counter Output Timing Example (DATA = 1)

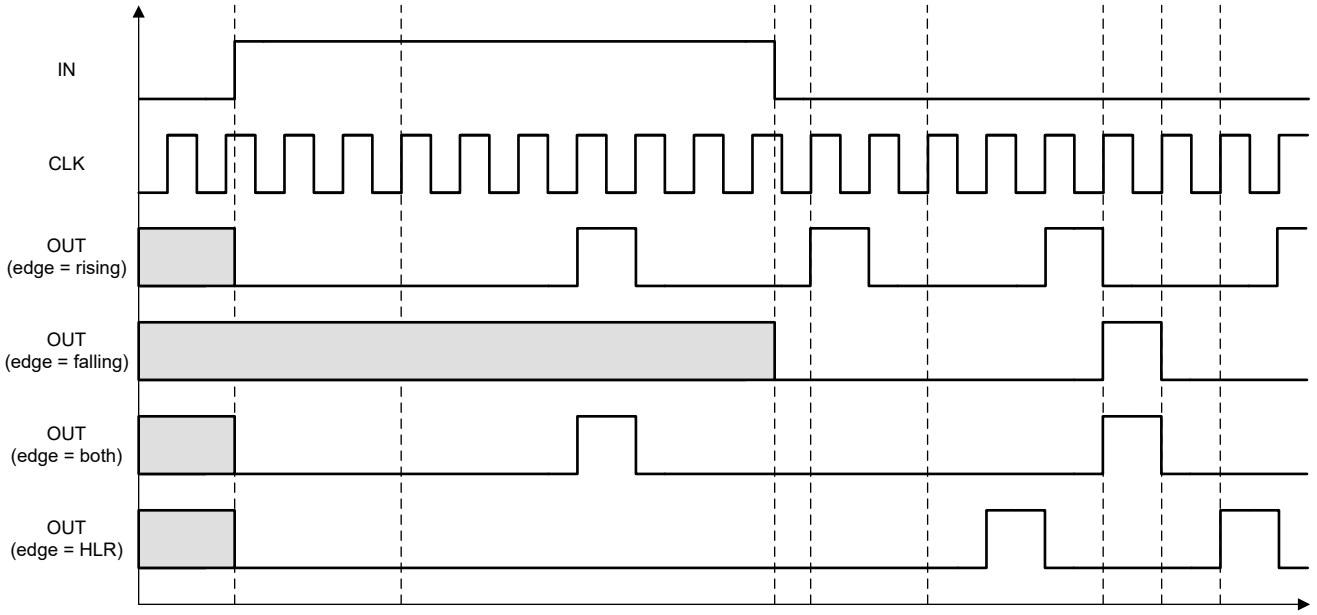


Figure 7-15. Counter Output Timing Example (DATA = 3)

Figure 7-16 shows an example of how the Counter macro-cell operates when the IN signal is shorter than the counter length (shown when edge select parameter is set to "both").

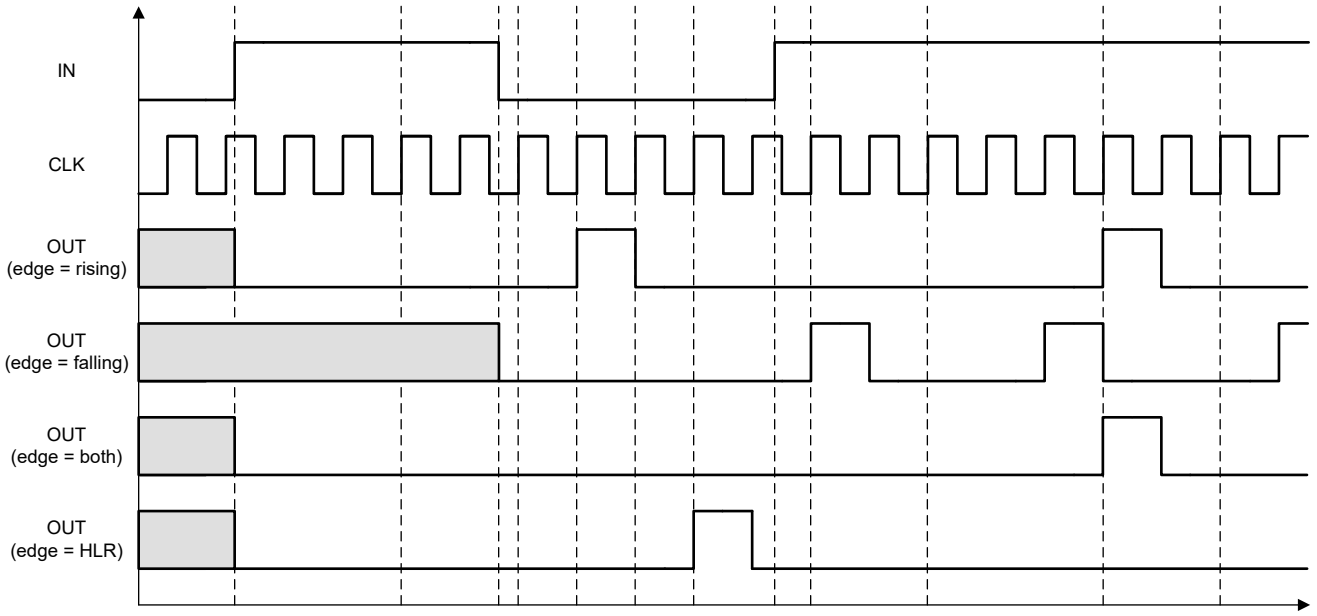


Figure 7-16. Counter Output Timing Example with RST < DATA (DATA = 3)

7.3.5 Programmable Deglitch Filter or Edge Detector Macro-Cell

The TPLD1201-Q1 has one macro-cell that can be configured as a programmable filter (PFLT) or edge detector (EDET). The PFLT macro-cell can be used to generate a delay (t_{pflt_d}) characterized by t_{pflt_pw} and t_{pflt_pd}. t_{pflt_pw} can be set to 125ns, 250ns, 375ns, or 500ns and t_{pflt_pd} is a fixed value. Furthermore, the output of the macro-cell can be configured to one of four options: rising edge detection, falling edge detection, both edge detection, or both edge delay. Lastly, the filter operates as a short low-pass filter and its output can be set as non-inverted or inverted.

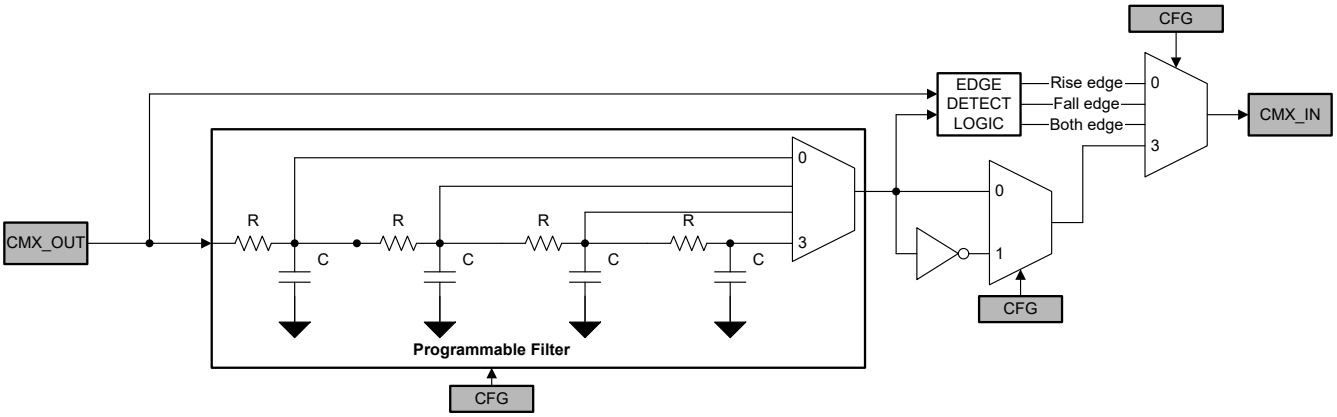


Figure 7-17. Programmable Filter and Edge Detector Block Diagram

Note

The input signal must be longer than t_{pflt_d}, otherwise it will be filtered out.

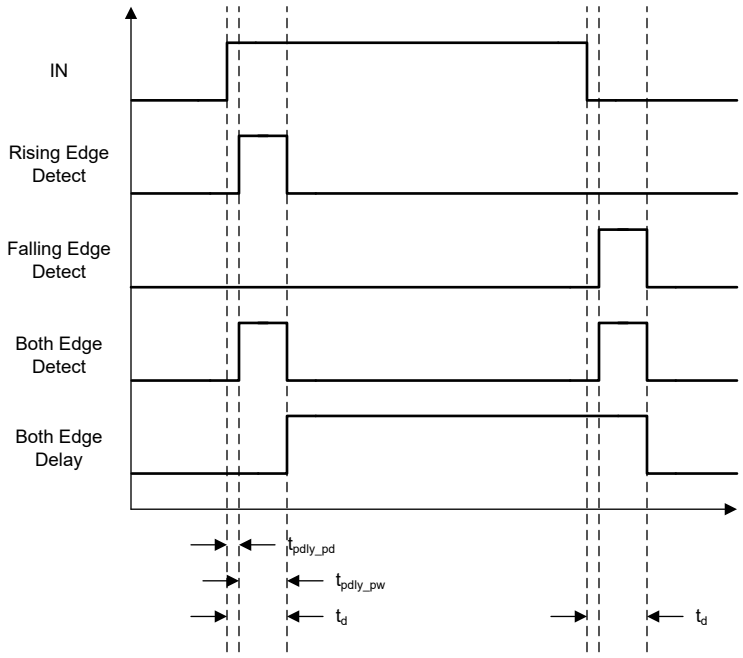


Figure 7-18. Programmable Filter and Edge Detector Output Timing Diagram Example

7.3.6 Selectable Frequency Oscillator

The TPLD1201-Q1 has one internal oscillator, selectable to operate at 25kHz or at 2MHz. The user can select one of these operating frequencies for the OSC macro-cell, or the internal oscillator could be bypassed and the operating frequency can come from an external clock.

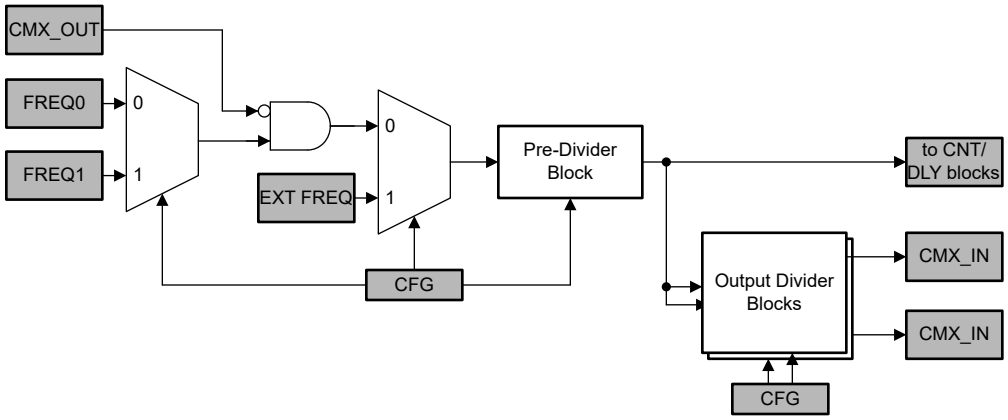


Figure 7-19. Oscillator Block Diagram

Following the operating clock input, there are two divider stages that allow users the flexibility of various clock frequencies for use throughout the device.

The first stage divider allows the selection of up to four options from the operating oscillator frequency as listed in *Oscillator Frequency Modes*. The output of the first divider stage is routed directly to the counter/delay generator macro-cell CLK inputs, where a separate second divider stage is available.

The output of the first divider stage is also routed into a second divider stage within the oscillator macro-cell. The oscillator macro-cell has two separate second stage dividers, allowing for the output of two separate clocks (OUT0 and OUT1) into the connection mux. See *Oscillator Frequency Modes*

7.3.6.1 Oscillator Power Modes

When using the device's internal oscillator, there are two configuration settings available:

- Force power on: the internal oscillator will continuously run as long as the device is powered on.
- Auto power on: the internal oscillator will dynamically power on when any macro-cell requests the oscillator directly from the pre-divider block output and not through the connection mux, and then power off once the task is complete.
- External power on/off: the internal oscillator will be powered down when PDWN is asserted High. PDWN signal takes priority over the oscillator power modes. This is only applicable when the internal oscillator is selected and is bypassed when an external clock is used.

Table 7-12. Frequency Options and Limits

Frequency Option	MIN	TYP	MAX
FREQ0	23.75kHz	25kHz	26.25kHz
FREQ1	1.9MHz	2MHz	2.1MHz
EXT	-	-	-

Table 7-13. Oscillator Pre-dividers

Pre-Divider Option	Magnitude
P0	1
P1	2
P2	4
P3	8

Table 7-14. Oscillator Output Dividers

Output Divider Options	Magnitude
OD0	1
OD1	2
OD2	3
OD3	4
OD4	8
OD5	12
OD6	24
OD7	64

7.3.7 Analog Comparators (ACMP)

There are two analog comparator (ACMP) macro-cells in the TPLD1201-Q1. The analog comparator compares two voltages (IN+ and IN-) and outputs a digital signal (OUT) indicating which input is larger, a High signal for IN+ and a Low for IN-.

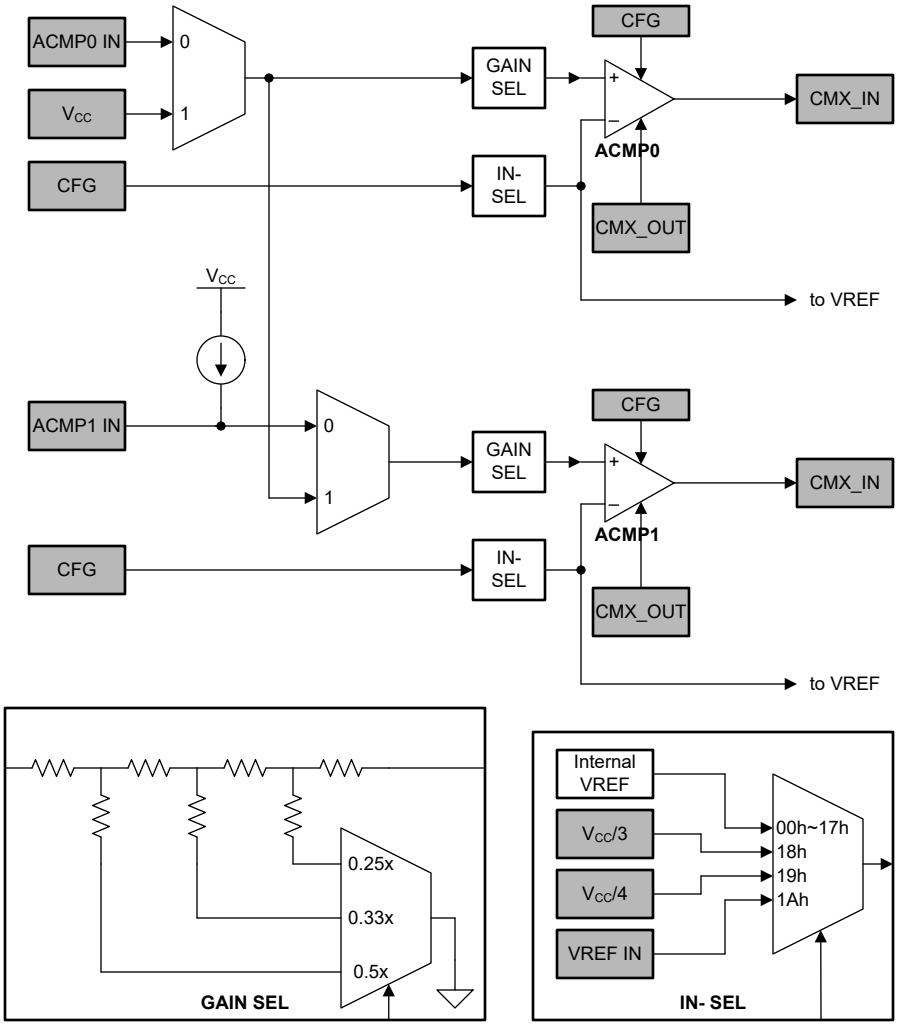


Figure 7-20. ACMP Block Diagram

For the ACMP macro-cell to operate, the power up signal (PWR UP) needs to be asserted high. By connecting to signals coming from the connection mux, it is possible to have each ACMP always on, always off, or switched on dynamically based on a digital signal coming from the connection mux. When powered down, the ACMP will output a low signal.

- PWR UP = 1: ACMP is powered up.
- PWR UP = 0: ACMP is powered down.

Upon power-up, the ACMP output will remain low, and then become valid 100µs (typical) after POR signal goes high. During this time, ensure the internal oscillator is not powered down.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources with a selectable gain stage before going into the analog comparator. ACMP1 also has a 100µA pullup current source option for external sensor excitation purposes. The negative input signal is either created from an internal VREF or from an external source.

Table 7-15. ACMP0 and ACMP1 Input Sources

Parameters	ACMP0(1)	ACMP1(2)
IN+ source	Analog Input 0 (shared with IO1)	Analog Input 1 (shared with IO4)
	V_{CC}	ACMP0 IN+
IN- source	150mV	150mV
	...	...
	1200mV	1200mV
	V_{CC}/3	V_{CC}/3
	V_{CC}/4	V_{CC}/4
	VREF Analog Input (shared with IO2)	VREF Analog Input (shared with IO2)

(1) Positive Analog input source to ACMP.
(2) Negative Analog input source to ACMP. Internal VREF thresholds are optimized near 1200mV.

IN+ gain: Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connection to the analog comparator.

IN- voltage range: 150mV to 1.2V through the internal VREF, V_{CC}/3, V_{CC}/4, or external source.

Hysteresis: Each ACMP has four selectable hysteresis options 0mV, 25mV, 50mV and 200mV. The hysteresis is selectable if the internal VREF macro-cell or an external VREF input is used.

- **0mV**: will disable the input signal hysteresis.
- **25mV**: is a +12.5mV and -12.5mV hysteresis. For VREF = 1V, the trigger points will be 1.0125V and 0.9875V.
- **50mV**: is a +25mV and -25mV hysteresis. For VREF = 1V, the trigger points will be 1.025V and 0.975V.
- **200mV**: is a +100mV and -100mV hysteresis. For VREF = 1V, the trigger points will be 1.1V and 0.9V.

If hysteresis is desired, ensure the hysteresis is less than the VREF, otherwise the negative trigger point will be pushed below device ground which may stress the device beyond the Recommended Operating Conditions and reduce the lifetime of the device.

Low bandwidth: The ACMP cell has a selection for the bandwidth of the input signal, which can be used to save power and reduce noise impact when lower bandwidth signals are being compared.

If V_{CC}/3 and V_{CC}/4 are not used at ACMP negative input, they can be disabled to reduce power consumption.

7.3.8 Voltage Reference (VREF)

The voltage reference (VREF) produces a fixed (constant) voltage, providing references to the analog comparators and external circuitry. The TPLD1201-Q1 has a voltage reference macro-cell to provide references to the two analog comparators. This macro-cell can supply a user selection of fixed voltage references, /2, /3 and /4 reference off of the V_{CC} power supply to the device, and externally supplied voltage references from the VREF Analog Input (shared with IO4). The macro-cell also has the option to output a reference voltage on the VREF Analog Output (shared with IO7).

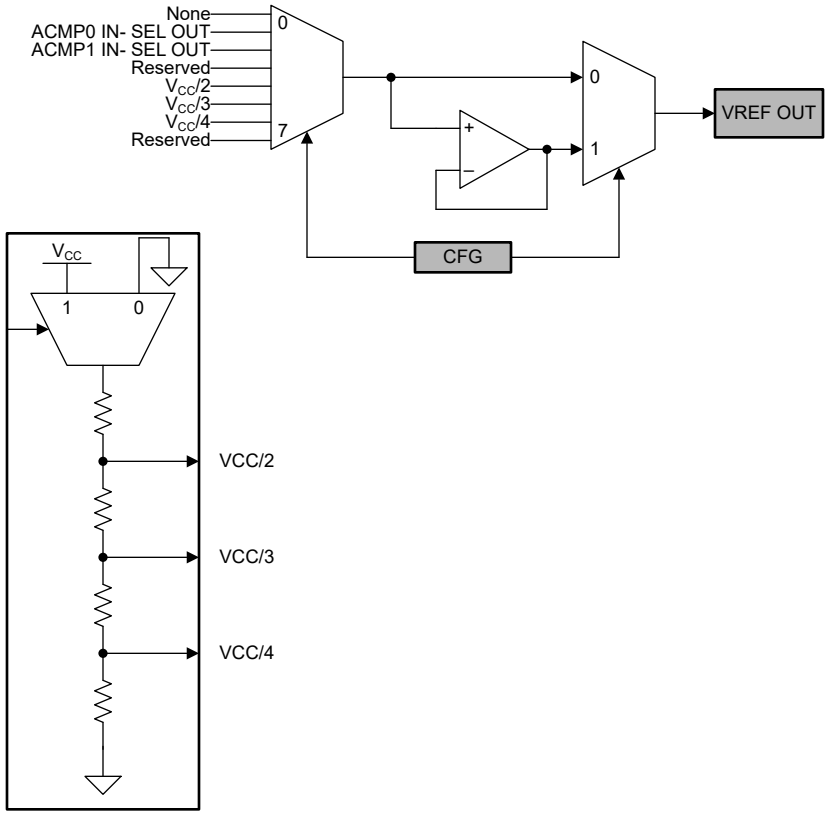


Figure 7-21. Voltage Reference Block Diagram

If V_{CC}/2, V_{CC}/3, and V_{CC}/4 are not used at VREF select, they can be disabled to reduce power consumption.

Force bandgap on keeps the bandgap on while the chip is powered.

Output active buffer parameter enables the active output buffer on VREF.

Table 7-16. VREF Range

V_{CC}	VREF Range
1.71V - 5.5V	150mV - 1.2V

7.4 Device Functional Modes

7.4.1 Power-On Reset

The TPLD1201-Q1 has a power-on reset (POR) macro-cell that provides correct device initialization and operation of all macro-cells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{CC} power is first ramping to the device, and also while the V_{CC} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macro-cells inside the device, and finally to the state of the I/O pins.

The power-on Reset (POR) macro-cell will produce a logic High signal as an output when the device power supply (V_{CC}) rises to approximately V_{PORR} and device completely starts up. All outputs are in high impedance state and chip starts loading data from OTP. The reset signal is released for internal macro-cells and all the registers are initialized to their default states. Figure 7-22 shows POR system generates a sequence of signals that enable certain macro-cells.

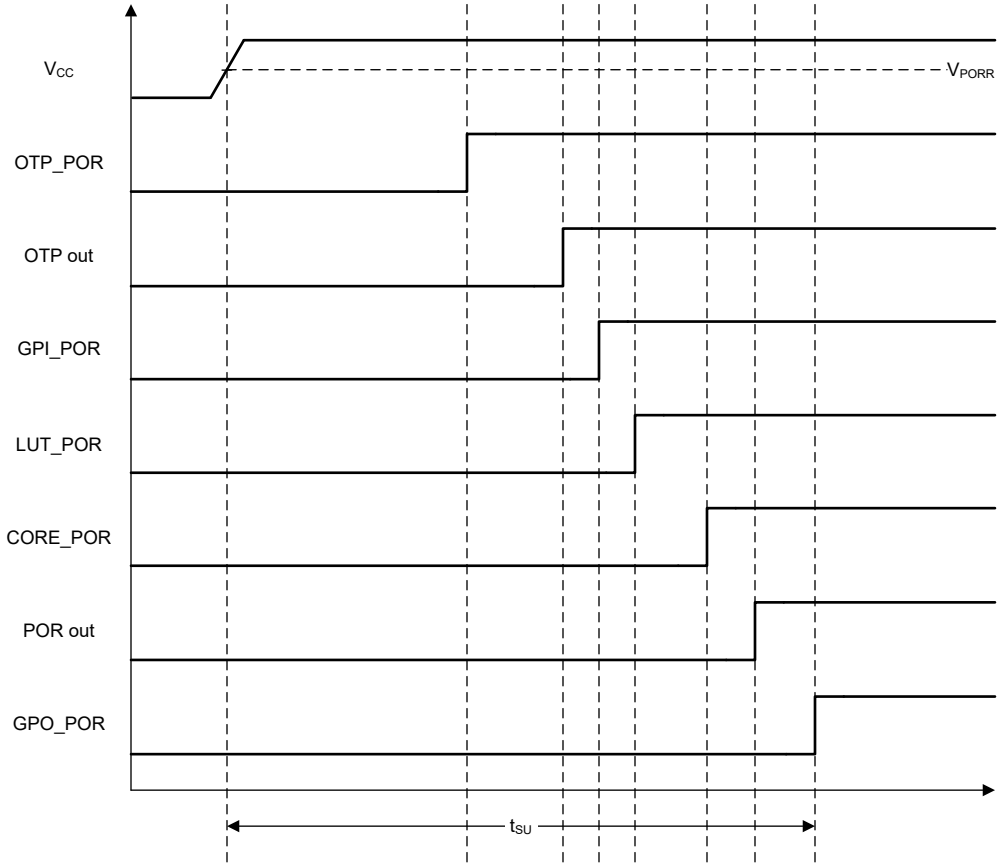


Figure 7-22. POR Sequence

As shown in Figure 7-22, after the V_{CC} has start ramping up and crosses the V_{PORR} threshold:

- First, the on-chip OTP memory is reset.
- Next, the device reads the data from OTP memory, and transfers this information to configure each macro-cell and the connection mux.
- The third stage resets the GPIOs that are configured as inputs and then enables them.
- After that, the LUTs are reset and become active. After LUTs, the delay cells, OSC, DFFs, latches and pipe delay are initialized.
- After all macro-cells are initialized, the internal POR signal generated by the POR macro-cell goes from low to high.
- The last portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point.

Delay blocks will pass their inputs through to the output during the startup sequence without delaying the signal per the configuration, so a LUT added in front of the input of a DLY that ANDs the DLY input with POR will cause the input signal to not appear until the device has fully powered up.

GPIO quick charge: There is an option to connect a 2kΩ resistor in parallel to any configured pull up/pull down resistors to help inputs get to the right voltage faster, especially if there is significant capacitance. The 10kΩ, 100kΩ and 1MΩ GPIO pull up/pull down resistors are not enabled until the POR sequence is completed.

Initialization: All internal macro-cells are initialized to a low level by default. Starting from when V_{CC} exceeds V_{PORR}, macro-cells in the TPLD1201-Q1 are powered on and forced into a reset state.

The VREF output pin driving signal can precede POR output signal going high by 3µs to 5µs. The POR signal going high indicates the mentioned power-up sequence is complete.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The configurable logic and timing blocks of TPLD1201-Q1 allow for the device to provide symmetric power-up and power-down signals for numerous components. In this application the device is configured to output the maximum amount of power- up and power-down sequencing signals based on a counter/delay macro-cell.

8.2 Typical Application

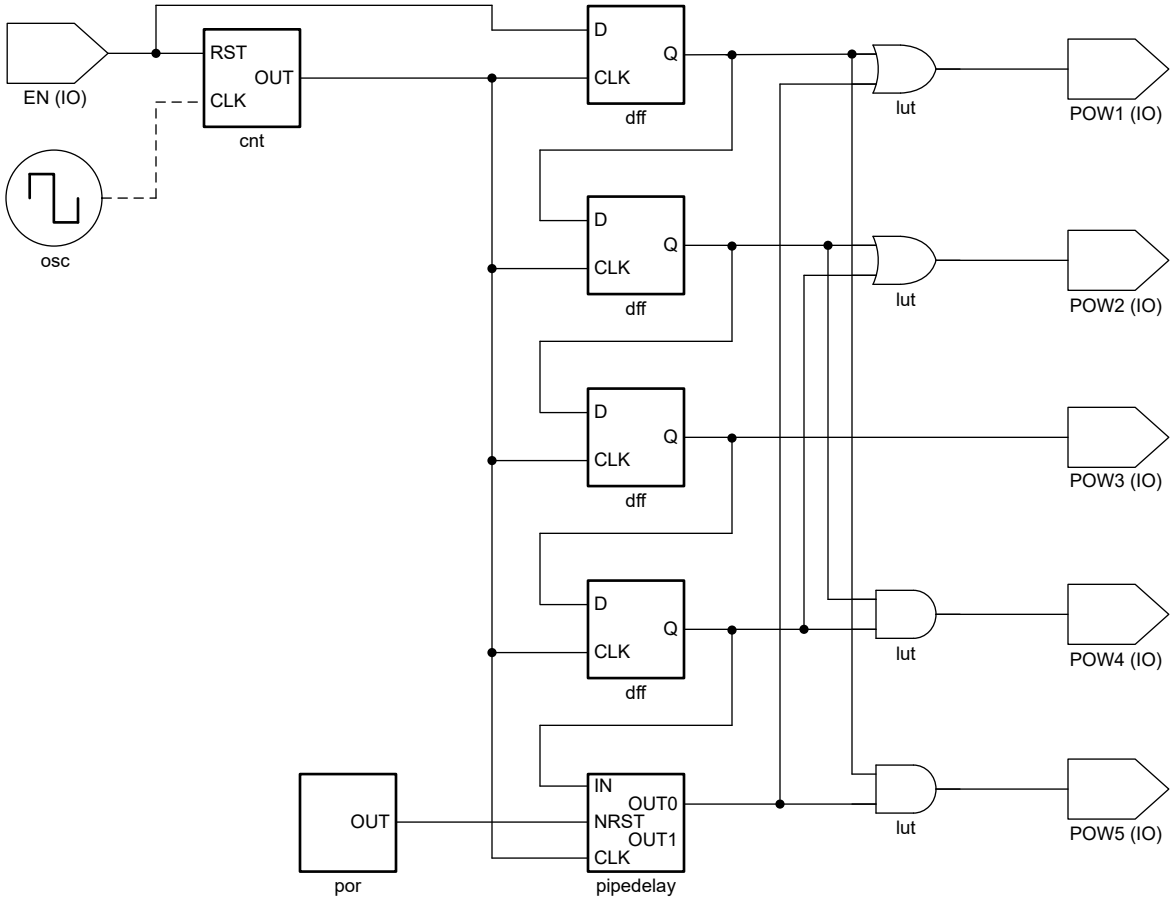


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the TPLD1201-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the TPLD1201-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The TPLD1201-Q1 can drive a load with a total capacitance less than or equal to 15pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 15pF.

The TPLD1201-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} andV_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ or $V_{t-(min)}$ to be considered a logic LOW, and $V_{IH(min)}$ or $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the TPLD1201-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The TPLD1201-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

The TPLD1201-Q1 can be used with no signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*.The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the TPLD1201-Q1 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Application Curves

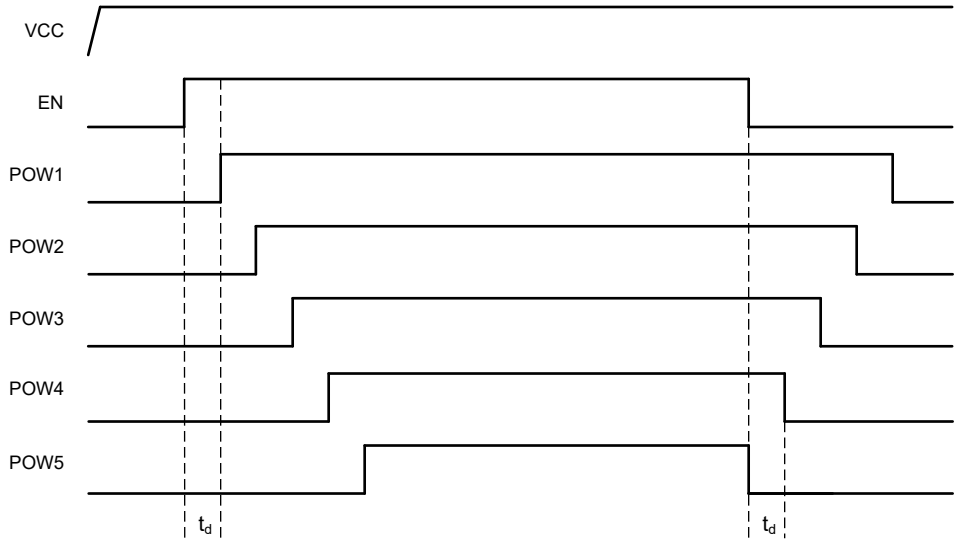


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Section 5.3*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

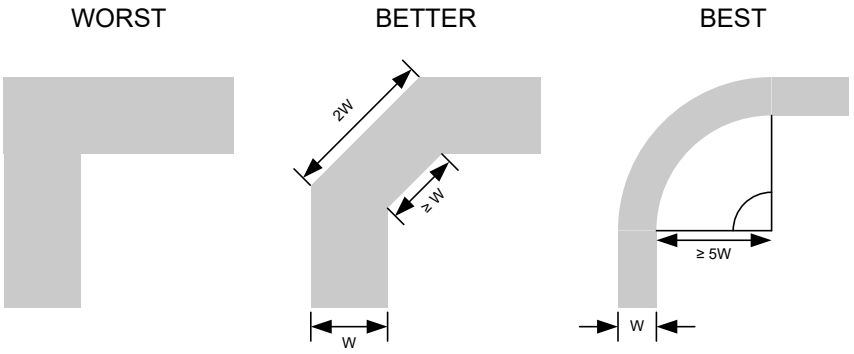


Figure 8-3. Example trace corners for improved signal integrity

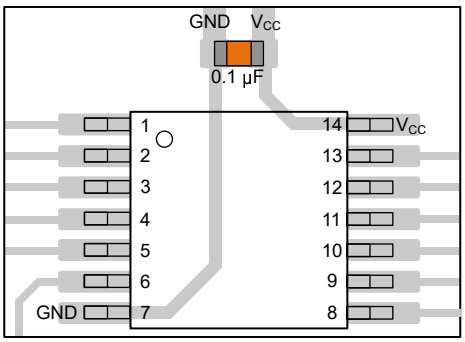


Figure 8-4. Example bypass capacitor placement for TSSOP and similar packages

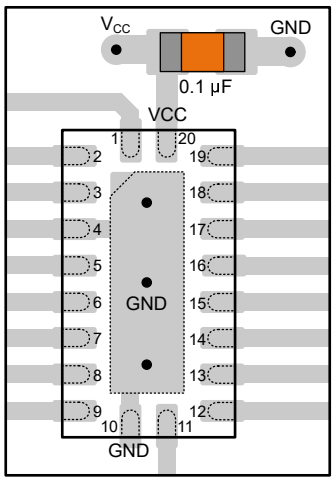


Figure 8-5. Example bypass capacitor placement for WQFN and similar packages

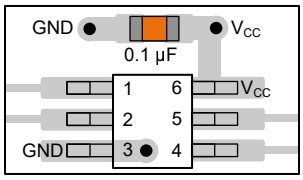


Figure 8-6. Example bypass capacitor placement for SOT, SC70 and similar packages

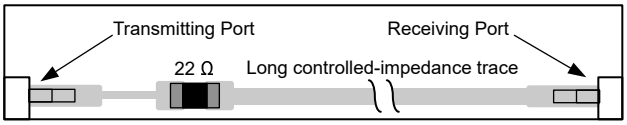


Figure 8-7. Example damping resistor placement for improved signal integrity

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2024) to Revision A (April 2025)	Page
• Changed marketing status from Advance Information to Production data	1
• Added additional detail describing the Programmable Logic IC	16

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPLD1201DGSRQ1	Active	Preproduction	VSSOP (DGS) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPLD1201DGSRQ1.A	Active	Preproduction	null (null) |	3000 | LARGE T&R	-	Call TI	Call TI	See PTPLD1201DGSRQ1	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPLD1201-Q1 :

- Catalog : TPLD1201

NOTE: Qualified Version Definitions:

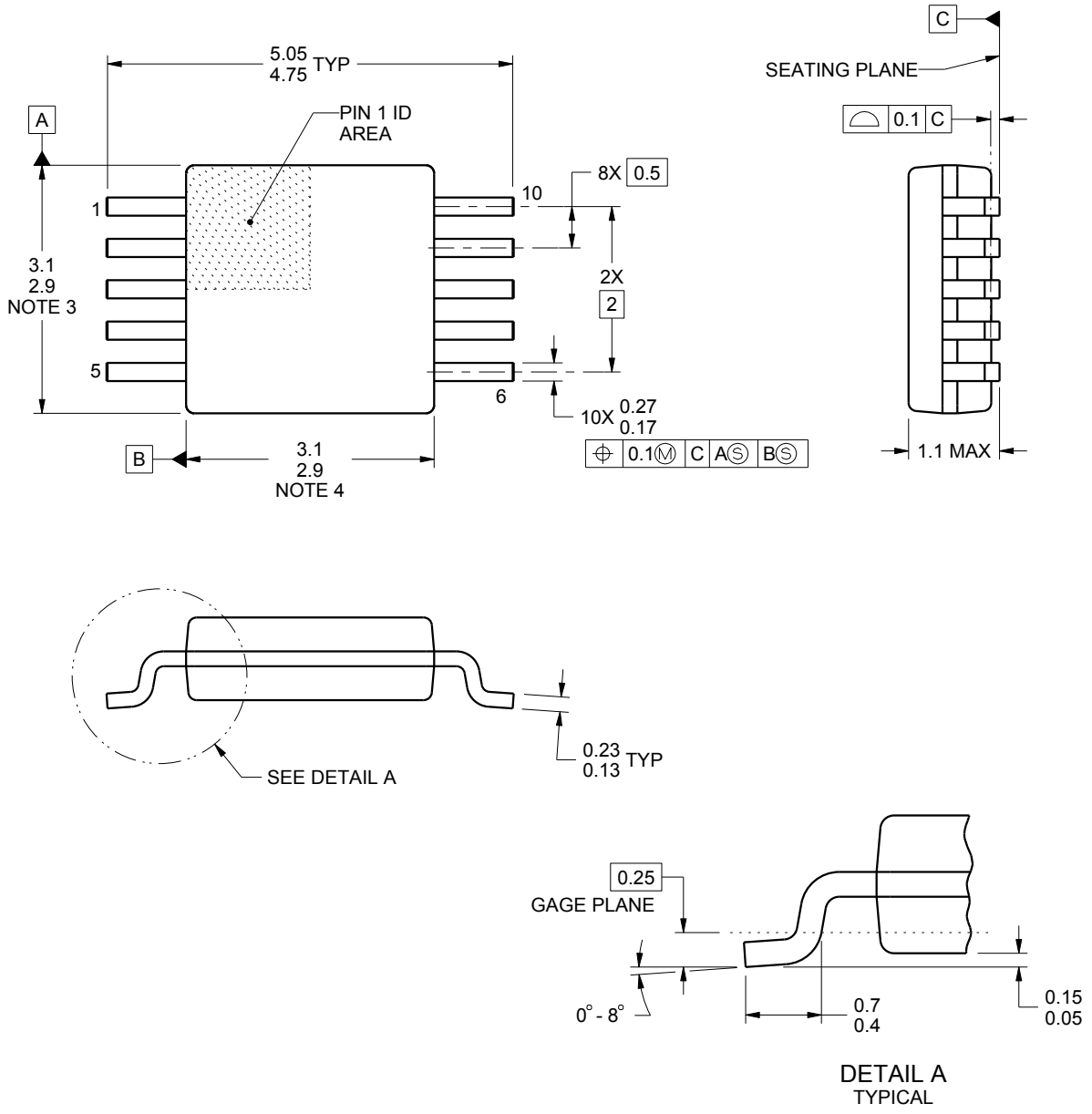
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DGS0010A

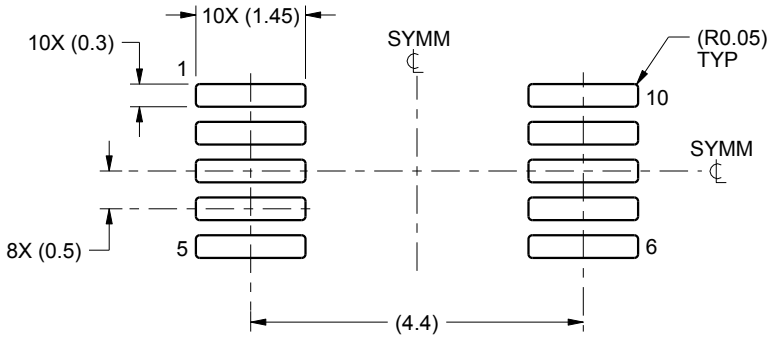
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

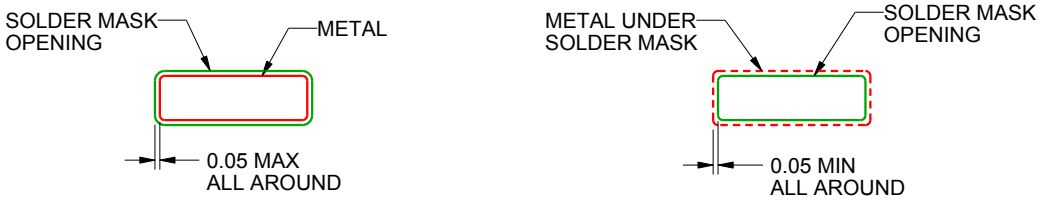


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

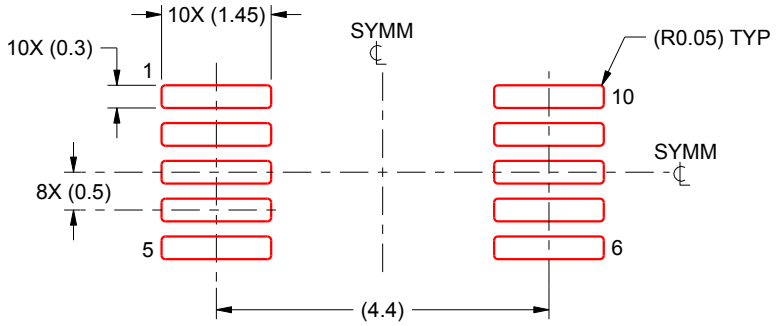


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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